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Analysis and Design of a Sub-THz Ultra-Wideband Phased-Array Transmitter

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Abstract

This thesis investigates circuits and systems for broadband high data-rate transmitter systems in the millimeter-wave (mm-wave) spectrum. During the course of this dissertation, the design process and characterization of a power efficient and wideband binary phase-shift keying (BPSK) transmitter integrated circuit (IC) with local oscillator (LO) frequency multiplication and 360° phase control for beam steering is studied.
All required circuit blocks are designed based on the theoretical analysis of the underlying principles, optimized, fabricated and characterized in the research laboratory targeting low power consumption, high efficiency and broadband operation.
The phase-controlled push-push (PCPP) architecture enabling frequency multiplication by four in a single stage is analytically studied and characterized finding an optimum between output power and second harmonic suppression depending on the input amplitude. A PCPP based LO chain is designed. A circuit is fabricated establishing the feasibility of this architecture for operation at more than 200 GHz. Building on this, a second circuit is designed, which produces among the highest saturated output powers at 2 dBm. At less than 100 mW of direct current (DC) power consumption, this results in a power-added efficiency (PAE) of 1.6 % improving the state of the art by almost 30 %.
Phase-delayed and time-delayed approaches to beam steering are analyzed, identifying and discussing design challenges like area consumption, signal attenuation and beam squint. A 60 GHz active vector-sum phase-shifter with high gain of 11.3 dB and output power of 5 dBm, improving the PAE of the state of the art by a factor of 30 achieving 6.29 %, is designed. The high gain is possible due to an optimization of the orthogonal signal creation stage enabled by studying and comparing different architectures leading to a trade off of lower signal attenuation for higher area consumption in the chosen electromagnetic coupler. By combining this with a frequency quadrupler, a phase steering enabled LO chain for operation at 220 GHz is created and characterized, confirming the preceding analysis of the phase-frequency relation during multiplication. It achieves a power gain of 21 dB, outperforming comparable designs by 25 dB. This allows the combination of phase

control, frequency multiplication and pre-amplification. The radio frequency (RF) efficiency is increased 40-fold to 0.99 %, with a total power consumption of 105 mW.

Motivated by the distorting effect of beam squint in phase-delayed broadband array systems, a novel analog hybrid beam steering architecture is devised, combining phase-delayed and time-delayed steering with the goal of reducing the beam squint of phase-delayed systems and large area consumption of time-delayed circuits. An analytical design procedure is presented leading to the research finding of a beam squint reduction potential of more than 83 % in an ideal system. Here, the increase in area consumption is outweighed by the reduction in beam squint. An IC with a low power consumption of 4.3 mW has been fabricated and characterized featuring the first time delay circuit operating at above 200 GHz. By producing most of the beam direction by means of time delay the beam squinting can be reduced by more than 75 % in measurements while the subsequent phase shifter ensures continuous beam direction control. Together, the required silicon area can be reduced to 43 % compared to time-delayed systems in the same frequency range.

Based on studies of the optimum signal feeding and input matching of a Gilbert cell, an ultra-wideband, low-power mixer was designed. A bandwidth of more than 100 GHz was achieved exceeding the state of the art by 23 %. With a conversion gain of –13 dB, this enables datarates of more than 100 Gbps in BPSK operation.

The findings are consolidated in an integrated transmitter operating around 246 GHz doubling the highest published measured datarates of transmitters with LO chain and power amplifier in BPSK operation to 56 Gbps. The resulting transmitter efficiency of 7.4 pJ/bit improves the state of the art by 70 % and 50 % over BPSK and quadrature phase-shift keying (QPSK) systems, respectively.

Together, the results of this work form the basis for low-power and efficient next-generation wireless applications operating at many times the datarates available today.

Zusammenfassung

Diese Dissertation untersucht Schaltungen und Systeme für breitbandige Transmittersysteme mit hoher Datenrate im Millimeterwellen (mm-wave) Spektrum. Im Rahmen dieser Arbeit werden der Entwurfsprozess und die Charakterisierung eines leistungseffizienten und breitbandigen integrierten Senders basierend auf binärer Phasenumtastung (BPSK) mit Frequenzvervielfachung des Lokaloszillatorsignals und 360°-Phasenkontrolle zur Strahlsteuerung untersucht. Alle erforderlichen Schaltungsblöcke werden auf Grundlage von theoretischen Analysen der zugrundeliegenden Prinzipien entworfen, optimiert, hergestellt und im Forschungslabor charakterisiert, mit den Zielen einer niedrigen Leistungsaufnahme, eines hohen Wirkungsgrades und einer möglichst großen Bandbreite.
Die phasengesteuerte Push-Push (PCPP)-Architektur, welche eine Frequenzvervierfachung in einer einzigen Stufe ermöglicht, wird analytisch untersucht und charakterisiert. Dabei wird ein Optimum zwischen Ausgangsleistung und Unterdrückung der zweiten Harmonischen des Eingangssignals in Abhängigkeit von der Eingangsamplitude gefunden. Es wird eine LO-Kette auf PCPP-Basis entworfen. Eine Schaltung wird präsentiert, die die Machbarkeit dieser Architektur für den Betrieb bei mehr als 200 GHz nachweist. Darauf aufbauend wird eine zweite Schaltung entworfen, die mit 2 dBm eine der höchsten publizierten gesättigten Ausgangsleistungen erzeugt. Mit einer Leistungsaufnahme von weniger als 100 mW ergibt sich ein Leistungswirkungsgrad (PAE) von 1.6 %, was den Stand der Technik um fast 30 % verbessert.
Es werden phasenverzögerte und zeitverzögerte Ansätze zur Steuerung der Strahlrichtung analysiert, wobei Entwicklungsherausforderungen wie Flächenverbrauch, Signaldämpfung und Strahlschielen identifiziert und diskutiert werden. Ein aktiver Vektorsummen-Phasenschieber mit hoher Verstärkung von 11.3 dB und einer Ausgangsleistung von 5 dBm, der mit einer PAE von 6.29 % den Stand der Technik um den Faktor 30 verbessert, wird entworfen. Die hohe Verstärkung ist zum Teil auf eine Optimierung der orthogonalen Signalerzeugungsstufe zurückzuführen, die durch die Untersuchung und den Vergleich verschiedener Architekturen ermöglicht wird. Bei der Entscheidung für einen elektromagnetischen Koppler rechtfertigt die geringere

Signaldämpfung einen höheren Flächenverbrauch. Durch die Kombination mit einem Frequenzvervierfacher wird eine LO-Kette mit Phasensteuerung für den Betrieb bei 220 GHz geschaffen und charakterisiert, was die vorangegangene Analyse der Phasen-Frequenz-Beziehung während der Multiplikation bestätigt. Sie erreicht einen Leistungsgewinn von 21 dB und übertrifft damit vergleichbare Designs um 25 dB. Dies ermöglicht die Kombination von Phasensteuerung, Frequenzvervielfachung und Vorverstärkung. Der Hochfrequenz-Wirkungsgrad wird um das 40-fache auf 0.99 % bei einer Gesamtleistungsaufnahme von 105 mW gesteigert.
Motiviert durch den verzerrenden Effekt des Strahlenschielens in phasengesteuerten Breitbandarraysystemen, wird eine neuartige analoge hybride Strahlsteuerungsarchitektur untersucht, die phasenverzögerte und zeitverzögerte Steuerung kombiniert. Damit wird sowohl das Strahlenschielen phasenverzögerter Systeme als auch der große Flächenverbrauch zeitverzögerter Schaltungen reduziert. Es wird ein analytisches Entwurfsverfahren vorgestellt, das zu dem Forschungsergebnis führt, dass in einem idealen System ein Potenzial zur Reduktion des Strahlenschielens von mehr als 83 % besteht. Dabei wird die Zunahme des Flächenverbrauchs durch die Verringerung des Strahlenschielens aufgewogen. Es wird ein IC mit einer geringen Leistungsaufnahme von 4.3 mW hergestellt und charakterisiert. Dabei wird die erste Zeitverzögerungsschaltung entworfen, die bei über 200 GHz arbeitet. Durch die Erzeugung eines Großteils der Strahlrichtung mittels Zeitverzögerung kann das Schielen des Strahls bei Messungen um mehr als 75 % reduziert werden, während der nachfolgende Phasenschieber eine kontinuierliche Steuerung der Strahlrichtung gewährleistet. Insgesamt kann die benötigte Siliziumfläche im Vergleich zu zeitverzögerten Systemen im gleichen Frequenzbereich auf 43 % reduziert werden.
Auf der Grundlage von Studien zur optimalen Signaleinspeisung und Eingangsanpassung einer Gilbert-Zelle wird ein Ultrabreitband-Mischer mit geringem Stromverbrauch entworfen. Dieser erreicht eine Ausgangsbandbreite von mehr als 100 GHz, die den Stand der Technik um 23 % übertrifft. Bei einer Wandlungsverstärkung von –13 dB ermöglicht dies Datenraten von mehr als 100 Gbps im BPSK-Betrieb.
Die Erkenntnisse werden in einem integrierten, breitbandigen Sender konsolidiert, der um 246 GHz arbeitet und die höchsten veröffentlichten

gemessenen Datenraten für Sender mit LO-Signalkette und Leistungsverstärker im BPSK-Betrieb auf 56 Gbps verdoppelt. Die daraus resultierende Transmitter-Effizienz von 7.4 pJ/bit verbessert den Stand der Technik um 70 % bzw. 50 % gegenüber BPSK- und Quadratur-Phasenumtastung (QPSK)-Systemen.
Zusammen bilden die Ergebnisse dieser Arbeit die Grundlage für stromsparende, effiziente, mobile Funkanwendungen der nächsten Generation mit einem Vielfachen der heute verfügbaren Datenraten.

Statement of authorship

I hereby certify that I have authored this document entitled *Analysis and Design of a Sub-THz Ultra-Wideband Phased-Array Transmitter* independently and without undue assistance from third parties. No other than the resources and references indicated in this document have been used. I have marked both literal and accordingly adopted quotations as such. There were no additional persons involved in the intellectual preparation of the present document. I am aware that violations of this declaration may lead to subsequent withdrawal of the academic degree.

Dresden, 17th January 2023

Luca Steinweg

Contents

List of Symbols

Symbol	Unit	Description
$A(j\omega)$	—	System gain factor of a control system
$\underline{a}_i$	$\sqrt{W}$	Complex wave flowing into of a measured port i
α	dB/m	Attenuation constant of the propagation constant γ
$\underline{b}_i$	$\sqrt{W}$	Complex wave flowing out of a measured port i
β	rad/m	Phase constant of the propagation constant γ
BR	bit/s	Bit rate
BW	Hz	Bandwidth
BW_{rel}	—	Relative bandwidth
C	F	Capacitance
c	m/s	Speed of light: $c = 299\,792\,458\,\mathrm{m\,s^{-1}}$
C'	F/m	Shunt capacitance of a transmission line per unit-length
$C_{BC,ext}$	F	Extrinsic base-collector capacitance
$C_{BC,int}$	F	Intrinsic base-collector capacitance
C_{BC}	F	Base-collector capacitance
$C_{BE,int}$	F	Intrinsic base-emitter capacitance
C_{BE}	F	Base-emitter capacitance
C_{ch}	bits/s	Channel capacity
$C_{j,int}$	F	Internal depletion capacitance
d	m	Distance between two neighboring antennas in an antenna array
d_{max}	m	Maximum allowable distance between antenna elements for given constraints
d_{min}	$\sqrt{J}$	Minimal vectorial distance between two symbols in a modulation scheme
e	C	Charge of an electron: $e = 1.602 \times 10^{-19}$ C
ε	F/m	Electrical permittivity

Continued on next page

Symbol	Unit	Description
ε_r	—	Relative electrical permittivity
$\bar{\varepsilon}_b$	J	Mean energy per bit
η_{DC}	—	DC-efficiency
η_{RF}	—	RF-efficiency
η_{tot}	—	Total efficiency
f	Hz	Frequency
f_c	Hz	Frequency at the center of the analyzed band
f_{max}	Hz	Maximum frequency of oscillation
$f_{T,int}$	Hz	Intrinsic transit frequency
f_T	Hz	Transit frequency
G	dB	Power gain
G	S	Conductance
G'	S/m	Shunt conductance of a transmission line per unit-length
g_m	S	Transistor transconductance
G_r	dB	Receiver antenna gain
G_t	dB	Transmitter antenna gain
$\underline{\gamma}$	—	Complex propagation constant: $\underline{\gamma} = \alpha + j\beta$
$\underline{H}(j\omega)$	—	System transfer function of a control system
$\underline{h}_{21}$	—	Current gain
I	A	Current flowing into the input of a transmission line
I_c	A	Collector current of a bipolar transistor
I_{in}	A	Current flowing into the input of a transistor
I_{inj}	A	Injected current
I_{out}	A	Current flowing into the output of a transistor
I_s	A	Saturation current of a bipolar transistor
j	—	Imaginary unit
k_b	J/K	Boltzmann constant: $k_b \approx 1.381 \times 10^{-23}\,\mathrm{J\,K^{-1}}$
L	H	Inductance
l	m	Length of a specific transmission line
L'	H/m	Series inductance of a transmission line per unit-length
Δl	m	Difference in length between neighboring antenna paths in an antenna array
l_{TL}	m	Length of a specific transmission line
l'_{TL}	m	Infinitesimally small transmission line length
λ	m	Wavelength
λ'	m	Effective wavelength of a signal propagating over a transmission line
λ_c	m	Wavelength at the center frequency
m	—	Number of bits per symbol
M	—	Modulation order of a given modulation scheme

Continued on next page

Symbol	Unit	Description
μ	H/m	Magnetic permeability
N	—	Frequency multiplication factor
N_{arr}	—	Number of elements in an antenna array
N_{x}	—	Transistor unit size multiplication factor
ω	rad	Circular frequency
$\Delta\omega_{3\,\mathrm{dB}}$	rad	3-dB-bandwidth
ω_{c}	rad	Center frequency
ω_{L}	rad	Locking range of an injection locked oscillator
ω_{osc}	rad	Intrinsic oscillation frequency of a resonator
P_r	dBm	Received Power
P_t	dBm	Transmitted Power
φ	°	Phase in degrees
$\Delta\varphi$	°	Difference in phase between two paths
$\Delta\varphi_{\mathrm{c}}$	±°	Maximum allowable phase shift of the phase-shifter in a hybrid beam steering system to limit the maximum beam squint to $\Delta\theta_{\mathrm{max}}$
φ_{noise}	°	Phase noise
Q	—	Quality factor of a resonator
r	m	Radius: Usually used as a distance from a point source to a target
R	Ω	Resistance
R'	Ω/m	Series resistance of a transmission line per unit-length
$R_{\mathrm{B,ext}}$	Ω	External base resistance
$R_{\mathrm{B,int}}$	Ω	Intrinsic base resistance
r_{be}	Ω	Base-emitter resistance
s	m	Length of the transmission channel of an antenna array
S/N	—	Signal-to-Noise Ratio
$\underline{S}_{\mathrm{x,y}}$	—	Scattering parameters from port y to x
SR	Bd	Symbolrate, also: Baudrate
T	s	Time period of a periodic signal
t	s	Time
τ	s	Time delay of a transmission line
$\Delta\tau$	s	Difference in time delay between two paths
θ	°	Direction to which the main lobe of an antenna array is steered
θ_{c}	°	Direction to which the center frequency component in an observed spectrum is steered by an antenna array

Continued on next page

Symbol	Unit	Description
θ_{max}	°	Maximum beam direction allowed by given constraints
$\Delta\theta_{\text{max}}$	°	Maximum allowable beam squint in a hybrid beam steering system
θ_{obs}	°	Direction from which the propagation pattern of an antenna array is observed
θ_{phase}	°	Beam direction of a phase-delayed antenna array
$\theta_{\text{phase,max}}$	°	Maximum beam direction contribution of the phase-shifter in a hybrid beam steering system
θ_{TTD}	°	Beam direction of a time-delayed antenna array
$\theta_{\text{TTD,max}}$	°	Maximum beam direction contribution of the time-delay stage in a hybrid beam steering system
V	V	Voltage at the input of a transmission line
$\widehat{V}$	V	Voltage amplitude of a sinusoidal signal
v_{p}	m/s	Phase velocity: $v_{\text{p}} = \lambda/T$
V_{T}	V	Thermal voltage: $V_{\text{T}} = \frac{k_{\text{b}}T}{e}$
V_{Y}	V	Early-effect voltage
w	m	Width of the squinted beam at a certain distance s
x'	—	Number of elements in an antenna array in x-direction
y'	—	Number of elements in an antenna array in y-direction
z	m	Coordinate in the direction of the propagation along a transmission line
$\underline{Z}$	Ω	Complex impedance
$\underline{Z}_{\text{L}}$	Ω	Load impedance
Z_0	Ω	Characteristic impedance of a transmission line
ζ	K	Temperature

End of table

Acronyms

f_{max}	maximum frequency of oscillation
f_T	transit frequency
1G	First Generation Systems
5G	Fifth Generation Systems
6G	Sixth Generation Systems
ADC	analog-to-digital converter
ASK	amplitude shift keying
AWGN	additive white gaussian noise
BB	baseband
BER	bit error rate
BiCMOS	bipolar CMOS
BJT	bipolar junction transistor
BPSK	binary phase-shift keying
CB-CPW	conductor-backed coplanar waveguide
CDMA	code division multiple access
CMOS	complementary metal-oxide-semiconductor
CPW	coplanar waveguide
DAC	digital-to-analog converter
DC	direct current
DHBT	double heterojunction bipolar transistor
DSP	digital signal processor
DUT	device under test
EM	electromagnetic
ENOB	effective number of bits
ERP	effective radiated power
EVM	error vector magnitude

FD	full-dimension
FDMA	frequency division multiple access
FEM	finite element method
FSA	frequency spectrum analyzer
FSPL	free space path loss
GaAs	Gallium Arsenide
GaN	Gallium Nitride
Gbps	giga bit per second
GCPW	grounded coplanar waveguide
GSG	ground-signal-ground
GSSG	ground-signal-signal-ground
HBT	heterojunction bipolar transistor
IC	integrated circuit
IF	intermediate frequency
ILO	injection-locked oscillator
InP	Indium Phosphide
InP	Indium Phosphide
IoT	Internet of Things
LO	local oscillator
M2M	Machine-to-Machine
MAG	maximum available power gain
MIM	metal-insulator-metal
MIMO	multiple-input multiple-output
mm-wave	millimeter-wave
MOM	metal-oxide-metal
MOS	metal-oxide-semiconductor
PA	power amplifier
PAE	power-added efficiency
PAM	pulse amplitude modulation
PAPR	peak-to-average power ratio
PCB	printed circuit board
PCPP	phase-controlled push-push
PDK	process design kit
PLL	phase-locked loop
PMOS	p-type metal-oxide
PP	push-push
PRBS	pseudorandom binary sequence
PSD	power-spectral-density
PSK	phase-shift keying

QAM	quadrature amplitude modulation
QPSK	quadrature phase-shift keying
RF	radio frequency
RMS	root mean square
RTO	real-time oscilloscope
SDMA	space division multiple access
Si	Silicon
SiC	Silicon Carbide
SiGe	Silicon Germanium
SNR	signal-to-noise ratio
SOC	system on chip
SPDT	single-pole double-throw
TEM	transverse electromagnetic mode
TTD	true time delay
VCO	voltage-controlled oscillator
VGA	variable gain amplifier
VNA	vector-network analyzer
WLAN	Wireless Local Area Network

Prior Publications

This dissertation contains results previously published in the form of journal articles [Ste1]–[Ste4] and conference papers [Ste5]–[Ste8]. References to the respective previous publications are given at the beginning of the subchapters. Some figures and tables are already included in the previous publications and were, in some cases, merely adapted and supplemented for this work. In such cases, the original publication is referenced in the figure caption. The previous publications are also listed separately at the beginning of the bibliography. For an overview of further scientific publications, co-authorships are also listed there [9]–[13].

1. Introduction

1.1. Motivation

Powerful communication networks are the backbone of today's globally connected world. Many technological trends, such as the digitization of private life, connecting families and friends around the world, and professional life, with applications like Industry 4.0 and the Internet of Things (IoT), which require a high level of automation and Machine-to-Machine (M2M) communication, as well as Sixth Generation Systems (6G) for mobile networks depend heavily on reliable and fast data transmissions. Current trends show that more and more devices connect to the Internet on a daily basis. It is estimated that 66 % of the world's population will have Internet access, resulting in nearly 30 billion network devices, by 2023, of which about one-third will be M2M connections [14]. The developments described above create a need for specialized networks to satisfy a variety of requirements. On the one hand, large Internet hubs around the world need to be connected by transoceanic cables whose throughput capacity cannot be high enough. On the other hand, novel applications such as IoT, Edge Computing [15] and self-driving cars [16], [17] require very high mobility, low latency and high transmission speed. Finally, the expected 5.7 billion mobile subscribers require reliable and fast service while maximizing battery life by optimizing the energy efficiency of the electronic end-user devices. Low energy consumption is also crucial from a sustainability perspective, as communication systems are increasingly contributing to global carbon emissions [18], [19].
With growing compute power and distribution of mobile devices, current communication technologies become insufficient. As a solution,

mm-wave systems, enabled by recent technological developments, are particularly promising for next-generation mobile applications:
With typical antenna types scaling with wavelength and frequencies as high as 300 GHz, the dimensions of the corresponding antennas decrease significantly [20]. For example, a dipole of length $\lambda/2$ only measures about 611 µm in length at 245 GHz in free air and becomes even smaller on silicon substrates with relative permitivities of $\varepsilon_r = 3 \ldots 4.5$. This enables the integration of the antennas directly on-chip, reducing assembly complexity and overall system cost. In addition, antenna arrays with many elements become feasible while keeping the overall system size below a few centimeters of edge length. Such array arrangements can contribute to reduce interfering signals and combine transmitter power or receiver gain in a static or dynamic manner. Another significant advantage of the mm-wave spectrum is the very large possible channel bandwidth both from a technological and from a regulatory point of view [21]. Large absolute bandwidths, and thus data-rates, can be achieved. Due to the high center frequencies, relative bandwidths, which generally limit passive and active circuits, maintain moderate values. With a high free space path loss (FSPL) and atmospheric absorption [22]–[24], interference between different applications is reduced. Thus, even many indoor networks are unlikely to interfere with each other, enabling each user to occupy a large amount of spectral bandwidth and maximize the personal data transmission speed.
With current technologies, there exist some severe challenges:
First, any semiconducting technology is limited in its applicable frequency band by the speeds achievable by its active components. In particular, the gain of transistors, independent of the specific type, decreases with rising frequencies due to rising parasitic influences. This makes it increasingly difficult to design functional and efficient circuits. Very high frequencies and/or signals with very high bandwidths that approach the transit frequency (f_T) of the chosen technology can result in the signals to be attenuated in some stages. Considerable effort is then required to produce high output powers that allow usable transmission ranges. This usually comes at the expense of chip area and DC power consumption. Novel circuits that provide energy-efficient solutions with low area consumption are therefore inevitably the focus of efforts to design mm-wave systems for mobile devices. In addition, the effects of small parasitics in the passive components – such

as resistors, inductors and capacitors, but also transmission lines and via stacks – are amplified at higher frequencies, resulting in additional signal attenuation on the chip and thus lower efficiency. This poses a major challenge to the design process and increases the cost of technologies that can reach these frequencies.
Second, the attenuation in the transmission channel must be analyzed in detail, as it is a major contributor to the power budget of a mm-wave transceiver system. The Friis transmission equation

$$\frac{P_r}{P_t} = \left(\frac{\lambda}{4\pi r}\right)^2 G_t G_r, \tag{1.1}$$

with the gain values of transmitting antenna G_t and receiving antenna G_r, describes the FSPL increasing with rising frequencies of the transmitted signals and the distance r between transmitter and receiver [20]. This results in frequency components at the high end of the mm-wave spectrum experiencing FSPL of approximately 80 dB for the first meter in dry air. In high humidity, fog or even rain, this value can further increase significantly [25]. With 6G standards being discussed for frequencies up to the THz range [26], this will be further exacerbated. Here, a combination of many parallel transmitters or receivers in a dynamic antenna array can be advantageous. Superimposed on the FSPL is the atmospheric absorption with many attenuation maxima at which H_2O or O_2 molecules resonate [25]. This must be taken into account when defining the operating frequency range.
Third, established transceiver systems extend achievable datarates for a given bandwidth by employing complex modulation schemes which encode many bits of data into a single transmitted analog symbol. However, such higher-order modulation schemes require highly linear modulator circuits and elaborate baseband chains which are based on high-speed and high-resolution digital-to-analog converters (DACs) and analog-to-digital converters (ADCs). This results in a significant design challenge, leading to complex designs with high area requirements and high power consumption.
In summary, mm-wave wireless technologies offer many benefits and opportunities for modern applications to satisfy the demand for an

increasing number of mobile subscribers and higher datarates. However, these benefits do not come without challenges that require significant research to enable future mobile networks. This work contributes to that effort by investigating, designing and characterizing novel circuits and transmitter designs extending the available datarates while maintaining a low power consumption to comply with the requirements of mobile devices.

1.2. Objective of this Thesis

This thesis is based on the research carried out within the research project *ADAMIS – Adaptive Millimetre-wave Integrated Transmitters*, which was publicly funded by the *Deutsche Forschungsgemeinschaft (DFG)*.

The objective of this work is to study suitable circuits capable of providing the demanded rising datarates while maintaining low power consumption in mobile devices.
A low-power, high-efficiency, and broadband BPSK transmitter with beam steering capability for datarates up to 50 Gbps will be designed. To this end, novel approaches to the design of LO chains, broadband modulators, and beam steering architectures will be investigated and realized.
Recently, some impressive results were achieved for transmitters [27] and large antenna arrays [28] in BiCMOS technology around 180 GHz. The feasibility of very broadband BPSK modulation was shown in [29] with a stand-alone modulator design. In the 240 GHz band, some more complete transceiver systems achieved up to 30 Gbps with BPSK modulation [30]–[32], using the same technology. Typically, the required DC power is high, resulting in degraded transmitter efficiency per bit. Other works use more complex modulation schemes to achieve datarates greater than 50 Gbps [33], [34].
First, this work aims to improve the state of the art by focusing on low power consumption and power efficiency in each circuit block and, from a systematic point of view, on optimal allocation of the consumed DC power. This is motivated by the use of the designed system in future mobile devices. Novel approaches for mm-wave LO chains are investigated and implemented to optimize power consumption based on the underlying architecture.
Second, a low-order modulation scheme can be advantageous as it allows high-speed and high-resolution DACs to be omitted reducing the power consumption in a transmitter system. With the associated lower number of bits per symbol, the development of design techniques for wideband circuits to maintain very high datarates of up to 50 Gbps is motivated.
Third, to counteract the high FSPL in the mm-wave spectrum, techniques for dynamically steerable antenna arrays are investigated and discussed. A circuit is designed to provide beam steering capabilities

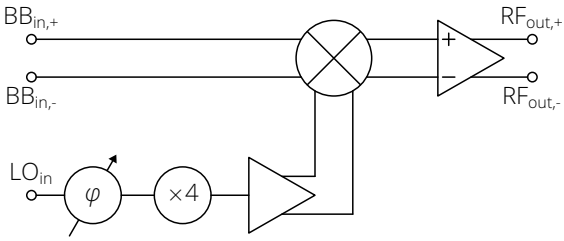


Figure 1.1: Simplified block diagram of a direct modulation BPSK transmitter system consisting of a LO chain, a broadband modulator and a broadband power amplifier and antenna.

in the integrated transmitter. In addition, problems associated with broadband beam steering will be analyzed and an architecture to reduce these effects is designed.

A band of operation ranging from 220 GHz to 270 GHz is chosen as this allows a very high absolute bandwidth, while maintaining a moderate relative bandwidth of 20 %. The frequency range places the channel in between two absorption maxima of atmospheric H_2O at approximately 180 GHz and 315 GHz [25]. This minimizes the atmospheric contribution to sideband distortion. The targeted system architecture is shown in Fig. 1.1. The chain consists of a tunable active phase shifter, operating at 61.5 GHz and responsible for beam steering, in front of a frequency multiplier by a factor of four. The buffered LO signal drives a broadband modulator. The resulting modulated signal is then amplified by a broadband differential power amplifier which is contributed by project partner *Joachim Hebeler* of the *Karlsruhe Institute of Technology (KIT)*. The design is intended to allow flexible and adaptive combination of multiple adjacent transmit paths in a linear antenna array.

To support the findings of the investigations, specialized ICs are designed, fabricated and characterized in the research laboratory.

1.3. Structure of this Thesis

This thesis consists of seven chapters.
In the introduction, the motivation and objectives of this thesis are stated.
Chapter 2 provides an overview of the existing integrated circuit fabrication technologies and materials available for the targeted transmitter. The use of the selected 130 nm SiGe BiCMOS technology is discussed and justified. In addition, a brief overview of digital modulation techniques is provided, motivating the use of the BPSK modulation scheme.
The third chapter deals with LO chains with the possibility of frequency multiplication by a factor of four. Based on the proven push-push architecture, the PCPP architecture is presented. This enables frequency quadrupling in a single conversion stage. Two circuits operating at frequencies higher than 200 GHz are designed and fabricated. While the first IC demonstrates the feasibility of this approach in the targeted frequency band, the second design improves upon this approach and results in a high-efficiency and output power circuit for generating LO signals for mm-wave applications.
Next, various approaches to beam steering are discussed in chapter 4. First, a 90° phase shifter operating at 60 GHz is designed and characterized for use in a phase-steerable LO chain. By combining it with a frequency quadrupling multiplier, the ability to control the phase over the full range at more than 200 GHz is demonstrated. Second, the effect of beam squinting in wideband systems is investigated. To mitigate this problem, a novel hybrid beam steering architecture that combines time-delayed and phase-delayed steering and operates in the 220 to 250 GHz range is presented.
Chapter 5 describes the design of a broadband modulator. This is conceived for BPSK operation, reducing the requirements for digital preprocessing of the transmitted data. By optimizing the proven Gilbert cell architecture, 100 GHz of RF bandwidth is achieved. This enables high data rates even for low-order modulations.
Finally, the circuit blocks were combined in chapter 6 to produce a complete BPSK transmitter with LO beam steering, capable of data rates of up to 56 Gbps. This design can compete with systems that use more complex modulation schemes in terms of data rate, while

reducing power consumption and significantly improving transmitter and RF efficiency.
The results are summarized in the conclusion along with an outlook on possible points of interest for future research.

2. Overview of Employed Technologies and Techniques

Modern communication applications require ever higher data transmission speeds. These are generally enabled by a combination of high-order modulation schemes and the shift towards higher frequency bands in the millimeter-wave (mm-wave) and sub-THz spectra where large absolute bandwidth is available. Satisfying these demands increases the complexity of the selection of appropriate semiconductor materials, production methods and interconnecting techniques. Due to the high frequencies of operation, common approaches like realizing systems on printed circuit boards (PCBs) become unfeasible. Even the interconnections of multiple chips, via bond wire [35] or flip-chip assemblies [36], introduce significant attenuation and mismatch to the signal path. This motivates the consolidation of many circuits into a monolithic system on chip (SOC). Accompanying the reduction of parasitic attenuation, the miniaturization enabled by the integration can reduce the overall cost of the systems.

2.1. Integrated Circuit Technology

Integrated circuit technologies provide both passive and active elements. This section focuses on typical performance characteristics of active devices. These are first introduced using a bipolar junction transistor (BJT) as an example, followed by a presentation of the most relevant integrated circuit technology options for this work.

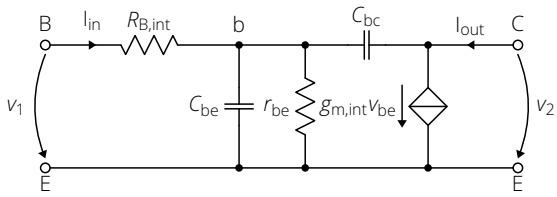


Figure 2.1: Simplified equivalent dynamic internal circuit model of a BJT [37].

2.1.1. Performance Parameter

The analysis of the intrinsic behavior of a BJT for radio frequency (RF) operation is based on the simplified equivalent circuit model, which is given in Fig. 2.1. Most commonly, the transit frequency (f_T) and the maximum frequency of oscillation (f_{max}) are calculated and used to compare different processes and technologies. Both figures can be determined from the small-signal behavior. Thus, there exists a significant influence of the bias point of the transistors on the possible performance, which is, therefore, a high design priority, trading off collector current, power consumption and frequency behavior.
While the influence of parasitics like C_{be} and C_{bc} is small at low frequencies, resulting in high current amplification values, a first order lowpass behavior leads to the reduction of $\underline{h}_{21}(f)$ for higher frequencies. The transit frequency is defined as the frequency where forward current amplification is reduced to one while the output is shorted [38]:

$$\underline{h}_{21}(f)|_{f=f_T} = \left|\frac{\underline{I}_{out}}{\underline{I}_{in}}\right|_{f=f_T,\underline{v}_2=0} = 1. \tag{2.1}$$

Analyzing the intrinsic behavior of a BJT [39], [40],

$$f_{T,int,BJT} = \frac{g_{m,int}}{2\pi(C_{BE,int} + C_{BC,int})} \tag{2.2}$$

illustrates the influence of the parasitic capacitances on the frequency behavior. In an actual integrated circuit, additional parasitics are introduced due to necessary connections of the transistor to the metal planes enabling the interface with the surrounding circuitry. The

characterization of novel device technologies can be challenging due to ever higher f_T in the range of many hundreds of gigahertz [41]. More practically, the current amplification can be calculated via the S-parameters according to [42]

$$\underline{h}_{21}(f) = \frac{-2\underline{S}_{12}(f)}{(1-\underline{S}_{11}(f))(1+\underline{S}_{22}(f)) + \underline{S}_{12}(f)\underline{S}_{21}(f)}, \tag{2.3}$$

with an established vector-network analyzer (VNA) measurement setup. Typically, this is done for some tens of gigahertz until the 3-dB-bandwidth is determined. From there, the actual f_T is extrapolated assuming the aforementioned first order lowpass. However, this introduces uncertainty in the actual value of f_T.
The maximum frequency of oscillation is defined as the frequency where the maximum available power gain (MAG) is equal to one [38]. MAG is defined as the power gain at perfect, conjugate matching. This is also known as the maximum unilateral gain. While f_{max} can be calculated from the small-signal parameters, the strong influence of the external parasitics is reflected in [43]

$$f_{\mathrm{max,BJT}} = \sqrt{\frac{f_{\mathrm{T,int,BJT}}}{8\pi(R_{\mathrm{B,ext}}C_{\mathrm{BC,ext}} + R_{\mathrm{B,int}}C_{\mathrm{jC,int}})}} \tag{2.4}$$

with the internal and external components of the base resistance R_B, the partial capacitance of C_{BC} connected between $R_{B,int}$ and $R_{B,ext}$ called $C_{BC,ext}$ and the internal depletion capacitance $C_{jC,int}$. In practice, it is common to demand f_{max} of 2 – 10 times of the circuit's target operating frequency to ensure sufficient available gain enabling the design of oscillators and amplifier based circuits [38]. This is, however, not always possible for mm-wave and sub-THz designs further increasing the design complexity.

2.1.2. III/V Technology

Semiconductor technologies based on elements belonging to the third (III) and fifth (V) main group of elements in the periodic table are called III/V semiconductors. These typically feature a very high charge mobility [44]–[46] resulting in some of the fastest transistors currently available [47].

With materials like Gallium Arsenide (GaAs) and Gallium Nitride (GaN) already used in consumer electronics, some more complex compounds were introduced using Indium Phosphide (InP) in the collector under a GaAs material producing a double heterojunction bipolar transistor (DHBT) [48]. These advances produce transit frequencies of more than 500 GHz [47]–[49] with some reaching a f_{max} of up to 1 THz [50]. Besides the high transistor speeds, the III/V technology is also promising for high-power applications like mobile electronics and electronic vehicle chargers due to the very high thermal conductivity of materials like GaN in comparison to Silicon (Si) [44]. While the RF performance is superior, the integration of large scale systems remains challenging. Although current research tries to combine Si and III/V substrates [46], [51], the design of complex and high-density digital circuits is impossible due to the unsatisfied need for complementary metal-oxide-semiconductor (CMOS) devices. The integration challenge is further compounded by the limitation to small wafers, frequent defects and, thus, generally lower yield [52].

2.1.3. CMOS Technology

CMOS processes build the backbone of large scale integrated digital architectures. With metal-oxide-semiconductor (MOS) transistors requiring no constant input current and complementary logic, consisting of p- and n-channel devices, limiting the drain current to only flow dynamically during switching, low power and fast digital circuits are possible. Due to very low power consumption per stage, this allows systems with billions of transistors distributed over a very small area [53] while thermal dissipation can be managed.
CMOS processes are aggressively scaled resulting in ever smaller process nodes. Currently, technologies like TSMC's 5 nm processes [54] are in production. However, such very small process nodes are specifically optimized for digital operation. Other technology nodes, like 22 nm *FDX*™FD-SOI by GlobalFoundries [55], integrate digital and RF circuits. This eases the design of SOCs resulting in overall lower cost. Due to the enhanced channel control and reduced substrate leakage, both very low power circuits [56] and highly performant circuits in the

mm-wave bands [57] are possible. However, with a backgate dependent f_{max} of 290 GHz and 250 GHz for NMOS and PMOS devices, respectively, the frequency range of operation is limited [55].
Due to ever smaller structures, parasitic influences are relatively increased, degrading parameters like f_{max}. This is mainly due to the very small metal dimensions, which introduce significant resistance to the gate interface. Additionally, reduced breakdown voltages [55] lead to reduced capabilities to generate high-power RF signals.

2.1.4. BiCMOS Technology

BiCMOS processes combine both bipolar and CMOS devices [58]. First created in 1969 [59], this approach enables mixed-signal circuits by combining dense digital designs with highly performant bipolar transistors for analog operation [60].
The performance of this technology type can be further shaped by introducing additional materials like Germanium and Carbon, resulting in Silicon Germanium (SiGe) and Silicon Carbide (SiC) materials, respectively [41], [61]. These are called IV-IV compound semiconductors.
An approach to improving the speed of the bipolar transistors is the introduction of Germanium to the base of the transistors. This reduces the band gap and effectively improves the carrier mobility compared to pure Si [52]. The resulting active device is called a SiGe heterojunction bipolar transistor (HBT). SiC is especially advantageous for power electronics due to the larger band gap resulting in higher breakdown voltages and improved thermal conductivity in comparison to pure Si [61], [62].
Current SiGe BiCMOS technologies commonly provide f_T/f_{max} of many hundreds of gigahertz. The popular SG13G2 node from IHP, for example, features performance figures of f_T/f_{max} =350 GHz/450 GHz [63], [64]. This technology was recently advanced to SG13G3 [65] with f_T/f_{max} = 470 GHz/700 GHz improving the performance with minimal necessary changes to existing designs [66]. In the literature, performance improvements up to $f_T = 1.1$ THz and $f_{max} = 2.5$ THz are predicted within in the next years [43], illustrating the relevance of SiGe BiCMOS technologies in the future.
Finally, the well established SG13G2 technology from IHP [64] was chosen for this project. Due to the high available f_T and f_{max}, moderate

costs, high availability and the potential for integrating RF and digital systems, this technology is ideal for the design of a transmitter system. However, with f_{max} approximately 1.6-times the upper frequency limit of the channel, the design challenge for amplifier based architectures remains high with limited available power gain.

2.2. Transmission Lines and Passive Structures

A precise understanding of the wave propagation on transmission lines is fundamental for the design of complex mm-wave circuits. At very high frequencies or very long distances, in relation to the signal wavelength, feeding signals to a circuit and interconnecting different circuit elements are not trivial. In the following, the general concepts behind transmission lines are discussed, followed by a comparison of different line types in the context of the target system operating at frequencies higher than 200 GHz.

2.2.1. Concept of Transmission Lines

A lumped-element circuit model of a general transmission line of infinitesimally small unit length l'_{TL} along an axis z is given in Fig. 2.2. All lumped components are referenced to l'_{TL}. For a steady-state sinusoidal signal, this model is described by the *Telegrapher* equations [67]:

$$\begin{aligned} \frac{dV(z)}{dz} &= -(R' + j\omega L')\, I(z) \\ \frac{dI(z)}{dz} &= -(G' + j\omega C')\, V(z). \end{aligned} \tag{2.5}$$

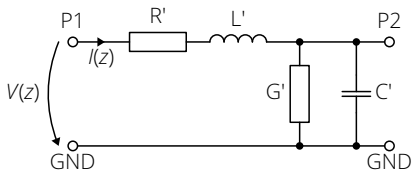


Figure 2.2: Model of an infinitesimally short piece of transmission line of length l'_{TL} along an axis z [67].

This set of equations is, then, simultaneously solved according to

$$\frac{d^2V(z)}{dz^2} - \gamma^2 V(z) = 0$$
$$\frac{d^2I(z)}{dz^2} - \gamma^2 I(z) = 0, \tag{2.6}$$

with the complex propagation constant

$$\gamma = \alpha + j\beta = \sqrt{(R' + j\omega L')(G' + j\omega C')} \overset{R',G'\to 0}{=} j\omega\sqrt{L'C'}. \tag{2.7}$$

For the special case of an ideal, lossless transmission line, both R' and G' in Fig. 2.2 approach zero. This assumption is used to simplify the following calculations and results in a phase constant of

$$\beta|_{R',G'\to 0} = \frac{\gamma(R', G' \to 0)}{j} = \omega\sqrt{L'C'}, \tag{2.8}$$

with an attenuation constant of $\alpha \overset{R',G'\to 0}{=} 0$. The effective wavelength λ' of the signal propagating over the transmission line is

$$\lambda' = \frac{2\pi}{\beta}. \tag{2.9}$$

The phase velocity

$$v_\mathrm{p} = \frac{\omega}{\beta} \overset{R',G'\to 0}{=} \frac{1}{\sqrt{L'C'}} \tag{2.10}$$

is the frequency dependent velocity of propagation of a signal's frequency components [68]. A non-constant phase velocity leads to dispersion, resulting in a distorted signal. However, if

$$\frac{R}{L} = \frac{G}{C} \tag{2.11}$$

is satisfied for a lossy line with linear phase, a distortion free transmission line is realized.
From the equation set Eq. 2.6, the characteristic impedance

$$Z_0 = \sqrt{\frac{R' + j\omega L'}{G' + j\omega C'}} \overset{R',G'\to 0}{=} \sqrt{\frac{L'}{C'}} \tag{2.12}$$

can be found. This determines the center point around which a certain transmission line rotates a connected impedance in the Smith chart.
A wave propagates in a transverse electromagnetic mode (TEM) mode if there is no electric or magnetic field in the direction of propagation. Many transmission lines discussed in the following operate in quasi-TEM mode, which specifies a propagation mode which is very close to TEM allowing the assumption of TEM operation to reduce the mathematical complexity. From this, β and v_p, specified in Eq. 2.8 and 2.10, can be written as

$$\beta \overset{\mathrm{TEM}}{=} \omega\sqrt{\mu\varepsilon} = \gamma \tag{2.13}$$

$$v_\mathrm{p} = \frac{\omega}{\beta} \overset{\mathrm{TEM}}{=} \frac{\omega}{\gamma} \overset{R',G'\to 0}{=} \frac{\lambda'}{2\pi}\omega. \tag{2.14}$$

Finally, the time delay introduced by lossless transmission line in quasi-TEM mode of length l_TL

$$\tau = \frac{l_\mathrm{TL}}{v_\mathrm{p}} = \frac{l_\mathrm{TL}\beta}{\omega} = \frac{l_\mathrm{TL}\sqrt{C'L'}}{\omega} = \frac{\sqrt{CL}}{\omega} = \frac{-\varphi}{\omega} \tag{2.15}$$

can be determined by dividing the forward transmission phase by the angular frequency. Given a constant phase velocity, the time delay is constant as well.

2.2.2. Comparison of Transmission Line Types for Millimeter-Wave Operation

The most frequently used transmission line type in integrated circuits and circuit boards is the microstrip line, shown in Fig. 2.3a. Here, a single-ended conductor is realized in the top metal layer. Below is a metal layer providing the reference ground. The characteristic impedance of this line type is defined by the ratio of conductor width and substrate height [67], [69].
Another common option are coplanar waveguide (CPW) style transmission lines. These consist of a similar single-ended conductor but feature parallel metal strips on the top metal layer connected to ground. In the most basic configuration, there is no grounded bottom layer, which enables the design of these lines on single-layer technologies. However, both lateral ground planes must be connected periodically

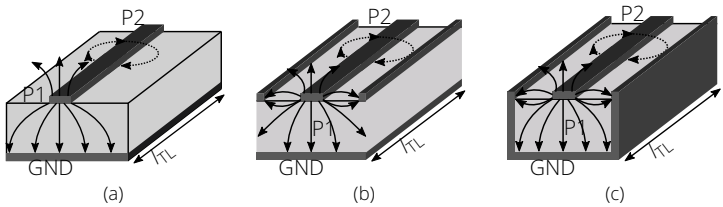


Figure 2.3: Simplified sketch of three common types of transmission lines used to transmit high frequency signals. The solid and dotted field lines indicate the electric and magnetic fields, respectively. (a) Microstrip transmission line. (b) CB-CPW transmission line without grounded sidewalls. (c) GCPW transmission line with grounded sidewalls.

to assure the same potential on both sides. Additional flexibility in the layout is introduced as the characteristic impedance cannot only be varied by the conductor width but also by the spacing between the conductor and the grounding sidewalls [70]. This allows the designer to optimize the line width according to possible connected components. Finally, a general CPW structure allows for easy interconnection with GSG RF-probe pads and enables strictly defined boundaries for the design of open and short waveguide elements [71]. A conductor-backed coplanar waveguide (CB-CPW) structure [71], shown in Fig. 2.3b, introducing a grounded metal sheet, can be extended by connecting the ground plane to the top layer grounded conductors creating grounded sidewalls with stacked vias. This line architecture, depicted in Fig. 2.3c, is called a grounded coplanar waveguide (GCPW). It shorts any exited substrate resonances up to high frequencies, improving the thru behavior [72] enabling the use of this line type for mm-wave and sub-THz designs.

All presented line types are based around conductors placed at the top of the substrate. Therefore, the bottom part of the field exhibits a higher effective electric permitivity than the top part. This results in a electromagnetic field component in the direction of propagation. Thus, no ideal TEM mode is exited and all discussed line types operate in quasi-TEM mode.

Fig. 2.4 compares the behavior of microstrip, CB-CPW and GCPW for frequencies up to 700 GHz. Every line's cross section was optimized for a characteristic impedance of 50 Ω with the CB-CPW and GCPW line sharing the same dimensions. The finite element method (FEM) simulated results show the behavior of a 200 µm long line equating to approximately 110° of phase delay at 245 GHz of phase delay. The GCPW line achieves approximately 10 dB better matching, shown in Fig. 2.4a, while limiting the thru loss to less than 0.5 dB up to 700 GHz without showing any resonant behavior as depicted in Fig. 2.4b.
Analyzing the deviation from an ideal linear phase behavior in Fig. 2.4c, the GCPW line resembles a theoretical transmission line the closest. This transfers to the simulated time delay results depicted in Fig. 2.4d, showing the lowest dispersion and therefore variation in phase velocity for the GCPW line over the entire simulated frequency range. Due to the better matching and thru behavior and very low dispersion, the GCPW line type is well suited for high-frequency and broadband signal. This transmission line architecture is therefore chosen to realize the signal feeding and distributed elements [71] in the designed circuits.

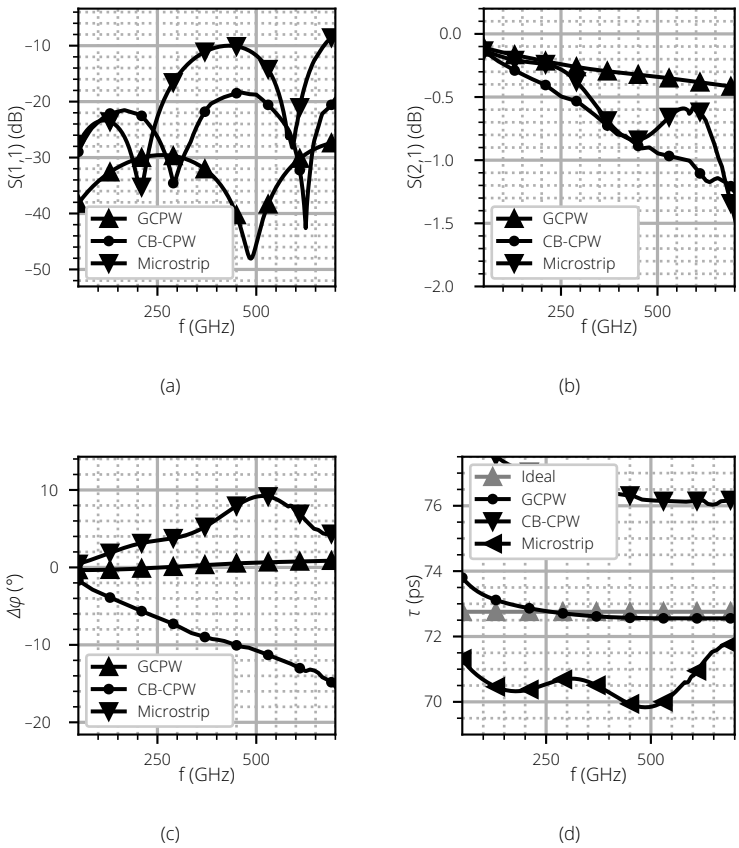


Figure 2.4: FEM simulation results of microstrip, CB-CPW and GCPW transmission lines over frequency up to 700 GHz. (a) Input reflection factor. (b) Forward transmission factor. (c) Phase deviation from an ideal transmission line with linear phase behavior. (d) The time delay calculated from the simulated phase behavior, according to Eq. 2.15.

2.3. Digital Modulation

The process of encoding digital information in a typically much higher frequency bandpass signal is called digital modulation. By inserting the digital message in an analog signal, the data can be transmitted via a defined transmission channel. Focusing on linear modulation schemes, the information can be carried by the amplitude and/ or the phase of the transmitted signal. The general goal of any modulation scheme is to transport the information over the channel with a minimal bit error rate (BER), high datarates and low channel bandwidth while being robust against interference and disturbances from effects like fading, multi-path propagation and noise among others. In the following, the most typical linear digital modulation schemes are presented and compared [73]. Any signal and band shaping methods like filtering the output signal with a root-raised-cosine filter are omitted from this analysis.
Every modulation type encodes the digital information in symbols. The order of a modulation scheme M defines the number of available symbols which can transmit

$$m = \log_2(M) \text{ bits/symbol.} \tag{2.16}$$

Typically, the order of a modulation scheme is noted as a number in front of the name of the modulation type. The bit rate BR and symbol rate SR are not necessarily equal and are related by

$$BR = m \cdot SR. \tag{2.17}$$

The resulting symbols can be illustrated in the complex number space as shown in Fig. 2.5. As any interference and noise spreads the actually

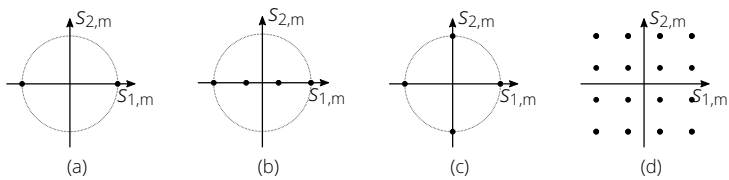


Figure 2.5: Constellation diagrams of different modulation schemes. (a) BPSK/ 2 - ASK. (b) 4 - PAM/ 4 - ASK. (c) QPSK. (d) 16 - QAM.

received symbol compared to the ideal symbol, the minimum distance between two neighboring symbols d_{min} decides the immunity against any deteriorating effects. This metric depends on both the order of the modulation as well as the transmitted energy per bit $\mathcal{E}_{\text{b}}$. For modulations with $M > 2$, there exists a potential for multiple simultaneous bit errors to occur if an erroneous symbol is detected. Gray-coding, which produces a Hamming distance of 1 between neighboring symbols, can alleviate this issue [74].
Pulse amplitude modulation (PAM), which is also called amplitude shift keying (ASK), encodes the digital information in the amplitude of the transmitted signal. All symbols are on the real axis as shown in Fig. 2.5a and 2.5b. The minimum distance between symbols is

$$d_{\text{min,PAM}} = \sqrt{\frac{12 \log_2(M)\overline{\mathcal{E}_{\text{b}}}}{M^2 - 1}}. \tag{2.18}$$

While relying on a simple modulation principle, a major drawback is the limited spectral efficiency resulting from omitting the imaginary axis. Additionally, complex channel estimation is necessary, as any distance change between transmitter and receiver introduces varying attenuation which directly influences the amplitude decision limits of the receiver [75].
The second basic principle of linear modulation is to encode the information in the phase of the bandpass signal. This is called phase-shift keying (PSK). The lowest order implementation is binary phase-shift keying (BPSK), or 2-PSK, which is equivalent to 2-ASK, as shown in Fig. 2.5a. Different codes are possible. Either the separate phase states are assigned to logical ones and zeros or a phase change is associated with a one or zero while a steady phase is associated with the other value easing the synchronization between sender and receiver. As only the phase is varied, the amplitude remains constant, thus, reducing the linearity requirements of power amplifiers in the transmitter and low noise amplifiers in the receiver. Quadrature phase-shift keying (QPSK) can be viewed as an extension of BPSK where two BPSK signals are orthogonally combined. The resulting minimum distance between symbols is

$$d_{\text{min,PSK}} = 2\sqrt{\log_2(M)\mathcal{E}_{\text{b}}}\,\sin(\pi/M). \tag{2.19}$$

Interestingly, 8-PSK has a higher minimum symbol distance than 4-PAM and is therefore more resistant against interference while achieving a higher bit rate for the same bandpass bandwidth. This is due to the more efficient utilization of the symbol space [75]. The peak-to-average power ratio (PAPR), and therefore the linearity requirements, can be further reduced by exploiting techniques like differential PSK [76] and offset PSK [73], which avoid crossing the origin of the constellation diagram.
Finally, quadrature amplitude modulation (QAM) combines the use of amplitude and phase for the encoding of information. It therefore utilizes the full signal space resulting in a minimum symbol distance of

$$d_{\mathrm{min,QAM}} = \sqrt{\frac{6\log_2(M)\overline{\mathcal{E}_\mathrm{b}}}{M-1}}. \tag{2.20}$$

At the same interference resistance as 4-PAM, 16-QAM can transmit twice as many bits for the same bandwidth and average energy per bit. However, due to modulating both amplitude and phase, producing a higher PAPR [77], this modulation scheme requires highly linear circuits and precise channel estimation [75].
Concluding the findings, the minimum distance between symbols reduces for higher modulation orders. This makes the transmission more sensitive towards interference and noise. Higher-order modulations enable higher data rates for a given bandwidth, but require more complex digital baseband circuits to create and interpret the according signals. M-QAM shows the highest interference resistance for a given bandwidth and data rate, but poses strict requirements on the linearity of the transceiver circuits. This work is not strictly restricted in terms of bandwidth due to the very large available spectrum above 200 GHz. Due to the high spectral sparsity resulting from the high free-space and atmospheric attenuation in this band of operation, any issues resulting from interference and multi-path are also inherently limited. A low order modulation scheme is advantageous as it alleviates the need for complex, large and power consuming digital-to-analog converter (DAC) circuits. Due to the high sensitivity to changes in attenuation, ASK modulation is discarded. The resulting system will, thus, be designed for a BPSK modulation scheme, combining both a low-complexity baseband architecture in the transmitter and receiver, a high d_{min} and a low sensitivity to changes in signal power levels.

3. Frequency Quadrupler

This chapter focuses on the local oscillator (LO) signal creation and performance parameters of the LO signal chain operating at 245 GHz. Its task is to supply subsequent stages with a precise and reliable signal specifying the channel center frequency. To optimize the transmitter system performance, a LO chain has to combine the capability to deliver high output power levels with the suppression of unwanted harmonic frequency components, a very low phase noise and a low direct current (DC) power consumption. First, fundamental oscillator architectures and frequency multiplication based architectures are compared. Next, different circuits and approaches to LO generation by frequency multiplication are discussed analyzing the respective characteristics.
A novel approach to frequency multiplication over 200 GHz – the phase-controlled push-push architecture – is presented. An analytical model is devised, studied and compared to ideal simulation results. The low DC power requirements and high possible power efficiency enabled by this circuit topology is finally shown by two different fabricated integrated circuits (ICs). The design of an oscillator circuit at 60 GHz, completing the LO chain, is out of scope of this thesis, referring to many other works contributing to this aspect [11], [78], [79].

3.1. Theoretical Analysis of Frequency Multiplication Circuits

Two different architectures exist for local oscillator chain design: First, a fundamental oscillator providing the needed channel frequency directly [80]. Second, the output signal of a lower frequency oscillator

can be up-converted to a higher harmonic signal resulting in the goal channel frequency [28]. The use of a fundamental voltage-controlled oscillator (VCO) can be performant and efficient both in terms of power consumption [78] as well as phase noise performance [81]. This is especially true for systems operating at sub 60 GHz. However, by increasing the oscillator frequency much further towards the sub-THz band, additional challenges are introduced to the design process.
To achieve oscillation, the *Barkhausen criterion* [82]

$$|\underline{H}(j\omega) \cdot \underline{A}(j\omega)| \geq 1 \tag{3.1}$$

must be satisfied. With the complex system transfer function $\underline{H}(j\omega)$ and the complex system gain factor $\underline{A}$, sufficient gain must be available to allow the circuit to start and maintain oscillation. This requires a sufficient maximum frequency of oscillation (f_{max}) from the technology. Even with modern technologies further improving this performance metric, designs of fundamental-mode VCOs close to f_{max} are still complex, resulting in large power consumption and chip area [79]. As the phase and frequency behavior of a free-running oscillator can be too unstable for a transmitter system, especially in applications where the employed modulation scheme relies on one or both of these metrics, a phase-locked loop (PLL) [83]–[85] is commonly used to stabilize the oscillator signal. This architecture locks the VCO output signal to a given, low frequency reference signal to improve the frequency and phase stability. A significant design challenge concerning PLLs arises from the dependence on frequency division circuits, which are increasingly difficult to realize at high frequencies resulting in a significant area and power consumption [86]–[88].
Alternatively, a low frequency signal source can be combined with a frequency multiplication circuit. This approach enables the use of existing, proven oscillator circuits, reducing design complexity and is, thus, very commonly used in the LO generation of systems operating in the millimeter-wave (mm-wave) and sub-THz spectrum [28], [30]–[32], [89]. One drawback of an ideal frequency multiplication by N architecture is the increased phase noise by a factor of [90]:

$$20 \cdot \log_{10}(N) \text{ dB}. \tag{3.2}$$

This stems from the multiplication of the argument of a voltage signal $s_0(t)$

$$s_0(t) = \cos(\omega \cdot t + \varphi_{\text{noise}}) \tag{3.3}$$

producing an up-converted signal $s_N(t)$

$$s_N(t) = \cos\left(N \cdot (\omega \cdot t + \varphi_{\text{noise}})\right) = \cos\left(N \cdot \omega \cdot t + N \cdot \varphi_{\text{noise}}\right), \tag{3.4}$$

consisting of both the desired frequency $N \cdot \omega$ as well as the phase noise contribution $N \cdot \varphi_{\text{noise}}$. In theory, the fundamental oscillator approach is superior in terms of phase noise [81], as this avoids the increase of phase noise by the multiplier circuit. When comparing real world circuits operating at more than 150 GHz, however, multiplier based circuits are shown to exceed the fundamental oscillator architecture [91]. This is especially true when weighing all performance metrics stated above and depends on the specific performance of the oscillator and the multiplier itself.

Any frequency multiplication circuit employs desired non-linear behavior to produce harmonics of the input signal. The wanted harmonic is then extracted intrinsically by the circuit architecture or a matching network. Three general approaches can be observed most frequently: Single diode based, mixer based and amplifier based architectures. Single diode based multipliers [92] exploit the non-linear characteristic of diodes. Here, mostly Schottky diodes are used due to their low forward voltage drop and fast switching speeds [39]. Large signal power is supplied to a diode which rectifies the signal and produces all possible signal harmonics. Finally, the wanted harmonic is selected by a suitable band-pass filter and optionally amplified. From a system perspective, diodes are often not suitable due to the low conversion gain and therefore inherent demands of very high radio frequency (RF) input power. Multipliers using a mixer architecture either consist of passive structures like diode ring mixers or active structures like Gilbert-cells [93], [94]. The latter type is usually preferred due to higher conversion gain paired with lower necessary signal power levels. To achieve a frequency multiplication, the mixer circuit is supplied with two signals of frequencies ω_1 and ω_2. Assuming an amplitude of 1 and phase offset of 0, the two input signals get ideally multiplied as

$$s_{\text{mix}}(t) = \cos(\omega_1 \cdot t) \cdot \cos(\omega_2 \cdot t) = \frac{1}{2}\left(\cos((\omega_1 - \omega_2) \cdot t) + \cos((\omega_1 + \omega_2) \cdot t)\right). \tag{3.5}$$

Often, to achieve frequency doubling, both inputs of the chosen mixer circuit are connected to the same input signal, resulting in $\omega_1 = \omega_2$

and, thus, the mixed signal $s_{\text{mix}}(t) = \frac{1}{2}(\cos(2\omega_1 \cdot t) + 1)$. The accompanying signal power attenuation of 6 dB is usually further increased by additional losses in passive structures and can be reduced by possible power gain of active stages.
Lastly, amplifier based architectures, more specifically the push-push architecture [95], [96], also rely on the generation of harmonics due to non-linear behavior. However, in contrast to single diode based multipliers, the signal amplitudes of the resulting harmonics can be influenced. A band-pass filter at the output extracts the wanted harmonic signal and suppresses the remaining harmonic spurs. Due to a lower DC operating point, the power consumption is often lower than the power used by active mixer circuits while comparable conversion gains and output powers are achievable thus realizing better efficiency. However, in contrast to Gilbert-cell based mixers, push-push circuits produce single-ended output signals only.
The following sections introduce a recently developed approach to frequency multiplication called phase-controlled push-push (PCPP). First, this is theoretically and mathematically analyzed. Then, two different circuits employing this concept are shown and discussed. Finally, the frequency multiplication stage in section 3.4 is used in a mm-wave transmitter front-end in chapter 6.

3.2. Phase-Controlled Push-Push Principle for Frequency Quadrupling

The phase-controlled push-push architecture was first introduced in [97] and later shown for different frequency bands in [Ste1], [Ste6], [98]. It builds on the well established push-push architecture used for frequency doubling [96], [99], [100]. Here, the architecture depicted in Fig. 3.1, exploits the creation of harmonics of low biased differential amplifiers. By biasing the transistors $Q_{1,2}$ in class AB and supplying a differential signal to the bases, the incoming signal is full-wave rectified. Filtering the high frequency components at the output extracts the second harmonic. Due to the differential structure of this approach, the odd harmonics are inherently suppressed, relaxing the requirements on the output filter. This concept can be mathematically shown by adding the two rectified collector currents:

$$I_{c1} = I_s \cdot \exp\left(\frac{\widehat{V} \cdot \cos(\omega t) + V_{be,0}}{V_T}\right) = I_{c,OP} \cdot \exp\left(\frac{\widehat{V} \cdot \cos(\omega t)}{V_T}\right) \tag{3.6}$$

$$I_{c2} = I_s \cdot \exp\left(\frac{\widehat{V} \cdot (-\cos(\omega t)) + V_{be,0}}{V_T}\right) = I_{c,OP} \cdot \exp\left(\frac{\widehat{V} \cdot (-\cos(\omega t))}{V_T}\right) \tag{3.7}$$

$$I_{c1} + I_{c2} = I_{c,OP}\left(\exp\left(\frac{\widehat{V} \cdot \cos(\omega t)}{V_T}\right) + \exp\left(\frac{\widehat{V} \cdot (-\cos(\omega t))}{V_T}\right)\right) \tag{3.8}$$

with the saturation current I_s, the pn-junction threshold voltage $V_{be,0}$ and the input signal amplitude $\widehat{V}$. By exploiting the series identity of the sum of exponential functions with inverted arguments [101] this can be transformed to

$$I_{c1} + I_{c2} = I_{c,OP}\left(2 + \left(\frac{\widehat{V}}{V_T}\right)^2 \cos(\omega t)^2 + \frac{1}{12}\left(\frac{\widehat{V}}{V_T}\right)^4 \cos(\omega t)^4 + \ldots\right) \tag{3.9}$$

$$= I_{c,OP} \sum_{n=0}^{\infty} \frac{2}{(2n)!}\left(\frac{\widehat{V}}{V_T}\cos(\omega t)\right)^{2n}. \tag{3.10}$$

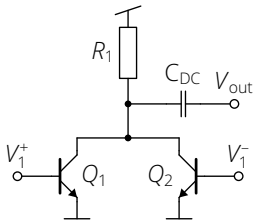


Figure 3.1: Simplified schematic of a push-push frequency doubler stage.

With the complete transformation of Eq. 3.10 shown in section A.1, the approximate result for the summed output current can be written as

$$\begin{aligned} I_{c1} + I_{c2} \approx I_{c,OP} \Bigg(& 2 + \frac{1}{32}\left(\frac{\hat{V}}{V_T}\right)^4 + \frac{1}{2}\left(\frac{\hat{V}}{V_T}\right)^2 \\ & + \cos(2\omega t)\left(\frac{1}{24}\left(\frac{\hat{V}}{V_T}\right)^4 + \frac{1}{2}\left(\frac{\hat{V}}{V_T}\right)^2\right) \\ & + \cos(4\omega t)\left(\frac{1}{96}\left(\frac{\hat{V}}{V_T}\right)^4\right)\Bigg), \end{aligned} \tag{3.11}$$

displaying the exclusion of odd harmonics and small contribution of harmonics higher than the second. The input signal amplitude leads to the expansion of the collector current bias point. Overall, this proves the push-push architecture to be an effective approach to frequency doubling.

Extending the push-push circuit by stacking another transistor pair $Q_{3,4}$, as shown in Fig. 3.2a, enables a PCPP frequency quadrupler. The transistor pair $Q_{1,2}$ is biased in class B and $Q_{3,4}$ are biased in class AB. Differential RF signals are supplied to $Q_{1,3}$ and $Q_{2,4}$. The inverse phases are symbolized accordingly by marking the input signals + or –. This phase and operation point setup results in the combination of the full-wave rectifying behavior of the aforementioned push-push architecture with a further signal manipulation by transistors $Q_{1,2}$, resulting

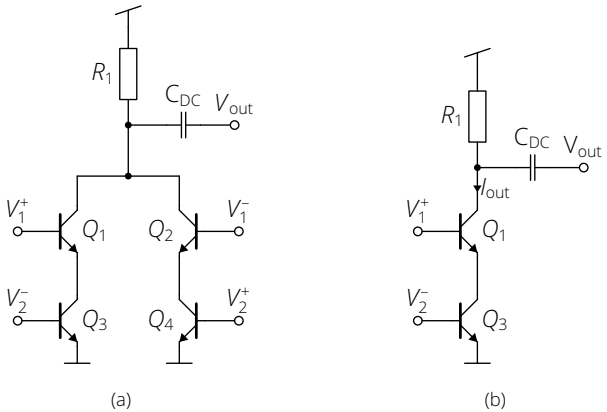


Figure 3.2: Simplified schematic of the studied PCPP architecture. (a) Schematic of a differential PCPP stage. (b) Schematic of a single-ended transistor pair used in the PCPP circuit.

in the creation of the fourth harmonic. The major advantage in this topology, in comparison to cascading two standard push-push stages to produce the fourth harmonic, is the re-use of the DC current flowing through the stacked transistors reducing the total power consumption. Additionally, this results in a reduced area consumption due to fewer output matching networks.

As the PCPP principle is not very broadly published yet [Ste1], [Ste6], [97], [98], it will be mathematically modeled and analyzed in depth, enabling a further understanding of the underlying principles and potential optimizations of the operation points and signal input amplitudes. For the sake of simplifying the analysis, only one half of the topology shown in Fig. 3.2a will be examined, as depicted in Fig. 3.2b, describing half a period of the input signal. This approach can then be extended to the differential circuit. All variables follow the indices of the single-ended schematic.

First, three different operation conditions must be distinguished as defined by [97]:

(A) Q_1 is in cutoff resulting in no output signal,

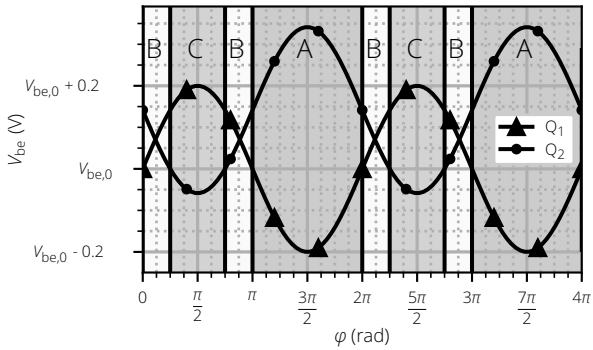


Figure 3.3: Base-emitter voltages of a single-ended PCPP transistor stack shown in Fig. 3.2b.

(B) Q_1 is forward active, while Q_3 is in saturation,

(C) Q_3 moves into sub-threshold and towards cutoff.

The base-emitter voltages

$$V_{be,1} = \widehat{V} \cdot \sin(\varphi) + V_{be,OP,1} \tag{3.12}$$

$$V_{be,3} = -\widehat{V} \cdot \sin(\varphi) + V_{be,OP,3} \tag{3.13}$$

for these states are illustrated in Fig. 3.3 over the phase φ, referenced to the transistors pn-junction threshold voltage $V_{be,0}$. This allows an examination independent of the technology node and specific frequency band. While the operation point of Q_1 is set to a constant value of

$$V_{be,OP,1} = V_{be,0}, \tag{3.14}$$

the operation point of Q_3 is calculated as

$$V_{be,OP,3} = \widehat{V} \sin\left(\frac{\pi - \nu}{2}\right) + V_{be,0} \tag{3.15}$$

for the input signal amplitude $\widehat{V}$ to remain in sub-threshold – state C – for a given phase ν in radians, determining the relative width of case B and case C.

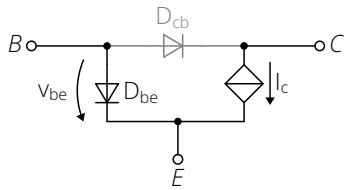


Figure 3.4: Transport version of the Ebers-Moll large signal model of a NPN bipolar transistor [39], [102]. D_{cb} (gray) is only forward biased if the transistor is operated in saturation.

The output signal of the circuit is defined as

$$V_{out} = V_{cc} - R \cdot I_{out} \tag{3.16}$$

$$\text{with } I_{out} = I_{c1} = I_{c3}. \tag{3.17}$$

Accordingly, the output current I_{out} has to be determined for every case of operation.

Case A

While Q_1 is in cutoff, there exists no output current and thus no output signal. Additionally, V_{c3} is connected to ground by Q_3.

Case B

The behavior of Q_3 in saturation can be modeled by the *Transport* version of the *Ebers-Moll-model* [39], [102] shown in Fig. 3.4. This is a common large-signal model suitable for hand calculation and modeling. It provides a relatively simple static representation of a bipolar transistor, excluding the *Early-* and *Avalanche-Effects* [103]. While the collector-base diode D_{cb} is reverse-biased in forward-active operation, further reducing the model complexity, both the D_{cb} as well as D_{be} are forward biased in saturation. Typically, saturation is defined by $V_{bc} > 0 \wedge V_{be} > 0$. However, according to [103], a pn-junction is not fully forward biased until a certain value for V_{bc} is exceeded, resulting in an extension of the forward active mode of the transistor by some tenths of a Volt. This

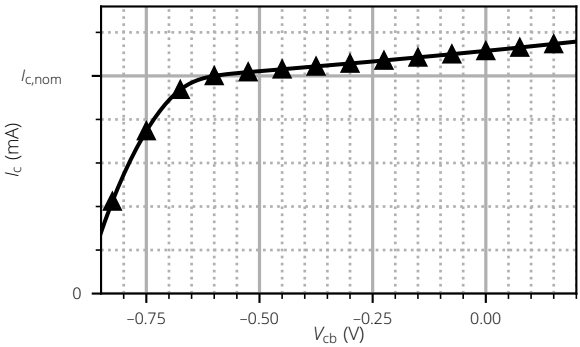


Figure 3.5: Normalized simulated results of the collector current of the employed bipolar transistors over the collector-base voltage for a constant base current showing the saturation of I_c at approximately −0.6 V.

can be observed in the normalized simulated I_c over V_{cb} behavior of the used transistors, shown in Fig. 3.5, resulting in an offset of approximately −0.6 V. Accordingly, V_{cb} has to be larger than 0.6 V and $V_{be} > 0$ for Q_2 to operate in saturation. The collector current I_{c1} of Q_1, in the forward active region,

$$I_{c1} = I_s e^{\frac{V_{be1}}{V_T}} (1 + \frac{V_{ce}}{V_Y}) \tag{3.18}$$

$$= I_s e^{\frac{V_1 - V_{c3}}{V_T}} (1 + \frac{V_{ce}}{V_Y}) \approx I_s e^{\frac{V_1 - V_{c3}}{V_T}} \tag{3.19}$$

depends, neglecting the Early-Effect, on the collector potential V_{c3} of Q_3. With both diodes of Q_3 forward biased, its collector current

$$I_{c3} = I_s \cdot e^{\frac{V_{be,3}}{V_T}} - I_{s,cb} \cdot e^{\frac{V_{bc,3}}{V_T}} \tag{3.20}$$

$$\Rightarrow I_{c3} = I_s \cdot e^{\frac{V_2}{V_T}} - I_{s,cb} \cdot e^{\frac{V_2 - V_{c3}}{V_T}} \tag{3.21}$$

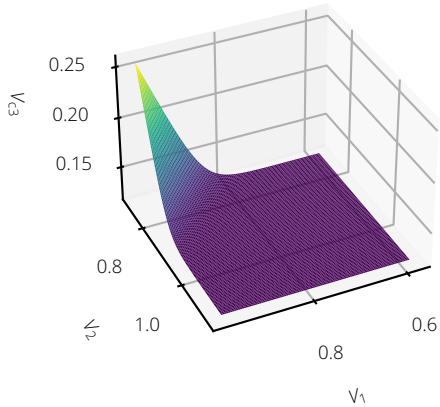


Figure 3.6: Collector voltage V_{c3} of Q_3 in Fig. 3.2b in saturation.

is calculated with the saturation current $I_{s,cb}$ of D_{cb}. Applying *Kirchhoff's* first law at node x, marked in Fig. 3.2b, and $I_{c1} = I_{c3}$ with the substitution of $a = \frac{I_{s,cb}}{I_s}$, the expressions

$$I_s \cdot e^{\frac{V_1 - V_{c3}}{V_T}} = I_s \cdot e^{\frac{V_2}{V_T}} - I_{s,cb} \cdot e^{\frac{V_2 - V_{c3}}{V_T}} \tag{3.22}$$

$$e^{\frac{V_2}{V_T}} = e^{\frac{V_1 - V_{c3}}{V_T}} + \frac{I_{s,cb}}{I_s} e^{\frac{V_2 - V_{c3}}{V_T}}. \tag{3.23}$$

are found. This is transformed to

$$V_{c3} = V_T \ln\left(a e^{\frac{V_2}{V_T}} + e^{\frac{V_1}{V_T}}\right) - V_2, \tag{3.24}$$

according to the calculations and conditions shown in section A.2, depending on the two input signals V_1 and V_2. Assuming a typical value of $a = 100$ [103] and a signal amplitude of $\widehat{U} = 200$ mV the dependency of V_{c3} on V_1 and V_2 is illustrated in Fig. 3.6. With all values for Eq. 3.19 determined, case B is fully described.

Case C

During case C, transistor Q_3 moves into the sub-threshold region for a predefined phase angle ν. From $I_{c1} = I_{c3}$ with $I_b = \frac{I_c}{B}$ follows $I_{b1} = I_{b3}$ for equally scaled transistors. This leads to $V_{be,1} = V_{be,3}$. Therefore, the collector currents can be written as

$$I_{c1} = I_{c3} \tag{3.25}$$

$$I_s e^{\frac{V_2}{V_T}} = I_s e^{\frac{V_1 - V_{c3}}{V_T}}. \tag{3.26}$$

Simple transformation directly relates the input voltages to

$$V_{c3} = V_1 - V_2. \tag{3.27}$$

This is then inserted into Eq. 3.19 to calculate the output signal.

Combined cases

Finally, all three cases are combined into piecewise defined functions for the output current.

$$I_{out} = \begin{cases} 0 & \text{, Case A} \\ I_s e^{\frac{V_1 - V_T \ln\left(a e^{\frac{V_2}{V_T}} + e^{\frac{V_1}{V_T}}\right) - V_2}{V_T}} & \text{, Case B} \\ I_s e^{\frac{V_2}{V_T}} & \text{, Case C} \end{cases} \tag{3.28}$$

This is then inserted into Eq. 3.16. Assuming a diode relation of $a = 100$, a input signal amplitude of $\widehat{U} = 200\,\text{mV}$ and a sub-threshold angle of $\nu = \frac{\pi}{2}$, the output signal shown in Fig. 3.7 is produced for the single-ended circuit depicted in Fig. 3.2b. This shows a strong fourth harmonic signal for the first π radians while the output signal is zero for the second half of the input signal. However, combining two single ended PCPP circuits into a differential architecture, resulting in the schematic shown in Fig. 3.2a, the differential excitation of the two half circuits produces a continuous output signal with the strong fourth harmonic component as depicted in Fig. 3.8. With the model producing the expected transient signal, the harmonic behavior of the circuit can be studied. The normalized results of a numerical calculation of the power-spectral-density (PSD) of the combined signal are

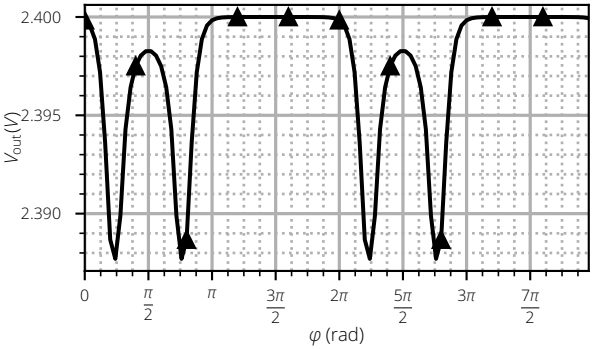


Figure 3.7: Mathematical model of the output signal of the single-ended PCPP stage in Fig. 3.2b output for $a = 100$, $\widehat{U} = 200$ mV and $v = \frac{\pi}{2}$.

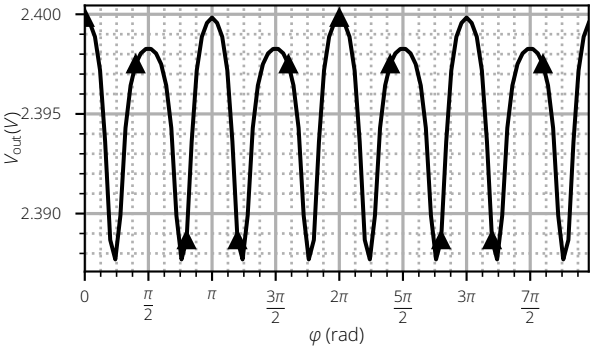


Figure 3.8: Mathematical model of the output signal of the differential PCPP stage in Fig. 3.2a output for $a = 100$, $\widehat{U} = 200$ mV and $v = \frac{\pi}{2}$.

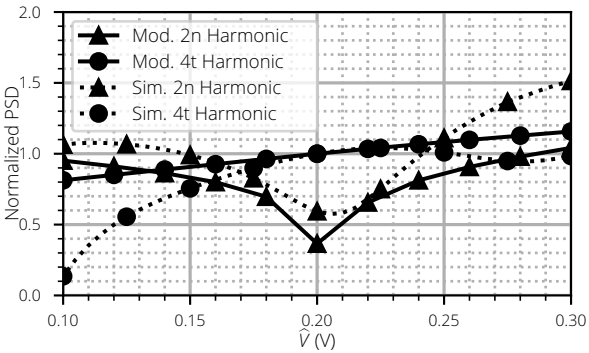


Figure 3.9: Mathematical model and ideal simulation results of the harmonic components of the output signal of a differential PCPP stage in Fig. 3.2a over input signal amplitude for $a = 100$ and $v = \frac{\pi}{2}$.

shown in Fig. 3.9 for input signal amplitudes between 100 mV and 300 mV. Here, the central research finding is, that, given the chosen model characteristics, an optimum input signal amplitude of 200 mV exists in an ideal PCPP circuit which produces a large fourth harmonic signal while minimizing the second harmonic.

Model Limitations

The model described above experiences some limitations due to simplifications, reducing the model complexity while preserving the important basic principles and correlations needed for strong evidence and explanation of the circuit behavior. These limitations, foremost, concern both the *Avalanche effect* and the *Early effect*. While the first phenomenon is not applicable in the model analyzed, the Early-Effect causes only a negligible expansion of the collector current, shown in Fig. 3.5, and is therefore omitted. Additionally, all frequency dependent behaviors as well as the saturation of the transistors in the real world due to an excess of input power is ignored. This approach was chosen to focus on the basic principles and allows for an universal

analysis. This is also reflected in the chosen, purely resistive, output load and the assumed ideal match of all transistor base inputs. In real designs, it is not feasible to perfectly match all transistor inputs as $Q_{1,2}$ and $Q_{3,4}$. Additionally, the matching complexity is increased by the precise phase delays required at the bases of the individual transistors. Finally, some model parameters like the size relation between D_{cb} and D_{be} as well as the transistor saturation current could only be estimated to allow for descriptive, numeric results.

3.3. Stand-alone Phase-Controlled Push-Push Quadrupler

The frequency quadrupler presented in this section 3.3 was previously published in [Ste1].
Following the analysis in section 3.1, a LO chain architecture based on frequency multiplication is realized. Targeting minimum power consumption, the first reported PCPP based frequency multiplication circuit operating at frequencies higher than 200 GHz is realized as a proof of feasibility of the principle in the target frequency band.

Architecture

A low frequency input signal is supplied via an external laboratory reference signal source. With sinusoidal signal sources for the use in laboratories or integrated oscillators [78] commonly available up to 67 GHz and a target channel frequency of 245 GHz, the minimum needed integer multiplication factor

$$\left\lceil \frac{f_{\text{target}}}{f_{\text{source,max}}} \right\rceil = N, \tag{3.29}$$

is calculated to a value of $N = 4$. This multiplication factor is commonly achieved by a chain of two frequency doubling circuit blocks [94], [96], [100], [104]. These usually consist of either push-push (PP) circuits [96], Gilbert-cells [94] or a combination of both [104]. Other designs have optimized the biasing of a Gilbert-cell to maximize the fourth harmonic in a single stage [105] or exploited tunable signal clipping to create the wanted harmonics [95]. This design will further investigate the PCPP approach, first shown in [97], to enable efficient frequency quadrupling in a single stage and thus extend the feasibility of this approach to frequencies larger than $\frac{1}{2} f_{\text{max}}$. To enable a fair and precise characterization of the underlying principle and performance, the design features no input nor output buffers, as these commonly inflate DC-, RF- and total efficiency values.
The resulting system is shown in Fig. 3.10. It consists of a Wilkinson divider at the input, a delay line balun, the PCPP quadrupler core and an output matching network which also selects the target harmonic.

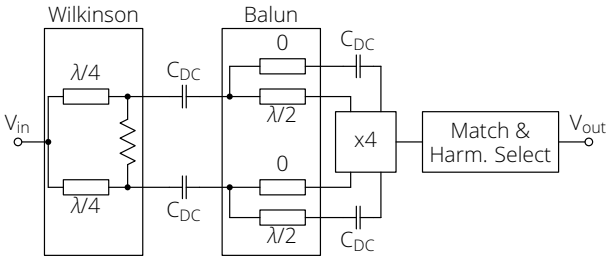


Figure 3.10: Overview of the stand-alone PCPP quadrupler circuit architecture and building blocks.

Circuit Design

At the input of the circuit, a passive 2-way Wilkinson divider [38], [106] splits the signal equally. Consisting of two $\frac{\lambda}{4}$ transmission lines with line impedance $Z = \sqrt{2}Z_0$, it splits the supplied input power into two phase-equal parts while providing a matched input and high isolation between the two output ports. Additionally, if any power is reflected by the attached circuitry, this is consumed in the 100 Ω output resistor, thus further enabling independent behavior of both paths. A delay line balun is connected by DC-blocking capacitors, scaled to provide a very low series impedance $\underline{Z} = \frac{1}{j\omega C}$ for the RF signal. The line pairs with characteristic impedance of $Z_0 = 50\,\Omega$ provide a difference in length of $\frac{\lambda}{2}$ equaling 180° of phase angle. According to the port definitions in Fig. 3.11, this approach leads to a amplitude imbalance of 0.5 dB and 0.8 dB, shown in Fig. 3.12, or 189° and 202° of phase difference, depicted in Fig. 3.13 at 61 GHz, respectively. The frequency quadrupler core is depicted in Fig. 3.14. Based on [97], it shows an extended architecture, employing a pseudo-differential cascode $Q_{1...4}$ at the bottom of the PCPP circuit. As a cascode can provide larger signal swing than an emitter stage, and the signal amplitude between the lower and upper stage dictates the total signal amplitude of the circuit. This maximizes the output power of the quadrupler. Special care was taken during the layout process to minimize the length of the base of $Q_{2,4}$ to the RF ground connection to avoid any potential

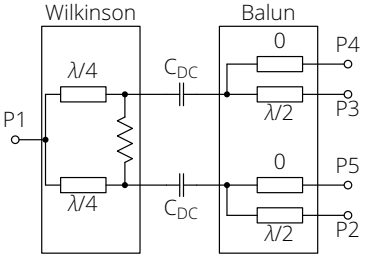


Figure 3.11: Overview of the passive input network of the stand-alone PCPP quadrupler circuit and the simulation port definitions.

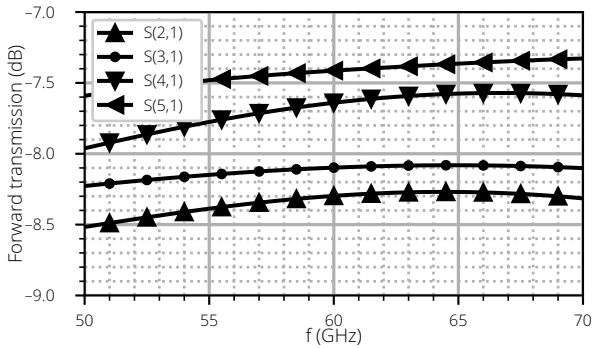


Figure 3.12: Simulation results of the forward transmission factors of the passive input network of the stand-alone PCPP quadrupler.

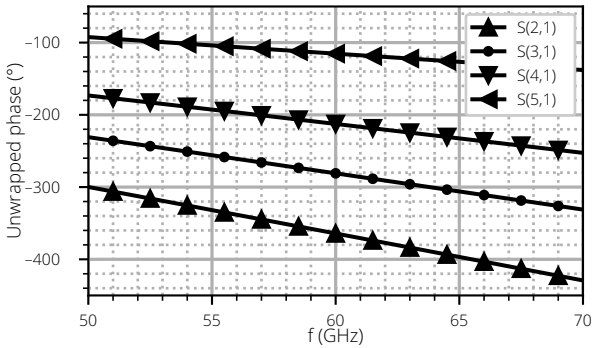


Figure 3.13: Simulation results of the unwrapped phase behavior of the passive input network of the stand-alone PCPP quadrupler.

stability issues arising from a parasitic series inductance in combination with an imperfect differential signal. Thus, the grounding capacitor was directly inserted into the grounded wall between the two pseudo-differential paths, minimizing the connection lengths. Connected by a low impedance series line, acting as inter-stage matching, the upper stage is realized as a single transistor $Q_{5,6}$. All transistors are the same size and are optimized trading off DC power consumption, transit frequency and especially RF power delivery capability. During the layout process, special attention was paid to creating a symmetrical circuit to intrinsically suppress odd harmonics. As even harmonics in the output spectrum are far away from the targeted fourth harmonic signal, these are less complex to filter only requiring low order filter structures. The quadrupler core is connected to the input stage, which includes the necessary series transmission lines matching the two stages. As the input impedances at the bases of each stage differ, the performance is optimal at a phase difference other than 180°. A resonant matching network consisting of both transmission lines and series capacitors forms the output stage. This includes an open stub line TL_9, which is designed to cancel the second harmonic, which is intrinsically strong

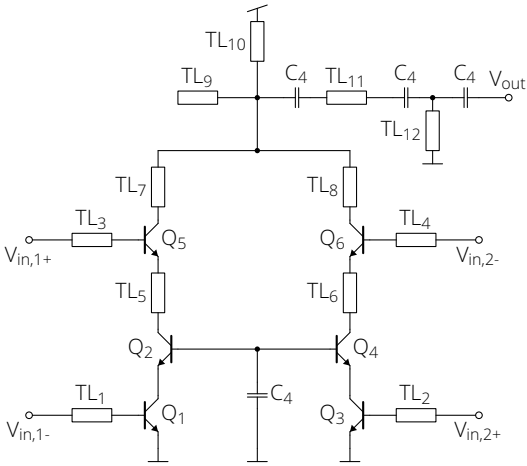


Figure 3.14: Simplified schematic of the stand-alone PCPP quadrupler core.

in a push-push based architecture, while the remaining elements provide a matched output and maximize the output power.

Simulation and Measurement Results

The fabricated integrated circuit is shown in Fig. 3.15. In total, the chip area is 1.02 mm^2 – most of which is used for the passive signal feed structures and pads – with only 0.24 mm^2 covered by the actual active core. At a RF input power of 3.5 dBm, the active core consumes 22.4 mW. The biasing circuitry uses 12.6 mW of DC power. Due to the low operation point, the input power has significant influence on the DC power consumption. With rising input power levels, the DC power consumption increases as well. This expansion of the operation point is expected for transistors biased by a voltage source and will be further analytically studied later.
For characterization in the lab, a 67 GHz vector-network analyzer (VNA) is combined with frequency extension modules in the 220–330 GHz frequency range. At the input, the network analyzer was used as the

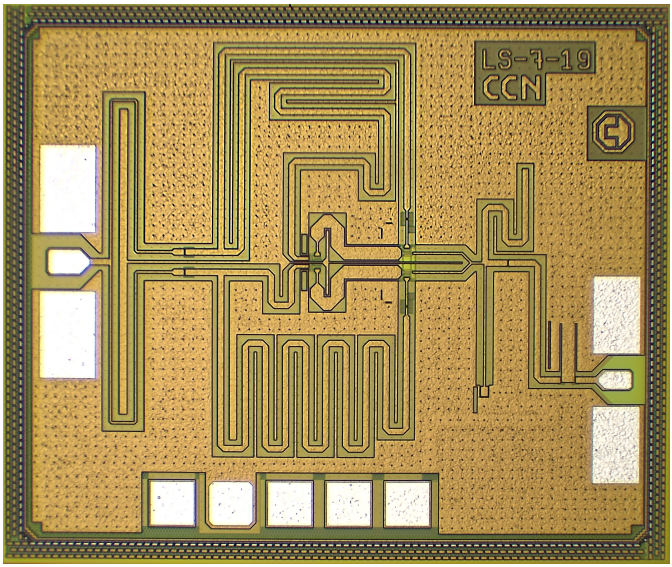


Figure 3.15: Chip photograph fabricated stand-alone PCPP quadrupler circuit sized 1.1 mm × 0.93 mm = 1.02 mm^2. [Ste1] © IEEE 2020

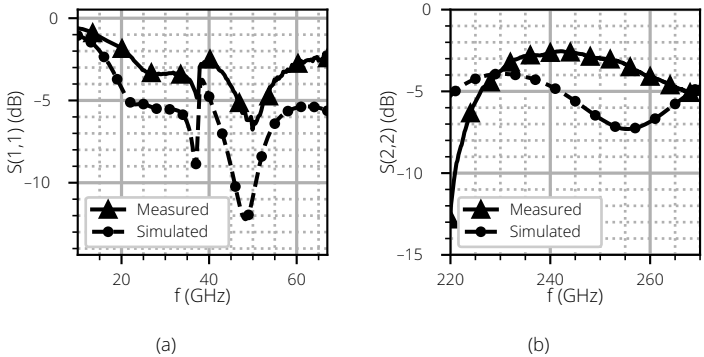


Figure 3.16: In- and output matching behavior of the stand-alone PCPP quadrupler at small-signal conditions. (a) Input match over input frequency range. (b) Output match over transformed frequency range. [Ste1] © IEEE 2020

signal source, feeding an external power amplifier connected to a ground-signal-ground (GSG) probe. A frequency converter module attached to a GSG waveguide probe via a waveguide s-bend is used as a receiver at the output. Both in- and output were power calibrated to allow precise large signal measurements. At the input, this was done using a coaxial power probe while a second converter module was calibrated as power source which then fed known power levels to the receiving converter at the output. The attenuation introduced by the different probes was de-embedded according to the respective data-sheet values.

The input and output matching characteristics are shown in Fig. 3.16. The measurements fit the simulation within a 2.5 GHz frequency shift at the input and, following the quadrupler behavior, a 10 GHz shift at the output.

Fig. 3.17 shows the output power spectrum of the second and fourth harmonic of the input signal as well as the low frequency local oscillator input signal feedthrough. This is shown over the full input frequency range with the equivalent fourth harmonic frequency being marked at the top. The fourth harmonic achieves a maximum output power

of –8.4 dBm at 255.5 GHz from 3.5 dBm of input power at 63.875 GHz. De-embedding the losses of the passive signal feeding network, this equates to a conversion loss of 10.4 dB of the quadrupler core. A 3-dB-bandwidth of 12.8 GHz equates to a relative bandwidth of 5 %. Measured and simulated results match well within the 10 GHz of frequency offset discussed above. The input signal is suppressed by more than 45 dB over the entire frequency range, even improving upon the simulated value. At the frequency range of operation, the second harmonic is suppressed by 10 dB. Here, the suppression is heavily affected by an imperfect layout of the meandered open stub TL_9 in Fig. 3.14, employed to further attenuate the second harmonic. Post-measurement electromagnetic simulations show a parasitic coupling effect of part of the meandered transmission line to the immediate output, which was not modeled during the original design process. This leads to a significant degradation of the suppression of the second harmonic. By replacing the layout of TL_9 with a straight line, the second harmonic suppression can be improved by 10 dB in simulations.

The input power was swept between –2.7 dBm and 3.5 dBm at the probe tip. The resulting output power is shown in Fig. 3.18. It rises linearly following the behavior theoretically predicted in Fig. 3.9. For orientation, both the typical and the worst case simulation results are included. It can be seen that the circuit behavior is, without further analyzing the wafer, well predicted by the worst case simulation.

Finally, the DC power consumption of the circuit is analyzed. Fig. 3.19 shows a steady increase of power consumption with rising input power. This is due to the fact that the low voltage biased transistors' operation points expand according to the analytical deductions shown in section A.3. As the modified Bessel function $\mathbb{I}_0(x)$ is steady and monotonously rising for $x > 0$, a constant increase of collector current and thus, given a constant voltage supply, power consumption is expected. The measured and analytically calculated, per Eq. A.17, power consumption match well in behavior. The deviations can be explained by assumptions like a purely real load impedance at the base of the transistors and neglecting any influence of mismatch in the analytical model.

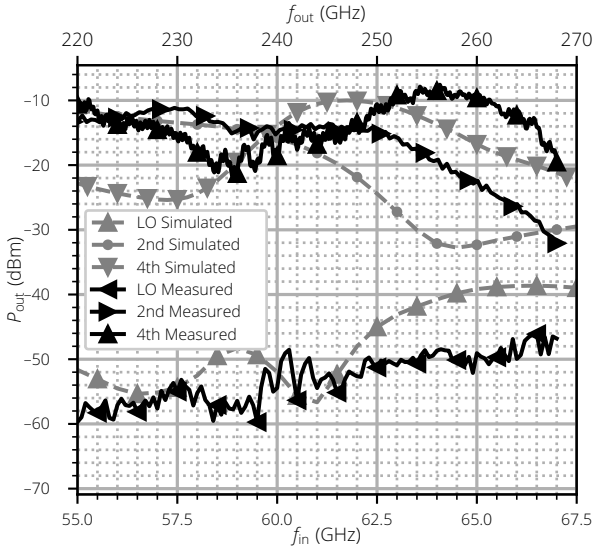


Figure 3.17: Output power spectrum of the stand-alone PCPP quadrupler over input frequency. [Ste1] © IEEE 2020

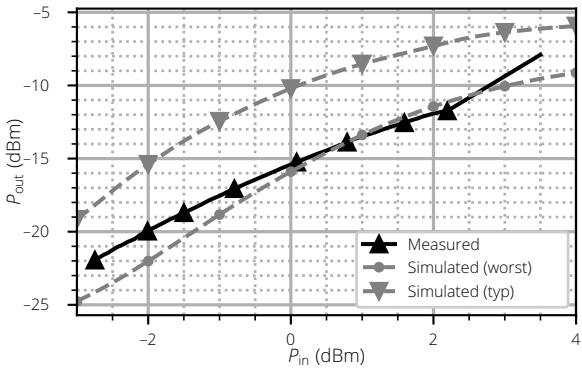


Figure 3.18: Input power sweep of the stand-alone PCPP quadrupler at an output frequency of 255 GHz. [Ste1] © IEEE 2020

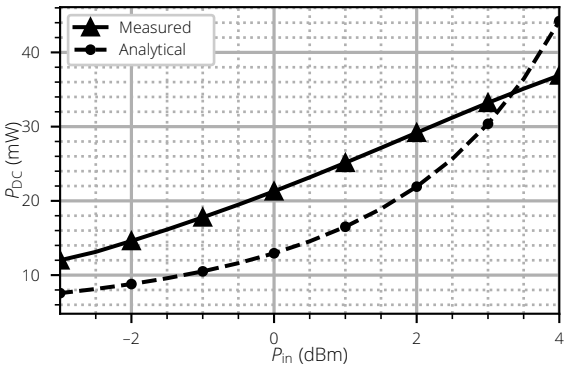


Figure 3.19: DC power consumption of the stand-alone PCPP quadrupler over input power compared to the analytically calculated power consumption based on Eq. A.17. [Ste1] © IEEE 2020

Conclusion

This feasibility study shows that the theoretical insights into the PCPP principle can be applied in an effective architecture for mm-wave local oscillator signal generation based on the multiplication of a lower frequency input signal. A key research finding is the possibility of transferring the theoretically studied behavior of the PCPP architecture to the mm-wave spectrum, establishing its feasibility at frequencies larger than 200 GHz and $\frac{1}{2}f_{\mathrm{max}}$. A major advantage of this architecture is the very low DC power consumption which stems from the reuse of the collector current in the two stacked stages combined with low biased transistors typical for PP based architectures. The relation between the input power level and the DC power consumption was theoretically studied and compared to the measurements. A tradeoff between DC power consumption and output power is therefore possible by modulating the input power.

Compared to the state of the art in Tab. 3.1, the circuit achieves the highest frequency of operation while consuming less than a fourth of the power of Gilbert-cell based [94] and PP diode hybrid systems [100]. Even when comparing to circuits combining Gilbert-cells with PP doubling [104] or pure PP based systems [96], the power consumption is halved.

A comparison to a conventional circuit based on cascaded push-push and Gilbert-cell stages [104], which also does not employ any amplifiers at in- or output, highlights the advantages of this topology. At 0.63 % a more than fifteen-fold increase of total efficiency can be observed while achieving a 8 dB higher output power of –8.4 dBm and a conversion loss reduction of 12 dB.

Table 3.1: State of the art of current millimeter-wave frequency multiplier circuits [Ste1].

	This	[97]	[92]	[100]	[94]	[104]	[96]
Architecture	PCPP	PCPP	Diode	PP/Diode	Gilbert	PP/Gilbert	PP
Multiplication factor	4	4	2	2×2	2×2	2×2	2×2
Technology	130 nm SiGe	130 nm SiGe	GaAs Schottky	90 nm SiGe	130 nm SiGe	130 nm SiGe	130 nm SiGe
Center frequency (GHz)	255.5	129	212.5	229.5	150	222.5	186
Relative bandwidth (%)	5	12.4	21.2	13.5	28	29.2	36.6
P_{in} (dBm)	3.5/-4[+]	-3	20	5	-2.8	8	-1
P_{out} (dBm)	-8.4	-2.4	13.3	2	2.2	-16.4	-1
Buffer (in/out)	no/no	yes/yes	no/no	interstage	no/no	no/no	no/yes
Area (mm^2)	1.02	0.27	module	1.44	0.61	0.45	1.3
P_{DC} (mW)	22.4	35.2	89	200	100	48	45
Total efficiency (%)	0.63	1.61	11.31	0.73	1.65	0.04	1.7

[+] excluded attenuation of passive input balun

3.4. Phase-Controlled Push-Push Quadrupler based LO-chain with High Output Power

The circuit described in this section 3.4 was published before in [Ste6]. A typical drawback of frequency multiplication circuits, especially in the mm-wave and sub-THz range, is the need to supply large RF power to the input of the circuit [100], [104]. This is often combined with limited output power [95], [96], due to a commonly negative conversion gain, resulting in overall low efficiency. As LO chains typically drive subsequent stages like modulators this is particularly negative.
Building on the proof of concept of employing the PCPP architecture in circuits operating at frequencies higher than 200 GHz, this circuit extends the principle into a highly performant LO chain for mm-wave transmitters as described in chapter 6. An IC is realized combining moderate necessary input power levels, high power gain, large output power and high efficiency, thereby improving the state of the art significantly.

Local Oscillator Chain Architecture

The block architecture of the proposed LO quadrupler is shown in Fig. 3.20. Instead of a purely passive input feed network, the external, low frequency LO signal is fed into an active balun. This produces a differential signal from the single-ended input signal [107] and amplifies it, thus reducing the impact of potential losses in the LO signal distribution network in a larger communication system. Additionally, this ensures sufficient signal power for optimal operation in the following quadrupler stage, while isolating any input variations from the sensitive quadrupler core. The subsequent PCPP based mm-wave quadrupler [Ste1], [97], building on the results of section 3.3, synthesizes the fourth harmonic of the input signal in a single stage while being tuned for minimum power consumption. This enables the allocation of DC power to the stages with more intrinsic gain to improve total system efficiency. At the output, an injection-locked oscillator (ILO) buffer amplifier [11], [108] provides large gain and output power. Due to the high Q-factor of this circuit, further frequency selection is enabled, suppressing parasitic harmonics and providing a high degree of spectral purity. One particular advantage of using ILOs, besides the

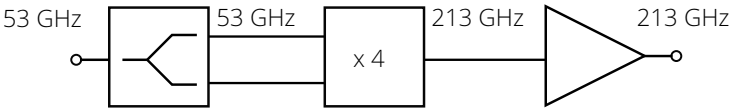


Figure 3.20: Simplified architecture of the proposed LO chain consisting of an active input balun, a PCPP frequency quadrupler and an ILO output amplifier.

large narrow band gain, is the negligible effect on the noise, which is solely dependent on the preceding signal source [109].

Circuit Design

At the input of the LO chain, an active balun converts the single-ended externally supplied signal to a differential signal. The circuit, shown in Fig. 3.21, is based on an asymmetrically excited, differential cascode [110]. The high gain provided by the cascode architecture enables the compensation of losses introduced by the LO distribution network. Additionally, the reverse isolation, inherent to cascodes [111], separates the sensitive quadrupler core from impedance variations in the LO supply and the separate signal paths. To optimize for DC power consumption and reduce the needed area, a single-stage design, shown in Fig. 3.21, was preferred to a multi-stage design [107], [112], despite the slightly higher gain and phase imbalances. Any resulting gain and phase variations is considered in the design process of the inter-stage network between balun and quadrupler core. The circuit is supplied at 3.6 V, enabling the stacking of three transistors and the resistive load, achieving the optimum collector current for maximum transit frequency. Reducing the gain and phase imbalance of the balun, capacitor $C_{1;1}$ is directly connected to the collector of $Q_{1;2}$ coupling the in-phase output to the input of $Q_{1;3}$ in the differential path. At the operation frequency of 53 GHz, the capacitance of 500 fF results in an impedance of 6 Ω in the coupling path. In simulation, with an input power of –10 dBm, this results in a difference between in-phase and differential output of less than 0.6 dB of gain, as shown in Fig. 3.22. The phase imbalance is lower than 9°, as depicted in Fig. 3.23. The achieved performance suffices to omit a second balancing stage, avoiding the associated DC power consumption. Inductive input matching

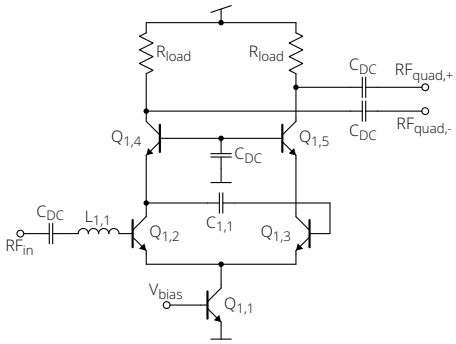


Figure 3.21: Schematic of the active balun at the input of the LO chain operating at around 53.25 GHz. [Ste6] © IEEE 2021

is used to optimize the gain of the balun [107]. Addressing the area consumption concerns when employing electromagnetic coils, it was found by studying and comparing the approaches in electromagnetic (EM) simulations that transmission line matching would result in an even larger footprint, while passive component matching introduces higher forward attenuation. By DC decoupling the input, the connection to other circuits is eased and enables simple biasing of $Q_{1;2}$. An input power sweep, shown in Fig. 3.24, was simulated at 53 GHz. A saturated output power of –4 dbm was reached at input power values larger than –5 dBm. The small-signal gain is approximately 9 dB. Together this shows the active balun to function as an effective input buffer.

Next, the LO signal is frequency multiplied by the PCPP multiplication stage shown in Fig. 3.25. Relying on the principle described in section 3.2, this is inspired by the circuit presented in section 3.3 and [97]. However, in contrast to the aforementioned quadrupler circuit, the revised PCPP quadrupler stage is optimized with a focus on low DC power consumption. This is realized by scaling the transistors to half the size and eliminating the additional voltage overhead required by the cascode architecture in Fig. 3.14. The resulting reduced output signal power is acceptable due to the high sensitivity of the ILO output amplifier described in the next section. Special care was taken with

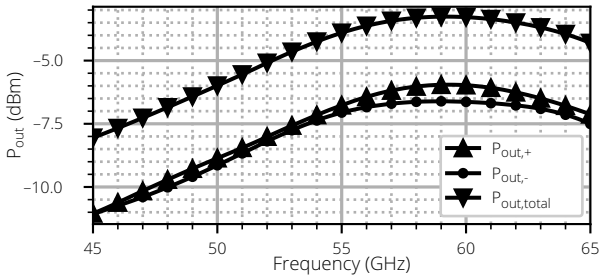


Figure 3.22: Simulated output power spectrum of the active balun shown in Fig. 3.21 over the input frequency at an input power of −10 dBm.

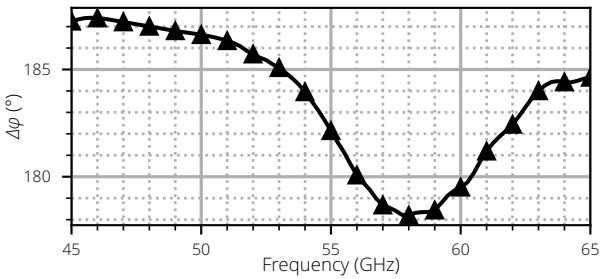


Figure 3.23: Simulated phase behavior of the active balun shown in Fig. 3.21 over the input frequency.

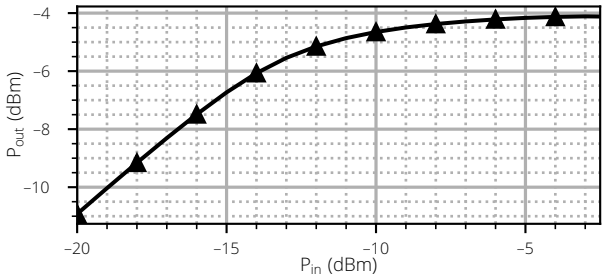


Figure 3.24: Simulated input power sweep of the active balun shown in Fig. 3.21 at 53 GHz.

the input feeding network of the PCPP stage. Differential and in-phase signals cross before being DC decoupled by the capacitors $C_{2;1,\ldots,4}$ enabling the separation of the DC bias points with $Q_{2;1,2}$ and $Q_{2;3,4}$ sharing the same bias voltage. The feed lines $TL_{2;5,\ldots,8}$ are optimized in layout and length by EM simulations targeting the fourth harmonic signal. This is especially crucial as, in contrast to the ideal model, described in section 3.2, the input impedances of the stacked transistors differ, causing deviating transient base-emitter voltages and therefore resulting in the need for adjusted matching to achieve optimal performance. The parasitic creation of other harmonics is less important in this design step as the following ILO stage inherently bandpass filters the quadrupler output signal. At the output, a transmission line network $TL_{2;1,\ldots,4}$ provides inter-stage matching optimized for the fourth harmonic with the second harmonic being suppressed by the open transmission line $TL_{2;4}$. The resulting layout is shown in Fig. 3.26.
Finally, at the output of the studied signal chain, the signal power is amplified by an ILO. A block diagram for a general feedback based oscillator is given in Fig. 3.27, resulting in the transfer function

$$\frac{\underline{V}_{\text{out}}}{\underline{V}_{\text{in}}} = \frac{\underline{A}(j\omega)}{1 - \underline{H}(j\omega) \cdot \underline{A}(j\omega)}. \tag{3.30}$$

ILO architectures build on this concept and extend it by introducing an injection source. The principle of injecting a signal of frequency ω_{inj} into an oscillator core resonating at ω_{osc} was studied as early as

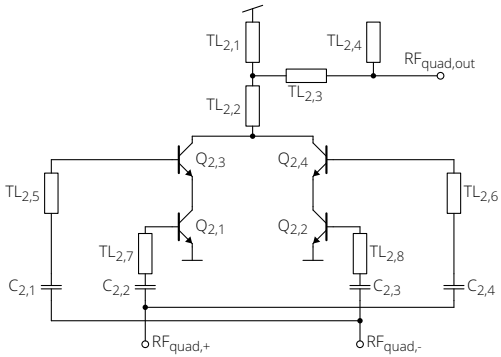


Figure 3.25: Schematic of the 53.25 GHz to 213 GHz PCPP quadrupler. [Ste6] © IEEE 2021

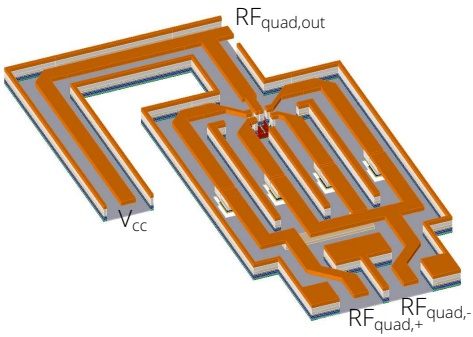


Figure 3.26: 3D view of the designed PCPP quadrupler circuit with an optimized input network.

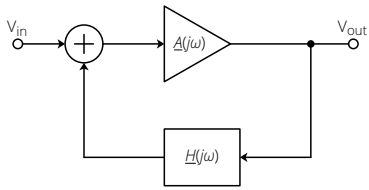


Figure 3.27: General block diagram of an amplifier based sinusoidal oscillator with positive feedback.

1946 in [113] and further investigated up to recent years [109], [114]. Shown in Fig. 3.28a is the basic concept of injection locking. Here, a parallel LCR resonator tank is assumed to operate in resonance at $\omega_{osc} = 1/\sqrt{LC}$. Due to the cancellation of the effects of the inductance and capacitance, no phase shift is introduced by the resonator while both the ideal inverter and the transistor in emitter configuration contribute a 180° phase shift resulting in 360° of phase shift in the feedback path. Given sufficient gain in the system in Fig. 3.28a, at $\varphi_0 = 0$, the circuit will thus oscillate at the resonance frequency of the LCR tank, according to the Barkhausen phase criterion Eq. 3.1 [38], [82]. When a phase shift $\varphi_0 \neq 0$ is introduced to the system, however, the phase condition is not met anymore for ω_{osc}. Therefore, the oscillation frequency changes so that a phase contribution of the LCR tank compensates φ_0. In the analyzed architecture, the phase shift is realized by introducing a sinusoidal signal I_{inj}, as shown in Fig. 3.28b, which, given appropriate frequency ω_{inj} and amplitude, forces the circuit to oscillate at the injected frequency, thus achieving injection locking [109]. The locking process is completed when the phase angle between injected signal and output signal is constant. *Adler* [113] formulates three conditions to be met to produce injection locking [114]:

1. The injected frequency must be close to the pass band of the resonant circuit.

2. The time constant of the feedback amplitude control must be small in comparison to the inverse of the frequency difference of the oscillator and the injected signal. This is always ensured for instantaneous circuits like the one presented.

3. The locking signal is much smaller than the output signal.

The resulting locking range for injection locked oscillators [109], [114]

$$\omega_L \approx \frac{\omega_{osc}}{2Q} \frac{I_{inj}}{I_{out}} \tag{3.31}$$

is determined by the quality factor of the oscillator Q as well as the relation of the magnitudes of the injected current and output current. In turn, this translates to the necessary injection amplitude in terms of the distance between the injected and oscillator free-running frequency [114]

$$\frac{I_{inj}}{I_{out}} > \left| \frac{\omega_{osc} - \omega_{inj}}{\frac{\omega_{osc}}{2Q}} \right| . \tag{3.32}$$

The sensitivity of an ILO circuit is defined as the necessary injection power to achieve a fully locked state resulting in maximum output power. A small injection signal suffices when the injection frequency approaches the free-running frequency, while higher signal power is needed to achieve injection locking for larger frequency deviations. This is due to less gain in the signal chain shown in Fig. 3.27 further away from the pass band center frequency.

The presented circuit, shown in Fig. 3.29, employs an adapted Colpitts oscillator architecture [11], [108]. A simplified view illustrating this is given in Fig. 3.30. At the input, a bipolar cascode, consisting of the transistors $Q_{3;1,2}$ with an electromagnetic transmission line output network $TL_{3;1,2}$, acts as an input amplifier and isolates the sensitive oscillator core from surrounding circuitry. The circuit was optimized to trade off gain and power consumption to achieve a high sensitivity paired with high efficiency. Providing a constant input impedance to the oscillator core, this avoids potential frequency de-tuning. The buffered signal is then injected into the oscillator circuit. The oscillator core itself consists of the resonator elements $TL_{3;4}$ and $C_{3;1}$ together with the transistor $Q_{3;3}$. $TL_{3;3}$ is a $\lambda/4$-line, providing a DC path to ground, while presenting an open to the RF signal. A detailed 3D-view of the resulting layout is shown in Fig. 3.31. The resonator inductance is realized by $TL_{3;4}$ which is connected to ground via a process design kit (PDK) metal-insulator-metal (MIM) capacitor to enable the biasing of the transistor. At the emitter of $Q_{3;3}$, the capacitance is realized as a metal-oxide-metal (MOM) capacitor including all available metal layers. In contrast to MIM capacitors, this approach is chosen to avoid

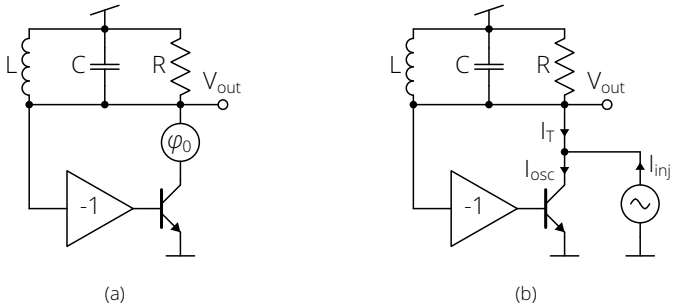


Figure 3.28: Systematic concept of an injection locked oscillator [109]. (a) General architecture with arbitrary phase shift φ_0. (b) ILO architecture with signal insertion to produce the required phase shift.

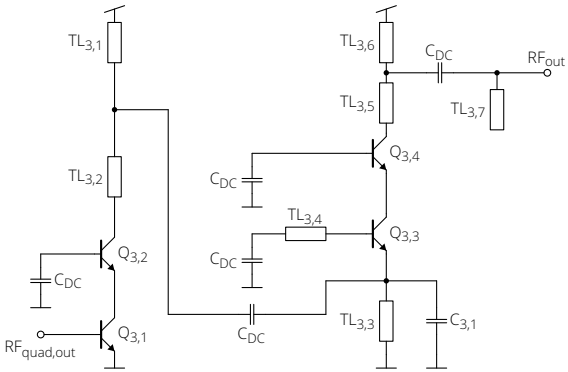


Figure 3.29: Schematic of the 213 GHz ILO output buffer. [Ste6] © IEEE 2021

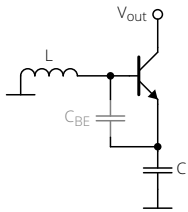


Figure 3.30: Simplified schematic of a common collector Colpitts oscillator.

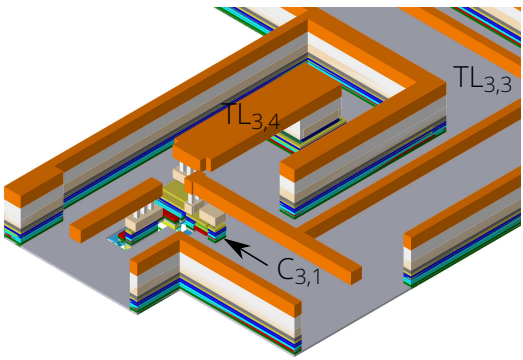


Figure 3.31: 3D image of the designed ILO core layout including the base stage output buffer. [Ste6] © IEEE 2021

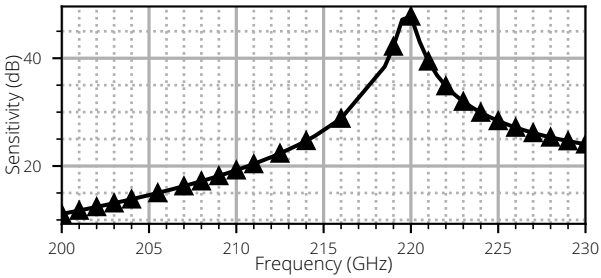


Figure 3.32: Simulated sensitivity of the ILO at the 1 dB compression point.

the associated, relatively large influence of process variations on very small capacitors. Additionally, this capacitor type is favorable as it is directly connected to the emitter of $Q_{3;3}$, which avoids inductive parasitics when connecting to MIM capacitor. As the circuit is designed for the use in a LO chain, which is inherently narrow band, the bandwidth is traded for large output power. With no additional discrete resistance added, this results in the simulated sensitivity shown in Fig. 3.32. This is extracted by sweeping the power at each input frequency up to the point where the 1 dB-compression point is reached in a stand-alone simulation using ideal 50 Ω terminals. Slight deviations to the real-world behavior of this metric are accepted to accommodate for convergence issues when simulating the full circuit. A sensitivity higher than 30 dB is reached from 216 GHz to 224 GHz. The output signal of the oscillator is amplified by $Q_{3;4}$ in base configuration, which is optimized for maximum output power. Finally, at the output, a transmission line based output network was optimized by a load-pull simulation to produce the maximum output power. Both the cascode buffer at the input as well as the oscillator and output buffer are supplied via zero-ohm lines [115] to achieve a well described transition from RF path to DC supply with very low impedance to ground for high frequencies.

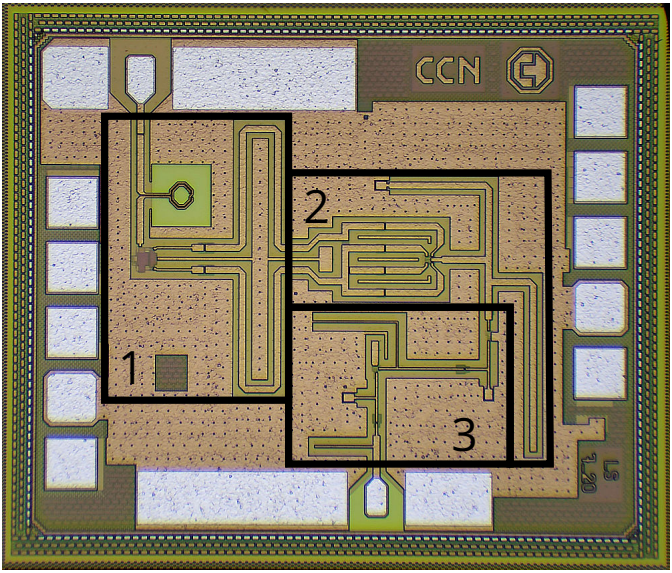


Figure 3.33: Chip microphotograph of the fabricated high output power LO chain measuring 825 µm × 983 µm = 0.811 mm^2. 1) Active balun.
2.) PCPP quadrupler. 3.) ILO buffer. [Ste6] © IEEE 2021

Simulation and Measurement Results

The fabricated circuit is shown in Fig. 3.33. The total chip area of 0.811 mm^2 splits into 0.110 mm^2 for the input balun (1), 0.095 mm^2 for the PCPP quadrupler (2) and 0.069 mm^2 for the ILO (3). In total, the three stages consume 92.9 mW. The measurement setup was extended to enable the characterization of all harmonics up to the fourth harmonic signal. This was enabled by a 67 GHz network analyzer in conjunction with multiple frequency extension setups using harmonic mixers theoretically covering a total band ranging from 0 GHz to 330 GHz. All setups were power calibrated using both coaxial and waveguide calorimeters with converter modules as reference

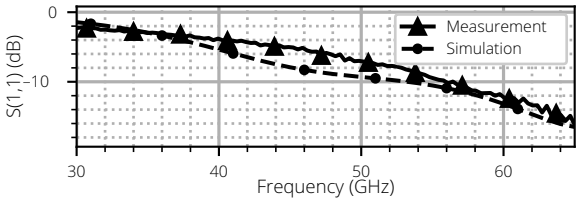


Figure 3.34: Measured and simulated small-signal input reflection factor of the LO chain over input frequency. [Ste6] © IEEE 2021

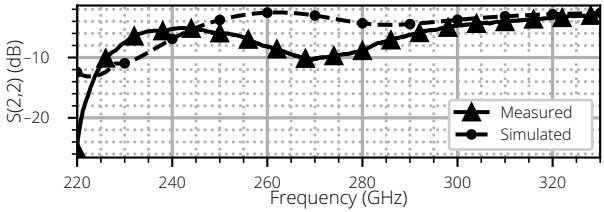


Figure 3.35: Measured and simulated small-signal output reflection factor of the LO chain over output frequency.

sources where needed. The probe characteristics were de-embedded according to the respective data sheets.
The matching behavior at the input is shown in Fig. 3.34. At the center frequency of 53 GHz at the input, a match of −8 dB is achieved. The simulation predicts the measured behavior. At the output a match of better than −5 dB is achieved as shown in Fig. 3.35. The simulation predicts the measurement well within a slight rotation in the complex plane. The behavior of the frequency harmonics results of the first through fourth harmonic are shown in Fig. 3.36 at −9 dBm input power. Here, the separate harmonics were characterized with a focus around the center frequency. The separate measurement setups experience a smooth transition at the crossing points. One particular example of this is the transition between the 140 GHz to 220 GHz setup and

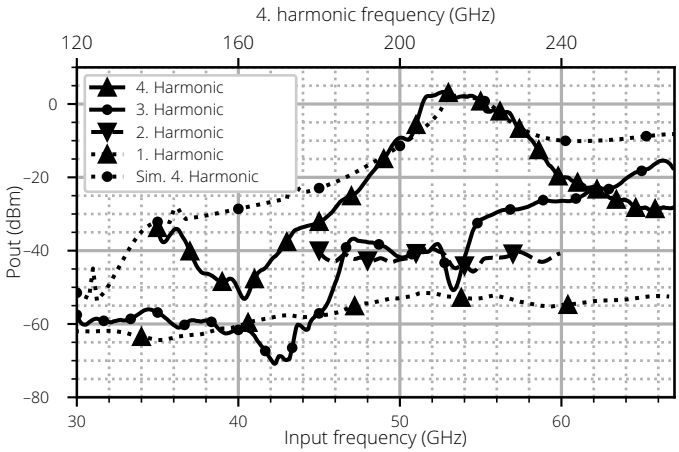


Figure 3.36: Measured output power of the first to fourth harmonic signal of the LO chain with the simulated fourth harmonic as a reference. The input power was set to −9 dBm. [Ste6] © IEEE 2021

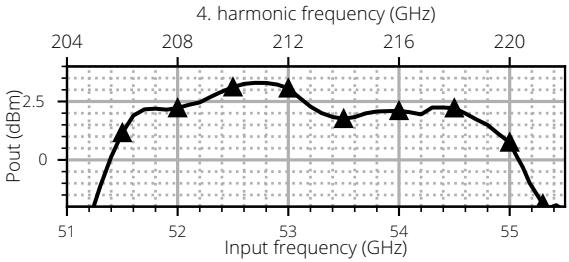


Figure 3.37: Magnified subsection of the measured fourth harmonic output power of the LO chain at –9 dBm. [Ste6] © IEEE 2021

the 220 GHz to 330 GHz setup of the fourth harmonic output power. At the center frequency of 212.9 GHz, the output power at the fourth harmonic is 2 dBm. With the simulated center frequency of 216.7 GHz, the deviation is limited to 1.8 %, illustrating a well-behaved model of both the sensitive quadrupler and ILO core.
Zooming into the measured passband of the fourth harmonic in Fig. 3.37, a 3-dB-bandwidth of 15.5 GHz is observed. An especially flat output power, at a power level of 2.4 dBm ± 1 dB, is achieved from 206.4 GHz to 219.2 GHz with the maximum output power at 211 GHz of 3.4 dBm. The flatness of the output spectrum can be explained by the high sensitivity of the ILO stage. With this, the signal power from the quadrupler stage is sufficient to drive the ILO into saturation in the depicted band. The total efficiency and power-added efficiency at the center frequency are

$$\eta_{\text{tot}} = \frac{P_{\text{out,lin}}}{P_{\text{DC}} + P_{\text{in,lin}}} = 1.7\% \tag{3.33}$$

and

$$\eta_{\text{PAE}} = \frac{P_{\text{out,lin}} - P_{\text{in,lin}}}{P_{\text{DC}}} = 1.6\%. \tag{3.34}$$

Extracted from the measurements shown in Fig. 3.36, the suppression of the first, second and third spurious harmonics are depicted in Fig. 3.38. At the center frequency, more than 45 dB of suppression of all harmonics is achieved. Over the entire 3-dB-bandwidth of

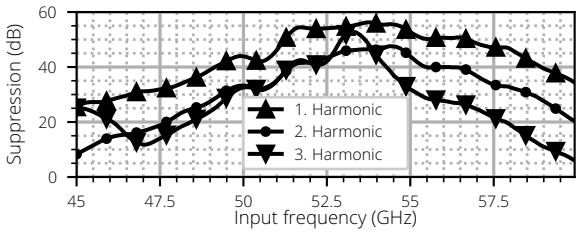


Figure 3.38: Harmonic suppression measurement results of the LO chain of the first, second and third harmonics over input frequency at –9 dBm of input power. [Ste6] © IEEE 2021

the fourth harmonic signal, all measured spurious harmonics are suppressed by more than 30 dB.

The input power is swept at 53 GHz at the input producing a 212 GHz signal at the output, shown in Fig. 3.39. After a linear rise of the output power, saturation is achieved at an input power of –9.8 dBm resulting in 2 dBm at the output and 11.8 dB of saturated gain. This shows that the analysis above was done within the saturated region.

Conclusion

The prove of concept of a PCPP frequency quadrupling high gain and high output power LO chain operating at 212.9 GHz was presented. This extends the PCPP approach of frequency multiplication by four to efficiently provide large output power to directly drive subsequent modulator stages. A theoretical analysis of the locking behavior of ILOs, with the locking range depending directly on the injected signal amplitude, allows a trade-off in DC power allocation between the frequency quadrupler and ILO buffer stage. Since a small bandwidth is sufficient in this LO generation circuit, the output power requirement of the quadrupler stage is reduced which allows this stage to be biased for low DC power consumption without decreasing the overall system output power. This maximizes the efficiency of the combined LO chain.

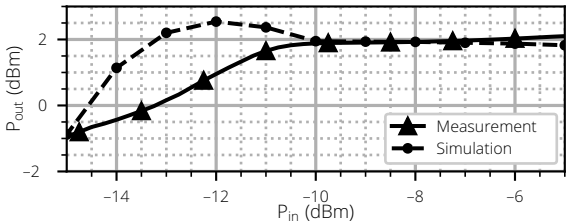


Figure 3.39: Measured and simulated output power of the fourth harmonic of the LO chain at the output center frequency of 212 GHz for an input power sweep from −15 dBm to −5 dBm. [Ste6] © IEEE 2021

Compared to the state of the art, shown in Tab. 3.2, the described system shows one of the largest saturated output powers at 2 dBm. Increasing the conversion gain to 11.8 dB results in an improvement of more than 6 dB in comparison to [95]. The low DC power consumption of 92.9mW produces a competitive total power efficiency of 1.7 %. A power-added efficiency (PAE) of 1.6 % increases the state of the art by 28.7 % [94]. A high degree of signal purity is maintained with a harmonic suppression larger than 30 dB and a maximum of 45 dB at the center frequency.

Table 3.2: State of the art of frequency multiplication circuits capable of LO generation at around 200 GHz.

	This	[Ste1]	[92]	[94]	[95]	[96]
Architecture	Buffered PCPP	PCPP	Diode	Gilbert	Adj. PP	PP
Multiplication factor	4	4	2	2 x 2	4	2 x 2
Technology	0.13 µm SiGe	0.13 µm SiGe	GaAs	0.13 µm SiGe	0.13 µm SiGe	0.13 µm SiGe
Center frequency (GHz)	212.9	255.5	212.5	150	191.5	186
Relative bandwidth (%)	7.3	5	21.2	28.0	19.3	36.6
$P_{out,sat}$ (dBm)	2	-8.4	13.3	2.2	-6	-1
$Gain_{sat}$ (dB)	11.8	-4.4	-6.7	5	5.3	0
Harmonic suppression (dB)	>30	10	-	<30	28-40	52
P_{DC} (mW)	92.9	22.4	89	100	63	45
Total efficiency (%)	1.7	0.6	11.3	1.6	0.4	1.7
Power-added efficiency (%)	1.6	<0	<0	1.1	0.3	0
Area (mm^2)	0.811	1.02	-	0.61	0.78	1.3

4. Array Systems and Dynamic Beam Steering

When multiple antennas are placed spatially close together and transmit the same signal, the propagating fields of the separate antennas are superimposed forming an antenna array system. From this results a new radiation characteristic diverging from the radiation pattern of a single antenna. Typically, the main lobe, which is the lobe propagating in the direction of the normal vector on the antenna plane, is narrowed in comparison to a unit antenna. When the antenna spacing is chosen correctly, other propagation directions, so called side lobes or grating lobes, are attenuated due to destructive interference. Depending on the application and its specific requirements, the array size can be chosen both in x and y direction resulting in a $(x' \times y')$-array, where $x', y' \in \mathbb{N}$ with $N_{\text{arr}} = x' \cdot y'$ separate array elements.
Beam steering is the static or dynamic control of the propagation vector of the main lobe of an antenna array system by influencing the phases (and or amplitudes) of the signals supplied to the separate array elements. A simplified view of a steerable $(1 \times x')$-linear array [116] is given in Fig. 4.1. The steering capability is achieved via the control units $\text{ctrl}_{1,2,\ldots,N_{\text{arr}}}$, which are further discussed in section 4.1.
With transmission speed requirements resulting in channel frequencies constantly increasing to accommodate the necessary bandwidths, modern communication systems move towards ever higher frequencies producing an increased free space path loss (FSPL) [117]. This motivates the combination of the output power or gain of many parallel transmitters or receivers, respectively. Additionally, this results in high spatial diversity and the suppression of interfering signals. The

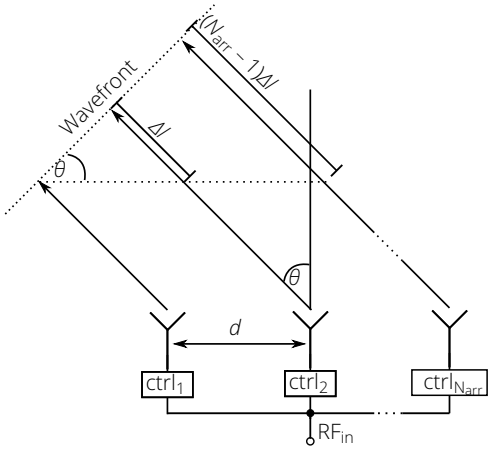


Figure 4.1: Simplified and generalized ($1 \times N_{arr}$)-array with arbitrary path control for beam steering.

signal-to-noise ratio (SNR) of the array system can be increased by focusing of the beam.

Many modern application including radio telescopes [118], [119], and mobile communication protocols like Fifth Generation Systems (5G) [120], [121], Sixth Generation Systems (6G) [26] and WiFi standards [122], can profit from beam steering capabilities. Enabled by high frequencies and, therefore, small antenna footprints, massive multiple-input multiple-output (MIMO) systems can produce very narrow beam shapes [123]. In mobile communication systems, the dynamic steering capabilities of antenna arrays are used to establish links with narrow beam widths by scanning many spacial directions [121], provide space division multiple access (SDMA) [120], full-dimension MIMO [124] in smart antennas and even allow tracking and sensing of people and objects [26], [122].

In the following, the main lobe is named the beam and is oriented in the beam direction θ as a deviation from the normal vector in degrees as noted in Fig. 4.1. Simplifying the analysis, this work will only cover linear arrays. These are characterized by antenna elements with equidistant spacing and linear alignment. The presented findings can simply

be extended to 2D antenna arrays as, given the array is of a rectangular shape, the behavior can be predicted by superimposing two perpendicular, linear arrays. The shape of the propagation pattern of linear antenna arrays is described by the normalized array factor AF [116], [125]

$$AF(\theta_{\text{obs}}) = \frac{\sin\left(\frac{N_{\text{arr}}\pi d}{\lambda}\left[\sin(\theta_{\text{obs}}) - \sin(\theta)\right]\right)}{N_{\text{arr}}\sin\left(\frac{\pi d}{\lambda}\left[\sin(\theta_{\text{obs}}) - \sin(\theta)\right]\right)} \tag{4.1}$$

with the beam direction θ, the observed direction θ_{obs} and the distance between antenna elements d. The resulting normalized array factors at $d = \frac{\lambda}{2}$ for both $\theta = 0°$ and $\theta = 20°$ are depicted in Fig. 4.2 for a single tone signal. It can be observed, that the array factor gets narrower for larger array systems. This is especially prominent in the first step between $N_{\text{arr}} = 2$ and $N_{\text{arr}} = 4$. The array factor is symmetrical around 0° in the case of no applied beam steering as shown in Fig. 4.2a. All side lobes decrease monotonously for large observation directions. At larger beam directions, more power is shifted towards the side lobes as depicted in Fig. 4.2b. Nevertheless, this illustrates the capabilities of an array system to focus the power of many elements into narrow spacial directions compared to a single antenna transmitter. The literature presents many mm-wave systems combining and steering the output power or receiver gain in this way [26], [120], [121].

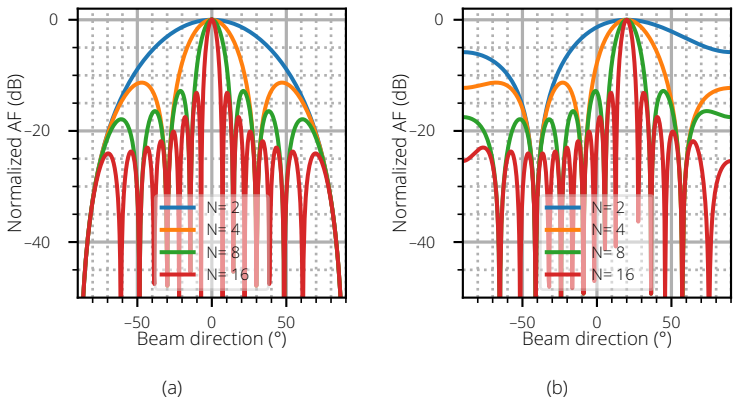


Figure 4.2: Theoretical calculation of the normalized array factor *AF* for linear antenna arrays with $N_{\text{arr}} = [2, 4, 8, 16]$ antenna elements and an antenna spacing of $d = \lambda/2$. (a) At $\theta = 0°$, the array factor is symmetrical around 0°. (b) At a beam direction of $\theta = 20°$, the side lobe power increases.

4.1. Theoretical Analysis of Beam Steering

Some of the theoretical analyses, deductions and equations in this section are based on, or published in [Ste3].
In the following, different approaches for circuits enabling beam steering, specifically time-delayed and phase-delayed beam steering, will be discussed weighing both advantages and drawbacks. These can then be used in the control units introduced in Fig. 4.1. Additionally, the influence of the spacing of the antenna elements as well as different architectures of beam steering systems are analyzed. All numerical results are calculated for a minimum example array sized (2×1).

4.1.1. Time-Delayed Beam Steering

Time delay based systems use digitally, tuneable delay cells of finite resolution as the control units introduced in Fig. 4.1. These are typically placed in line with the high frequency and broadband radio frequency (RF) path. At lower frequencies these can be realized as inverter chains [126], while delay lines in conjunction with RF switches are preferred in the mm-wave spectrum, or when very high bandwidths are needed [119], [127]–[129]. However, delay lines typically require large silicon area to incorporate RF-switches and delay lines, providing sufficient time delay. Additionally, due to the long necessary transmission lines and mismatch in the RF-switches, substantial attenuation can be introduced [128].
As an ideal time delay based system directly synthesizes the path delay $\Delta\tau$ occurring from an antenna further away from the target, it mimics a spacial rotation of the antenna array. With Fig. 4.1 as a simple example of a linear array, the time delay between two neighboring antennas to produce the expected wavefront calculates to

$$\Delta\tau = \frac{\Delta l}{c} = \frac{d}{c} \cdot \sin(\theta). \tag{4.2}$$

This means that path 1 has to be delayed by $\Delta\tau$ to reach the wavefront in phase with path 2. Accordingly, every path i has to be time delayed by

$$\Delta\tau_i = (n - i) \cdot \Delta\tau. \tag{4.3}$$

This results in the steering direction

$$\theta_{\mathrm{TTD}} = \arcsin\left(\frac{c\Delta\tau}{d}\right), \tag{4.4}$$

with the speed of light c, as the approximate propagation speed of electromagnetic waves in free air, the time delay difference between neighboring antenna elements $\Delta\tau$ and the distance between antenna elements d. Ideally, the delay values are constant for the entire band of operation of the time delay. The steering direction θ_{TTD}, is therefore independent of frequency as only the propagation delay is tuned.

4.1.2. Phase-Delayed Beam Steering

The second, and far more common way of beam steering is phase delayed beam steering [28], [130], [131]. Both passive [132]–[134] and active tuneable phase shifters [Ste5], [135], [136] are available for this application. One advantage, especially of active phase shifters, is the very low area consumption [Ste5], [135] which allows their usage in large, scaled array systems. Additionally, many phase shifters allow continuous phase and gain tuning only limited by the resolution of the digital-to-analog converter (DAC) setting the operation point of the active components. By introducing a constant phase shift over the full band of operation, this approach simulates the path delay between two neighboring antenna elements. For a single tone signal at frequency f the relation between a time delay and the corresponding phase shift can be written as

$$\Delta\varphi = 360^\circ \cdot f \cdot \Delta\tau. \tag{4.5}$$

Transforming for $\Delta\tau$ and inserting this in Eq. 4.4, produces

$$\theta_{\mathrm{phase}} = \arcsin\left(\frac{\lambda}{d}\frac{\Delta\varphi}{360^\circ}\right), \tag{4.6}$$

which displays the steering behavior of a phase-delayed system. As the wavelength λ remains in the expression, the steering behavior is frequency dependent. While the resulting steering is functionally identical for time-delayed and phase-delayed systems when analyzing single-tone signals, the behaviors diverge with increasing signal bandwidth. The resulting implications are discussed in the following section.

4.1.3. Analysis of Beam Squint in Broadband Phase-Delayed Arrays

Driven by the constant need for higher data transmission speeds, many current designs strive for ever higher bandwidths. When the entire frequency band of operation is phase shifted with a constant phase offset, this introduces varying beam angles for each infinitesimally small frequency bin, as can be deducted from Eq. 4.6 resulting in a widened main beam. This effect is called beam squint [137]. Combining beam squint of many degrees and mm-wave arrays only measuring some square millimeters in size, this can introduce substantial bandpass characteristics, thus leading to attenuation distortion and degrading the channel capacity [138]. Fig. 4.3 shows the steering behavior of an ideal time-delayed array structure in Fig. 4.3a and an ideal phase-delayed beam steering architecture in Fig. 4.3b according to Eq. 4.4 and Eq. 4.6. This is evaluated for an example signal ranging from 220 GHz to 250 GHz which equates to a relative bandwidth BW_{rel} of 12.8 %. This frequency range illustrates the significance of beam squint even at moderate bandwidths. The ideal time-delayed steering system, shown in Fig. 4.3a, points the main beam of all frequency components in the same direction for all steering inputs. Contrarily, the phase-delayed architecture results in beam squint which is depicted in detail in Fig. 4.4, exceeding 5° at approximately 100° of phase shift and 11° at 150° of phase shift between neighboring sub-antennas. To simplify further analysis and reduce the number of variables, the distance between the antenna elements d is fixed at half the wavelength of the center frequency f_c of the studied band at $d = \frac{\lambda_c}{2}$. The rationale for choosing this value is given in section 4.1.5. With this condition, Eq. 4.6 is simplified according to the identity

$$\frac{\lambda}{d} \overset{d=\frac{\lambda_c}{2}}{=} 2\frac{\lambda}{\lambda_c} = 2\frac{f_c}{f} \tag{4.7}$$

$$\Rightarrow \theta_{\text{phase}} = \arcsin\left(\frac{f_c}{f}\frac{\Delta\varphi_c}{180°}\right). \tag{4.8}$$

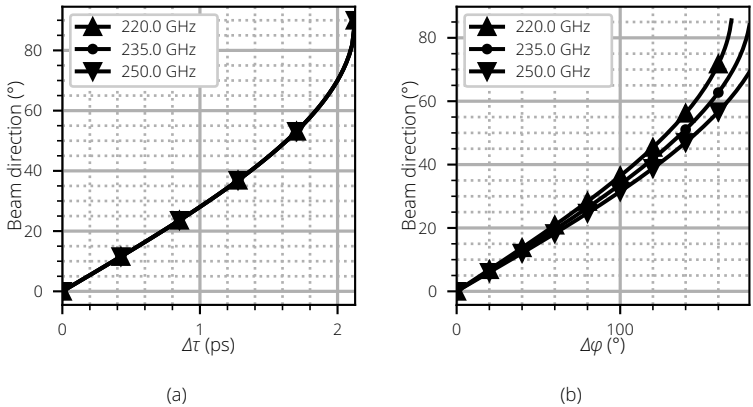


Figure 4.3: Comparison of the steering behavior of (a) a time-delayed and (b) a phase-delayed steering system. An example frequency band of 220 GHz to 250 GHz was chosen with a relative bandwidth of 12.8 %. [Ste3] © IEEE 2022

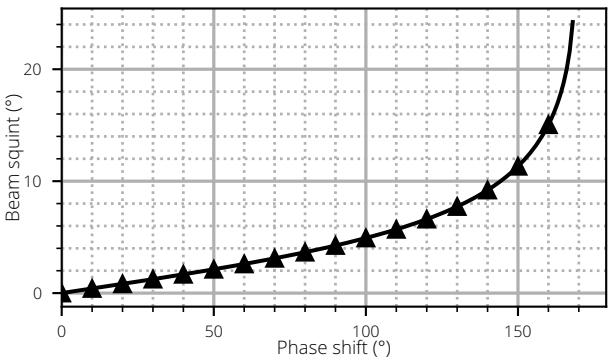


Figure 4.4: Beam squint resulting from phase-delayed steering of the 220 GHz to 250 GHz example signal according to Fig. 4.3b. [Ste3] © IEEE 2022

The resulting beam squint between the upper and frequency band limits f_u and f_l, symmetric to f_c, with the relative bandwidth BW_{rel}, $f_u = f_c\left(1 + \frac{BW_{rel}}{2}\right)$ and $f_l = f_c\left(1 - \frac{BW_{rel}}{2}\right)$

$$\begin{aligned}\Delta\theta^{\circ}_{squint} &= \arcsin\left(\frac{\Delta\varphi^{\circ}_{c} f_c}{180^{\circ} f_l}\right) - \arcsin\left(\frac{\Delta\varphi^{\circ}_{c} f_c}{180^{\circ} f_u}\right); \text{with } \Delta\varphi_c = 180^{\circ}\cdot\sin(\theta^{\circ}_{c}) \\ &= \arcsin\left(\frac{\sin(\theta^{\circ}_{c})}{\left(1 - \frac{BW_{rel}}{2}\right)}\right) - \arcsin\left(\frac{\sin(\theta^{\circ}_{c})}{\left(1 + \frac{BW_{rel}}{2}\right)}\right) \qquad (4.9)\end{aligned}$$

can be written strictly in terms of the phase-delayed steering direction at the center frequency θ_c and the relative bandwidth of the analyzed frequency band BW_{rel}. This produces an universal expression independent of the specific frequency of operation. The numeric results of Eq. 4.9 for relative bandwidths from 2 % to 30 % are depicted in Fig. 4.5 for beam directions ranging from –60° to 60°. From this it is clear, that a phase-delayed system can only produce significant steering angles together with small, single digit beam squint values for very small relative bandwidths of less than 10 % or very small beam directions. The severity of this effect was studied and is highlighted when analyzing the spacial width of the beam caused by the squinting behavior. Fig. 4.6 depicts possible beam directions for the f_l, f_c and f_u components. The beam direction deviations of the f_l and f_u components from the targeted θ_c

$$\theta_1 = \theta_c - \theta_u \qquad (4.10)$$

$$\theta_2 = \theta_l - \theta_c \qquad (4.11)$$

are defined first. Next, the resulting total width

$$w = d_1 + d_2 \qquad (4.12)$$

is introduced as the sum of the two deviation distances $d_{1,2}$ at the distance s from the array. Both of these distances can be calculated by the trigonometric relation

$$d_1 = s\cdot\tan(\theta_1) \qquad (4.13)$$

$$d_2 = s\cdot\tan(\theta_2). \qquad (4.14)$$

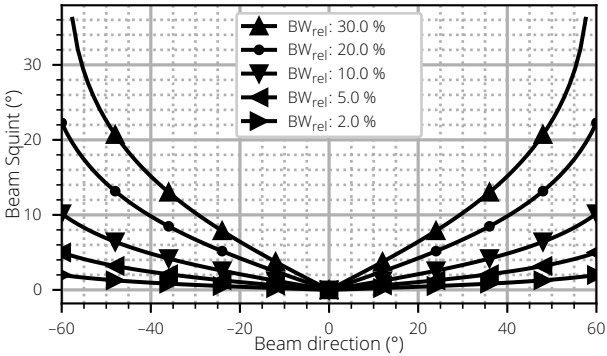


Figure 4.5: Phase-delay induced absolute beam squint in degrees over beam direction for relative bandwidths ranging from 2 % to 30 %. [Ste3] © IEEE 2022

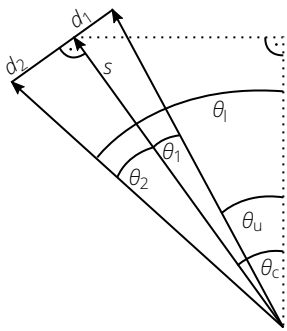


Figure 4.6: Sketch of the resulting the different beam directions caused by phase-delayed beam steering resulting in beam squinting producing a spatial beam width $w = d_1 + d_2$ at a distance s.

By inserting Eq. 4.13 and Eq. 4.14 in Eq. 4.12 an expression for the spacial beam width

$$\Rightarrow w = s\left(\tan(\theta_c - \theta_u) + \tan(\theta_l - \theta_c)\right) \tag{4.15}$$

depending on the respective beam directions of the frequency components in the evaluated frequency band is found. Finally, with the steering directions of the f_l and f_u

$$\theta_l = \arcsin\left(\frac{\sin(\theta_c)}{1 - \frac{BW\text{–rel}}{2}}\right) \tag{4.16}$$

$$\theta_u = \arcsin\left(\frac{\sin(\theta_c)}{1 + \frac{BW\text{–rel}}{2}}\right) \tag{4.17}$$

expressed in terms of the goal beam direction referred to the center frequency θ_c and inserted in Eq. 4.15 the spacial beam width

$$w = s\left(\tan\left(\theta_c - \arcsin\left(\frac{\sin(\theta_c)}{1 + \frac{BW_{rel}}{2}}\right)\right) + \tan\left(\arcsin\left(\frac{\sin(\theta_c)}{1 - \frac{BW_{rel}}{2}}\right) - \theta_c\right)\right). \tag{4.18}$$

can be expressed as a function of only the relative bandwidth and the beam direction of the center frequency. Fig. 4.7 depicts a numeric example for the same signal as above ranging from 220 GHz to 250 GHz. The resulting normalized beam pattern is illustrated in Fig. 4.7a. At $s = 5$ m of distance and steering directions larger than 40°, the beam is calculated by Eq. 4.18 to be wider than 0.5 m as shown in Fig. 4.7b. As typical mm-wave antenna arrays in this frequency range measure some millimeters in width, this causes a strong narrow-band band-pass characteristic in the channel.

4.1.4. Hybrid Digital-Analog Beam Steering

For completeness, hybrid digital-analog systems combine the digital precoding of the base-band with analog phase control [139]–[141]. Dynamic configurations connecting multiple RF chains with all array antennas or antenna subsets [142], enable adaptable MIMO applications at the cost of computational overhead and increased circuit design

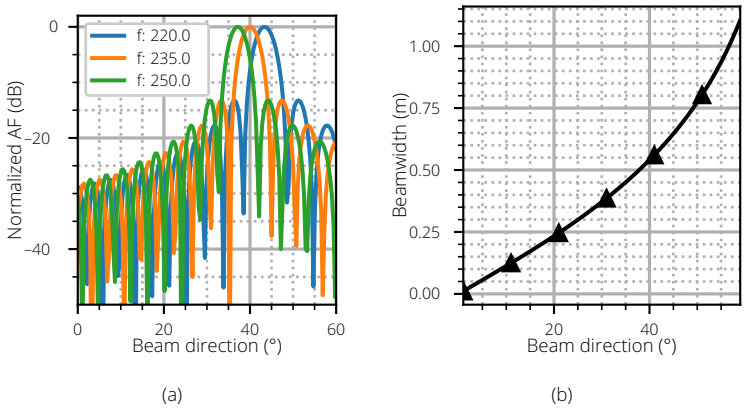


Figure 4.7: Analysis of the beam width of an ideal phase-delayed array due to beam squinting caused by phase-delayed steering for a signal ranging from 220 GHz to 250 GHz with a relative bandwidth of 12.8 %. (a) Normalized array factors at 40° goal steering direction. (b) Resulting spatial beam width at a distance of $s = 5$ m.

complexity. Thus, this technique is especially valuable in modern communication networks, where the antenna array can be dynamically adjusted to its momentary demands [140], [143], [144]. However, these require complex analog-to-digital converters (ADCs) and DACs to employ the associated algorithms requiring high DC power and complicate the use in systems with very high data rates.

4.1.5. Antenna Spacing

With the understanding of the steering behavior of both phase-delayed and time-delayed arrays the spacing of the antennas within an array, impacting the array characteristics and performance, can be analyzed. The focus of this work will be put on the more common uniformly organized antenna arrays [20]. However, the literature presents algorithms working with non-uniformly spaced antennas [145] and distributed systems of physically independent transmitters [146]–[148]. The following deductions are done for single-tones signals resulting in equivalent effects for phase-delayed and time-delayed systems. Following [137], grating lobes appear when the argument of Eq. 4.6 produces more than one real result due to the periodicity of the phase, resulting in multiple valid beam directions of constructive interference

$$\theta_{\text{grating}} = \arcsin\left(\frac{(i \cdot 360^\circ + \Delta\varphi)}{360^\circ}\frac{\lambda}{d}\right); \forall\, i \geq 0. \tag{4.19}$$

This reduces the array's directivity, and can cause issues like multi-path propagation which can deteriorate the data link quality of the user or other users. However, this issue is mitigated at mm-wave and sub-THz links due to the high free-space and atmospheric attenuation [149]. From Eq. 4.19, the condition to avoid grating lobes is calculated as

$$\left|\frac{(i \cdot 360^\circ + \Delta\varphi)}{360^\circ}\frac{\lambda}{d}\right| > 1; \forall i \geq 1, \tag{4.20}$$

leaving the only real result of Eq. 4.19 at $i = 0$. This can then be transformed to

$$d_{\text{max}} = \frac{\lambda}{1 + |\sin(\theta_{\text{max}})|} \tag{4.21}$$

with the maximum wanted steering direction θ_{max} and the allowed maximum antenna distance d_{max} for which no grating lobes appear.

Accordingly, full $\pm 90^\circ$ of beam direction control can only be achieved for $d \leq \frac{\lambda}{2}$. Even though smaller antenna spacing would relax the requirements on the maximum phase shift or time delay needed for a certain beam direction, in practice, this is often not practical due to the physical size of the antennas and transmitter circuitry, as well as the interest of maximizing the total array aperture. In specific applications it is possible to trade of steering angle for relaxed antenna spacing accompanied by a larger array aperture while also limiting grating lobes.

4.1.6. Analysis of Steered Array Configurations

Different beam steering architectures [150] are capable to produce precise beam steering are presented in Fig. 4.8. Either architecture can employ both phase-delayed and time-delayed. However, time-delayed systems, due to their larger area consumption and higher design complexity, should only be considered when the direction control stage is in the path of the broadband modulated signal.
The RF beam steering architecture is the least complex architecture and, thus, commonly used [151]. As shown in Fig. 4.8a, the base-band signal is first modulated and up-converted. A separate delay is applied for every antenna element in the RF band. One advantage is the use of only one modulator stage. In the case of a transmitter, the modulator needs to satisfy the requirements resulting from the used modulation scheme as well as minimize noise for optimized signal quality. The design complexity is shifted towards the beam control circuitry. Special care must be taken to produce minimal magnitude variations between the paths to optimize the array performance [152].
The beam control can also be introduced into the local oscillator (LO)-chain which is depicted in Fig. 4.8b and realized in [Ste4], [153]. Every transmitter path features a separate modulator which is fed by both the baseband (BB)-signal and the separately controlled LO-signal. Here, the requirements towards the beam control circuits are reduced in terms of transmission magnitude variation, non-linearity and noise performance. Additionally, this can reduce the necessary maximum phase shift when frequency multiplication circuits are used in the LO-chain. This will be further discussed in section 4.2. Finally, the bandwidth requirement of the beam steering circuit is strongly reduced. The major disadvantage of this approach is the increased number of

circuits elements and the subsequently larger silicon area and potentially higher power consumption from a systematic point of view depending on the application. By calculating the output signal of an ideal up-conversion mixer fed with a intermediate frequency (IF) signal oscillating a ω_1 with an amplitude of 1 and a LO signal with a frequency of ω_{LO} and a phase-shift of $\Delta\varphi$ at an amplitude of 1

$$\sin(\omega_1 \cdot t) \cdot \sin(\omega_{LO} \cdot t + \Delta\varphi) = \tag{4.22}$$

$$\Leftrightarrow \quad \frac{1}{2}\left(\cos\left((\omega_{LO} - \omega_1) \cdot t + \Delta\varphi\right) - \cos\left((\omega_{LO} + \omega_1) \cdot t + \Delta\varphi\right)\right) \tag{4.23}$$

it can be shown, that the phase-shift introduced to the LO signal is present in both sidebands after mixing.
The IF beam steering architecture, shown in Fig. 4.8c, employs two mixing stages. The BB signal is first up-converted before the beam control circuits introduces the steering characteristic. This is then followed by another stage of up-conversion to produce the goal frequency band [154]. While this relaxes some beam control requirements, twice the number of mixers excludes this architecture for use in low-power and low-cost systems.
Lastly, Fig. 4.8d depicts the digital beam steering architecture. Here, a complex base-band signal is produced by a digital signal processor (DSP) which is then transformed to analog signals by high-speed DACs which are up-converted and fed to the antennas [155]. Depending on the transmission speeds, this method requires a very highly performant DSP and DAC architecture which commonly use large silicon area and DC power.

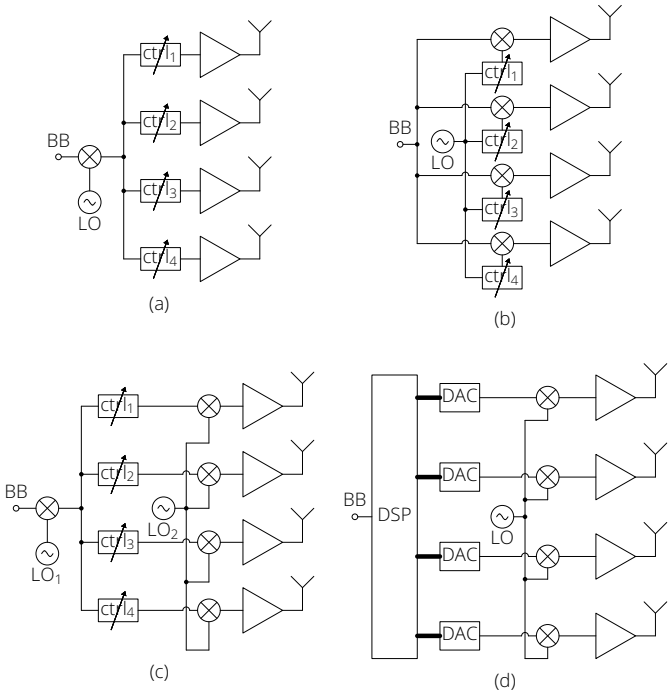


Figure 4.8: Simplified example beam steering circuit configurations for a (4 × 1)–linear array. (a) RF beam steering. (b) LO beam steering. (c) IF beam steering. (d) Digital beam steering.

4.2. Local Oscillator Phase Shifting with Vector-Modulator Phase Shifters

This section focuses on LO beam steering. The LO supply chain is a crucial element to the function of any transmitter. To maximize the transmitter performance, the LO chain has to be able to supply sufficient power to drive the modulator into saturation. At the same time the phase noise and noise floor must be minimized to avoid degradation of the SNR of transmissions. This is especially crucial when using modulation schemes like phase-shift keying (PSK) which encode the data stream in the phase information of the modulated signal [156]. Excessive phase noise, can spread the constellation diagram, degrading the bit error rate (BER) and lead to reciprocal mixing, thus, widening the spectrum. Additionally, the noise floor has direct degrading effect on the error vector magnitude (EVM) of the data transmission [81]. Referring to chapter 3, many mm-wave systems exploit frequency multiplication stages to up-convert a low-frequency oscillator signal to the channel frequency [30], [34]. By combining the phase-shifting stage with a frequency multiplication stage, the necessary phase control range is divided by the multiplication factor. With the frequency being defined as the derivative of the phase

$$\frac{d\varphi}{dt} = \omega = 2\pi f \tag{4.24}$$

the phase can be up-converted alongside the frequency. According to

$$N \cdot \varphi = N \left(\int_{\mathrm{T}} 2\pi f t dt \right) = 2\pi (N \cdot f)t + N \cdot \varphi_0, \tag{4.25}$$

the same multiplication factor N is applied to the phase as to the frequency during frequency multiplication.

4.2.1. Single-Voltage-Controlled Active Vector-Sum Phase Shifter

The presented circuit was published in [Ste5].
Enabled by the placement of the phase-shifting circuit in front of a frequency quadrupler, a phase shifter in the 60 GHz band with 90° of phase control with a frequency quadrupler circuit allows to design

a LO chain with 360° phase control in the mm-wave spectrum. The phase-shifter is optimized for maximum gain and output power, which completely eliminates the need for an additional LO input buffer. This eases the system design significantly and reduces overall power consumption.
Different realizations of phase shifters are capable of fulfilling the requirements in a LO chain. Common architectures can be split into digital and analog approaches. Delay line based circuits [157] and switched passive networks [129] are discrete, while reflection type phase shifters [133] and vector modulators [135] use analog control voltages. In larger systems, these are produced by DACs.
With both delay line and switched network type phase shifters generally consuming large silicon area, these were omitted from further investigation. The vector-sum modulator approach was then preferred to the reflection type architecture due to the high available gain and output power properties. Both characteristics are crucial to produce a phase-shifter circuit with enough gain and output power to act as an input buffer at the same time.
This architecture is able to produce output signals of varying amplitudes and phases by combining multiple different complex signal vectors. These are then fed to separate variable gain amplifiers (VGAs), which are biased to weigh the signals to produce a wanted amplitude and phase when adding the separate signals in the complex plane. Omitting the phase rotation caused by the frequency of the signals $S_{\mathrm{I,Q}}$ with the amplitudes $A_{\mathrm{I,Q}}$ results in

$$S_{\mathrm{I}} = A_{\mathrm{I}} \tag{4.26}$$

$$S_{\mathrm{Q}} = j \cdot A_{\mathrm{Q}} \tag{4.27}$$

$$S_{\mathrm{I}} + S_{\mathrm{Q}} = A_{\mathrm{I}} + j \cdot A_{\mathrm{Q}} \tag{4.28}$$

$$\mathrm{mag}(S_{\mathrm{I}} + S_{\mathrm{Q}}) = \sqrt{A_{\mathrm{I}}^2 + A_{\mathrm{Q}}^2} \tag{4.29}$$

$$\arg(S_{\mathrm{I}} + S_{\mathrm{Q}}) = \arctan\left(\frac{A_{\mathrm{Q}}}{A_{\mathrm{I}}}\right), \tag{4.30}$$

which enables the creation of any vector in the first quadrant of the complex plane. Assuming linear operation of the VGAs, amplitude and

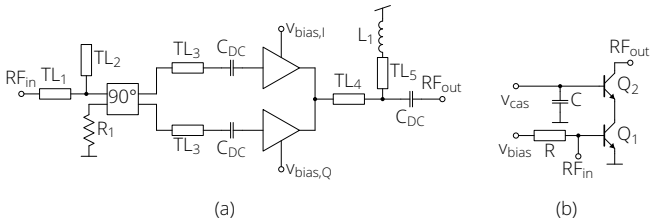


Figure 4.9: Simplified schematic of the proposed vector-sum phase-shifting system. (a) Schematic of the vector-sum phase-shifter. (b) Schematic of the cascode-based VGAs. [Ste5] © IEEE 2021

gain relations of the quadrature paths are linearly dependent as well, leading to

$$\frac{A_Q}{A_I} = \frac{G_Q}{G_I}. \tag{4.31}$$

From this, the phase of the combined vector

$$\varphi = \arctan\left(\frac{G_Q}{G_I}\right) \tag{4.32}$$

can be determined as a function of the gain of the VGAs.

Circuit Design

The proposed circuit is shown in Fig. 4.9a. Preceded by a transmission line input matching network, a quadrature stage feeds two VGAs. An output network employing both transmission lines as well as an discrete inductor is optimized for maximum output power.
There exist different approaches to quadrature signal generation. While active circuits capable to create these signals are available [158], a far more practical and, therefore, more common approach in the mm-wave spectrum is the use of passive structures like polyphase filters [159] or electromagnetic (EM) couplers [160], [161]. The schematic of a basic quadrature polyphase filter is shown in Fig. 4.10 with input and output loads depicted in gray. From this, the transfer functions of two signals

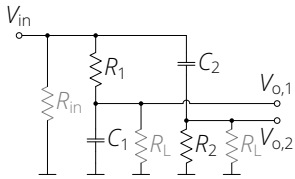


Figure 4.10: Schematic of a quadrature polyphase filter.

$$V_{o,1} = \frac{R_L}{R_1 + R_L + j\omega C_1 R_1 R_L} \tag{4.33}$$

$$V_{o,2} = \frac{1}{1 - j\frac{1}{\omega C_2 \frac{R_2 R_L}{R_2 + R_L}}} \tag{4.34}$$

show a first order lowpass characteristic at port 1 and a first order highpass characteristic at port 2. As the phase difference of 90° is to be combined with minimal magnitude imbalance, the 3 dB-frequencies of both filters are set to the center frequency. This creates –45° of phase shift at the lowpass and 45° at the highpass. At the same time each signal is ideally attenuated by 3 dB, excluding any parasitics. While the area consumption is very low, the high attenuation is a major drawback compared to coupler based architectures which generally exhibit less than 1 dB of attenuation [79], [162] caused by parasitics in the design. The broadside directional coupler based quadrature generation is chosen due to the reduced signal attenuation. As only one quadrature stage is needed, due to the reduced phase requirements discussed above, with a the coupler length of $\lambda/4$, resulting in a small footprint at mm-wave frequencies, the absolute area penalty is limited. Broadside coupling was chosen to improve the coupling factor and reduce the signal attenuation and magnitude imbalance. The resulting footprint is depicted in Fig. 4.11, with the simulated phase and magnitude behavior shown in Fig. 4.12. At 55 GHz, a maximum attenuation of 0.8 dB is achieved. The phase is nearly constant over the full EM simulation range centered at a value of 80°. This is a result of full system optimization including inter-stage networks and the VGAs.

A cascode architecture, as shown in Fig. 4.9b, was chosen to realize the VGAs. This combines high gain and output power while the high intrinsic reverse isolation separates the quadrature signal paths. By

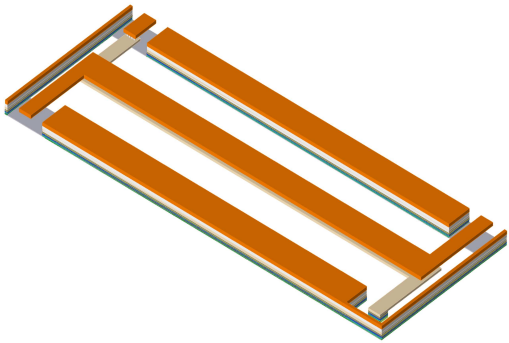
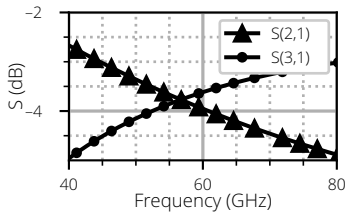
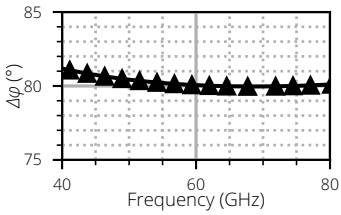


Figure 4.11: 3D view of the designed broadside directional coupler to produce orthogonal signals.



(a)



(b)

Figure 4.12: EM simulated behavior of the passive broadside directional coupler. (a) Magnitude of in-phase and quadrature signal. (b) Phase difference between the output signals.

shorting the outputs of the cascodes, the signals are superimposed producing the wanted signal vector. The gain of the single cascodes is adapted by varying the bias voltage of the transistors Q_1 in emitter configuration, keeping the steering complexity low. In large integrated systems, this is commonly done by complex DACs consuming high DC power and large silicon area. For use in beam steering applications, these must feature a high resolution to avoid quantization error resulting in additional side lobes [163]. To reduce this issue, a low-power and small differential stage, shown in Fig. 4.13, is devised to produce the in-phase and quadrature bias voltages from only one control voltage. A constant bias voltage v_{bias} of 1.75 V is applied to one side of the differential pair, while the voltage v_{in} is varied from 1.25 V to 2.25 V. In doing so, the small bias current I_0 can be dynamically allocated between the I- and Q-bias-paths. These currents are then mirrored by p-type metal-oxide (PMOS) active loads provided by the used BiCMOS technology. The PMOS current mirrors are scaled 8:1 to limit the differential core power consumption to 225 µW while the minimum size [63] bipolar transistors are fed appropriate collector currents consuming a total of 4.2 mW from a 2.6 V supply. This additional DC power is offset by the elimination of one high-precision DAC [164], [165] compared to two DACs in typical vector-sum circuits. Finally, the currents through $Q_{3,4}$ produce the bias voltages $v_{\text{bias,I,Q}}$ and are mirrored with a scaling factor of 2:1 to the VGAs. The collector current of $Q_{3,4}$

$$I_{\text{c}} = \frac{1}{2} I_0 \left[1 + \tanh\left(\frac{v_{\text{in}} - v_{\text{bias}}}{2V_{\text{T}}} \right) \right] \approx \frac{1}{2} I_0 \left(1 + \frac{v_{\text{in}} - v_{\text{bias}}}{2V_{\text{T}}} \right), \tag{4.35}$$

with $\tanh(x) \approx x$ for small x, can be assumed linearly dependent on the biasing input voltage to ease the interpretation. Additionally, the gain of a bipolar cascode

$$G_{\text{cas}} \approx -g_{\text{m,B}} \cdot Z_{\text{L}} = -\frac{I_{\text{c,op}}}{V_{\text{T}}} Z_{\text{L}}, \tag{4.36}$$

with the transconductance of the base stage transistor $g_{\text{m,B}}$, the operation point collector current $I_{\text{c,op}}$, the thermal voltage V_{T} and the load impedance Z_{L}, is linearly dependent on the collector current. Thus, Eq. 4.36 and 4.35 with Eq. 4.32 result in an output phase which approaches linear dependency on v_{in}. The output magnitude is constant

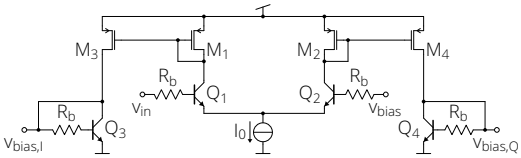


Figure 4.13: Schematic of the low-power differential circuit supplying the bias signals to the VGAs of the vector-sum phase-shifter in Fig. 4.9. [Ste5] © IEEE 2021

with phase but can be adjusted by modifying I_0, changing the maximum collector currents in the bipolar current mirrors and, therefore, the VGAs.

Simulation and Measurement Results

The manufactured circuit is shown in Fig. 4.14. A small total chip area of 0.388 mm^2 is used. In total, the chip consumes 12.1 mW from the 2.6 V supply voltage. At 4.8 mW, approximately one third of the total power consumption is allocated to the bias circuit depicted in Fig. 4.13. Shown in Fig. 4.15, the circuit is matched better than –15 dB for frequencies higher than 54 GHz. The simulation predicts the measurements well. Additionally, the maximum small signal gain of 12.4 dB is reached at 49 GHz with a steering voltage of $v_{\text{in}} = v_{\text{bias}} = 1.75$ V producing the same bias current in both the I and Q path VGAs. At ±0.9 dB, a flat gain curve is shown over the operating band of the circuit. The behavior of the measured circuit matches the simulation results within a loss of 1.5 dB of gain.
The measured phase states over frequency are depcited in Fig. 4.16. The goal phase steering capability of 90° is achieved from 44.4 GHz to 64.7 GHz limiting the overall band of operation. This results in a relative bandwidth of 37.2 %.
Measured at 60 GHz, the tuning behavior of the circuit is shown in Fig. 4.17. The small signal gain magnitude, depicted in Fig. 4.17a, is stable with little deviations from the mean value of ±0.375 dB across the full tuning range of v_{in} from 1.25 V to 2.25 V. Referenced to the 21 measured states of v_{in}, this produces a root mean square (RMS) magnitude error of less than 0.23 dB. Fig. 4.17b shows the phase tuning behavior.

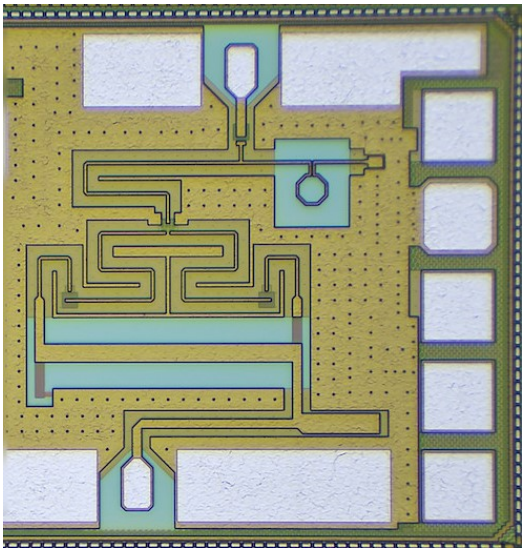


Figure 4.14: Microphotograph of the fabricated vector-sum phase-shifter measuring 604 µm x 642 µm=0.388 mm^2. [Ste5] © IEEE 2021

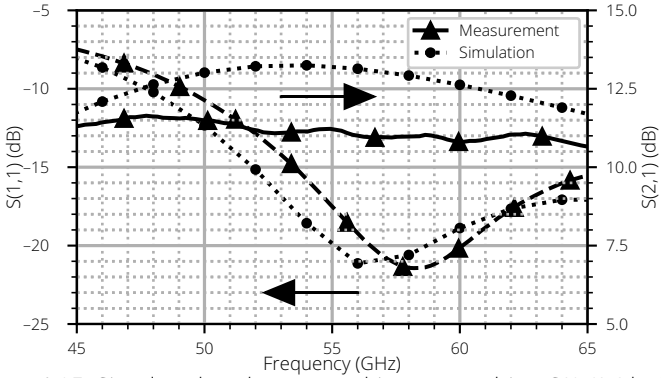


Figure 4.15: Simulated and measured input matching S(1,1) (dashed) and forward transmission factor S(2,1) (solid) of the vector-sum phase-shifter at the center steering voltage $v_{\text{in}} = v_{\text{bias}} = 1.75\,\text{V}$. The dotted lines show the simulation results. [Ste5] © IEEE 2021

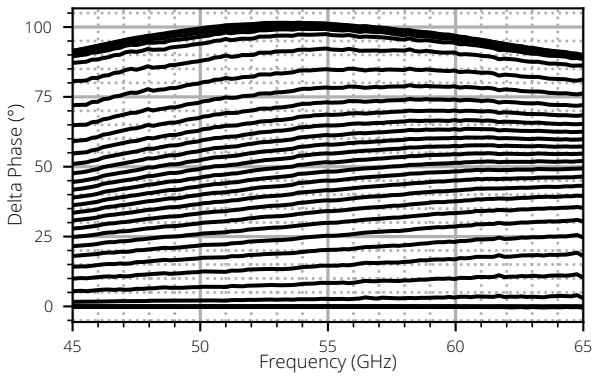


Figure 4.16: Measured phase values of all analyzed bias steps of the vector-sum phase-shifter over frequency. [Ste5] © IEEE 2021

The simulation matches the measured values very well within a maximum deviation of 5°. Additionally, the strong linear behavior confirms the deductions drawn from Eq. 4.32, 4.36 and 4.35. In total the circuit behaves predictably which simplifies the operation and integration in a larger system without complex calibration or compensation needed. Two easily computable analytical models predicting the phase behavior were extracted from the measurements in Fig. 4.17b and used as references. A linear fit

$$\Delta\varphi = k_{\mathrm{lin},1} \cdot v_{\mathrm{in}} + k_{\mathrm{lin},2} \tag{4.37}$$

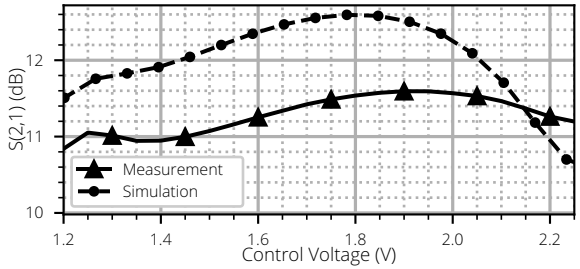
is found with $k_{\mathrm{lin},1} = 78.13\,^{\circ}\,\mathrm{V}^{-1}$ and $k_{\mathrm{lin},2} = -90.43^{\circ}$. Additionally, a function based on an arc-sine function in radians

$$\Delta\varphi = k_{\mathrm{asin},1} \cdot \arcsin(k_{\mathrm{asin},2} \cdot v_{\mathrm{in}} + k_{\mathrm{asin},3}) + k_{\mathrm{asin},4} \tag{4.38}$$

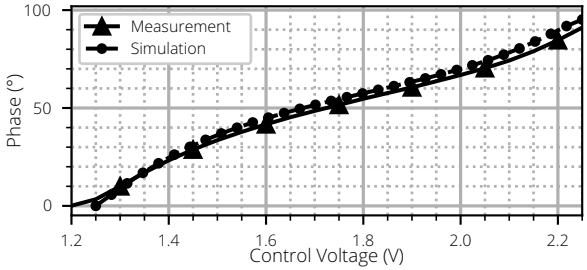
is fitted with $k_{\mathrm{asin},1} = 0.66$, $k_{\mathrm{asin},2} = 1.79\,\mathrm{V}^{-1}$, $k_{\mathrm{asin},3} = -3.22$ and $k_{\mathrm{asin},4} = 0.88\,\mathrm{rad}$. The deviation of the phase tuning behavior from these models is depicted in Fig. 4.18. The linear model results in a maximum deviation of 7°. Generally providing a deviation of less than 4°, this results in an RMS phase error of 2.63°. With an absolute error of less than 2°, the arcsin-model reduces the RMS phase error to 0.89°.
Finally, the large signal behavior is analyzed with a input power sweep at 55 GHz shown in Fig. 4.19 at *vin* = 1.75 V. Simulation and measurements are in good agreement. While $\mathrm{oP}_{1\mathrm{dB}}$=–0.8 dBm, the output power saturates at 5.0 dBm. This produces a power-added efficiency (PAE) of 6.3 %. Neglecting the biasing circuitry, which accounts for 39.2 % of the total power consumption, the core PAE is 10.6 %.

Conclusion

The proof of concept of a high-output-power 90° vector-sum phase shifter at 54.6 GHz with single-voltage tuning was presented. This circuit is especially useful in a LO chain of mm-wave phased arrays in conjunction with phase-frequency multiplication stages. Both polyphase and coupler based approaches to the required quadrature phase generation were studied. The higher area requirement of a coupler-based architecture is outweighed by the significantly lower signal attenuation. Another key finding is the possibility of precisely steering the phase with a single tuning voltage. A circuit providing a linear relation of input



(a)



(b)

Figure 4.17: Simulated and measured forward transmission factor of the vector-sum phase-shifter over the full tuning range $1.25\,\mathrm{V} \leq v_{\mathrm{in}} \leq 2.25\,\mathrm{V}$ at 60 GHz. (a) Magnitude over phase control voltage. (b) Output phase steering over the control voltage range. [Ste5] © IEEE 2021

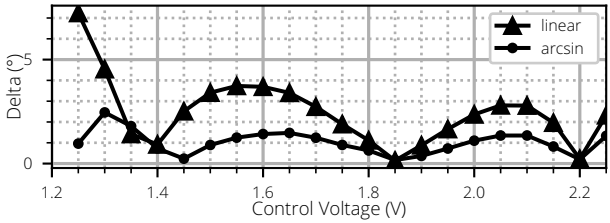


Figure 4.18: Analysis of the measured absolute phase deviation of the vector-sum phase-shifter from the ideal linear model in Eq. 4.37 and arc-sine behavior given in Eq. 4.38 for v_{in} from 1.25 V to 2.25 V at 60 GHz. [Ste5] © IEEE 2021

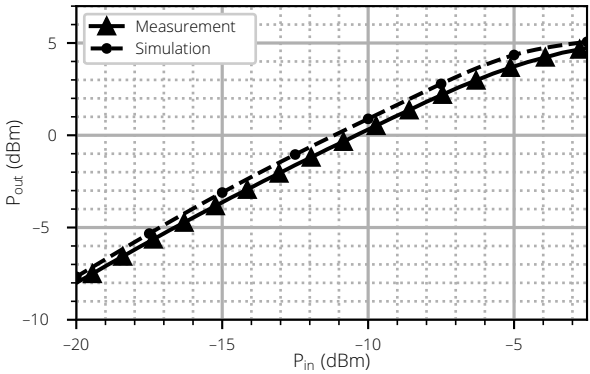


Figure 4.19: Simulated and measured output power for a input power sweep of the vector-sum phase-shifter at $v_{\text{in}} = 1.75$ V at 55 GHz. [Ste5] © IEEE 2021

voltage and phase is analytically studied and realized in the integrated circuit (IC). While the proposed DC bias circuit increases the power consumption of the measured IC, it can significantly reduce the overall power consumption in a larger system by reducing the total number of necessary DACs.

A comparison to the state of the art of mm-wave phase shifters in a similar frequency band is given in Tab. 4.1. At 20.3 GHz of bandwidth, the circuit shows the largest relative bandwidth at 37.2 % improving the state of the art by 68 % and tripling the relative bandwidth of 11.6 % of designs around 60 GHz [166], [167]. With a competitive small signal gain of 11.3 dB at 60 GHz, the highest oP_{1dB} of all compared circuits is achieved at –0.8 dBm. The very high saturated output power of 5.0 dBm stands out and allows direct driving of subsequent passive and active frequency multiplication circuits as described in chapter 3. In the interest of a fair comparison, the RMS phase error is evaluated after applying the multiplication factor of $N = 4$ to the measured results. This produces estimated values of 3.6° and 10.5° for the arc-sine and linear fit respectively which are competitive with the compared circuits. Finally, the high PAE of 6.29 % is a 30-fold improvement of the state of the art.

Table 4.1: State of the art of phase-shifter circuits at millimeter-wave frequencies.

	[Ste5]	[168]	[129]	[166]	[167]	[169]
Technology	0.13 µm SiGe BiCMOS	0.18 µm SiGe BiCMOS	0.13 µm SiGe BiCMOS	90 nm CMOS	90 nm CMOS	0.13 µm SiGe BiCMOS
Method	Vector Sum	Vector Sum	Delay + VGA	Delay + VGA	Vector Sum	Vector Sum
Phase range (°)	90	360	360	360	360	360
Center frequency (GHz)	54.6	87.5	80	60.5	60.5	180
Bandwidth (GHz)	20.3	19	8	7	7	40
Relative bandwidth (%)	37.2	21.7	10	11.6	11.6	22.2
S(2,1) (dB)	11.3	19	16.1	-8.4	1.1	-9.5
Δ Insertion loss (±)	0.375	0.5	-	3	0.75	0.9
RMS gain error (dB)	0.23	-	0,6 - 1,1	< 2	0.75 – 1.6	0.35
Δ Phase (±)	2/ 7	5	-	4.9	12.5	15
RMS Phase Error (°)	0.89/ 2.63	-	3,9 - 10,4	3.3	2.3 – 7.6	2
Output P_{1dB} (dBm)	-0.8	-	-11.9	-11.4	-9.7	-
P_{sat} (dBm)	5.0	-	-	-	-7[4]	-
DC power (mW)	12.1 (7.2)[2]	13.2[3]	32.94	31.2	19.8	8.6
PAE (%)[1]	6.3 (10.6)[2]	-	0.19	-1.79	0.01	-
Area (mm^2)	0.388	0.370[3]	1.28	0.799	0.610	0.375

[1] at 1-dB compression; [2] brackets assume power consumption without DC circuitry; [3] estimated; [4] maximum measured

4.2.2. 225 GHz Frequency Quadrupling LO Chain with Phase Control

The presented circuit was published in [Ste7].
With common LO chains suffering from high power consumption, low gain and small output power levels, this section exemplifies the performance potential of a high gain phase-shifter [Ste5] in conjunction with a high output power frequency quadrupler [Ste6]. The combination of high gain and low DC power consumption results in a highly efficient architecture. The LO chain enables direct driving of subsequent modulator stages, without additional amplification, while providing frequency multiplication and full range phase control to enable beam steering in a large array system.

Circuit Design

By combining a phase shifter [Ste5] operating at 55 GHz with a high-power frequency quadrupling stage [Ste6] to produce the targeted sub-THz frequency band, a high-output power, phase-steering LO chain is studied and devised. The resulting system architecture is shown in Fig. 4.20. Both the frequency and phase of the input signal are multiplied according to Eq. 4.25. Hereby, a phase-shift range of 90° at a frequency of 55 GHz can be up-converted to 360° at 220 GHz. Enabled by the large gain and high output power of the phase shifter, the quadrupler stage can be directly driven. Together, this allows the creation of the fourth harmonic of the input frequency at low input power levels. An injection-locked oscillator (ILO) at the output of the multiplication stage provides high output power and enables the driving of subsequent stages like modulators.

Simulation and Measurement Results

Two separate chips, containing the phase shifter and frequency quadrupler, were fitted to a printed circuit board (PCB), supplying the necessary DC voltages, and connected via a GSG bond interface. The resulting assembly is shown in Fig. 4.21. This results in a combined silicon area of 1.2 mm^2 which can be significantly reduced by further integrating the circuit. The total power consumption of 105 mW splits into 11.5 % for the phase-shifter and 88.5 % for the quadrupler. The

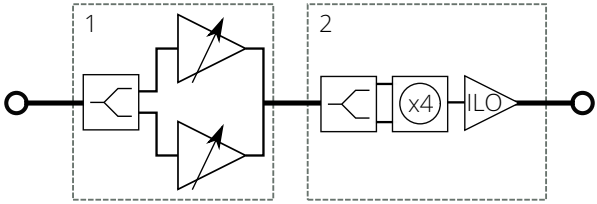


Figure 4.20: Proposed architecture of the phase-steering LO chain consisting of a 90° vector-sum phase shifter [Ste6] operating at 55 GHz in series with a high-power frequency quadrupler [Ste5]. [Ste7] © IEEE 2022

circuits were analyzed on a wafer prober. Combining a 67 GHz vector-network analyzer (VNA) with two frequency converter module setups allowing to characterize a continuous frequency band ranging from 140 GHz to 330 GHz. Each converter module, together with the associated S-bend and waveguide probe, was separately power calibrated and the probe losses, specified in the data-sheets, were de-embedded. The characterization of the phase behavior is challenging as the input frequency is up-converted by the frequency multiplier circuit resulting in different frequencies at in- and output. This is shown in Fig. 4.22 with the wave going into the circuit from Port P_1 $\underline{a}_1(f)$ and the wave exiting the circuit into P_2 at four times the frequency $\underline{b}_2(4f)$. This renders a typical S-parameter calibration and the measurement of the forward transmission factor

$$\arg(\underline{S}_{21}(f)) = \arg\left(\frac{\underline{b}_2(f)}{\underline{a}_1(f)}\right), \tag{4.39}$$

according to [38], impossible. Instead, the VNA was configured to supply a constant input power in the low frequency range while the absolute phase over frequency of the output signal $\arg(\underline{b}_2(4f))$ was recorded by a converter module. The correct frequency multiples at the in- and output were setup in the port configuration of the VNA. With the lowest tuning voltage setting as a reference measurement, relative phase differences were calculated post-measurement. Typically, both $\underline{a}_1(f)$ and $\underline{b}_2(f)$ are evaluated with the same LO signal in the VNA, removing the influence of the internal LO generator on the measurement values produced by Eq. 4.39. A drawback of measuring only the output wave

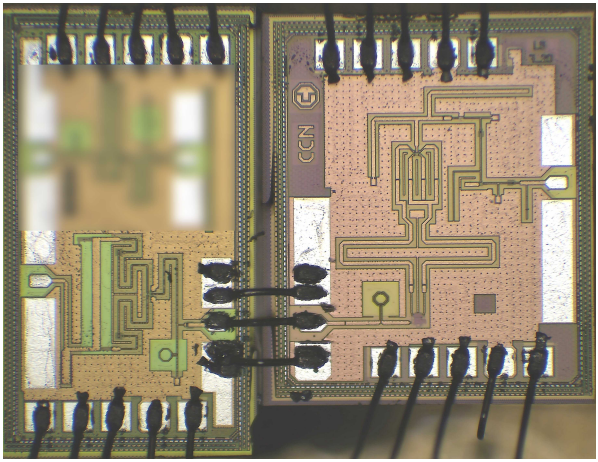


Figure 4.21: Photograph of the bonded phase shifter (left) and frequency quadrupler (right) chips producing the phase-steering LO chain. Including all pads, the phase shifter measures 604 µm × 642 µm and the quadrupler uses 825 µm × 983 µm of silicon area. [Ste7] © IEEE 2022

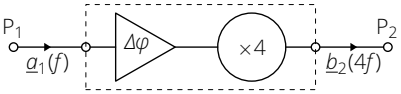


Figure 4.22: Simplified overview of the measurement ports for characterizing the phase-steering LO chain.

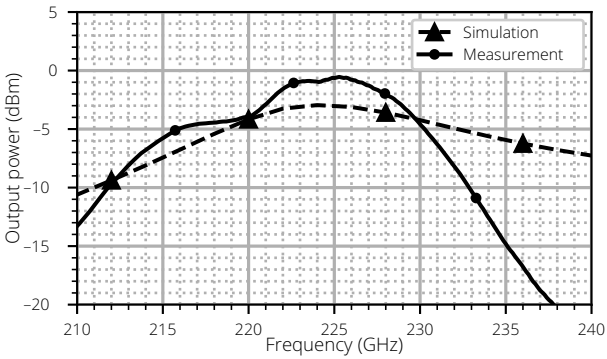


Figure 4.23: Simulated and measured mean output power of the phase-steering LO chain over frequency at an input power of $P_{\text{in}} = -17$ dBm. [Ste7] © IEEE 2022

$\underline{b}_2$ lies in the jitter and phase noise, introduced by the local oscillator within the VNA, not being compensated which can therefore deteriorate the measurement precision. Averaging 20 measurement runs per control state reduces the resulting random phase error. There was no effect on the recorded output power. Finally, the phase noise of the LO chain was analyzed. This was done by extending a 67 GHz spectrum analyzer combined with a 220 GHz to 330 GHz sub-harmonic mixer.
The up-converted signal output power at an input power of −17 dBm was averaged over all control voltage steps and is shown in Fig. 4.23 from 210 GHz to 240 GHz. At the junction point of the two measurement setups at 220 GHz the transition is smooth within a slight local reduction in output power. This can be explained by differences of the power calibrations as well as the separate manual contacting of the chips with probes suitable for the characterized frequency bands. Centered around 225 GHz, a 3-dB bandwidth of 8.9 GHz is measured which results in 4 % of relative bandwidth. The simulation predicts the measurement within an increase in maximum power of 2.5 dB and a stronger lowpass characteristic. Both can be explained by modeling uncertainties in the bondwires and ILO. Fig. 4.24 shows the complex output signal in the polar plane at the center frequency of 225 GHz.

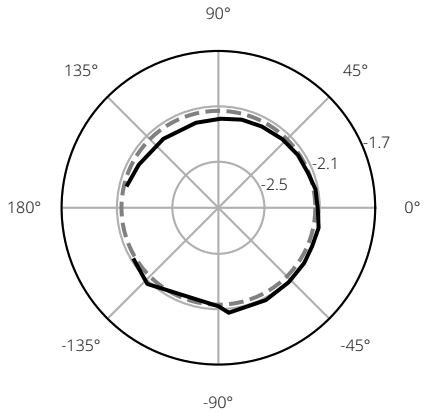


Figure 4.24: Measured polar output power of the phase-steering LO chain in dBm over the full control range of v_{in} from 1.2 V to 2.25 V shown in solid black. As a reference the mean measured output power is plotted in dashed gray. [Ste7] © IEEE 2022

The mean measured output power level is given as a gray dashed line which the measured result follows closely. A maximum phase shift of 330° can be realized. The lack of 30° of phase control can be explained by mismatch introduced between the stages and should be avoided in a fully integrated system by a precise design of an inter-stage matching network to enable precise beam steering with many antenna elements.

The phase steering behavior is further analyzed in Fig. 4.25, showing all measured phase states from v_{in} ranging from 1.2 V to 2.25 V over the 3-dB-bandwidth . With the phase tuning range increasing with frequency, the full band of operation maintains a phase range of more than 300°.

In the following, the measured results are related to the ideal behavior – a constant magnitude and a predictable phase control – at 225 GHz and an input power level of –17 dBm. As shown in Fig. 4.26a, the amplitude deviation from the mean value of the measurement is less than

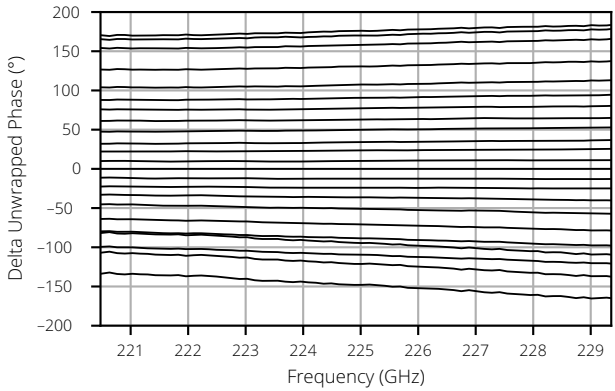


Figure 4.25: Measured phase states of the phase-steering LO chain over the tuning range of v_{in} from 1.2 V to 2.25 V over frequency for the 3-dB band. [Ste7] © IEEE 2022

±0.064 dB. The resulting RMS magnitude error is 0.04 dB which is approximately a fifth of the standalone phase shifter [Ste5]. This can be explained by the magnitude limiting characteristic of the output buffer ILO. The phase deviation from the fitted arc-sine behavior is depicted in Fig. 4.26b. With a maximum of ±12.8° the RMS phase error is only 4.7°. This is approximately five times the phase error of [Ste5], deviating by 1.14° from the predicted quadrupling of the RMS error.

The large signal behavior, as a crucial characteristic of a LO chain, was investigated by sweeping the input power as shown in Fig. 4.27. At 225 GHz the saturated output power is 0.16 dBm. The system is in compression at iP_{1dB} = −20.54 dBm at 55 GHz or oP_{1dB} = −0.55 dBm at 220 GHz respectively. Accordingly, the linear power gain is 21 dB at 225 GHz. Simulation and measurement results match within a 2.5 dB as observed in Fig. 4.23.

As the phase noise in the LO chain can have significant negative influence on a data transmission system [156], the phase noise was measured and is depicted in Fig. 4.28. A value of −110 dBc/Hz is recorded at an offset frequency of 10 MHz. Compared to the generator's noise behavior, starting from 10 kHz, the phase noise is increased by 12 −14 dB.

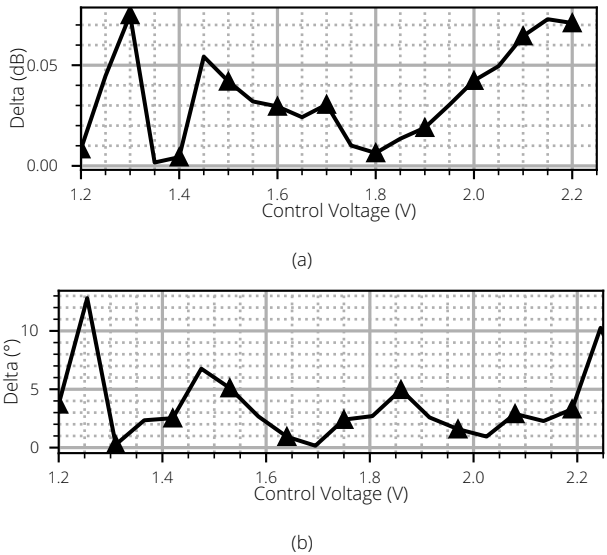


Figure 4.26: Measured magnitude imbalance and phase deviation from ideal arc-sine behavior of the phase-steering LO chain over the tuning range of v_{in} from 1.2 V to 2.25 V at 56.25 GHz. (a) Absolute magnitude deviation from the mean magnitude value. (b) Absolute phase deviation from the ideal phase value. [Ste7] © IEEE 2022

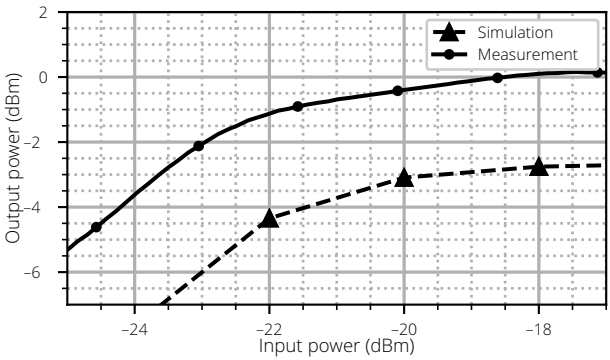


Figure 4.27: Measured and simulated output power for an input power sweep of the phase-steering LO chain at 56.25 GHz at the input resulting in a 225 GHz output signal. [Ste7] © IEEE 2022

This agrees with the predicted 12.04 dB increase of phase noise at a frequency multiplication factor of $N = 4$ according to Eq. 3.2.

Conclusion

An efficient mm-wave LO chain with high output power and gain with phase control was investigated. A phase shifter in conjunction with a frequency multiplication stage enables 330° of phase control range at 225 GHz at the output. The presented circuit proves the theoretical principle of multiplying both the phase and frequency as described by Eq. 4.25. Another research finding is the possibility of significantly reducing the RMS magnitude error by including an amplitude limiting amplifier at the output. This was achieved by an ILO with high sensitivity. With LO chains commonly driving subsequent stages into saturation, the associated loss of linearity is acceptable in this application.
A high gain of 21 dB is combined with a high saturated output power of 0.16 dBm. These values improve the state of the art, shown in Tab. 4.2, by 25 dB and 17 dB respectively. At 0.99 % of drain efficiency and 10.7 % of gain efficiency, comparable circuits are outperformed by

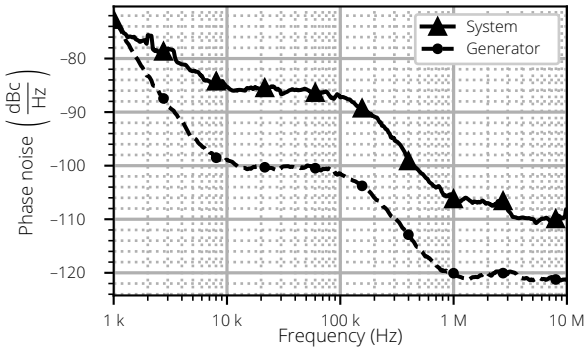


Figure 4.28: Measured phase noise of the phase-steering LO chain at 56.25 GHz at the input with the generator behavior as a reference. [Ste7] © IEEE 2022

a factor of 40 and 2.5, enabled by the low power consumption of 105 mW. These results are achieved while maintaining a competitive RMS phase error of 4.7° and phase noise of −110 dBc/Hz at 10 MHz offset. The RMS magnitude error improves the state of the art by a factor of 8 at 0.04 dB.

Table 4.2: State of the art of mm-wave phase-shifting systems operating at around 200 GHz and above.

	[Ste7]	[169]	[170]	[171]	[172]	[173]
Technology	130 nm SiGe BiCMOS	130 nm SiGe BiCMOS	55 nm BiCMOS	45 nm CMOS	130 nm SiGe BiCMOS	250 nm InP
Method	VS[1] 90°+ f×4 + Buffer	VS[1]360°	Reflect. 60°+ f×2 + Shilo×3	VS[1] 90°+ Buffer + 4x	VS[1] 360°+ Buffer	VS[1]360°
Center frequency (GHz)	225	180	285	390	235	270
Relative bandwidth (%)	4	22.2	10.5	10.2	12.8	37
Gain (dB)	21	-9.5	-18	-12.5	-7.2	-13.7
RMS gain error (dB)	0.04	0.35	-	-	0.6	1.2
Gain variation (±dB)	0.0635	-	2	2[3]	-	1.9
RMS phase error (°)	4.7	2	-	6[3]	2.5	10.2
Phase variation (±°)	12.8	13	-	-	-	-
Phase noise @ 10 MHz(dBc/Hz)	-110	-	-115	-	-	-
$P_{out,max}$ (dBm)	0.16	- [2]	-17	-	-	-
oP_{1dB} (dBm)	-0.55	- [2]	-	-	-	-14
P_{DC} (mW)	105	8.6	80	191.125	118.6	31.9
Drain efficiency (%)	0.99	-	0.025	-	-	-
Gain efficiency[4] (%)	10.7	3.9	0.2	0.1	0.4	0.6
Area (mm^2)	1.2	0.375	1.313	1.016	0.12	0.23

[1] Vector-sum phase-shifter [2] Small-signal analysis only; [3] Vector modulator stand-alone; [4] $\frac{Gain_{lin}}{P_{DC}} \cdot 1mW$

4.3. Hybrid True-Time and Phase-Delayed Beam Steering

The presented work was published in [Ste3].
Commonly, beam steering systems use either phase delayed or time delayed architectures as described in section 4.1. Motivated by the inherent beam squinting caused by phased steering of broadband signals and the discrete tuning range and large area of time delayed architectures, a novel, hybrid approach for beam steering combines minimal beam squinting while using small silicon area and maintaining continuous beam direction tuning. The proposed architecture employs both analog phase delayed and discrete time delayed steering. In doing so, the first time-delay circuit operating at frequencies over 200 GHz is shown. An universally applicable design process is described and demonstrated for an example (2×1)-array system.

Hybrid Architecture

The proposed hybrid beam steering system is shown in Fig. 4.29. The two paths in the example array are controlled by a time delay and phase delay in series. Together these two steering mechanisms produce the combined steering angle

$$\theta = \theta_{\text{phase}} + \theta_{\text{TTD}}. \tag{4.40}$$

In the following, an universal design process of a hybrid analog beam steering system is presented for a (2×1)-array. The signal is characterized by the center frequency f_c and the relative bandwidth BW_{rel}. A simplified overview of the design flow is given in Fig. 4.30. As the first step, the goal performance characteristics must be defined. Namely these are the necessary maximum steering angle θ_{max} and the maximum allowable beam squint $\Delta\theta_{\text{max}}$. Reasonable values for these two parameters depend on the specific application.
In the interest of minimizing both the silicon area consumption and the design complexity, the steering contribution of the phase shifter is maximized. The maximum allowable beam steering by the phase shifter $\theta_{\text{phase,max}}$ is bound, however, by the beam squint limit $\Delta\theta_{\text{max}}$. Accordingly, the value of $\theta_{\text{phase,max}}$ can be numerically determined

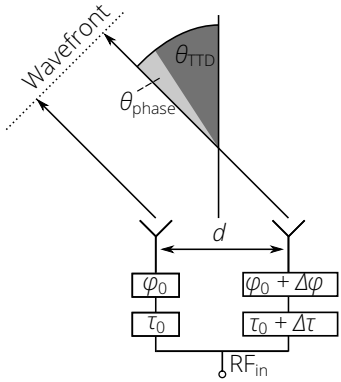


Figure 4.29: Proposed hybrid beam direction steering architecture combining phase and time delay. [Ste3] © IEEE 2022

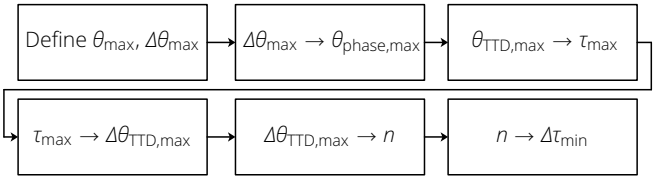


Figure 4.30: Flowchart of the design process of the proposed analog hybrid beam steering architecture.

from Eq. 4.9. In the following, a phase shifter with symmetrical phase control from $-\Delta\varphi_{\mathrm{c,max}}$ to $+\Delta\varphi_{\mathrm{c,max}}$ is assumed. With $\theta_{\mathrm{phase,max}}$ and

$$\Delta\varphi_{\mathrm{c,max}} = \sin\left(\theta_{\mathrm{phase,max}}\right) \cdot \frac{2\pi d}{\lambda_{\mathrm{c}}} \cdot \frac{180^\circ}{\pi} \overset{d=\frac{\lambda_c}{2}}{=} \sin(\theta_c) \cdot 180^\circ, \tag{4.41}$$

the maximum absolute phase shift $\Delta\varphi_{\mathrm{c,max}}$, which exactly produces the allowable beam squint amount, is determined. Next, with $\theta_{\mathrm{phase,max}}$ defined, the time-delay circuit's contribution to the steering direction

$$\theta_{\mathrm{TTD,max}} = \theta_{\mathrm{max}} - \theta_{\mathrm{phase,max}}. \tag{4.42}$$

can be calculated. This allows to determine the maximum necessary total time delay

$$\Delta\tau_{\mathrm{max}} = \frac{d}{c} \sin\left(\theta_{\mathrm{TTD,max}}\right), \tag{4.43}$$

which the delay circuit has to provide. The resolution of the time delay, defining the delay step width, is calculated next. Keeping with the goal to minimize the area consumption of the time delay circuit, the maximum beam direction gap between two time steps is bound by the maximum allowable phase-delayed steering contribution $\Delta\varphi_{\mathrm{c,max}}$. From this, the coarsest possible resolution, thus, producing the least delay steps, is found. Assuming a target beam direction between two time delay steps, the phase shifter adjusts the beam direction starting from the closest time delay step. At a maximum, this converges in the middle between two time delay steps. The maximum beam direction gap, given an equidistant time delay resolution, is found between the largest and second largest delay state caused by the non-linear steering behavior of time delayed architectures as shown in Fig. 4.3a. Ensuring that the phase shifter can cover the gap, producing continuous beam direction control, the condition

$$\Delta\theta_{\mathrm{TTD,max}} \overset{!}{\geq} \theta_{\mathrm{TTD,max}} - 2 \cdot \theta_{\mathrm{phase,max}} = \theta_1, \tag{4.44}$$

with the constant θ_1 as a substitute to simplify the following expressions, must be fulfilled. Further, the maximum possible time delay step at the end of the time-delayed steering range

$$\begin{aligned}\Delta\theta_{\mathrm{TTD,max}} &= \arcsin\left(\frac{c\Delta\tau_{\mathrm{max}}}{d}\right) - \arcsin\left(\frac{c\left(\frac{2^n-2}{2^n-1}\right)\Delta\tau_{\mathrm{max}}}{d}\right)\\ &= \theta_{\mathrm{TTD,max}} - \arcsin\left(\left(\frac{2^n-2}{2^n-1}\right)\sin\left(\theta_{\mathrm{TTD,max}}\right)\right)\end{aligned} \tag{4.45}$$

can be written in terms of the maximum time-delayed steering direction $\theta_{\mathrm{TTD,max}}$ and the resolution n. From Eq. 4.45 with Eq. 4.44 the minimum necessary resolution

$$n = \left\lceil \frac{1}{\log(2)} \log\left(\frac{\sin(\theta_1)d - 2c\Delta\tau_{\mathrm{max}}}{\sin(\theta_1)d - c\Delta\tau_{\mathrm{max}}}\right)\right\rceil. \tag{4.46}$$

is specified. Concluding the system design, the minimum time step

$$\Delta\tau_{\mathrm{min}} = \frac{\Delta\tau_{\mathrm{max}}}{2^n - 1} \tag{4.47}$$

can be obtained by dividing $\Delta\tau_{\mathrm{max}}$ by the number of resulting time steps.
In the following a numeric example for a signal with a center frequency of 235 GHz and a bandwidth of 30 GHz is presented to illustrate the proposed system design flow:

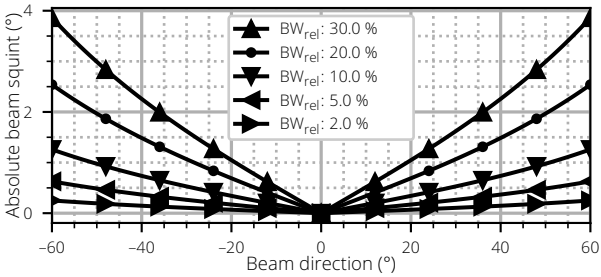
1. The design goal is to limit the beam squint to 2° up to a steering direction of 60°.

2. The distance between two antennas is $d = \lambda_c/2 \Rightarrow d = 637.8\,\mu\mathrm{m}$.

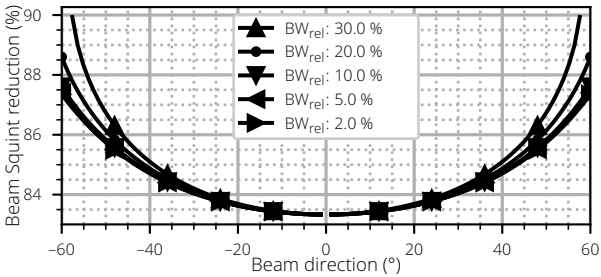
3. The relative bandwidth is $BW_{\mathrm{rel}} = 12.8\,\%$.

4. Numerically solving Eq. 4.9 for the allowable beam squint produces a maximum phase-delayed steering angle of $\theta_{\mathrm{phase,max}} = 15.18°$.

5. From Eq. 4.6, the necessary symmetrical phase shift of $\pm\Delta\varphi_c = 47.13°$ is determined.



(a)



(b)

Figure 4.31: Analysis of the theoretical beam squint behavior of an ideal 2-bit hybrid beam steering architecture over relative bandwidths from 2 % to 30 % and beam directions from –60° to 60°. (a) Remaining beam squint introduced by the steering contribution of the phase shifter. (b) Relative reduction of the maximum beam squint compared to an ideal, conventional phase-delayed steering system. [Ste3] © IEEE 2022

6. Accordingly the time delay stage must provide the remaining $\theta_{\mathrm{TTD,max}} = 44.82^\circ$ of beam direction control.

7. Eq. 4.43 produces a maximum necessary time delay of $\Delta\tau_{\mathrm{max}} = 1.5\,\mathrm{ps}$.

8. The necessary number of bits is calculated according to Eq. 4.44 – 4.46 to $n = \lceil 1.35 \rceil = 2$.

9. With the calculated number of bits the unit time step $\Delta\tau_{\mathrm{min}} = 0.5\,\mathrm{ps}$ is determined per Eq. 4.47.

The superior performance of this approach for an ideal 2-bit system is highlighted in Fig. 4.31. The maximum beam squint generated by the hybrid system is determined by inserting the maximum steering angle produced by the phase shifter according to Eq. 4.45 in Eq. 4.9. This results in beam squint values of less than 4° for relative bandwidths of up to 30 %, as shown in Fig. 4.31a. Accentuating the potential performance of the proposed architecture, Fig. 4.31b compares the remaining beam squint to a traditional phase-delayed steering system. With the maximum beam squint values reduced by more than 83 % for all analyzed bandwidths and beam directions, the presented approach shows its effectiveness in reducing the beam squint while maintaining continuous beam direction control. The flexible and configurable design flow can be applied to various signals independent of the absolute frequency band and can, with small changes to the presented math, be expanded to larger array systems.

Circuit Design

True Time Delay Circuit

At the core of the hybrid steering architecture is the time delay cell. The simplified schematic is shown in Fig. 4.32. This is build from two single-pole double-throw (SPDT) switches which are based on $\lambda/4$-dividers, bipolar RF-switches and different length transmission lines $\mathrm{TL}_{\mathrm{delay}}$ and $\mathrm{TL}_{\mathrm{ref}}$.

A single-stage shunt configuration [174] was chosen to limit the overall silicon footprint of the SPDT architecture. The input signal is fed to a 50 Ω-quarter-wavelength divider. Each of its two transmission lines is

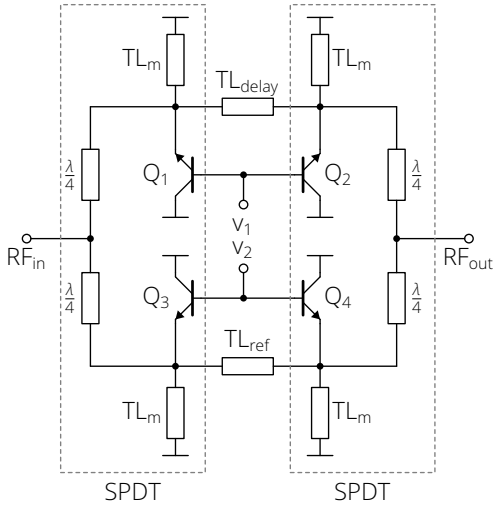


Figure 4.32: Simplified schematic of the proposed true-time delay cell with the heterojunction bipolar transistors (HBTs) in reverse saturated configuration employed in the hybrid beam steering circuit. [Ste3] © IEEE 2022

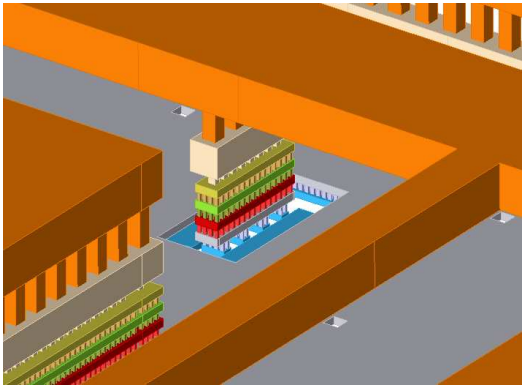


Figure 4.33: 3D view of the HBT switch in the SPDT of the time delay circuit placed under the RF transmission line. [Ste3] © IEEE 2022

connected to a heterojunction bipolar transistor (HBT) switch. The architecture is based on the transformation of a RF-ground, produced by the switches, to a RF-open by the $\lambda/4$-lines. Assuming a perfect switching behavior of $Q_{1,\ldots,4}$, this results in a complete reflection of the input signal and, thus, a high isolation of the turned off path. To improve the thru characteristic of the time delay stage, a second SPDT is connected at the output to avoid any signal leakage into the turned off path. The switching transistors are set up in reverse saturated configuration [175], connecting the emitter to the signal line and the collector to ground. Compared to the forward saturated arrangement, this is shown to reduce the insertion loss of the SPDTs [175], [176]. Per path, the transistor pairs are configured as pairs sharing a bias voltage at the respective bases. A scaling factor of $N_x = 4$ of the unit transistor size [63] results from an optimization for minimum insertion loss. Finally, the layout, shown in Fig. 4.33, was optimized to minimize parasitic effects resulting in the best possible RF-ground, when the transistors are switched on, and minimum insertion loss when switched off. A binary signal switching from 0 V to 1 V and vice-versa functions as the control signal supplied to V_1 and V_2. High-impedance transmission lines TL_m provide a path to ground for the base current. Further,

the electrical length was optimized to 38° at 235 GHz, to reduce the insertion loss and compensate for remaining parasitics from the bipolar switches. To achieve the required difference in path delay, the delay lines TL_{ref} and TL_{delay} feature unequal lengths. The length, width and line routing was carefully optimized using finite element method (FEM) simulations of the entire delay cell, to minimize the variations in frequency behavior and produce constant time delay steps over the band of operation. This extensive process is necessary to include all possible parasitics as even small delay variations of some femtoseconds introduce observable beam direction differences at mm-wave frequencies. Two different delay cells, following the numeric values calculated in the design flow described above, are designed. The short, unit delay cell was simulated to provide a time delay difference between the two paths of 0.53 ps. At 1.14 ps, the larger delay cell successfully provides approximately twice the simulated short delay. At the center frequency of 235 GHz, this produces a phase shift of 44.8° and 96.4° in free-space, respectively. This results in a theoretical maximum beam direction of 51.7°. The deviations from the ideal unit step of 0.5 ps are due to a focus on designing for the most constant time step over frequency. With some phase control reserve in the phase shifter, in comparison to the calculated minimum necessary value of ±47.13°, a continuous beam direction control is enabled.

Phase Shifter Circuit

The necessary phase control is realized in a vector-sum phase shifter designed for ±45° of phase shift as shown in Fig. 4.34. At the input, the necessary orthogonal signals are produced by a 4-finger Lange coupler [160]. This electromagnetic coupler architecture is advantageous for its large bandwidth, low insertion loss and high phase precision. A simulated phase deviation of less than ±4° and transmission factor deviation of ±0.4 dB is shown in Fig. 4.35. The simulated insertion loss is low at approximately 1 dB. Next, the orthogonal signals are fed to separate VGAs, which weigh the I- and Q-signals to produce the wanted phase and amplitude functionally similar to the circuit presented in section 4.2.1. Based on bipolar cascodes, the *Miller Effect* within the amplifiers is reduced which significantly increases the circuits frequency of operation. A transistor of size of $N_x = 2$ [63] optimizes small-signal gain, bandwidth and DC power consumption. The VGAs are controlled

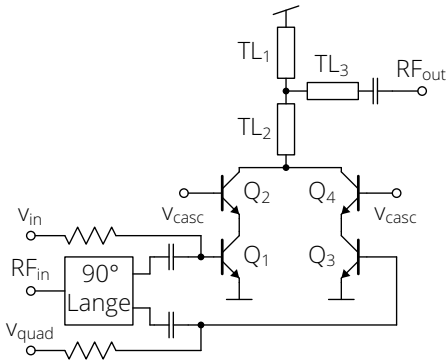


Figure 4.34: Simplified schematic of the proposed phase shifter based on a vector-sum architecture to be used in the hybrid beam steering circuit. [Ste3] © IEEE 2022

via the bias voltage of the emitter-configured transistors $Q_{1,3}$ by varying the voltage from 0.79 V to 0.85 V. Assuming the ideal phase shift of $\pm 45°$ this enables a $\pm 14.5°$ of beam direction steering.

Simulation and Measurement Results

Providing a feasibility study, the proposed circuit, shown in Fig. 4.36, was designed and produced in a 130 nm SiGe BiCMOS technology. The design features a 2-bit true-time delay stage, marked 1, and a phase shifter labeled 2. Most of the total chip area of 0.665 mm^2 is used by the time delay core at 0.134 mm^2 while the phase shifter uses 0.046 mm^2, with the pads and DC-lines accounting for the rest. With 0.43 mW for the time delay and 3.90 mW from a 2.2 V supply line consumed by the phase shifter, a total of 4.33 mW of DC power is used. The circuit was characterized using a network analyzer as well as frequency converter modules enabling a measurement band of 220 GHz to 330 GHz. A small IF bandwidth of 100 Hz ensured high measurement precision. Further, every measurement result is the product of three independent measurement runs which are averaged to reduce possible random phase errors of the measurement equipment.

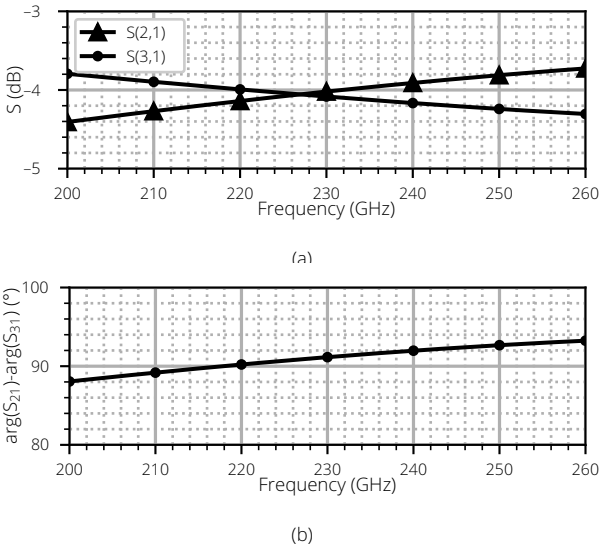


Figure 4.35: Electromagnetic simulation results of the designed Lange coupler producing the orthogonal signals for the vector-sum phase-shifter in the hybrid beam steering circuit. (a) Forward transmission factors from the input to the two output ports. (b) Phase difference of the orthogonal outputs. [Ste3] © IEEE 2022

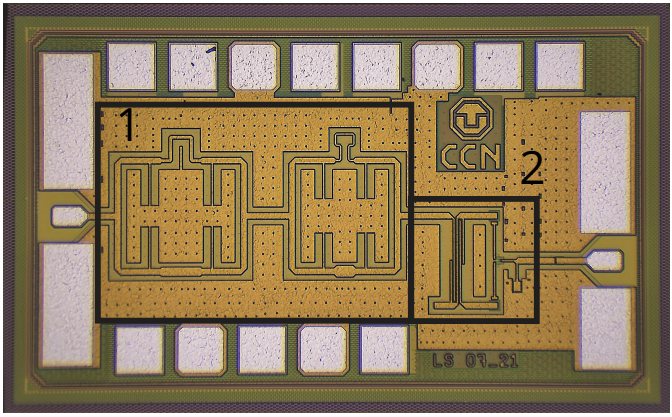


Figure 4.36: Chip photograph of the fabricated hybrid beam steering circuit consisting of a 2-bit time delay stage (1) and a 90° vector-sum phase-shifter (2). The circuit measures 0.632 mm × 1.052 mm = 0.665 mm^2. [Ste3] © IEEE 2022

Small-Signal Reflection and Transmission Measurements

Shown in Fig. 4.37, is the input reflection coefficient over frequency. Illustrating that the input of the circuit is unaffected by the change of time delay state or phase shift, all measured settings are plotted and an average is given to ease the analysis. The resulting input reflection is better than –10 dB for the whole frequency band of operation, matching the simulation. Minor differences in matching between the time delay states can be attributed to parasitics and non-ideal behavior in the SPDT-switches.

At a phase shifter supply voltage of 2.2 V and a bias voltage of 0.832 V at both emitter stages, the forward transmission factor is shown in Fig. 4.38. With a center frequency of 235 GHz, the 3-dB-bandwidth is 30.1 GHz which equates to a relative bandwidth of 12.1 %. At 232 GHz, the maximum small-signal gain is –8.6 dB. Within a slight degradation of bandwidth and frequency of operation of approximately 3 % the simulation predicts the measurements well.

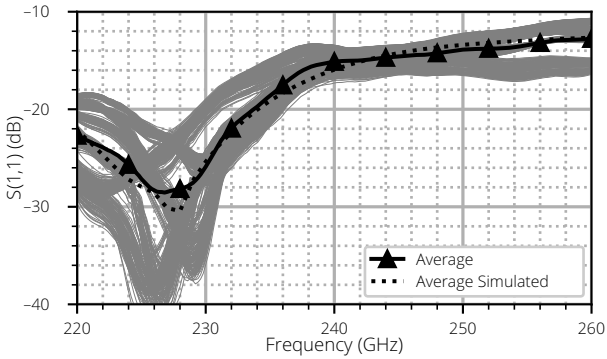


Figure 4.37: Measured (solid) and simulated (dotted) reflection coefficient at the input of the hybrid beam steering circuit. The full set of measurements for all time delay states and phase shifter bias voltages from 0.79 V to 0.85 V are given in gray. An average of all measured states is given in black to ease the interpretation. [Ste3] © IEEE 2022

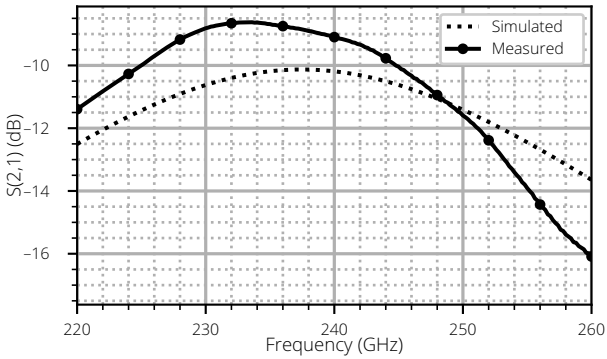


Figure 4.38: Measured (solid) and simulated (dotted) forward transmission factor of the hybrid beam steering circuit over frequency. The phase shifter is biased at a supply voltage of 2.2 V and 0.832 V as bias voltage to both transistors in emitter configuration. [Ste3] © IEEE 2022

The forward transmission factor varies by less than ±1.5 dB across the four possible time delay states. This is shown in Fig. 4.39 for a constant bias voltage of 0.82 dB at the emitters. With all measurements producing parallel frequency dependent behavior, the bandwidth remains unchanged for all delay states. As will be shown later, the phase shifter features enough dynamic range to fully compensate any resulting change in output power.

Analysis of the time delay stage

Analyzing the measured transmission phase for all time delay states over frequency for constant operation conditions of the phase shifter, shows the phase characteristic to be continuous, steady and monotonously falling as depicted in Fig. 4.40. This behavior is expected for transmission lines, as described in section 2.2, and avoids broadband signal distortion [67] enabling the circuit to perform in broadband operation. The phase differences, referenced to 'TTD Step: 1', are shown in Fig. 4.41. A linear fit for each measured line, representing the ideal behavior, highlights the very linear and monotonous characteristic.

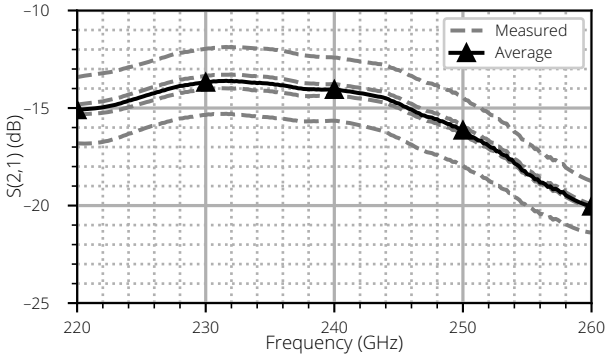


Figure 4.39: Measurement of the forward transmission behavior of the hybrid beam steering circuit over frequency for all time delay steps. The phase shifter is biased at a supply voltage of 2.2 V and 0.82 V as bias voltage to both transistors in emitter configuration. [Ste3] © IEEE 2022

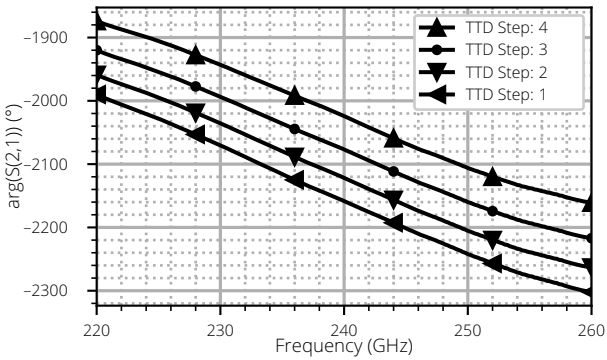


Figure 4.40: Measured unwrapped phase behavior over frequency of the forward transmission produced by the time delay circuit for all time delay states. The phase shifter operation point is constant at bias voltage of 0.82 V. [Ste3] © IEEE 2022

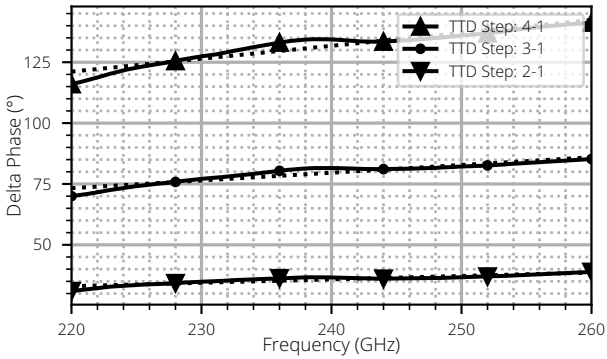


Figure 4.41: Measured relative phase differences produced by the time delay circuit over frequency in relation to 'TTD Step: 1'. A linear fit, representing the ideal behavior, is given as dotted lines for each measurement. [Ste3] © IEEE 2022

From this, time delay differences can be calculated per Eq. 2.15 and 4.5, which produces mean time delay values of 0.39ps, 0.88ps and 1.47ps, shown in Fig. 4.42. Compared to the simulated mean values, a maximum deviation of less than 200 fs can be observed, which can be attributed to small parasitics and modeling imprecisions partly caused by process variations.

Fig. 4.43 shows the analysis of the frequency dependent deviations of the time delay states from their respective mean values. These are difficult to calibrate for and can lead to frequency dependent differences in the resulting beam direction. Therefore, these values must be minimized. For the measured frequency band, a maximum absolute deviation of 65 fs is recorded, while the deviations are mostly lower than 20 fs. Further, this produces RMS delay errors of 7.9 fs, 15.6 fs and 23.7 fs.

Finally, considering the systematic influence of the aforementioned measurements, the implications on the beam direction of the example (2×1)-antenna array will be discussed. From Fig. 4.42 with Eq. 4.4,

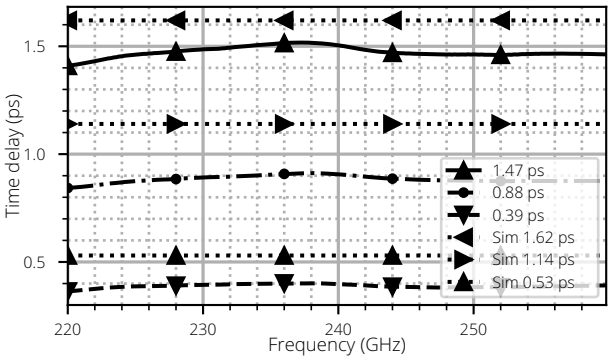


Figure 4.42: Calculated time delay over frequency resulting from the phase behavior of the time delay circuit. The measurement results are shown as solid lines and the respective simulated values depicted as dotted lines. The average measured delays are 0.39 ps, 0.88 ps and 1.47 ps. [Ste3] © IEEE 2022

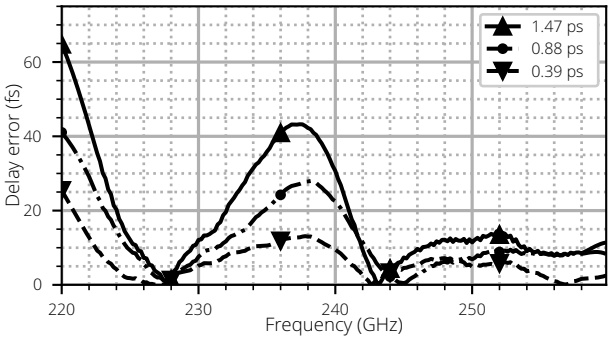


Figure 4.43: Measured absolute delay variation produced by the time delay circuit as a deviation from the respective mean values. This results in RMS delay errors of 7.9 fs, 15.6 fs and 23.7 fs. [Ste3] © IEEE 2022

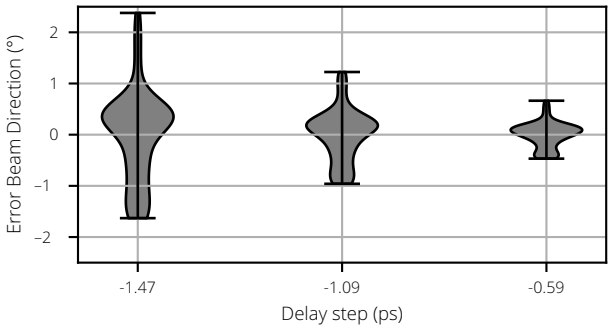


Figure 4.44: Measured violin plot of the beam direction error distribution as a measure of the deviation from the mean beam direction produced by the time delay circuit for the respective time delay states. [Ste3] © IEEE 2022

beam directions of 10.5°, 24.6° and 43.9° are expected which is a deviation of 3.9°, 7.8° and 7.8° to the simulation. The distribution of the deviation of the beam direction from the particular measured mean values over frequency for all time delay states is given in Fig. 4.44. With the largest time step producing the highest absolute deviations of less than ±2.5°, all time steps show a concentration of the beam error around zero. This leads to the conclusion that high steering precision over the frequency band can be achieved.

Analysis of the phase shifter stage

The phase shifter is characterized by sweeping the bias voltage supplied to the transistors $Q_{1,3}$, in emitter configuration, from 0.79 V to 0.85 V producing any possible combination. At 235 GHz, this produces the output vector field shown in Fig. 4.45. For the given control range, the phase shifter enables gain control from −16 dB to −10 dB producing a dynamic range of 6 dB. This confirms that a full compensation of the variation in forward transmission caused by the time delay stage, shown in Fig. 4.39 is possible. With ±35° of phase control, the beam direction of the example (2×1)-array can be steered by a maximum of

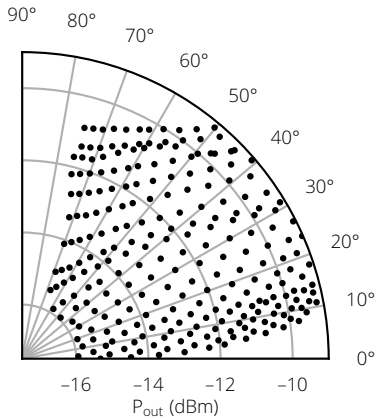


Figure 4.45: Semi-logarithmic representation of the measured transmission vector of the phase-shifter in polar representation. The results are shown at 235 GHz, sweeping the bias voltages of $Q_{1,3}$ in Fig. 4.34 from 0.79 V to 0.85 V. [Ste3] © IEEE 2022

±11.2° according to Eq. 4.6. Further, enhancements in the inter-stage matching, coupler and output network can extend this range.

Combined Analysis and Prediction of the Hybrid System Performance

According to the measurements above, the combined hybrid system can provide a steering range of ±54.6°. The steering algorithm producing the total beam direction while minimizing the total beam squint,

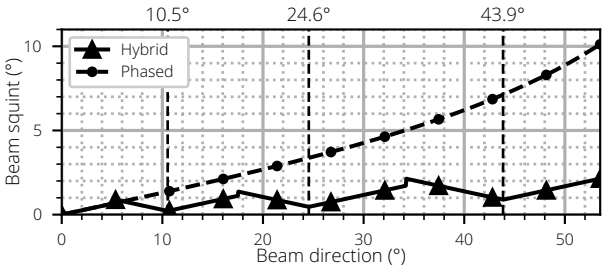
$$\theta = \begin{cases} \theta_{\text{phase}}, & 0 \leq \theta \leq \frac{\theta_{\text{TTD},1}}{2} \\ \theta_{\text{phase}} + \theta_{\text{TTD},1}, & \frac{\theta_{\text{TTD},1}}{2} < \theta \leq \frac{\theta_{\text{TTD},1}+\theta_{\text{TTD},2}}{2} \\ \theta_{\text{phase}} + \theta_{\text{TTD},2}, & \frac{\theta_{\text{TTD},1}+\theta_{\text{TTD},2}}{2} < \theta \leq \frac{\theta_{\text{TTD},2}+\theta_{\text{TTD},3}}{2} \\ \theta_{\text{phase}} + \theta_{\text{TTD},3}, & \frac{\theta_{\text{TTD},2}+\theta_{\text{TTD},3}}{2} < \theta \end{cases} \tag{4.48}$$

is a piecewise defined function, with $\theta_{\text{phase}} = \{-11.2°, \cdots, 11.2°\}$. Fig. 4.46a depicts the remaining total beam squint as a sum of the beam squint produced by the phase shifter and the RMS beam direction error of the time delay stage for the band of operation. At a

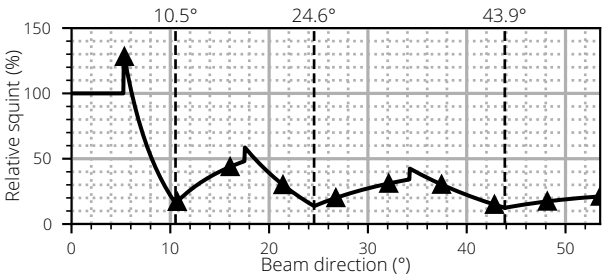
relative 3-dB-bandwidth of 12.8 %, a maximum beam squint of less than 2.5° is shown up to 54.6° of steering direction. While the steering steps enabled purely by the time delay stage are marked, the transitions between neighboring delay steps are placed according to Eq. 4.48 producing fully continuous beam direction control. Compared to the behavior of an ideal phase shifter, the measured hybrid steering system can reduce the beam squint by more than 50 % at beam directions larger than 8° as shown in Fig. 4.46b.

Conclusion

An innovative hybrid beam steering architecture combining low beam squinting, enabled by time-delayed steering, with analog control and small area consumption, contributed by phase-delayed beam steering, was developed. Based on the theoretical analysis of the behavior of phase-delayed and time-delayed beam steering systems, a design process for a novel hybrid analog beam steering architecture is devised. As a key research finding, it is shown that the system is capable of theoretical reductions in beam squint, inherent to phase-delayed systems, by more than 83 %, as the contribution of the phase-shifter to the overall steering direction is minimized. At the same time, the system provides fully analog beam direction control and minimizes the area demands. With the design process detailed and example performance requirements defined, a circuit was analyzed, designed, fabricated and characterized to prove the feasibility of this approach.
The state of the art of circuits capable to provide beam direction steering in the mm-wave band is given in Tab. 4.3. The designed circuit features the first true time delay circuit over 200 GHz. Three delay steps of 0.39 ps, 0.88 ps and 1.47 ps are selectable with a maximum delay variation of less than 65 fs. In contrast to to all compared time delay circuits, this work enables continuous beam direction control. This is achieved by using a phase shifter at the output which provides analog beam direction control. Combined, this reduces the silicon area, compared to the closest time delay circuit [128], by 43 %. Contrasting the beam squint behavior with a stand-alone phase shifter in the same band [172], a reduction in maximum beam squint by more than 75 %, for large steering directions, is possible for a (2 × 1)-antenna array. The combined small-signal gain of –8.6 dB is competitive with typical mm-wave phase shifters while improving upon state-of-the-art time



(a)



(b)

Figure 4.46: Mathematical remaining squint prediction of the proposed hybrid beam steering system based on the measurement results at the relative 3-dB-bandwidth of 12.8 %. The predicted error combines the RMS beam direction error of the time delay stage and the beam squint caused by the phase shifter. (a) Absolute hybrid squint (solid) in comparison to the beam squint of an ideal phase shifter. (b) Relative improvement of the beam squint referenced to the beam squint of an ideal phase shifter. [Ste3] © IEEE 2022

delay circuits without any buffer amplifiers. Additionally, the phase shifter, due to its flexibility with dynamic range of at least 6 dB can fully compensate the gain variation between delay configurations of ±1.5 dB. A possible resulting phase error can be compensated by precisely calibrating the phase-shifter by characterizing its transfer behavior and fitting a function to the measurement results with the needed output power value and phase delay as variables. This can also be used to account for any process variations or modeling inaccuracies in the sensitive time delay stage enabling highly reliable and precise beam steering. At 4.33 mW of DC-power consumption, an efficient circuit was designed using less than 20 % of the power of the only design operation in a similar frequency range [128] and less than 35 % of the power of 360° phase shifters [135], respectively.

Table 4.3: State of the art of circuits enabling beam direction steering in the mm-wave frequency range.

	This	[128]	[177]	[178]	[135]	[179]	[172]
Architecture	TTD + Phase	TTD	TTD	TTD	Phase Shifter	Phase Shifter	Phased 4–channel
Technology	0.13 µm SiGe BiCMOS	0.13 µm SiGe BiCMOS	0.13 µm SiGe BiCMOS	0.25 µm SiGe:C BiCMOS	0.13 µm SiGe BiCMOS	0.25 µm InP HBT	0.13 µm SiGe BiCMOS
Center frequency (GHz)	235	140	35	30	175	275	235
Relative bandwidth (%)	12.8	42.9	28.6	133.3	17.1	25.5	12.8
Maximum delay (ps)	1.47	6.64	54‡	32	—	—	—
Maximum eq. phase (°)	124.4	334.7	680.4	345.6	360	360	360
Delay resolution (ps)	0.39	0.44	18‡	continuous	—	—	—
Phase resolution (°)	33 + continuous	22.2	226.8	—	continuous	24	continuous
Gain (dB)	-8.6	-21.5	10§	-15.5	-6.2	-13	-5.25
Gain variation (±dB)	1.5	1.4	X†	1.3	—	X†	3
Beam squint (°)*	2.5	—	—	—	14.4	22.8	10.5
P_{DC} (mW)	4.33	22.84	104	passive	12.4	X†	137.8**
Area (mm^2)	0.665	1.166	1.44	0.22	0.428	X†	3.99

* Maximum possible value for a 2x1 array at 54.6° steering angle

† not given

‡ calculated

** per channel

§ System with LNA in each path

5. Ultra-Wide Band Modulator for BPSK Operation

The proposed circuit described below was published in [Ste8].
Modulator circuits are at the heart of any transmission system as they encode the digital information to be transmitted in a high frequency RF signal.
This circuit extends the limits for binary phase-shift keying (BPSK) based systems in silicon technologies by exploiting the available bandwidth in the 245 GHz channel by allowing a 3-dB-bandwidth above 100 GHz – therefore enabling datarates of up to 100 Gbps.
In the literature, many systems operating in a comparable frequency band are limited to approximately 10 % of relative bandwidth and solely rely on high-order modulation schemes [30], [180]–[182] to achieve some tens of gigabit per second datarates. These systems are however limited, due to the associated linearity and signal-to-noise ratio (SNR) requirements, which are difficult to fulfill when channel frequencies approach transit frequency (f_T) [27]. Additionally, with very high data rates, where the base band signal reaches into the millimeter-wave (mm-wave) frequency range itself, high-order modulation schemes require baseband chains featuring, among others, complex digital-to-analog converters (DACs) consuming large direct current (DC) power [183]. Together, this motivates the use of wideband systems using low-order modulations for high-datarate transmissions.

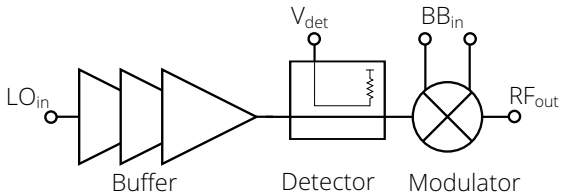


Figure 5.1: Simplified overview of the modulator system consisting of a local oscillator (LO) buffer, a power detector to characterize the available local oscillator (LO) power and the modulator circuit. [Ste8] © IEEE 2022

Circuit Design

The architecture of the designed integrated circuit is presented in Fig. 5.1. In the signal chain before the modulator core is a three-stage input buffer and a power detector. These are included solely to aid the characterization in the research laboratory. First, the externally supplied local oscillator (LO) from the laboratory signal source is amplified by a cascaded cascode amplifier. The transistors are binary scaled $N_x = 1, 2, 4$ times the unit transistor [63]. This optimizes both gain and output power. The subsequent RF power detector based on a electromagnetic narrow-side directional coupler with a terminated port eliminating the reflected wave. While attenuating the thru signal by 0.315 dB at 245 GHz in FEM simulation, the coupling factor for the forward wave towards the power detection circuit is –13.86 dB. The directionality is 16.9 dB ensuring robustness against any possible reflections from the modulator LO input. The coupled signal is fed to a square-law power detector. This consists of a diode rectifier, based on a bipolar transistor, a capacitor and a RF load which is realized as a p-type metal-oxide (PMOS) transistor for improved dynamic range of the power detector compared to a linear load [184].
Both these circuits can be reconsidered in a fully integrated implementation as shown in chapter 6 with respect to the surrounding system.
A simplified schematic of the proposed mixer core is shown in Fig. 5.2. A double-balanced Gilbert-cell architecture [185] is chosen due to its broadband performance. Particular attention must be paid to which

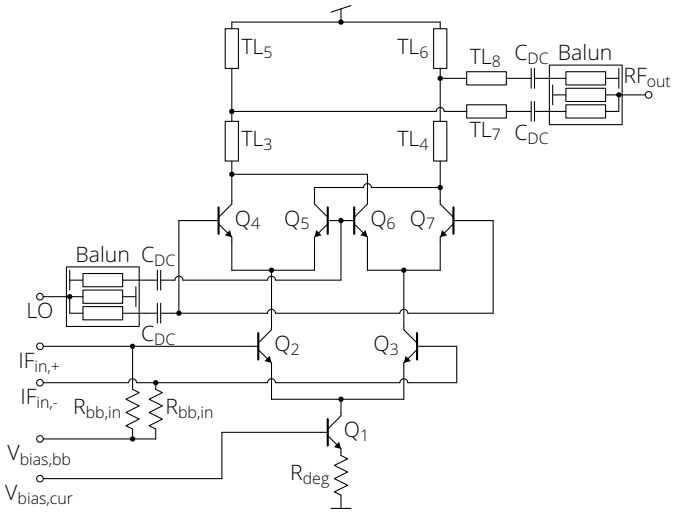


Figure 5.2: Simplified schematic of the proposed double-balanced mixer based on a Gilbert cell. [Ste8] © IEEE 2022

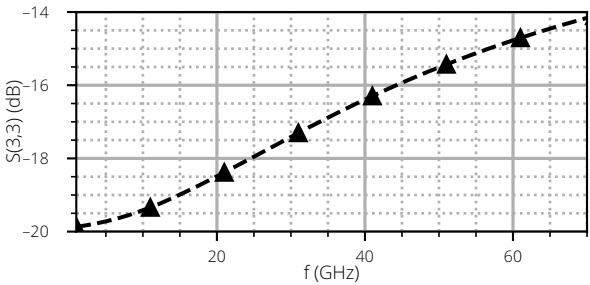


Figure 5.3: Simulated input matching of the differential input port of the double-balanced mixer shown in Fig. 5.2.

input of the Gilbert cell is fed with the baseband and LO signal, respectively. The literature points towards both possible arrangements [186], [187]. As this design strives to maximize the achievable bandwidth, the baseband signal itself is very wideband reaching well into the mm-wave spectrum at more than 50 GHz. Thus, to avoid complex broadband baseband amplifiers with a band of operation starting from DC [188], [189] capable to drive $Q_{4,\ldots,7}$, the baseband signal is supplied to $Q_{2,3}$ while the LO signal is connected to the upper transistor set. This is enabled by very powerful, narrow-band LO chains as presented in section 3.4. Finally, broadband, resistive input matching of the transistors $Q_{2,3}$ is possible as a consequence which in turn maximizes the system bandwidth. A simulated differential input match of better than −14 dB up to 70 GHz, including the probe pads, is shown in Fig. 5.3.

A current source, built from Q_1 with degenerated emitter and supplied from a current mirror, not shown in the schematic, sets the operation point current and enables true differential operation. Sets of transistors $Q_{2,3}$ and $Q_{4,\ldots,7}$ are connected to the baseband and local oscillator signal. $Q_{4,\ldots,7}$ are of minimum size while $Q_{2,3}$ are scaled with $N_x = 2$. This results in an optimum for power consumption and bandwidth. A three-line balun [190] converts the single ended LO input signal to a differential signal.

At the differential output, a matching network based on transmission lines is optimized for bandwidth and conversion gain. This is

connected through DC-blocks to another three-line balun [190] accomplishing the differential to single-ended conversion to allow the characterization in the research laboratory using the available GSG probes. Commonly, baseband (BB) and RF amplifiers are found in state of the art mixer designs [181], [182], [187]. As such buffers can skew figures like conversion gain substantially, this design omits any such amplifiers enabling an independent characterization of the mixer core performance.

Simulation and Measurement Results

The manufactured and characterized circuit is depicted in Fig. 5.4 featuring the input buffer (1), power detector (2) and mixer core (3) covering an area of 0.148 μm^2, 0.023 μm^2 and 0.158 μm^2 respectively. A total chip area, including all pads, of 1116 $\mu m \times 812\ \mu m = 0.906\ mm^2$ is used. With the LO power amplifier consuming 67.8 mW and the modulator using 27.2 mW, the total power consumption is 95.0 mW.
The measurement setup, for the characterization on the wafer prober, is based around a spectrum analyzer with an extended frequency range enabled by waveguide harmonic mixers. The LO signal is provided by a converter module fed by a external signal source. All devices in the LO and RF bands are calibrated using suitable calorimeters characterizing the behavior for every measured frequency and source power value. Compensating the frequency response of the laboratory equipment, cables and DC-blocks in the baseband signal chain, a 2D calibration script determines correction factors for each set of frequency and power values. The resulting maximum deviation of the baseband signal power is reduced to 0.045 dB with a mean variance for the characterized power steps of 10^{-4}dB. The behaviors of the probes are de-embedded with the values provided in the respective data-sheets.
The input and output matching behavior is depicted in Fig. 5.5. Wit the LO input, illustrated in Fig. 5.5a, matched better than –10 dB, minimum power reflection is assured which allows for precise characterization. The RF output port, shown in Fig. 5.5b, experiences reflections of less than –5 dB.
Fig. 5.6 shows the output power spectrum. Both harmonic mixer setups are combined to achieve a consecutive characterization from

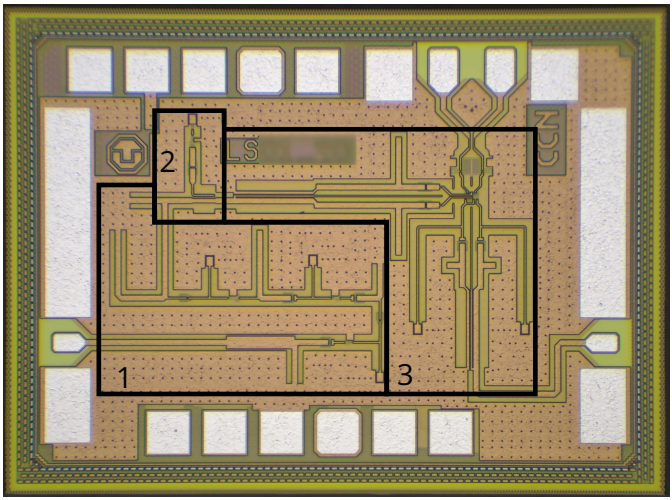


Figure 5.4: Microphotograph of the realized wideband modulator using a chip area of 1116 µm × 812 µm = 0.906 µm^2. The input buffer (1), a power detector (2) and the mixer core (3) sub-modules are labeled. [Ste8] © IEEE 2022

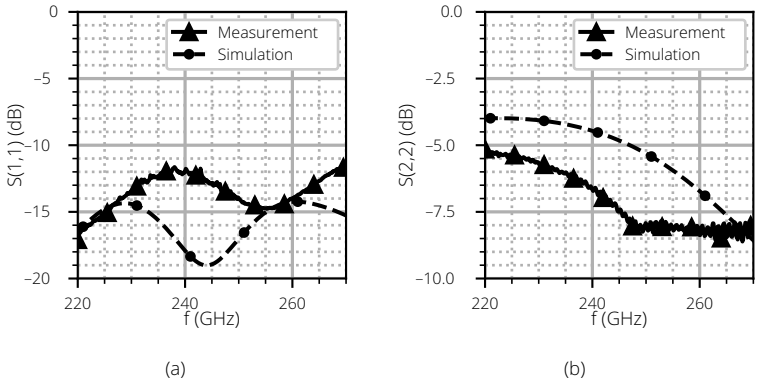


Figure 5.5: Simulated and measured reflection factors of the wideband modulator. (a) Input reflection factor. (b) Output reflection factor. [Ste8] © IEEE 2022

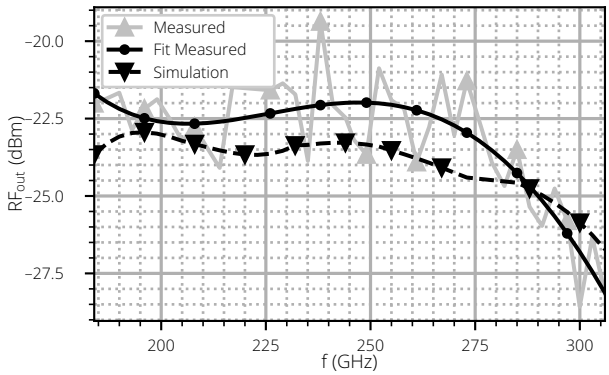


Figure 5.6: Simulated and measured spectrum of the output power of the wideband modulator at a baseband input power of $P_{BB} = 2.2\,\text{dBm}$ and a LO input power of $P_{LO} = -15.8\,\text{dBm}$. [Ste8] © IEEE 2022

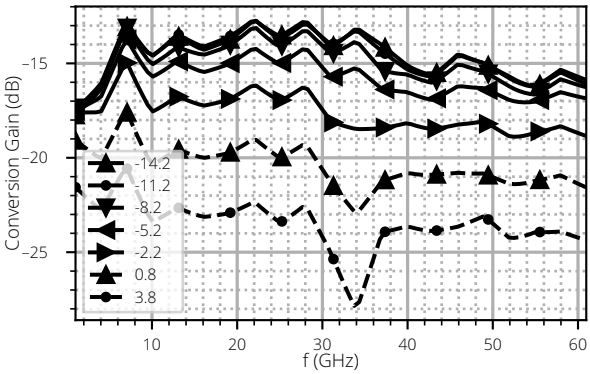


Figure 5.7: Measured spectrum of the conversion gain of the wideband modulator over baseband input power steps at a local oscillator input power of P_{LO} = −15.8 dBm. [Ste8] © IEEE 2022

184 GHz to 306 GHz. The analyzed bandwidth is limited by the maximum baseband signal frequency while allowing the compensation of the frequency response of the measurement setup to achieve a constant baseband input power over the frequency range. The measured variation in output power is a result of the difficult power calibration with long settling times and temperature dependent behavior of the waveguide calorimeter. A numeric fit allows for a precise determination of the RF bandwidth. At −15.8 dBm of local oscillator input power, a baseband input power of −2.2 dBm produces a 3-dB-bandwidth of 103.9 GHz.

Following from the power spectrum, the conversion gain is calculated and shown in Fig. 5.7 for calibrated baseband input power levels ranging from −14.2 dBm to 3.89 dBm. The LO input power is kept constant at −15.8 dBm. A maximum conversion gain of −13 dB can be observed for baseband input power levels of −5.2 dBm and less.

Enabling a precise characterization of the circuit's linearity, deterministic input power levels must first be ensured. While the baseband power levels are calibrated the internal LO power levels are monitored

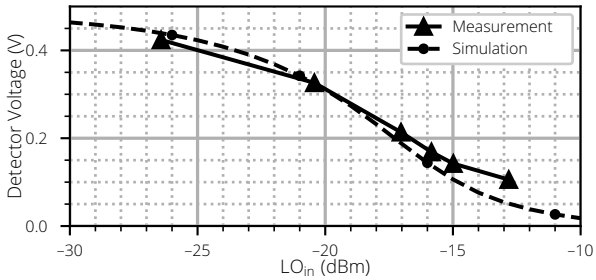
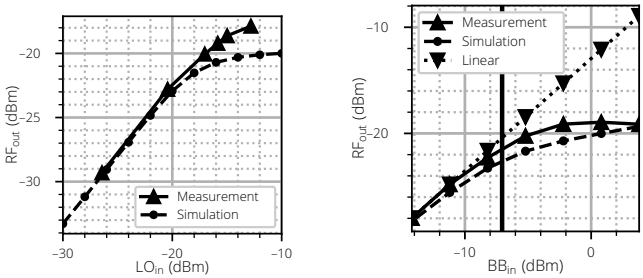


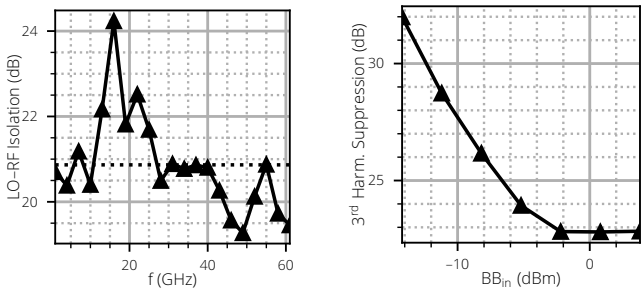
Figure 5.8: Simulated and measured DC output voltage of the RF power detector characterizing the available signal power provided by the LO buffer in front of the wideband modulator. [Ste8] © IEEE 2022

by the integrated power detector. Both measured and simulated output voltage for given input powers are given in Fig. 5.8. The measured values are well predicted by the simulation. Accordingly, the LO buffer amplifier can be assumed to operate as expected. Shown in Fig. 5.9a, is an input power sweep of the LO input power at a baseband frequency of 19 GHz at a constant baseband power of –4 dBm. Simulation and measurement results fit together well within a 2 dB deviation towards the end of the sweep. A likely reason for this is a deviation in the maximum output power of the input buffer amplifier. Fixing the LO input power at –15.8 dBm and the baseband input frequency at 19 GHz the baseband power is swept from –14.2 dBm to 3.8 dBm as shown in Fig. 5.9b. The simulation agrees well with the measurement. A vertical line marks the 1-dB-compression point compared to the linear gain marked by the dotted line at iP_{1dB}=–7.1 dBm.
Finally, unwanted harmonics are investigated in Fig. 5.10. A typical problem for modulated signals is LO-feedthrough directly interfering with the data transmission. As depicted in Fig. 5.10a, the LO suppression is 20.7 dB in average, while the value remains nearly constant over the entire baseband frequency range. Due to the differential structure, the circuit architecture inherently suppresses any second harmonic signal well. The third harmonic signal, however, can interfere with neighboring channels. A minimum suppression of –22.1 dB



(a) (b)

Figure 5.9: Simulated and measured input power sweep of the wideband modulator for a baseband input frequency of f_{BB} = 19 GHz. (a) Baseband input power sweep with the vertical line marking the 1 dB-compression point. (b) Local oscillator input power sweep. [Ste8] © IEEE 2022



(a) (b)

Figure 5.10: Measured suppression of unwanted harmonics of the wideband modulator at a baseband input frequency of f_{BB} = 19 GHz. (a) Suppression of local oscillator signal with the resulting mean marked as a dotted line. (b) Suppression of the third inter-modulated harmonic. [Ste8] © IEEE 2022

is achieved. In an integrated system this is further enhanced by subsequent bandpass amplifier stages.

Conclusion

This chapter proposes an ultra-wideband double-balanced mixer with an analog bandwidth of more than 100 GHz enabling BPSK operation with data transmission speeds up to 100 Gbps. The performance is achieved by analyzing the effects of possible signal feeding orders. Supplying the BB signal to the lower transistor pair allows for very broadband resistive matching of the baseband input port. Overall this circuit trades maximum conversion gain for bandwidth. Tab. 5.1 compares the performance of state-of-the-art mixer and modulator circuits. The mixer core consumes the lowest DC power of only 27.2 mW, while the core area is 0.158 mm^2. This work exceeds the second highest absolute bandwidth by 23 % [187] achieving an output spectrum up to 85 % of the transit frequency. At –13 dB of conversion gain, this work is competitive to the compared modulator cores without baseband or output amplifier and even outperforms designs in a III/V technology [180]. This is accompanied with a high LO isolation of 20.7 dB and a third harmonic suppression of 22.1 dB enabling reliable data transmission.

Table 5.1: State of the art of current millimeter-wave phase-shift keying (PSK) modulator circuits.

	This	[180]	[181]	[182]	[30]	[187]
Modulation	BPSK	QPSK	Quadrature	OOK, IQ	BPSK	Quadrature
Technology	130 nm SiGe BiCMOS	250 nm InP HBT	130 nm SiGe BiCMOS	130 nm InP HBT	130 nm SiGe BiCMOS	130 nm SiGe BiCMOS
f_t (GHz)	350	350	350	—	300	350
Center frequency (GHz)	245	300	190	630	240	180
Bandwidth (GHz)	103.9	30	17	30	35	80
Relative bandwidth (%)	42.4	10	8.9	4.8	14.6	44.4
LO power (dBm)	-15.84	-5	-10.3	0	-5	-5
IF power (dBm)	-2.2	-3.5	-3	-6	-8	-11
Buffers	LO	No	RF	RF	BB, LO, RF	BB, LO, RF
Conversion gain (dB)	-13	-15	-3	—	9	10
LO – RF isolation (dB)	20.7	25	—	10	23	8
Output P_{sat} (dBm)	-16.8	—	-6	-31.5	-2.3	3.5
Area (mm^2)	0.906	0.986	1.462	1.37	1.25	1.4
DC power (mW)	27.2	40	36.5	200	375	151

6. Broadband BPSK Transmitter System for Datarates up to 56 Gbps

The circuit presented in this chapter was published in [Ste4]. Great thanks go to *Joachim Hebeler (KIT, Karlsruhe)* for his cooperation and significant contributions, which are specified in detail in the following chapter.
The proposed circuit extends the achievable measured datarates of BPSK transmitters operating at frequencies higher than 200 GHz to more than 50 Gbps. This was done with a focus on low power consumption resulting in a transmitter efficiency even exceeding systems employing high-order modulation schemes. Additionally, this circuit features local oscillator (LO) signal phase control allowing beam steering in transmitter arrays. By combining the output power of many transmitters, the free space path loss (FSPL) accompanying the very high channel frequency can be counteracted in this way.
The system was designed to enable the flexible combination of multiple transmitters. This allows for modularity and adaptability optimizing for, either, maximum transmitted RF power in long-distance, or low signal-to-noise ratio (SNR) scenarios or low-power consumption for mobile and battery powered applications. This is enabled by a physically narrow layout of the fabricated integrated circuit (IC) to minimize the distance between neighboring transmitters and, therefore allow suitable antenna spacing, as described in section 4.1.5.

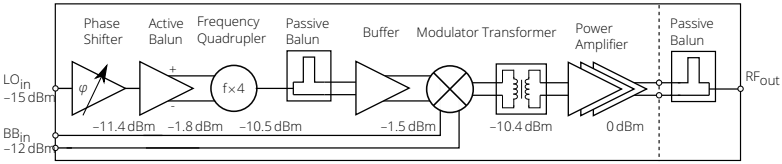


Figure 6.1: Overview of the proposed transmitter architecture. The LO chain consists of an active 90° phase shifter [Ste5], an active balun [Ste6], a PCPP quadrupler [Ste6] and a buffer. After the broadband modulator [Ste8], the signal is amplified by a three-stage power amplifier [191]. The simulated signal power budget is given for a single-tone input signal at an output bandwidth of 52 GHz. [Ste4] © IEEE 2022

6.1. System Architecture

An overview of the modules in the designed system is given in Fig. 6.1 with simulated signal power values at a RF bandwidth of 52 GHz noted for each stage of the transmitter.

An externally generated 61.5 GHz LO signal is fed to the circuit. At the input, an active 90° phase shifter [Ste5], presented in section 4.2.1, buffers the LO signal and allows for precise phase control enabling LO based beam steering, as described in section 4.1.6. The phase-shifter first architecture moves complexity from the broadband RF section to the narrowband LO chain. Placing the phase shifter in front of the frequency multiplication stage, enables the optimization for gain and output power to drive the subsequent stages. A slight penalty in area consumption is caused by the inherently larger passive structures. From a 2.6 V supply, 1.9 mA and 5.5 mA are consumed by the direct current (DC) bias control circuitry and the phase shifter core, respectively, totaling to a power consumption of 19.2 mW. An active balun based on an asymmetrically excited differential cascode circuit, with capacitive coupling for improved phase and magnitude balance, converts the single-ended LO signal to differential and drives the frequency multiplication-by-four stage [Ste6]. These circuits are further analyzed in section 3.4. In contrast to [Ste6], the inductor based input matching network was replaced with a transmission line based inter-stage matching network. A 4 V source supplies 41.2 mW to the active

balun including all bias circuitry. A phase-controlled push-push (PCPP) architecture, described in section 3.2, was chosen for the frequency quadrupler circuit for its high area efficiency and low power consumption. Both characteristics are enabled by alleviating a second stage entirely in comparison to more conventional 2×2 frequency multiplication circuits based on the push-push architecture [96], [100]. Building on [Ste6], an improved input and output interstage matching network enables a lower conversion loss and a smaller footprint. During operation, the circuit is simulated to consume 21.4 mW from a 2 V supply. Completing the LO chain, a delay line balun feeds the LO signal to a buffer amplifier based on a differential cascode with a transmission line based output network for interstage matching. By choosing $N_x = 2$ [63] transistors, the circuit was optimized for high gain and output power to drive the modulator into LO saturation. All transistors are biased with 1.2 V of V_{CE} to enable a high signal swing while avoiding collector-emitter breakdown. In total, 43.5 mW of DC power from a 3.6 V supply is consumed by the buffer amplifier. Overall, the LO chain provides approximately 13.5 dB of power gain while multiplying the frequency of the input signal. This allows low LO input power levels while ensuring maximum output power of the subsequent modulator. Additionally, by requiring a lower frequency signal at the input, the complexity of all associated feeding networks, frequency generation circuits and phase-locked loops (PLLs), in a scaled array, can be significantly reduced.

A broadband BPSK modulator, based on [Ste8] described in chapter 5, based on a Gilbert cell is fed by a differential baseband (BB) input and driven by the LO chain explained above. The signal feeding order was adapted with the BB signal being supplied to the upper transistors and the LO signal connected to the lower transistors. This enables an in-line arrangement of the circuit elements in the system layout reducing the area consumption of the system considerably, without changing the proven modulator core significantly. Fig. 6.2 depicts the resulting schematic. Transistor Q_1 operates as a current source with emitter degeneration for improved operation point stability. It is scaled by $N_x = 4$ [63]. $Q_{2,3}$ and $Q_{4,\ldots,7}$ are binary scaled with each stage halved in size. By supplying the BB signal to the upper transistors, a differential cascode circuit is formed for every bit period reducing the Miller effect and, therefore, optimizing the operating bandwidth. A transformer based output network both matches the modulator to

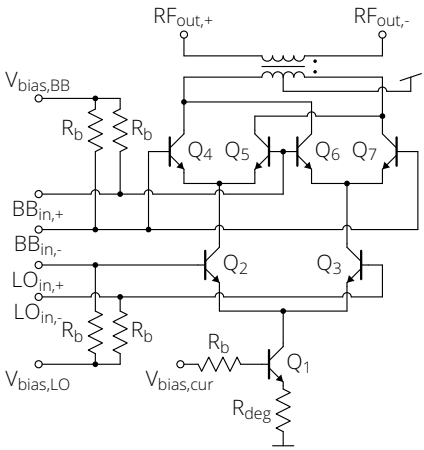


Figure 6.2: Simplified schematic of the modulator used in the broadband transmitter based on a Gilbert cell architecture with a transformer output stage. [Ste4] © IEEE 2022

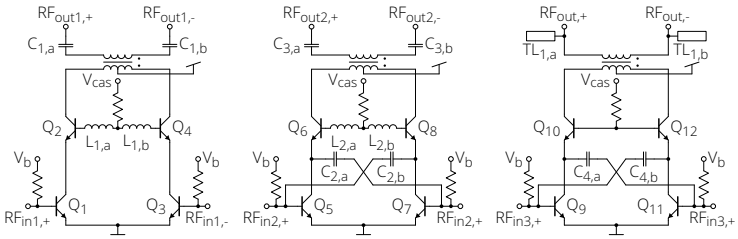


Figure 6.3: Simplified schematic of the three-stage differential power amplifier at the output of the broadband transmitter [191]. [Ste4] © IEEE 2022

the power amplifier input and feeds the 3.6 V supply via a center tap. A total of 34.9 mW is consumed.

The power amplifier, shown in Fig. 6.3, was contributed by the author's project partner *Joachim Hebeler (KIT, Karlsruhe)* and is based on [191]. It features a three stage design of cascaded pseudo-differential cascodes for reduction of the Miller effect. While the transistors of the first stage are scaled by four times the unit size [63] to limit power consumption and input capacitance, the latter stages feature transistors scaled to eight times the unit size. The first two stages add base inductors to the upper transistor pairs for an improved frequency response [192]. This is aided further by capacitive neutralization in the last two stages [193]. Low impedance open stubs match the power amplifier to the 100 Ω differential output. Combined, the three stages consume 250 mW from separate 3 V and 4 V supplies.

Finally, a passive, folded *Marchand* balun [194] was designed by *Joachim Hebeler (KIT, Karlsruhe)*, which can be connected via a ground-signal-signal-ground (GSSG) bond interface, enabling the characterization and probing in the laboratory.

6.2. Measurement Technique and Results

The fabricated chip, shown in Fig. 6.4, measures 837 µm × 1920 µm = 1.6 mm^2. Including all pads, the transmitter consumes 1514 µm × 765 µm = 1.158 mm^2 of this with the rest being used by the passive balun interface enabling probing in the laboratory which can later

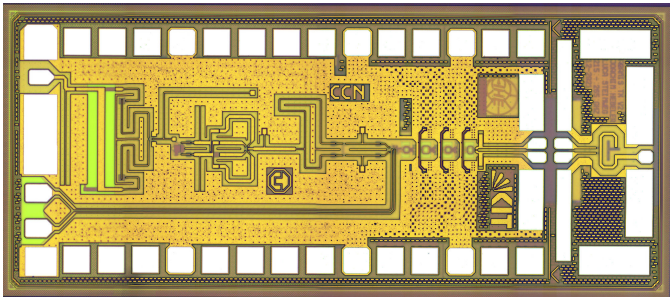


Figure 6.4: Photograph of the fabricated fully integrated transmitter circuit. A total silicon area of 837 µm × 1920 µm = 1.6 mm^2 is used with the transmitter consuming 1514 µm × 765 µm = 1.158 mm^2. [Ste4] © IEEE 2022

be removed with a full-cut laser dicer and replaced by an antenna connected via a bond wire interface [13]. Excluding the pads, the transmitter uses less than 0.7 mm^2, exemplifying the potential for a very area efficient integration in a larger system. A RF PCB was designed, depicted in Fig. 6.5, enabling the characterization of a single transmitter chip in the laboratory. All necessary DC supply voltages are fed via a flat ribbon cable. Both the single-ended LO and differential BB signals are supplied via edge-mount 1.85 mm connectors and fed to the circuit via transmission lines optimized by electromagnetic simulation. The IC is placed in a precisely designed cavity to minimize the length of the bond wire connections. GSG and GSSG configurations, respectively, were employed with optimized PCB geometries to further minimize the attenuation and maximize the matching at the BB and LO signal ports. In a larger array system the package size and complexity could be reduced by mounting the ICs with flip-chip technology. The total power consumption during operation of 412.7 mW divides into 127.7 mW for the LO chain, 33.9 mW for the broadband modulator and 251.1 mW consumed by the power amplifier at the output. Fig. 6.6 shows the power consumption distribution with the power amplifier (PA) using approximately 60 % of the total DC power.

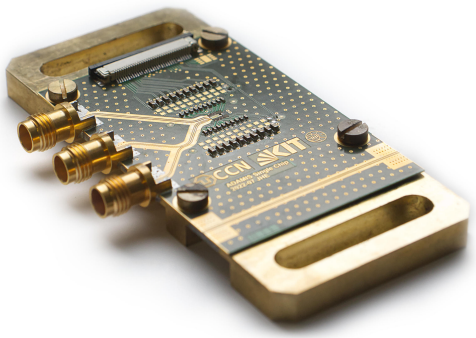


Figure 6.5: Photograph of the designed RF PCB feeding the LO and BB signals and DC voltages to the broadband transmitter IC.

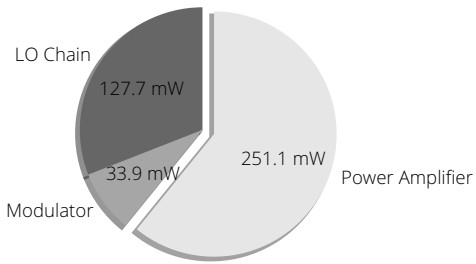


Figure 6.6: Distribution of the DC power consumption of the main hierarchical system blocks of the broadband transmitter.

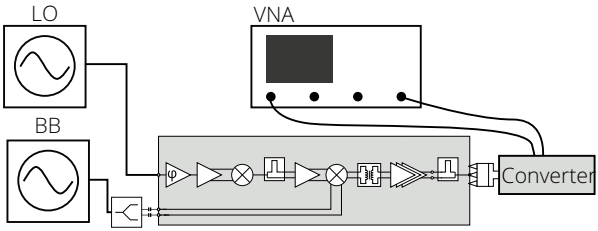


Figure 6.7: Simplified overview of the measurement setup used for the small-signal characterization of the broadband transmitter. [Ste4] © IEEE 2022

Small-Signal Characterization

The small-signal characteristics were recorded with the measurement setup shown in Fig. 6.7. A vector-network analyzer (VNA) operating up to 67 GHz was calibrated at the reference planes of an attached 1.85 mm RF cable. The matching behavior was done single-ended for each separate connector. A frequency converter module, operating from 220 GHz to 330 GHz, with a waveguide S-bend and ground-signal-ground (GSG) probe was then calibrated at the probe tip with a reference substrate to characterize the output. At the LO port, a match of better than –10 dB is achieved in the band around the input channel frequency of 61.5 GHz as shown in Fig. 6.8a. Mixed-mode S-parameters were calculated in software from the single-ended measurement results at the BB ports [195]. The resulting differential-differential input match is shown in Fig. 6.8b. The reflection coefficient is below –9 dB for frequencies higher than 20 GHz. Fig. 6.8c shows the output reflection factor at the output of the passive balun enabling direct probing. A match of better than –4 dB is measured for the full characterized frequency range from 220 GHz to 330 GHz with minima at 237.5 GHz and 286 GHz.

Large-Signal Characterization

The measurement setup for the large signal characterization is presented in Fig. 6.9. Two laboratory signal sources with tightly coupled reference signals supply sine signals to both the LO and, via an external

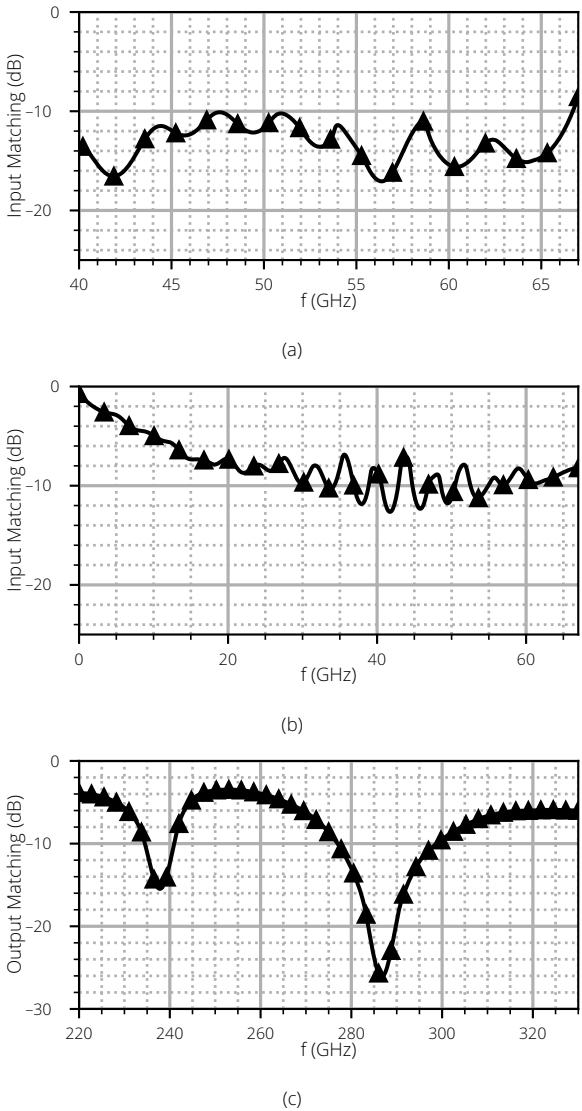


Figure 6.8: Measured reflection coefficients of the the broadband transmitter. (a) Input reflection factor at the LO port. (b) Input reflection factor at the BB port. (c) Output reflection factor at the RF pad. [Ste4] © IEEE 2022

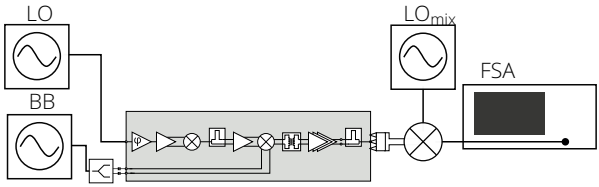


Figure 6.9: Simplified overview of the measurement setup used for the large-signal characterization of the broadband transmitter. [Ste4] © IEEE 2022

balun operating up to 67 GHz, the differential BB ports. External capacitors provide DC decoupling at the BB inputs. All ports were 2D power calibrated at the connectors for all measured frequency and power level combinations. This assures reliable and constant input power values over the entire band of operation and compensates for the frequency dependent attenuation of the cables and connectors as well as possible power variations of the signal sources. An external waveguide mixer with up to 40 GHz of available intermediate frequency (IF) bandwidth is directly connected to the probe operating as a receiver. The necessary LO signal (LO_{mix}) is supplied by a third laboratory signal source and internally multiplied with a factor of 24. By introducing a 240 MHz offset to the transmitter LO signal, a low-IF receiver architecture is possible allowing the characterization of both the sidebands and the LO feedthrough. Both LO signal sources are tightly coupled with a 1 GHz synchronization signal to achieve the best possible relative frequency and phase stability. A frequency spectrum analyzer (FSA) operating up to 67 GHz is used to evaluate the output signal of the receiver mixer.

First, the RF output spectrum, shown in Fig. 6.10, is measured and analyzed. The RF bandwidth $f_{RF} = f_{LO} \pm f_{BB}$ is analyzed up to 52 GHz between the two first-order mixing products. A quadratic fit of the measured RF output power is given as a dashed gray line to provide a higher resolution bandwidth calculation. At a LO power of –10 dBm and a BB power level of –5 dBm, simulation and measurement results agree within an up to 4 dB lower measured output power at the end of the band. 3.5 dBm of maximum RF output power is reached at the minimum measured bandwidth of 2 GHz. This results in a power-added

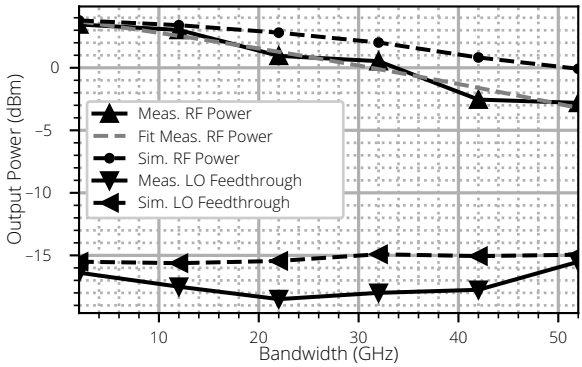


Figure 6.10: Simulation and measurement results of the output power and LO feedthrough of the broadband transmitter at a LO and BB power levels of –10 dBm and –5 dBm respectively. [Ste4] © IEEE 2022

efficiency (PAE) of 0.44 % and a RF efficiency of 0.54 %. Due to the stronger roll-off compared to the simulation, the 3-dB-bandwidth is 26.15 GHz. Simulated and measured LO feedthrough match well, resulting in a LO power level of approximately –17 dBm resulting in a LO suppression of more than 12 dB across the spectrum. The slow roll-off of the output power qualifies the transmitter circuit for high data-rates. Ensuring that the LO chain is capable to drive the modulator into saturation, the LO input power is swept in Fig. 6.11 at a bandwidth of 52 GHz and a BB power level of –5 dBm. The losses introduced by the PCB transmission lines are de-embedded by means of a reference measurement of a thru connection with two edge-mounted connectors. It is clear that a LO input power of –29 dBm suffices to drive the output into saturation.

A BB power sweep, shown in Fig. 6.12 for a bandwidth of 52 GHz and a LO power level of –10 dBm, characterizes the linearity of the system. Here, both the modulator and power amplifier behavior are superimposed. As above, the losses caused by the PCB assembly excluding the bondwire interface are de-embedded. Simulation and measurement agree within a stronger compression of the measurement leading to

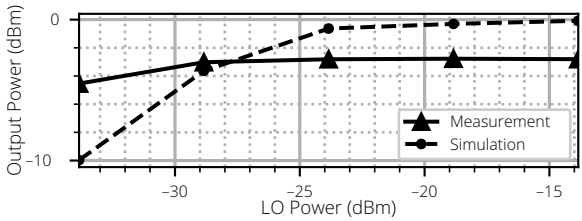


Figure 6.11: Simulation and measurement results of the LO power sweep of the broadband transmitter at a bandwidth of 52 GHz and −5 dBm of BB power. [Ste4] © IEEE 2022

a lower saturated output power as seen before in Fig. 6.10. A iP_{1dB} of −15.40 dBm produces an output power of oP_{1dB}=−6.25 dBm. Accordingly, a linear gain of 10.15 dB is achieved.
With the LO frequency being up-converted in the LO chain, there exists no reference phase for the characterization of the phase shifting performance at the output. As a direct measurement of the phase at the output is, therefore, impossible, a measurement technique was developed to enable the characterization of the LO phase tuning at the RF output. The BB signal source is turned off and a 100 kHz sine signal is connected to the phase tuning input repeatedly sweeping the phase over the full input range from 1 V to 2.5 V. As a result a phase modulated output signal centered at the LO frequency can be observed and is recorded by a real-time oscilloscope (RTO) replacing the spectrum analyzer. The signal is then further processed in a software I-Q receiver to recover the phase information. By fitting a sine signal to the first four periods of the signal, a synthetic reference signal can be determined for the receiver. This is possible with minimum error, as the phase tuning is much slower than the down-converted LO at 240 MHz. Fig. 6.13 shows the matching simulated and measured phase steering behaviors. Both results produce the expected linear characteristic enabled by the employed DC steering circuit [Ste5]. A total phase range of 380° is measured. By setting the I and Q paths of the vector phase shifter off quadrature by some degrees, and, thus, increasing the total

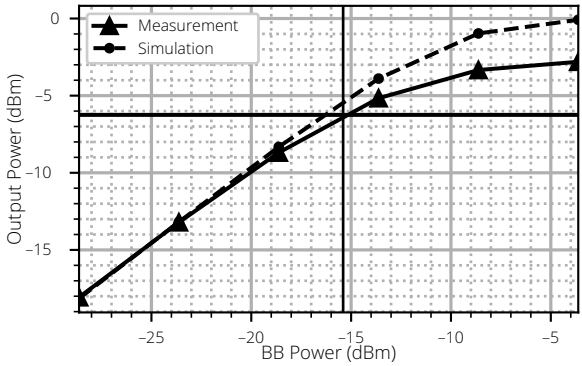


Figure 6.12: Simulation and measurement results of the BB power sweep of the broadband transmitter at a bandwidth of 52 GHz and −10 dBm of LO power. [Ste4] © IEEE 2022

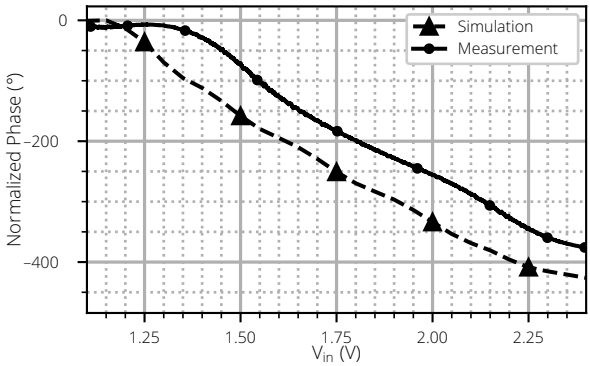


Figure 6.13: Simulation and measurement results of the LO phase steering behavior of the broadband transmitter over the full tuning range from 1 V to 2.5 V. [Ste4] © IEEE 2022

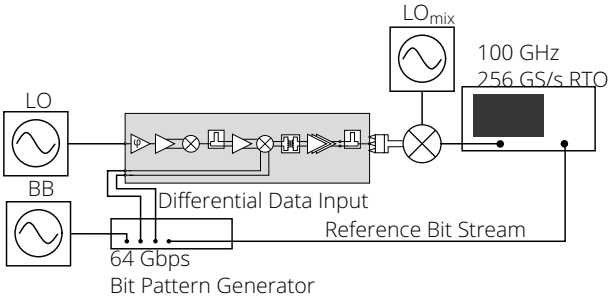
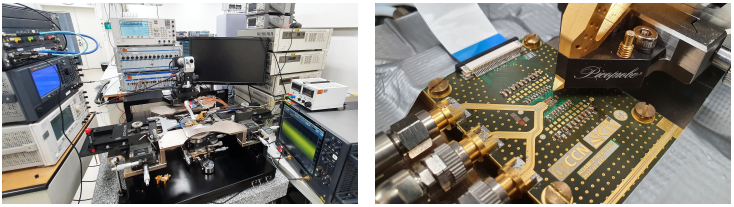


Figure 6.14: Overview of the measurement setup to evaluate the data transmission behavior and bit rate of the broadband transmitter. [Ste4] © IEEE 2022

phase range, the most linear section of the phase control can be used further simplifying the beam steering.

BPSK Transmission Characterization

The measurement setup is extended with a bit pattern generator capable of data rates up to 64 Gbps, feeding a pseudorandom binary sequence (PRBS)-31 signal to the transmitter IC as shown in Fig. 6.14. The advantage of using long PRBS sequences is that high randomness in the data is achieved including long series of zeros or ones which places high demands on the transmitter. At the output of the transmitter, a laboratory broadband receiver mixer is connected via a GSG probe. The down-converted signal is then digitized by a high-sampling-rate RTO. A photo of the assembled measurement setup is shown in Fig. 6.15a with a closeup of the PCB mounted on the wafer prober chuck depicted in Fig. 6.15b.
The modulated signal is first down-converted to a center frequency of 30 GHz, 20 µs time frames are recorded at 256 GS/s. Enabling the bit error rate (BER) calculation, the input data stream from the bit source is mirrored at a third output and fed directly to the second channel of the RTO as a reference. The transmitter was characterized for data rates from 16 Gbps to 60 Gbps in 4 Gbps steps. With most publications in the literature characterizing full transmitter-receiver chains to



(a) (b)

Figure 6.15: Photographs of the bit rate measurement setup for the broadband transmitter in the research laboratory. (a) Display of the measurement setup for the data transmission characterization. (b) Closeup of the RF PCB fully operational and mounted on the wafer prober chuck. [Ste4] © IEEE 2022

overcome the high bandwidth demands [29], [30], [33], [196], this approach, by employing a commercially available laboratory receiver featuring the highest IF-bandwidth of 40 GHz, enables the characterization of the transmitter stand-alone. Hereby, any uncertainties introduced by antennas, the receiver circuit or the mechanical alignment within the measurement setup can be avoided.

The very broadband nature of this transmitter IC poses a tough challenge towards the measurement setup and software-based analysis post-measurement: With the proposed transmitter being capable of data rates higher than 50 Gbps and a low-IF hardware receiver architecture, the available IF-bandwidth of the measurement equipment is exceeded. The maximum possible data rate is further limited by the maximum possible sampling rate of the RTO as full IQ-demodulation is not available. With the baseband signal covering a high percentage of the available receiver bandwidth, the filtering of unwanted or interfering signal components is challenging. Avoiding self-interference of the sidebands necessitates a high-order filtering of the RF signal. Eliminating one sideband entirely leads to a non-constant envelope of the baseband signal which, in turn, leads to a reduced eye-opening. Additionally, feedthrough of the low-frequency signal LO_{mix} in the receiving mixer overlays the IF signal resulting in coherent noise. A precise,

narrow-band digital filter is needed to avoid the degradation of the SNR. With the very high used bandwidths, the signal power is spread over a large frequency band. At the same time, the noise power

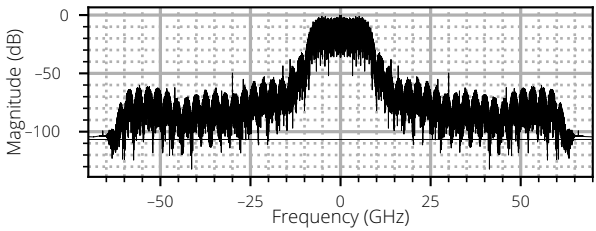
$$P_{\text{noise,therm}} = k \cdot \zeta \cdot BW, \tag{6.1}$$

with the *Boltzmann* constant k, is proportional to the bandwidth BW at a given temperature ζ. This results in an increase in thermal noise by 5.74 dB for the characterized data rates. The RTO features an effective number of bits (ENOB) of only five bit at the maximum bandwidth. At a full scale amplitude of 160 mV, this results in a voltage resolution of 5 mV. The manufacturer states a RMS noise of 1.5 mV. Together, this results in degradation of the SNR in terms of raising the noise floor by approximately 25 dB from 16 Gbps to 60 Gbps which is visible in the measured spectra shown in Fig. 6.16. Finally, the coaxial cable, used to connect the receiver to the RTO can introduce an additional frequency dependent attenuation of up to 2 dB. Combined with the reduced precision for low signal levels in the RTO, this can result in non-recoverable loss of information.

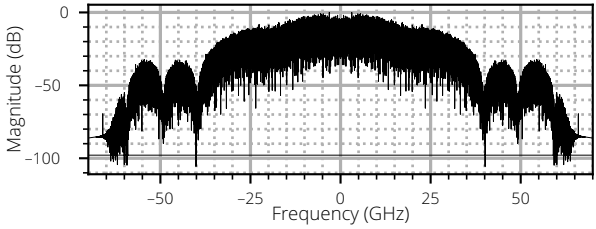
Fig. 6.17 shows the architecture of the software-defined receiver devised by *Joachim Hebeler (KIT)*. First, the necessary LO signal is recovered by analyzing the LO feedthrough of the transmitter for every measured time frame. A precise determination of the frequency and phase of the signal used for the down-conversion in software is crucial to achieve a coherent receiver. By using the information in the LO leakage signal, most of the possible drift in phase or frequency can be compensated. After applying a matched filter with a filter factor of 0.35, the reference bit timing is aligned and the received signal is sampled.

The resulting eye diagrams are shown in Fig. 6.18 for data rates ranging from 16 Gbps to 60 Gbps. With the maximum data rate providing a reasonably open eye of 56 Gbps and the total system power consumption of 414 mW, the transmitter is measured to be very efficient at 7.4 pJ/bit. Higher data rates can be possible with an improved measurement setup with higher bandwidth or a specifically designed integrated receiver system.

By aligning the reference bit stream, captured at the second channel of the RTO, with the demodulated and sampled received signal, a BER can be determined for every measured data rate as shown in Fig. 6.19. Special care must be taken to compensate any path delay differences to achieve meaningful results. An equalizer is employed to correct the



(a)



(b)

Figure 6.16: Measured normalized spectrum of the IF signal of the broadband transmitter at (a) 16 Gbps and (b) 60 Gbps. The spectrum was calculated via a fast fourier transform of the measured time series data.

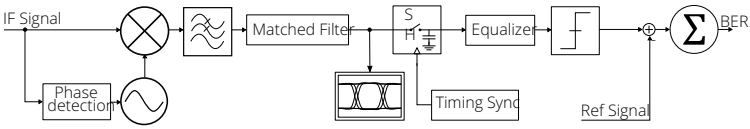


Figure 6.17: Simplified block diagram of the software-defined receiver architecture devised for the characterization of the broadband transmitter. [Ste4] © IEEE 2022

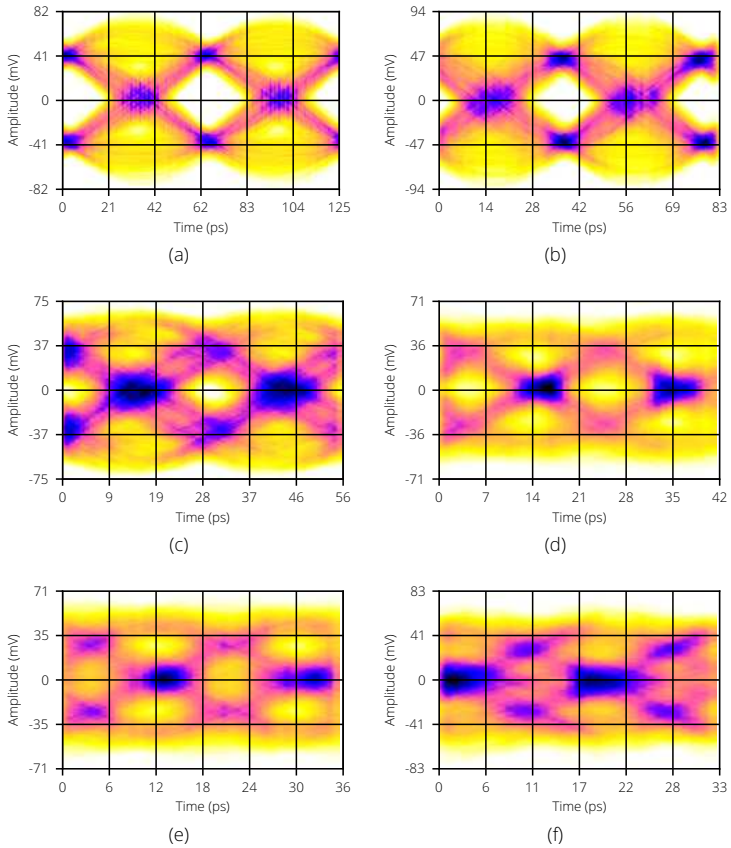


Figure 6.18: Eye diagrams measured at the output balun of the broadband transmitter. (a) 16 Gbps. (b) 24 Gbps. (c) 36 Gbps. (d) 48 Gbps. (e) 56 Gbps. (f) 60 Gbps. [Ste4] © IEEE 2022

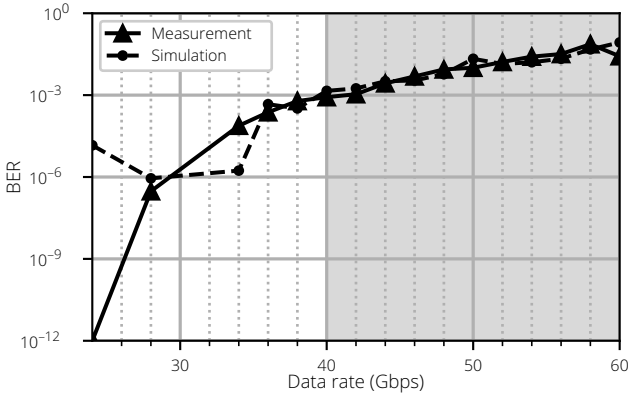


Figure 6.19: Measured bit error rate for data rates of the broadband transmitter up to 60 Gbps. The measurement range exceeding the 3-dB-bandwidth of the laboratory receiver is marked in gray. [Ste4] © IEEE 2022

frequency-dependent characteristics of the measurement equipment. Very low BERs require a very high number of measured bits N_{bits} to achieve a targeted confidence level CL. The number of recorded bits, measurement duration and volume of data to be stored and analyzed must therefore be weighed against each other. Here, the necessary number of bits was estimated for $CL = 0.95$ and a BER of $5 \cdot 10^{-8}$ per

$$N_{\text{bits}} = -\frac{\ln(1 - CL)}{BER}, \tag{6.2}$$

resulting in $N_{\text{bits}} \approx 60 \cdot 10^{6}$. Again, the transmitter exceeds the bandwidth of the available measurement equipment, illustrated by the gray background in Fig. 6.19.

6.3. Summary and performance comparison

A proof of feasibility of a fully integrated wideband transmitter with LO phase steering is presented combining the theoretical and practical

research findings of this thesis. A maximum data rate of 56 Gbps was achieved using BPSK modulation, thus avoiding highly complex and power consuming digital baseband processing typical for high-order modulations. The system shows that broadband systems, exploiting the large available bandwidth in the mm-wave spectrum, can deliver similar or even higher data rates as transmitters employing complex modulation types while reducing the transmitter and systematic power consumption. This was achieved while incorporating a LO quadrupling stage with integrated 360° phase control allowing beam steered applications. Additionally, this enables a simpler LO signal distribution network in the 60 GHz band for large transmitter array systems. Compared to the state of the art presented in Tab. 6.1, this transmitter doubles the highest reported data rate to date for BPSK systems to 56 Gbps. These results can potentially be further increased once wideband measurement setups become available. Earlier publications reach comparable data rates but do not include LO chains nor power amplifiers [29], heavily limiting the usability in actual applications. The high output power of 3.5 dBm with a power consumption of 414 mW produces a RF efficiency of 0.54 %, doubling the next highest compared value [33]. Further highlighting the efficiency of the proposed circuit, a transmitter efficiency of 7.4 pJ/bit equals to a reduction in energy per bit of 70 % compared to other complete transmitters employing BPSK modulation [30], [196]. Studying higher-order modulation schemes, the transmitter efficiency is 50 % higher than the compared QPSK system [33] and even improves upon a 16-QAM system [34] by 23 %. These values are calculated ignoring the power consumption introduced by the digital-to-analog converter (DAC) stages in the BB chain necessary for high order modulation schemes which would further increase the advantage of the presented system.

Table 6.1: Current state-of-the-art of millimeter wave transmitters in 130 nm SiGe BiCMOS technology operating at frequencies above 200 GHz.

	This Work	[30]	[196]	[33]	[29]	[34]
Modulation	BPSK	BPSK	BPSK/ QPSK	QPSK	BPSK	16-QAM
Transmitter modules	360° LO-Phase Steering, LO×4, LO Buffer, Modulator, PA	BB Buffer, LO×8, LO Buffer, Modulator, PA	LO×16, LO Buffer, IQ-Modulator, PA	LO×16, LO Buffer, IQ-Modulator, PA	LO Buffer, Modulator	LO×16, LO-Buffer, IQ-Modulator, BB-Buffer, PA
Center frequency (GHz)	246	240	240	230	190	230
3 dB bandwidth (GHz)	26.15	35	20	35	60	28
$P_{RF,TX}$ (dBm)	3.5	-0.8	-4.4	4.5*	-6	5
iP1dB (dBm)	-15.4	-25	-15	—	-7	-14
Data rate (Gbps)	56	25	25	65	40/ 50	100
P_{DC} (mW)	414	625*	1033	960	32	960
η_{RF}† (%)	0.54	0.13	0.04	0.29	0.78	0.33
Transmitter efficiency (pJ/bit)	7.4	25.0	41.3	14.8	3.9/ 3.1	9.6
Area (mm^2)	1.16	1.25	1.61	1.40	0.70	1.52

†: $\eta_{RF} = P_{RF,TX}/P_{DC}$; *: estimated

7. Conclusion and Outlook

This research work investigated low power integrated circuits for a broadband binary phase-shift keying (BPSK) transceiver system operating at frequencies higher than 200 GHz capable of datarates up to 56 Gbps, doubling the state of the art, with local oscillator (LO) phase control for beam steering. Optimizations for low-power and broadband operation, exploiting the large available bandwidth at the upper end of the millimeter-wave (mm-wave) spectrum, produce a maximum transmitter efficiency of 7.4 pJ/bit at a power consumption of 411 mW, which are both the best reported for transmitters featuring LO chain, modulator and power amplifier (PA) in this frequency band. The fabricated transmitter can be combined with others to create a flexible and re-configurable beam steered antenna array. This was enabled by the analysis, design and implementation of innovative approaches for frequency multiplication and beam steering in multiple test integrated circuits (ICs) for characterization in the research laboratory. Additionally, a novel architecture for beam steering with minimal beam squint in broadband circuits was devised. With this, the objectives of this work, namely reducing the power consumption, increasing the energy efficiency and maximizing the datarate in a beam steerable transmitter for mobile operation were fully met.

Significant contributions and advances to the state of the art are achieved, outperforming many published performance metrics by some multiples.

A system with low power consumption and excellent efficiency has been designed by optimizing all stages separately while taking into account system requirements by allocating power with maximum effectiveness. Among others this includes:

- The phase-controlled push-push (PCPP) architecture, extending the more established push-push (PP) circuit, for frequency multiplication by four was mathematically modeled and analyzed. A takeaway of the research is the existence of an input signal amplitude optimum that combines high output power with a low-power second harmonic spur. By generating four times the frequency in a single stage and reusing the collector currents in two stacked stages, there is significant potential for high-efficiency systems.

- The designed LO-chain offers a frequency multiplication by a factor of four by employing the PCPP architecture. It is the first circuit of this topology to operate above 200 GHz. Combined with an injection-locked oscillator (ILO), producing 2 dBm of output power, the result is an area- and power-efficient circuit. The power-added efficiency (PAE) is increased by 28.7 % compared to the state of the art while maintaining high output spectrum purity with harmonic rejection of more than 30 dB.

- An active 90° vector-sum phase-shifter was designed for LO beam direction steering. Polyphase filters and electromagnetic (EM) couplers were studied and analytically compared. An EM coupler is preferential due to the significantly lower signal attenuation outbalancing the increased array consumption. A differential bias circuit eliminates the need for one of the two high-resolution digital-to-analog converters (DACs) normally required. The increased power consumption of the circuit of 4.8 mW is justified by the possible reduction in complexity and total power consumption in a larger array system. With the high available saturated output power of about 5 dBm and a gain of more than 10 dB, an additional buffer becomes unnecessary. Due to the low power consumption of 12.1 mW, including the biasing circuit, the PAE was increased 30-fold compared to the state of the art achieving a value of 6.3 %.

- A Gilbert cell-based modulator has been optimized for wideband operation, limiting power consumption to 27.2 mW while maintaining a competitive conversion gain of –13 dB. Further, high-speed and high-resolution, and thus power hungry, converter circuits are avoided in the baseband chain, by optimizing for BPSK as the modulation scheme.

With the very large absolute bandwidth available at the high end of the mm-wave spectrum, low complexity modulation schemes such as BPSK allow high datarates. While many designs use relatively narrowband architectures with high-order modulations, the approach presented in this work avoids complex digital circuits that consume a lot of energy for digital preprocessing of the data streams.

- Different signal feeding architectures for Gilbert cells were analyzed. By supplying the baseband (BB) signal to the lower transistor pair, a broadband, resistive input match from direct current (DC) to more than 50 GHz can be achieved. Based on this, a ultra-wideband mixer circuit was developed that can achieve bandwidths of up to 100 GHz improving the state of the art by 23 %. This enables BPSK-based data transmission with datarates of more than 100 Gbps.

Given the high free space path loss (FSPL) and atmospheric absorption accompanying the high frequencies in the mm-wave spectrum, array systems were studied to counteract the resulting attenuation. Different techniques that allow dynamically steerable arrays of many parallel transmitters have been analyzed and applied in fabricated ICs.

- By combining a 90° phase shifter operating in the 60 GHz frequency range with a high-power frequency quadrupler, phase control of 330° at 225 GHz was achieved. This confirms the theoretical analysis of the direct phase-frequency relation when multiplied. By combining the two circuits, a total power gain of 21 dB was achieved, resulting in a drain efficiency of 0.99 % and exceeding the state of the art by a factor of 40.

- The characteristics of time-delayed and phase-delayed steering were studied. From this, the beam squint resulting from phase-steered systems was identified as an issue and modeled in terms of steering direction and relative bandwidth.

- A novel hybrid phase-time-delayed beam steering architecture with analog beam direction control was devised to both counteract beam squint and minimize the area consumption. A design flow for the architecture was analytically described with the key research finding being that beam squint can be reduced by more than 83 % in an ideal system. This resulted in the design and fabrication of the first time-delay circuit operating at above 200 GHz. By combining a 2-bit time delay stage with a 90° active vector sum phase shifter, signal attenuation can be limited and the chip area can be halved compared to time delay circuits operating in the same frequency band. The system enables more than 75 % reduction in beam squint. Compared to typically large time-delay control circuits, the required area is reduced by 50 %.

The findings and improvements above enabled the subsequent design of the record-breaking BPSK transmitter described.

In future work, the transmitter should be integrated with an optimized on-chip antenna. Alternatively, an off-chip antenna can be connected to the ground-signal-signal-ground (GSSG) interface at the output of the transmitter circuit. It is of great interest to characterize the transmit power in free space. If assembly is required, special care must be taken to make the shortest possible bond connection between the transmitter and the antenna. Flip-chip connections can potentially reduce transition losses and improve matching. The analysis can be extended by combining multiple transmitters into a steerable antenna array. Transmission ranges of up to 10 m seem feasible by focusing the aggregated transmitted power in the direction of the receiver.
Next, the transmitter topology can be easily extended to a quadrature phase-shift keying (QPSK) system. While this requires a redesign of the IC by adding a second modulator, the total area and power consumption are negligible since the modulator in this design consumes less than 0.009 mm^2 and 34 mW, respectively. This allows the datarate to be doubled, resulting in more than 100 Gbps with two orthogonal signals at the same bandwidth.
Finally, a suitable wideband receiver should be developed to provide a full data link. Since the characterization of the transmitter remains limited by the intermediate frequency (IF) bandwidth of the available measurement equipment, there is potential for further improvements

in datarate. Many circuit modules such as the LO chain and modulator can be reused for a receiver design with minimal adjustments.

In conclusion, the goals of this thesis of designing low power, high efficiency and wideband circuits and architectures for a transmitter system for mobile applications were achieved.
The research presented demonstrates datarates of 56 Gbps, doubling the datarate of state-of-the-art transmitters, featuring a LO chain, a modulator and a power amplifier, using low-order modulation schemes. By focusing on low power consumption and effective allocation of the consumed DC power, the highest reported transmitter efficiency for fully equipped transmitters above 200 GHz was measured at 7.4 pJ/bit. This was achieved while enabling beam steering in large antenna arrays. Many submodules have been characterized to improve the state of the art many times over established performance metrics. Together, the presented, significant technological advances provide a proof of feasibility for next-generation ultra-wideband low-power mobile communication systems.

A. Appendix

A.1. Sixth Order Series Expansion of an Ideal Push-Push Stage

$$I_{c1} + I_{c2} = 2 + \frac{1}{1152}\left(\frac{\widehat{V}}{V_T}\right)^6 + \frac{1}{32}\left(\frac{\widehat{V}}{V_T}\right)^4 + \frac{1}{2}\left(\frac{\widehat{V}}{V_T}\right)^2 \tag{A.1}$$

$$+ \cos(2\omega t)\left(\frac{1}{768}\left(\frac{\widehat{V}}{V_T}\right)^6 + \frac{1}{24}\left(\frac{\widehat{V}}{V_T}\right)^4 + \frac{1}{2}\left(\frac{\widehat{V}}{V_T}\right)^2\right) \tag{A.2}$$

$$+ \cos(4\omega t)\left(\frac{1}{1920}\left(\frac{\widehat{V}}{V_T}\right)^6 + \frac{1}{96}\left(\frac{\widehat{V}}{V_T}\right)^4\right) \tag{A.3}$$

$$+ \cos(6\omega t)\left(\frac{1}{11520}\left(\frac{\widehat{V}}{V_T}\right)^6\right) \tag{A.4}$$

$$+ \ldots \tag{A.5}$$

A.2. Calculation of the PCPP stage in saturation

$$e^{\frac{V_{\text{in},2}}{V_\text{T}}} = e^{\frac{V_{\text{in},1}-V_{\text{c}2}}{V_\text{T}}} + \frac{I_{\text{s,cb}}}{I_\text{s}} e^{\frac{V_{\text{in},2}-V_{\text{c}2}}{V_\text{T}}} \tag{A.6}$$

$$\Leftrightarrow 0 = -e^{-\frac{V_{\text{c}2}}{V_\text{T}}} \left(-e^{\frac{V_{\text{in},1}}{V_\text{T}}} - a \cdot e^{\frac{V_{\text{in},2}}{V_\text{T}}} + e^{\frac{V_{\text{in},2}}{V_\text{T}} + \frac{V_x}{V_\text{T}}} \right) \quad \Big| -e^{-\frac{V_{\text{c}2}}{V_\text{T}}} \neq 0 \tag{A.7}$$

$$\Rightarrow 0 = -e^{\frac{V_{\text{in},1}}{V_\text{T}}} - a \cdot e^{\frac{V_{\text{in},2}}{V_\text{T}}} + e^{\frac{V_{\text{in},2}}{V_\text{T}} + \frac{V_x}{V_\text{T}}} \quad \Big| -e^{\frac{V_{\text{in},2}}{V_\text{T}} + \frac{V_x}{V_\text{T}}} \tag{A.8}$$

$$\Big| \cdot (-1) \Big| \ln \tag{A.9}$$

$$\Rightarrow \frac{V_{\text{in},2}}{V_\text{T}} + \frac{V_x}{V_\text{T}} = \ln \left(e^{\frac{V_{\text{in},1}}{V_\text{T}}} + a \cdot e^{\frac{V_{\text{in},2}}{V_\text{T}}} \right) \quad \Big| -\frac{V_{\text{in},2}}{V_\text{T}} \Big| \cdot V_\text{T} \tag{A.10}$$

$$\Rightarrow V_{\text{c}2} = V_\text{T} \ln \left(a e^{\frac{V_{\text{in},2}}{V_\text{T}}} + e^{\frac{V_{\text{in},1}}{V_\text{T}}} \right) - V_{\text{in},2} \tag{A.11}$$

$$0 \neq a e^{\frac{V_{\text{in},1}}{V_\text{T}}} + e^{\frac{V_{\text{in},2}}{V_\text{T}}} \tag{A.12}$$

$$V_\text{T} \neq 0 \tag{A.13}$$

$$a = \frac{I_{\text{s,cb}}}{I_\text{s}} = \frac{A_{\text{cbj}}}{A_{\text{ebj}}} \tag{A.14}$$

A.3. Expansion of the operation point of a bipolar transistor biased via a base-emitter voltage when supplied with a large input signal of amplitude

$$\bar{I}_c = \frac{1}{2\pi}\int_0^{2\pi} I_s \exp\left(\frac{\hat{V}\cdot\sin(\omega t) + v_{be,0}}{V_T}\right) d\omega t \tag{A.15}$$

$$= I_{C,op}\cdot\frac{1}{2\pi}\int_0^{2\pi} \exp\left(\frac{\hat{V}\cdot\sin(\omega t)}{V_T}\right) d\omega t \tag{A.16}$$

$$= I_{C,op}\cdot \mathbb{I}_0\left(\frac{\hat{V}}{V_T}\right) \tag{A.17}$$

with modified Bessel function [101] $\mathbb{I}_0(x) = \int_0^{2\pi} \exp(x\cdot\sin(\omega t))d\omega t$ (A.18)

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List of Figures

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