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Design of a Sigma-Delta ADC in 65nm CMOS Process

Michael Lee Thompson III

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Michael Lee Thompson III

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Abstract

Analog and digital signals both play a vital role in electrical engineering and the technology of today. As the role of electrical and computer engineers becomes more deeply involved in the development of new technology, an understanding of how these signals are utilized, and what they represent, is a necessity. Due to the inherent limitations involved with analog signals, there is a need for these signals to be accurately and efficiently converted to digital signals for processing. The job of the analog-to-digital converter, or ADC, is to receive this analog input signal (voltage or current) and create a digital representation of it based on a specified number of bits, or resolution. In this paper, the design and testing of a sigma-delta analog-to-digital converter will be presented. An explanation of how each component operates within the system will be discussed and the results of testing each of these components as well as the system as a whole will be provided. It will be seen that from fundamental building blocks such as switched-capacitors, op-amps, and digital logic, a fast and efficient system of converting analog to digital signals can be derived. Sigma-delta converters are an increasingly common architecture of ADC used due to the small number of components needed and the low noise, high resolution conversion offered. Through the process of designing and simulating a very basic sigma-delta converter, the fundamental concepts of integrated circuit design, signal processing, and ADC design will be thoroughly explored.

Acknowledgements

First, I would like to thank Dr. Alan Mantooth for the opportunity to work on this challenging project for the completion of my honors degree. The resources provided by the IC design group allowed me to ask questions and get answers to problems that I wouldn't be able to solve myself. Next, I would like to thank the College of Engineering and specifically the Electrical Engineering department for providing me with a great education and the resources to learn a depth of practical knowledge in a variety of areas contributing to this project including circuits, electronics, digital signal processing, and analog IC design. Finally, I would like to thank my family for their support throughout my college career. My professors have been a great benefit to me on campus, but my family has been with me through everything outside of it and I wouldn't be here today without their encouragement.

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Introduction

An Analog-to-Digital Converter (ADC) simply is any system which converts a continuous analog signal to a discrete digital signal [1]. Analog to digital conversion of signals is most important for providing an input to a computer that can be read and processed. It is important that the converters involved in translating analog signals to digital signals be as accurate as possible in order to preserve as much of the original signal as possible. There are many types of analog-to-digital converters including successive approximation, dual slope, pipelined, flash, and sigma-delta. Each type of converter has various advantages and disadvantages which must be considered for a particular application. This project will involve the design of one such converter: the sigma-delta ADC.

A sigma-delta ADC has the advantage of providing a low-noise, high-resolution output at the cost of a limited sample rate. This trade-off is the result of oversampling- a technique used to sample a signal at a rate much higher than the Nyquist rate [2]. A typical application of a sigma-delta ADC would involve the necessity for a highly accurate input signal recreation without caring as much about the speed of the processing. Such examples include data acquisition, power quality monitoring, and voiceband audio communication.

The next few sections will discuss the signal processing fundamentals needed for an understanding of the sigma-delta ADC architecture. After this background has been introduced, the sigma-delta ADC will be discussed in greater detail followed by a thorough discussion of how each component works and the design process followed. Next, the results of each of the individual components as well as the full ADC will be provided and analyzed. Finally, the conclusions of the project will be drawn and future work involved with the project will be mentioned.

Analog and Digital Signals

The distinction between analog and digital signals can be traced back to the early days of electronic communication. In the 19th century, signals were primarily only analog and consisted of those transmitted as continuous waves of sound, light, or electricity. With the advent of digital computers in the mid-20th century, digital signals emerged as a new way to represent and transmit information. Digital signals were initially used for data processing and storage within these early computers, but eventually, their reliability and efficiency made them an attractive alternative to analog signals in a range of applications including telecommunications and audio recordings. Despite the growing prevalence of digital signals, analog signals continue to be used in many contexts due to their ability to provide a theoretically infinite resolution and a more natural representation of physical phenomena. The historical distinction between analog and digital signals has shaped the development of electronic communication technologies and continues to influence their use today.

Analog signals are continuous waveforms that vary over time and can take on any potential value, while digital signals are discrete, consisting of a series of on-off pulses, typically represented as the binary values 0 or 1. The primary advantage of digital signals over analog signals is their ability to be more resistant to noise and distortion [1]. This is because digital signals are represented as discrete levels, where the tolerance for error can be much greater. On the other hand, analog signals can easily be affected by interference or environmental factors that can alter the shape of the waveform. The difference between a typical analog and digital signal can be seen below (Figure 1).

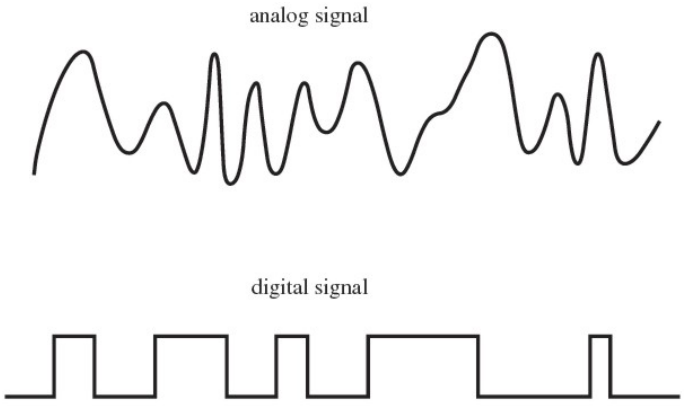

Figure 1: Analog Signal Versus Digital Signal

The benefit of analog signals is that they have a potentially infinite resolution and can provide more precise and accurate information than digital signals. However, due to the inherent limitations of analog signals, most modern communication systems convert these analog signals into digital signals in order to achieve increased reliability and flexibility. Additionally, the infinite-valued continuous analog signals cannot be easily stored in a computer, so there is a need to convert the signal into an approximation of it that can be stored and processed. These two reasons among many others create a need for the existence of an analog-to-digital converter.

Analog-to-Digital Converter Fundamentals

As previously mentioned, an analog-to-digital converter (ADC) is a system that converts an analog signal into a digital signal. The process of conversion typically and primarily involves two main steps: sampling and quantization. During the sampling step, the analog signal is measured at regular intervals, and each measurement is stored as a digital value. The rate at which the signal is sampled is known as the sampling rate, and it determines the highest frequency that can be accurately represented in the digital signal [1]. The next step, quantization, involves mapping the continuous range of analog values to a finite set of digital values. The

number of bits used to represent each sample, known as the resolution, determines the precision of the digital signal. A higher resolution results in a more accurate representation of the analog signal but requires more memory and processing power.

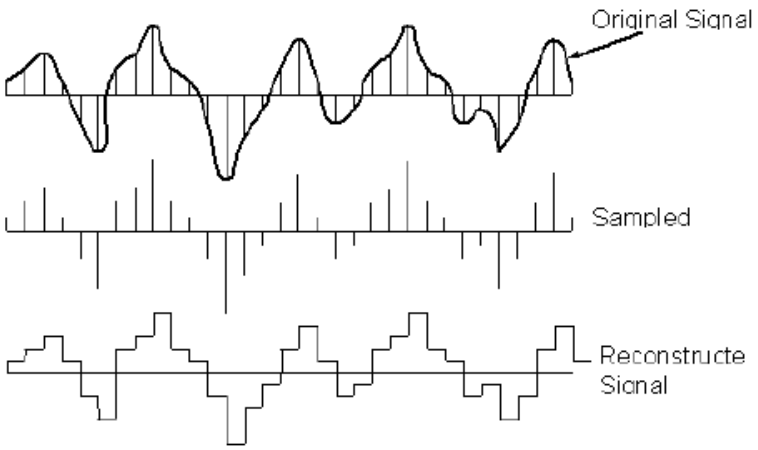

Figure 2: Analog Signals are Sampled and then Reconstructed

Most ADCs are composed of several key fundamental building blocks. The front-end of the ADC is the analog input stage, which buffers the incoming analog signal. The sampling stage primarily consists of a sample-and-hold circuit which is used to hold the voltage level of the input signal constant during the sampling process. The quantization stage uses a comparator that compares the voltage level of the input signal to the voltage reference and generates a binary output signal. Finally, a digital output interface converts the output of the ADC into a real digital representation by using a variety of signal processing and data formatting features.

ADCs can be implemented using different architectures and topologies, such as successive approximation, delta-sigma, flash, and pipeline. The choice of topology is chosen depending on the specific requirements of the application, such as sampling rate, resolution, power consumption, and noise performance. In the next section, the advantages and disadvantages of each of these different architectures will be discussed.

Analog-to-Digital Converter Architectures

The different ADC architectures, including successive approximation, flash, pipeline, and sigma-delta have their own unique strengths and weaknesses. Successive approximation ADCs are one of the most popular architectures because of their good balance between speed and resolution [3]. They have moderate power consumption and can provide decent resolution. Flash ADCs are the fastest of all the architectures and are used in high-speed applications such as video processing. However, they are limited in resolution and typically have lower power efficiency. Pipeline ADCs offer high sampling rates and moderate to high resolution, making them well-suited for high-speed and high-resolution applications. They are widely used in communication systems, video processing, and instrumentation. Finally, sigma-delta ADCs have excellent resolution and are widely used in audio applications [4]. They employ oversampling techniques to achieve high resolution with relatively low sampling rates. Ultimately, the choice of ADC architecture depends on the specific requirements of the application, such as sampling rate, resolution, power consumption, and noise performance [5].

The Sigma-Delta Converter

A Sigma-Delta Analog-to-Digital Converter is used for converting an analog signal to a high-resolution digital signal. This high resolution is achieved primarily through the concept of oversampling. Oversampling is the process of sampling a signal at a frequency rate much higher than the bandwidth of the signal [1]. This rate is much higher even than the Nyquist rate (which is defined as twice as large as the bandwidth of the signal). Oversampling has the effect of greatly increasing the resolution of the signal at the cost of reducing throughput. The reduction in throughput is due to the relatively large amount of time needed to sample the signal. In addition

to providing a higher resolution recreation of the analog input signal, oversampling also has the effect of increasing the signal-to-noise ratio and avoiding aliasing.

There are many components which go into the creation of a sigma-delta ADC system. The primary functional units are a difference amplifier, integrator, comparator, and DAC (Digital-to-Analog Converter). These components are arranged in such a way to produce a feedback system of which the block diagram can be seen below [3, Figure 3]. The importance of each of these components will be discussed in greater detail later in this section.

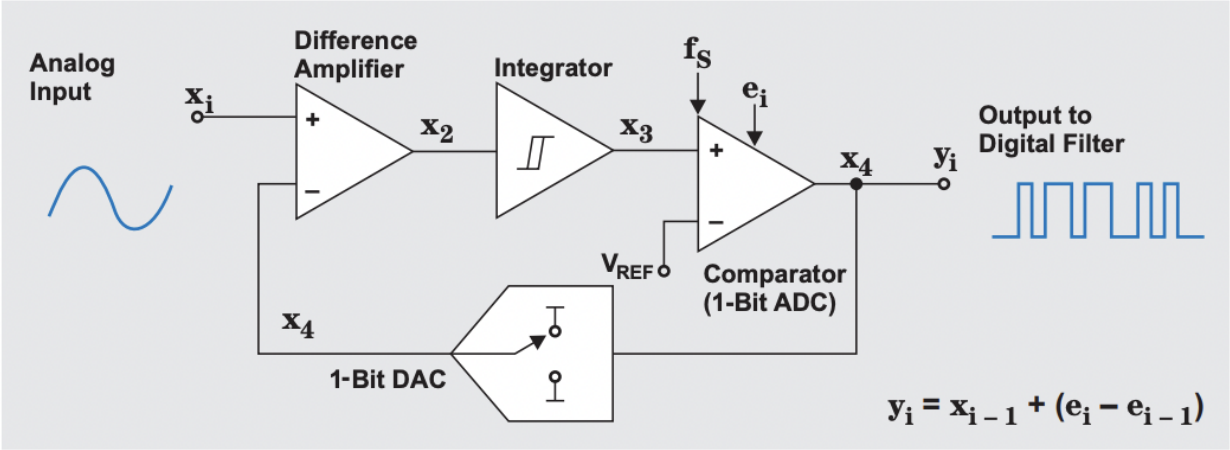

Figure 3: First-Order Sigma-Delta ADC Block Diagram

The first component in the sigma-delta system is the difference amplifier. A difference amplifier is an amplifier which produces an output that is the difference between its two inputs. Here, the difference amplifier is used to subtract the analog output of the converter from the analog input signal and produce a noise-reduced voltage that can be provided to the integrator [6]. The analog input signal is the non-inverting (+) input of the difference amplifier and the output of the DAC block is the inverting (-) input of the difference amplifier.

Connected to the output of the difference amplifier is the integrator component. An integrator amplifier performs the mathematical operation of integration on the output of the

difference amplifier. The output of the integrator is a voltage proportional to the magnitude of and duration that the input has deviated from 0V.

After integrating the signal, the next component in the system flow is the comparator. A comparator is used to take the analog output of the integrator to the digital domain. In the sigma-delta converter, this performs the actual operation of translating the analog voltage to digital values. A comparator amplifier is effectively a differential amplifier operated in saturation. It compares the input voltage (output of the integrator) against a reference voltage and outputs only either Vdd or Vss (0V) depending on whether the input or the reference is higher. A comparison of the input signal to the reference voltage is necessary for determining the value of the signal being read through the converter system and converting the signal to the digital domain of 1 and 0 (typically 5V and 0V respectively). Once the signal has been converted by the comparator, it will be output as the digital result of the analog-to-digital converter.

At the output of the comparator is a feedback loop which involves the use of a DAC (Digital-to-Analog Converter). This is implemented as a simple 1-bit DAC which has the effect of converting the single polarity (0V/5V) logic signal (which is the output of the comparator) to the V-/V+ signal necessary for providing negative feedback to the difference amplifier. This allows for much of the fluctuation caused by noise and other disturbances to be removed from the system in subsequent iterations of conversion.

Once the top-level functionality of the sigma-delta converter has been understood, it will be important to convert these design units in the block diagram into a more practical design. A block diagram consisting of the same components as previously described (differential amplifier, integrator, comparator (quantizer), and DAC) can be seen below with a lower-level typical implementation of each of the components [7, Figure 4]. The difference amplifier is not labeled

in this diagram, however it is represented by the summer in the top diagram and will be implemented as a differential amplifier in the bottom diagram. This low-level system will be used as a guideline for designing the sigma-delta converter.

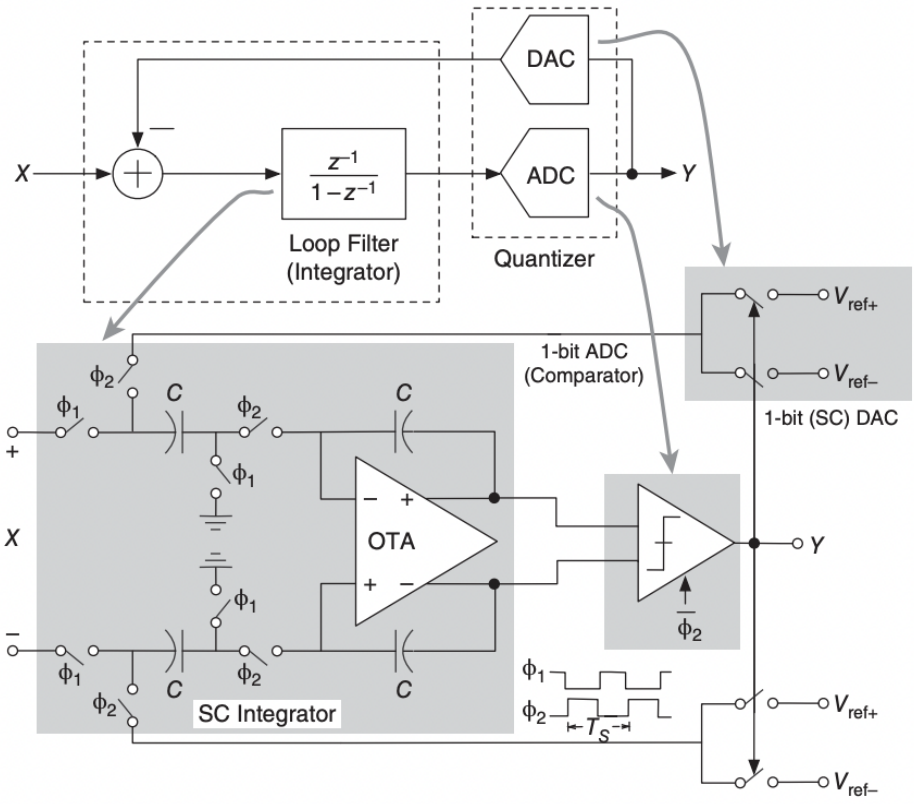

Figure 4: Fully Differential Circuit Implementation of a First-Order Sigma-Delta ADC

Now that functionality and primary components of the sigma-delta ADC have been introduced, the following sections will go into detail about each of the components and how they were designed to create the sigma-delta converter of this thesis.

Fully Differential Amplifier

Fully differential amplifiers are an important building block in the design of electronics. They are amplifiers that amplify the difference between two input signals (voltage or current) while rejecting common-mode signals that are present on both inputs. Fully differential amplifiers are commonly used in applications where common-mode noise is a concern, such as in data acquisition, instrumentation, and communication systems [7]. Fully differential amplifiers offer several advantages over single-ended amplifiers, such as higher common-mode rejection, lower noise, and higher linearity. Fully differential amplifiers can be implemented using different circuit topologies, such as the folded-cascode, telescopic, and current-feedback amplifiers, each with its own advantages and disadvantages.

Designing a fully differential amplifier involves several steps and considerations. The first step is to select the appropriate amplifier topology based on the desired specifications and performance requirements [8]. For this project, a folded-cascode topology was chosen as it represents a moderate trade-off of power, speed, and complexity. The next step is to determine the desired gain and bandwidth of the amplifier, which depends on the application. The amplifier's stability and phase margin must also be analyzed to ensure that the amplifier does not oscillate or become unstable. The next step is to select the biasing scheme and the power supply voltage, which affect the amplifier's linearity, noise, and power consumption. The choice of the feedback network and the compensation scheme is also critical for ensuring stable operation and good transient response.

Although a layout was not created for this design, the amplifier's layout must also be carefully designed to minimize parasitic capacitance, inductance, and noise. The amplifier must

be simulated and verified using appropriate models and simulation tools to ensure that it meets the desired specifications and performance requirements.

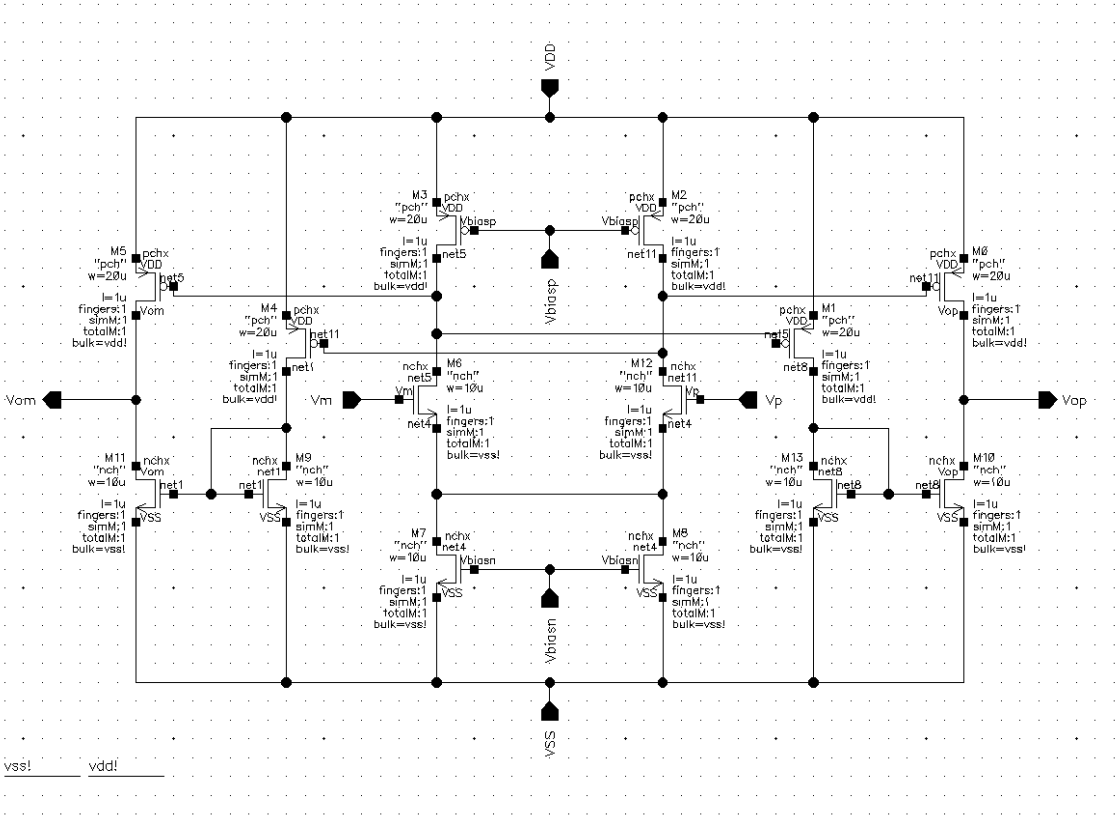

Figure 5: Schematic for the Fully Differential Amplifier

Above, the schematic for the fully differential amplifier designed for this project can be seen. A feature length of 1um was chosen in order to provide a more easily attainable high-gain and reduce design complexity. For the fully differential amplifier designed, a gain of 55.27 dB was achieved along with a unity frequency of 128.9 MHz and a phase margin of 38 degrees. This proved to be enough gain to amplify signals that are practically very small. Along with a decent frequency response and good stability, this amplifier could be considered a satisfactory input device for the ADC system. The fully differential amplifier was tested using a 50 mV sine wave. The transient response can be seen below with the input being amplified to the power rails.

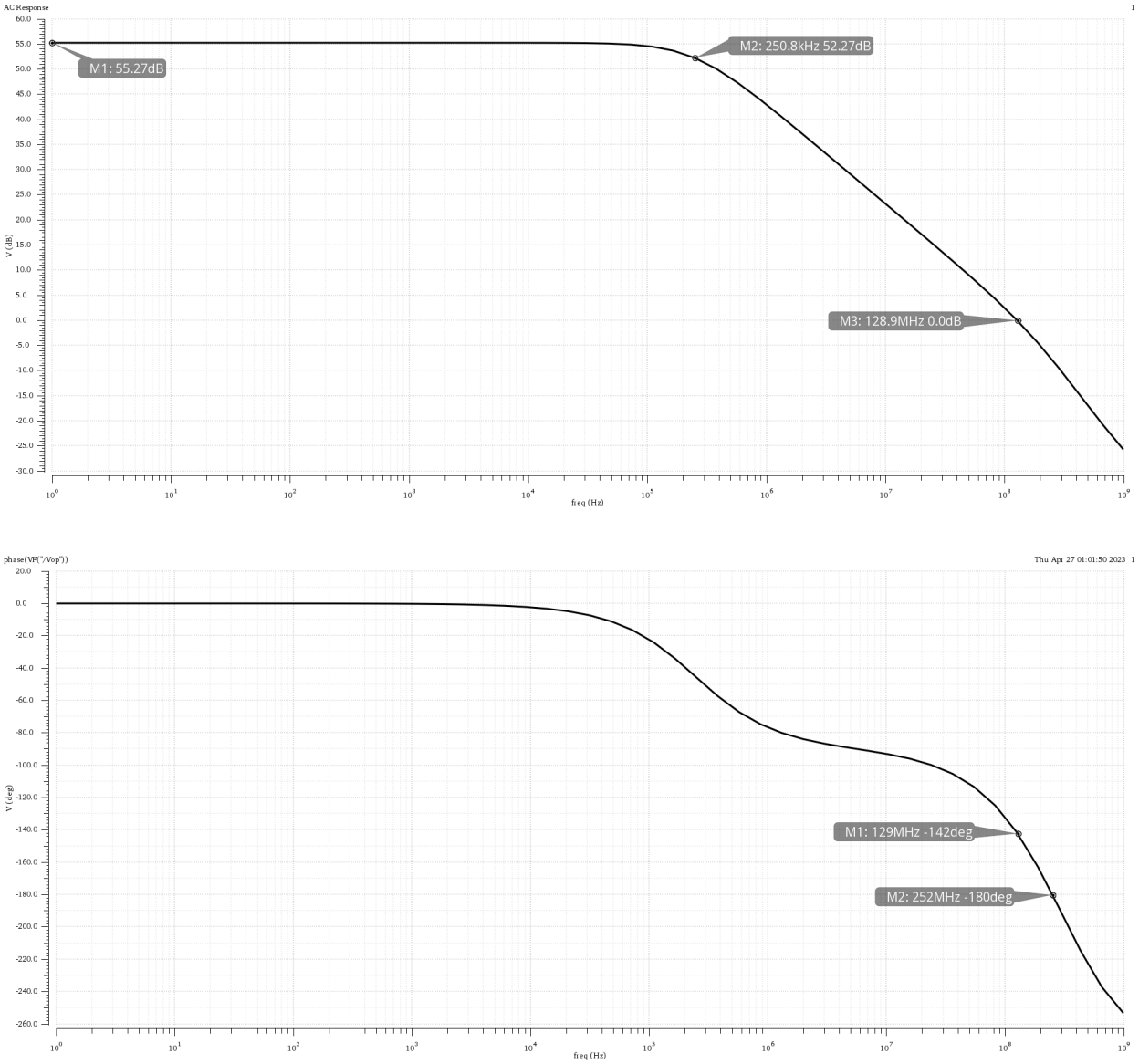

Figure 6: Bode Plot for the Fully Differential Amplifier

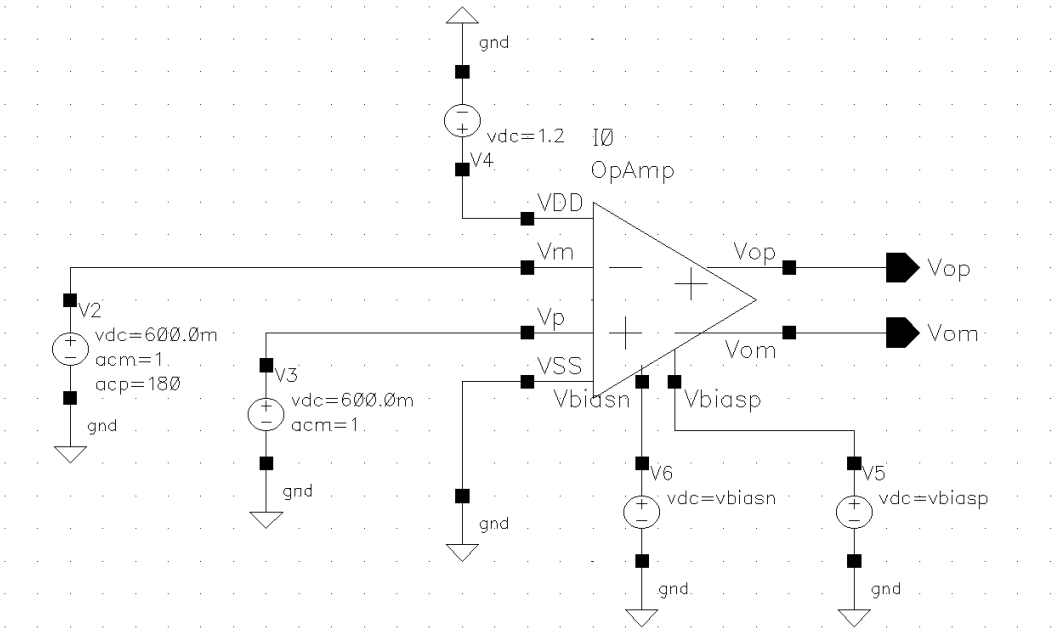

Figure 7: Schematic for Testing the Amplifier

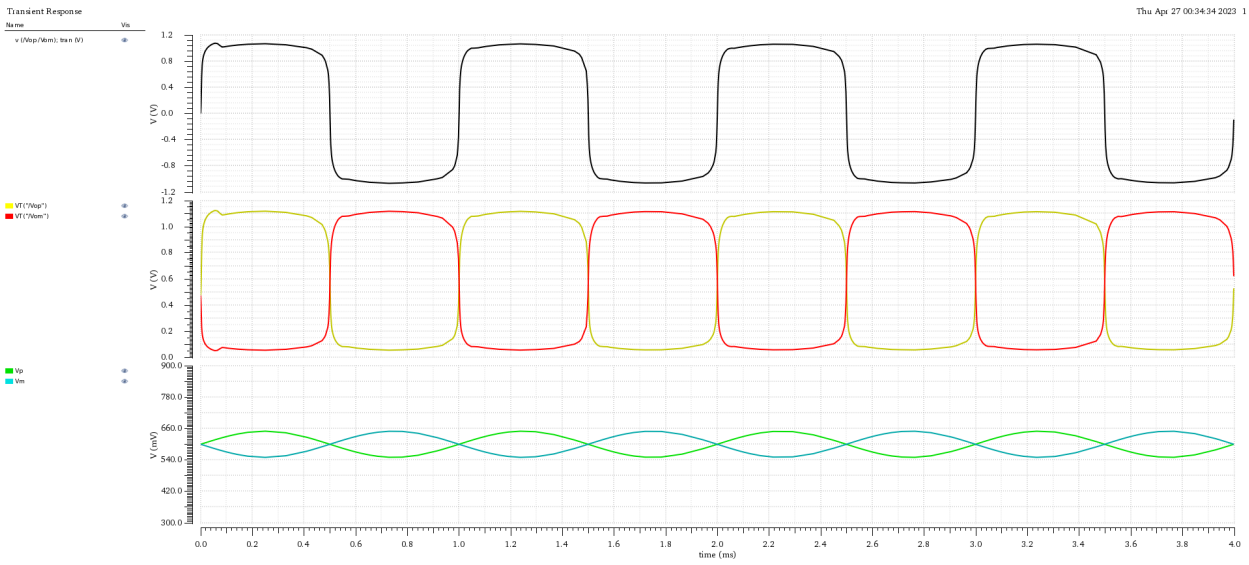

Figure 8: Transient Response for the Fully Differential Amplifier

Integrator

Integrator amplifiers are electronic circuits that perform the mathematical integration of an input signal with respect to time [9]. They are commonly used in signal processing applications. The most basic integrator amplifier consists of an operational amplifier and a feedback capacitor, which stores charge and provides the integration function. Integrator amplifiers have a transfer function that rolls off at low frequencies, which makes them useful for filtering out low-frequency noise and DC offset. However, integrator amplifiers are prone to stability problems due to the accumulation of phase shift at high frequencies. To mitigate this issue, integrator amplifiers often employ a compensation network, such as a resistor-capacitor network or an active compensation circuit.

Designing an integrator amplifier involves several steps and considerations. The first step is to select the appropriate operational amplifier based on the desired specifications and performance requirements. Since an operational amplifier was already created in the previous step to handle the inputs of the system (the fully differential amplifier), this op-amp can be converted to an integrator for the fulfillment of this component. The next step in building the integrator is to determine the value of the feedback capacitor and input resistor, which depends on the application and the required frequency response. The capacitor value must be large enough to provide sufficient integration, but not so large as to cause stability problems or excessive noise. The product of the capacitor and resistor values is known as the integrator time constant [10]. The choice of the compensation network and the location of the compensation capacitor is critical for ensuring stable operation and good frequency response.

As mentioned, the fully differential amplifier designed in the previous step was adapted to create an integrator circuit. In order to create the integrator circuit, a switched capacitor

network was created to sample the input and effectively act as a controlled resistor. A non-overlapping set of clocks was used to control the “filling” of the capacitors (Figure 10).

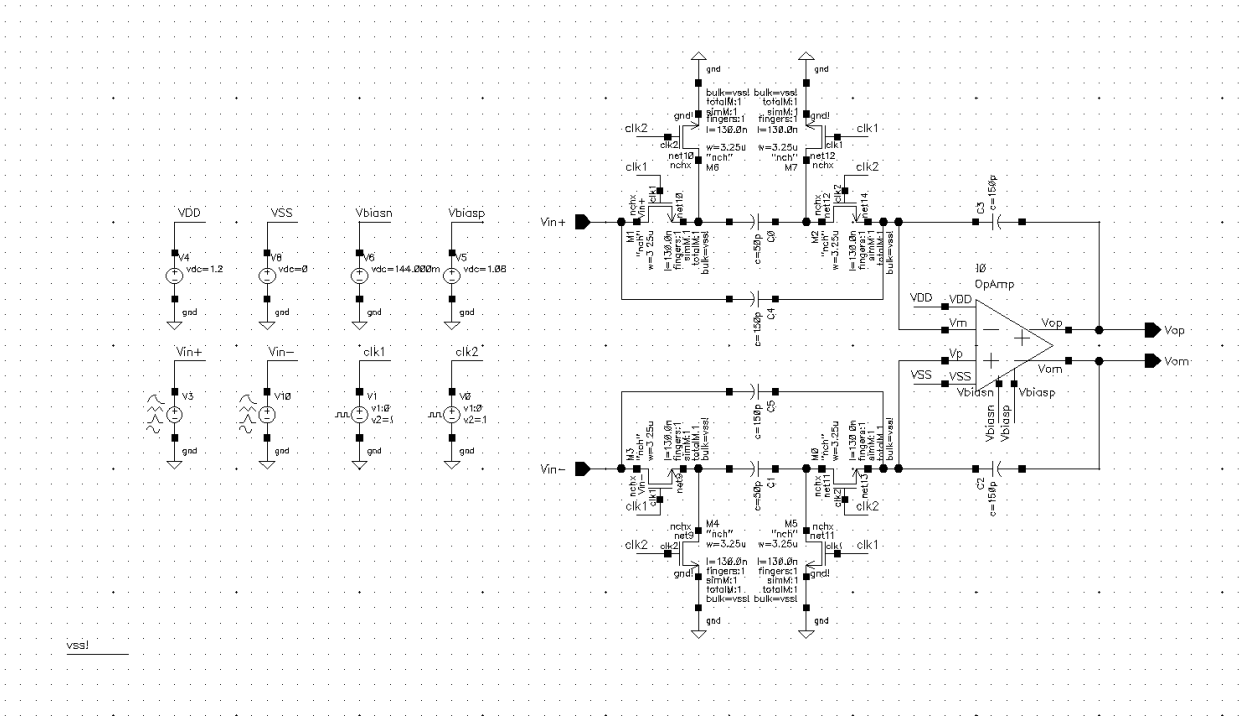

Figure 9: Schematic for the Integrator Circuit

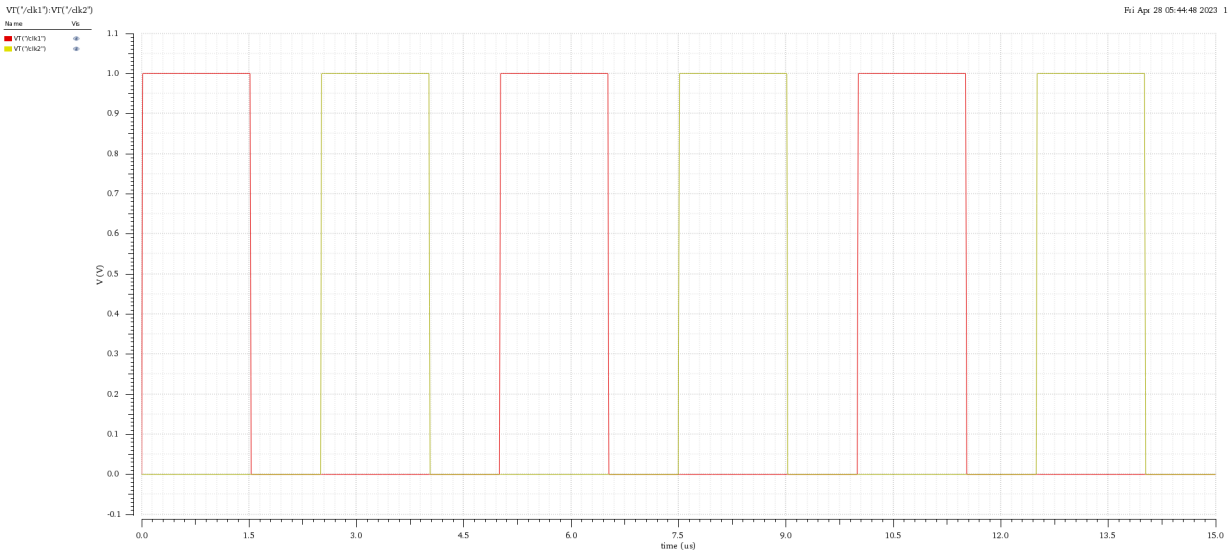

Figure 10: Non-overlapping Clocks with Period of 5 us (200 kHz freq.)

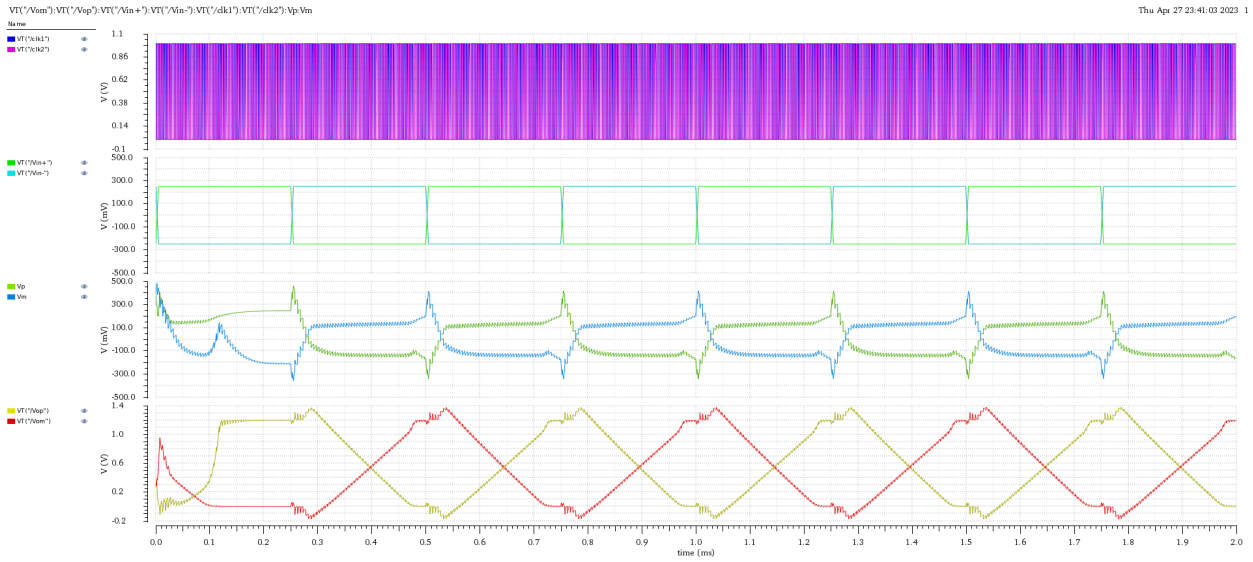

Figure 11: Transient Response for the Integrator Circuit (Square Wave)

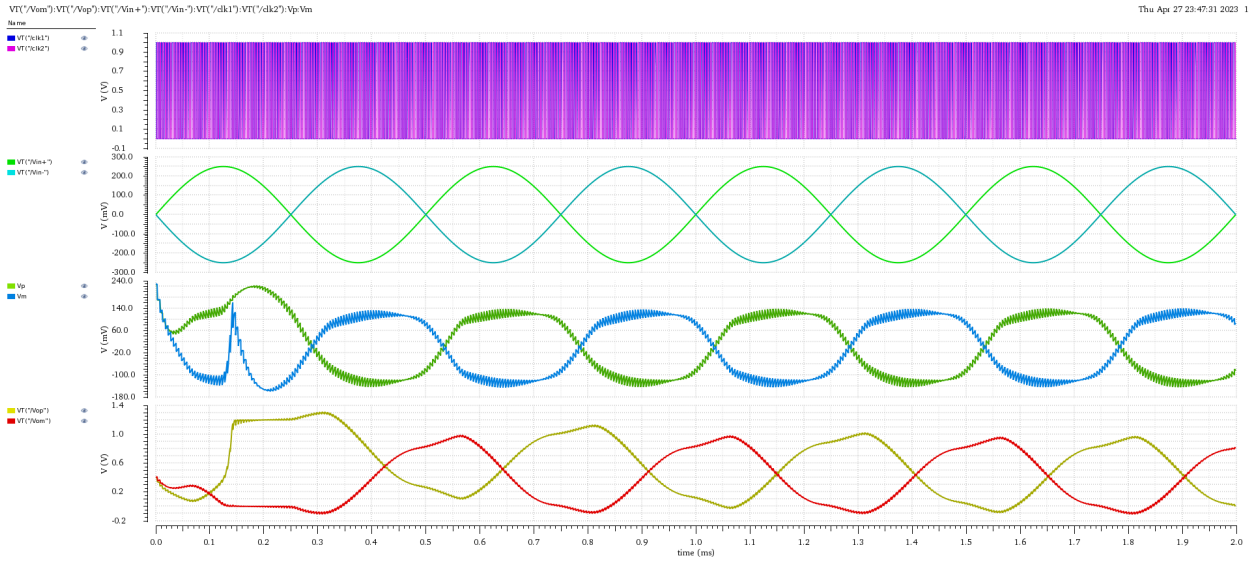

Figure 12: Transient Response for the Integrator Circuit (Sine Wave)

The integrator circuit was tested with both a square wave and a sine wave in order to test its integration response with different inputs. The integral of a square wave is a triangular wave and the integral of a sine wave is the corresponding negative cosine wave. As seen from the results, the correct integration for both of these inputs was achieved with minimal delay.

Comparator

The next stage in the sigma-delta converter is the comparator. Comparators are circuits that compare two input voltages and provide a digital output indicating which voltage is higher [1]. The basic latched comparator consists of a differential amplifier, a latch, and a reset switch. The differential amplifier amplifies the difference between the two input voltages, and the output of the differential amplifier is fed into the latch. The latch stores the output of the differential amplifier and provides the digital output. The reset switch is used to reset the latch to a known state, which ensures that the comparator operates correctly.

Latched comparators are widely used in analog-to-digital converters, oscillators, and other applications where precise voltage comparison is required. The speed of the comparator is typically the limiting factor for conversion speed of most ADC designs [7]. Designing a latched comparator involves several key steps and considerations. The first step is to select the appropriate transistor sizing for the differential amplifier and latch to ensure the required gain, speed, and noise performance. It is worth noting that the choice of transistor sizing also affects the power consumption and layout area of the circuit. The next step is to select the threshold voltages for the latch and reset switch to ensure proper operation and minimize the risk of metastability. The comparator must also be simulated using appropriate models and simulation tools to ensure that it meets the desired specifications and performance requirements.

For the purposes of this project, a simple discrete-time comparator was created. This component compares the input (output of the integrator) to a reference voltage in order to generate the digital bitstream representing the value of the analog signal being converted.

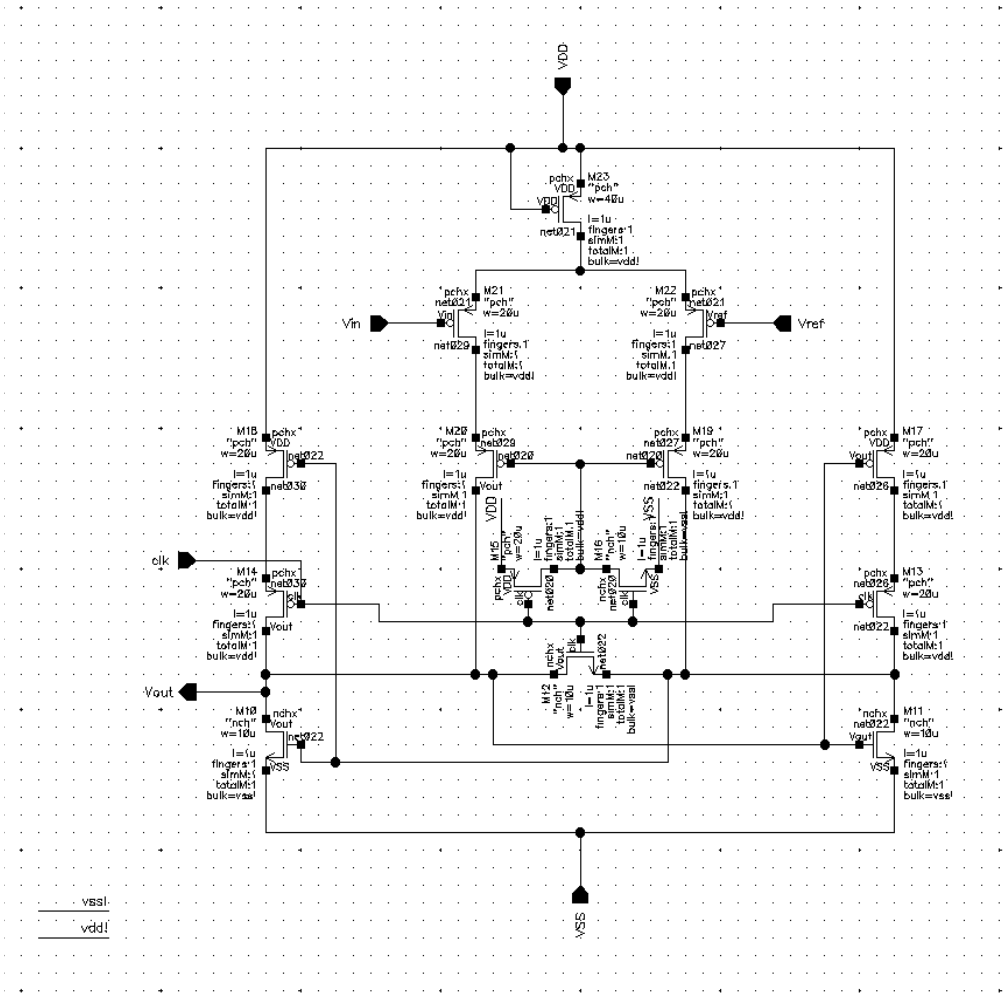

Figure 13: Schematic for the Comparator

The first test performed on the comparator was a triangle wave input and a reference voltage of 0 V (ground). For this test, the correct output was clearly observed with the comparator generating a 1 when the triangle wave was above 0V and a 0 when the triangle wave was below 0V. For the next test, the integrator designed in the previous step was connected to the input of the comparator and the inverting output was used as the reference. This makes the design fully differential. Once again, the correct output was observed with the stream of 1s and 0s generated by the comparator tracking the relative value of the integration from the integrator circuit.

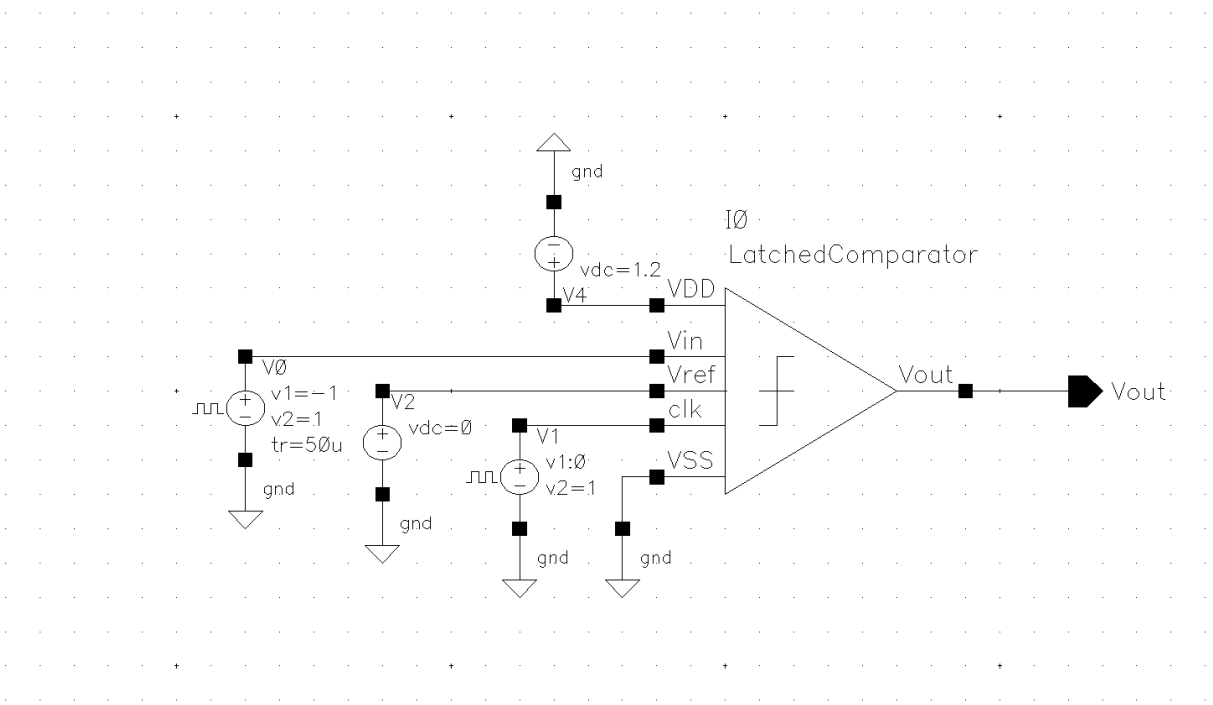

Figure 14: Schematic for Testing the Comparator

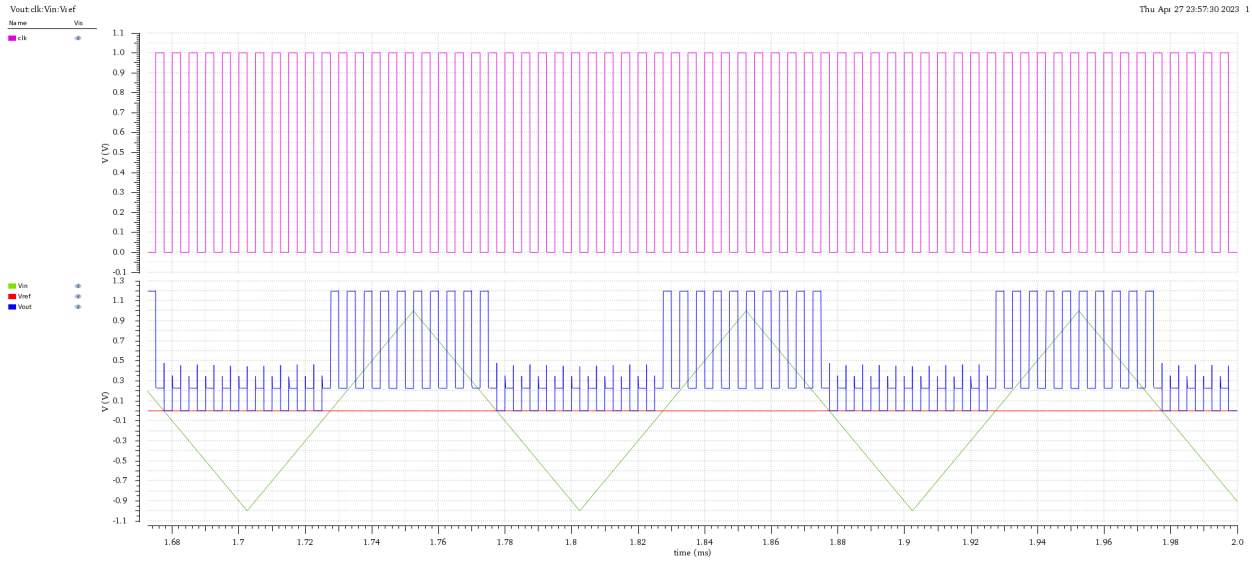

Figure 15: Transient Response for the Comparator (Triangle Wave)

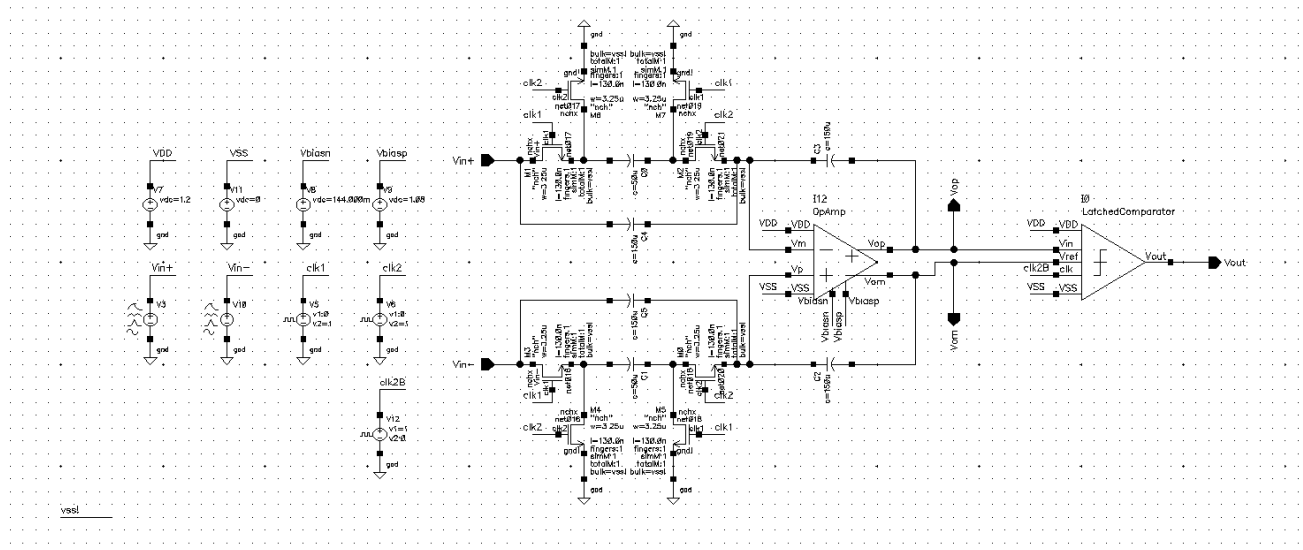

Figure 16: Adding the Integrator to the Input of the Comparator

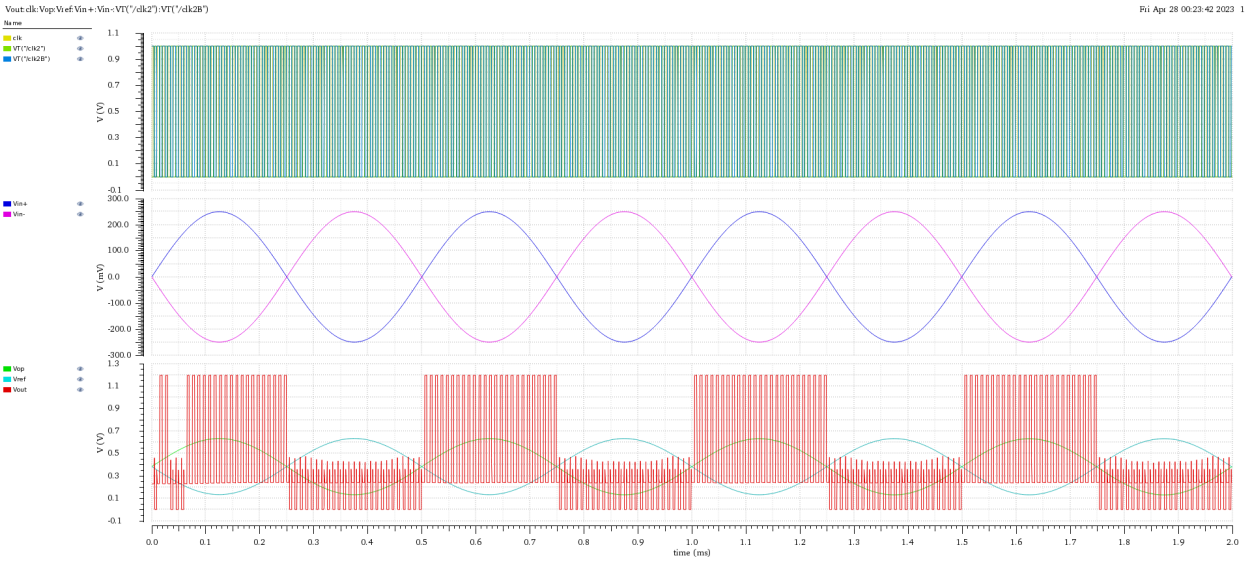

Figure 17: Transient Response for the Comparator (Integrator Connected)

DAC Feedback

A 1-bit digital-to-analog converter (DAC) is an essential component in the feedback loop of a sigma-delta converter. The sigma-delta modulator generates a high-frequency bit stream, which represents the analog input signal, and the low-resolution DAC converts the bit stream back into an analog signal. This converted analog signal is compared to the input signal using the differential amplifier. The feedback loop ensures that the output of the converter accurately represents the input signal with high resolution and low distortion. The choice of the DAC dynamic range in part determines the performance of the sigma-delta converter, and the DAC must have good linearity, low noise, and high settling time to achieve high-performance and high-speed operation.

Designing a DAC for a sigma-delta converter involves several considerations. The first step is to determine the required resolution, which determines the number of quantization levels and the accuracy of the DAC output. Typically, a 1-bit DAC is used. Next, the DAC topology must be selected based on the desired performance specifications, such as settling time, linearity, and noise. A common approach is to use a simple resistor-ladder or capacitive-digital DAC, which can achieve good linearity and settling time performance while being relatively simple to implement. The selection of the reference voltage and the biasing scheme also affects the DAC performance, particularly the linearity and dynamic range. The DAC must be carefully simulated to ensure that it meets the desired specifications and performance requirements, including frequency response, settling time, linearity, and noise. Finally, the DAC must be integrated into the sigma-delta converter's feedback loop and tested within the context of the full system [11].

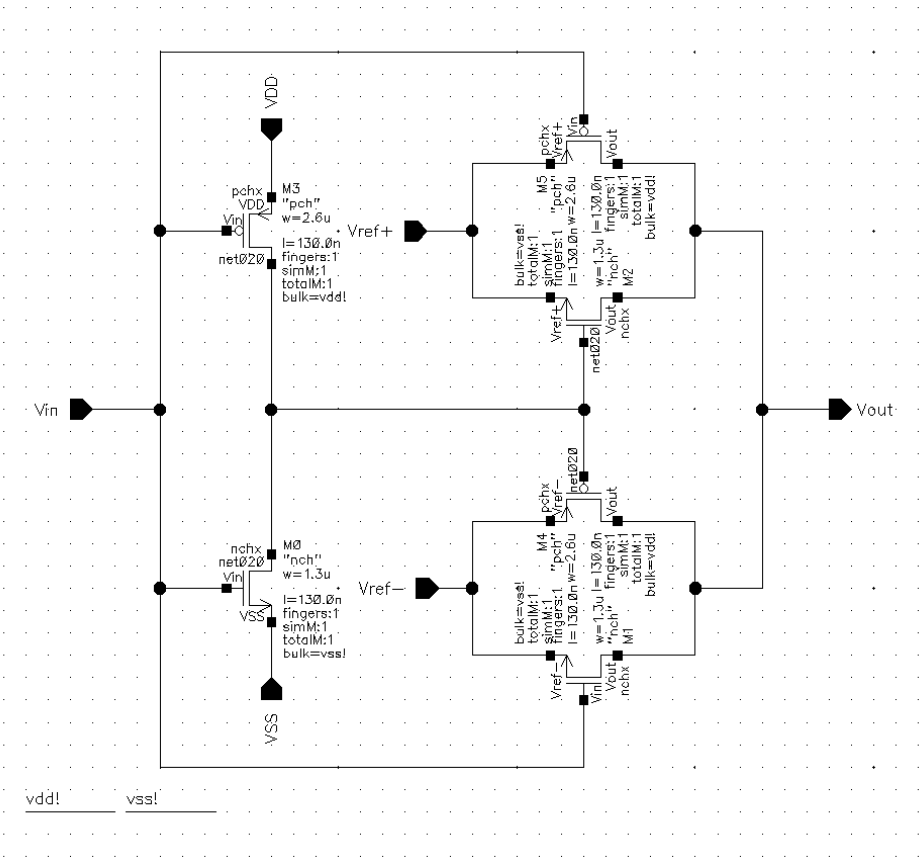

Figure 18: Schematic for the 1-Bit DAC

Digital Decimation Filter

A decimator and a low-pass filter are related concepts within digital signal processing, but they serve different purposes. A low-pass filter is a signal processing technique that attenuates the high-frequency components of a signal while allowing the low-frequency components to pass through. The output of a low-pass filter is a filtered version of the input signal that has a reduced bandwidth. Low-pass filters are commonly used to remove noise from signals or to prepare signals for further processing [12].

A decimator, on the other hand, is a signal processing system that reduces the sampling rate of a signal by removing samples from the input signal. The output of a decimator is a

downsampled version of the input signal that has a lower data rate. Decimation is often used to reduce the computational load of subsequent processing stages or to reduce the storage requirements of a signal [12].

While a decimator and a low-pass filter both involve reducing the bandwidth of a signal, they differ in their approach. A low-pass filter reduces the bandwidth of the signal by attenuating high-frequency components, while a decimator reduces the bandwidth of the signal by reducing the sampling rate. In practice, a decimator may incorporate a low-pass filter to remove the high-frequency components of the signal before downsampling to avoid aliasing effects. Therefore, a decimator and a low-pass filter can be used together in a signal processing pipeline.

For the sigma-delta converter, a decimation filter is used in order to convert the output of the modulator into a reconstructed digital signal that can then be used by a computer [7]. The output of the sigma-delta modulator is a modulation that represents the relative value of the converted signal. This modulation has to be converted into a valued digital signal. This is the job of the filter. Additionally, the filter is designed so that the high-frequency components of the converted signal are removed and the signal can be more efficiently stored and processed by the computer.

Results

After designing and testing each of the components individually, the full sigma-delta modulator was tested using various input signals.. The results for each input test of the sigma-delta modulator can be seen below. A variety of different signals were applied to the modulator in order to determine its effectiveness in converting signals of different magnitude, frequency, and shape.

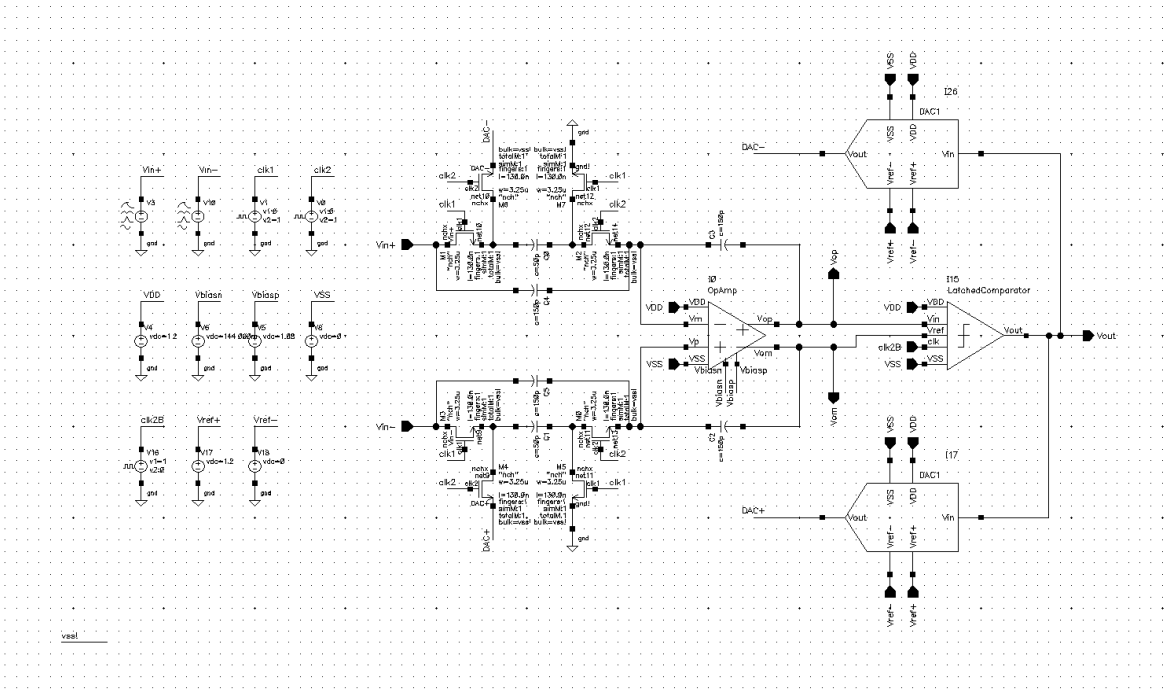

Figure 19: Schematic for the Sigma-Delta Modulator

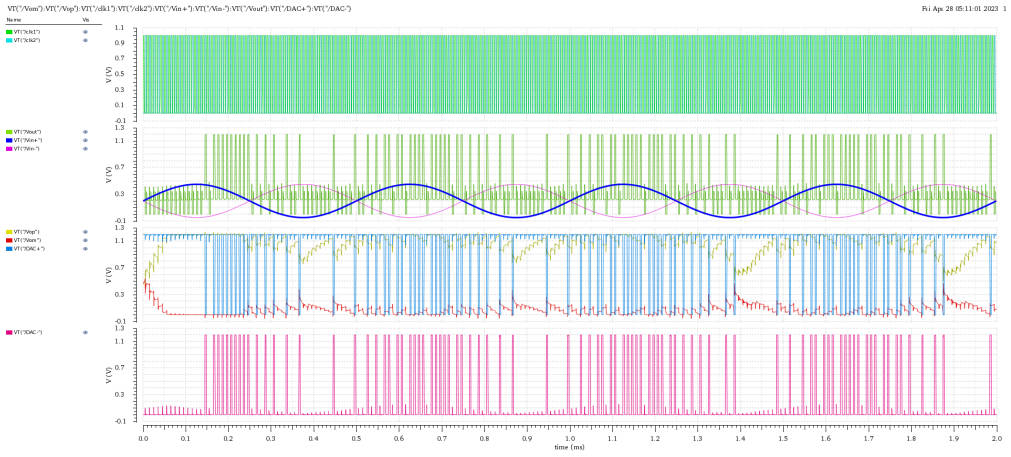

Figure 20: Sine Wave Input (2 kHz, 250 mV)

Note that for each test, the first window shows the non-overlapping clocks used for the sampling and comparator. The second window shows the modulated output in green, the input signal in blue, and the inverted input in pink. The third window shows the positive DAC feedback in blue and the value of the integration and its inverse in yellow and red respectively. Finally, the fourth window shows the negative DAC feedback in pink.

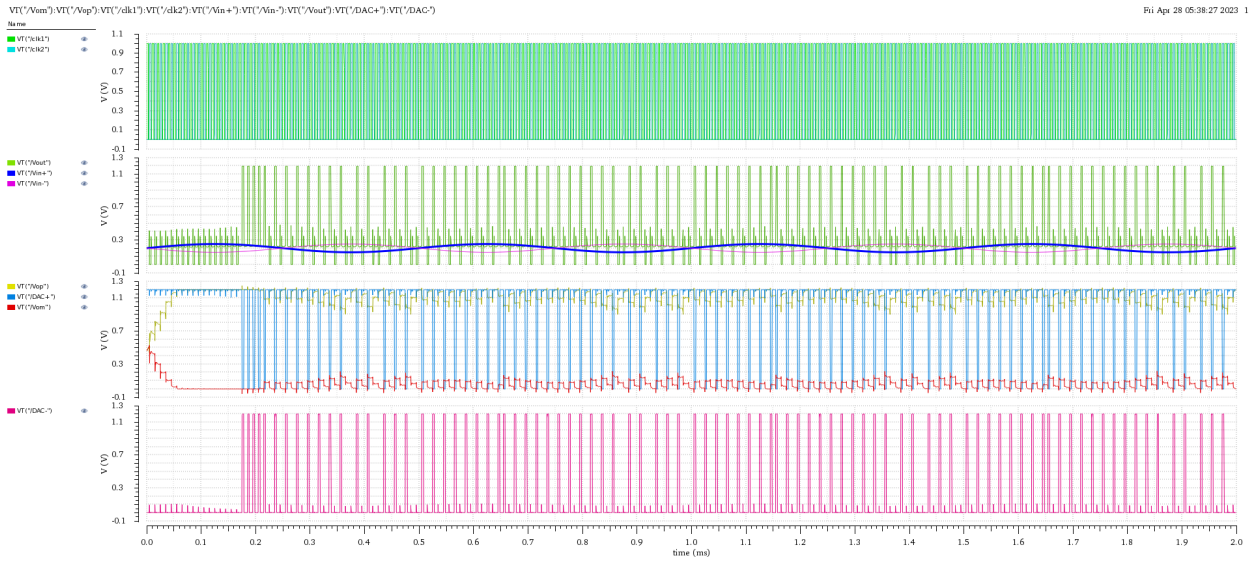

Figure 21: Sine Wave Input (2 kHz, 50 mV)

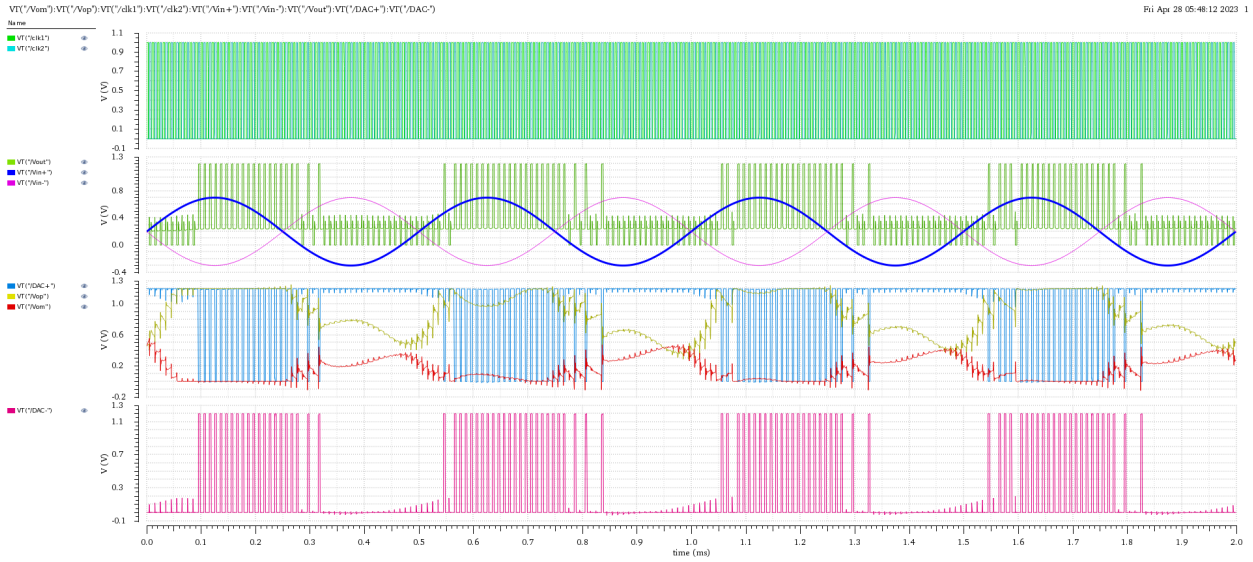

Figure 22: Sine Wave Input (2 kHz, 500 mV)

As seen from the first few sine wave input tests, the converter generated an output whose modulation is determined by the magnitude of the input. A higher magnitude sine wave input resulted in a denser modulation representing a value that is closer to the full-scale value (1.2 V), while a lower magnitude resulted in a more sparse modulation.

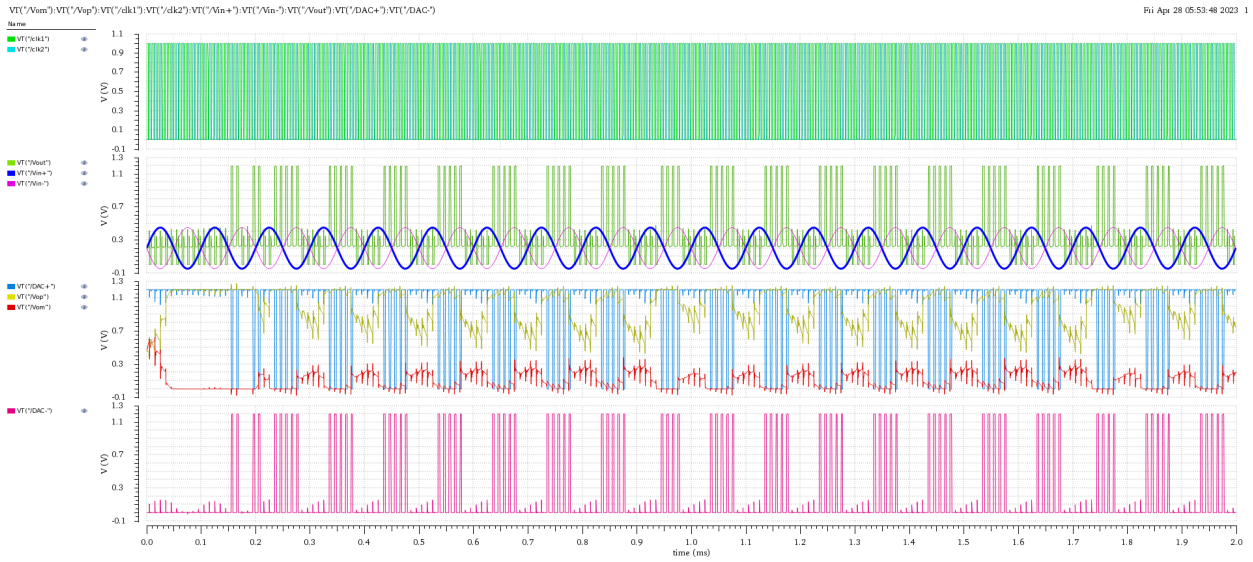

Figure 23: Sine Wave Input (10 kHz, 250 mV)

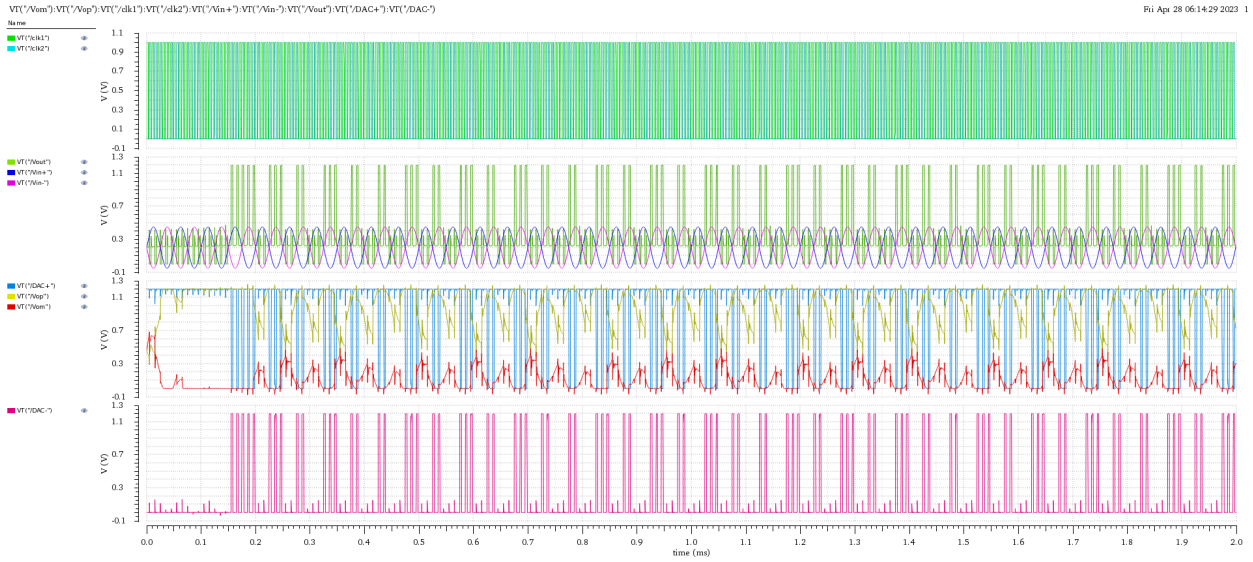

Figure 24: Sine Wave Input (20 kHz, 250 mV)

It can be seen from these plots the impact increasing the frequency of the input signal has on the output. The sigma-delta converter has been demonstrated to handle input frequencies of up to 20 kHz with very little quantization error. Due to the speed limitations of the components, pushing the input frequency higher begins to degrade the accuracy of the converter, but the performance demonstrated is good overall.

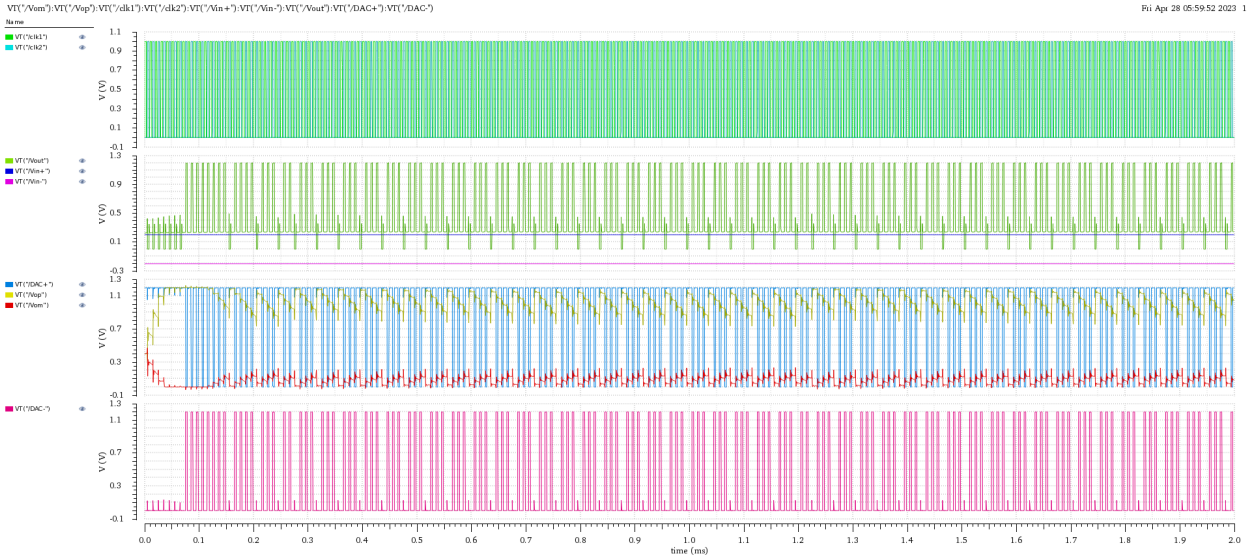

Figure 25: Constant DC Input (200 mV)

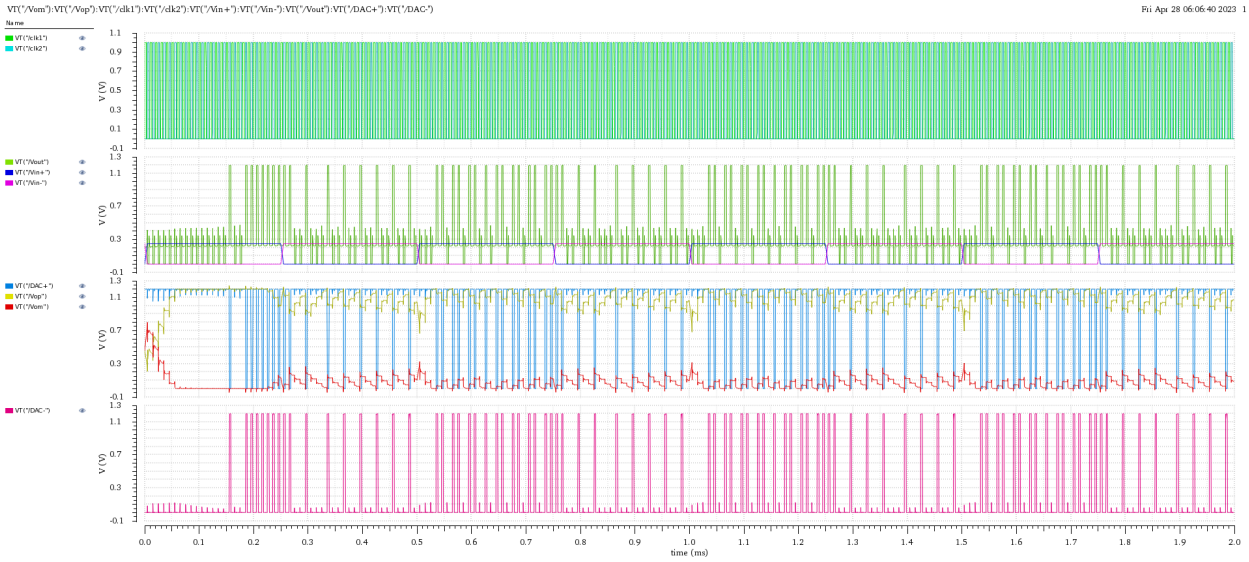

Figure 26: Square Wave Input (250 mV, T = 0.5ms)

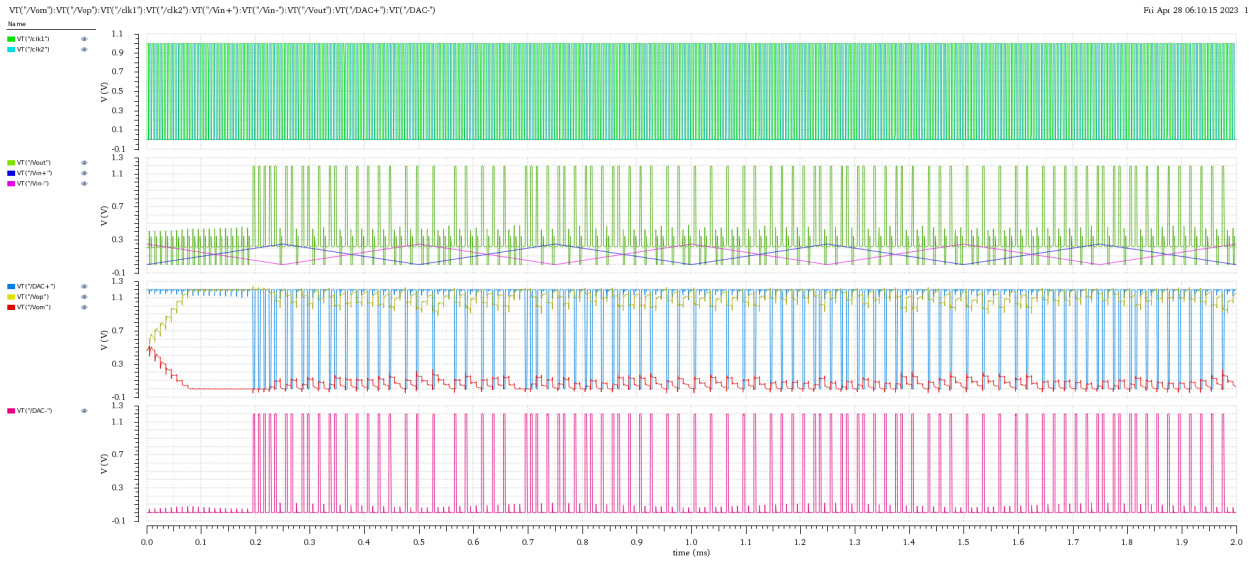

Figure 27: Triangle Wave Input (250 mV, T = 0.5 ms)

After testing the impact of input magnitude and frequency, the final tests sought to demonstrate the performance of the converter in handling conversions of non-sinusoidal signals. The first test provided a constant DC voltage to the input of the converter. The output of this test was a signal with a constant modulation, which is to be expected as the input value does not change. For the second test, the modulator was provided with a square wave input. This type of input is similar to the DC voltage test except that half of the signal is at lower voltage than the rest. This resulted in a modulated output that was dense at the high values and less dense at the low values- similar to the sine wave input. For the last test, a triangle wave input was provided to the system. In this case, a varying modulated output was created with peaks in the input resulting in a higher density of pulses.

Overall, the sigma-delta converter was demonstrated to perform well under a variety of tests. In each of these tests, the modulated output changed depending both on how fast the input changed as well as the relative values of the input. This behavior is what was expected from the design, and is desired for tracking the value of the analog input signal necessary for conversion.

Conclusion

This paper has first detailed the fundamentals in understanding analog to digital conversion followed by a detailed description of the design and testing process of a simulated sigma-delta ADC in the TSMC 65nm CMOS process. The project involved the implementation of various components including a fully differential amplifier, integrator, latched comparator, and 1-bit DAC. The design involved the creation of a 1st-order single-bit sigma-delta modulator, which provided an adequate trade-off between circuit complexity and performance while most importantly demonstrating the fundamental behavior of the sigma-delta converter. The simulation results have demonstrated the ability of the sigma-delta ADC to achieve a relatively low-noise conversion, while maintaining moderate linearity and speed.

Although the decimation filter was not created for the converter here, the design and simulation of the modulator itself was the most important goal and primary focus. In designing the sigma-delta modulator of this project, the concepts of analog-to-digital conversion were utilized in many ways to achieve the desired functionality. Many important fundamentals in ADC design were learned throughout this project including switched-capacitor filters, latched comparators, DACs, and modulation. Overall, the project has shown the significance of design considerations in the implementation of a variety of important electronics building blocks, and can be used as a foundation for further developments in an understanding of mixed-signal integrated circuit design.

Future Work

One of the most obvious next steps of the project would be to design the decimation filter necessary to convert the modulated signal into the true digital signal representation. The addition of this component would allow for a better analysis of how well the ADC converted the input.

In addition to adding a decimation filter, there was some discrepancy between the theoretical results of the design and the results produced that would ideally need to be corrected. Much of this error is likely due to noise created by a variety of factors including clock feedthrough, charge injection, DC offset, and the imperfect integration of the input signal.

After improving the signal-to-noise ratio and performance of the simulated design, the next step of the project would be to create a layout of the design. Creating the layout for an integrated circuit involves converting the individual transistors to their material implementation and routing interconnects to connect them together. Design rules are utilized to ensure that the layout meets desired specifications. Once the layout is complete, it is verified through simulation to ensure it operates in the same way as the system's schematic representation.

After creating the layout, this layout would in theory then be used to fabricate a physical chip that could then be tested. It would be important to ensure that the real chip behaves as simulated, so many more considerations would be given to creating the layout and schematics in an analog-friendly manner if the chip were to be considered for fabrication. Such considerations would include the design being simulated for additional requirements such as methods to work given process, voltage, and temperature variations as well as shielding between the analog and digital components. Once the initial design is updated to meet these additional requirements, the chip could then be fabricated and tested.

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