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# An Accurate and Efficient Electro-thermal Compact Model of SiC Power MOSFET including Third Quadrant Behavior

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# An Accurate and Efficient Electro-thermal Compact Model of SiC Power MOSFET including Third Quadrant Behavior

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by

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## Abstract

Due to narrower bandgap and lower critical electric field, silicon (Si) power devices have reached their limit in terms of the maximum blocking voltage capability. Exploiting this limitation, wide bandgap devices, namely silicon carbide (SiC) and gallium nitride (GaN) devices, are increasingly encroaching on the lucrative power electronics market. Unlike GaN, SiC devices can exploit most of the established fabrication techniques of Si power devices. Having substrate of the same material, vertical device structures with higher breakdown capabilities are feasible in SiC, unlike their GaN counterpart. Also, the excellent thermal conductivity of SiC, compared to GaN and Si, let SiC devices operate at higher temperatures (~ 300°C). Hence, a more compact and cost-effective power electronic system can be designed with SiC devices without cumbersome cooling requirements. Specifically, SiC power MOSFETs have started to dominate applications such as three-phase inverters, PWM rectifiers, DC-DC converters in the 1.2 kV – 3.3 kV voltage range. However, SiC power MOSFET's full potential can only be harnessed with accurate and efficient simulation tools that enable optimally designed systems without multiple cost and time-consuming prototyping. Significant work has already been done on the compact modeling of SiC power MOSFET. However, those works focus on the first quadrant behavior. The third quadrant behavior, especially the gate bias dependent body diode characteristics, needs proper modeling for synchronous rectification, freewheeling diode action, dead time optimization, and EMI analysis. Further, the existing physics-based compact models lack efficient and continuous temperature scaling, which is essential for efficient and accurate simulation of power electronic systems with significant self-heating.

This dissertation reports on an accurate and efficient electro-thermal model of the SiC power MOSFET that will include the third quadrant behavior with the body diode. In modeling body

diode characteristics, the gate bias dependency and reverse recovery are included for the first time. For accurate switching characteristics, gate dependency of the input capacitance has been included. Accurate Miller capacitance modeling both at very low bias and at very high bias is ensured without adding too many model parameters. Avalanche-induced breakdown characteristics are included to make the model capable of predicting Safe Operating Area (SOA). Double pulse tests (DPT) at various temperatures were performed to validate the model's switching characteristics accuracy. A buck converter was implemented with the same half-bridge configuration as the DPTs to validate the model's performance with self-heating effects. Various other power electronics topologies are simulated to validate the accuracy and efficiency of the developed model. Detailed comparison with a previous physics-based model and a vendor-provided empirical model highlights the importance of the developed model in terms of accuracy and efficiency. Lastly, an easy-to-follow parameter extraction procedure has been described to enable broader use of the model among power electronics designers.

**Acknowledgments**

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# Chapter 1. INTRODUCTION

## 1.1. Motivation

Power electronics applications such as three-phase inverters, PWM rectifiers, DC-DC converters, traction inverters, etc., require an anti-parallel diode for freewheeling current conduction. In the case of Si IGBTs, the only viable option is to use an external anti-parallel diode as novel structures like RC-IGBTs [1] are still in the research stage. SiC Schottky Barrier Diodes (SBDs) are widely used as the anti-parallel diode for high voltage Si IGBTs. On the contrary, power MOSFETs have a built-in anti-parallel diode called the body diode. The body diode is formed by the series formation of *p* body, *n*- drift region, and *n*+ drain contact. This structure is a *p*-*i*-*n* configuration and requires the removal of the minority carriers before blocking the reverse voltage. This removal of minority carriers leads to a phenomenon known as reverse recovery, which occurs when the diode is initially forward-biased and charges build up in the drift region. When the device is switched off, these charges must be removed. Hence, the diode suffers from the reverse recovery current ($I_{rr}$) during the turn-off. Having a thinner and heavier doped drift region, the SiC power MOSFET suffers from significantly less $I_{rr}$ than its Si counterpart. However, it is not negligible and can reach up to 30% of the load current during switching [2].

An alternative to the body diode is to use an external SBD with the power MOSFET. Though SBDs do not suffer from reverse recovery current and the forward voltage drop ($V_f$) is less than half of the body diode's drop, the use of external SBD causes other problems. First, it increases the output capacitance ($C_{oss}$) by adding an extra junction capacitance. Second, SBD occupies more area in a compact module design. Third, the external connections such as bond wires add parasitic inductance, causing high overshoot and oscillation during switching. Therefore, using the body diode instead of the SBD increases the current rating, reduces cost, and makes the design compact.

Though early generation SiC power MOSFETs' body diode suffered from reliability issues [3], those issues have largely been managed in the newer generations [4]. Increasingly, more designers are opting for using the body diode in their designed systems.

To truly utilize the SiC MOSFET's features in power electronics circuit design, accurate simulation models of the devices are required. Unlike low-voltage analog integrated circuits (ICs), power electronic device modeling did not emphasize the entire circuit-level simulation due to the available models' poor convergence properties. Circuit-level designers still rely on analytical modeling for specific effects of the circuits. Previously, for a frequency level below 40 kHz, this approach was acceptable. However, with the introduction of wide bandgap devices with lower parasitic capacitances and lower reverse recovery, the frequency limit of power electronics circuits is approaching the MHz range [5]. In such cases, electromagnetic interference (EMI) has become a significant issue. It will be beneficial to simulate and optimize the entire circuit with accurate models of the devices and passives considering EMI, reliability, stress, etc., along with the power losses. So, reliable device models with attractive convergence properties will undoubtedly benefit power electronics circuit designers.

In the world of device modeling, physics-based compact models are a compromise between two extremes: numerical models and empirical models. Instead of overloading information about charge concentration, potential distribution, electric field, etc., compact models provide accurate predictions of device performance at different bias points based on the simplified physics-based equations. These models instead opt for convergence and more rapid simulation time in Newton-Raphson algorithm based simulators. Hence, these models should be computationally efficient and avoid discontinuities in derivatives. This is essentially the definition of a "compact" model. It

compactly represents the 2 and 3 dimensional phenomena with a derivation of analytical expressions suitable for a differential, algebraic solution space.

Any modern circuit or system design requires multiple components. Each component has several parameters that affect the performance of the overall circuit or system. So, there is always a need for optimization based on the performance requirements. Designers either rely on simplistic models for such optimization or use analytical models for particular effects and then optimize the system more or less manually. However, with increasing power, frequency, and size restraints, these optimizations are becoming increasingly more complex. So, just an accurate compact model is not enough. It also needs to be efficient in terms of simulation time. For example, one of the most important and widely used components of the high-frequency power electronics system is the inductor. The parasitic inductances of the cables, traces, and other passives introduce ringing and EMI that ultimately have a severe impact on the system's efficiency and reliability. Unlike simplistic ideal switch models used in MATLAB/Simulink, an accurate power device model can predict the ringing and EMI, saving the circuit from disastrous failures. This type of prediction could particularly be beneficial for SiC power MOSFETs that can operate in the MHz range [6]. Thus, more attention needs to be given to the convergence efficiency along with the accuracy when developing compact models for SiC power MOSFETs.

McNutt *et al.* [7] is one of the earliest contributions to the physics-based compact modeling of SiC power MOSFETs. The introduction of unique expressions for low-voltage turn-on of the corners of the MOSFET and enhanced transconductance for the linear region due to carrier concentration gradient for non-uniform doping in the channel, the model made a great stride towards physics-based compact modeling of SiC power MOSFETs. However, due to the use of a proprietary tool for parameter extraction, the model is not accessible for many users. A modified version of [7]

was presented by Mudholkar *et al.* [8], which included a more accurate description of the MOS channel, the drift region, non-linear capacitances, and the internal charges. Also, [8] presents a user-friendly parameter extraction process from the data commonly available in commercial devices' datasheets. This model was groundbreaking in terms of user accessibility in this regard. Kraus *et al.* [9] focused on the interface trapped charge in the SiC gate oxide and the effects of trapped charge on mobility and surface potential. One of the novelties of the model in [9] is that it modeled the bias-dependent drift resistance for a SiC power MOSFET. However, there were no specific details about modeling the body diode or the body diode's gate dependency. An extensive summary of the models published before 2014 can be found in [10]. No explicit mention of the modeling of body diode can be found in those efforts. The paper in [11] presented gate current modeling of the SiC power MOSFET, which can help with optimizing gate driver design. But significant mismatch can be seen between the simulated and measured results casting doubt on the usefulness in power loss calculations. In [12], an innovative idea of using neural networks for parameter extraction was presented. This approach can significantly reduce the workload of using compact models in circuit simulation and optimization. In [2], a Fourier solution based analytical model of the body diode was provided. However, the model has no gate bias dependency and is not a part of an overall MOSFET model. Some empirical models provide gate-dependent body diode characteristics. However, simulated results hardly match with the measured data [13]. STMicroelectronics developed a model [14] for their internal use. This model has empirical gate dependency. However, they have a look up table (LUT) based capacitance-voltage (C-V) characteristics.

Apart from the gate voltage-dependent body diode characteristics and the reverse recovery, there is a lack of efficient electro-thermal models of the SiC power MOSFET. Though [7], [8] provide

temperature dependency of the different parameters and accurately fit isothermal behavior at different temperatures, continuous temperature scaling and self-heating capability of these models are not verified by experimental data. In [15] however, the authors present an electro-thermal model capable of predicting the device behavior both inside and outside the SOA. But, it lacks the third quadrant behavior. Moreover, the C-V model is purely empirical. In [16], the model of [7] has been used with some modifications to include the leakage-induced breakdown. The model can predict short circuit (SC) failure, validated with measured UIS tests at different temperatures. However, the model does not have third-quadrant behavior included. So, in the case of synchronous rectification, this model will fail to give appropriate loss prediction. The paper in [17] presents an electro-thermal model with self-heating and body diode characteristics. The model is physics-based and requires device fabrication information. For circuit designers, this information is difficult to access. Moreover, the gate dependency of the body diode is not explicitly described. The breakdown mechanism is not included, and so SC simulation is not possible with this model. In [18], the authors describe an electro-thermal model and validate it at different temperatures. Nevertheless, the switching characteristics are not validated. Moreover, there is no mention of third-quadrant characteristics in the paper.

Parasitic inter-electrode capacitances are substantially more influential in determining the MOSFET model's dynamic behavior than the conduction branch. So precise inter-electrode capacitance modeling is required, at least in the operating range of the device. The paper in [19] presents an extensive literature study on the existing capacitance models of the power MOSFET. According to [19], current physics-based and semi-physical models are lacking in terms of C-V modeling compared to the Look-Up Table (LUT) based models. However, LUT-based models cannot predict device scaling and often suffer from convergence issues. The paper in [20] presents

a physics-based accurate model for Miller capacitance (*Cgd*). But it does not provide the gate dependency of the gate to source capacitance (*Cgs*).

Therefore, there is a significant scope of developing a compact physics-based electro-thermal model of SiC power MOSFET with accurate and efficient expressions for both the first and third quadrant behavior, including the reverse recovery of the body diode.

## 1.2. **Research Objectives**

This research aims to develop an accurate and efficient electro-thermal model of SiC power MOSFET for power electronics system simulation. The model will include accurate and efficient expressions for the third quadrant behavior without compromising the first quadrant's accuracy and efficiency. It will have the gate dependency of the body diode and enable simulation of gate voltage oscillation due to crosstalk. Since the body diode is a *p-i-n* configuration structure, it requires the inclusion of reverse recovery. The model will include expressions of the reverse recovery current for accurate overshoot simulation. Necessary modification of the MOSFET expressions will also enable the model to fit the third quadrant characteristics for synchronous converters accurately. For switching characteristics, Miller capacitance ($C_{rss}$) will be accurately modeled at low voltages and high voltages. The gate bias dependency of the input capacitance ($C_{iss}$) will be included. The model will include expressions for the avalanche-induced breakdown voltage for accurate safe operating area (SOA) simulation. The model parameters will be accurately and efficiently made temperature-dependent for a fast and accurate electro-thermal simulation of a system with significant self-heating. Lastly, an easy-to-follow parameter extraction procedure will be developed to make the model easy to use for system designers.

## 1.3. **Key Contributions**

The key contributions of this dissertation are:

a. Gate bias dependent body diode inclusion in SiC power MOSFET model
b. Body diode's reverse recovery modeling for accurate overshoot simulation
c. Accurate modeling of the third quadrant characteristics combining the reverse channel current with the body diode current
d. New smoothing approach to incorporate different physical effects into the model without degrading convergence properties
e. Inclusion of gate bias dependent input capacitance (*Ciss*) and accurate Miller capacitance (*Crss*) at the low voltage region
f. Inclusion of the temperature dependency in the first and third quadrant behavior with the body diode's reverse recovery
g. Verification of the model's accuracy at predicting switching loss by Double Pulse Tests at different temperatures
h. Verification of the electro-thermal model's accuracy by a synchronous Buck converter study
i. Verification of the model's efficiency and convergence properties in a complex power electronics circuit application

## 1.4. **Dissertation Outline**

The main contents of this dissertation are divided into the following chapters:

- Chapter 2: Modeling the first quadrant characteristics
- Chapter 3: Modeling the third quadrant characteristics
- Chapter 4: Modeling Capacitance Voltage (C-V) characteristics
- Chapter 5: Modeling Temperature Dependency

- Chapter 6: Double Pulse Tests (DPTs) at different temperature
- Chapter 7: Synchronous Buck Converter Test
- Chapter 8: A convergence evaluation study
- Chapter 9: Parameter extraction procedure
- Chapter 10: Conclusions and Future Work

In the remainder of this dissertation, model parameters are highlighted by boldface italics (example: ***Vthxy***), whereas simple italic font (example: *Vds*) denotes the bias points (voltage, current, charge). Temperature scaling parameters have '***co***' at the end, and temperature-dependent parameters are denoted by '*_t*'. The model input parameters for room temperature are highlighted with '***0***'. Subscript '*y*' stands for either *f* = forward conduction or *r* = reverse conduction. Subscript 'x' stands for either *l* = low gate voltage region or *h* = high gate voltage region.

# Chapter 2. MODELING THE FIRST QUADRANT CHARACTERISTICS

A physics-based compact model's internal relationship can be represented by various physical parts of the SiC power MOSFET as different subcircuit components shown in Fig. 2-1. There are three external nodes: Drain, Source, and Gate. These nodes are available to the users for biasing different voltages. Three more internal nodes (AI, SI, and DI) are defined to accommodate the voltage drop across the series resistances to reach the device structure's intrinsic drain, source, and the base region. A virtual node Qm is defined as representing the charge build-up during body diode conduction. The voltage, charge, and current in these nodes are interdependent. These dependencies are expressed with physics-based compact differential, algebraic expressions in the model.

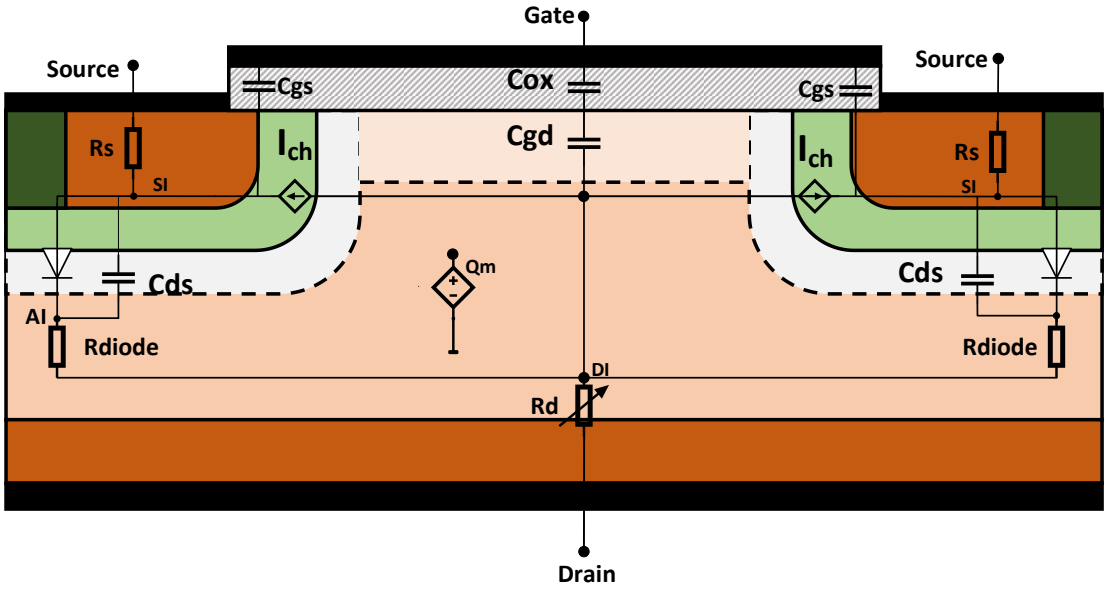


Fig. 2-1. Subcircuit mnemonic representation of the different parts of the SiC power MOSFET model overlaid on the cross-sectional physical structure of the MOSFET device.

## 2.1. **Channel current modeling**

The channel current ($I_{ch}$) expressions for the first quadrant are modified from the physics-based model developed in [8]. There are two components in the channel current expression. One component is for the low gate voltage region ($I_{moslf}$), and one is for the high gate voltage region ($I_{moshf}$).

$$I_{ch} = I_{moslf} + I_{moshf} \tag{1}$$

[8] explains the reason behind these two components' existence as the result of the early turn-on at the corner regions of a vertical MOSFET. Since the electric field is higher at the MOSFET's corner regions, an inversion occurs at a lower gate voltage. Due to early turn-on, these corners carry most of the current at the low gate voltage. Current through the central device area becomes prevalent at a higher gate voltages. Here higher gate voltage means gate voltages higher than the Miller voltage, i.e. ($V_{gs} > V_{Miller}$). Alternatively, the different threshold voltages ($V_{thl\_t}, V_{thh\_t}$) for low and high gate voltages can be explained in terms of interface state charges at the gate oxide. The number of filled interface trap states depends on the applied electric field. Depending on the density of the filled trap states, it takes different gate electric fields to invert the channel region. Also, the MOS capacitor seen by the inversion channel differs depending on the filled trap states, and it changes the vertical electric field and channel mobility. Hence, different transconductance parameters ($K_{pl\_t}, K_{ph\_t}, K_{fl\_t}, K_{fh\_t}$) are required to express, and thus fit the model to experimental data, the channel current of a SiC power MOSFET accurately. Moreover, carrier diffusion occurs between different sections of the channel region due to having different doping profiles. This diffusion is drain bias dependent. Hence, different transconductance parameters are required for the linear ($K_{fl\_t}, K_{fh\_t}$) and for the saturation region ($K_{pl\_t}, K_{ph\_t}$).

There is an enhanced linear region in a SiC power MOSFET compared to its Si counterpart. This phenomenon is termed ‘soft saturation’. The reason behind this dilation is the existence of more prominent interface trapped charges. The two-dimensional effect of these trapped charges affects the electric field over the gate-drain overlap area. The carriers' velocity saturates gradually in the presence of this interface trapped charge-induced electric field [21], [22]. This gradual transition from linear to saturation region is included in the model with the pinch-off parameter (*pvf*). Since the trapped charge distribution depends on the gate voltage, the pinch-off voltage parameter also depends on the gate voltage. Instead of making it a variable and increasing the model's convergence time, two different constant pinch-off parameters (***pvf$_l$***, ***pvf$_h$***) are used for low and high gate voltage regions to accurately capture this effect. So, the channel current expression becomes:

$$I_{mosxf} = k_{fxf\_}t \cdot k_{pxf\_}t \cdot Vgs_{effxf} \cdot Vds_{effxf} - \boldsymbol{pvf}_{\boldsymbol{x}}^{K_{xf}-1} \cdot Vds_{effxf}^{K_{xf}} \cdot \frac{Vgs_{effxf}^{\frac{2-K_{xf}}{K_{xf}}}}{1+\Theta_{xf\_}t \cdot Vgs_{effxf}} \tag{2}$$

$$K_{xf} = \frac{\boldsymbol{k}_{fxf\_}t}{\boldsymbol{k}_{fxf\_}t - \frac{\boldsymbol{pvf}_{\boldsymbol{x}}}{2}} \tag{3}$$

Eq. (3) makes the transition between linear and saturation region continuous at the pinch-off voltage using the intermediary transconductance term, $K_{xf}$. Recall here that the subscript $x = l, h$ represents low gate voltage and high gate voltage region, respectively.

Though physics-based and accurate, most of the existing compact models of SiC power MOSFETs lack continuity in the higher-order derivatives due to the model expressions' piecewise nature. This lack of continuity limits the model's convergence capability in transient analysis and limits the step size, affecting the simulation's speed [23]. The developed model solves this issue by replacing the

piecewise equations with continuous ones. This is done by making the *Vds* and *Vgs* continuous weighted functions, namely, $Vdseff_f$ and $Vgseff_f$. as shown with Eq. (4) and (5).

$$Vgs_{effxf} = \frac{\ln(1 + e^{Vgs - V_{thxf\_t}})}{1 + e^{-(Vgs - V_{thxf\_t} - 2\boldsymbol{\partial})}} \tag{4}$$

$$Vds_{effxf} = Vds_{satxf} - \frac{1}{2}\left( (Vds_{satxf} - Vds_f - \boldsymbol{\partial}) + \sqrt{(Vds_{satxf} - Vds_f - \boldsymbol{\partial})^2 + 4 \cdot \boldsymbol{\partial} \cdot Vds_{satxf}} \right) \tag{5}$$

$Vds_{satxf}$ is the saturation voltage and expressed as

$$Vds_{satxf} = \frac{Vgs_{effxf}}{\boldsymbol{pvf_x}} \tag{6}$$

Effective first-quadrant drain to source voltage, $Vds_f$ decouples the first quadrant channel current expression from the third quadrant operation without using a piecewise equation.

$$Vds_f = \frac{1}{2}\left(Vds + \sqrt{Vds^2 + 4\boldsymbol{\partial}^2}\right) \tag{7}$$

Here, $\boldsymbol{\partial}$ is a smoothing parameter. The value of $\boldsymbol{\partial}$ should be $0.1\mu \leq \boldsymbol{\partial} \leq 1\mu$ range to ensure minimum impact on the device's accuracy while maintaining the smooth transition from the first to third quadrant. If it is too small ($\leq 0.1\mu$), there is no gradual change between the third and the first quadrant. But too large ($\geq 1\mu$) value will make current at zero voltage too large to give a very inaccurate result.This approach of weighted functions to decouple expressions between the first and third quadrant effectively enable the model to be continuous in the higher-order derivatives.

The parameters related to the first quadrant channel current modeling is listed in Table 2-1.

**Table 2-1. Parameters for Channel Current Modeling**

| Notation | Definition |
|---|---|
| $V_{thlf\_t}$ | Low current threshold voltage |
| $V_{thhf\_t}$ | High current threshold voltage |
| $\Theta_{lf\_t}$ | Transverse electric field mobility factor at the low gate voltages |

**Table 2-1. Parameters for Channel Current Modeling (Cont.)**

| Notation | Definition |
|---|---|
| $\Theta_{hf}\_t$ | Transverse electric field mobility factor at the high gate voltages |
| $k_{plf}\_t$ | Saturation region transconductance parameter at low gate voltages |
| $k_{phf}\_t$ | Saturation region transconductance parameter at high gate voltages |
| $k_{flf}\_t$ | Triode region transconductance parameter at low gate voltages |
| $k_{fhf}\_t$ | Triode region transconductance parameter at high gate voltages |
| $\boldsymbol{pvf_l}$ | Pinch-off parameter for low-gate voltage region |
| $\boldsymbol{pvf_h}$ | Pinch-off parameter for high-gate voltage region |
| $\boldsymbol{\partial}$ | Smoothing parameter |

## 2.2. **On-resistance modeling**

The total resistance seen by the current during conduction ($R_{total}$) can be divided into three components: channel resistance ($R_{ch}$), source resistance ($R_s$), and drain resistance ($R_d$). $R_{ch}$ is the intrinsic channel resistance and comes from the voltage-current relation of Eq. (2). The $R_s$ contains the contact resistance between metal contact and the highly doped source region. The bias dependency of this resistance is negligible and can be expressed by a constant parameter (***rs***).

$$R_{total} = R_{ch} + rs\_t + R_{df} \tag{8}$$

However, $R_{df}$ has three major components with different dependencies on the bias conditions. First, there is a constant part due to the metal's contact resistance and the highly doped $n^+$ substrate. It has been modeled by a constant parameter (***rd***).

$$R_{df} = rd\_t + R_A + R_{jfet} \tag{9}$$

Second, the accumulation region resistance ($R_A$) is formed in the undepleted accumulation region due to the gate's overlap on the drain region. The resistance in this accumulation is lower compared to the bulk area. As the drain bias increases, this *Vds*-induced depletion region increases from the

lateral direction. With the reduction in accumulation width in the lateral direction, the resistance of the current path decreases.

$$W_{dep} = \sqrt{2 \cdot \varepsilon_{sic} \cdot \frac{Vds_f}{e \cdot nb}} \tag{10}$$

$$W_a = \boldsymbol{wb} - W_{dep} \tag{11}$$

$$R_A = \frac{W_a}{e \cdot \boldsymbol{a} \cdot \boldsymbol{nb} \cdot \mu_e} \tag{12}$$

The depletion width ($W_{dep}$) increases with increasing forward bias conditions. This increase in the depletion region decreases the accumulation region ($W_a$), reducing the $R_A$.

The modeling of the JFET region resistance ($R_{jfet}$) is a topic of active research. Different approaches have been adopted in previous models. In [9], the authors adopted a semi-physical approach to model the drift region where both drain and gate voltage dependencies of the resistance are modeled. Since that model is a surface potential-based model, the approach is not adopted in threshold voltage-based models. In this work, the JFET region resistance is modeled using an empirical formula developed in [24].

$$R_{jfet} = \left(Vds_f \cdot \boldsymbol{RDVD}\right) \cdot \left(1 + \boldsymbol{RDVG1} + \frac{\boldsymbol{RDVG1}}{\boldsymbol{RDVG2}} \cdot Vgs\right) \tag{13}$$

**Table 2-2. Parameters for On-resistance Modeling of the First Quadrant**

| Notation | Definition |
|---|---|
| *rs_t* | Parasitic source resistance |
| *rd_t* | Constant drain resistance for forward conduction |
| ***RDVD*** | Drain-dependency parameter of the drift resistance |
| ***RDVG1*** | First gate-dependency parameter of the drift resistance |

**Table 2-3. Parameters for On-resistance Modeling of the First Quadrant (Cont.)**

| Notation | Definition |
|---|---|
| ***RDVG2*** | Second gate-dependency parameter of the drift resistance |
| ***a*** | Total active area |
| ***nb*** | Doping in the base region |

## 2.3.**Leakage current and breakdown modeling**

Though switching loss plays a significant role in determining a power electronic system's efficiency, it is important to have breakdown characteristics to design reliable systems, especially with the large *dv/dt* of wide bandgap devices. Moreover, the breakdown voltage (*vbr_t*) changes with temperature making it essential to model it over temperature in an electro-thermal model. This model includes the leakage current-induced breakdown voltage mechanism. Though more relevant for practical failures of the device, the mechanical damage-induced breakdown is not modeled here.

The leakage current is caused by three primary effects: a. Thermal generation Current. b. Diffusion current, and c. Avalanche multiplication current [25]. Though these three leakage currents have different physical mechanisms, they are all temperature-dependent and proportional to the square root of *Vds*. Instead of using different expressions for these leakage currents, a unified expression, Eq. (14), has been used in this model to include the leakage current characteristics.

$$I_{leakage} = \frac{I_{leakage0\_t}}{\boldsymbol{\tau_{leakage}}} \sqrt{\boldsymbol{nb} \cdot Vds_f} \tag{14}$$

$I_{leakgae0\_t}$ is the leakage current at zero drain voltage. It depends on device geometry and intrinsic carrier concentration. $\tau_{leakage}$ is the lifetime of the carriers in the channel region. $Vds_f$ is the

effective voltage for breakdown characteristics used for a smooth transition into the breakdown region.

According to [25], the failure of a SiC power MOSFET is primarily determined by the increase of temperature at the JFET region. The increasing temperature increases the leakage current due to avalanche multiplication. This increased leakage current turns-on the parasitic *npn* transistor. The avalanche effect caused by the increased leakage current is modeled according to the method described in [26].

$$M = \frac{1}{1 - \left(\frac{Vds_f}{\boldsymbol{vbr}}\right)^{\boldsymbol{bvn}}} \tag{15}$$

$$I_{mult} = (M - 1) \cdot I_{mos} + M \cdot I_{leakage} \tag{16}$$

Here, $I_{mult}$ is the avalanche multiplication current. $M$ is the multiplication factor that depends on the blocking voltage. The channel current $I_{mos}$ includes the gate dependency of the breakdown voltage.

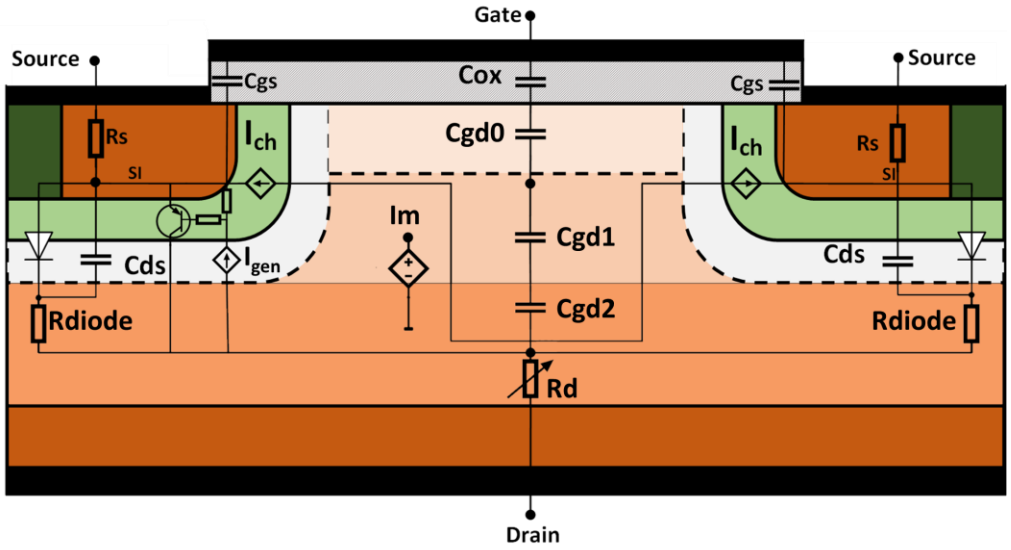


Fig. 2-2. Subcircuit mnemonic representation showing the parasitic *npn* for breakdown modeling.

The inclusion of thermal runway in the model is accomplished with a generic SPICE-like *npn* device as the parasitic bipolar junction transistor (BJT). This *npn* is formed between the source contact, body, and drift region of the power MOSFET as shown in Fig. 2-2. Table 2-4 lists the parameters related to the breakdown characteristics.

**Table 2-4. Parameters for Breakdown Modeling**

| Notation | Definition |
|---|---|
| $I_{leakage0}\_t$ | Intrinsic leakage current |
| $\tau_{leakage}$ | Constant drain resistance for forward conduction |
| *vbr_t* | Constant drain resistance for reverse conduction |
| ***bvn*** | Exponential avalanche multiplication exponent |

## 2.4. **First quadrant model validation**

The developed model can accurately fit the first quadrant characteristics of a SiC power MOSFET. Different commercially available SiC power MOSFETs with various ratings have been characterized to the model. Table 2-4 lists the devices characterized for validation in this dissertation, but the number of devices and their ratings are increasing through collaborations with our power electronics group. The Keysight B1505A was used for the measurements. The industry-standard parameter extraction tool IC-CAP has been used to extract the model parameters. The parameter extraction procedure, along with the sequence, is described in Chapter 8. Appendix I describes the routine used in IC-CAP for the extraction. In this subsection, only the accuracy of the first quadrant characteristics is highlighted.

**Table 2-5. List of Commercial Devices Measured for Model Validation**

| Device part number | Company name | Voltage rating (V) | Current rating (A) |
|---|---|---|---|
| **C3M0025065D** | Wolfspeed | 650 | 97 |
| **C2M0080120D** | Wolfspeed | 1200 | 36 |
| **C2M0045170D** | Wolfspeed | 1700 | 72 |

The output characteristics are fit during the parameter extraction procedure, and so they show excellent accuracy. Fig. 2-3 shows the comparison of the simulated results of the developed model with the measured data for the devices C2M0080120D and C2M0045170D. The RMS error is 1.2% and the maximum error is 8% in the rated operation range. Fig. 2.4 shows the comparison with the model of [8]. The RMS error is more than 4% and maximum error is 9%. Both models share the same fundamental equations as mentioned in the model development section, and so the accuracy is almost equal in the first quadrant characteristics in an isothermal situation. Nevertheless, having two pinch-off voltage parameters (***pvfl***, ***pvfh***), the presented model can fit the linear to saturation transition regions more accurately than [8] for all the gate voltages.

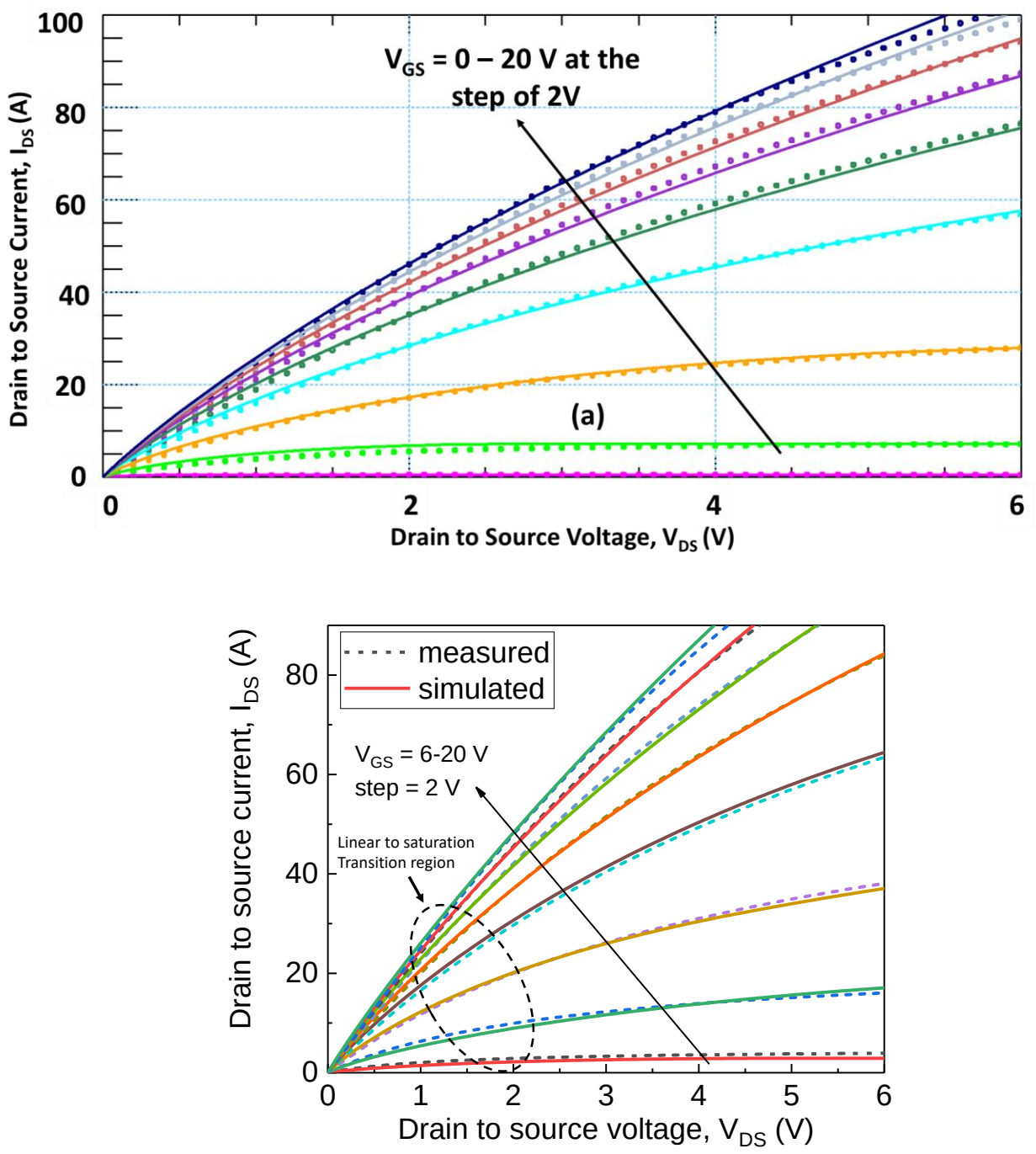


Fig. 2-3. Simulated with the presented model (solid line) and measured (dash line) first quadrant output characteristics of (a) C2M0045170D (b) C2M0080120D.

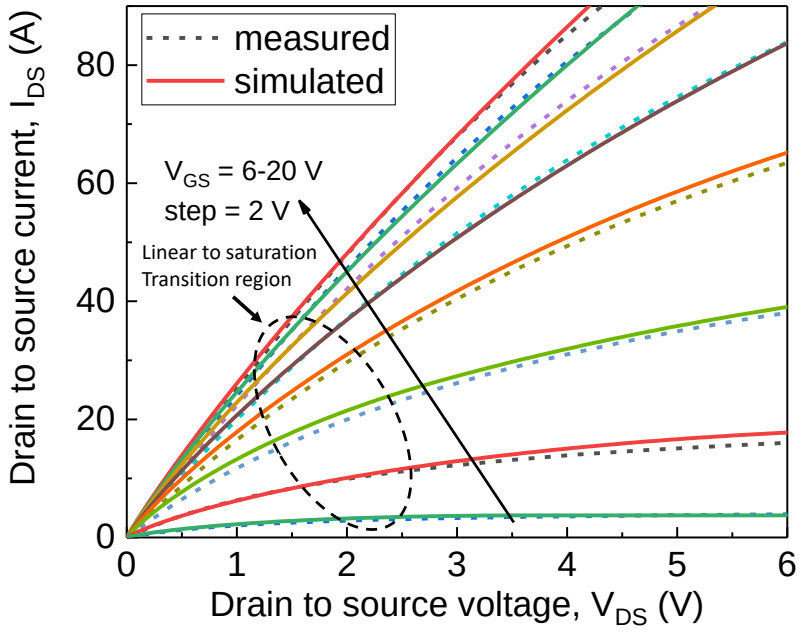


Fig. 2-4. Simulated with the previous model of [8] (solid line) and measured (dash line) first quadrant output characteristics of C2M0080120D.

For conduction loss analysis, on-resistance accuracy as a function of the gate drive voltage is the most crucial factor. The following figures show the model's accuracy to simulate the *Rds(on)* for different SiC MOSFETs at their desired gate voltage drive.

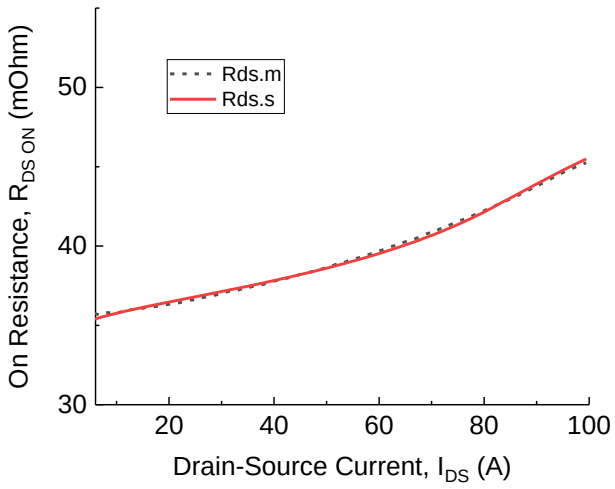


Fig. 2-5. Measured and simulated $R_{DS(on)}$ at Vgs = 20 V of C2M0080120D.

Unlike [8], the presented model's parameter extraction procedure does not depend on the transfer characteristics of the device. Still, the extracted model perfectly fits the devices' transfer characteristics as shown in the figures below.

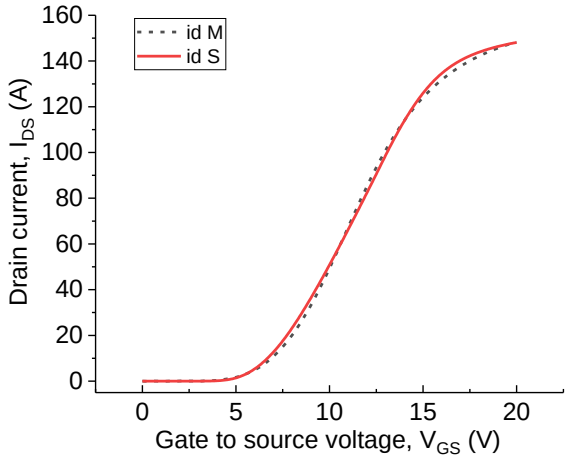


Fig. 2-6. Measured and simulated transfer characteristics of C2M0080120D.

Fig. 2-7 shows the model's capability to simulate the leakage current and breakdown characteristics. Due to the proper smoothing technique, the inclusion of the breakdown characteristics does not create any convergence problem.

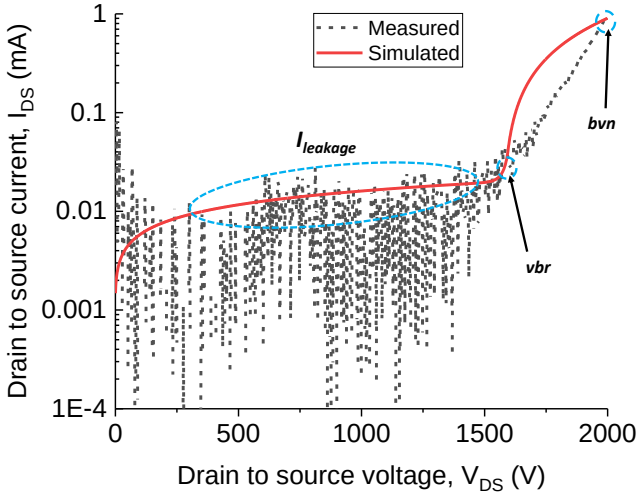


Fig. 2-7. Leakage current and breakdown characteristics related parameter extraction.

# Chapter 3. MODELING THE THIRD QUADRANT CHARACTERISTICS

The third quadrant operation ($Vds < 0$, $Ids < 0$) is marked by the opposite direction of current compared to first quadrant operation. In this operation range, there are two mechanisms for current flow. First, current can flow across the inversion channel formed by the positive gate voltage. This is the same MOSFET mechanism as the first quadrant, except that the current flows from source to drain. Second, the body diode conduction, where current flows as a result of the *p-i-n* diode conduction mechanism. For an accurate simulation of the third quadrant behavior, both of these effects need to be accurately included.

## 3.1. **Reverse MOSFET conduction**

The channel region sees an inversion of charge for *Vgs* higher than the threshold voltage, even when *Vds* is negative. Majority carriers, i.e., electrons, can travel from source to drain through this low resistive path. This is the channel conduction mechanism. This mechanism dominates when the voltage drop across the body diode is insufficient to turn on the diode.

Though the mechanism is the same, the threshold voltage, transconductance, and on-resistance are not the same as the first quadrant. Numerical simulation has been performed to verify this difference. In Fig. 3-1 we can see the charge distribution at the first and third quadrant conditions. $|Vds|$ is kept at 1 V so that the body diode is not turned on. An inversion layer is formed at $Vgs$ = 5.6 V for the third quadrant condition. However, there is no inversion layer for the first quadrant. It means that threshold voltage is lower for third quadrant operation. This difference in threshold voltage arises from the depletion layer between *p* base and *n* drift region. For a negative drain bias referenced to the source, the depletion layer thickness is less than when the drain has a positive bias. The continuous inversion channel can form at a lower gate voltage because the depletion

width is less for the third quadrant case. The transfer curves (Fig. 3-2) from the numerical simulation verify this assertion.

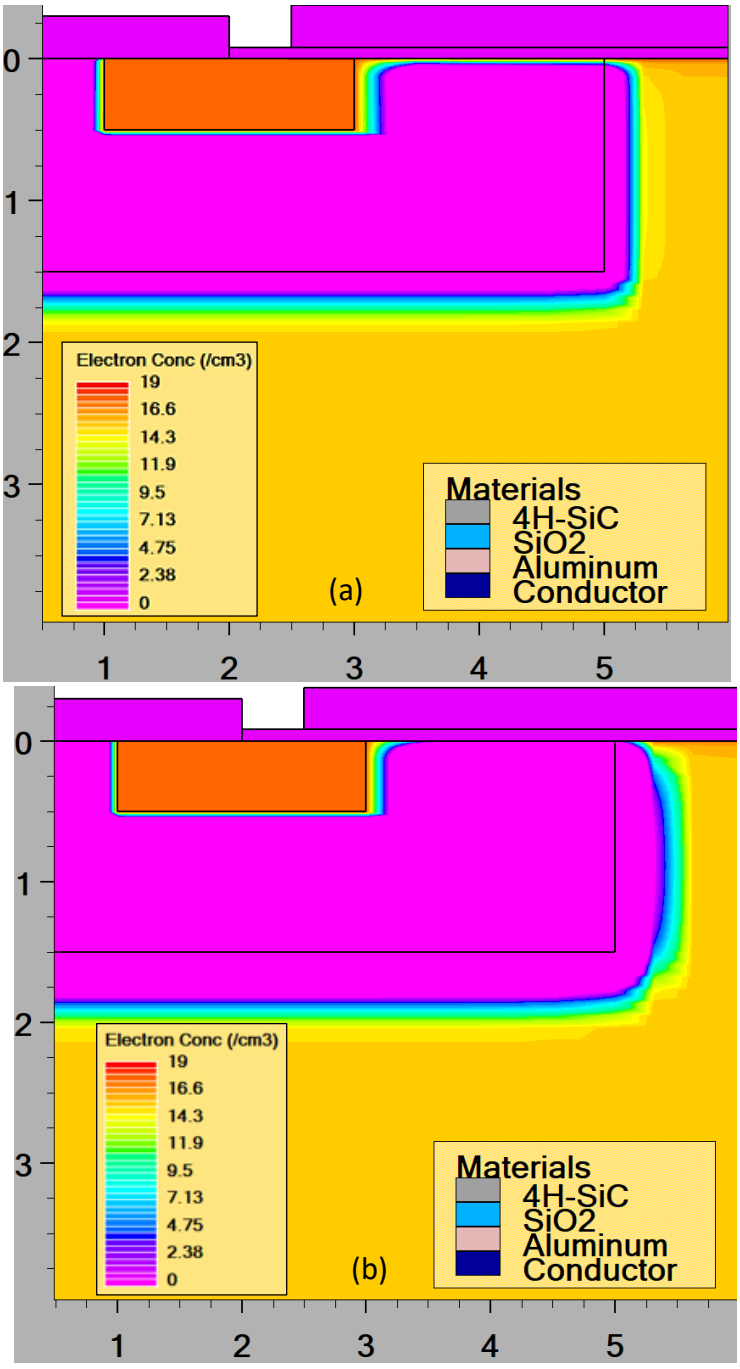


Fig. 3-1. Numerical simulation of SiC power MOSFET to observe inversion channel condition (a) For Vgs = 5.6 V, Vds = -1 V (b) For Vgs = 5.6 V, Vds = 1 V.

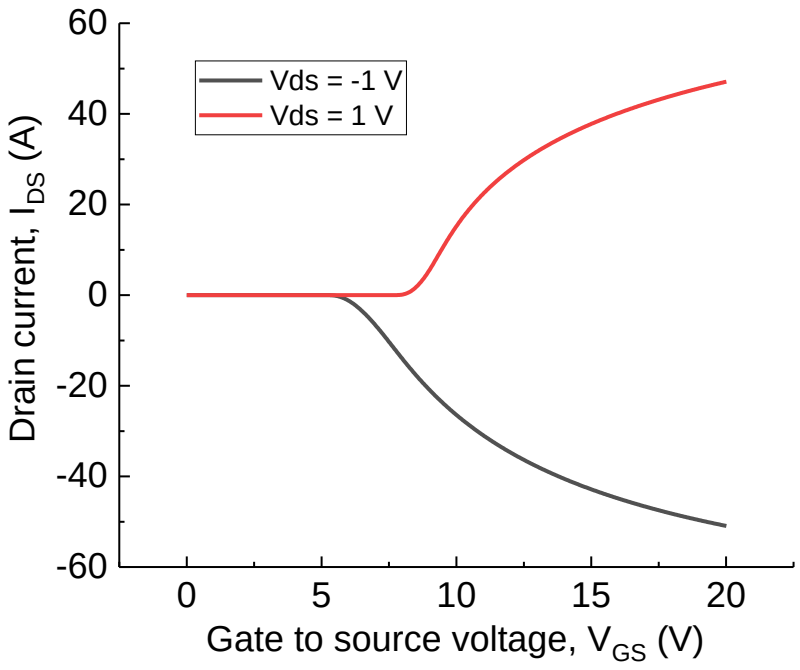


Fig. 3-2. TCAD simulated transfer characteristics of a SiC power MOSFET at the first and third quadrant operation.

These differences in the first and third quadrant require separate sets of parameters for accurate modeling. In the developed model, the first and third quadrant are decoupled from each other. The decoupling is achieved using the weighted functions of the bias voltages. The channel current in the third quadrant is modeled by the equations below.

$$I_{chr} = I_{moslr} + I_{moshr} \tag{17}$$

$$I_{mosxr} = k_{fxr\_}t \cdot k_{pxr\_}t \cdot Vgs_{effxr} \cdot Vds_{effxr} - \boldsymbol{pvf_x^{K_{xr}-1}} \cdot Vds_{effxr}^{K_{xr}} \cdot \frac{Vgs_{effxr}^{\frac{2-K_{xr}}{K_{xr}}}}{1+\theta_{xr\_}t \cdot Vgs_{effxr}} \tag{18}$$

$$K_{xr} = \frac{\boldsymbol{k_{fxr}}}{\boldsymbol{k_{fr}} - \frac{\boldsymbol{pvf_x}}{2}} \tag{19}$$

$$Vgs_{effxr} = \frac{\ln(1 + e^{Vgs - V_{thxr\_}t})}{1 + e^{-(Vgs - V_{thxr\_}t - 2\boldsymbol{\partial})}} \tag{20}$$

$$Vds_{effxr} = Vds_{satxr} - \frac{1}{2}\left((Vds_{satxy} - Vds_r - \boldsymbol{\partial}) + \sqrt{(Vds_{satxr} - Vds_r - \boldsymbol{\partial})^2 + 4 \cdot \boldsymbol{\partial} \cdot Vds_{satxr}}\right) \tag{21}$$

$$Vds_{satxr} = \frac{Vgs_{effxr}}{\boldsymbol{pvf_x}} \tag{22}$$

$$Vds_r = Vds - \frac{1}{2}\left(Vds + \sqrt{Vds^2 + 4\boldsymbol{\partial^2}}\right) \tag{23}$$

$$R_{dr} = \boldsymbol{rdr} \tag{24}$$

**Table 3-1.Parameters for Channel Current Modeling of the Third Quadrant**

| Notation | Definition |
|---|---|
| $V_{thlr}\_t$ | Low current threshold voltage for reverse conduction |
| $V_{thhr}\_t$ | High current threshold voltage for reverse conduction |
| $\Theta_{lr}\_t$ | Transverse electric field mobility factor at the low gate voltages for reverse conduction |
| $\Theta_{hr}\_t$ | Transverse electric field mobility factor at the high gate voltages for reverse conduction |
| $k_{plr}\_t$ | Saturation region transconductance parameter at low gate voltages for reverse conduction |
| $k_{phr}\_t$ | Saturation region transconductance parameter at high gate voltages for reverse conduction |
| $k_{flr}\_t$ | Triode region transconductance parameter at low gate voltages for reverse conduction |
| $k_{fhr}\_t$ | Triode region transconductance parameter at high gate voltages for reverse conduction |
| $rdr\_t$ | Constant drain resistance for reverse conduction |

In the third quadrant, the high current region is dominated by the body diode characteristics. So $R_{jfet}$ and $R_A$ are negligible for the channel current conduction modeling. Instead, a constant reverse

drain current resistance parameter (***rdr***) is used for the on-resistance modeling. Table 3-1 lists the parameter set for the third quadrant channel current modeling.

### 3.2. **Body diode modeling**

In the power MOSFET, the *n*+ source and *p*- body are physically and electrically shorted to stop the parasitic *npn* BJT activation. Hence, a *p*-*i*-*n* diode structure is formed between *p* body, lightly doped *n*-type drift region, and heavily doped *n*+ drain contact. This diode structure is an anti-parallel configuration across the MOSFET conduction path. This inherent diode structure of the vertical MOSFET structure is called the body diode. However, this diode only turns on when the voltage drop across the *p*-body and *n*-drift region's junction is higher than the diode's built-in voltage ($V_f$). Once the diode turns-on, the current starts to flow through this low resistive path. As a result, diode-like characteristics dominate the higher voltage output characteristics for the third quadrant behavior.

For *Vgs* less than the threshold voltage, there is an absence of the inversion layer in the channel region, so current can only flow through the body diode. The body diode starts to conduct when the source to drain voltage, *Vsd* is greater than $V_f$. However, $V_f$ is a function of the potential barrier. An increase in the potential barrier due to increasing negative gate bias increases the potential barrier at the *p*-*n* junction [27], [28]. The part of the *n*-type region just under the gate is termed the JFET region because of JFET-like behavior in the presence of two approaching depletion regions. The area's potential remains close to zero when *Vgs* = 0 V. An accumulation layer is formed with the increasing positive *Vgs*. This accumulation layer reduces the potential barrier at the *p*-*n* junction. Thus, the $V_f$ voltage also decreases between the body and the drift region [28]. The maximum positive *Vgs* for which the body diode conduction is the only conduction mechanism is determined by the first knee voltage parameter, *vk1*. In the accumulation layer's presence, the

injection efficiency changes from the theoretical SiC *p-i-n* configuration and becomes gate dependent. This effect is modeled as a change in the ideality factor because barrier height is a function of ideality factor. The constant part of the ideality factor is expressed as a parameter (*ND_t*), while the bias-dependent part of the ideality factor is expressed with the following equations.

$$V_{bdiodeff} = V_{bdiode} - \frac{1}{2}\left(V_{bdiode} + \sqrt{V_{bdiode}^2 + 4\boldsymbol{\delta}^2}\right) \tag{25}$$

$$V_{gsnreff\_vk1} = (Vgs - vk1\_t) - \frac{1}{2}((Vgs - vk1\_t) + \sqrt{(Vgs - vk1\_t)^{\mathbf{2}} + 4\boldsymbol{\delta}^2}) \tag{26}$$

$$t_1 = -kvsg_{1\_}t \cdot V_{gsnreff\_vk1} \tag{27}$$

$$t_2 = t_1 \qquad if\ t_1 > 0,\ \ else \qquad t_2 = \frac{-t_1}{2t_1 - 1} \tag{28}$$

$$ND_1 = ND\_t + t_2 \tag{29}$$

$$t_{\mathrm{mp1}} = e^{\frac{-V_{bdiodeff}}{Nd_1 * V_T}} \tag{30}$$

$ND_1$ is the effective ideality factor. Since the body diode is a third quadrant characteristic and there is no symmetric behavior in the first quadrant, it needs to be decoupled and only effective for appropriate conditions. This is accomplished through the weighted function of the bias voltages with Eqs. (25) and (26). Eq. (25) makes the expression for the voltages across the body diode ($V_{bdiodeeff}$) continuous for the first and third quadrant without using any conditional statements, while Eq. (26) expresses the effective gate to source voltage ($V_{gsnreff\_vk1}$) modified with the parameter ***vk1***. Here $t_1$, $t_2$, and $t_{mp1}$ are intermediary terms for the calculation, and $V_T$ is the thermal voltage.

Opposite to the positive gate bias, negative gate bias creates and extends a depletion layer in the JFET region. Hence, the potential barrier in the *p*-*n* junction increases, which leads to the increase of $V_f$. The depletion width reaches its maximum when a certain negative gate voltage is applied and remains the same after that [28]. This can be seen in the body diode characteristics with tightly packed curves after a particular negative gate voltage value. It means that the effect of *Vgs* on controlling the potential barrier has reached saturation. This saturation gate voltage for the body diode is assigned as a model parameter ***vk2***. For *Vgs* < ***vk2,*** there is minimal effect of gate voltage on the body diode curves. The vertical electric field created from the gate controls the overall carrier injection through the body diode junction. So the gate voltage dependency is modeled by a multiplier of the body diode saturation current (***Isbody***).

$$V_{gsnreff\_vk2} = (Vgs - vk2\_t) - \frac{1}{2}((Vgs + vk2\_t) + \sqrt{(Vgs + vk2\_t)^2 + 4\delta^2}) \tag{31}$$

$$t_3 = -\frac{V_{gsnr_{eff\_vk2}}}{kvsg_2\_t} \tag{32}$$

$$t_4 = t_3 \qquad if\ t_3 > 0,\ \ else \qquad t_4 = \frac{-t_3}{2t_3 - 1} \tag{33}$$

$$t_{\mathrm{mp2}} = e^{-t_4} \tag{34}$$

$$I_{bdiode} = \frac{\boldsymbol{Isbody}}{t_{mp2}} \cdot (t_{mp1} - 1) \tag{35}$$

Total body diode current ($I_{bdiode}$) is expressed by Eq. (35). The effective gate voltage for the diode saturation ($V_{gsnreff\_vk2}$) smoothes out the *Vgs* in the < ***vk2*** range. Here, $t_3$, $t_4$, and $t_{mp2}$ are the intermediary terms of the overall equation.

### 3.3. **Body diode resistance modeling**

The body diode current conduction goes through a different path compared to the channel current. This can be seen from the numerical simulation. It does not see the JFET or accumulation region. Instead, the body diode conduction is bipolar in nature. As a result, conductivity modulation takes place in the *p-i-n* structure of the body diode. At room temperature, the conductivity modulation up to the rated current level can be modeled using just a constant parameter ***rdiode0***. However, at the higher temperatures (>150°C) the conductivity modulation becomes severe even within the rated current range. It is then necessary to include the conductivity modulation in the developed model for proper simulation of the body diode's third quadrant characteristics.

Physics-based modeling of conductivity modulation requires iterative solutions [29]. Besides being computationally expensive, this solution often leads to convergence issues. Alternatively, an empirical approach has been taken to model the conductivity modulation. This approach aims to include the gate voltage dependency on the slopes of the body diode curves. From the output characteristics, it is seen that at higher *Vgs* the conductivity modulation is higher due to lower potential barriers. The diode path resistance is expressed as:

$$rdiode\_t = \frac{rdiode0\_t}{1 + rdiovgs\_t \cdot V_{gsnreff\_vk1}} \tag{36}$$

Here, *rdiode0_t* is the resistance seen in the body diode conduction path at *Vgs = vk1_t*· *rdiovgs_t* is the tuning parameter for the gate dependency. Both of these are temperature-dependent.

### 3.4. **Reverse recovery modeling**

The *p-i-n* structure of the body diode goes through high-level injection during the operation. This results in minority carrier build-up in the drift region of the body diode. This excess charge diffuses from the center of the drift region towards the terminal when the diode is reversed biased.

Therefore, instead of a snappy turn-off, reverse recovery causes the body diode to turn-off gradually. This effect is different from the softer recovery caused by the drain to source capacitance (*Cds*). Capacitive current is non-dissipative, i.e., total loss during turn-on and turn-off is zero. But reverse recovery current is dissipative and causes a significant amount of power dissipation during switching [30]. It is therefore imperative to model the reverse recovery of the body diode in high voltage SiC MOSFETs, where peak reverse recovery can reach up to 30% [2].

The reverse recovery effect is included in this model following the method of [30]. While [30] showed how to implement reverse recovery current in a diode conduction mechanism, this work extends the idea for a gate-dependent body diode, part of an overall power MOSFET. The basic charge-control method is extended with the simplification of the lumped charge concept. A virtual node, *Qm*, is added as the representative of the total stored charge in the middle of the drift region. The total injected charge (*Qe1*) into the drift region is proportional to the body diode current ($I_{bdiode}$). The amount of charge recombined is expressed as (*Qe1* - *Qm*). An iterative relation exists between the total diode current and the total charge. $Q'_{m1}$ stands for the stored charge before recombination, and $Q_{m1}$ stands for the stored charge after the recombination.

$$Q_{e1} = \boldsymbol{\tau} \cdot I_{bdiode} \tag{37}$$

$$I_m = (Q_{e1} - Q_{m1})/TT\_t \tag{38}$$

$$Q_{m1} = \tau\_t \cdot (I_m - \frac{d}{dt} Q'_{m1}) \tag{39}$$

Eq. (38) expresses the relation between recombination current ($I_m$) with the recombined charge. Eqs. (38) and (39) are solved iteratively at each time step for the total diode current, including the reverse recovery of the stored charge in the middle of the drift region. For modeling the reverse

recovery, we need to add two parameters. *TT_t* is the total transit time, and *τ_t* is the carrier lifetime.

Though this approach is computationally expensive due to iteration, the model's overall efficiency has been improved by the smoothing approach that decouples the first and third quadrant characteristics. No piecewise conditional statement is used for the current and charge expressions. So, even the higher-order derivatives are continuous for any real values.

**Table 3-2.Parameters for Body Diode Modeling**

| Notation | Definition |
|---|---|
| ***Isbody*** | Diode saturation current |
| *vk1_t* | The positive knee gate voltage |
| *vk2_t* | The negative knee gate voltage |
| $kvsg_1\_t$ | Gate dependent body diode gain factor |
| $kvsg_2\_t$ | Gate dependent body diode gain factor for negative gate voltages |
| *ND_t* | Body diode ideality factor |
| *rdiode_t* | The series resistance of the body diode |
| *rdiovgs_t* | Gate bias dependent conductivity modulation parameter |
| *τ_t* | The lifetime of the minority carriers in the drift region |
| *TT_t* | Diffusion transit time |

### 3.5. **Third quadrant model validation**

Having different parameter sets for the first and third quadrant characteristics allows the developed model to replicate these two quadrants' asymmetric characteristics accurately. Fig. 3-3 shows the

capability of the model to capture the asymmetric transfer characteristics of the two quadrants.

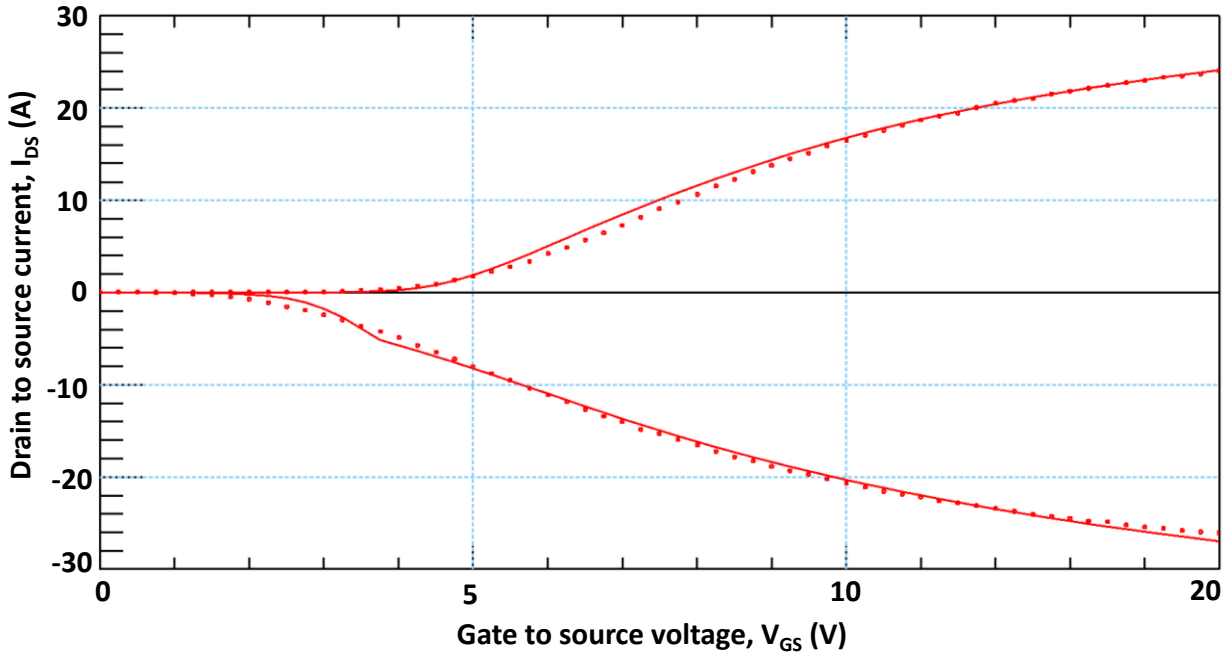


Fig. 3-3. Measured (dot) and simulated (solid) asymmetric transfer curves of C2M0045170D for the first and the third quadrant operation with Vds = |1| V.

Most of the previous models, [8] for example, have the symmetric first and third quadrant characteristics for $Vgs > |V_{threshold}|$. As a result, they cannot accurately simulate the MOSFET behavior in all regions of operations. This can be seen in Fig. 3-4. While the presented model has an error of 0.2%, the model of [8] has an error of around 9%. This accuracy is important for the simulation of applications where the MOSFET's third quadrant characteristics are used. For example, in synchronous rectification, the third quadrant MOSFET characteristics are utilized to lower conduction loss. So, the model of [8] will have a 9% error just in conduction loss calculations. The switching loss calculation will have an even higher error percentage due to the lack of a reverse recovery model.

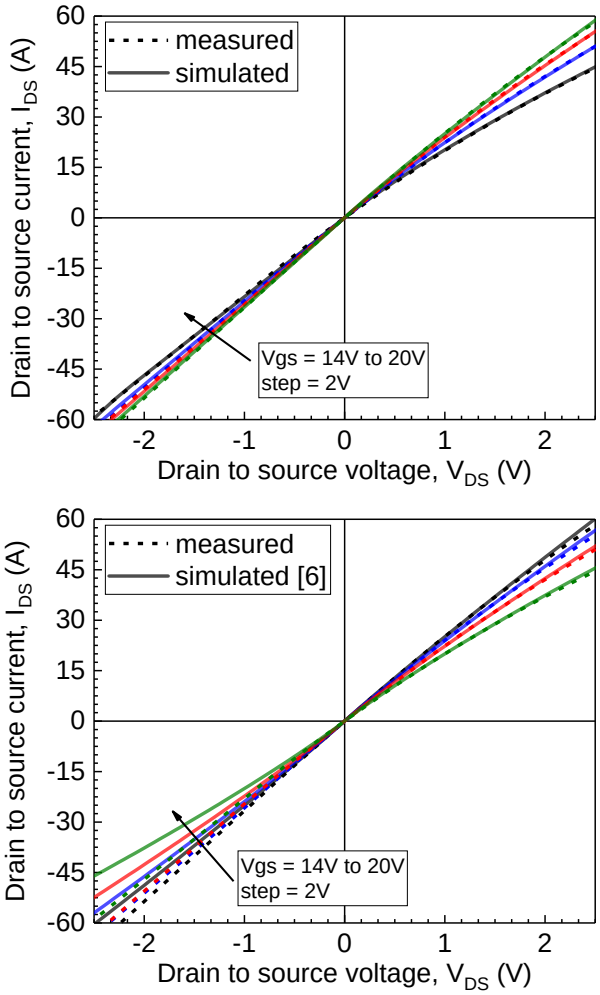


Fig. 3-4. Comparison with measured asymmetric output characteristics at first and the third quadrant with the simulated results of (a) the presented model (b) model of [8].

Fig. 3-5 shows simulated and measured reverse output characteristics of the device. Unlike any previous model, the developed model can accurately fit body diode curves for any gate voltage. Accurate modeling of the body diode's gate dependency is important because calculating the body diode's conduction loss depends on it. Commonly, the body diode is either biased to -5 V or 0 V to make it function like a freewheeling diode. A separate SPICE diode model fit to either -5 V or 0 V is used for circuit simulation. However, this approach has limitations because it cannot predict the body diode's behavior when the gate bias changes. For example, due to crosstalk in the gate loop, the gate bias might see large positive or negative voltage spikes and gate oscillations. These

gate bias nonidealities are common in high *dv/dt* and *di/dt* switching applications. Hence, for accurate simulation at the high-frequency applications (≥ 40 kHz), the body diode's gate dependency model is required. Electromagnetic Interference (EMI) simulation, as described in [31], can be an example.

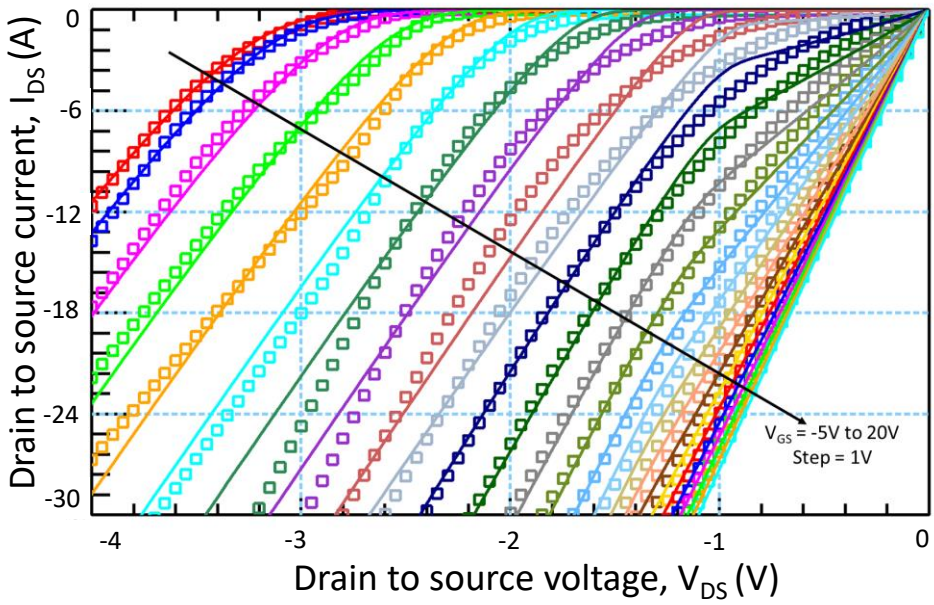


Fig. 3-5. Simulated with the presented model (solid line) and measured (symbols) third quadrant output characteristics of C2M0080120D.

In [8], the gate to source capacitance (*Cgs*) has been modeled with a constant value. This approach has been followed in most physics-based models due to negligible variation of *Cgs* with the drain to source voltage (*Vds*). For the datasheet-based modeling approach, this is the only way as most of the datasheets only provide the interelectrode capacitances' variation with *Vds*. However, as shown in Fig. 4-1, the measured data shows a significant variation of *Cgs* with gate voltage (*Vgs*) variation. This variation in *Cgs* is important in the case of SiC power MOSFETs, since from turn-off to turn-on, a significant gate voltage sweep is applied. To the best of author's knowledge, there is no physics based model for a SiC power MOSFET that includes gate dependent capacitance characteristics.

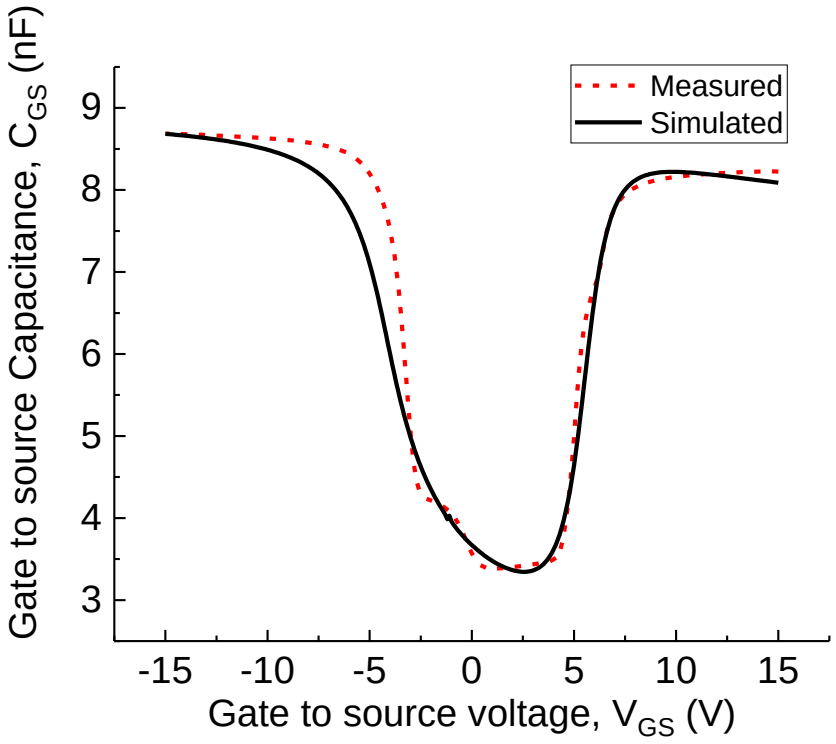


Fig. 4-1. Gate to source capacitance (*Cgs*) vs Gate to source voltage (*Vgs*).

*Cgs* mainly depends on the charge distribution in the channel region. There are three states of charge distribution in the channel region based on the *Vgs*. At the negative gate bias, the *p*-doped channel region shows the accumulation of positive charges. As a result, *Cgs* is equal to the intrinsic oxide capacitance (***Cox***). With the increasing positive gate voltage, the channel region enters into depletion. The depletion layer acts as an insulator, unlike the accumulated positive charge. This depletion layer grows thicker with the increasing positive voltage, and the *Cgs* decreases. However, the inversion charges at the surface again create the condition *Cgs* ≈ ***Cox*** at the advent of inversion.

The constant capacitance is modeled at the accumulation state using Eqs. (40) – (42). Here, ***Vdep*** is a model parameter that signifies the start of the depletion state. ***Cgsacc*** is another model parameter that is equal to the near-constant capacitance in the accumulation state.

$$Vgs_{acc} = \frac{1}{2}\left((Vgs + \boldsymbol{Vdep}) + \sqrt{(Vgs + \boldsymbol{Vdep})^2 + 4\boldsymbol{\delta}^2}\right) \tag{40}$$

$$Vgs_{acceff} = (Vgs + \boldsymbol{Vdep}) - Vgs_{acc} \tag{41}$$

$$Qgs_{acc} = \boldsymbol{Cgsacc} * Vgs_{feff} \tag{42}$$

$$Vgs_{dep} = \frac{1}{2}\left((Vgs - \boldsymbol{Vinv}) + \sqrt{(Vgs - \boldsymbol{Vtd})^2 + 4\boldsymbol{\delta}^2}\right) \tag{43}$$

$$Vgs_{depeff} = (Vgs - Vgs_f) + \frac{\boldsymbol{Gp}}{2}\left(-1 + \sqrt{1 - \frac{4Vgs_f}{\boldsymbol{Gp}}}\right) \tag{44}$$

$$Qgs_{dep} = \boldsymbol{Cgsinv} * Vgs_{reff} \tag{45}$$

The gradual decrease of the *Cgs* in the depletion state is modeled by Eqs. (43) – (45). This decrease continues until the inversion of the channel charge takes place. The inversion voltage is denoted by the parameter ***Vinv***, a different parameter than the threshold voltage of the static

characteristics to ease parameter extraction. ***Cgsinv*** is a parameter equal to the nearly constant capacitance at the inversion state.

The total channel charge distribution that leads to the gate to source capacitance is expressed as

$$Qgs = Qgs_{dep} + Qgs_{acc} \qquad (46)$$

The Miller capacitance (*Crss*) is a depletion capacitance caused by the gate electrode's overlap on the drain region. Since the capacitance is between the input and the device's output terminals, it plays a negative feedback role, slowing down the gate voltage's transition rate [20]. In [20], it was shown that the traditional SPICE models have about 50% error in predicting the Miller capacitance at the low gate voltage region. Fig. 4-2 shows the simulation results of the model of [8]. It has a maximum error of 72% and an overall RMS error of 15% with the measured results. The reason behind this mismatch is the approximation that there is only one continuous depletion region. For more accurate modeling of the Miller capacitance, [20] adopted a concept called segmented-cascaded depletion regions. In this work, the concept is implemented in a different fashion. *Cdg* is formed with a series combination of oxide capacitance and the drift region depletion capacitance. The oxide capacitance (***Cox***) is a fixed component, and the depletion capacitance varies with the *Vdg* bias.

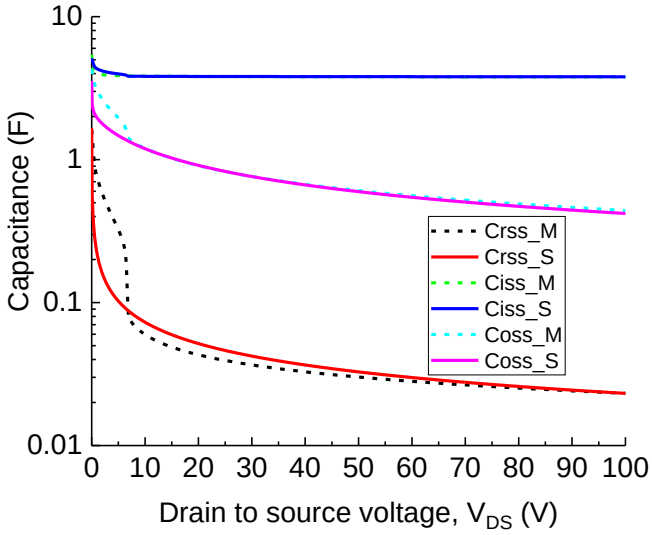


Fig. 4-2. Simulated C-V characteristics of the model [8] and its large mismatch with the measured results at low voltage region.

In advanced SiC MOSFET device structures [32], [33], the JFET and following drift region have different doping concentrations and thicknesses. So, there exist multiple layers of depletion regions. Each depletion region sees the previous depletion region as a fixed capacitance and then varies with the applied *Vdg* bias. It requires modeling multiple depletion capacitances with their own doping concentrations and overlap areas to capture the effect adequately. Information of these regions is rarely available to circuit designers. Instead of multiple doping concentrations and overlap areas, the effect can be accurately modeled with a different initial capacitance ($\boldsymbol{Cox_i}$). Hence, the Miller capacitance, *Cgd* can be accurately expressed with Eqs. (47) – (54):

$$\sum_{i=0}^{k} Qgd_i = Qgd_{ni} + Qgd_{pi} \tag{47}$$

$$Qgd_{ni} = Vdgeff_{ni} \cdot \boldsymbol{Cox_i} \tag{48}$$

$$Qgd_{pi} = Vdgeff_{pi} \cdot Cgd_{ji} \tag{49}$$

$$C_{gd_{ji}} = \frac{\boldsymbol{Cox_i} \cdot Cgd_i}{\boldsymbol{Cox_i} + Cgd_i} \tag{50}$$

$$Cgd_i = \varepsilon_{sic} \cdot \frac{\boldsymbol{agd}}{wgd_i} \tag{51}$$

$$wgd_i = \sqrt{2 \cdot \varepsilon_{sic} \cdot \frac{Vdgeff_{pi}}{q \cdot nb}} \tag{52}$$

$$Vdgeff_{pi} = \frac{1}{2}\left((Vdg - \boldsymbol{vtd_i}) + \sqrt{(Vdg - \boldsymbol{vtd_i})^2 + 4\boldsymbol{\partial}^2}\right) \tag{53}$$

$$Vdgeff_{ni} = (Vdg - \boldsymbol{vtd_i}) - Vdgeff_{pi} \tag{54}$$

For $\boldsymbol{i} = 0$, ***Cox*** signifies the gate oxide capacitance. For the later cascaded structures, $\boldsymbol{Cox_i}$ depicts the fixed minimum capacitance of the previous cascaded capacitor, at the transition voltage parameter ($\boldsymbol{vtd_i}$). Usually, only two cascaded capacitor structures are enough to accurately fit the measured *Cgd* characteristics. $Qgd_i$ depicts the total charge associated with Miller capacitance of one of the capacitors of the total cascaded structure. $Qgd_{ni}$, $Qgd_{pi}$, $Vdgeff_{ni}$, and $Vdgeff_{pi}$ are temporary terms used for making the expression continuous instead of using piecewise conditional statements. $wgd_i$ stands for the depletion width associated with each cascaded structure. With large enough applied *Vdg*, the depletion region reaches the N+ substrates. From there on, the depletion width does not change much before breakdown. The *Cdg* takes a minimum value fixed by the parameter ***Cdgmin***. The simulated C-V characteristics of the presented model compared with the measured results are shown in Fig. 4-3. The presented model's simulated *Crss* show less than 10% maximum error and less than 2% RMS error with the measured results.

The cascaded depletion regions also affects the drain to source capacitance (*Cds*) and ultimately the output capacitance (*Coss*). Instead of one depletion capacitance, the total *Cds* is a combination

of *i* number of depletion capacitances. Each depletion capacitance is expressed with the following equations.

$$\sum_{i=0}^{k} QdS = Qds_{ni} + Qds_{pi} \tag{55}$$

$$Qds_{ni} = \boldsymbol{cds_i} \cdot V_{bdiodefn} \tag{56}$$

$$Qds_p = \boldsymbol{cds_i} \cdot Vbi^m \cdot \frac{(Vbi+V_{bdiodefpi})^{\boldsymbol{1-m}} - Vbi^{\boldsymbol{m}}}{\boldsymbol{1-m}} \tag{57}$$

$$Vbi = \frac{kT}{e} \ln(\frac{\boldsymbol{nb} \cdot 10^{16}}{n_i^2}) \tag{58}$$

$$V_{bdiodefpi} = \frac{1}{2}((Vbdiode - \boldsymbol{vtdi}) + \sqrt{(Vbdiode - \boldsymbol{vtdi})^2 + 4\boldsymbol{\partial}^2}) \tag{59}$$

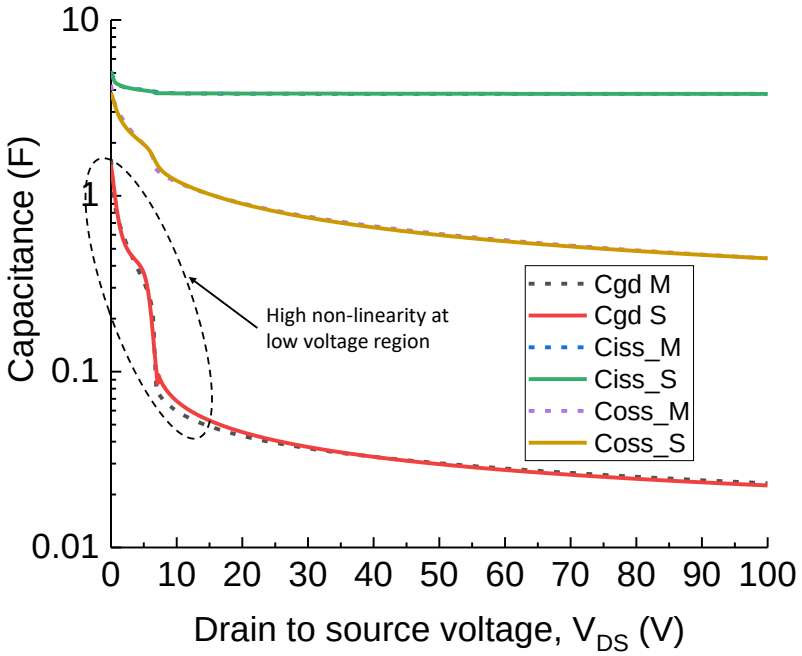


Fig. 4-3. Comparison of the presented model's simulated C-V characteristics with the measured results.

Table 4-1 lists the parameters used for the C-V modeling.

**Table 4-1.Parameters for Capacitance Modeling**

| Notation | Definition |
|---|---|
| ***cgsacc*** | Gate to source capacitance *at the accumulation state* |
| ***cgsinv*** | Gate to source capacitance *at the onset of inversion state* |
| ***vacc*** | Accumulation state onset voltage |
| ***vinv*** | Inversion state onset voltage |
| ***Gp*** | Doping gradient at the channel region |
| ***vtd0*** | First gate drain overlap depletion threshold voltage |
| ***vtd1*** | Second gate drain overlap depletion threshold voltage |
| ***Cox0*** | Gate oxide capacitance |
| ***Cox1*** | Initial constant capacitance at the onset of second depletion region |
| ***Cgdmin*** | Constant capacitance at the high voltage region |
| ***m*** | Junction grading coefficient |
| ***nb*** | Drift region doping concentration |
| ***wb*** | Metallurgical drift region width |
| ***a*** | Device active area |
| ***agd*** | Gate length overlap active area |

# Chapter 5. MODELING TEMPERATURE DEPENDENCY

The device characteristics of the SiC power MOSFET heavily depend on the junction temperature. The junction temperature however, depends on the power dissipated by the device itself. To create a self-heating model, it is mandatory to make the temperature a variable to include this simultaneous effect. Apart from the terminal voltages, temperature becomes another input variable, and the output currents become a function of temperature. This dependency is incorporated by making the model parameters a function of temperature. Since the temperature dependencies depend on multiple factors, it is extremely difficult to make accurate physics-based expressions with good convergence properties. Instead, empirical equations are used to capture these physics-based phenomena for efficient implementation in SPICE-like simulators.

## 5.1. **Temperature scaling of the first quadrant behavior**

The first quadrant model has been modified from [7] and [8]. The temperature dependencies of these models are sufficient for isothermal simulations at the rated temperature range. However, self-heating included electro-thermal simulations using these models often cause convergence issues. This is due to the lack of a feedback mechanism in the temperature dependencies, which is apparent in practical cases. This work modifies the temperature dependencies of the critical parameters for well converged electro-thermal simulations.

The most prominent effect of temperature is seen in the threshold voltage shift. With increasing temperature, the threshold voltage decreases in SiC power MOSFETs. This decrease is due to the increase in the thermal generation of minority carriers in the channel region. Previous models like [7], [8], and [9] used linear relations to include this characteristic. However, such formulations cause non-convergence in electro-thermal simulations as the threshold voltage might become

negative during the iterative simulation process. Measured results also contradict this approximation of linear decrease. The article in [34] shows experimental data proving that at higher temperatures (>200°C) the threshold voltage decreases at a much lower rate than comparatively lower temperatures. A linear decreasing relation will not be able to predict the correct behavior in electro-thermal simulations. The non-linearity of the threshold voltage decrease with increasing temperature is shown in Fig 5-1.

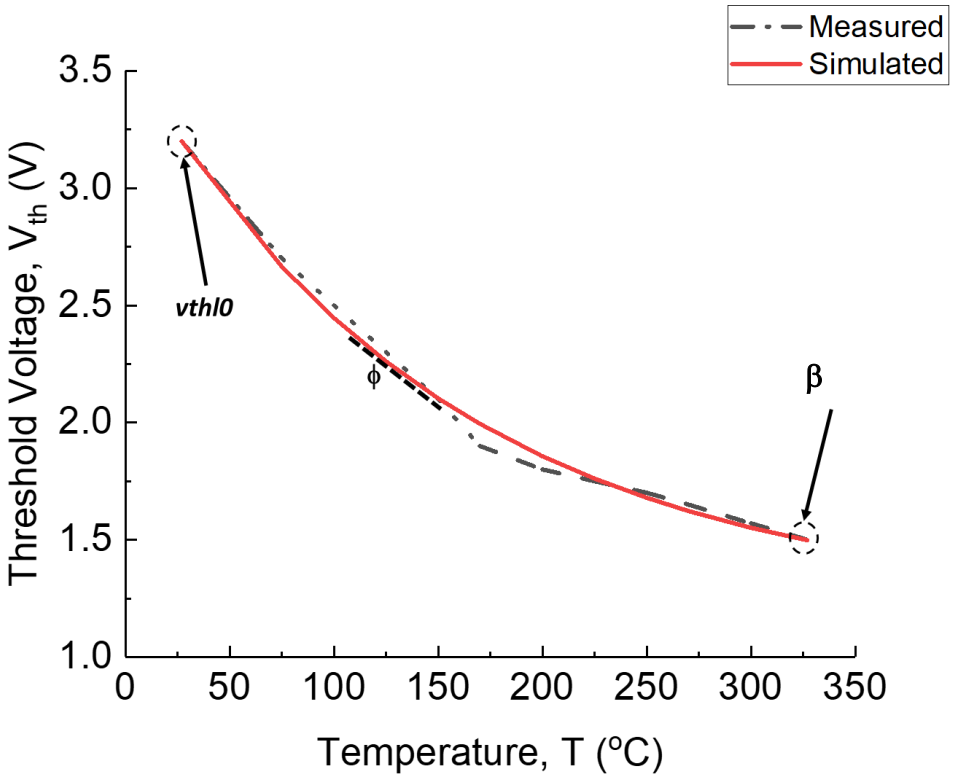


Fig. 5-1. Threshold voltage variation with temperature in SiC power MOSFETs and the related parameter extraction.

This non-linearity is modeled with Eq. (60) modifying the method described in [15]. In [15], the effect of the interface charges at high temperatures is included through the mobility equation. However, as described earlier, the interface charge's effect is included in the developed model by separate threshold voltages ($vth_l\_t$, $vth_h\_t$) for low and high gate voltage regions, respectively.

$$Vth_x\_t = \left[ (\boldsymbol{Vth0_x} - \boldsymbol{\beta_x}) \cdot e^{-\boldsymbol{\varphi_x}(tempdiff)} \right] + \boldsymbol{\beta_x} \quad (60)$$

$$tempdiff = temperature - \boldsymbol{tnom} \quad (61)$$

Here $\boldsymbol{Vth0_x}$ stands for the threshold voltage at room temperature. $\boldsymbol{\beta_x}$ stands for the minimum threshold voltage at the higher temperatures (>300°C). The measured threshold voltage at the maximum temperature can be assigned as its value. $\boldsymbol{\varphi_x}$ is a fitting parameter.

The temperature dependence of the transconductance largely depends on the mobility. Two different transconductance parameters ($k_{px}\_t$, $k_{fx}\_t$) are used for the linear and saturation region, respectively, to develop this model, as described earlier. The parameter $k_{px}\_t$ is extracted from the saturation region of the drain current. For the low gate voltage region, the saturation current increases with the increasing temperature. It means the transconductance parameter ($kp_l\_t$) increases. For the high voltage region, the saturation current decreases with the higher temperature i.e., $kp_h\_t$ decreases. The reason behind these opposite trends is the presence of two mobility controlling mechanisms [15]. The first mechanism is carrier scattering due to the presence of filled interface states. At the low gate voltage region, this scattering controls the mobility of the channel. With the increasing temperature, the interface states are less likely to be filled, and so, the scattering mechanism drops. Increased mobility increases the low gate voltage transconductance. However, the trend is not linear as it saturates at some higher temperatures. The temperature dependency of the transconductance at the low gate voltage region can be expressed with Eq. (62). Fig. 5-2 shows the extracted $kpl_f$ values at different isothermal measurements. The simulated results show the fit of the temperature scaled model.

$$kpl_f\_t = \boldsymbol{kpl0_f} \cdot \boldsymbol{mklp_f} \cdot (1 - e^{-\boldsymbol{al_f} \cdot tratio}) \quad (62)$$

$$tratio = \frac{temperature}{\boldsymbol{tnom}} \tag{63}$$

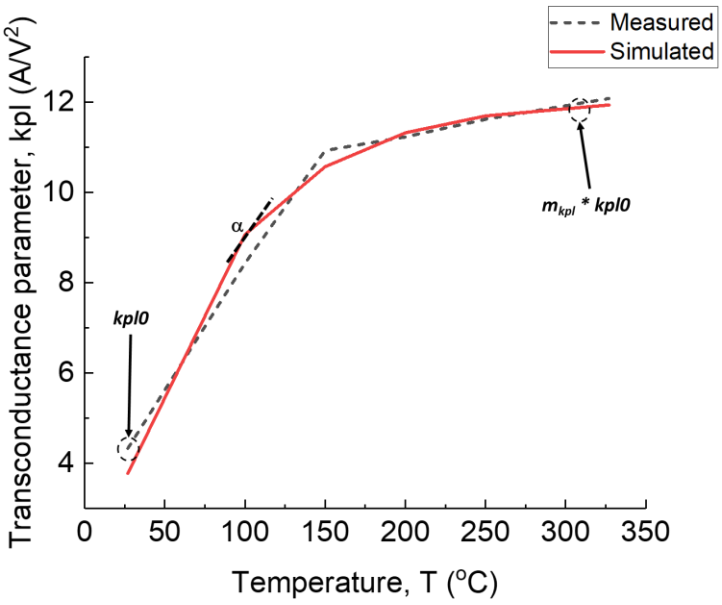


Fig. 5-2. $kpl_f\_t$ variation with temperature in SiC power MOSFET and related parameters extraction.

In the high gate voltage region, the effect of interface charge is less even at room temperature. The controlling mechanism for mobility is lattice scattering. This scattering increases with the increasing temperature. So the transconductance at the high gate voltage region decreases as the temperature increases. Even in this case, a weak saturation can be noticed. This trend can be incorporated into the model using Eq. (65).

$$kph_f\_t = \boldsymbol{kph0_f} \cdot tratio^{-\boldsymbol{\alpha h_f}} \tag{64}$$

**Table 5-1. Temperature Scaling Parameters for the First Quadrant Characteristics**

| Notation | Definition |
|---|---|
| $\boldsymbol{\beta}$ | Minimum threshold voltage at the high temperature |
| $\boldsymbol{\varphi}$ | Slope adjusting parameter for the temperature-dependent threshold voltage |
| ***mklp*** | Adjustment multiplier for high-temperature transconductance |
| $\boldsymbol{\alpha l}$ | Slope adjusting parameter for *kpl* |
| $\boldsymbol{\alpha h}$ | Slope adjusting parameter for *kph* |
| $\boldsymbol{rdtemp_f}$ | Temperature coefficient of the drain resistance |
| $\boldsymbol{rstemp_f}$ | Temperature coefficient of the source resistance |
| $\boldsymbol{\theta ltemp_y}$ | Temperature coefficient of the transverse electric field parameter |

The on-resistance ($Rds_{on}$) varies with temperature. The drift region resistance determines the major part of the $Rds_{on}$ at high current. With increasing lattice scattering at high temperatures, the drift region resistance increases. Moreover, the source terminal's constant resistance also increases due to increasing scattering at the heavily doped areas. As can be seen from Fig. 5-3, the drain resistance shows an exponential rise with increasing temperature. It can be expressed with Eq. (65).

$$rd_{y\_}t = \boldsymbol{rd0_y} \cdot e^{\boldsymbol{rdtemp} * tratio} \tag{65}$$

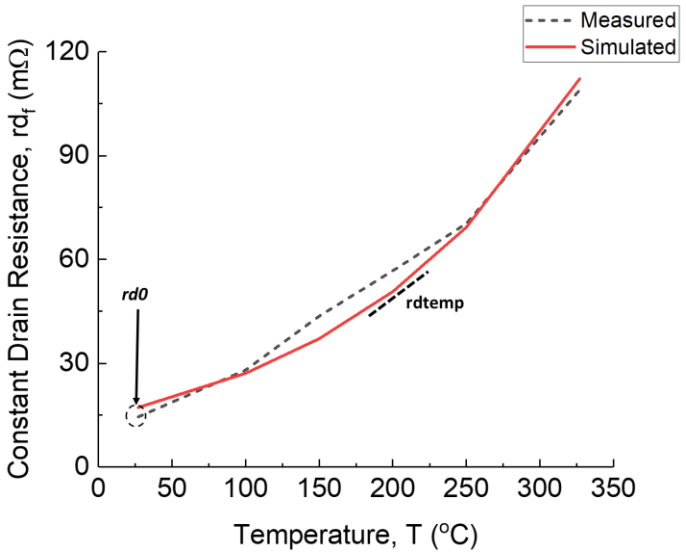


Fig. 5-3. $\boldsymbol{rd_f}$ variation with temperature in SiC power MOSFET and related parameters extraction.

The increase of the source terminal resistance is more gradual and can be expressed with the logarithmic expression of Eq. (66). Fig. 5-4 shows the fit source resistance variation in isothermal and temperature scaled simulation with Eq. (66).

$$rs_y\_t = \boldsymbol{rs0_y} + \boldsymbol{rstemp} \cdot \ln(tratio) \tag{66}$$

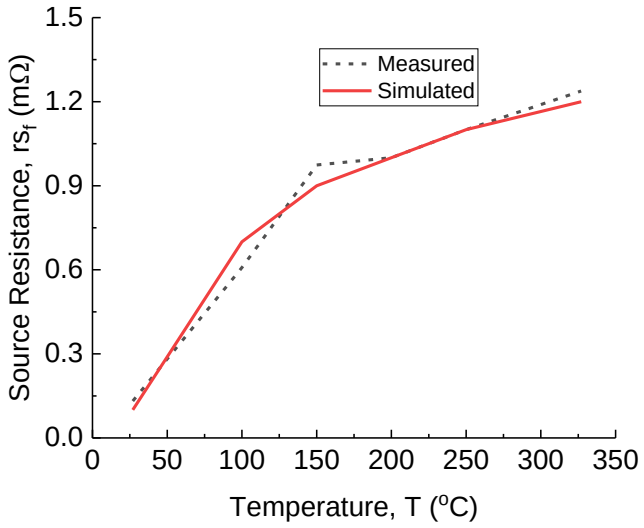


Fig. 5-4. $\boldsymbol{rs_f}$ variation with temperature in SiC power MOSFET and related parameters extraction.

Transverse electric field parameters increase with the temperature rise. Increased empty interface states cause this increase in the vertical electric field at a higher temperature. Less empty space enables the vertical electric field to strongly effect the channel charges. This temperature dependence can be modeled with Eq. (67).

$$\theta l_{f}\_t = \boldsymbol{\theta l0_f} + \boldsymbol{\theta ltemp_f} \cdot \ln(tratio) \tag{67}$$

The breakdown voltage ($V_{Br}\_t$) of SiC power MOSFET increases with temperature [35] as shown in Fig. 5-5. This increase is very linear and can be modeled with Eq. (69).

$$V_{Br}\_t = \boldsymbol{V_{Br0}} + \boldsymbol{VbrTemp} \cdot (tdiff) \tag{68}$$

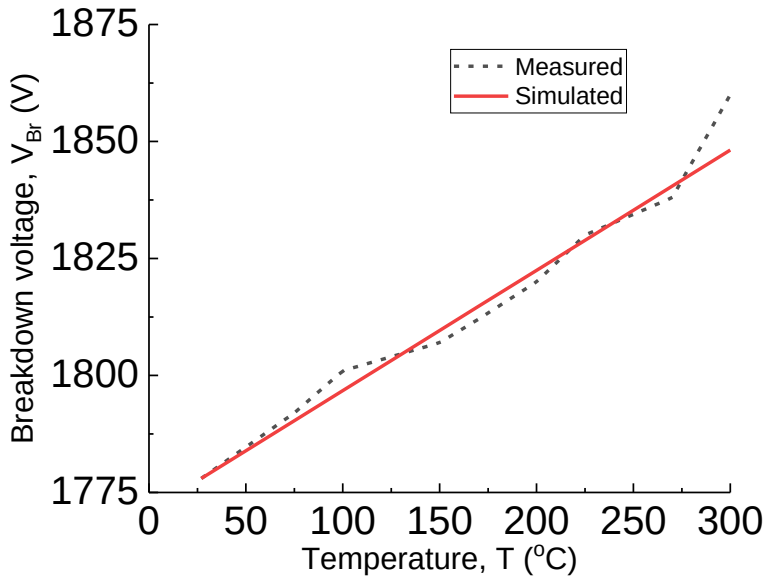


Fig. 5-5. Breakdown Voltage ($V_{Br}$) variation with temperature.

5.2. **Third quadrant temperature dependency modeling**

In the third-quadrant operation, i.e., ($Vds$ < 0) and ($Ids$ < 0), there are two paths for the current flow. First, the current can flow through the inversion channel as in MOS operation. Second, the current can flow through the body diode formed between the body and the drift region. The first mechanism dominates for gate voltage higher than the threshold voltage and the drain voltage less

than the forward drop of the *p-n* junction. As described earlier, the threshold voltage, transconductance, and on-resistance parameters of this MOS channel are different from the first quadrant operation and need different parameters for accurate modeling. Though the parameters are different for the forward and reverse conduction of the MOSFET, the reverse characteristic parameters' temperature dependences are the same as their first quadrant counterpart. So the temperature dependency of the third-quadrant MOS current related parameters can be expressed with the same equations as their first quadrant counterpart. However, the values of the temperature coefficients are different.

In the case of body diode conduction, diode resistance and conductivity modulation are both affected by temperature. Due to increasing lattice scattering with increasing temperature, the diode resistance increases. This can be seen in Fig. 5-6. This increase of the body diode's resistance is logarithmic and is modeled with Eq. (69).

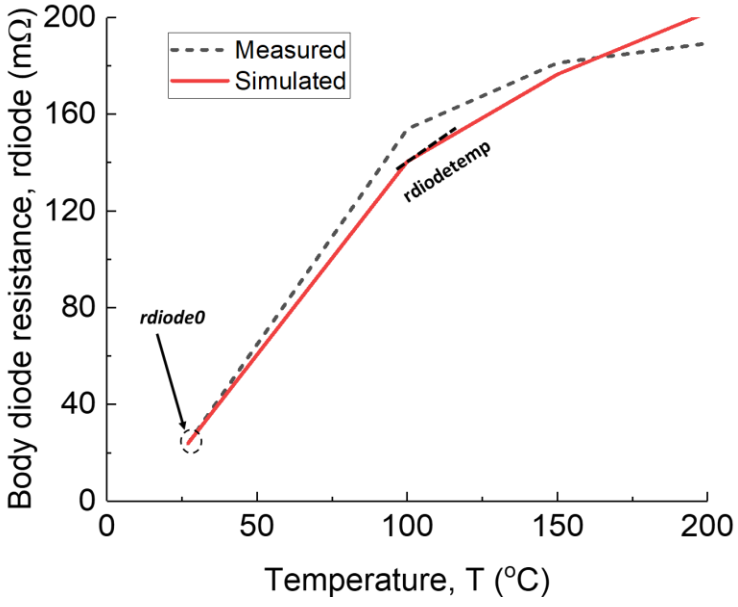


Fig. 5-6. Logarithmic variation of diode resistance with increasing temperature.

$$rdiode0\_t = \boldsymbol{rdiode0} + \boldsymbol{rdiodtemp} \cdot \ln(tratio) \tag{69}$$

Conductivity modulation in the power MOSFET's drift region increases with temperature due to increased minority carrier lifetime. It means that the decrease in resistance of the diode conduction part is more prominent than at room temperature. Hence, the conductivity modulation parameter *rdiovgs_t* becomes larger. The temperature dependence of *rdiovgs_t* is modeled with Eq. (70).

$$rdiovgs\_t = \boldsymbol{rdiovgs0} \cdot (tratio)^{\boldsymbol{rdiovgstemp}} \tag{70}$$

The forward voltage drop of the body diode at *Vgs* = ***vk1*** decreases with the increase in temperature. This decrease is related to the increase in intrinsic carrier concentration at higher temperatures. The decrease can be more stably modeled with an exponential function instead of a linear relation for better convergence. Eq. (71) shows the temperature dependence modeling of *ND_t*. Fig. 5-7 shows the fit of simulated and the extracted values of *ND_t* at different temperatures.

$$ND\_t = \boldsymbol{ND} \cdot \boldsymbol{ND_{TEMPCO1}} \cdot e^{-\boldsymbol{ND_{TEMPCO2}} \cdot tratio} \tag{71}$$

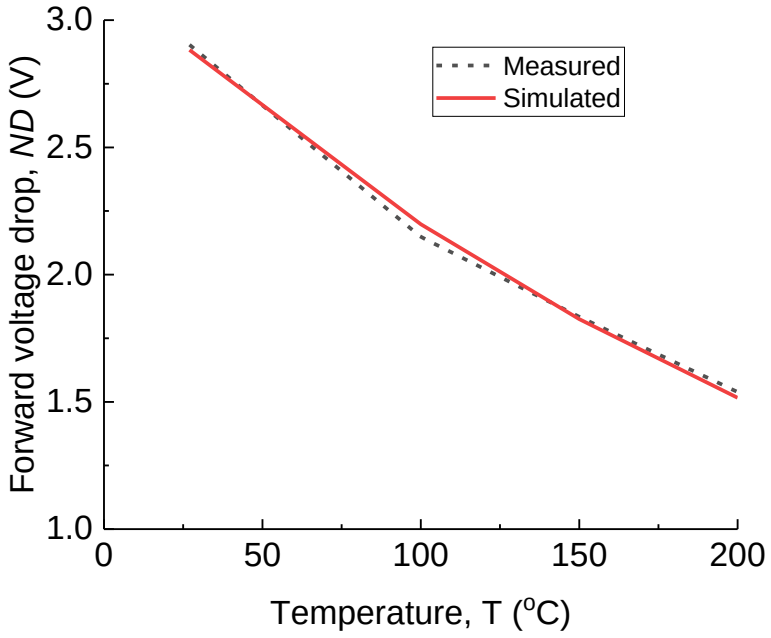


Fig. 5-7. Body diode's forward voltage drop variation with temperature.

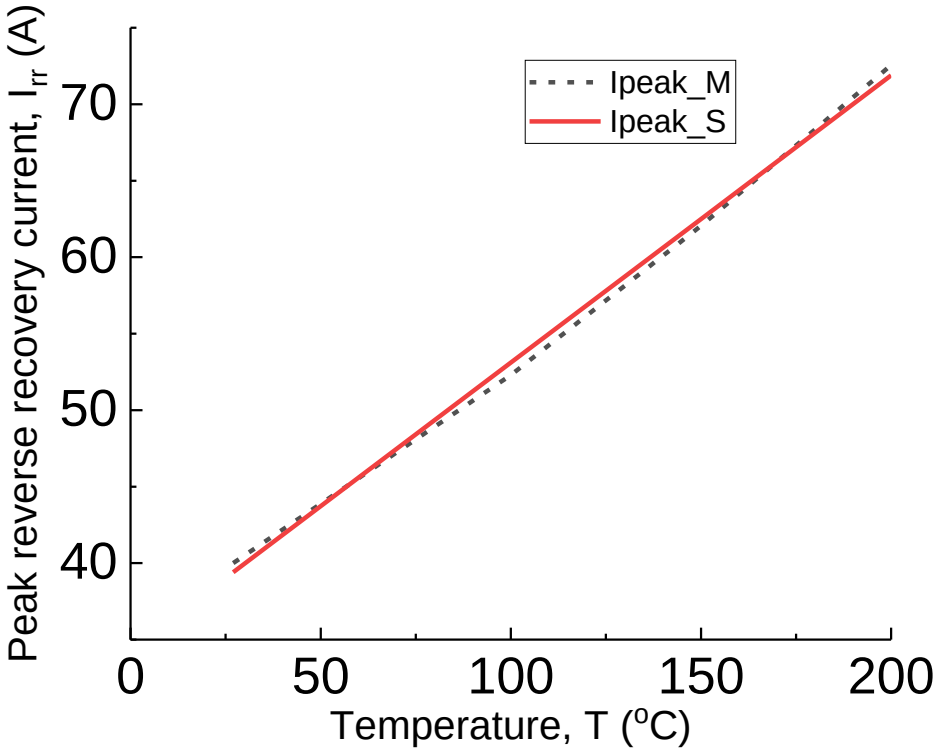


Fig. 5-8. Peak reverse recovery current ($I_{rr}$) variation with temperature.

Increasing temperature increases the carrier lifetime [36]. As a result, total reverse recovery time and peak reverse recovery current both increase. Fig. 5-8 shows the variation of peak reverse

recovery current with temperature. So a temperature dependency of the carrier lifetime parameter (τ) with Eq. (72) can accurately model the temperature scaling of revere recovery.

$$tau\_t = \boldsymbol{tau0} \cdot tratio^{\boldsymbol{tauTEMP}} \tag{72}$$

### 5.3.**Thermal model validation**

The developed model with a properly extracted parameter set can fit the output characteristics for a wider range of temperatures.

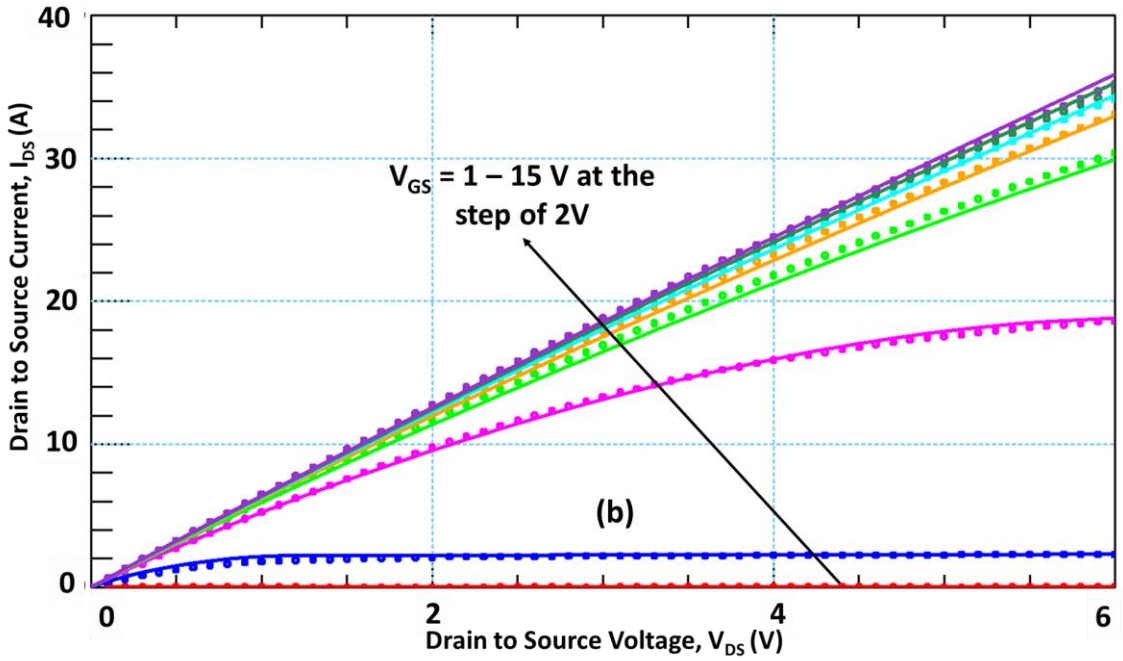


Fig. 5-9. Measured and simulated output characteristics at 327°C.

The transfer curves at different temperatures also verify the model's capability to fit the variation of threshold voltages at different temperatures. This is very important because it will determine the current sharing condition in a multiple device arrangement. Proper modeling of the threshold variation within different devices in a parallel combination and their temperature dependence will enable designers to design more reliable systems.

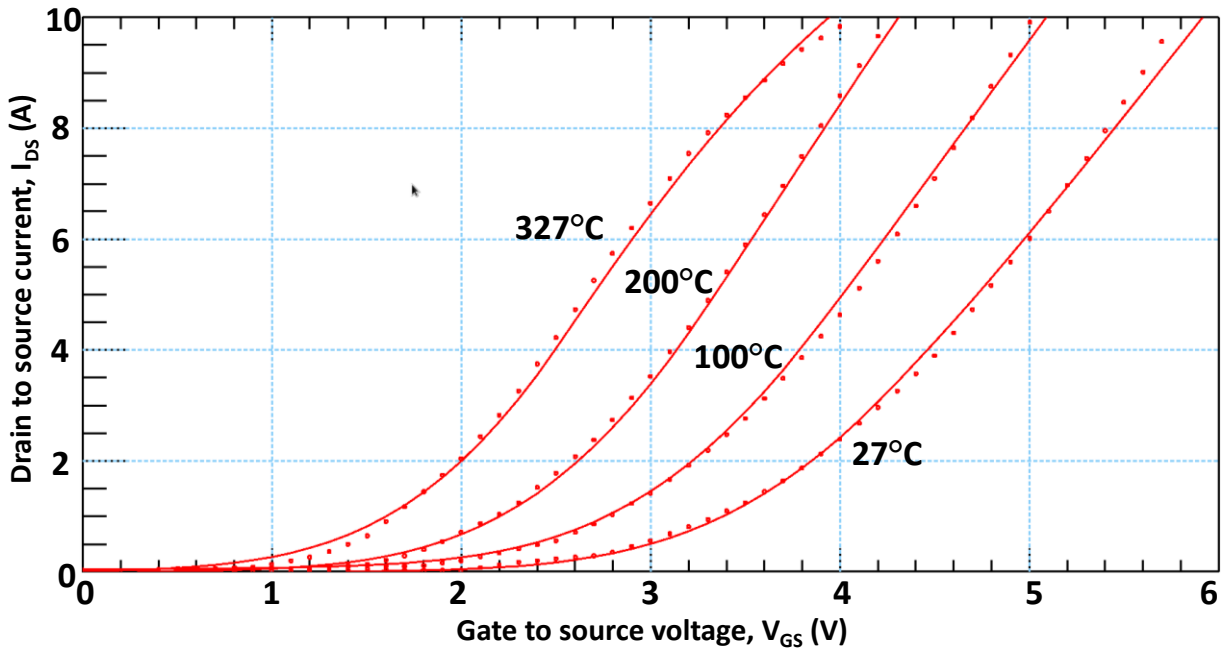


Fig. 5-10. Transfer curves of C2M0045170D at different temperatures for *Vds* = 2V.

The third quadrant output characteristics at different temperatures are shown below. The developed model can accurately fit the characteristics from room temperature to 327°C. At room temperature, the conductivity modulation is not that severe. But for higher temperatures, the effect is very prominent. According to the author's knowledge, no other existing model has shown the simulated result at this high temperature. Fig. 5-11 shows the third quadrant output characteristics at 200°C with significant conductivity modulation. The developed model can accurately simulate the output characteristics at different gate voltages. Fig. 5-12 shows the stability of temperature scaling of the developed model. The model can simulate the self-heating phenomena as evident of the lowering of the current in the output characteristics in the high *Vds* region.

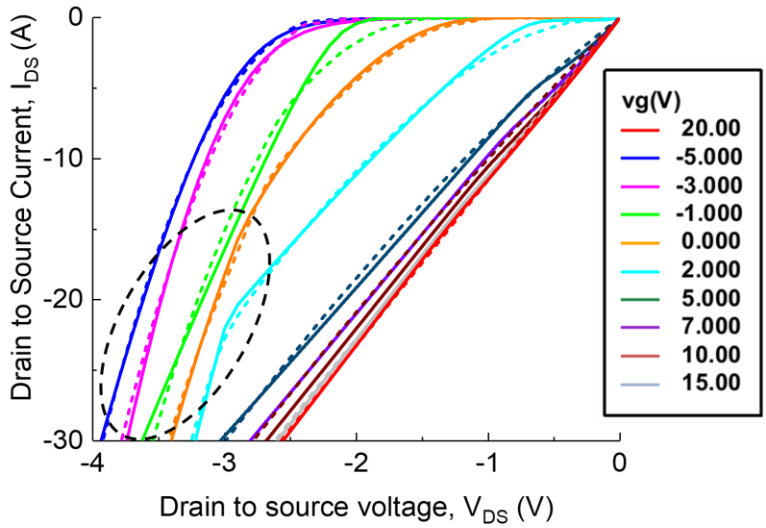


Fig. 5-11. Third quadrant output characteristics at 200°C.

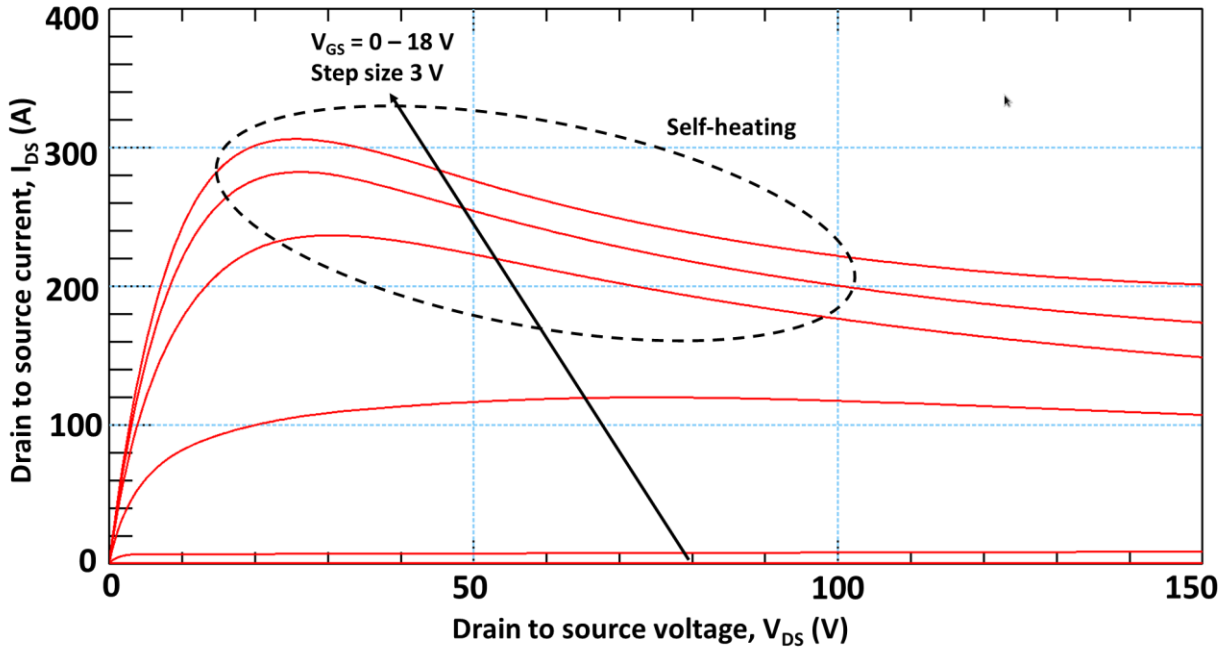


Fig. 5-12. Output characteristics with self-heating included.

# Chapter 6. DOUBLE PULSE TESTS (DPT) AT DIFFERENT TEMPERATURES

The double pulse test (DPT) is the most widely used method for transient characterization of the semiconductor switches in power electronics. The switching losses and the parasitic parameters related to any particular design can be extracted from the double pulse test results. Usually, a half-bridge configuration of two devices is used for DPT. There are two pulses in DPT, as the name suggests. The first gate pulse is longer, and it charges up the load inductor to the desired current level. The turn-off switching characteristic at the desired current level is measured at the end of this pulse. A freewheeling diode (FWD) is required to give the inductor current a conduction path when the device under test (DUT) is in the off-state. The half-bridge configuration's low side device is used as the DUT, while an anti-parallel diode of the high side device is used as the freewheeling diode. For power MOSFETs, the intrinsic body diode can be used as the anti-parallel freewheeling diode required for DPT. The second pulse is shorter so that the load current does not increase too much. This pulse is necessary for turn-on switching characterization at the desired current level. Parasitics from the board and the measurement probes affect the DPT results. So necessary care has to be taken for accurate analysis.

## 6.1. **Hardware realization**

A commercially available half-bridge evaluation board (KIT8020CRD8FF1217P) [37] from Wolfspeed is used for this characterization. The board is rated for up to 1000 V switching characterization and suitable for standard TO-247 packages. The board can be easily configured for several topologies from the basic phase-leg configuration. The general block diagram of the board can be seen in Fig. 6-1.


Fig. 6-1. KIT8020CRD8FF1217P half-bridge evaluation board [37].

Mornsun G1212S-2W isolated DC/DC converters are used for high side and low side isolated power. This DC/DC converter turns a +12 V input Vcc to -5V/19V output Vcc for the push-pull gate drive's secondary side. Though a SiC MOSFET can be turned-off at 0 V, a negative turn-off gate voltage prevents high *dv/dt* induced turn-on and increase noise immunity in addition to faster turn-off. Avago ACPL-W346 2.5A gate drivers are used in the board. A signal generator generated the necessary PWM signal with high resolution to drive the devices.

The board provides excellent access to the measurement points. BNC connectors are provided for the measurements of both high and low sides *Vgs* and *Vds*. The board PCB layout ensured that the low side *Vgs* and *Vds* had same ground. A ground-referenced probe is used for measuring low side *Vds*. The use of differential probes causes loop inductance at the measurement point. Therefore, a Tektronix TPP0850 probe was used for the *Vds* measurement. It has a very high voltage rating of

2.5 kV and a bandwidth of 800 MHz. Low side gate voltage was measured using a voltage probe with 10x attenuation.

Two very common methods of measuring current in power electronics circuits are 1. Current Viewing Resistor (CVR) and 2. Rogowski coil (RC). RC is a very convenient choice because it can be easily added to a circuit, and it is non-invasive. But RC suffers from bandwidth limitation. CVR, being just a resistor, has very high bandwidth. In high *dv/dt* switching of the SiC devices, this bandwidth is necessary for accurately capturing the overshoot magnitude and ringing oscillation frequency. Nevertheless, CVR is a physical passive that adds additional inductance and resistance to the power loop. Moreover, in continuous tests like the Buck Converter test, passives in the circuit heat up. In such cases, the accuracy of the measurements with CVR are not reliable as the value of the resistance changes with temperature. Fig. 6-2 shows the limitations of low bandwidth Rogowski coil compared to CVR in measuring high bandwidth oscillation.

The KIT8020CRD8FF1217P evaluation board provides two unpopulated through-hole contacts for CVR attachment. This CVR can be used for measuring the current through the low side device. However, the evaluation board with the same set-up will also be used for converter study. In such a case, it will be necessary to remove the CVR. So instead, a short loop was created using a copper wire in those test points. A high bandwidth (>120 MHz) AC/DC current probe TCP0030A from Tektronix has been used for taking the measurements. From the rough calculation it was seen that the oscillation frequency will be close to 70 MHz. So this current probe is enough for accurate measurement.

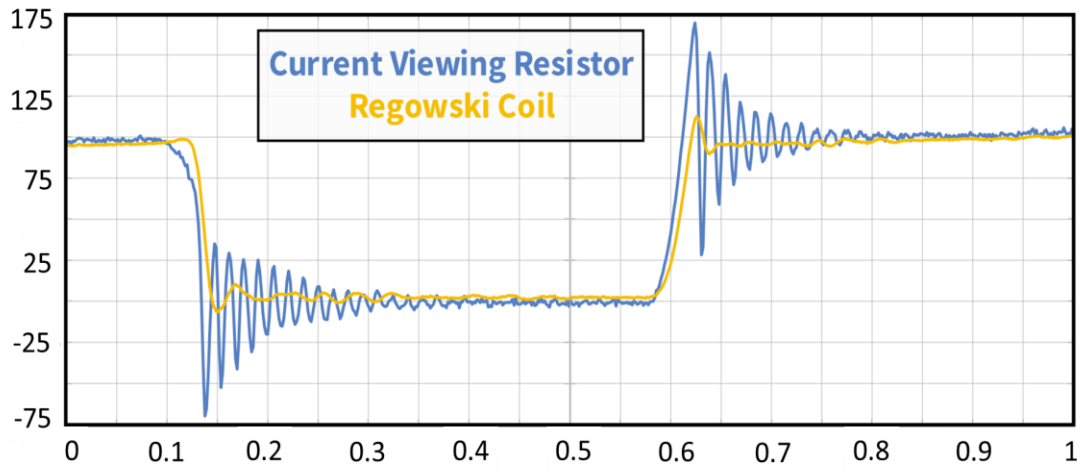


Fig. 6-2. Comparison of CVR and Rogowski Coil measured results (courtesy [38]).

For recording switching waveforms, a six-channel 05 series MSO Tektronix oscilloscope of 6.25 GS/s sampling rate and 2 GHz bandwidth oscilloscope has been used. The maximum switching voltage was 1000 V and was provided by Magan-power's 2 kV DC power supply. A 320 μH inductor was used as the clamped inductive load. The SiC devices are mounted on the board's backside and are attached to the hot plate with Kapton tape. A safety box surrounded the DPT board and the hotplate. A thermocouple was used for measuring and controlling the temperature of the device's cooling plate. Since the pulse durations are small, self-heating can be neglected for DPT. Hence the measurements can be termed isothermal measurements at the temperature set at the hotplate. Due to the limitations of the DPT board, tests were performed only up to 200°C. Fig. 6-3 shows the overall test set-up.

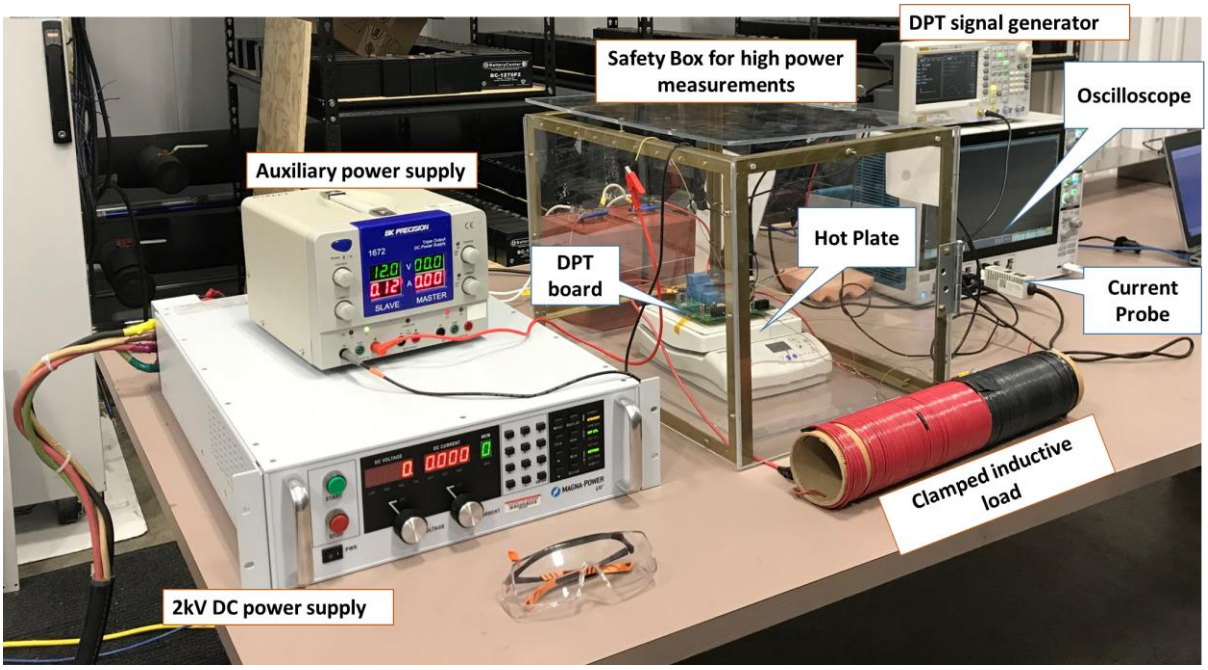


Fig. 6-3. Double Pulse Test set up.

## 6.2. **Results and analysis**

The turn-on and turn-off characteristics of a commercially available Wolfspeed C2M0045170D is tested at different voltages and currents over temperature in the double pulse test circuit. The maximum limits of the test are listed in Table 6-1.

**Table 6-1. Maximum Limits of the Double Pulse Tests' Variables**

| Variable | Maximum value |
|---|---|
| Maximum DC voltage | 1000 V |
| Maximum switching current | 30 A |
| Maximum junction temperature | 200°C |

The measured data is compared with the simulated results of the developed model. A simplified circuit schematic of the overall test set-up shown in Fig. 6-4 is used for the simulation. Parasitics of the test board are extracted using Q3D. The high-side device's body diode is working as a freewheeling diode. It is connected in parallel with the load inductor. The hand-made air-core

inductor is represented by a parallel-connected LCR model from the measured impedance data. The gate driver is simplified using a pulse voltage source, external gate resistance, and parasitic gate loop inductance. Internal gate resistances are measured using the Keysight B1505A. Package inductances are lumped with the external inductances to form the drain, source, and gate terminal inductances for top and low side devices.

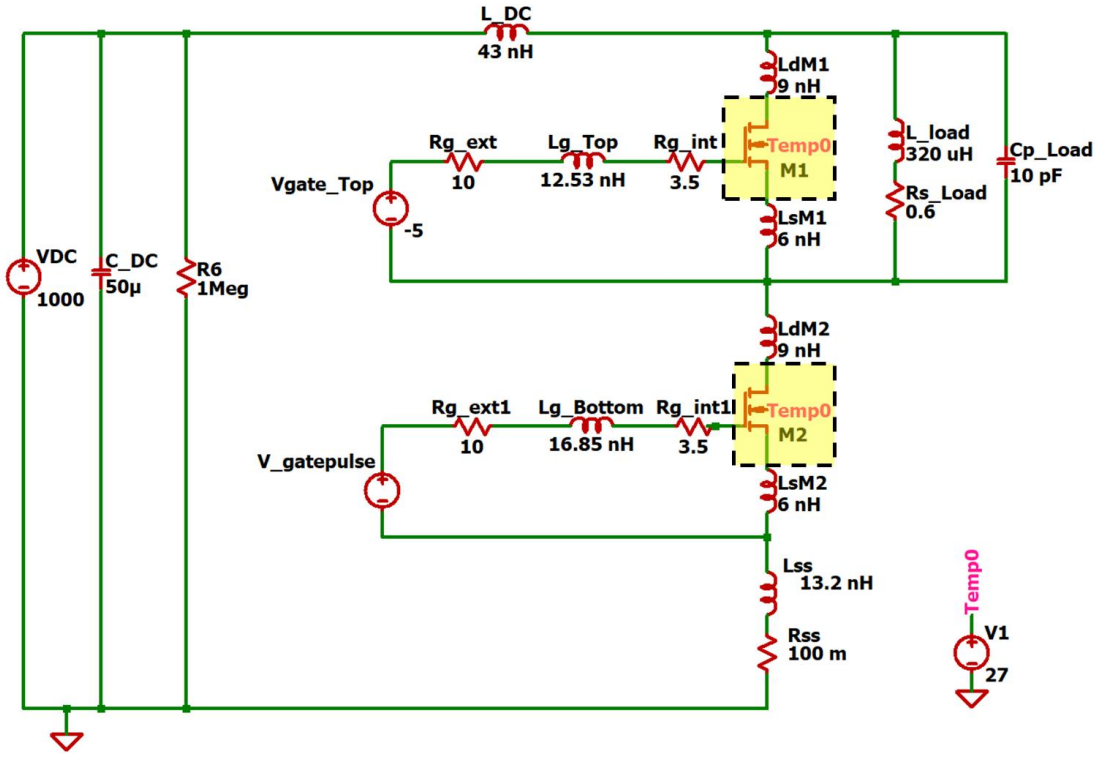


Fig. 6-4. Schematic of the double-pulse test bench for model verification.

Figs. 6-5 to 6-7 show the DPT results at room temperature. In Fig. 6-5 both the turn-on and turn-off gate voltage characteristics fit very closely with the measured results. Even the large negative spike at the beginning of the turn-on matches perfectly. This is because the reverse recovery is accurately modeled with the measured data instead of the datasheet information. The current of the body diode channels itself to the MOSFET during MOSFET's turn-on. The MOSFET's *Vgs* drops to adjust the *Ids* for a particular *Vds*. The frequency of the gate voltage oscillation also

matches, validating the updated model of *Ciss*. The *Vgs* curve for the turn-off switching also shows a close match.

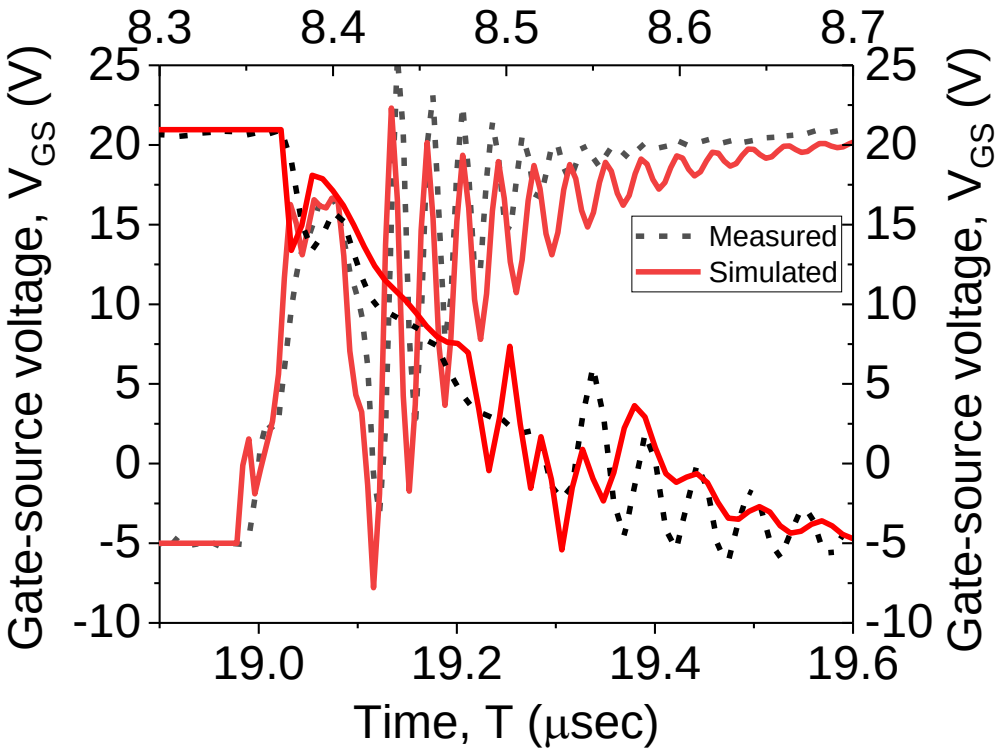


Fig. 6-5. Turn-on and Turn-off transient of the gate voltage at room temperature

Fig. 6-6 is the turn-on output characteristics. With the updated C-V models for accurate output capacitance for the high *Vds* region, the simulated results accurately fit the measured results. The kink at the beginning of the *Vds* drop is directly related to *Coss* dissipation, and it has been correctly modeled. The peak overshoot current during turn-on depends on the *Coss* dissipation as well as on the reverse recovery current of the body diode. With accurate modeling of these two features, the peak overshoot current's magnitude has been properly predicted. Accurate modeling of the *Coss* is also evident from the close match of the *Vds* and *Ids* curves' oscillation frequency. A little mismatch can be attributed to the probe capacitances that were not incorporated into the simulation.

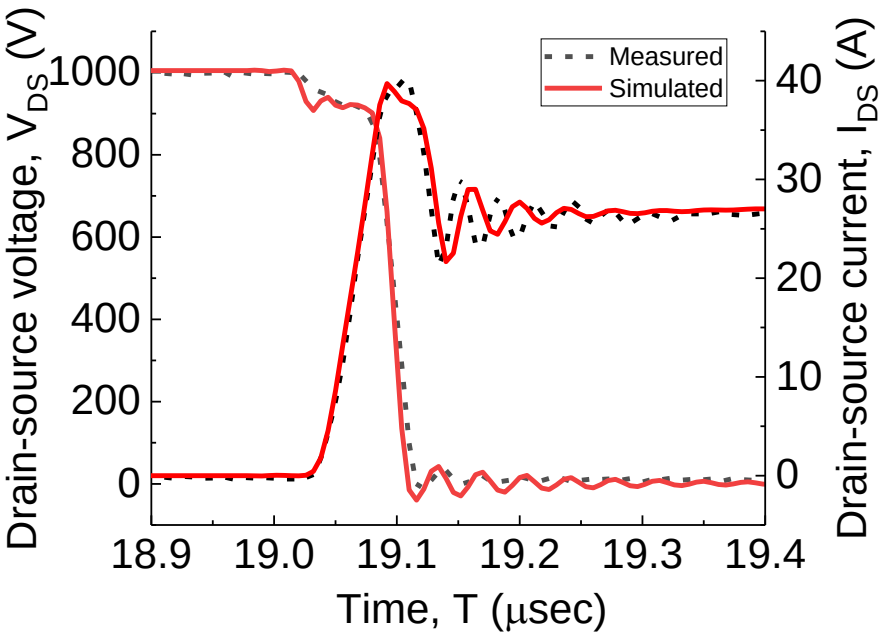


Fig. 6-6. Turn-on *Vds* and *Ids* at room temperature.

Fig. 6-7 shows the turn-off characteristics at room temperature. For turn-off characteristics, simulated *Vds* curve matches quite closely. There is a mismatch in the *Ids* curve. The variable internal gate resistance can explain the reason.

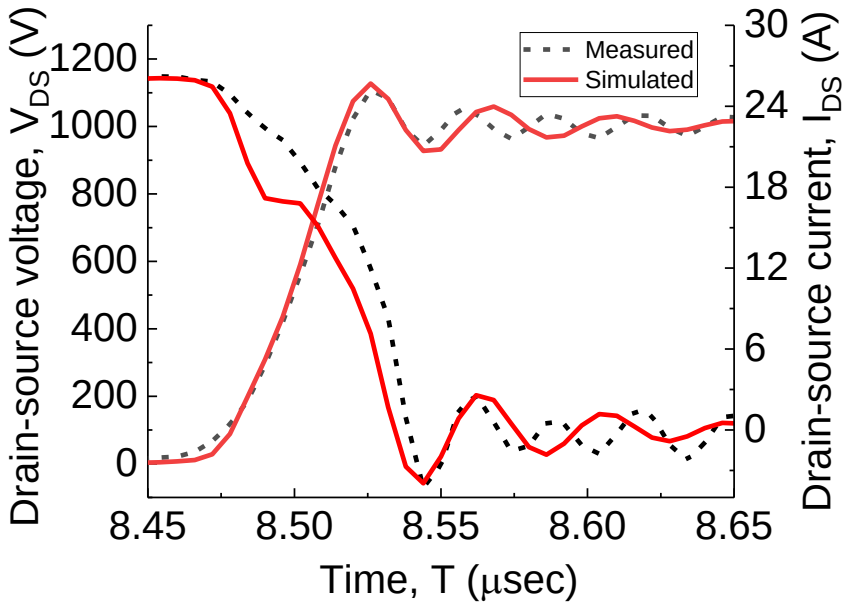


Fig. 6-7. Turn-off output characteristics.

The developed model is temperature scaled i.e. the temperature co-efficient of the parameters change the parameters to fit the output characteristics for the intended range of operation. In this work, the parameter set has been extracted for a maximum temperature of 300°C. But the evaluation board used for the DPT board is only rated up to 200°C. So the maximum temperature for which DPT was conducted was 200°C. Fig. 6-8 shows the *Vgs* curves at 200°C. Analogous to the room temperature results, the simulated *Vgs* curves match the measured ones, including the oscillation frequency and the large spikes. Fig. 6-9 shows the output characteristics during the turn-on at 200°C. *Coss* loss, peak overshoot magnitude, and the oscillation frequency of the overshoot all match the measured results very closely. In Fig. 6-10 the turn-off output characteristics during the switching are shown. Just like the room temperature, the simulated results match very closely with the measured data. This validates that the model can accurately predict the switching loss from the room temperature to up to 200°C.

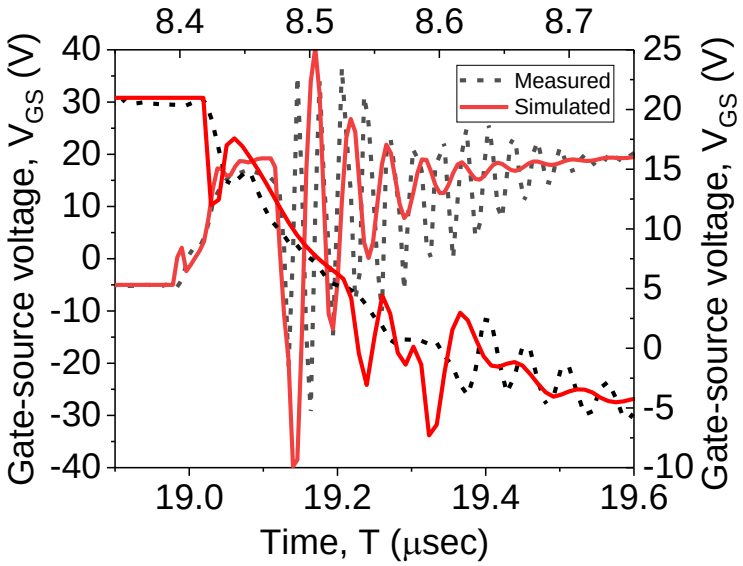


Fig. 6-8. Turn-on and Turn-off transient of the gate voltage at 200°C.

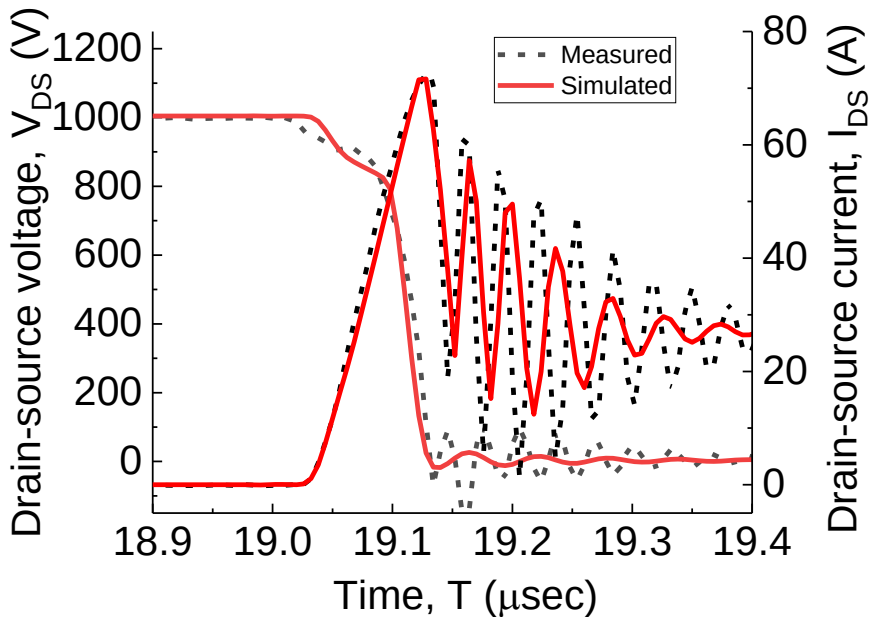


Fig. 6-9. Turn-on *Vds* and *Ids* at 200°C.

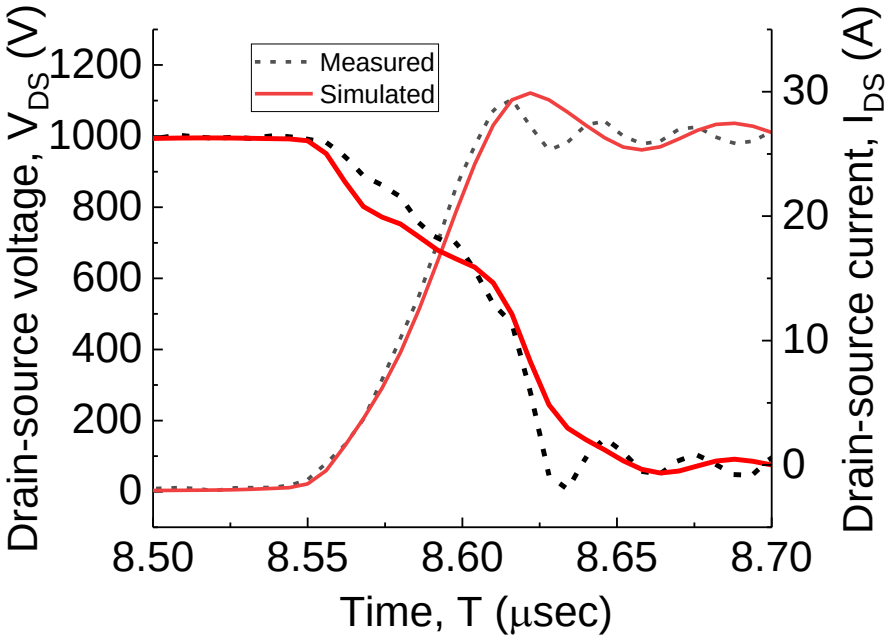


Fig. 6-10. Turn-off *Vds* and *Ids* at 200°C.

### 6.3.**Switching loss analysis**

One of the most important aspects of device modeling is to calculate the switching loss accurately. Due to nonlinear capacitance characteristics, it is challenging to calculate the switching loss analytically. Moreover, PCB parasitics' effects also play a role in determining the switching loss

of a particular set-up. So an accurate simulation model can help designers estimate the switching loss and optimize the layout of their design.

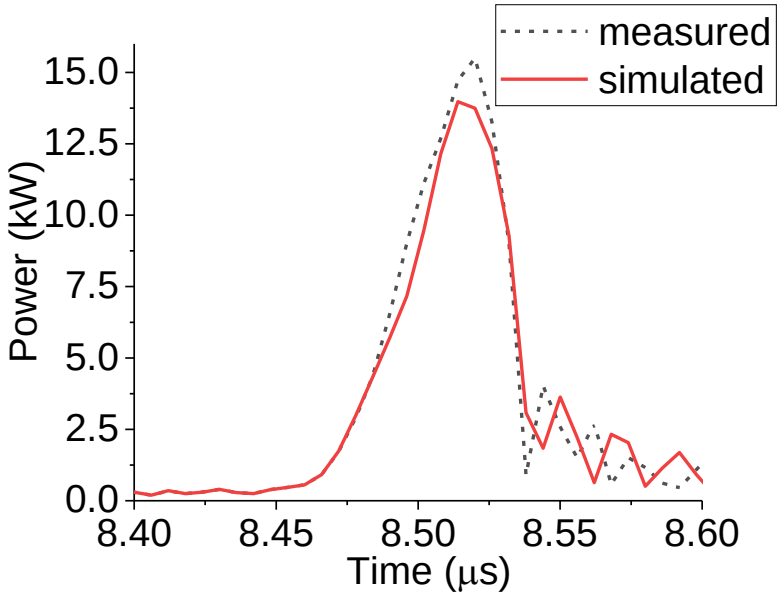


Fig. 6-11. Turn-off power loss at the room temperature.

Figs. 6-11 and 6-12 show the power loss during turn-off and turn-on at room temperature. The simulated and measured results closely match, validating the model's accuracy. Figs. 6-13 and fig. 6-14 show the switching power losses at 200°C. With the temperature scaling, the developed model predicts the switching loss quite closely, even at high temperatures.

Table 6-2 lists the measured and simulated turn-off and turn-on energy losses at different temperatures along with the percentage error of simulating total switching energy loss. As can be seen in the table, the developed model's accuracy exceeds the 90% mark. There is a drift in the accuracy with higher temperatures. This drift in the accuracy can be caused by the change in the values of the package parasitics and internal gate resistance. These effects are not incorporated in the model.

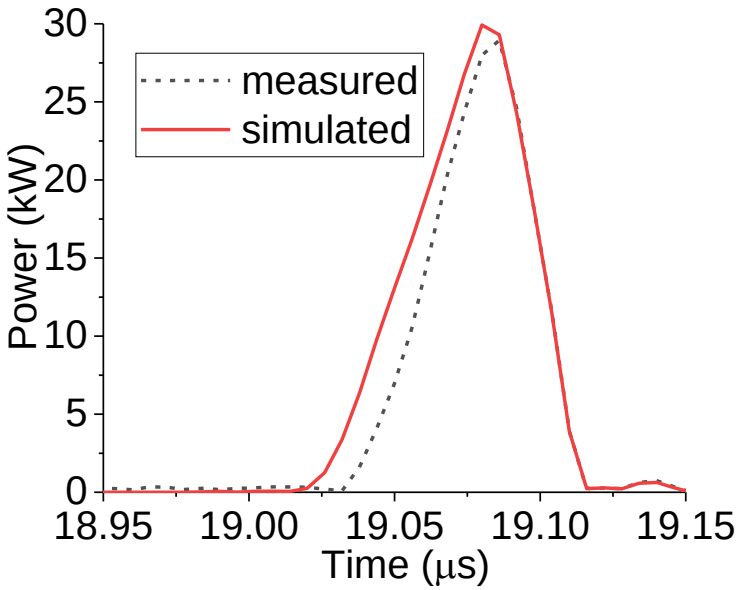


Fig. 6-12. Turn-on power loss at the room temperature.

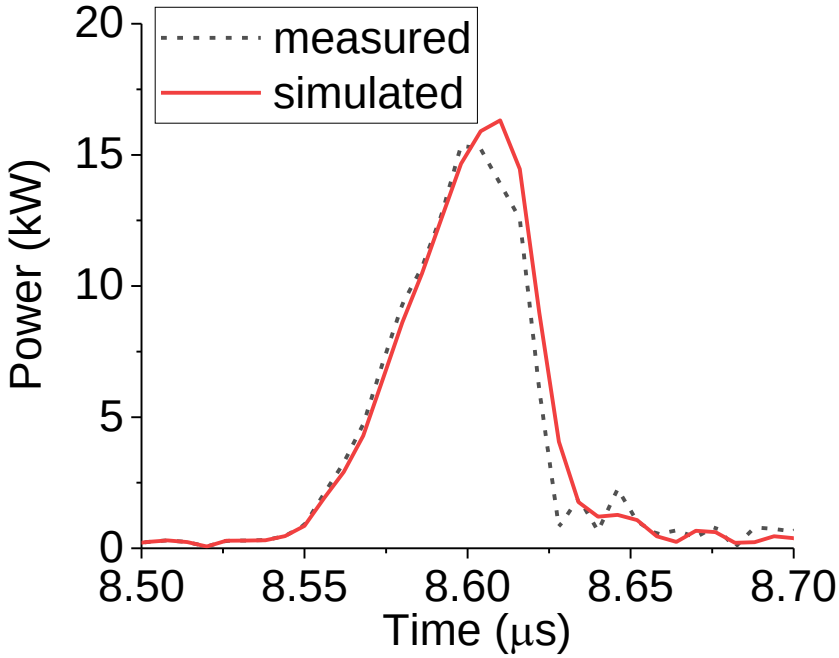


Fig. 6-13. Turn-off power loss at 200°C.

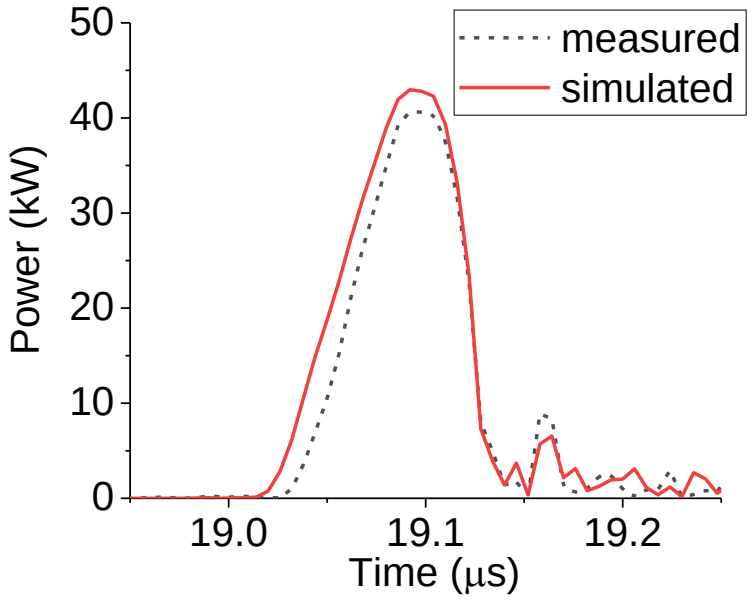


Fig. 6-14. Turn-on power loss at 200°C.

**Table 6-2. Switching Energy Loss at Different Temperatures**

| **Temperature** | **Results** | **Turn-off Switching Energy $E_{off}$(μJ)** | **Turn-on Switching Energy $E_{on}$(μJ)** | **Total Error (%)** |
|---|---|---|---|---|
| 27 °C | Measured | 693 | 1200 | - |
| | Simulated | 659 | 1338 | 5.4939 |
| 100 °C | Measured | 750 | 2200 | - |
| | Simulated | 687 | 2500 | 7.436461 |
| 150 °C | Measured | 772 | 2400 | - |
| | Simulated | 770 | 2700 | 8.587896 |
| 200 °C | Measured | 784 | 2800 | - |
| | Simulated | 781 | 3200 | 9.972369 |

## 6.4. **Comparison with the Old Model [8]**

This subsection performs a comparative analysis of the accuracy between the developed and old model of [8] in predicting switching losses. The main difference between the developed new and old models is that the new model has an accurate gate bias-dependent body diode with reverse recovery. The new model does not need any external diode model in the circuit simulation where the body diode has been used as a freewheeling diode. However, the old model needs a separate diode model to be fit with the body diode characteristics to simulate freewheeling. Hence, a separate SPICE diode model is fit to the *I-V* curve for the body diode for *Vgs* = -5V. The main weakness of this approach is that the SPICE model has no gate voltage dependence. The simulation will not have any cross-coupling effect in the gate loop of the high side device.

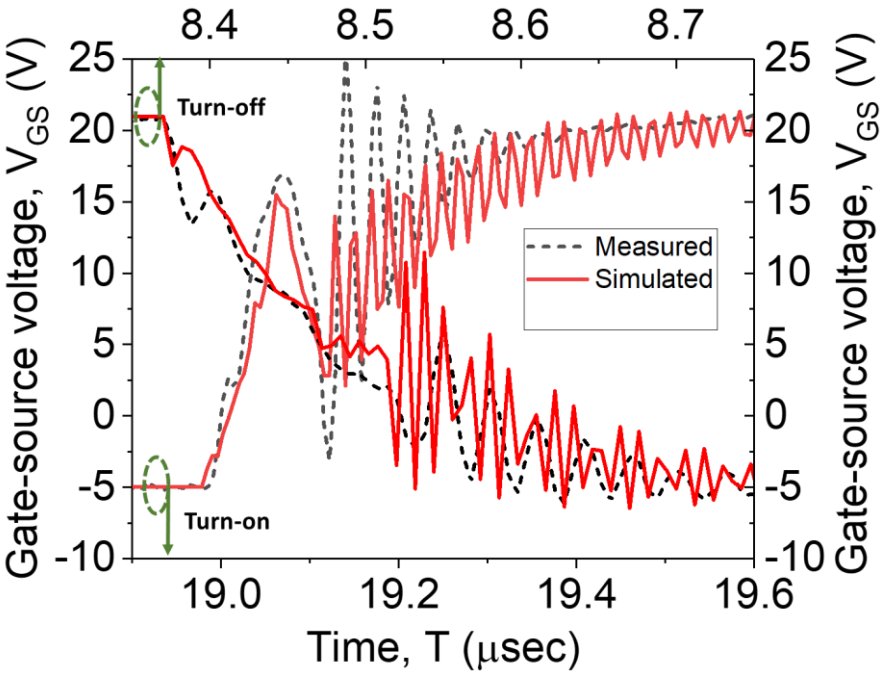


Fig. 6-15. Turn-on (bottom x-axis) and Turn-off (top x-axis) transient of the gate voltage with the old model.

Also, the junction capacitance of the diode model cannot accurately model the cascaded depletion layer-based output capacitance. The junction capacitance of the SPICE diode model is fit with the *Coss* characteristics of the body diode, which cannot be accurate for both low and high *Vds* region. The following figures show the comparison of the simulated results of the old model to the measured results.

Fig. 6-15 shows the turn-on and turn-off characteristics of the gate voltage. In the case of the turn-on, the Miller plateau has an apparent mismatch. While the old model has a rather flat Miller plateau, the measured result has a decreasing Miller plateau. With the gate voltage dependency in the *Ciss* and accurate modeling of *Cgd* in the high *Vds* region, the new model can fit the measured result more accurately. In the case of the turn-on *Vgs*, the large negative spike is not accurately captured in the old model due to the lack of gate voltage-dependent body diode and reverse recovery characteristics.

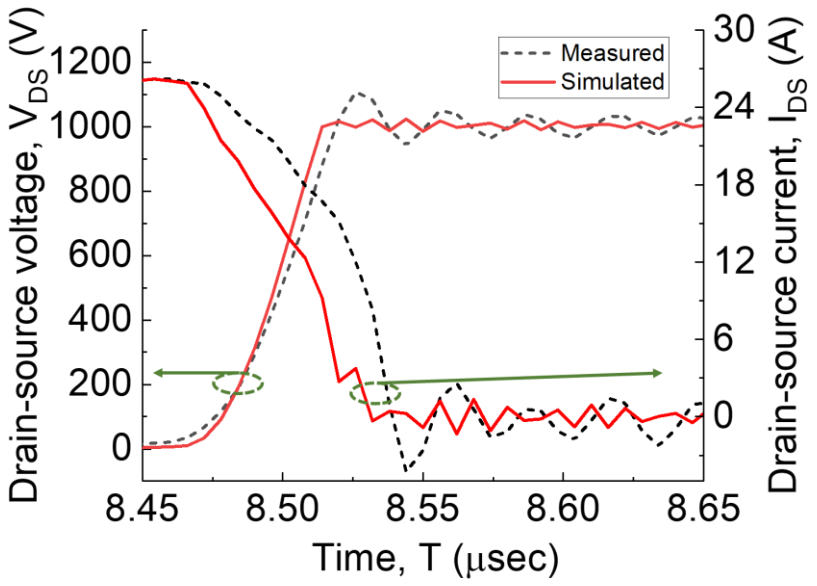


Fig. 6-16. Turn-off *Vds* and *Ids* characteristics with the old model.

Fig. 6-16 shows the turn-off output characteristics of the old model. Due to the lack of reverse recovery and accurate *Coss* characteristics, the old model cannot correctly fit the voltage overshoot of the *Vds* curve and negative spike of the *Ids* curve. The new and the old model do not incorporate the threshold voltage's hysteresis, so the turn-off current slope does not fit properly with the measured result. In Fig. 6-17 the turn-on output characteristics of the old model are shown. Due to the lack of accurate *Coss* modeling, the old model cannot accurately predict the *Coss* loss-induced dip in the Vds curve. Also, having no reverse recovery current, the current overshoot is less than the measured result.

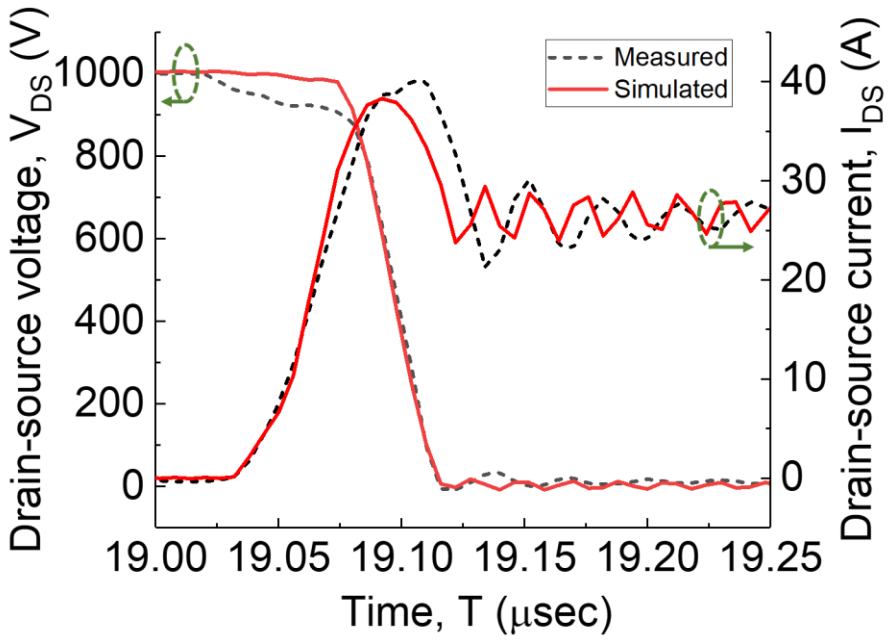


Fig. 6-17. Turn-off *Vds* and *Ids* characteristics with the old model.

Figs. 6-18 and 6-19 show the turn-off and turn-on power loss during the switching. The turn-off energy loss is 431 μJ and turn-on energy loss is 1286 μJ. Total switching loss error is 9.27% at room temperature. It is higher than the error percentage of the developed model by around 4%.

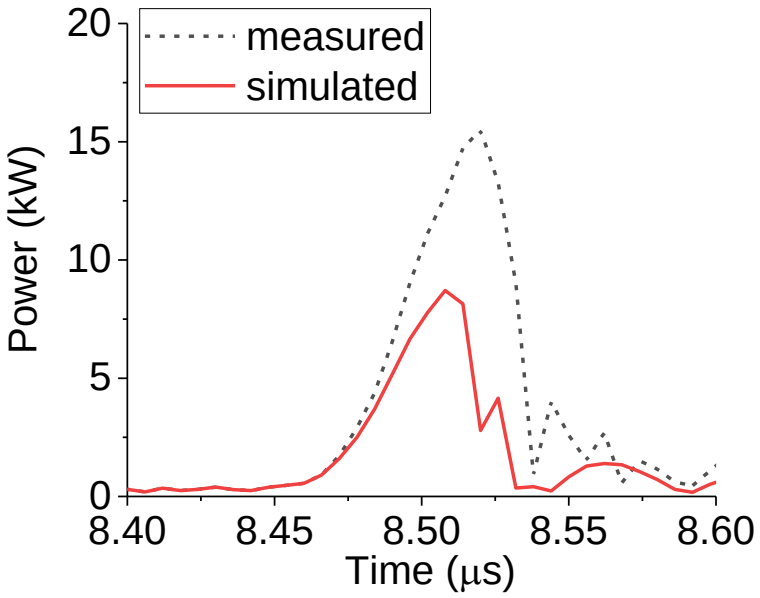


Fig. 6-18. Turn-off power loss at the room temperature with the old model.

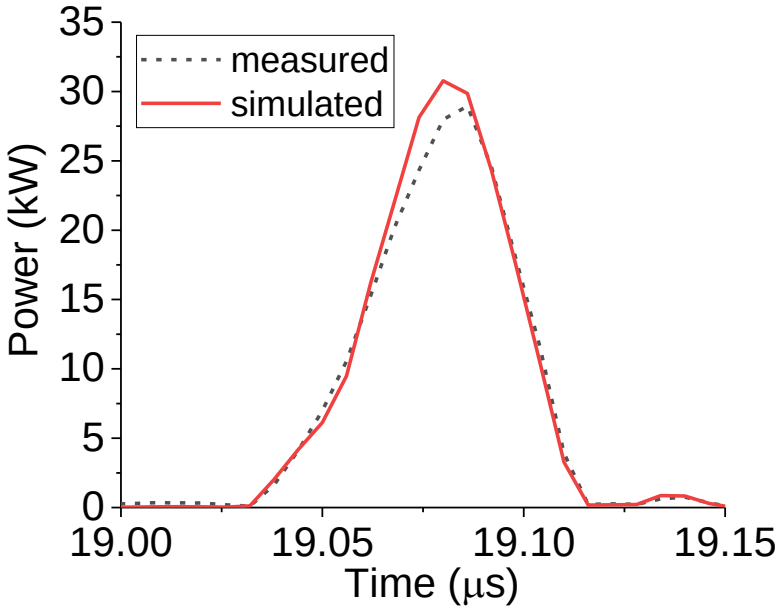


Fig. 6-19. Turn-on power loss at the room temperature with the old model.

# Chapter 7. SYNCHRONOUS BUCK CONVERTER TEST

A synchronous buck converter study has been performed to validate the presented model and emphasize the importance of self-heating included electro-thermal modeling. The synchronous buck converter has been designed using the same half-bridge configured DPT board (KIT8020CRD8FF1217P) discussed in the previous chapter.

## 7.1. **Hardware realization**

The synchronous buck converter has been designed using the same half-bridge configured DPT board (KIT8020CRD8FF1217P) discussed in the previous chapter. The specifications of the buck converter are listed in Table 7-1.

**Table 7-1. Synchronous Buck converter design parameters**

| Parameter | Value | Unit |
|---|---|---|
| Input voltage | 600 | V |
| Output voltage | 60 | V |
| Load current | 13 | A |
| Duty cycle | 0.1 | |
| Dead time | 500 | nS |
| Switching frequency | 40 | kHz |
| Output current ripple | ±2 | A |
| Filter capacitor | 450 | μF |
| Filter inductor | 320 | μH |
| Load resistance | 4.1 | Ω |
| Decoupling capacitor | 4500 | μF |

The input voltage for the converter is 600 V. The expected output voltage is 60 V with 10% duty cycle. The converter was switched with a frequency of 40 kHz. The dead time between the two switches was set to 500 ns from the recommendation of the manual. A large filter capacitor of 450 μF was selected for keeping the output voltage ripple small. The filter inductor of 320 μH and a load resistance of 4.1 Ω were used for the setup.

One of the realities of a power converter is self-heating. Switching loss coupled with the conduction loss increases the junction temperature of the switching devices. In the synchronous buck converter, both the high and low side devices of the half-bridge are switched. During the deadtime, the body diode conducts and causes the device to heat up further with comparatively large conduction loss and reverse recovery. The overall set-up is shown in Fig. 7.1.

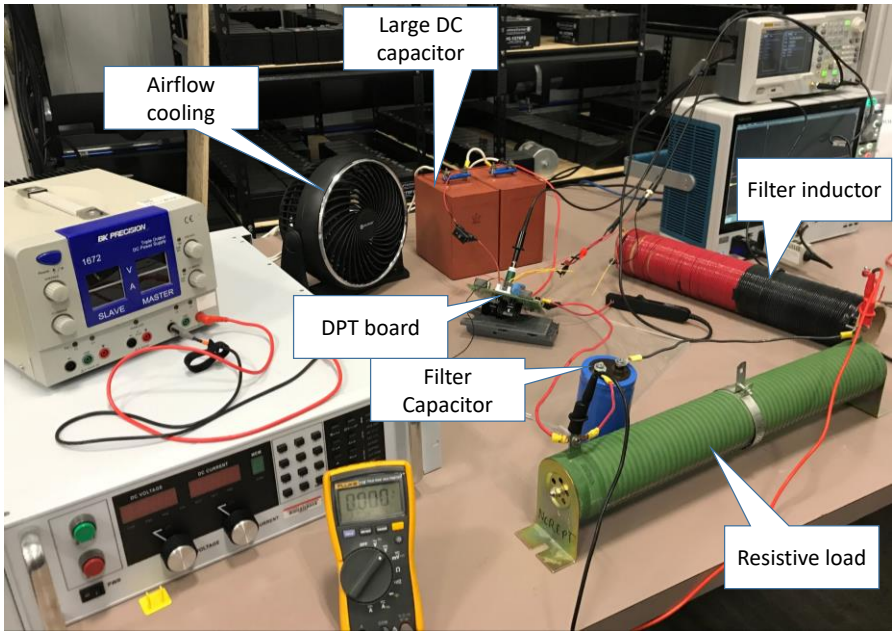


Fig. 7-1. Synchronous buck converter test set-up.

## 7.2. **Results and analysis**

A simplified schematic, shown in Fig. 7-2, of the overall test set-up is used for the simulation. Both high and low side devices dissipate energy during the operation. The total power dissipated is a summation of conduction loss and switching loss. This dissipated heat increases the junction temperature because of thermal impedances from the junction to the ambient. This self-heating affects the overall efficiency of the system. For having a proper temperature dependency in the model, it is expected that the simulation results will incorporate the self-heating effect and will predict the efficiency of the system accurately. The relationship between junction temperature and dissipated power is calculated with the following equations

$$T_j(time) = P_d(time) \cdot Z_{th}(time) + T_{amb} \tag{84}$$

$$P_d(time) = I_{ds}(time) \cdot V_{ds}(time) \tag{85}$$

Thermal impedance is extracted from the thermal impedance curve provided by the manufacturer. The extracted thermal impedance is included in the simulation by the equivalent Cauer network. Manufacturer provides the thermal impedance network from the junction to the thermal pad of the package. The developed equivalent Cauer network is shown in Fig. 7-2. The overall schematic for the simulation of the buck converter is shown in Fig. 7-3.

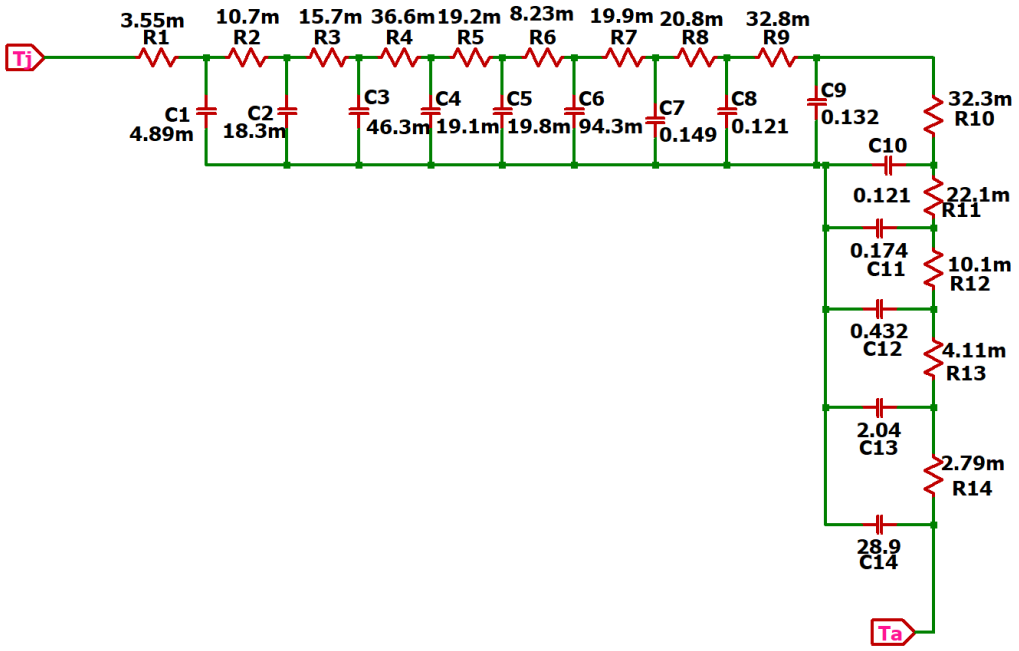


Fig. 7-2. Cauer thermal network for self-heating simulation.

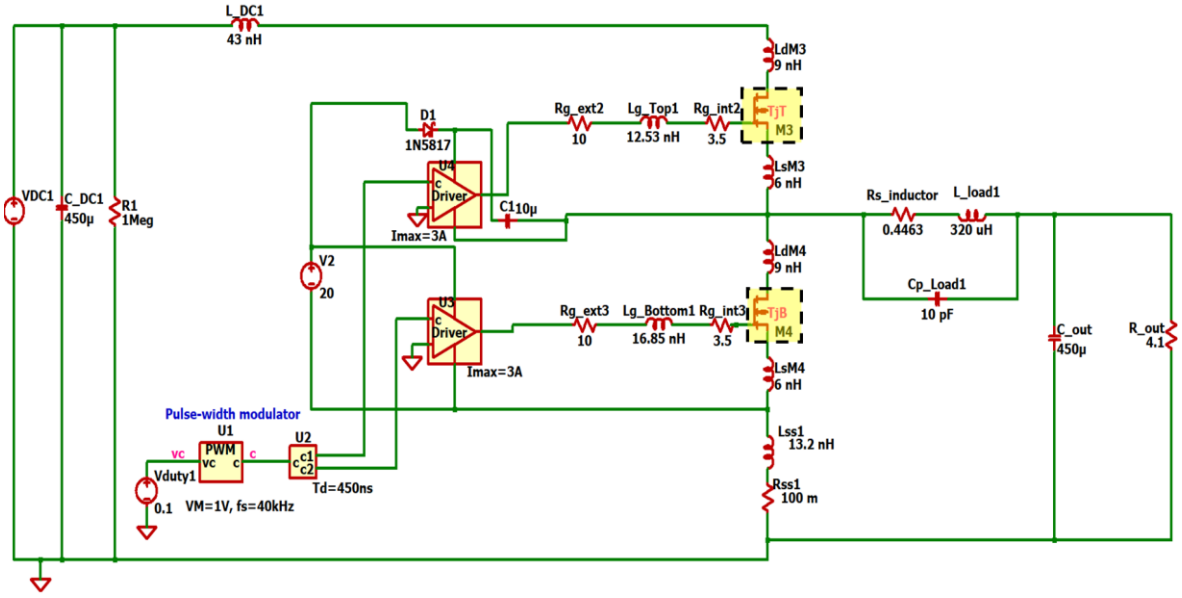


Fig. 7-3. Synchronous buck converter schematic.

Fig. 7-4 shows the measured and simulated output voltage. There is a 0.6 Ω cable resistance, and so the output voltage is close to 52.5 V. The chatter in the measured waveform is caused by the low resolution of the high-voltage differential probes.

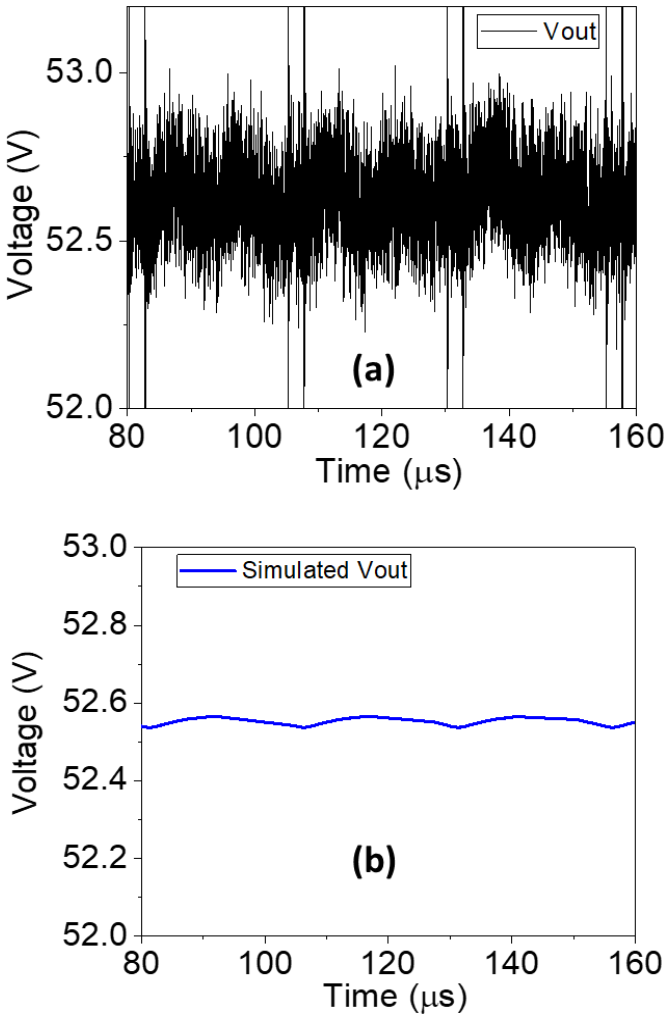


Fig. 7-4. (a) Measured and (b) simulated output voltage of the synchronous buck converter.

Fig. 7-5 shows the measured and simulated inductor current. The ripple current was found to be ±2A. Temperatures of the low and high side devices were measured using a thermocouple and DAQ (Data Acquisition) tool as shown in Fig. 7-6. Temperatures stabilize close to 140°C for the low-side device and close to 70°C for the high-side device. In the case of simulation, the steady-state temperatures for the devices are shown in Fig. 7-7. The high-side device has the steady-state

temperature of 79.5°C, and for the low-side device, it is 134.15°C. A differential probe was attached to a low-side device to measure Vds waveform. This differential probe provided a surface area for heat dissipation, and as a result, the low side device had less temperature than predicted by the model.

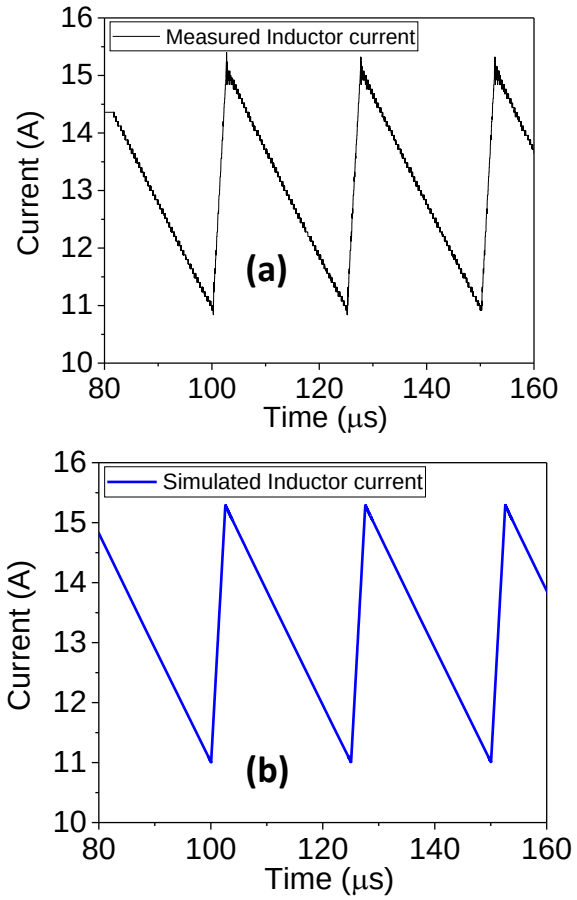


Fig. 7-5. (a) Measured and (b) simulated inductor current.

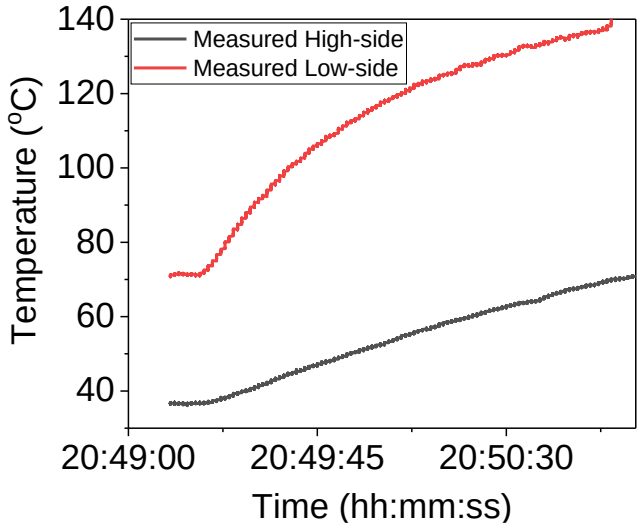


Fig. 7-6. Measured temperatures at the high-side and low-side device.

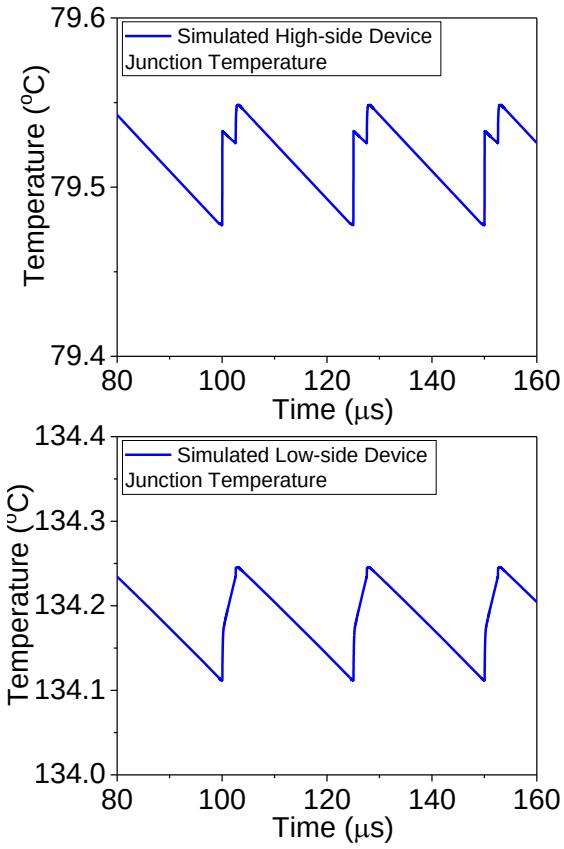


Fig. 7-7. Simulated temperatures at the high-side and low-side device.

# Chapter 8. CONVERGENCE STUDY

For a complete electro-thermal solution, the developed model not only needs to be accurate but also efficient in terms of simulation time. This requires the model to have good convergence properties in the context of Newton-Raphson-based simulators. One of the requisites to have better convergence properties is to have continuous higher-order derivatives. During simulation the Newton-Raphson algorithm continuously utilizes derivatives of the charge and current expressions. If the higher-order derivatives are not continuous, the lack of smoothness can send the iterative guesses far from the actual solution and the simulation fails to converge. So step size reduces in an attempt to avoid the large excursions, and the simulation takes longer to converge. In many cases, the simulation fails to converge. Hence, it is essential to study the convergence capability of any developed model along with its accuracy.

In the developed model, convergence properties have been ensured by making the current and charge expressions continuous. This is achieved by the use of weighted voltage expressions instead of using conditional statements. The approach is also termed as ‘Smoothing’. Smoothing the charge and current expressions improves the convergence properties of the model and reduces the simulation time. While strictly speaking, continuity in the first derivative is all that Newton-Raphson demands, practical experience indicates that the more continuously differentiable the model expressions are the better the convergence properties.

A complex circuit topology has been selected for testing the convergence capability of the developed model. The topology is a 5-level cascaded H-bridge, multi-level inverter (CHB-MLI). Fig. 8-1 shows the schematic of the simulated CHB-MLI. A total of 8 devices were used in the

topology. The topology drives a 1.5 mH, 50 Ω load. Fig. 8-2 shows the simulated output voltage waveform, and Fig. 8-3 shows the gate control signal used in the simulation.

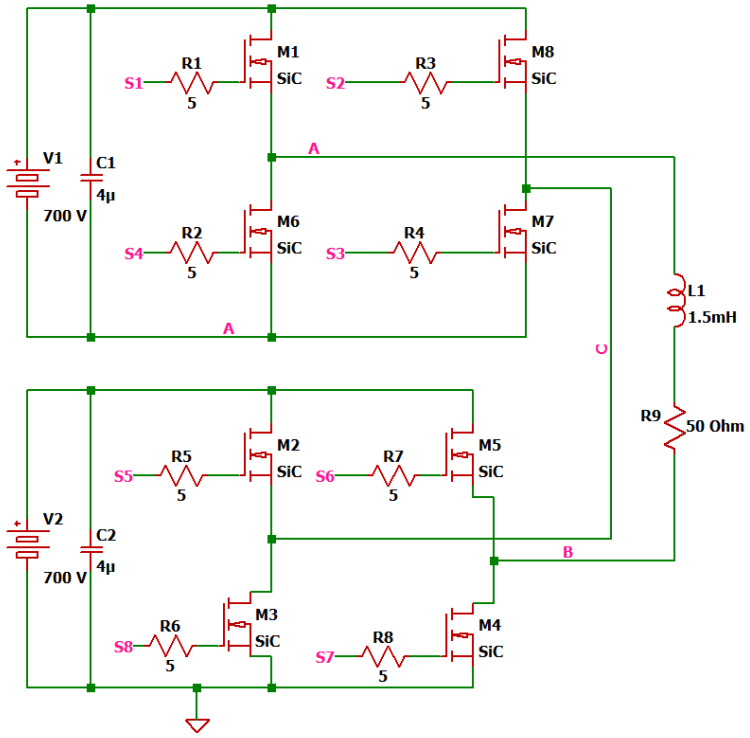


Fig. 8-1. Topology of the simulated CHB-MLI.

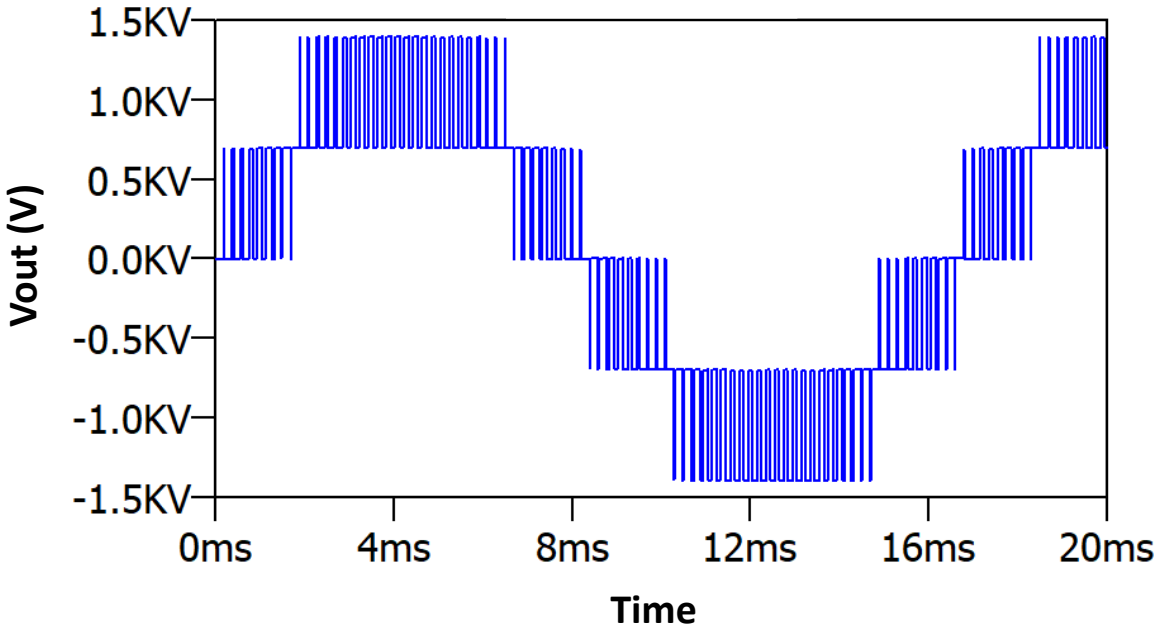


Fig. 8-2. Simulated output voltage waveform.

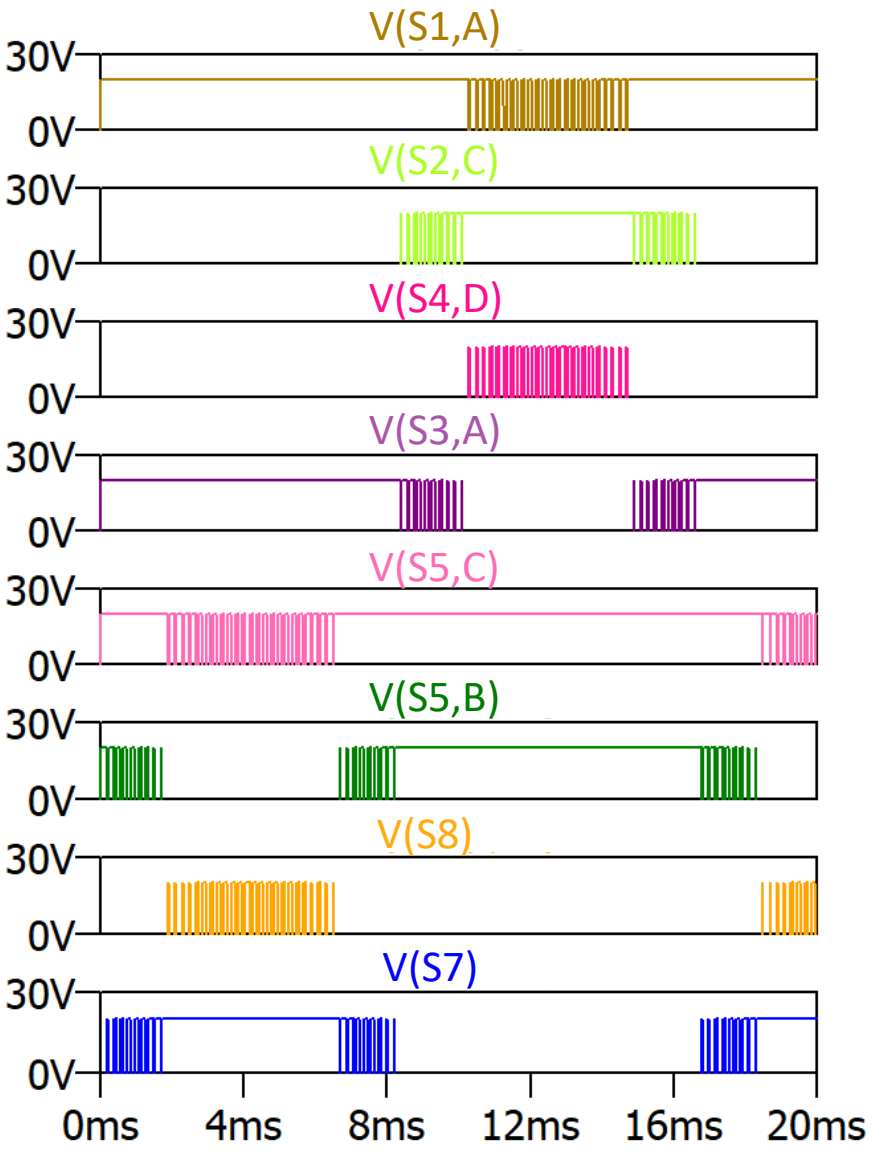


Fig. 8-3. Gate control signals for the simulation.

In LTSpice, the total simulation time for the circuit was 23.02 seconds using the presented model. The total iteration count was 76,857. The previous model of [8] takes 30.32 seconds for the simulation. A generic SPICE diode model is used for the body diode conduction with the model of [8]. The total iteration count is 106,537 in this case. When the vendor's empirical model was used, the total simulation time was 37.4 seconds, with a much larger total iteration count of 348,744.

Besides CHB-MLI, a more common circuit topology of a PWM 3-phase inverter was simulated as well. The schematic of the topology is shown in Fig. 8-4. Fig. 8-5 shows the PWM gate signal generation part of this topology. Fig. 8-6 shows the output of three-phase AC currents of the inverter. The original topology was collected from the LTSpice user forum and then modified for a SiC power MOSFET drive. The new model's total number of iteration was 963676, while the number is 1278973 for the old model. In the case of the vendor-provided model, the total iteration count is 2321214. It verifies the convergence capability of the developed model.

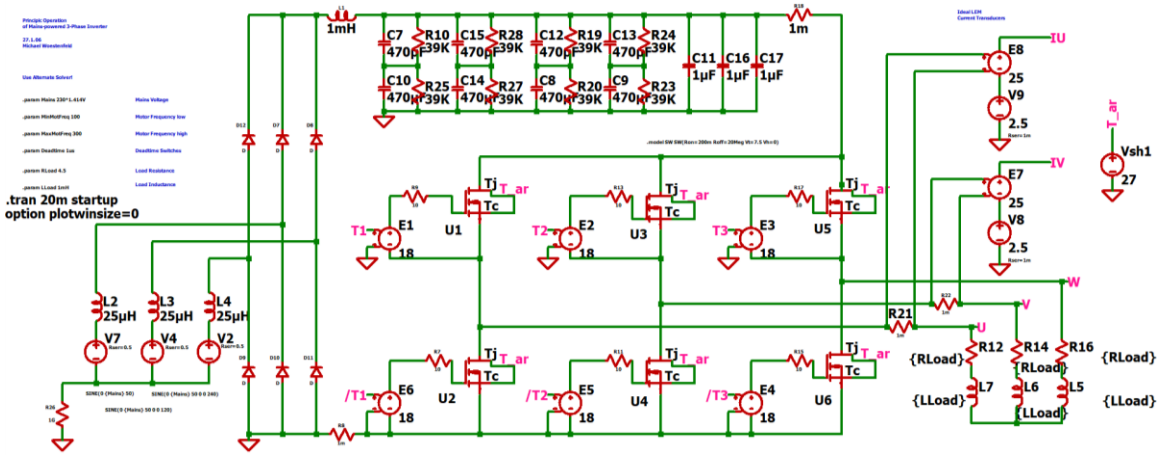


Fig. 8-4. PWM 3-phase inverter.

Another topology of a synchronous buck converter has been described in Chapter 7. These three topologies were simulated with the developed model, the model of [8], and the vendor-provided model. In Fig. 8-7, a comparison of these three models' performance on different topologies is shown in a chart type plot. The figure shows that the developed model is the most efficient despite having computationally expensive reverse recovery expressions.

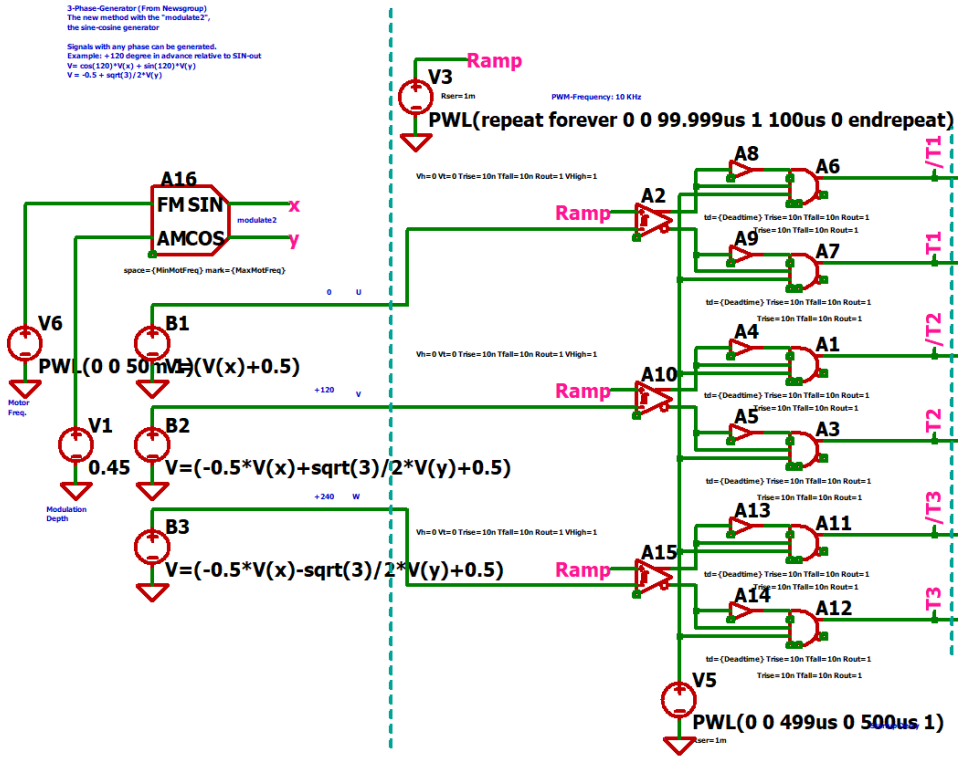


Fig. 8-5. PWM signal generation circuit.

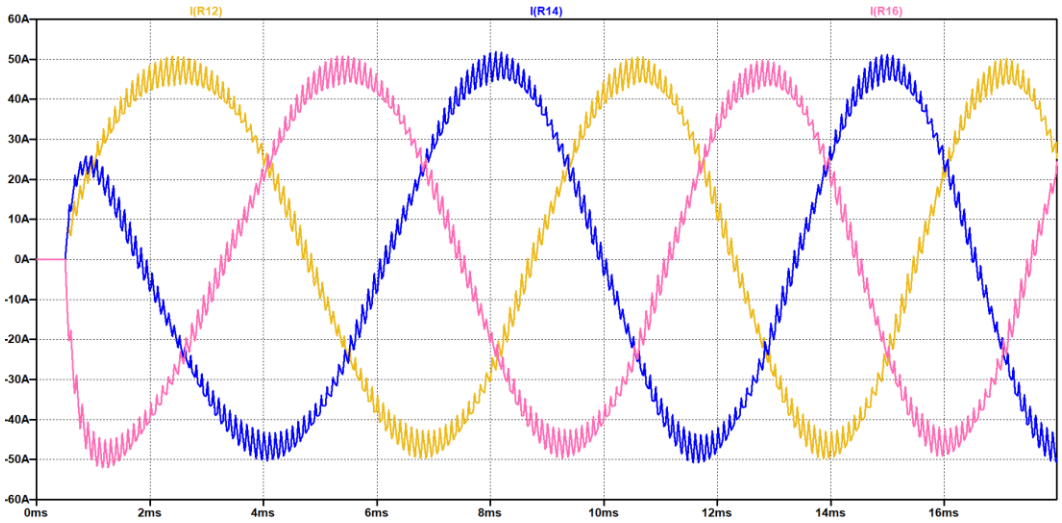


Fig. 8-6. Output three phase AC currents.

The difference in the efficiency with the model of [8] is not evident from the figure. However, [8] uses a generic SPICE diode model for freewheeling current conduction. This results in a lack of accuracy in switching loss. As discussed earlier, there is also a lack of accuracy in the third quadrant MOSFET behavior of the model [8] for synchronous operation. So considering overall accuracy and efficiency, the developed model is a better choice than [8].

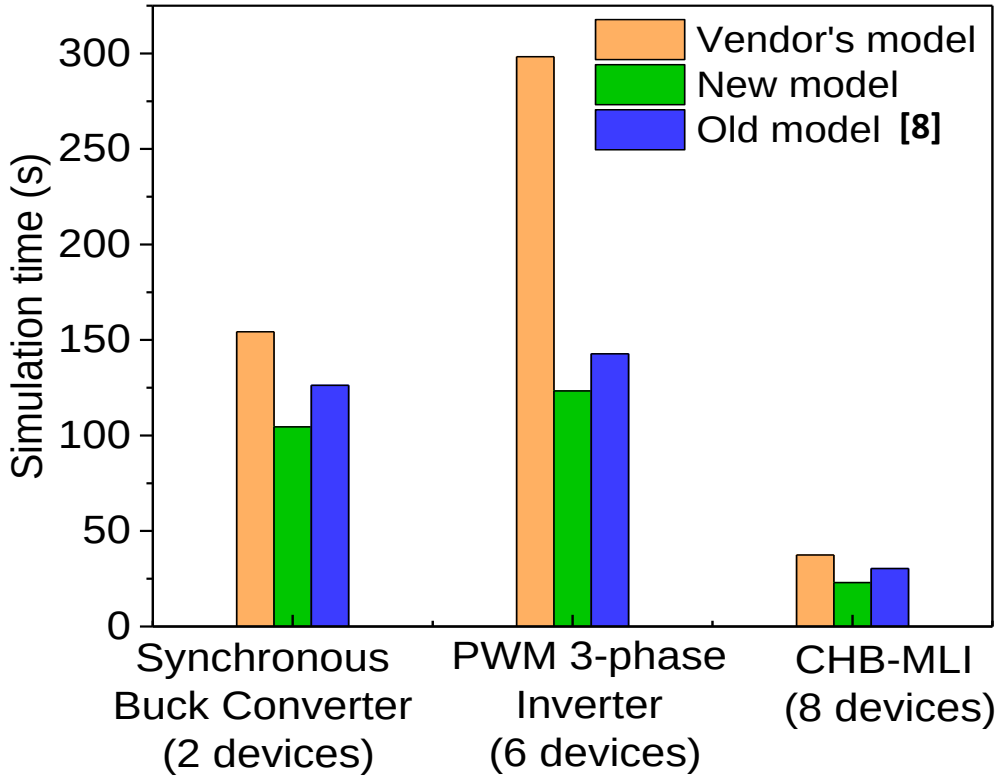


Fig. 8-7. Total simulation time comparison at different topologies.

# Chapter 9. PARAMETER EXTRACTION PROCEDURE

For any compact model, there should be a well-defined parameter extraction process. It allows the users to extract the model parameters from the available sets of data and use the extracted model to predict the intended circuit designs accurately. The parameter extraction procedure described in [8] is a straightforward yet accurate way to extract model parameters from the data available in the datasheet. This work follows the same approach. Here a 1700 V, 45 mΩ SiC MOSFET from Wolfspeed (C2M0045170D) is selected to extract the model parameters. Due to the availability of Keysight B1505A curve tracers, measured data is used for the extraction. However, this data is also commonly available in datasheets. If not specified otherwise, all these parameters are extracted by curve fitting the model with the measured results. Parameter extraction tools like IC-CAP [39] can be a good resource. Curve fitting functions in MATLAB or Python can also be used. The use of IC-CAP for the extraction procedure is described in Appendix I.

## 9.1. **C-V related parameter extraction process**

Extraction of the C-V parameters begins with *Crss* curve. The value of the parameter ***Cox0*** is assigned equal to the value of *Crss* at *Vds* = 0. ***Cox1*** is tuned to match the first plateau region of the *Crss* curve at the low *Vds* region (usually < 20 V). ***vtd1*** is the second depletion voltage, and the value of it is extracted from the onset of the abrupt downward transition of the *Crss* curve. ***Cgdmin*** is extracted from the near-constant value of the *Crss* at the very high *Vds* region. Parameter ***agd*** and ***nb*** is extracted from the slope of the *Crss* curve.

After the extraction of *Crss* related parameters, parameters related to *Coss* can be extracted. ***Cds0*** is used for fine tuning the zero voltage value of the *Coss* curve, and ***Cds1*** is used for fine tuning the plateau region part of the *Coss* curve. Though ***nb*** and ***agd*** also control the *Coss* curve slope,

these parameters' effect can be controlled using parameter ***m***. The extraction area of any of these particular parameters is highlighted on the Fig. 9-1.

Once the *Vds* dependent parameters are extracted, *Vdg* dependent parameters can be extracted from *Cgs vs Vgs* curve. Parameter ***Cgsacc*** and ***Cgsinv*** are extracted from the accumulation and inversion state of the curve. ***Vacc*** and ***Vinv*** parameters depict the onset of the accumulation and inversion, respectively. Extra care needs to be taken to fit the value at *Vgs* = 0 accurately. This value also determines the initial value of the *Ciss* vs *Vds* curve. Fine-tuning areas for different *Vgs* dependent parameters are shown in Fig. 9-2.

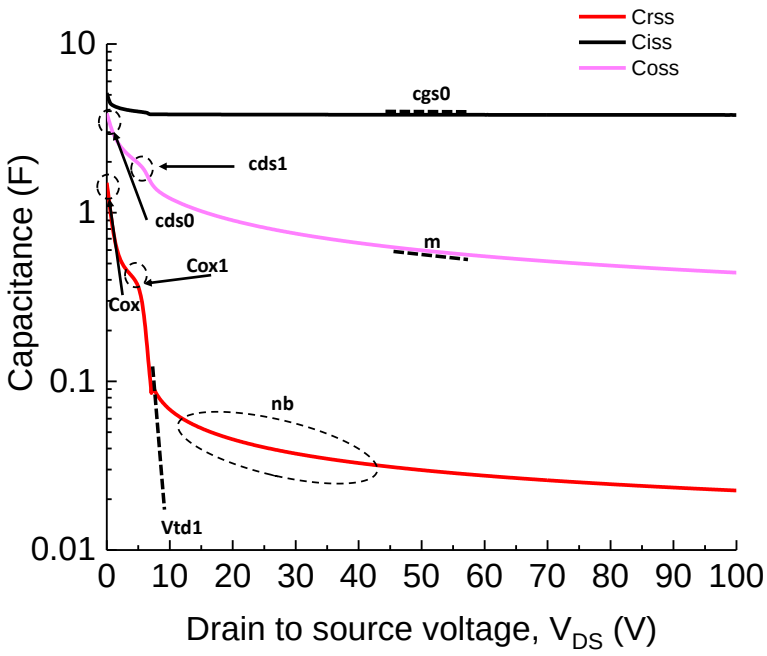


Fig. 9-1. Drain voltage related C-V parameter extraction procedure.

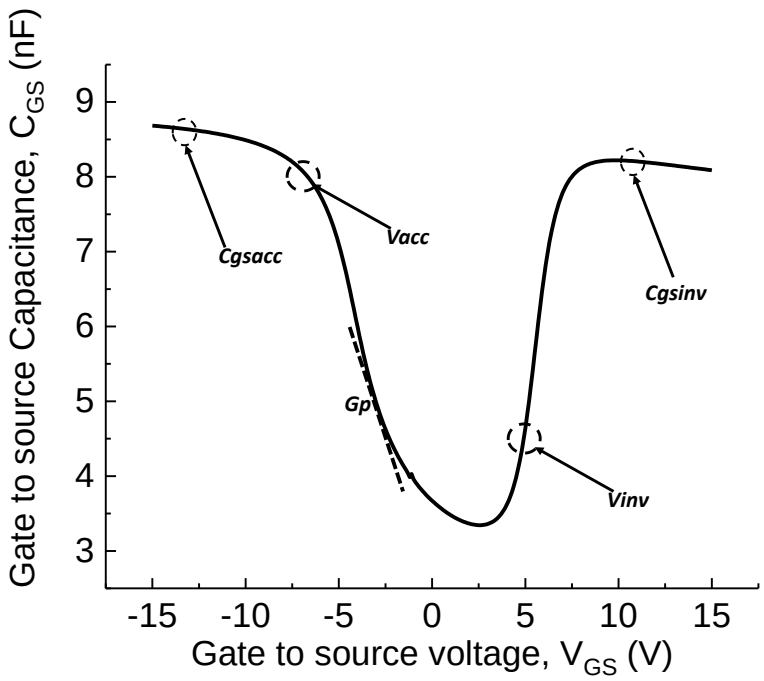


Fig. 9-2. Gate dependent *Cgs* related parameters extraction procedure.

## 9.2. **The first quadrant related I-V parameter extraction**

In the author's experience, many datasheets provide mismatched transfer and DC output curves. This means that drain current magnitudes do not correspond to the same drain and gate biases in the transfer curve and the DC output curves. If the transfer and DC output curves correspond, then the extraction procedure in [8] can be followed for parameter extraction of the first quadrant. Otherwise, it will be easier for users to rely on DC output characteristics. The modified extraction procedure presented in this work relies solely on the DC output characteristics to extract static I-V parameters to give users an alternative.

The first parameter to be extracted is $\boldsymbol{V_{thlf}}$. In the output curves, the gate voltage value for the lowest curve (usually in the range of 2~5 V) is the closest to the value of $\boldsymbol{V_{thlf}}$. So, extract the $\boldsymbol{V_{thlf}}$ value by curve fitting the *Ids*-*Vds* curve for the lowest gate voltage. $\boldsymbol{k_{plf}}$ is the saturation transconductance parameter for low *Vgs* curves. Here, low-gate voltage means *Vgs* < Miller voltage ($V_{Miller}$). $V_{Miller}$ value can be obtained from the datasheet or gate-charge plot. In the case of

C2M0045170D, it is about 9 V. $k_{plf}$ is extracted by fitting the saturation region of these low-gate voltage *Ids-Vds* curves. $k_{flf}$ is used to fit the triode region of the low-gate voltage curves. $\Theta_{lf}$ is the transverse electric field parameter used for fitting the *Id-Vds* curves' compression at the low gate voltages.

$V_{thhf}$ is the high-current threshold voltage. The value is obtained by matching the first curve at the *Ids-Vds* plot where $Vgs > V_{Miller}$. The transconductance of the higher $Vgs$ curves is tuned using parameters $k_{phf}$ and $k_{fhf}$ for saturation and triode region, respectively. Reduction in the mobility at the high transverse gate field is tuned using the parameter $\Theta_{hf}$. Series drain resistance parameter ***rd*** is used to control the bending of the curves at high gate voltages. In contrast, ***rs*** is used to fit the slope of the curves. All these parameters are extracted by curve fitting the DC output curves as shown in Fig. 9.3. The difference in the slopes of the curves for higher gate voltages can be adjusted using voltage-dependent drift-resistance parameters ***RDVD***, ***RDVG1***, ***RDVG2***.

Due to the presence of a large number of interface charges and their gradual emptying, the transition between the triode and saturation region is gradual in SiC MOSFET compared to its Si counterpart. This transition is tuned using pinch-off voltage parameters ($pvf_l$, $pvf_h$) as shown in Fig. 9-3. The lateral electric field generated by the interface charges influences the carrier velocity at the channel. So, carrier velocity saturates gradually in the presence of interface charge [40]. The extent of the velocity saturation depends on the gate voltage since the occupation of interface states with carriers is gate voltage-dependent. Hence, the low-gate voltage region and high gate voltage region need separate parameters for accurate fitting.

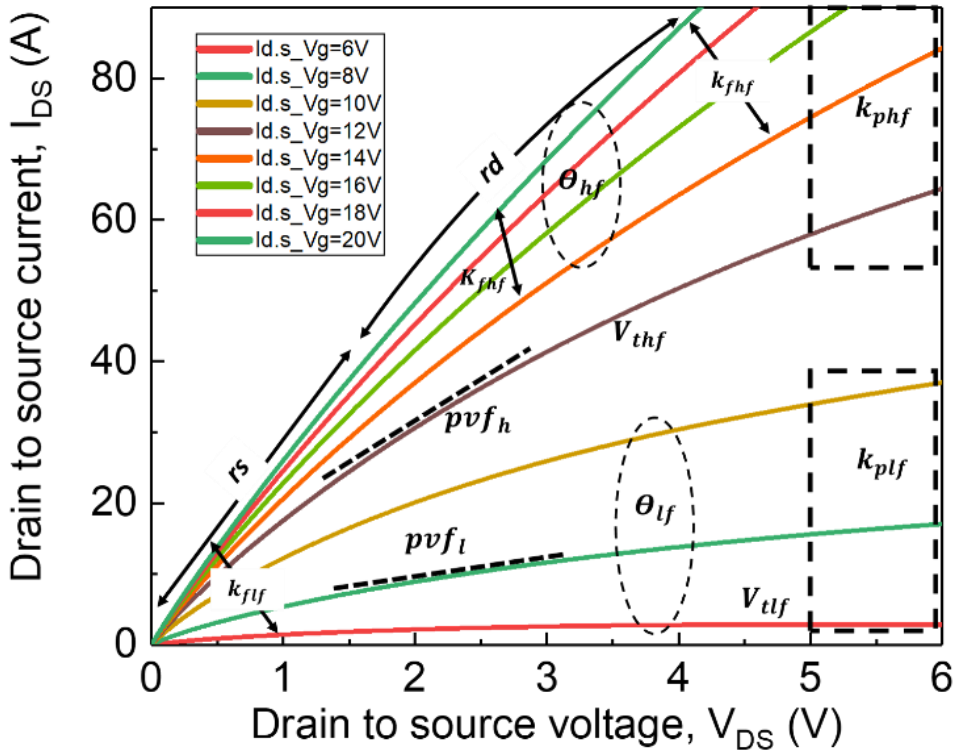


Fig. 9-3. First quadrant related parameters extraction from the output curves.

### 9.3. **Third quadrant related parameter extraction**

After extracting parameters related to the first quadrant characteristics, the third quadrant related parameters are extracted. Fig. 9-4 shows the third quadrant of the output characteristics and highlights the particular regions where each parameter plays the most dominant role. $\boldsymbol{V_{thlr}}$, $\boldsymbol{V_{thhr}}$, $\boldsymbol{k_{plr}}$,$\boldsymbol{k_{phr}}$, $\boldsymbol{k_{flr}}$, $\boldsymbol{k_{fhr}}$, and ***rdr*** are initially assigned to the same values of their first quadrant counterparts. These values should be fine-tuned to match their respective area in the third-quadrant characteristics where the MOSFET channel current dominates, i.e., $Vsd<V_f$, in this case, about 1.8 V.

The body diode ideality factor (***ND***) is tuned to fit the turn-on voltage for the curve of $Vgs$ = 0 V. Parameter ***vk2*** is fixed to the magnitude of the negative gate voltage value, after which the body diode transconductance saturates due to depletion. This means that the effect of the gate voltage remains almost the same. The gate voltage dependency of the body diode for $Vgs$ < ***vk2*** is

controlled using the parameter ***kvsg₂***. The value of the parameter ***vk1*** is assigned to the highest positive gate voltage for which only body diode characteristics dominate, i.e., for *Vgs* < ***vk1*** the MOSFET characteristics are negligible due to the absence of the inversion channel layer. Parameter ***kvsg₁*** is tuned to fix the spacing between these curves where the body diode characteristics dominate. Parameter ***rdiode*** is fine tuned to fix the slope of the body diode curves. The curves for *Vgs* > ***V<sub>thlr</sub>*** show both diode and MOSFET characteristics. So, the value of ***V<sub>thlr</sub>*** is tuned to match the first curve that shows these two characteristics. MOSFET characteristics dominate in the low current region and diode characteristics in the high current region. ***kplr*** is tuned to match the transconductance of the MOSFET characteristics. ***θ<sub>lr</sub>*** is tuned to match the spacing between these curves. ***k<sub>flr</sub>*** needs to be adjusted to fit the slopes of the MOSFET characteristics curves. Lastly, if the value of ***rdr*** = ***rd*** is too large to fit the slope of the MOSFET characteristics curves, reduction of ***rdr***'s value will give a perfect fit. Overall optimization of the third-quadrant parameters is required to get the best fit.

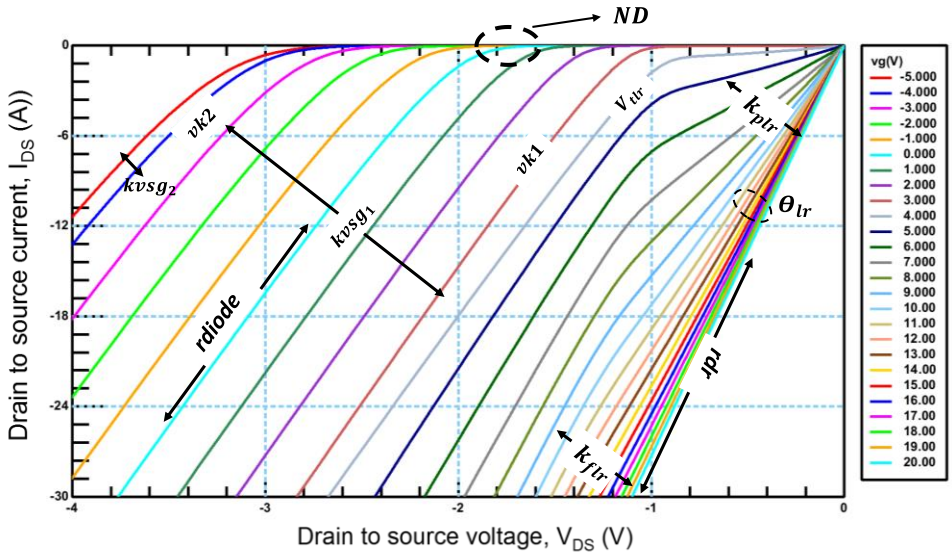


Fig. 9-4. Third quadrant related parameter extraction from the output curves.

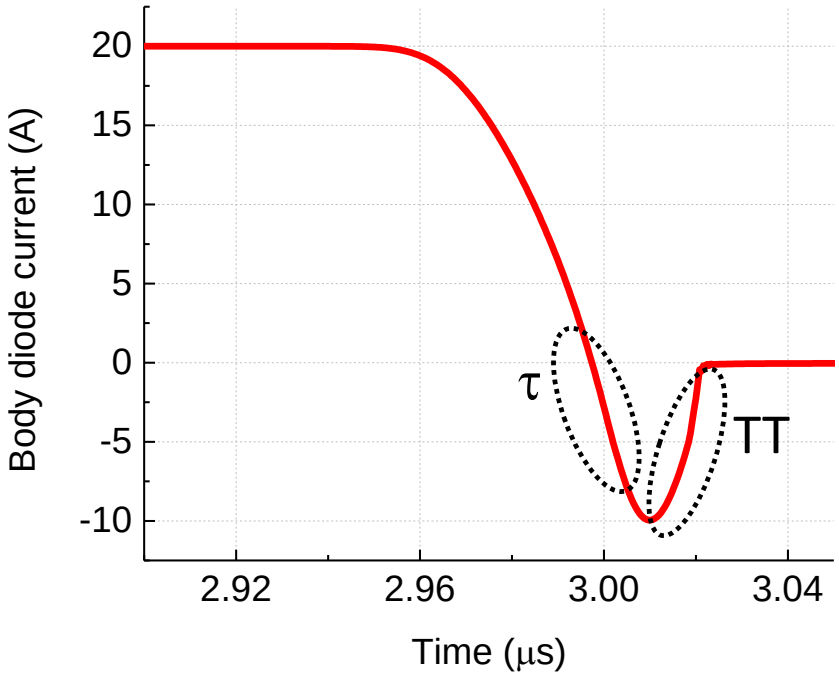


Fig. 9-5. Reverse recovery related parameter extraction.

The reverse recovery parameters ***TT*** and ***τ*** can be extracted. ***τ*** is the lifetime of the minority carriers in the drift region, and ***TT*** is the diffusion transit time of the stored charge. ***τ*** allows users to fit the peak reverse recovery current. ***TT*** is to be adjusted to get the total reverse recovery time. The fitting regions of these two parameters are highlighted in Fig. 9-5. The values of peak reverse recovery current and total reverse recovery time can be found from the datasheet. However, a simulation setup shown in Fig. 9-6 can be simulated with the given condition in the datasheet to get a visual representation of the parameters.

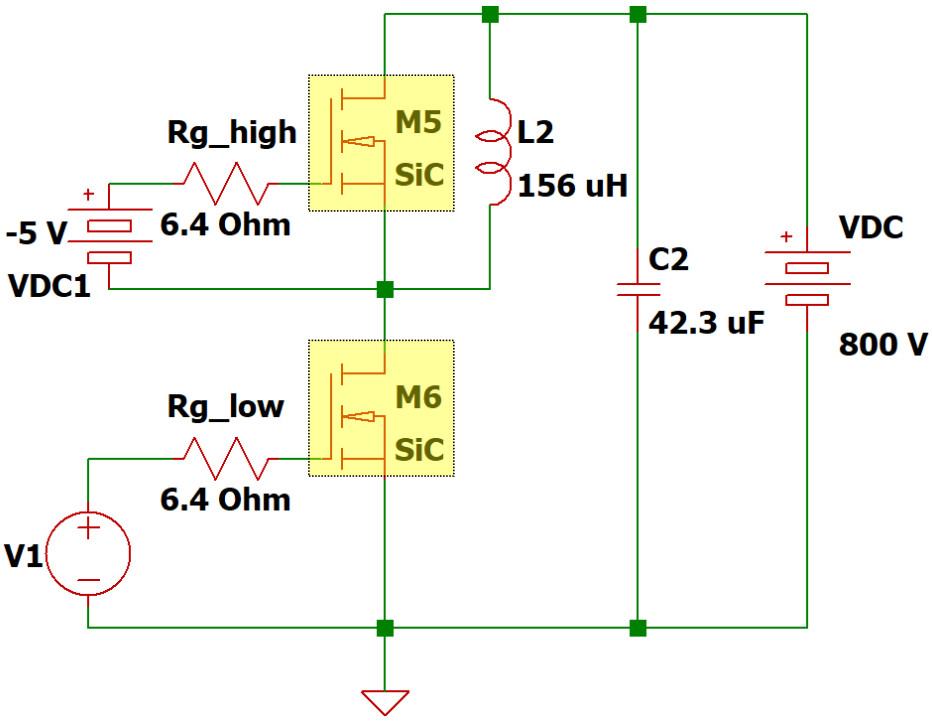


Fig. 9-6. Body diode reverse recovery test circuit from datasheet.

9.4. **Temperature scaling parameter extraction**

For a particular temperature, the isothermal model's parameter set can be extracted from the procedure described so far (Subsections 9.1- 9.3). During the extraction, temperature scaling parameters are kept at zero value. Once the parameter sets at different temperatures are extracted, any curve fitting tool can be used for relating the room temperature value of any particular parameter to the values at a higher temperature using the temperature scaling parameters and equations described in Chapter 5.

An alternative method is to use IC-CAP (or any similar software) to curve fit the higher temperature characteristics using the temperature scaling parameters. This is an efficient extraction technique. However, it requires a proprietary tool for extraction. Table 9-1 lists the extracted parameter set for C2M0045170D.

**Table 9-1. Extracted parameter set for C2M0045170D**

| Parameter | Description | Value<br>$y = f/r$ | Unit |
|---|---|---|---|
| $Vth0_{ly}$ | Low current threshold voltage at room temperature | 3.414 / 1.681 | V |
| $Vth0_{hy}$ | High current threshold voltage at room temperature | 7.361 / 7.361 | V |
| $\Theta 0_{ly}$ | Transverse electric field mobility factor at the low gate voltages at the room temperature | 0.1329 / 2.272 | $V^{-1}$ |
| $\Theta 0_{hy}$ | Transverse electric field mobility factor at the high gate voltages at the room temperature | 0.04948 / 0.04948 | $V^{-1}$ |
| $Kpl0_y$ | Saturation region transconductance parameter at low gate voltages at the room temperature | 3.568 / 27.01 | $A/V^2$ |
| $Kph0_y$ | Saturation region transconductance parameter at high gate voltages at the room temperature | 226.9 / 226.9 | $A/V^2$ |
| $Kfl0_y$ | Triode region transconductance parameter at low gate voltages at the room temperature | 2992 / 3624 | - |
| $Kfh0_y$ | Triode region transconductance parameter at high gate voltages at the room temperature | 998.8 / 998.8 | - |
| $pvf_l$ | Pinch-off parameter for low-gate voltage region | 0.7261 | - |
| $pvf_h$ | Pinch-off parameter for high-gate voltage region | 0.04821 | - |
| $\delta$ | Smoothing parameter | 1E-6 | - |
| ***rs0*** | Parasitic source resistance at the room temperature | 0.005663 | Ω |
| $rd0_y$ | Constant drain resistance for forward conduction at the room temperature | 0.009095 / 0.001838 | Ω |
| ***RDVD*** | Drain-dependency parameter of the drift resistance | 0.0003857 | $A^{-1}$ |
| ***RDVG1*** | First gate-dependency parameter of the drift resistance | 6.807 | Ω |
| ***RDVG2*** | Second gate-dependency parameter of the drift resistance | 840.3 | $V^{-1}$ |

**Table 9-2. Extracted parameter set for C2M0045170D (Cont.)**

| Parameter | Description | Value<br>*y= f /r* | Unit |
|---|---|---|---|
| ***a*** | Total active area | 0.1667 | $\mu m^2$ |
| ***nb*** | Doping in the drift region | 7.44E+16 | $cm^{-3}$ |
| $I_{leakage}0$ | Intrinsic leakage current at the room temperature | 1E-10 | A |
| $\tau_{leakage}$ | Constant drain resistance for forward conduction | 2.71E-06 | s |
| ***vbr0*** | Constant drain resistance for reverse conduction at the room temperature | 1780 | V |
| ***bvn*** | Exponential avalanche multiplication exponent | 0.6427 | - |
| ***Isbody*** | Diode saturation current | 1E-10 | A |
| ***vk10*** | The positive knee gate voltage at the room temperature | 3.209 | V |
| ***vk20*** | The negative knee gate voltage at the room temperature | 2.944 | V |
| $kvsg_10$ | Gate dependent body diode gain factor at the room temperature | 0.4649 | $V^{-1}$ |
| $kvsg_20$ | Gate dependent body diode gain factor for negative gate voltages at the room temperature | 0.8106 | V |
| ***ND0*** | Body diode ideality factor at the room temperature | 1.605 | - |
| ***rdiode0*** | The series resistance of the body diode at the room temperature | 0.03163 | Ω |
| ***rdiovgs0*** | Gate bias dependent conductivity modulation parameter at the room temperature | 0.02101 | $V^{-1}$ |
| $\tau 0$ | The lifetime of the minority carriers in the drift region at the room temperature | 1E-09 | s |
| ***TT0*** | Diffusion transit time at the room temperature | 2.914E-09 | s |
| ***cgsacc*** | Gate to source capacitance *at the accumulation state* | 2.888E-09 | F |
| ***cgsinv*** | Gate to source capacitance *at the inversion state* | 9.336E-09 | F |

**Table 9-3. Extracted parameter set for C2M0045170D (Cont.)**

| Parameter | Description | Value<br>*y= f /r* | Unit |
|---|---|---|---|
| ***vacc*** | Accumulation state onset voltage | 5.531 | V |
| ***vinv*** | Inversion state onset voltage | 3.414 | V |
| ***Gp*** | Doping gradian at the channel region | 0.3623 | $V^{-1}$ |
| ***vtd0*** | First gate drain overlap depletion threshold voltage | 0 | V |
| ***vtd1*** | Second gate drain overlap depletion threshold voltage | 6.5 | V |
| ***Cox0*** | Gate oxide capacitance | 1.543E-09 | F |
| ***Cox1*** | Initial constant capacitance at the onset of second depletion region | 3.802E-10 | F |
| ***Cgdmin*** | Constant capacitance at the high voltage region | 5.703E-12 | F |
| ***m*** | Junction grading coefficient | 0.7947 | - |
| ***wb*** | Metallurgical drift region width | 0.00015 | μm |
| ***agd*** | Gate length overlap active area | 0.0002272 | $\mu m^2$ |
| $\beta_y$ | Minimum threshold voltage at the high temperature | 1.302 / 0.5 | V |
| $\varphi_y$ | Slope adjusting parameter for the temperature-dependent threshold voltage | 0.003808 / 0.00875 | $°C^{-1}$ |
| $\alpha$***l*** | Slope adjusting parameter for *kpl* | 10 / 0.06858 | - |
| $\alpha$***h*** | Slope adjusting parameter for *kph* | 0.5309 / 0.5309 | - |
| ***rdtemp***$_y$ | Temperature coefficient of the drain resistance | 0.008514 / 0.01044 | - |
| ***rstemp***$_y$ | Temperature coefficient of the source resistance | 0.004847 / 0.004847 | - |
| $\theta$***ltemp***$_y$ | Temperature coefficient of the transverse electric field parameter | 0.1329 / 2.272 | - |

**Table 9-4. Extracted parameter set for C2M0045170D (Cont.)**

| Parameter | Description | Value<br>*y= f /r* | Unit |
|---|---|---|---|
| $\theta htemp_y$ | Temperature coefficient of the transverse electric field parameter | 0.04948 / 0.04948 | - |
| ***vbrtempco*** | Temperature coefficient of the breakdown voltage | 0.00148 | V °C$^{-1}$ |
| ***rdiodetempco*** | Temperature coefficient of the body diode resistance | 0.003797 | - |
| ***rdiodevgstemco*** | Temperature coefficient of the body diode's conduction modulation | 4.684 | - |
| $ND_{Tempco1}$ | Temperature coefficient of the forward voltage drop | 0.7685 | - |
| ***tautemp*** | Temperature coefficient of the carrier lifetime | 7E-10 | - |
| ***TTtemp*** | Temperature coefficient of the diffusion transit time | 1E-10 | - |

# Chapter 10. CONCLUSIONS AND FUTURE WORK

In this research, a physics-based compact model for a SiC power MOSFET that includes both the first and the third quadrant characteristics has been presented and validated. The model's uniqueness is to capture the body diode characteristics, including reverse recovery phenomena, without compromising the first quadrant characteristics' accuracy and convergence properties. Accurate and efficient third quadrant characteristics modeling is essential for circuit applications with synchronous rectification. Also, body diode modeling with reverse recovery allows accurate simulation of the circuit when the body diode is used as the freewheeling diode. Moreover, accurate gate-dependency modeling will enable circuit designers to think about more innovative approaches to utilize the power MOSFET's body diode. For the first time, this work included gate dependency of the input capacitance for a SiC power MOSFET model. The capacitance-voltage characteristics have been modeled in such a way that it accurately simulates the Miller capacitance at very low and high *Vds* region without using LUT approach. The model includes empirical expressions that capture the physical effect of the change in junction temperature on the device characteristics. In a world-first, the work simulates the temperature-dependent device characteristics up to 327°C with acceptable accuracy. The model's capability to accurately predict the switching characteristics at different junction temperatures has been validated with DPTs at different temperatures up to 200°C. A continuous test with a buck converter has been performed to validate the developed model's capability to predict a system's efficiency with self-heating. This work also describes a new parameter extraction procedure that only relies on the data commonly available in the commercial devices' datasheets for the users' ease. The developed extraction procedure only relies on the output characteristics, removing the confusion caused by the mismatch

between the DC transfer curve and the DC output curves, which is prevalent in many datasheets. The model's convergence properties have been validated by simulating different kinds of topologies, ensuring the usefulness of the model for broader power electronics circuit designs. Also, a comparison with a previous model [8] proves the presented model's utility in terms of accuracy and efficiency, despite adding computationally expensive third quadrant features. Hence, the presented electro-thermal model contributes to more accurate and efficient simulation of all kinds of power converters.

For parameter extraction, the model heavily depends on a commercial software IC-CAP. But open-sourced Python can be used to automate this procedure. Open-sourced simulators like LTspice can be used instead of proprietary simulators like Saber or Spectre. This will help to increase the outreach of the model. An extraction procedure using free curve fitting software like Python and open-sourced simulator like LTspice will surely increase the outreach of the developed model.

The work can be expanded for module-level modeling with the discrepancies among the multiple devices. The model parameters can be adjusted according to the predicted variation. For example, in the datasheet, the minimum, maximum, and typical values of the Threshold voltage are given. The threshold voltage for different devices in a circuit schematic can be assigned different values. This will result in different turn-on and turn-off for different devices within the circuit simulation. Hence current sharing mechanism can be predicted from the simulation. Similarly, the variation of $Rds_{on}$ and interelectrode capacitances can be also easily incorporated with the variation in the parameter set. So the model can be an excellent tool for analyzing device paralleling in a power module.

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# APPENDIX

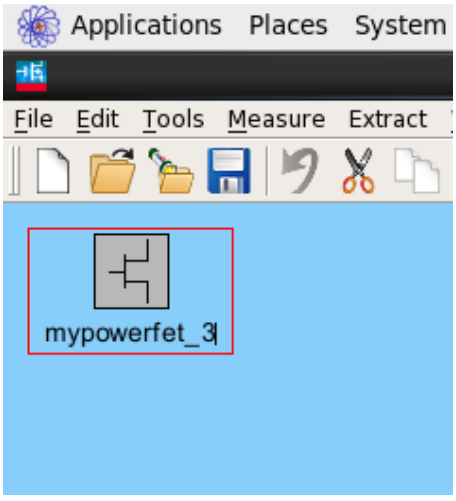
## Appendix-1: IC-CAP for Parameter Extraction

IC-CAP is a commercial software from Keysight Technologies©. The IC industries use it to extract different device models' parameters. Also, the tool is used for characterization, simulation, optimization, and statistical analysis. In this appendix, a step-by-step instruction is documented on using IC-CAP for extracting a parameter set of the developed SiC power MOSFET.

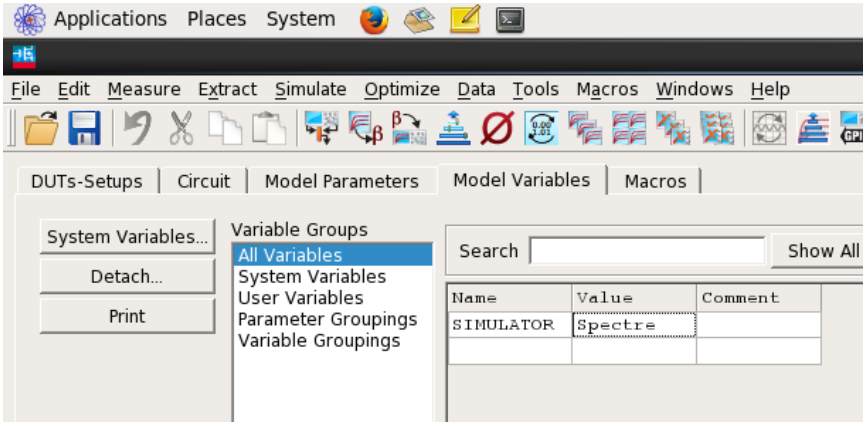
### A. Including a user-defined model

IC-CAP comes with various in-built models. These models can be called in the traditional net-list format. But a user-defined model, like the model developed here, needs to be included with an 'ahdl_include' statement. This is done in the circuit tab of a newly added module. The steps are shown below:

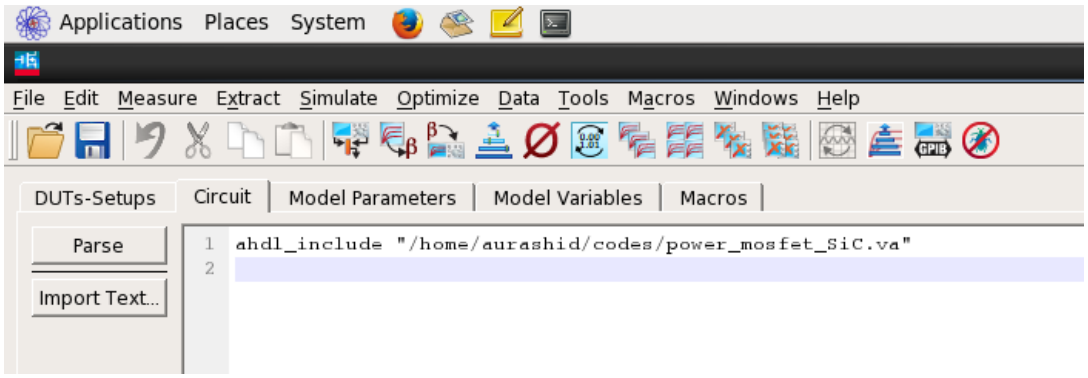
a. Open IC-CAP. Go to open → new. Rename the file suitably.



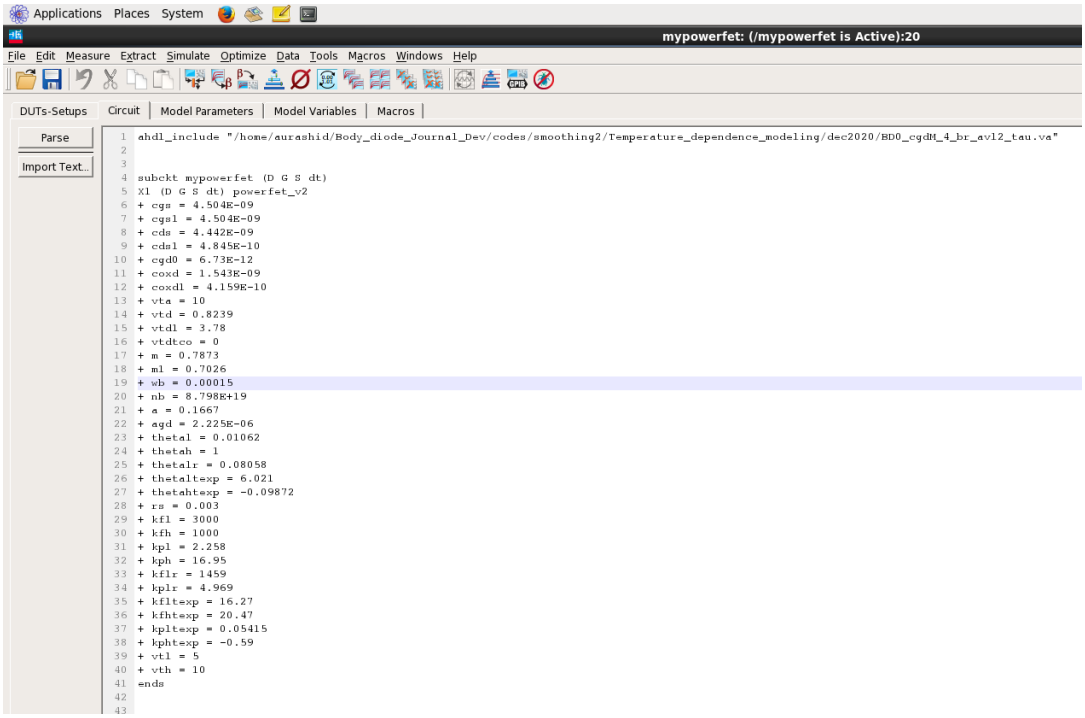
b. Open the module. Go to the Model Variables tab. Add ‘Spectre’ or ‘spmodeads’ as the Simulator. HSPICE, PSPICE can also be used. But then netlist has to be written with the corresponding format.




c. Go to the circuit tab. Add the Verilog-A source file of the developed model with the ahdl_include statement.



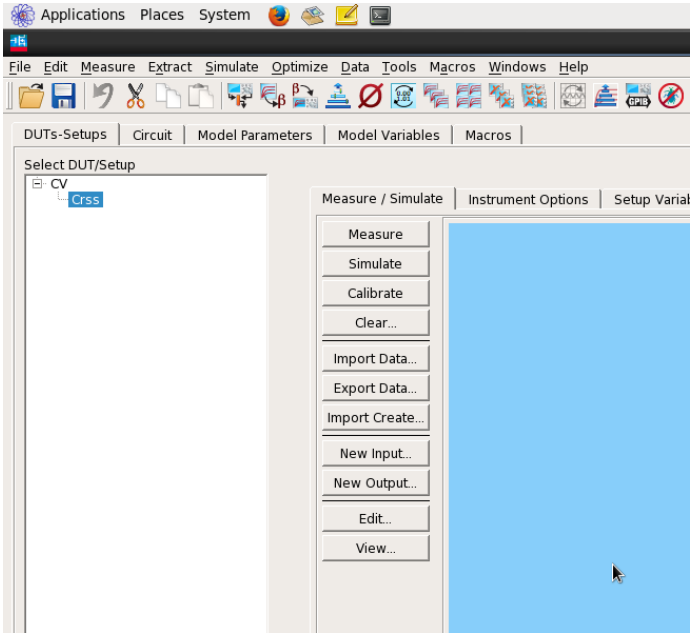

d. The model parameters are included in the module as a subcircuit. Add the necessary model parameters in the following format.




## B. Adding DUT for a particular simulation

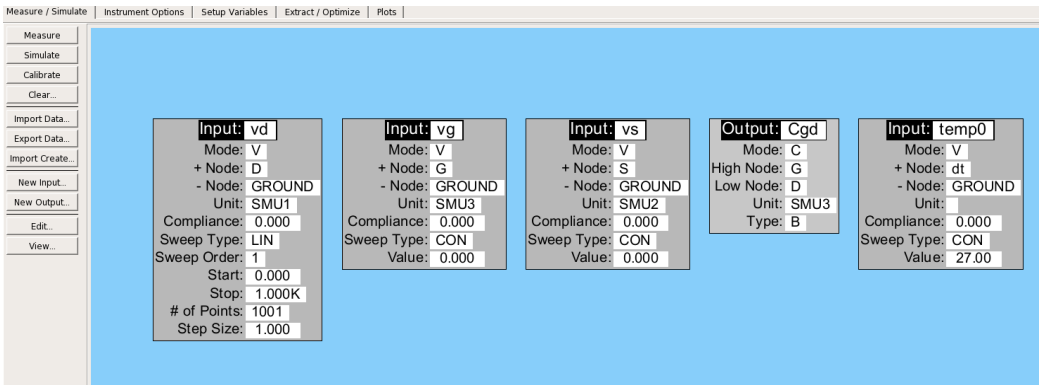
This section describes how to add a DUT for a particular type of simulation. We will have 4 kinds of DUT. For C-V extraction, for I-V extraction, for temperature parameters extraction, and for double pulse test (DPT) simulation.

a. Go to DUTs set-up tab and click on the add button at the bottom.

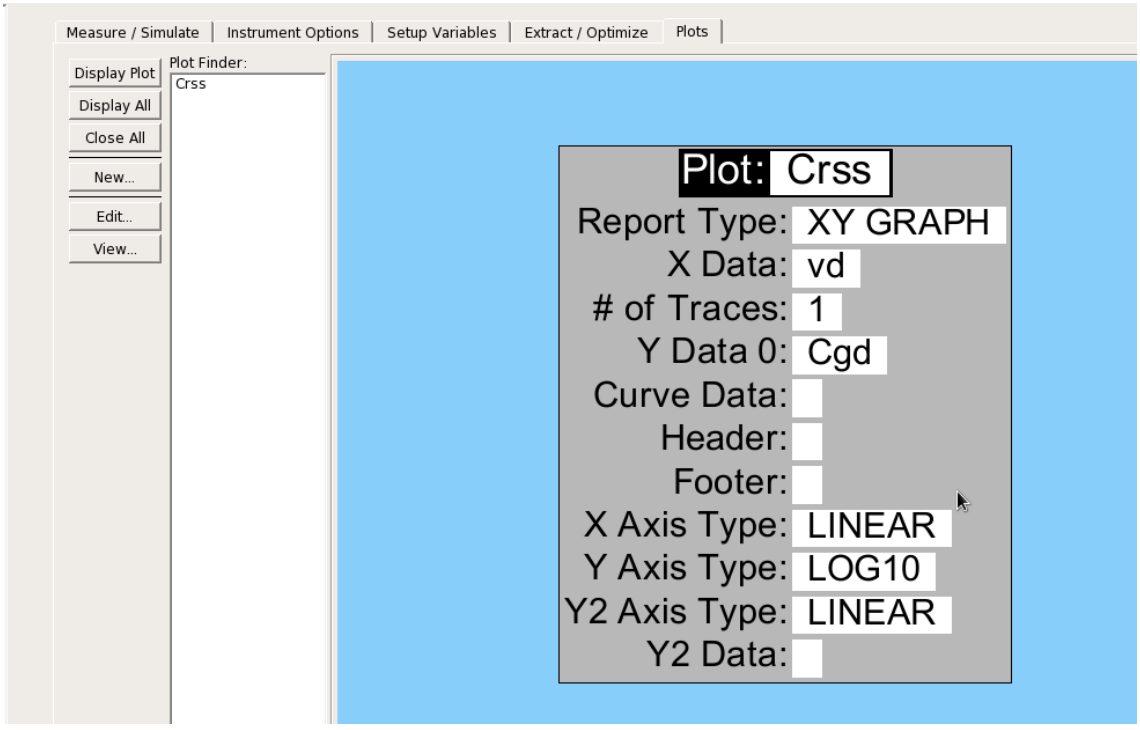




b. Add a DUT named C-V. Then click on the add button again and add a new set-up under C-V. In the set-up click on the ‘New input’. Add Vd, Vg, Vs, dt, as inputs. In the C-V measurement, Vds is swept from 0 to Vmax. Vgs remain zero. Vs is treated as the reference voltage. dt or the temperature node is assigned the room temperature value that is 27°C.

c. Then click ‘New Output’ button and add the output quantity we want to see. Here we are measuring Crss. So we need the capacitance across gate and drain. So add Cgd.




d. Then go to the plot tab. Click ‘New’. Give the plot name. Select “XY graph”. Put the name of x-axis data and y axis data. Select linear or Log10 graph.

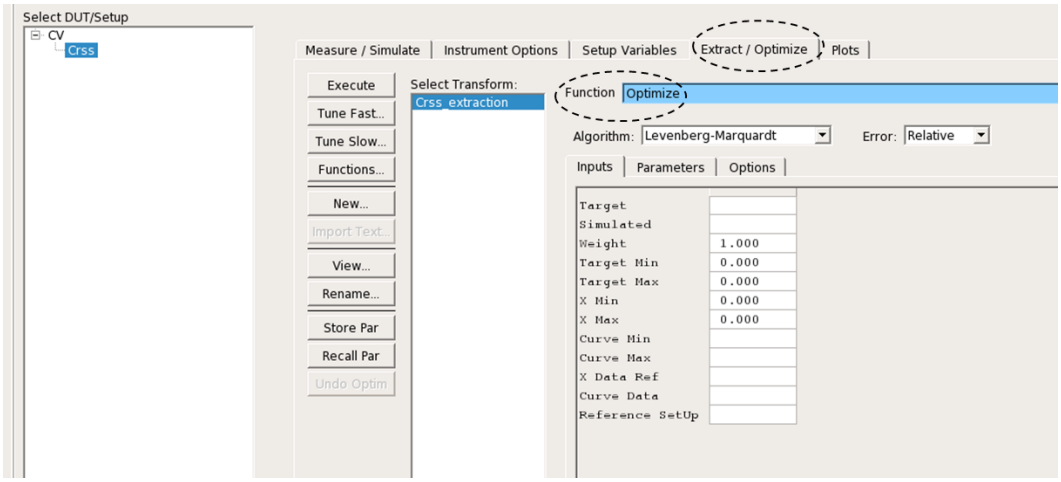



e. Simulate the setup with ‘Simulate’ button in the ‘Measure/simulate’ tab. Then export data to a folder. A .mdl file will created. Open it and put the measured data there. The measured data needs to be in equal space format. Use matlab to make the measured data equally spaced. Now get back to the module’s ‘Measure/Simulate’ tab and click import data. It

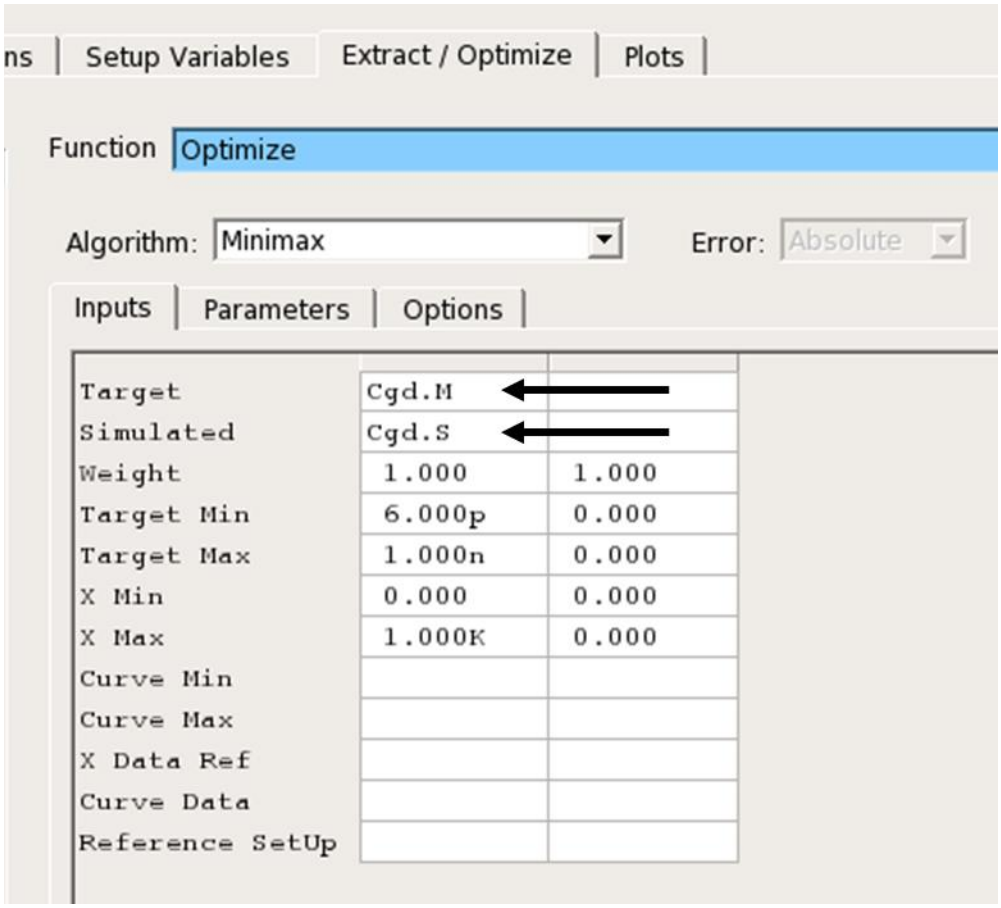
should automatically select the exported data file. Now go to ‘Plots’ tab. Select the plot and click ‘display’. It will show the overlay of measured and simulated data.

## C. Parameter extraction

a. Go to the ‘Extract/Optimize’ tab. Click on the ‘New’ button. Name it accordingly. Now write ‘Optimize’ in the ‘Function’ field.

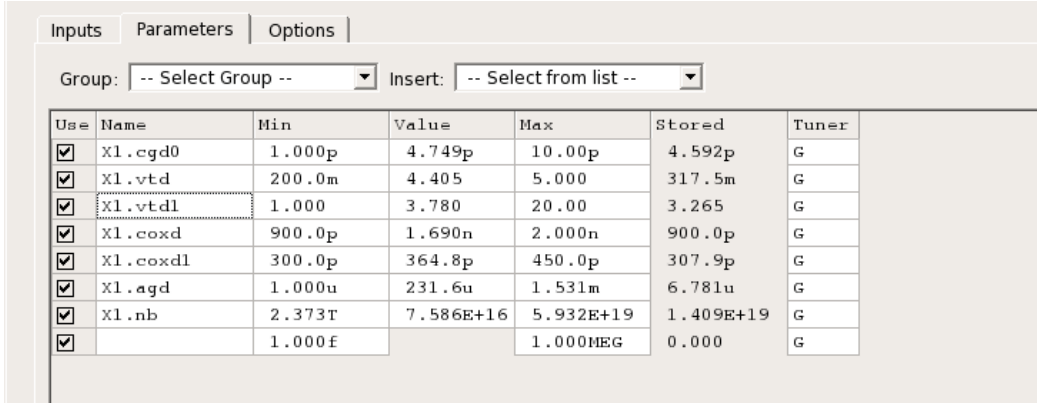



b. In the ‘Inputs’ tab’s ‘Target’ field, write the measured data. In this case it is ‘Cgd.M’. Give corresponding simulated term “Cgd.S”. For faster extraction, give the minimum and maximum values of the measured data. If simulated results only need to fit a specific range, give the minimum and maximum of that range. Also, give the corresponding x-axis range.

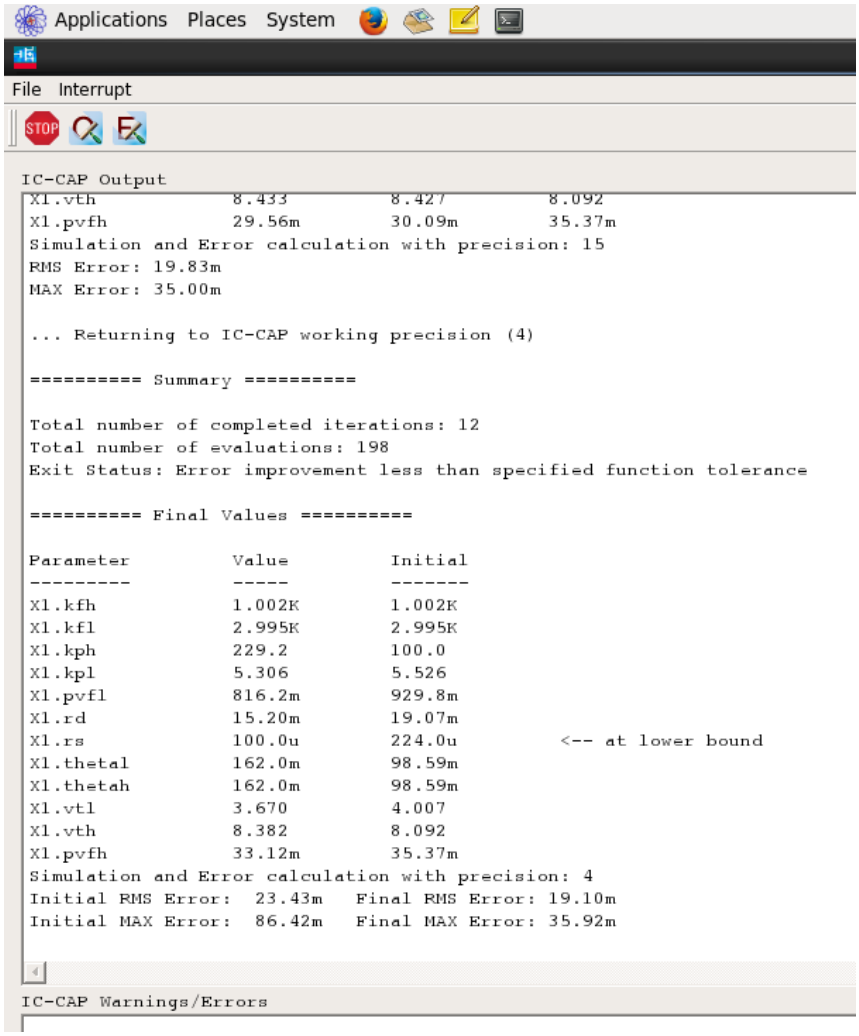



c. The ‘Algorithm’ should be either ‘Minimax’ or ‘Gradient’.

d. In the ‘Parameters’ tab, put the model parameter name related to simulated characteristics. Also, give a limited range around the probable values for each parameter. At first, give the range around the default value. This range needs to be updated several times during the extraction to get the best fit.



e. Now ‘Execute’ the extraction. IC-CAP will automatically try to fit the simulated results with the measured data by changing the parameter values within the given range. It will give the RMS error and maximum error after each iteration. Once it gets the best fit, the process will end and give an extracted set of parameters. Since parameters are given a limited range, changing the range might give a better fit. So several such attempts are usually required.

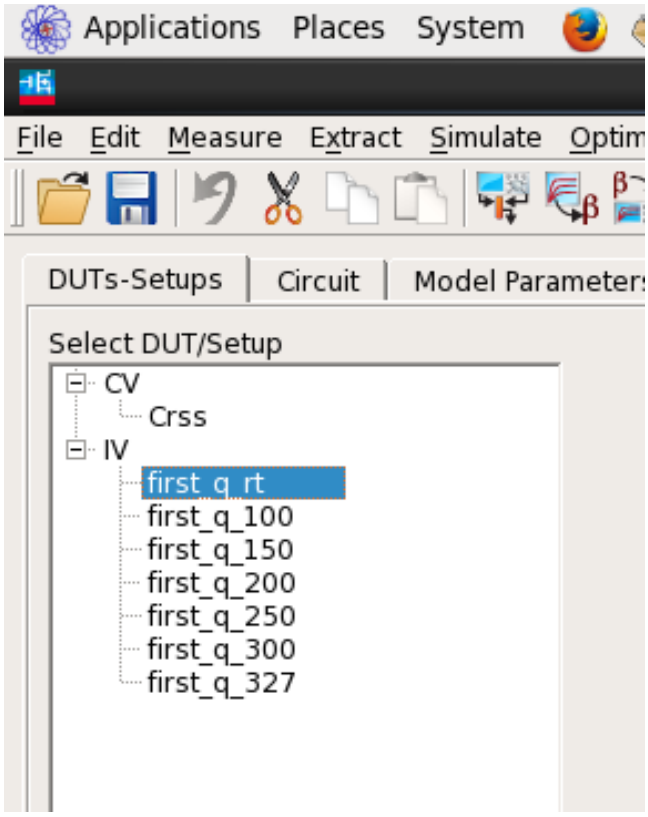



f. The procedure described so far can be used for extracting all the parameters for an isothermal case. Set the dt node value to the measurement temperature and make all the temperature co-efficients zero.

## D. Temperature scaling

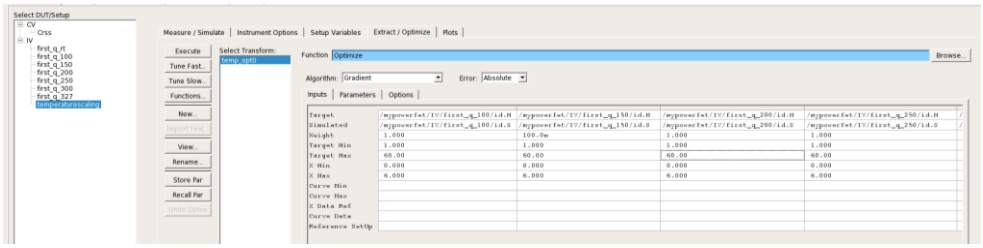
For temperature scaling, IC-CAP needs to fit multiple simulation results to the corresponding measured data. So the extraction procedure nees a little modification.

a. Make a similar measurement set-up for each temperature. Here the example of the first quadrant output characteristic is given. Only extract the parameter set for the room temperature one; keeping all the temperature scaling parameters' values zero.

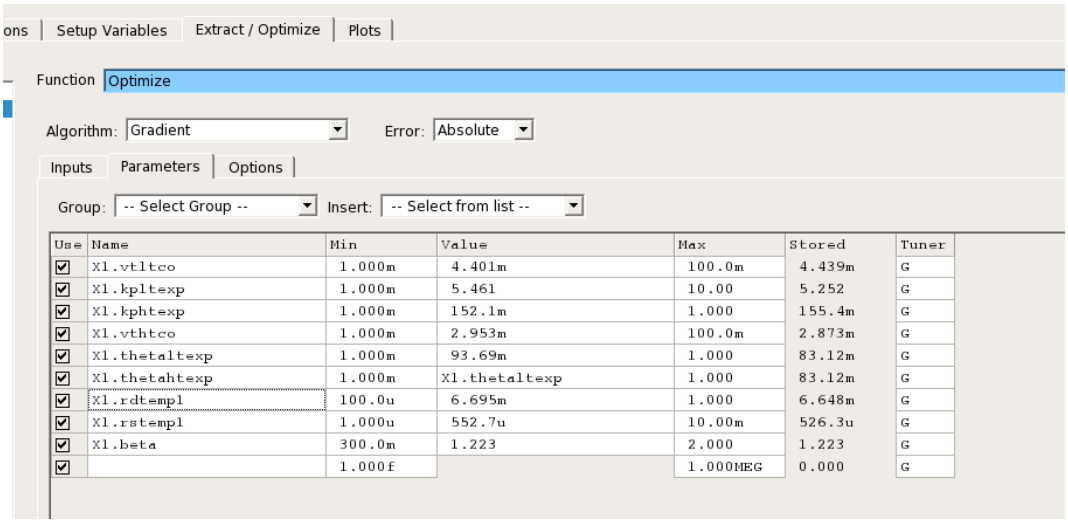



b. Open another set-up called temperature scaling. Giving any particular name is not important. But just to identify the purpose of any set-up.

c. Go to the 'Extract/optimize' tab. Add all the high-temperature test set-ups one by one in the columns. Give necessary x-axis and y-axis range. If any particular temperature is less critical than others, give its 'weight' less than the others.



d. Go to the ‘Parameters’ tab and add the necessary temperature scaling parameter related to the first quadrant I-V characteristics. Then execute. The simulation will be significantly slower than any single set-up simulation.




| Use | Name | Min | Value | Max | Stored | Tuner |
|---|---|---|---|---|---|---|
| ☑ | X1.vtltco | 1.000m | 4.401m | 100.0m | 4.439m | G |
| ☑ | X1.kpltexp | 1.000m | 5.461 | 10.00 | 5.252 | G |
| ☑ | X1.kphtexp | 1.000m | 152.1m | 1.000 | 155.4m | G |
| ☑ | X1.vthtco | 1.000m | 2.953m | 100.0m | 2.873m | G |
| ☑ | X1.thetaltexp | 1.000m | 93.69m | 1.000 | 83.12m | G |
| ☑ | X1.thetahtexp | 1.000m | X1.thetaltexp | 1.000 | 83.12m | G |
| ☑ | X1.rdtempl | 100.0u | 6.695m | 1.000 | 6.648m | G |
| ☑ | X1.rstempl | 1.000u | 552.7u | 10.00m | 526.3u | G |
| ☑ | X1.beta | 300.0m | 1.223 | 2.000 | 1.223 | G |
| ☑ | | 1.000f | | 1.000MEG | 0.000 | G |

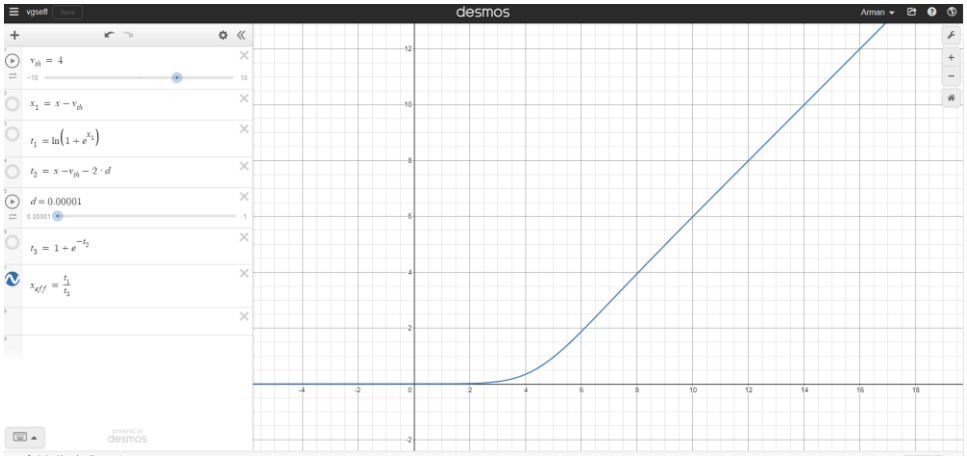
## Appendix-2: Thought Process for Modeling

Any modeling activity requires a lot of selection process among different alternatives. Modeling of the SiC power MOSFET is not different. There are two (usually) opposing standards for making any selection in modeling activity: Accuracy and Efficiency. Some of the key selections and the reasoning behind those selections are listed below:

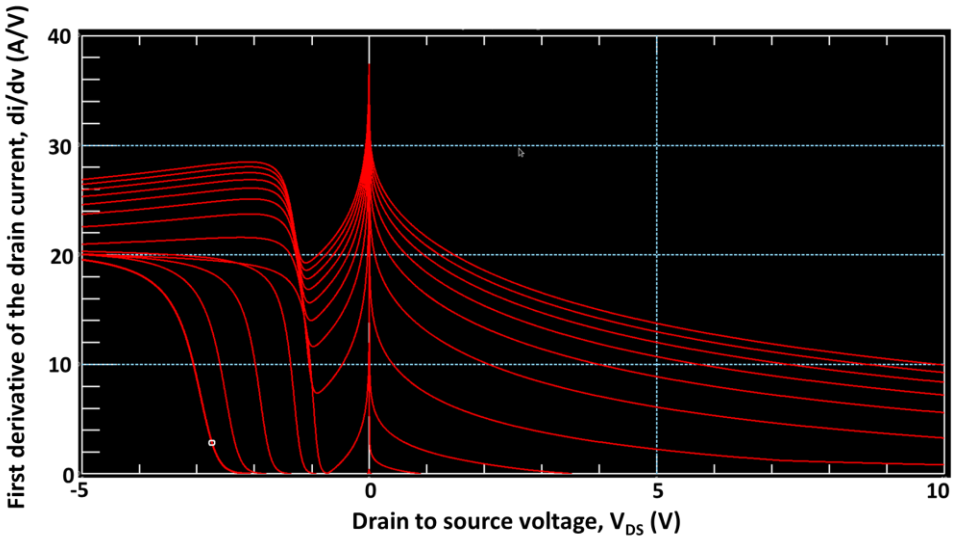
a. **Smoothing approach instead of conditional statement based approach:** Conditional statements or Conditionals always slows down the execution of a code. Conditionals are essential for writing up any code or models. But the presence of Conditionals in the analog section of the model slows down the code a lot. So it is crucial to reduce the number of Conditionals in the current and charge equations. These equations are iteratively updated during simulation. Instead 'Smoothing' approach should be used. In this approach, the input variables (terminal voltages, temperature) are made weighted functions depending on the area of operation. For example, take eq. (22).

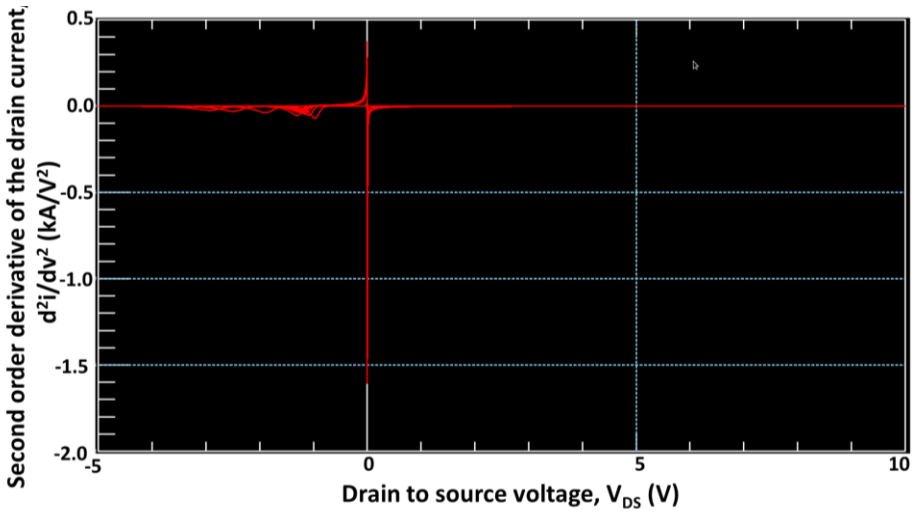
$$Vgs_{effxr} = \frac{\ln(1 + e^{Vgs - V_{thxr\_t}})}{1 + e^{-(Vgs - V_{thxr\_t} - 2\partial)}} \tag{22}$$

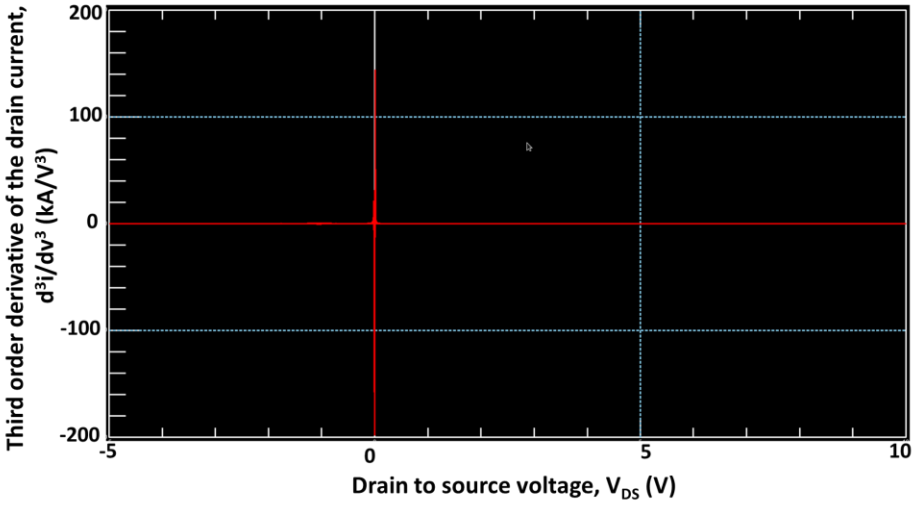
Here, the effective gate voltage ($Vgs_{effxr}$) is a weighted function of the gate voltage ($Vgs$). For $Vgs \leq V_{thxr\_t}$ effective gate voltage is a very small constant value close to 2δ. When $Vgs > V_{thxr\_t}$ effective gate voltage is a linear function of $Vgs$. This takes care of the on-state and off-state dependency of the channel current instead of using conditional statements. It can be seen in the following picture:




As a result of this modification, the higher order derivatives are continuous for this model. This can be seen in the pictures given below:






**b. Adding virtual nodes:**

The number of nodes determines the size of the solution matrix during the simulation time. External nodes provide input signals. As a result, the solution of the matrix becomes relatively easier. In the case of the internal nodes, there are no additional input conditions. So the solution takes a longer time.

Virtual nodes are a kind of internal nodes with indirect branch assignments. An example of indirect branch assignments can be:

V(n): V(p) = = 0;

It means that the node ‘n’ should be driven as a voltage source, and its magnitude must be such that it satisfies the condition of the voltage of node ‘p’ being 0. Here node ‘p’ is a virtual node. This node is not driven by any current, rather its assigned voltage is variable depending on the other factors.

Virtual nodes are iterative because it needs to fulfill certain conditions updated on the other nodes' bias conditions. As a result, the solution of the matrix takes a lot longer time. So it is desired to avoid ‘virtual’ nodes if possible.

But modeling some device physics, there is no alternative to using virtual nodes. For example, reverse recovery current ($I_{rr}$) depends on recombining charge in the drift region. Also, the amount of charge recombination depends on the amount of existing charge. So the amount of existing charge is a virtual node that satisfies the condition of $I_{bdiode}$ = = $I_{rr}$. Hence, a virtual node was included in the model despite having the penalty of the longer simulation time. In the case of the conduction modulation, a bias-dependent expression satisfactorily fulfill the need. So an additional virtual node was avoided.

**c. Making bias dependent resistances temperature-dependent:**

In a temperature-scaled self-heating enabled model, temperature works as a terminal variable just like a terminal voltage bias. It updates after each solution of the matrix. The parameters are made temperature-dependent with their respective temperature coefficients. With the update of the temperature, the temperature-dependent parameters are updated. In the case of resistances, they play as a branch element in the model. It is necessary to make them temperature-dependent because of the device

physics. Some resistances are also bias-dependent due to changes in the carrier concentrations with bias—for example, $R_A$, $R_{jfet}$, $R_{diode}$. These resistances are also temperature-dependent. However, if the resistances are both bias and temperature-dependent, it takes the simulator more time to converge.

On the other hand, these resistances might be guessed at very high values during the solution, making the convergence even more difficult due to branch current relation. So it is advisable to avoid temperature dependency of the bias-dependent resistance part. In this model, the temperature dependencies of the resistances are modeled with the temperature dependency of the constant resistances.