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Gating Methods for High-Voltage Silicon Carbide Power MOSFETs

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Gating Methods for High-Voltage Silicon Carbide Power MOSFETs

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ABSTRACT

The objective of this thesis is to assess the challenges associated with driving Silicon Carbide (SiC) power devices, and to compare the potential gate drive methods for these devices which address those challenges. SiC power devices present many benefits that make them suitable for next generation automotive, power utility grid, and energy management applications. High efficiency, increased power density, and reliability at high-temperatures are some of the main benefits of SiC technology. However, the many challenges associated with these devices have prevented their adoption into industry applications. The argument is made in this thesis that the gate driver is a key component in providing proper control to enable the reliable and high performance of these devices. Thus, as the main control mechanism, the gate driver topology should be carefully considered in the design of SiC-based converters.

In this thesis, the main issues and challenges of operating SiC power devices will be explored, and the common mitigation techniques will be discussed. Next, the switching operation of the SiC power MOSFET and the loss analysis will be performed for the voltage-mode and current-mode drivers. Additionally, a solution incorporating a multi-level voltage-mode driver is proposed as an alternative to the other methods. The comparison of these techniques and their ability mitigate EMI and other negative consequences of fast-switching while minimizing switching energy losses will be analyzed. This is done through the comparison of the methods based on the analytical approach, through the use of simulations using device models, and through experimentation. The multi-level driver is found to be good alternative to the conventional voltage-mode driver, and is thus assessed in detail in the experiments. Finally, the considerations for the experimental setup using the double pulse test (DPT) is also discussed. Conclusions are made based on the performance of the device under multi-level turn-off, and future considerations for enabling the next generation high-voltage SiC MOSFETs are discussed.

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DEDICATION

I would like to dedicate this to my parents for their continuous support and encouragement and for making me the person I am today. Thank you for giving me courage to pursue my dreams.

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CHAPTER 1

INTRODUCTION

1.1 Motivation for this Research

Silicon Carbide (SiC) power semiconductor devices are quickly gaining interest due to the many benefits they provide, enabling higher power density and efficiency. From a materials standpoint, SiC devices are set apart due to their properties as a wide bandgap semiconductor, referring to the distance between the valence and conduction bands. Using this material in a power device enables operation at high voltages, temperatures and frequency. SiC MOSFETs are available on the market in voltages ranging from 900 V to 1700 V [1, 2], and devices in the range of 10 kV to 15 kV have been fabricated and characterized in the literature [3, 4, 5]. Through the use of these devices, medium-voltage (MV) converters may become smaller because fewer devices are required. Additionally, the overall size of the converter can be further reduced by switching at higher frequencies resulting in smaller passive components.

SiC power devices provide many system-level benefits for a variety of applications. However, due to adverse side-effects, which were not previously a concern for power electronics designers, their implementation has to be carefully considered to mitigate those side-effects. For example, SiC devices can switch faster than any other device of its power class, defined by its *dv/dt* and *di/dt*, as shown in Figure 1.1, where *dv/dt* is the change in drain-source voltage and *di/dt* is the change in drain current. However, with voltage transitions up to, and exceeding, 80 V/ns, common-mode noise and failure of control circuitry can result [5]. The drain current transitions, or *di/dt*, are also very high, and result in voltage overshoot and resonant effects that can overstress the device or inhibit its performance.

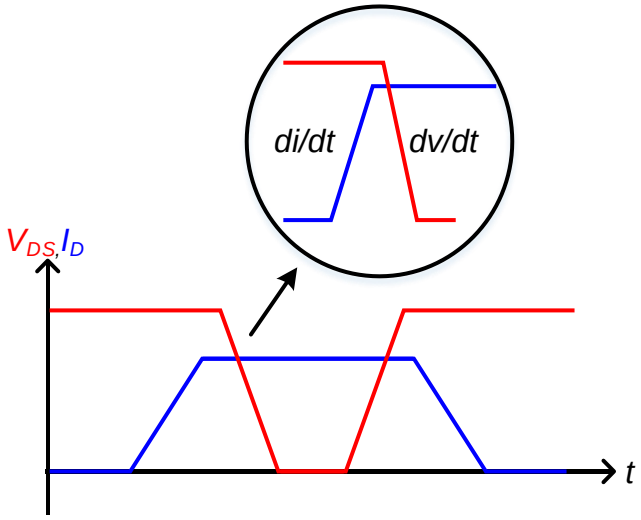

Figure 1.1. dv/dt and di/dt of a semiconductor device.

As shown in Figure 1.1, the *dv/dt* of the device is proportional to the voltage level and rise or fall times. This means as higher voltage devices become available, the *dv/dt* problem will be even more excessive. The impact of the *di/dt* is dependent on the parasitic inductances of the circuit, which can be moderated, but are unavoidable. To reduce detrimental effects due to parasitics, alternate device packaging techniques and board layout optimization have been employed. These solutions require additional design time and resources to implement, and can unnecessarily increase the complexity of the system. Thus, it is the goal of this thesis to provide solutions from the perspective of the gate driver. The optimization of performance and mitigation techniques is a key factor in the determination of the best gate driver for a specific application. This introduction discusses the benefits of SiC power devices to provide an understanding of why these devices are desirable, and why the gate driver is of significant importance in the converter design.

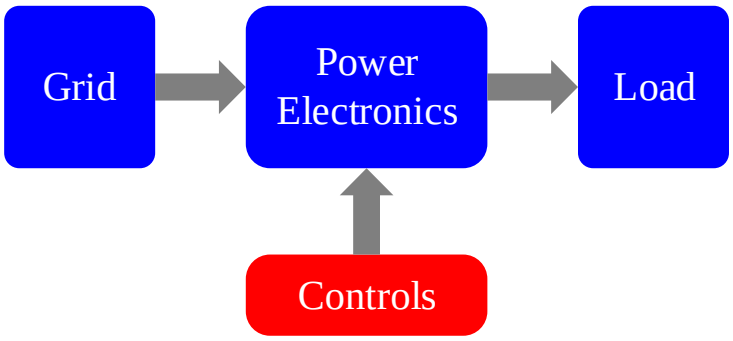

Figure 1.2. Power electronics as interfaces.

1.1.1 Power Semiconductor Devices

Power electronics circuits enable the conversion of power from one form to another in a variety of applications, ranging from electric vehicles to energy storage for the home. The grid is used to distribute power to loads ranging from residential to commercial, requiring either ac or dc power with various specifications. Thus, one of the main purposes of power electronics is to serve as the interface between the grid power and the end equipment, as shown in Figure 1.2.

These power electronics systems come in a variety of forms with regards to circuit topology and controls. Switch mode power converters are used in many applications to provide maximum control over the conversion process through the use of power semiconductor devices. These devices are the controllable switches that allow the designer to optimize the performance of the converter based on the switching scheme. The gate driver serves as the main interface between the

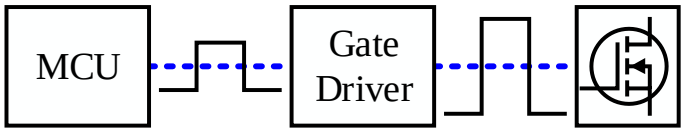

Figure 1.3. Gate driver signaling.

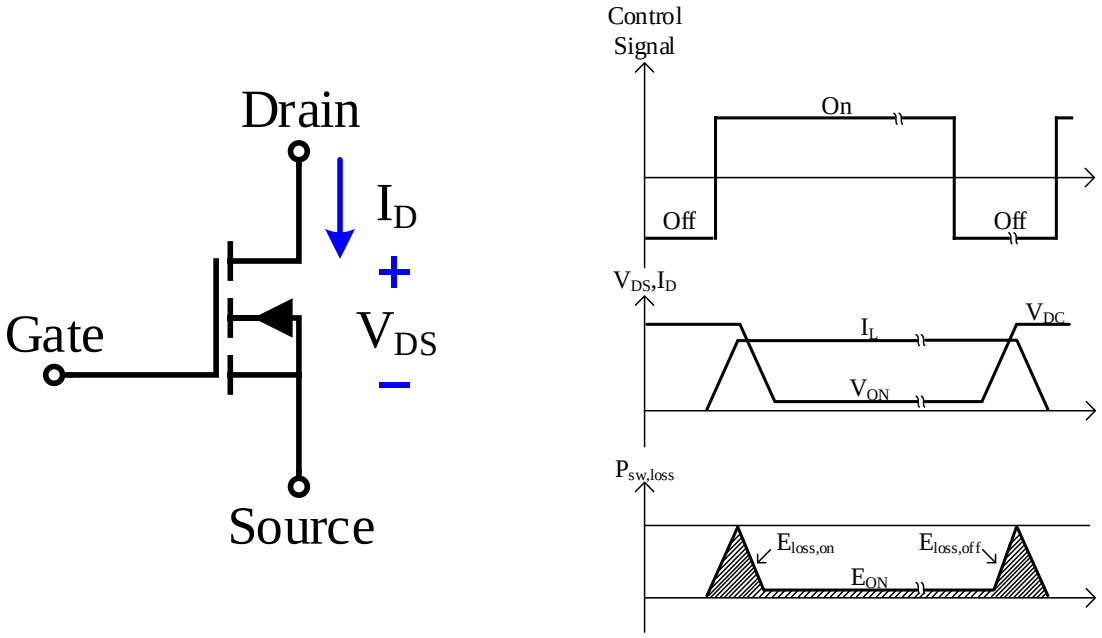

Figure 1.4. MOSFET switching waveforms.

designer's control algorithm and the switching device itself. As shown in Figure 1.3, the gate driver receives a control signal from the microcontroller unit (MCU) and converts it into a signal powerful enough to drive the semiconductor device, a MOSFET in this case.

There are a variety of gate drivers available on the market, all with the single goal of driving the power device. These drivers vary in drive strengths, protection functions, and other features. The selection of the gate driver is dependent on the power device being driven, and must provide sufficient drive strength to reduce the switching losses of the device. Figure 1.4 describes the basic switching process of a MOSFET and the consequence of power and energy losses.

When the signal is high, the device begins to conduct, and the drain current, I_D, rises while the drain-source voltage, V_{DS}, falls. During the on-state, V_{DS} will be close to 0 V and I_D will be at the maximum load current value. When the control signal is low the device becomes an open-circuit, and V_{DS} rises to the maximum voltage and I_D falls to 0 A. The switching power losses,

$P_{sw,loss}$, are an unavoidable consequence of switching a power device under hard-switching conditions. In an ideal case, the control signal has an infinite slope, resulting in the fast transition of the voltage across the device and current through the device. This is not physically realized due to various parasitic components affecting the speed of the driving signal, contributing more to the switching power losses shown in Figure 1.4. These losses translate into energy losses over time, which is the area under the waveform of $P_{sw,loss}$. The total switching losses of a particular converter are proportional to these energy losses, $E_{sw,loss}$, and the switching frequency. Fortunately, in recent years, WBG devices have been developed and provide switching performance as close to the ideal case than ever before. These devices switch at very fast rates, have lower conduction losses (E_{ON}), and have high breakdown voltages. Additionally, these devices have large thermal conductivity, allowing them to operate at higher temperatures. Comparisons of some of the main WBG devices versus Si devices can be found in [6]. Table 1.1 shows a comparison of some key characteristics.

Table 1.1. Comparison of SiC and Si power devices [1, 7].

Type				SiC MOSFET				Si BiMOSFET			
Manufacturer				CREE				IXYS			
Part #				C2M0045170D				IXBH42N170			
Voltage				1700 V				1700 V			
Max T_j				150 °C				150 °C			
Current (25 °C)				72 A				80 A			
$V_{DS(on)}$ or $V_{CE(sat)}$				~2 V				2.7 V			
V_F				4.1 V				2.8 V			
Internal Gate Resistance ($R_{G,int}$)				1.3 Ω				N/A			
Total Gate Charge				188 nC				188 nC			
t_{rise}	t_{fall}	$t_{delay(on)}$	$t_{delay(off)}$	20 ns	18 ns	65 ns	48 ns	188 ns	740 ns	36 ns	330 ns

As shown in the table, one advantage that the SiC device has over the Si device is the switching speed, having a turn-off time 41 times smaller. This results in lower energy losses, i.e. total switching losses. Additionally, the conduction losses for the SiC MOSFET are smaller, as it has a smaller on-state voltage versus the Si device's saturation voltage.

1.1.2 Applications for Wide-Band-Gap Power Devices

There are many power electronics systems that can benefit from the performance provided by SiC MOSFETs. For example, in hybrid electric vehicles (HEVs), both the inverter and the dc/dc converter operate in elevated temperatures, so the switching devices must be effective at these temperatures and have low on-resistance to reduce losses [8]. In [9], a comparison of dc/dc converters using Si versus SiC devices showed that the converter with SiC devices operating at 150 kHz still achieved higher efficiency than the Si converter at 20 kHz. That is a substantial achievement because switching losses increase linearly with the switching frequency, thus this demonstrates the exceptional benefits of SiC devices. The increase of frequency resulted in smaller passive components, such as the dc capacitor and choke inductor, reducing the total system volume and weight. Another challenge associated with vehicular converters is thermal management, and its contribution to the system's size and weight. Thus, it was shown that a 55 kW traction inverter drive using SiC devices allowed for the use of air cooling to significantly reduce the price in comparison to a liquid cooling system, all while maintaining similar size to that of the Si converter [10].

The Modular Multilevel Converter (MMC) is also a prime candidate for the utilization of high-voltage SiC devices [11]. The size and control complexity can be reduced by using fewer devices to achieve the high-voltage connection to the grid. It is expected that the losses will be reduced by using these devices, as opposed to Si. Using the MMC, battery energy storage can be

connected to the grid to enable additional energy in the case of grid failure or misoperation and provides the interface to recharge the batteries. With devices such as SiC MOSFETs that can operate at high voltage and high switching frequencies, the bulky 60 Hz line transformer can be replaced with a high-frequency transformer for galvanic isolation, reducing the size of the overall system. However, there are challenges with this implementation to ensure reliable operation of the SiC devices due to the complexity of the circuit and control. As will be discussed later, these challenges are made even more problematic because of SiC's very low short-circuit withstand time (SCWT), as compared to Si IGBTs.

Devices of lower switching speeds have typically been used in medium-voltage (MV) applications. These devices, such as gate turn-off thyristors (GTOs) and integrated gate-commutated thyristors (IGCTs), have high breakdown voltages at which the Si IGBT cannot reach. However, there is potential for SiC in these grid and utility applications due to the development of devices with 10 kV and 15 kV blocking voltages and fast switching speeds. For example, a solid-state transformer (SST) and grid-tied converter design utilizing 10 kV SiC MOSFETs is presented in [12]. The development of these converters are primarily focused on reducing the size of the typical 60 Hz transformer and increasing the efficiency while maintaining the galvanic isolation between the grid and distribution voltages. This converter includes the front-end converter (FEC), the dual active bridge (DAB), and low-voltage side converters. The FEC is connected to the 3-phase, 13.8 kV distribution grid, providing a voltage of 22 kV to the input of the DAB, generating a voltage of 11 kV across each device with an efficiency of 98% [12].

Such research shows the remarkable benefits that make SiC devices suitable for these high-temperature and high-voltage systems, yet, they are still not utilized widely in industry. The challenges associated with SiC devices have prevented their immediate adoption into industry

applications, but various solutions are being investigated throughout both industry and academia. Some of the main challenges are briefly described in the next section.

1.1.3 Challenges of Implementing SiC MOSFETs

Along with the many benefits associated with SiC power devices are some significant challenges that designers must anticipate. In an ideal case, SiC devices could be directly interchanged with their Si counterparts with the same control scheme and circuitry, with only the positive performance of SiC altering the system; however, this is not the case. This section serves as an introduction to some of the main challenges that come with using SiC MOSFETs.

There are many consequences due to the fast switching speeds of SiC, i.e. large *dv/dt* and *di/dt*. The parasitic circuit components, both inductive and capacitive, interact with these transitions and result in undesired voltages and currents derived from the following relationships:

$$V_{ind} = L * \frac{di}{dt} \quad (1)$$

and

$$I_{cap} = C * \frac{dv}{dt} \quad (2)$$

The parasitic inductances, as shown in Figure 1.5, include the internal device inductance from bond wires and the trace inductance of the circuit. These gate, source, and drain inductances (L_G, L_S, and L_D) will cause reduced driver strength and voltage spikes across the device.

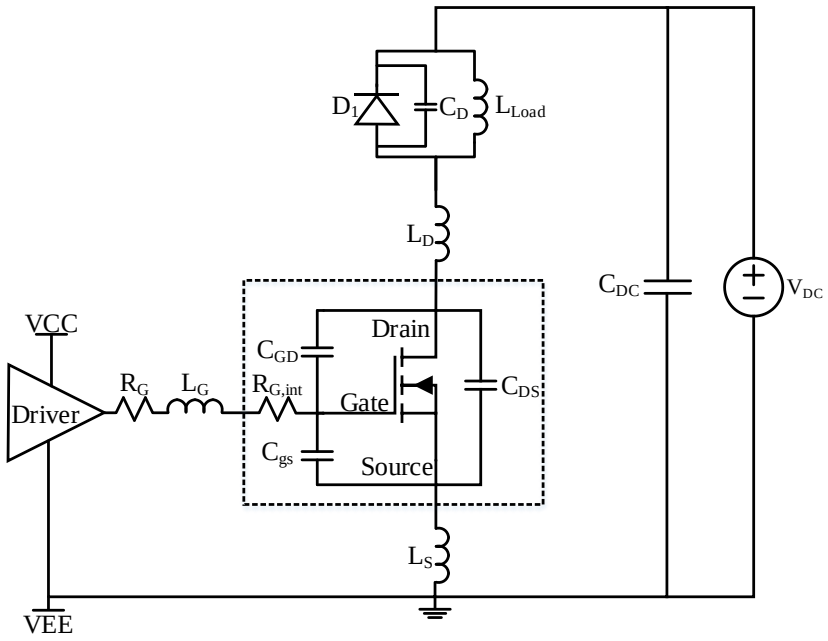

Figure 1.5. Parasitic model of a MOSFET switching circuit with a clamped inductive load.

The main capacitive elements of the circuit include the internal capacitors of the MOSFET, C_{GD}, C_{GS}, and C_{DS}, which prevent the device from acting as an ideal switch. The gate-to-drain capacitor, C_{GD} (Miller capacitance) also acts as a path for current to flow through the gate, causing false turn-on or crosstalk between two devices in a phase-leg [13]. Additionally, various forms of capacitive coupling become sources for common-mode currents, such as the gate driver isolation or the coupling of a module's baseplate to its heatsink [14].

Another disadvantage of SiC devices is their ability to withstand a short-circuit event, defined as the short-circuit withstand time (SCWT). Thus, protection of SiC devices is an important aspect of the design, even more so than for Si IGBTs. As described in [15], a SiC device may only have half the SCWT time of a Si IGBT. This requires the protection circuitry to be as fast as possible in order to detect the short-circuit before a catastrophic failure. Subsequently, the device must be shut down after detection. However, if the device is turned off at its normal speed,

the *di/dt* will exceed even the normal operating speed, and will cause very large voltage overshoots, which will degrade the device.

All of these challenges are difficult to deal with at low-voltage levels, and will only escalate as the voltage-level increases. Power devices are being investigated at 10 kV and 15 kV in order to increase power density and increase efficiency and performance [3, 4, 5]. These devices cannot be integrated into the power electronics systems they are designed for unless they are properly controlled. This is why the gate driver is such an integral technology to enable industry acceptance of high-voltage SiC MOSFETs. The benefits of these devices must be balanced with their negative side-effects to make their implementation both time- and cost-effective. Thus, the main consideration of this paper is the comparison of gating methods to enable SiC device technology.

1.1.4 Gating methods and considerations for SiC power devices

Due to the operational differences between SiC and Si transistors, the gate driver for SiC should also be different to provide features that may not be applicable for a Si device. Relevant gate drive considerations such as rise and fall time, propagation delay, and drive power are still important for SiC gate drivers. However, other considerations must also be made for SiC with regards to the isolation of the gate drive power supply, *dv/dt* immunity, variable gate drive strength, and protection mechanisms. A variety of gate driving techniques have been proposed to address these issues. For example, the use of larger gate resistances or snubbers have been proposed to reduce high *dv/dt* transients. While this method may suffice for IGBTs, they do not provide many benefits for SiC devices. There are many ICs on the market designed to drive SiC devices, which may provide a combination of a negative drive voltage, high common-mode transient immunity (CMTI), high output current, fast desaturation protection, two-level turn-off and Miller clamping. Many of these control functions are constant, and do not change based on the device's operating

conditions. This is an essential consideration for SiC MOSFETs as parameters such as the threshold voltage, Miller plateau voltage and energy losses change with the load conditions. Thus, research of SiC gate drivers is still ongoing to evaluate these variations to achieve optimized performance.

Gate drivers for 1.2 kV, 1.7 kV, and 10 kV SiC MOSFETs were developed in [16, 17, 18] to provide sufficient isolation, high-drive strength, and fast and reliable protection. An intelligent gate driver for 10 kV and 15 kV SiC MOSFETs was developed, addressing the careful design of the isolated power supply, resulting in a coupling isolation capacitance smaller than 1 pF, and providing fast protection and constant health-monitoring of the device [19, 20, 21]. Other gate drivers have also been designed to vary the drive strength during transitions to utilize the full performance benefits of SiC and still mitigate the effects of high *dv/dt*. These drivers are addressing the issues related to operational variations as mentioned before, and are entitled “active” gate drivers. These drivers typically utilize feedback or a pre-determined set of controls to change the drive strength during the turn-on or turn-off process. For example, an auxiliary circuit is designed to reduce crosstalk between the upper and lower devices in a phase-leg configuration [22]. Other active gate drivers have been created to enhance the speed at certain instances, i.e. during the Miller plateau region, using a variable gate resistance to reduce switching losses [23]. Some methods control the voltage level during transition to control the slew rates and mitigate EMI [24]. A variety of other drive types have also been considered, including resonant drivers, current-mode drivers, and other methods focused on mitigating the aforementioned challenges [25].

These gate driver solutions provide methods in which to mitigate the large *dv/dt*, *di/dt* and provide protection, but there has yet to be an in-depth investigation and comparison of the drive methods for high-voltage SiC devices. Active gating is considered a crucial method for SiC due to

the many variations of parameters affected by temperature or operating conditions. This thesis investigates the effects of different types of gate driver schemes on the performance of high-voltage SiC MOSFETs with an in-depth investigation of an active gating method utilized to mitigate the effects of high *dv/dt*.

1.2 Thesis Objectives

The objective of this thesis is to provide an investigation of the main challenges associated with the implementation of SiC power devices, as well as the solutions presented from the standpoint of the gate driver. The main factors affecting gate driver design are described, and the performance based on different drive-types will be assessed. The ability of those gate drivers to mitigate the main challenges while still enabling the high-performance of SiC devices is investigated. The drivers will be compared based on the performance of the SiC MOSFET operating during hard-switching and the subsequent power consumption and complexity of the driver itself. Other considerations in the design will also be described, such as the test setup and board layout. The main objectives will be accomplished through the following analyses:

- Assessment of the system-level challenges associated with operating SiC devices
- Comparison of the operation of the gate driver-based solutions
- Analysis of the tradeoffs between *dv/dt* and *di/dt* reduction and switching loss increase
- Considerations of gate drivers for future high-voltage SiC devices
- Suggestions for the optimal drive technique for the demands of the system

1.3 Thesis Organization

This thesis is organized as follows: the assessment of challenges and issues associated with utilizing the SiC power devices is presented in Chapter 2. The gate driver considerations and

impact of the different types is shown in Chapter 3. Chapter 4 will show the evaluation of the methods and discuss the tradeoffs of each. Chapter 5 will describe the experimental setup and design of the proposed gate driver. Finally, Chapter 6 will present the conclusions of the work and future considerations.

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CHAPTER 2

CHALLENGES OF IMPLEMENTING SIC MOSFETS

2.1 Introduction

As discussed in the previous chapter, SiC MOSFETs present a variety of benefits that make them ideal for applications which operate at high voltages, temperatures, and switching frequencies. However, many challenges present themselves due to circuit and device parasitic elements, as well as variations in the operating characteristics of the device. The consequences due to interactions of *di/dt* or *dv/dt* with parasitics can be detrimental to the device, and ultimately the system. The result of these interactions are excessive stress on the device, failure of the device, increased losses, and affected control signal integrity. These issues are further divided into specific topics of research such as crosstalk, self-turn-on, common-mode currents, voltage overshoot, reduced drive strength, and protection. This chapter will investigate these challenges in detail, providing the context for the necessity of an effective gate driver for high-voltage SiC MOSFETs.

2.2 SiC Operating Challenges and Solutions

2.2.1 Crosstalk and Self-turn-on

Silicon carbide devices are known for their ability to switch at very fast speeds with high *dv/dt* and *di/dt,* resulting in smaller switching power losses and the ability to operate at higher frequencies. Unfortunately, there are unintentional effects that manifest themselves when these SiC devices switch at *dv/dt* rates as high as 30 kV/μs or higher [1]. One side-effect of high *dv/dt* is crosstalk, meaning the interaction between complementary devices in a phase-leg, when the switching transient of one device causes the unintentional turning-on of the opposite device. This

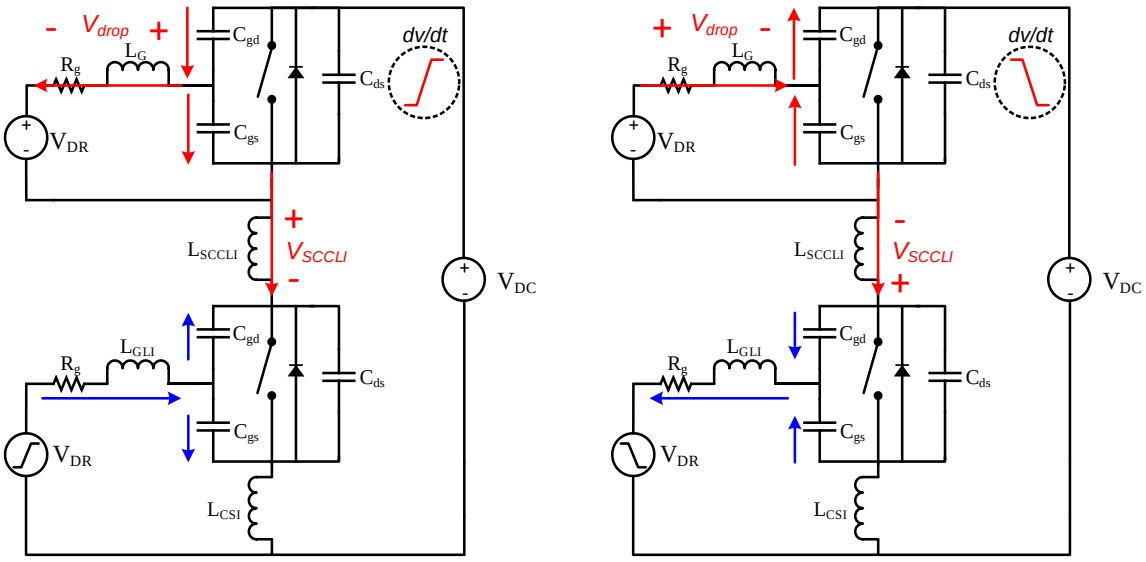
effect is referred to as false-turn-on, implying that the event occurred due to circuit parasitics and not as a result of a faulty control signal.

The main result of a false-turn-on is that both devices will be conducting at the same time, allowing high current to flow and a short-circuit to occur. Even if the short-circuit does not result in a catastrophic event, there are still reliability concerns due to high thermal losses and unnecessary electro-thermal stresses on the device's wire bonds and die [2]. Additionally, the likelihood of a false-turn-on is greater with higher temperature because the threshold voltage has a negative temperature coefficient, making it easier to turn on the device [3]. The shoot-through current also has a positive temperature coefficient, resulting in higher stress on the device at higher temperatures [3]. The potential for failure is greater for SiC devices compared to Si IGBTs because the SiC MOSFET has a lower short circuit withstand time (SCWT). In [6], it was reported to be 8 μs for a SiC MOSFET compared to the Si IGBT's 33 μs withstand time. This will affect the requirements for the protection circuitry and demonstrates the necessity to monitor the health of the device.

False-turn-on can be caused by the interaction with a complementary device or by a device's own high-speed transient and interaction with the common-source inductance, as demonstrated in [6]. In both cases, the Miller capacitance, C_{GD}, serves as the main pathway for current to flow to the gate. This is an uncontrolled variable, as it is inherent to the device. Some of the other variables affecting the likelihood of a false-turn-on are the threshold voltage, V_{th}, the internal gate resistance $R_{G,int}$ and the packaging inductances at the gate and source, L_G and L_S respectively, in the path of the gate current.

Crosstalk between two devices can occur during either the turn-on or turn-off transition of either device in a half-bridge due to the rapidly changing voltage and current sharing at the mid-point. During the turn-on of the lower device, as shown in Figure 2.1 (a), a negative-slope *dv/dt* transition occurs across the C_{GD} of the upper device. The *dv/dt* across C_{GD} results in a current that flows through the gate of the upper device, causing a voltage drop across the gate resistance, R_G and $R_{G,int}$, as well as the gate inductance, which increases the voltage of V_{GS}. If this voltage exceeds the threshold, the device will turn-on [5, 7]. This effect is further amplified due to ringing of L_{SCCLI} due to the high *di/dt*, causing additional power loss.

In the event of the lower device turning-off, there is a positive-slope *dv/dt* that causes current through C_{GD} of the upper device in the opposite direction, as shown in Figure 2.1 (b). This current flows through the R_G, L_G, and L_{SCCLI} causing a negative voltage that further pulls-down the device.



(a) Lower device turns on. *(b) Lower device turns off.*

Figure 2.1. Crosstalk of two devices in a phase leg.

If the device is already held at -5 V, the voltage may be pulled to a value exceeding the maximum negative bias, causing degradation of the gate oxide over time [5].

Various solutions with the gate drive circuitry have been evaluated to mitigate this problem. One commonly adopted solution is the use of a negative bias, -5 V, to hold the device in the off-state and cancel any positive voltage spikes. However, the magnitude of the voltage spikes may be large enough to still reach the threshold voltage, especially at higher temperatures when the threshold voltage is lower. The magnitude of the voltage spikes will be affected by the impedance in the gate loop, including R_G, L_G, and L_S. Thus, it is necessary to make the impedance as small as possible, which is achieved by changing the gate resistor. A higher R_G is typically used to reduce *dv/dt*, thus there is a tradeoff between the size of the resistor and the amount of impedance in the path. Another accepted solution is the use of an Active Miller Clamp (AMC) which provides a low-resistance path to ground for the current to flow. However, the physical location of the AMC determines the actual effectiveness of the method due to the presence of internal gate resistance and other interconnection inductances, which still may be large enough to cause false-turn-on [8]. Other methods of mitigating this problem include separate turn-on and turn-off gate paths or active gate drivers. A combination of the bipolar drive, with -5 V, separate turn-on and turn-off paths, and a snubber capacitor was recommended in [3].

2.2.2 Common-mode noise and isolation

When using SiC MOSFETs and other high-voltage power devices it is necessary to provide sufficient isolation. Aside from protecting the low-voltage control circuitry from high-voltage surges, it is also beneficial to isolate the grounds to prevent noise from reaching the controls. As shown in Figure 2.2, the main isolation barriers are created to protect the control signals via the

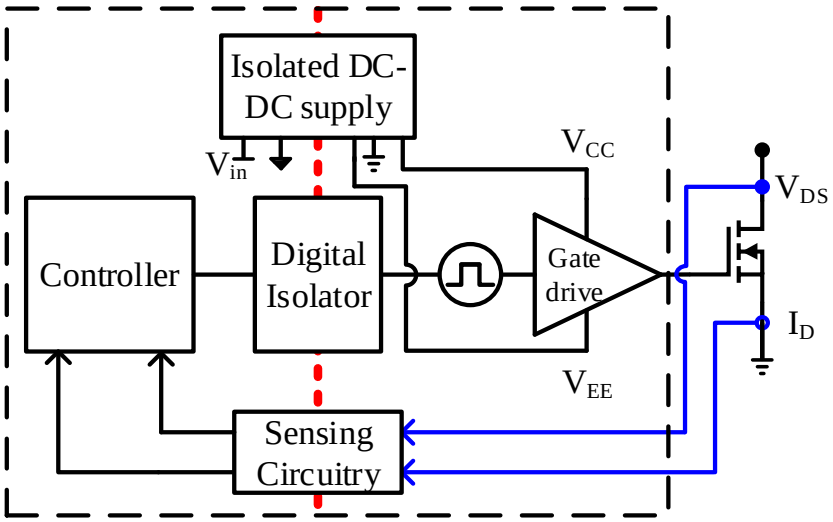


Figure 2.2. Gate driver and isolation barriers.

digital isolator and the isolated power supply for the gate driver. Additionally, the feedback signals through the sensing circuitry should also be isolated. Additional board layout techniques can be implemented to increase the isolation barrier, including the addition of slots or cutouts in the board to increase creepage, or the potting of the circuit in isolation material.

The upper device in the half-bridge must have an isolated signal, or level-shifted signal, due to its connection to the switch node of the phase-leg. This requires the use of an isolated gate driver or separate signal isolation using a digital isolator. This isolation barrier has a parasitic capacitance, as shown in Figure 2.3. Thus, due to the high *dv/dt* shown at the switch node, noisy currents will be allowed to flow through the control circuitry in the path shown in red [9]. Noise is then transferred to the ground on the primary side, and the control signal experiences a non-stable reference, which may affect the control signals. This results in serious problems, especially if the gate of a device is falsely triggered while a complementary device is on, resulting in shoot-through. Additionally, the isolation barrier of the gate driver's DC-DC converter must also be

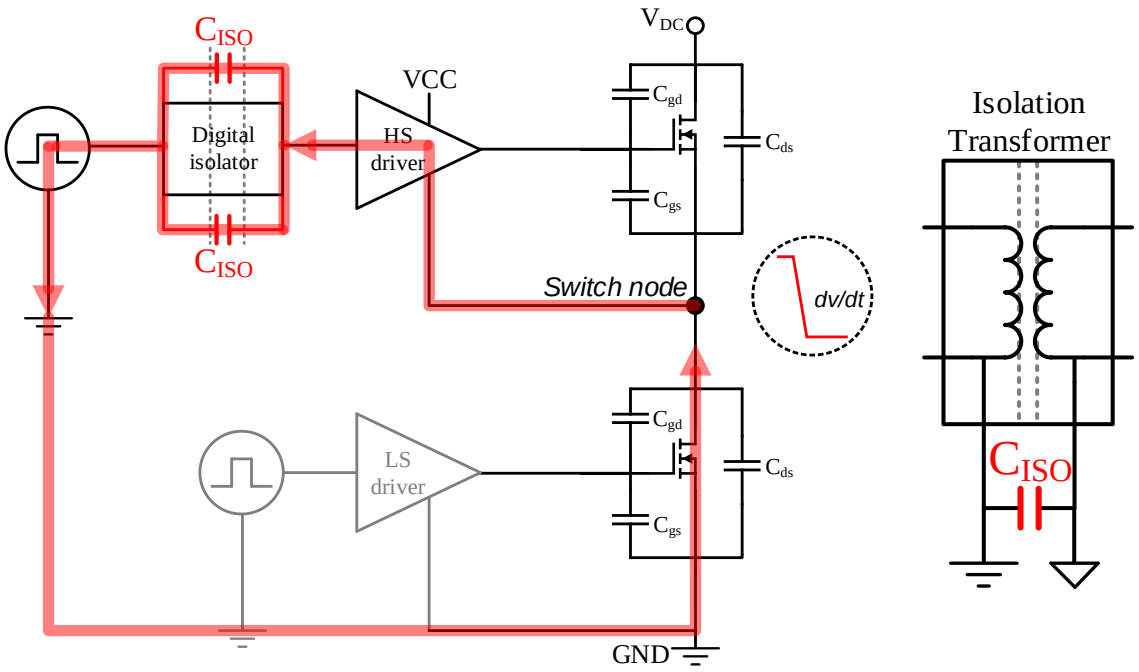


Figure 2.3. Common-mode current through isolation barriers.

designed to reduce the capacitance between transformer windings. In the same way as shown in Figure 2.3, common-mode currents are allowed to flow through the ground to the controls side of the isolation barrier through this power supply. Thus, it is necessary to carefully consider the design of these isolation barriers. Small isolation capacitance of the digital isolator and proper PCB layout can help reduce these effects [9]. The lower device's gate drive signals and power supply may also isolated, but this increases the complexity and number of components in the gate driver design. Additionally, the design of the high-voltage isolation transformer for the DC-DC converter should also be considered, and is a challenging task as described in [1].

Another technique to prevent the malfunction of the control signals due to common-mode noise issues is to use differential signaling for the gate drive signals. In this case, the single-ended signal from the digital signal processor (DSP), or other control card, is translated into a differential signal before being received and then translated back into a single-ended signal to drive the gate

driver. Differential signals are commonly used in digital applications which require very accurate signals and immunity to noise. One downfall of differential signaling is the additional components necessary to transmit the data, as well as the need for two wires, instead of one, to transmit a signal. A tradeoff exists between mitigation of *dv/dt* and design of the circuitry around the device based on the application's requirements with regards to EMI, switching loss and cost. Other methods of reducing common-mode noise may be through filtering using common-mode chokes at the inputs and outputs of the power supplies and DSP signal connections. However, common-mode chokes also introduce a delay, and are designed only for certain frequency response, requiring detailed tuning to harmonics that may also vary depending on the circuit. If care is not taken in the design of the isolation barriers and/or signaling connections, then it is likely that noisy grounds will affect the operation of the SiC MOSFETs and cause false triggering.

2.2.3 Parasitic Inductance

Another critical challenge in the implementation of SiC devices are the parasitic inductances in the device and circuit. The package of the SiC device, whether discrete or in a power module, and the circuit board layout affect the amount of parasitic inductances present in certain regions of the circuit. Each of these inductances can be lumped into the critical areas of the circuit, as shown in Figure 2.4. The interactions of *di/dt* during the turn-on and turn-off transitions result in ringing, voltage overshoot, or reduced driving speed. As described in [10], the parasitic inductances can be split into three main categories: the common-source inductance (CSI), the gate loop inductance (GLI), and the switched current commutation loop inductance (SCCLI). The CSI includes the inductance at the source inside the package of the SiC MOSFET, the source interconnect inductance, and the PCB source trace inductance. The GLI is the area enclosed by the gate drive current path, including the gate path from the gate driver through the source return path

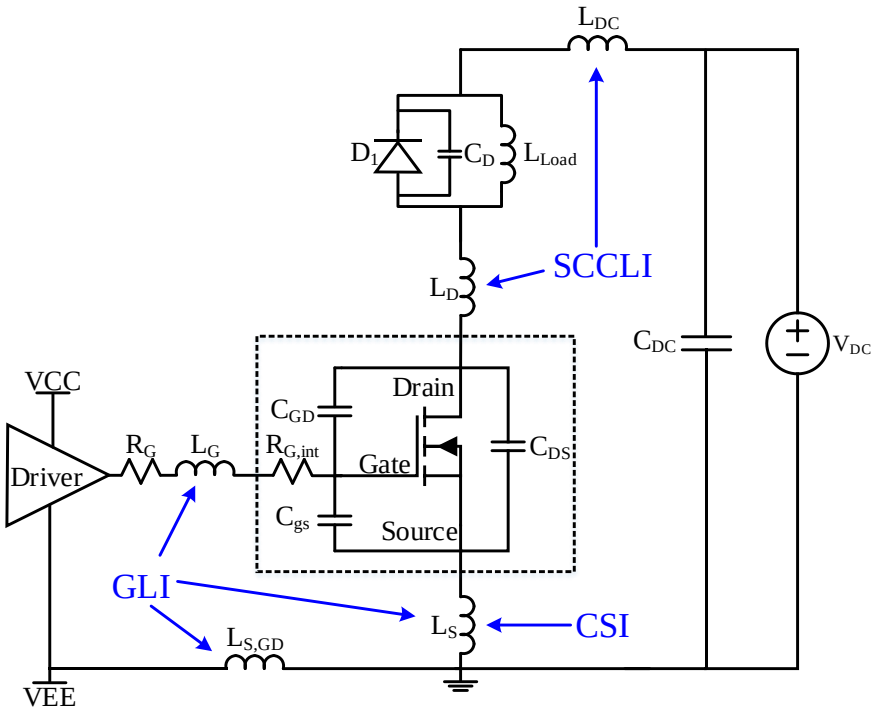


Figure 2.4. Parasitic components surrounding the SiC MOSFET.

back to the driver. Finally, the SCCLI includes the connections between the upper and lower devices in a phase-leg configuration, and results in the main voltage and current ringing of the power loop.

The drain inductance acts as a turn-on snubber for the MOSFET by limiting the *di/dt* of the drain current and reducing the drain-source voltage across the device (*L*di/dt*), thus reducing turn-on losses. However, at turn-off, the voltage induced across the inductor is added to V_{DS}, producing an overshoot and increases the turn-off switching losses. When the device is subjected to these voltage overshoots at every switching cycle the stress over time may decrease the device's lifetime.

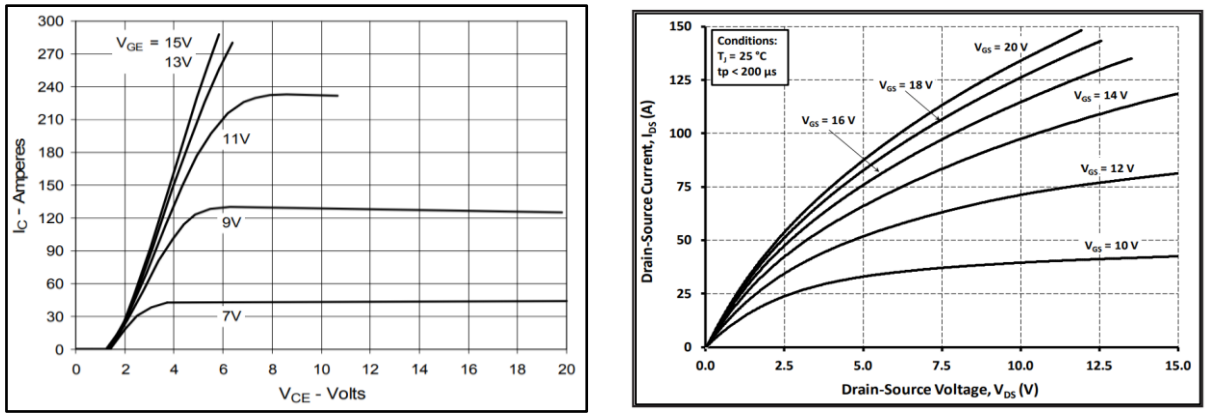
2.2.4 Protection

SiC MOSFETs can operate very efficiently at high-temperatures, and can actually switch faster as temperature increases. The speed at which they switch, however, also affects how fast

Figure 2.5. Failed SiC MOSFET due to short circuit.

they will reach a damaging level of current during a short circuit event. The ability to prevent, protect, or react to such an event is a critical part of the gate driver design. Short circuits will not only cause damage to the device over time, but can cause catastrophic failure of the device, see Figure 2.5. As discussed before, the SCWT of a SiC device can be almost half of the withstand time of a Si device [11, 12]. This means that the gate driver has to be able to detect a short-circuit event much faster than the gate driver for a Si device. Additionally, because SiC devices can switch so fast, the action of turning off the device when a short circuit is detected must be handled carefully so that a very large voltage spike is not caused due to the high *di/dt*. As mentioned in the previous section, excessive voltage overshoot can result in the fast degradation of the device. Thus, there are three main gate driver considerations for this problem, namely: 1) how the short-circuit is detected, 2) how fast the gate driver responds to the detection, and 3) what the gate driver does after detecting the short-circuit.

Typically, a short circuit is detected using the desaturation method, or DESAT, which is used to determine when the device moves from the saturation region to the active region. Unfortunately for SiC devices, the transition from saturation to active is not as clear as for a Si device, as shown in the characteristic curves in Figure 2.6. The DESAT method can still be utilized for a SiC MOSFET, but the design must be more precise than that of a Si device, or else false detections and unnecessary shut-down instances can occur. The DESAT method utilizes the on-resistance and the maximum current rating of the device to determine a normal on-voltage across the device. Usually a high-voltage desaturation diode in series with a zener diode is used to block the current signal to the DESAT pin of a gate driver IC until the reference voltage is surpassed, and DESAT is triggered. This means V_{DS} is being monitored at all times. Other than the difficulty in detecting the transition, this method also has the downfall of having to connect sensing circuitry to the high-voltage V_{DS} of the MOSFET. The isolation barrier needs to be sufficient to protect the control circuitry and the delay between the sensed signal and the controller's response needs to be very short. Additionally, the actual reference voltage for the DESAT protection should be adjustable based on the operating condition, such that a short circuit is not falsely detected.



(a) *Used with permission of IXYS.*

(b) *Used with permission of Cree Inc.*

Figure 2.6. (a) Si IGBT vs. (b) SiC MOSFET i-v characteristics [15, 16].

The speed of the detection must be fast. As described in [10], the SiC MOSFET can fail in half the time that a similarly rated Si IGBT would. When utilizing an IC gate driver with DESAT detection, the propagation delays and detection times from the datasheet should be considered [13]. The propagation delay, which applies to both turn-on and turn-off, will indicate how fast the driver will respond to a control signal telling it to turn-off the device. This is added to the time it takes for the control circuitry to detect the fault, which may also be given in the IC's datasheet if it has DESAT protection as a functionality. Additionally, the physical location of the gate driver will affect the speed at which it detects the fault because parasitic inductance increases with length of traces, and thus increases the propagation delay between the device and the driver.

Another aspect of the DESAT design is what action the gate driver takes to shut down the device in a controlled manner. If the device is turned off as usual, the current will fall at a very fast *di/dt* transition, causing large voltage overshoot due to parasitic inductances. Thus, the device should be shut down slowly to avoid over-voltages. This can be achieved through the use of large gate resistors to decrease the gate current during the transition, or by adding an intermediate voltage level during turn-off, sometimes called soft turn-off or two-level turn-off (TLTO) [11]. An intermediate voltage is utilized at this time to bring the current down to an acceptable level before completely shutting it down using the lowest drive voltage available, typically -5 V. Utilizing the intermediate voltage level allows the current to transition slowly, and will increase the SCWT of the device. In [11], the 1.2 kV SiC MOSFET was able to handle a short-circuit for 13 μs before failing when using an intermediate voltage of 15 V, versus surviving for 7 μs when the gate-source voltage was held at 20 V. This may cause a designer to conclude that the device should be driven at 15 V in order to improve the reliability of the device in these types of scenarios, however, the designer will then suffer the consequences of higher conduction losses because of greater $R_{ds(on)}$ at

lower V_{GS}. In [14], the Rowgowski coil is used to detect the current without measuring the voltage, providing complete isolation of the measurement, as well as avoiding the cost of false-triggering the fault signal if an incorrect voltage reference is used in DESAT. The *di/dt* information from the Rowgowski coil is processed through the use of an integrator sensing circuit and comparator to enable the fault signal. The coil must have a high bandwidth in order to measure all of the details of the waveform. Being a non-intrusive measurement, the impedance in the commutation loop is not affected. Alternatively, current shunt resistors, or current viewing resistors, are also utilized due to their very high bandwidth and high accuracy, but they must be inserted into the circuit itself. This may introduce additional inductance into the loop, but can be compensated with the measurement circuitry or precise design.

2.3 Conclusion

The challenges associated with using SiC MOSFETs may sound daunting, but the benefits are very appealing. Some common solutions to those challenges were discussed in this chapter. The role of the gate driver is to provide the necessary functions to enable the high performance of the device, while still maintaining the reliability and safety of the circuit around it. The gate driver for high-voltage SiC MOSFETs should include all the necessary functions to prevent failure of the device and system through careful design of the DC-DC converter isolation, other control signal isolation barriers, noise mitigation, and protection. Aside from these functions, the gate driver can actually be used to mitigate the challenges with regards to *dv/dt* and *di/dt* transients, and still achieve high performance. In the following chapters, the gate driver technology will be discussed, and the methodologies will be compared to determine the best driver for high-voltage SiC MOSFETs.

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CHAPTER 3

GATE DRIVE METHODS AND PERFORMANCE

3.1 Introduction

From Chapter 2, it was shown that poor gate driver design and ignorance of the challenges of driving SiC MOSFETs could result in an ineffective system. The main solution is to have a gate driver that enables the device to have low energy losses while still mitigating the *dv/dt* and *di/dt* to the levels required by the system. State-of-the-art gate driver technologies may not provide the control necessary to enable SiC MOSFETs. First, this chapter will introduce some of the main considerations for the gate driver. Secondly, two categories of gate driver circuits are discussed: the conventional voltage-mode driver and the current-mode driver. The theoretical operation of these drivers is outlined, and the main parameters of each are pointed out [1]. Finally, a multi-level voltage driver is proposed as a solution for mitigating the harmful effects of fast switching, and the theoretical analysis of this method is given.

3.2 Gate Driver Considerations

This section will first introduce the main considerations of the gate drive circuitry to effectively drive a power MOSFET. Many of these parameters are included in the device datasheet, such as the gate charge, its capacitances, the threshold voltage, the on-resistance, and the internal gate resistance. Firstly, MOSFETs are driven through the charging and discharging of its input capacitance, C_{iss}, which is the sum of the C_{GS} and C_{GD} capacitors. The amount of charge needed to fully turn-on the device is given as the gate charge, Q_G. The gate charge is found by applying a constant current at the gate and observing the time it takes for the gate-source voltage to rise to its

maximum value. In other words, the gate charge can be measured by taking the integral of the gate current over time.

$$Q_G = \int I_G dt \tag{3}$$

This is an important parameter because it defines the drive strength, I_G, which can be found using:

$$I_G = \frac{Q_{G,total}}{t_{rise/fall}} \tag{4}$$

Where $t_{rise/fall}$ is the desired rise and fall times of V_{GS}. The effects of the capacitors and their charge on the switching operation of the device can be further investigated by looking at the gate charge plot vs. V_{GS} located in the device datasheet. This plot is divided into three main regions during which the input capacitors, C_{GS} and C_{GD}, are being charged or discharged, as shown in Figure 3.1. The first portion of the gate charge figure represents Q_{GS}, during which C_{GS} is charged from the off-voltage to the Miller plateau. The flat region of the plot represents the so-called Miller plateau voltage, during which the current is redirected to charge C_{GD}. The Miller region is greatly

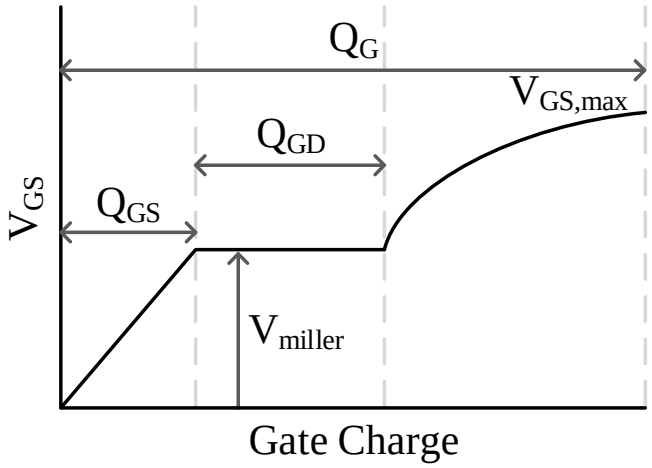


Figure 3.1. Gate charge plot.

dependent on the ratio of C_{GD} to C_{GS}. When the slope is non-zero, which is the case for SiC MOSFETs, some of the current flows through C_{GS} while C_{GD} is also being charged, making the voltage plateau non-flat. After the Miller plateau region ends, V_{GS} rises to the final turn-on voltage level, and all the current flows through C_{GS}.

It is also important to note that the Miller plateau voltage changes with the load, primarily due to the drain current. The duration of the plateau region, however, also tends to increase with larger V_{DS}. The equation below is commonly used to describe the Miller plateau voltage.

$$V_{miller} = V_{th} + \frac{I_D}{g_{fs}} \tag{5}$$

This value may not always be accurate due to variations of V_{th} and g_{fs}. V_{th} is the threshold voltage, or the minimum voltage required to enhance the device, and g_{fs} is the device's transconductance. The transconductance describes the change in the drain current, I_D, with a given change in V_{GS}.

This information will serve as a baseline for the minimum required drive strength. The gate current is controlled through various gate driver methods, each utilizing different ways of controlling it. These drivers will be discussed in the following section and the switching waveforms are given for each, with the equations given to describe each transition.

3.3 Conventional Voltage-Mode Gate Driver

The most common gate driver for power MOSFETs is the voltage-mode driver. This type of driver typically employs a type of totem-pole buffer, utilizing BJTs or MOSFETs, to pull the gate of the power device to a high or low voltage depending on the MOSFET's power rating. One

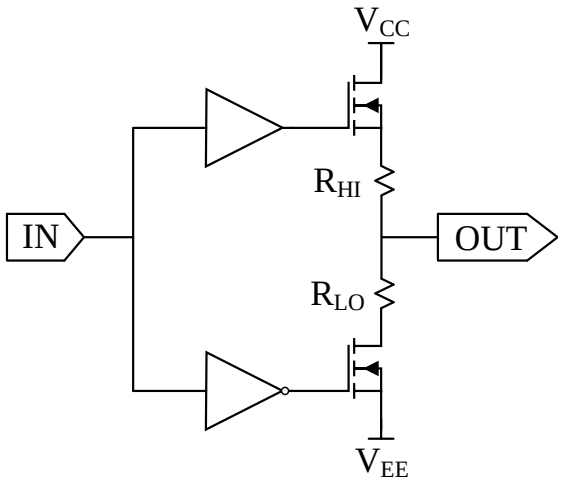


Figure 3.2. NFET totem-pole buffer.

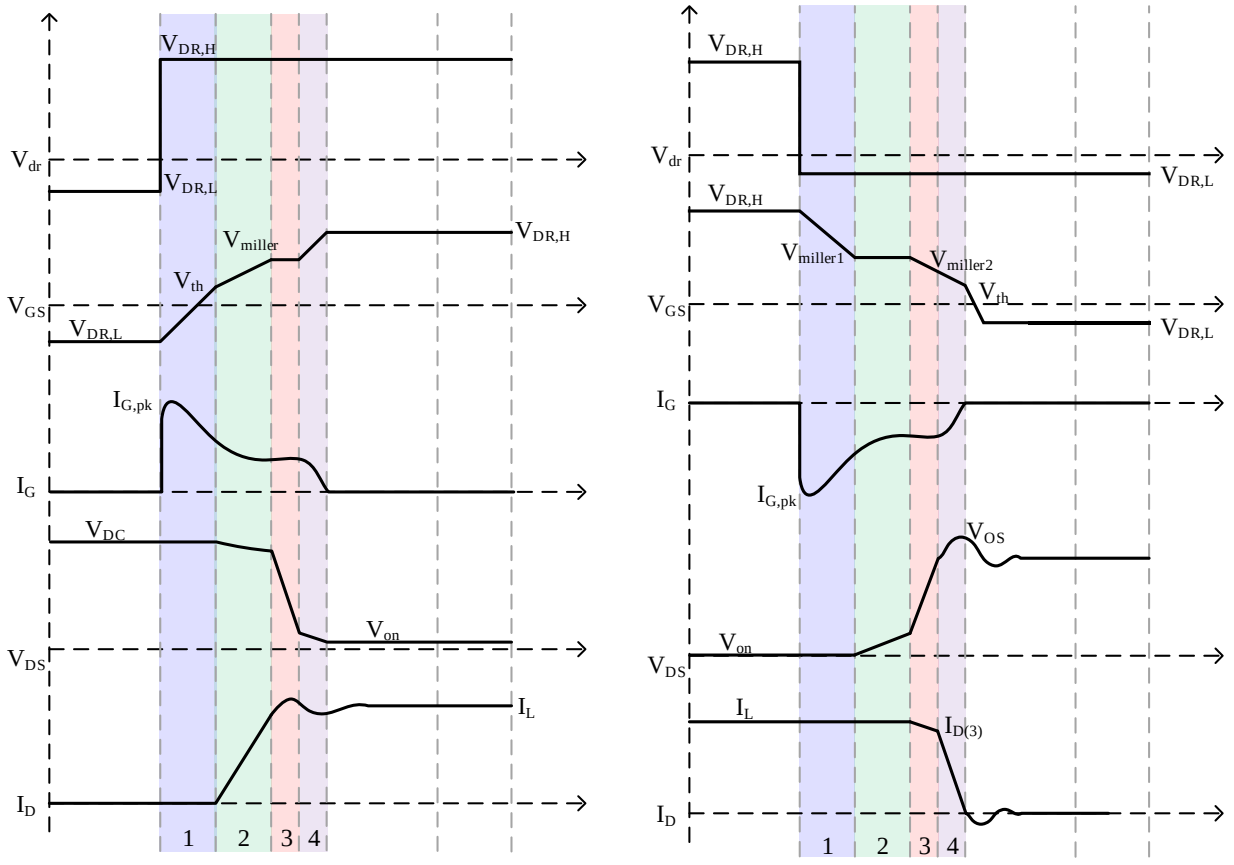
such topology is shown in Figure 3.2, where R_{HI} and R_{LO} are the output resistances of the driver [2].

The switching processes for turn-on and turn-off are shown in Figure 3.3, where V_{dr} is the drive voltage from the gate driver, V_{GS} is the voltage at the gate of the device, and I_G is the gate current, which charges and discharges the MOSFET's capacitors [1]. On the V_{GS} waveform, V_{th} is the device's threshold voltage, and V_{miller} is the Miller plateau voltage. $I_{G,pk}$ on the gate current waveform is the peak gate current. The drain-source voltage, V_{DS} is shown, as well as the drain current I_D, which are used to define the *dv/dt*, *di/dt* and energy losses. V_{on}, shown on the V_{DS} waveform, is the on-state voltage, which is dependent on the value of I_D and $R_{DS(on)}$. The high-level drive voltage, $V_{DR,H}$, is chosen based on the datasheet of the MOSFET, corresponding to the lowest on-resistance, $R_{DS(on)}$, during conduction. The low-level drive voltage, $V_{DR,L}$, is also the datasheet recommended value, typically a negative voltage for SiC MOSFETs. The negative voltage rail provides both a larger potential across the gate resistor to increase the discharge current, as well as increases the margin between the amplitude of gate ringing and the threshold voltage.

The turn-on process can be split into four main intervals: (1) the turn-on delay, (2) the current rise time, (3) the first voltage fall time, and (4) the second voltage fall time, as shown in Figure 3.3 (a). The relevant equations for these intervals are shown below.

During period (1) the gate voltage rises from $V_{DR,L}$ to V_{th}. C_{GS} is charged during this interval, and there are no losses in this period because the current still flows through the Schottky diode in the upper switch position.

During period (2) the current begins to rise across the MOSFET and there is a slight voltage drop on V_{DS} due to the power loop inductance SCCLI interaction with *di/dt*. The gate voltage



(a) Turn-on process. *(b) Turn-off process.*

Figure 3.3. Transient switching waveforms of a SiC MOSFET with a voltage-mode driver.

during this period rises from V_{th} to the Miller plateau voltage, V_{miller}. The drain current rise is dependent on the transconductance, g_{fs}, and the gate voltage, as described in (6).

$$I_d(t) = g_{fs}\left(V_{gs}(t) - V_{th}\right) \tag{6}$$

The duration of period (2) is found by rearranging the equation for the relationship between the voltage change and current in a capacitor, $I=C*dv/dt$, where the input capacitance is being charged:

$$t_{on(2)} = \frac{C_{iss}(V_{miller} - V_{th})}{I_g} \tag{7}$$

C_{iss} is equal to $C_{gd}+C_{gs}$, where C_{gd} can be split into two values, one when $V_{DS}>V_{gs}-V_{th}$ and the other when $V_{DS}<V_{gs}-V_{th}$. The Miller plateau voltage is found using:

$$V_{miller} = V_{th} + \frac{I_L}{g_{fs}} \tag{8}$$

To determine how the circuit components like the gate resistance, R_G and the common-source inductance, L_S, affect the losses during this period, the gate current can be found using Kirchoff's voltage law (KVL).

$$I_G = \frac{\left(V_{DR,H} - 0.5(V_{miller} + V_{th}) - L_s\left(\frac{I_L}{t_{on(2)}}\right)\right)}{R_G} \tag{9}$$

Using this expression for the gate current, the time interval can be re-written as:

$$t_{on(2)} = \frac{C_{iss}R_G I_L + L_s g_{fs} I_L}{\left(V_{DR,H} - 0.5V_{th} - 0.5V_{miller}\right) g_{fs}} \tag{10}$$

The current transition, *di/dt*, can now be found using (10) in:

$$\frac{dI_d}{dt_{on(2)}} = \frac{I_L}{t_{on(2)}} \tag{11}$$

Additionally, the voltage drop in V_{DS} due to the commutation loop inductance, L_{SCCLI}, can be described using the following equation

$$V_{ds}(t) = V_{DC} + V_d - L_{SCCLI}\frac{I_L}{t_{on(2)}} \tag{12}$$

Utilizing the expressions for V_{DS} and I_D, the energy losses during this period are found by integrating the product of the two.

$$E_{loss,on(2)} = 0.5\left(t_{on(2)} I_L (V_{DC} + V_d)\right) - \frac{1}{3}(I_L^2 L_{SCCLI}) \tag{13}$$

During this period, it is shown that $V_{DR,H}$, R_G, and L_S all affect the *di/dt* of the drain current through their relationship with the duration. The duration is included in the energy loss expression, and thus higher R_G and L_S will both result in higher energy losses. When $V_{DR,H}$ is larger, the duration will decrease. Surprisingly during this interval, the commutation loop inductance actually contributes to lowering the energy losses, due to the voltage drop on V_{DS}.

During periods (3) and (4) the voltage falls from V_{DC} to V_{ON} (I_L*$R_{DS(on)}$). There are two main slopes of *dv/dt* due to the variations in Miller capacitance with V_{DS}.

In period (3), V_{DS} falls from V_{DC} to V_{miller}. Using KVL, the gate current can be found as shown

$$I_G = \frac{\left(V_{DR,H} - V_{miller} - \frac{\left((C_d + C_L)(V_{DC} + V_d - V_{miller} + V_{th})\right)}{g_{fs} t_{on(3)}}\right)}{R_G} \tag{14}$$

Where C_d and C_L are the diode capacitance and inductor capacitance, respectively. During this period, these capacitors will cause some reverse current, causing additional losses. The duration of the first subinterval of period (3) is given by:

$$t_{on(3)} = \frac{\left((V_r - V_{miller} + V_{th}) C_{gd} R_G + \frac{(C_d + C_L)(V_{DC} + V_d - V_{miller} + V_{th})}{g_{fs}}\right)}{V_{DR,H} - V_{miller}} \tag{15}$$

where V_r represents the voltage after the drop due to the commutation loop inductance.

$$V_r = V_{DC} + V_d - L_{SCCLI} \frac{I_L}{t_{(2)}} \tag{16}$$

Thus, the negative slope *dv/dt* is expressed as:

$$\frac{dV_{DS}}{dt} = \frac{V_{miller} - V_{th} - V_r}{t_{(3)}} \tag{17}$$

And the energy losses during this transition can be found using:

$$E_{loss(3)} = 0.5t_{on(3)}I_L(V_r + V_{miller} - V_{th}) + 0.5(C_d + C_L)(V_{DC} + V_d - V_{miller} + V_{th})(V_r + V_{miller} - V_{th}) \quad (18)$$

Therefore, the dependence of the SCCLI is still present in this transition, as well as the dependence on R_G and $V_{DR,H}$ with regards to the *dv/dt* transition and energy losses. The contribution from the parasitic capacitances of the load inductor and diode are also factored in.

Period (4) represents the period during which the MOSFET moves into the ohmic region and V_{DS} falls to the final value, V_{ON}. During this interval, V_{DS} becomes smaller than V_{GS}-V_{th} and the value for C_{gd} becomes larger. The gate current during this interval is:

$$I_G = \frac{V_{DR,H} - V_{miller}}{R_G} \quad (19)$$

The duration of this subinterval is expressed as:

$$t_{on(4)} = \frac{(V_{miller} - V_{th} - V_{ON})C_{gd}R_G}{V_{DR,H} - V_{miller}} \quad (20)$$

The second *dv/dt* transition can be found using:

$$\frac{dV_{DS}}{dt} = \frac{V_{ON} - V_{miller} + V_{th}}{t_{on(4)}} \quad (21)$$

Finally, the energy losses during this interval are given by

$$E_{loss(4)} = 0.5 I_L t_{on(4)} (V_{miller} - V_{th} + V_{ON}) + 0.5(C_d + C_L)(V_{miller} - V_{ON} - V_{th})(V_{miller} + V_{ON} - V_{th}) \quad (22)$$

Still, the main contribution to the energy losses and *dv/dt* transition via the duration come from R_G. As mentioned previously, this is why R_G is often used to slow down the *di/dt* and *dv/dt*. The tradeoffs between energy losses and the mitigation of *di/dt* and *dv/dt* will be discussed later on in this chapter.

The turn-off process is very similar to turn-on, and can be split into four main intervals: (1) the turn-off delay, (2) the first voltage rise time, (3) the second voltage rise time, and (4) the current fall time, as shown in Figure 3.4 (b). In period (1), V_{GS} falls from $V_{DR,H}$ to V_{miller} at a rate dependent on the value of C_{gs}. There are no losses during this interval, but it does affect the maximum allowable switching frequency, so it is preferred that this is as small as possible.

Periods (2) and (3) describe the two *dv/dt* intervals. Period (2) is the first rise in voltage from V_{ON} to V_{miller}-V_{th}. The device goes into the ohmic region and I_D remains constant. In the same way as the turn-on intervals, KVL is used to find the gate current:

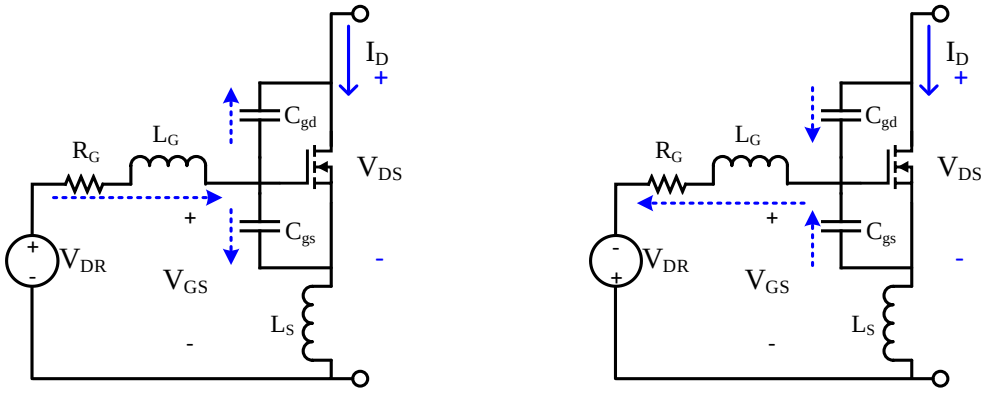


Figure 3.4. Turn-on and turn-off current paths of voltage-mode driver.

$$I_G = \frac{V_{miller} - V_{DR,L}}{R_G} \tag{23}$$

The duration is given by

$$t_{off(2)} = \frac{(V_{miller} - V_{th} - V_{ON})C_{gd}R_G}{V_{miller} - V_{DR,L}} \tag{24}$$

Where V_{ON} is the on-state voltage due to the voltage drop across $R_{DS(on)}$. The *dv/dt* can thus be found as:

$$\frac{dV_{DS}}{dt} = \frac{V_{miller} - V_{th} - V_{on}}{t_{off(2)}} \tag{25}$$

The energy losses are given by:

$$E_{loss,off(2)} = 0.5 I_L t_{off(2)}(V_{miller} - V_{th} + V_{ON}) \tag{26}$$

It is still found that these losses are dependent on $V_{DR,H}$ and R_G. It also should be noted that in the physical circuit, the gate resistance is defined as the total resistance, including the external resistor, the internal device resistance and any other copper resistance.

The second *dv/dt* transition occurs during period (3), during which the diode and load capacitors are discharged by the load current, causing I_D to drop slightly. The gate current is found using R_G, the negative drive voltage, $V_{DR,L}$, and the Miller plateau level:

$$I_G = \frac{0.5(V_{miller2} + V_{miller1}) - V_{DR,L}}{R_G} \tag{27}$$

There are two plateau levels for a SiC MOSFET due to the ratio between C_{gd} and C_{gs}, causing some current to flow through C_{gs} during the plateau region. Thus, in the above equation, the Miller voltage is shown as an average of these two values, and $V_{miller2}$ is found using:

$$V_{miller2} = V_{th} + \frac{\left(I_{D(3)} - \frac{(C_{ds} + C_{gd})(V_{DC} - V_{miller} + V_d + V_{th})}{t_{off(3)}}\right)}{g_{fs}} \tag{28}$$

The current level, $I_{D(3)}$, is the current due to its re-direction through C_L and C_d. This is found using the relationship between the *dv/dt* and capacitance.

$$\begin{aligned} I_{D(3)} &= I_L - (C_d + C_L) * \frac{dV_{DS}}{dt} \\ &= I_L - \frac{(C_d + C_L)(V_{DC} - V_{miller} + V_d + V_{th})}{t_{off(3)}} \end{aligned} \tag{29}$$

The duration of this time interval is thus given as:

$$t_{off(3)} = \frac{\left(C_{gd}R_G + \frac{C_{ds} + C_{gd} + C_d + C_L}{2g_{fs}}\right)(V_{DC} - V_d - V_{miller} + V_{th})}{V_{miller} - V_{DR,L}} \tag{30}$$

And the second *dv/dt* transition during period (3) is

$$\frac{dV_{DS}}{dt} = \frac{V_{DC} + V_d - V_{miller} + V_{th}}{t_{off(3)}} \tag{31}$$

The energy losses are given by:

$$E_{loss(3)} = 0.5\left(t_{off(3)}(V_{DC} + V_d - V_{miller} + V_{th})(2I_{D(3)} + I_L) + \left(t_{off(3)}(V_{miller} - V_{th})(I_{D(3)} + I_L)\right)\right) \tag{32}$$

The slope of the *dv/dt* is the highest during this interval, and should be monitored due to the issues mentioned in Chapter 2. However, if the *dv/dt* is reduced using R_G, the same effects will occur as mentioned during turn-on, resulting in increased energy loss.

Finally, period (4) describes the current fall time during which the current is diverted to the upper Schottky diode when it becomes forward biased. The current falls from $I_{D(3)}$, from the period (3), to zero. The gate current during this interval is described by

$$I_G = \frac{0.5(V_{miller} + V_{th}) - V_{DR,L} - L_S\frac{I_{D(3)}}{t_{off(4)}}}{R_G} \tag{33}$$

In this expression, L_S is the common-source inductance, CSI, which reduces the drive strength based on the *di/dt* of the drain current.

The duration of this period is found using:

$$t_{off(4)} = \frac{R_G I_{D(3)} C_{iss} + L_{SCCLI} I_{D(3)} g_{fs}}{\left(0.5V_{miller2} + 0.5V_{th} - V_{DR,L}\right) g_{fs}} \tag{34}$$

Thus, the *di/dt* transition can be found using Eq. (35).

$$\frac{dI_D}{dt} = \frac{I_{D(3)}}{t_{off(4)}} \tag{35}$$

During this transition, and as mentioned in Chapter 2, the device can experience overvoltage stress because of the voltage drop across the commutation loop inductance reacting with the *di/dt* transient. This overshoot voltage is given by the following equation:

$$V_{OS} = V_{DC} + V_d + L_S \frac{I_{D(3)}}{t_{off(4)}} \tag{36}$$

Finally, the energy loss during this period is given by:

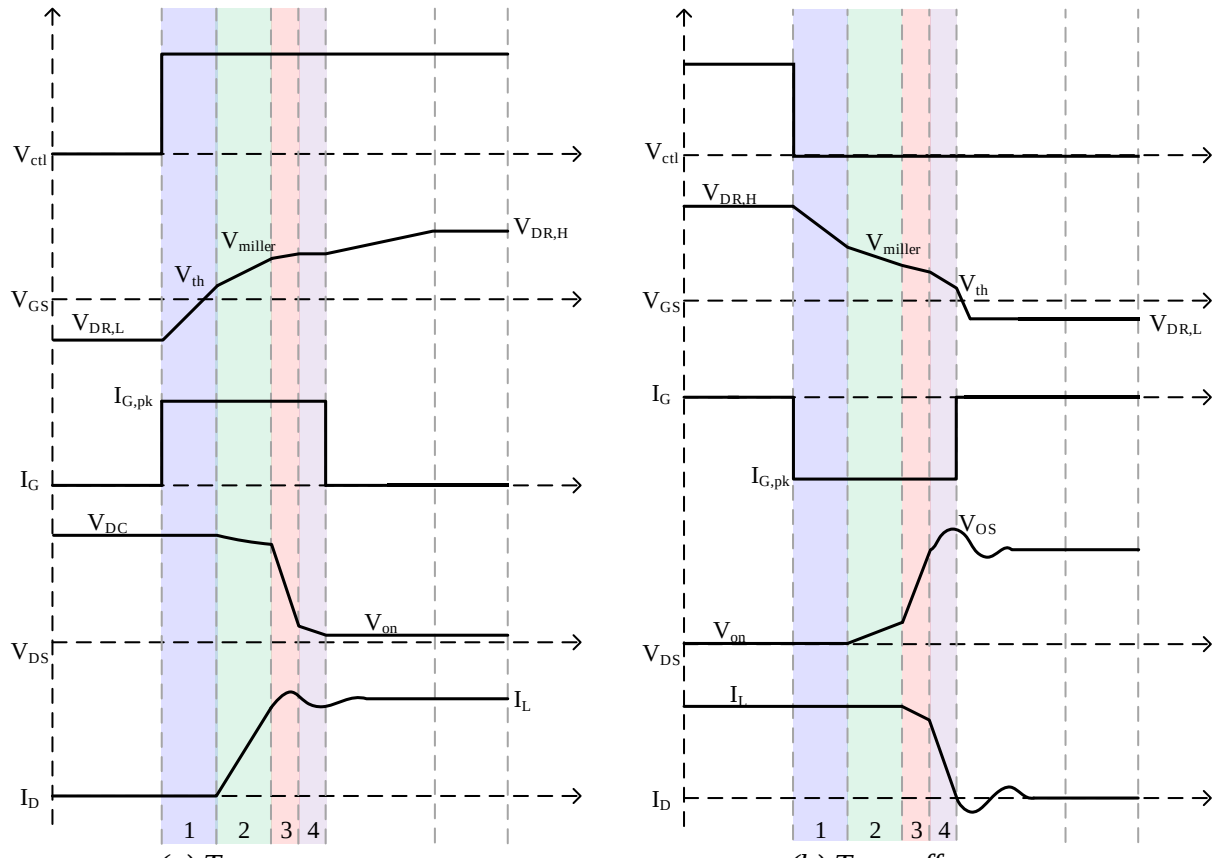
$$E_{loss(3)} = 0.5\left(t_{off(4)}(V_{DC} + V_d)\right) I_{D(3)} + L_{SCCLI} \frac{I_{D(3)}^2}{2} \tag{37}$$

Through these equations, it is found that the energy losses will increase when R_G, L_S or L_{SCCLI} increase and will be smaller if $V_{DR,L}$ is more negative.

In the final section of this chapter, the dependence of these equations on parasitics will be compared to the current-source transient analysis given in the following section.

3.4 Current-Mode Gate Driver

In order to improve the performance of the gate driver and prevent the effects of R_G, common-source (CSI) and commutation loop (SCCLI) inductances, researchers have been investigating the option of current-mode drivers [3–6]. The current-mode driver, as the name implies, provides constant current to the gate to drive the power MOSFET. The benefit of this method is that the current drive strength is no longer dependent on the value of R_G. Due to the constant level of current at the gate, the input capacitors, C_{gs} and C_{gd}, are charged and discharged at a constant rate, providing more consistent *di/dt* and *dv/dt* transitions. The waveforms showing the ideal operation of a current-source driver are shown in Figure 3.5.



(a) Turn-on process. *(b) Turn-off process.*

Figure 3.5. Transient switching waveforms of a SiC MOSFET with a current-mode driver.

In this section, the effect of I_G on the energy loss, *dv/dt*, and *di/dt* transitions is the main focus. The turn-on and turn-off processes are each divided into four periods. During turn-on, period (1) is the turn-on delay, (2) is the current rise time, (3) is the first voltage fall time, and (4) is the second voltage fall time.

During period (1) the gate voltage rises from $V_{DR,L}$ to V_{th} and C_{gs} is charged with a constant current, and there are no energy losses.

During period (2) the current begins to rise through the MOSFET and the same voltage drop on V_{DS} is still present due to the interaction between the loop inductance, SCCLI, and the *di/dt*. As opposed to the voltage-mode driver, the time duration of this period is dependent on the gate current, instead of the drive voltage. The same equations apply, but the duration will change because of the constant I_G.

$$t_{on(2)} = \frac{\left(C_{iss}(V_{miller} - V_{th})\right)}{I_G} = \frac{I_L C_{iss}}{g_{fs} I_G} \tag{38}$$

Here it is found that the duration is no longer dependent on R_G or L_S. The current transient, *di/dt*, is thus found as shown in Eq. 39.

$$\frac{dI_d}{dt_{on,2}} = \frac{I_L}{t_{on(2)}} \tag{39}$$

The expression for the energy loss is the same, but the duration has been changed based on the gate current.

$$E_{loss,on(2)} = 0.5\left(t_{on(2)} I_L (V_{DC} + V_d)\right) - \frac{1}{3}(I_L^2 L_{SCCLI}) \quad (40)$$

In periods (3) and (4), the voltage falls from V_{DC} to V_{ON}. As opposed to the voltage-mode driver, the *dv/dt* can be expressed with a single equation for both intervals.

The gate current is still held constant, and thus the magnitude of the change in voltage over time is only dependent on the current level and the input capacitance.

$$\frac{dV_{DS}}{dt} = \frac{I_G}{C_{gd}} \quad (41)$$

Two different slopes during (3) and (4) will still be observed because of the changes in C_{gd} based on V_{DS}.

The duration of (3) is found using:

$$t_{on(3)} = \frac{(V_r - V_{miller} + V_{th}) * C_{gd}}{I_G} \quad (42)$$

Where the *dv/dt* can also be expressed as:

$$\frac{dV_{DS}}{dt} = \frac{V_{miller} - V_{th} - V_r}{t_{on(3)}} \quad (43)$$

The energy losses during (3) are given as:

$$E_{loss(3)} = 0.5t_{on(3)}I_L(V_r + V_{miller} - V_{th}) + 0.5(C_d + C_L)(V_{DC} + V_d - V_{miller} + V_{th})(V_r + V_{miller} - V_{th}) \quad (44)$$

While the second voltage fall duration is expressed as:

$$t_{on(4)} = \frac{(V_{miller} - V_{th} - V_{ON}) * C_{gd}}{I_G} \quad (45)$$

This expression has the same dependence on C_{gd} and I_G as the voltage-mode driver. The voltage slope during this period is:

$$\frac{dV_{DS}}{dt} = \frac{V_{ON} - V_{miller} + V_{th}}{t_{on(4)}} \quad (46)$$

The energy losses during period (4) are written in the equation below. The loss due to the diode and load parasitic capacitors is still included, as it was in for the voltage-mode driver.

$$E_{loss(4)} = 0.5I_L t_{on(4)}(V_{miller} - V_{th} + V_{ON}) + 0.5(C_d + C_L)(V_{miller} - V_{ON} - V_{th})(V_{miller} + V_{ON} - V_{th}) \quad (47)$$

The turn-off transition is also divided into four subintervals: (1) the turn-off delay, (2) the first voltage rise time, (3) the second voltage rise time, and (4) the current fall time, as shown in Figure 3.5 (b). During period (1), the voltage falls from the maximum V_{GS} to V_{miller} and the time delay is dependent on the gate current.

During periods (2) and (3) the voltage rises with two slopes, in the same way as the turn-on transition, due to variations in C_{gd}. This transition is again controlled by the gate current through the relationship shown in equation (48).

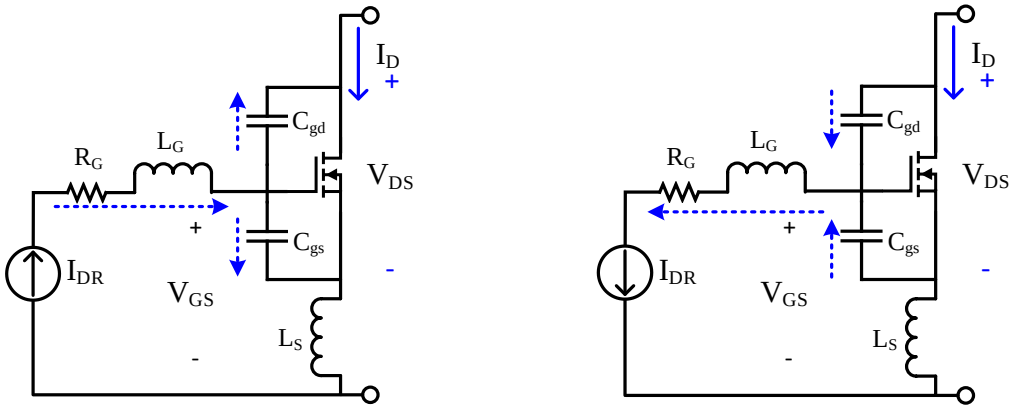
$$\frac{dV_{DS}}{dt} = \frac{I_G}{C_{gd}} \tag{48}$$

With the duration given by the same equation as that in the turn-on.

$$t_{off(2)} = \frac{(V_{miller} - V_{th} - V_{ON})C_{gd}}{I_G} \tag{49}$$

Thus, the losses during this period are

$$E_{loss(2)} = 0.5 I_L t_{off(2)} (V_{miller} - V_{th} + V_{ON}) \tag{50}$$



(a) (b)

Figure 3.6. Turn-on and turn-off current paths of current-mode driver.

During period (3), the diode and load capacitors are discharged, causing a current drop in I_L, which also occurs with the voltage-mode driver. The duration of this period can be written as:

$$t_{off(3)} = \frac{(V_{DC} - V_d - V_{miller} + V_{th})C_{gd}}{I_G} \tag{51}$$

The energy losses are given by:

$$E_{loss(3)} = 0.5\left(t_{off(3)}(V_{DC} + V_d - V_{miller} + V_{th})\left(2I_{D(3)} + I_L\right) + \left(t_{off(3)}(V_{miller} - V_{th})\left(I_{D(3)} + I_L\right)\right)\right) \tag{52}$$

Finally, the current falls to 0 in period (4) and V_{GS} falls below the threshold voltage. Both C_{gs} and C_{gd} are discharged, thus the duration is:

$$t_{off(4)} = \frac{I_{D(3)}C_{iss}}{g_{fs}I_G} \tag{53}$$

The *di/dt* transition can thus be written as:

$$\frac{dI_D}{dt} = \frac{I_{D(3)}}{t_{off(4)}} \tag{54}$$

The energy losses are found using the following equation, where LSCCI contributes to the losses.

$$E_{loss(4)} = 0.5 I_{D(3)} \left(t_{off(4)} (V_{DC} + V_d) \right) + L_{SCCLI} \frac{I_{D(3)}^2}{2} \quad (55)$$

The voltage overshoot due to *di/dt* is given below, where the *di/dt* determines the magnitude of the overshoot.

$$V_{OS} = V_{DC} + V_d + L_{SCCLI} \frac{I_{D(3)}}{t_{off(4)}} \quad (56)$$

As the gate current decreases, the duration will increase, leading to a smaller *di/dt*. This would, in turn, decrease the voltage overshoot and stress on the device, but would also increase losses. Thus, there is a compromise present for the current-mode driver, as well.

3.3 Multi-Level Gate Driver

As an alternative to the conventional voltage-mode and current-mode drivers, active gate drivers are proposed by researchers as alternatives to allow for greater control over the switching of the device. Due to the many variations of parameters, such as V_{th} and V_{miller}, due to temperature or operating conditions, the energy losses, *dv/dt* and *di/dt* will change too. Thus, the purpose of an active gate drivers is to sense these changes, and respond accordingly to enhance the performance of the switching device. Many kinds of active gate drivers have been proposed in the literature, including current injection, variable R_G, and variable voltage [7– 9]. Each have their benefits and drawbacks with regards to control complexity or additional cost. One method that has proved to be reliable in changing the *dv/dt* and *di/dt* is the multi-level voltage driver. During turn-on, it is desirable to speed up the transition to reduce the energy losses, which are higher than the turn-off energy losses. Thus, a voltage level higher than the typical on-state V_{GS} can be used to speed up

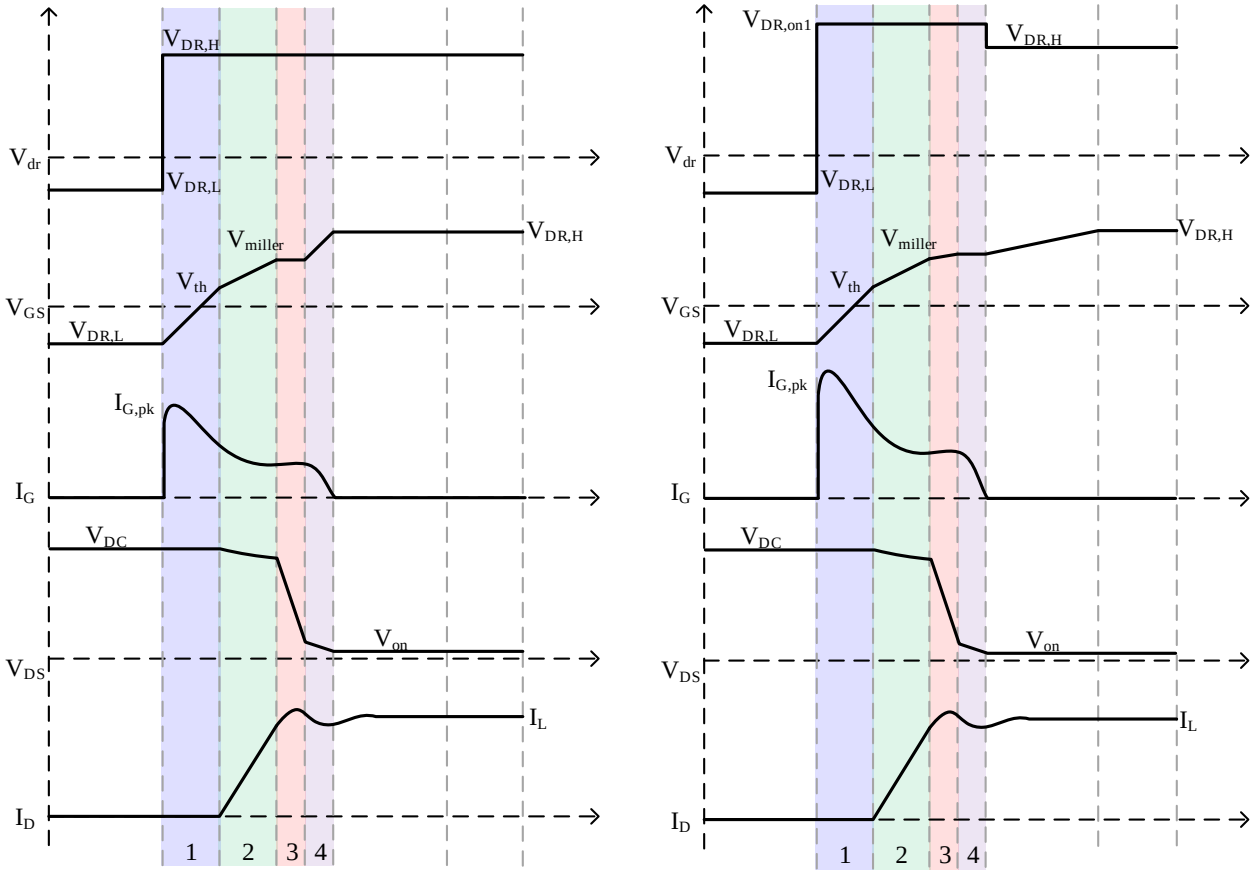
the transition. At turn-off, an intermediate voltage level can be used to reduce *dv/dt* in order to mitigate their interaction with parasitic capacitors in the circuit, and to reduce *di/dt* to reduce the voltage overshoot and stress on the device. This section will describe the methodology and theoretical operation of the multi-level voltage-mode driver.

3.3.1 Methodology of Multi-Level Gate Driver

In this section, the operation of the multi-level (ML) voltage-mode driver is discussed. This solution provides a way of controlling the drive strength during transitions without having to make physical changes to the circuitry, i.e. the gate resistor. This method is utilized differently for turn-on versus turn-off. For turn-on, it is desired to speed up the transitions due to the higher energy losses. Thus, a higher voltage level is utilized at the initial turn-on transition to increase the gate current, and thus the speed at which the input capacitors are charged. During the turn-off transition, the gate voltage is held at an intermediate level between the highest and lowest drive voltages to

Table 3.1. ML gate driver terminology.

V_{DR}	Drive Voltage	The gate driver output voltage
$V_{DR,H}$	High-level drive voltage	V_{GS} that results in the lowest $R_{DS(on)}$
$V_{DR,L}$	Low-level drive voltage	V_{GS} that holds the device low
$V_{DR,on1}$	First turn-on voltage	First voltage level applied at turn-on used to speed up the transition to reduce energy loss
$t_{int,on1}$	Turn-on ML time interval	The duration of $V_{DR,on1}$
$V_{DR,off1}$	First turn-off voltage	The first voltage level applied during the turn-off transient to reduce the turn-off delay
$V_{DR,off2}$	Second turn-off voltage	The second voltage level applied during the turn-off transient to slow down the transitions
$t_{int,off1}$	Turn-off $V_{DR,off1}$ time interval	The duration of $V_{DR,off1}$
$t_{int,off2}$	Turn-off $V_{DR,off2}$ time interval	The duration of $V_{DR,off2}$



(a) *(b)*

Figure 3.7. Transient waveforms for (a) conventional turn-on versus (b) ML turn-on.

slow down the speed. This presents tradeoffs, but slowing down the speed is necessary to control the *di/dt* and *dv/dt* transitions to prevent some of the challenges mentioned in Chapter 2. The operation of the turn-on and turn-off functions of the multi-level driver and the compromise between the reduction of switching speed and the minimization of energy losses are discussed in this section.

The terminology utilized in this section to describe the various voltage levels and time intervals is shown in Table 3.1. For turn-on, only one additional voltage level is evaluated, being

$V_{DR,on1}$. For turn-off, there are two voltage levels, $V_{DR,off1}$ and $V_{DR,off2}$, being the first and second voltage levels, respectively. Both processes are described below.

As shown in Figure 3.7, the waveforms for the multi-level turn-on driver are shown opposite to the normal turn-on waveforms. Due to the higher voltage, the average current during turn-on will be higher than the conventional method. This will result in smaller delay time, current rise time and voltage fall time. This method is easily implemented, as it uses the common voltage-mode driver with an adjustable voltage source to provide the higher initial level.

The variations in *dv/dt* and *di/dt* are shown against the resulting energy losses in Figure 3.8 and Figure 3.9. The *dv/dt* and *di/dt* both increase linearly with $V_{DR,on1}$, while E_{loss} decreases. The optimal voltage level during the turn-on is around 22 to 23 V where the minimal energy loss and *dv/dt* is reached. However, these results were calculated at a single load condition, thus other conditions may change the observed values, but the trend will be the same.

The turn-off multi-level driver waveforms are shown against the conventional turn-off in Figure 3.10. During period (1), the turn-off delay is dependent on the gate current, which decreases

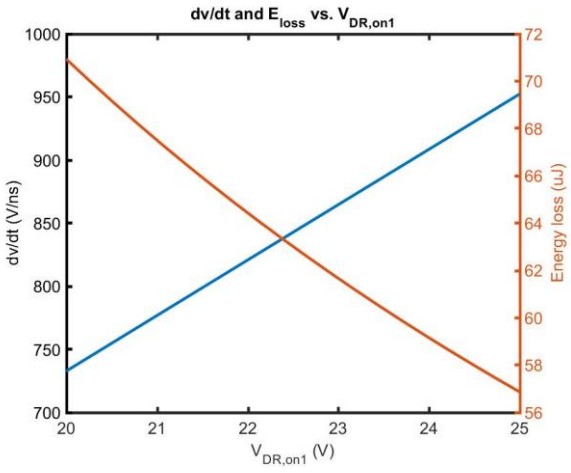


Figure 3.8. dv/dt and E_{loss} versus $V_{DR,on1}$.

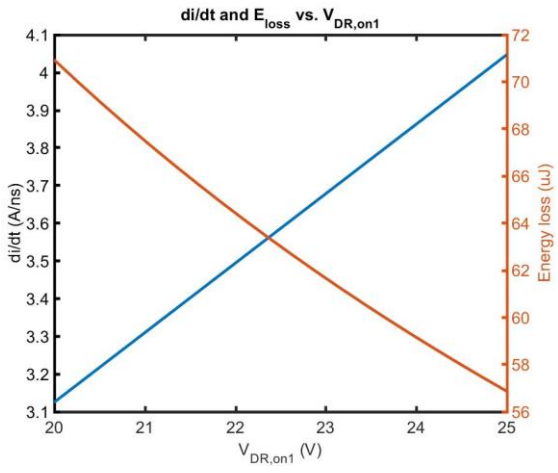


Figure 3.9. di/dt and E_{loss} versus $V_{DR,on1}$.

as the turn-off voltage decreases. Thus, to keep this delay as short as possible, $V_{DR,off1}$ is pulled down to the typical drive voltage, $V_{DR,L}$. During the next four periods, the voltage is brought back up to $V_{DR,off2}$ to slow down *di/dt* and *dv/dt*. This results in the reduction of V_{OS}, as well, due to the decrease of *di/dt*. This method requires the design of $V_{DR,off2}$ such that the energy losses are minimized while slowing the transitions to minimize EMI. The tradeoffs are described using the same equations described for the voltage-mode driver, in which $V_{DR,off2}$ is varied instead of R_G.

By observing the relationships shown in Figure 3.11 and Figure 3.12, $V_{DR,off2}$ should be somewhere in between -2 V and 2 V for this operating point to achieve low losses while still reducing the *dv/dt* and *di/dt*. Additionally, from the relationship between *di/dt* and the commutation

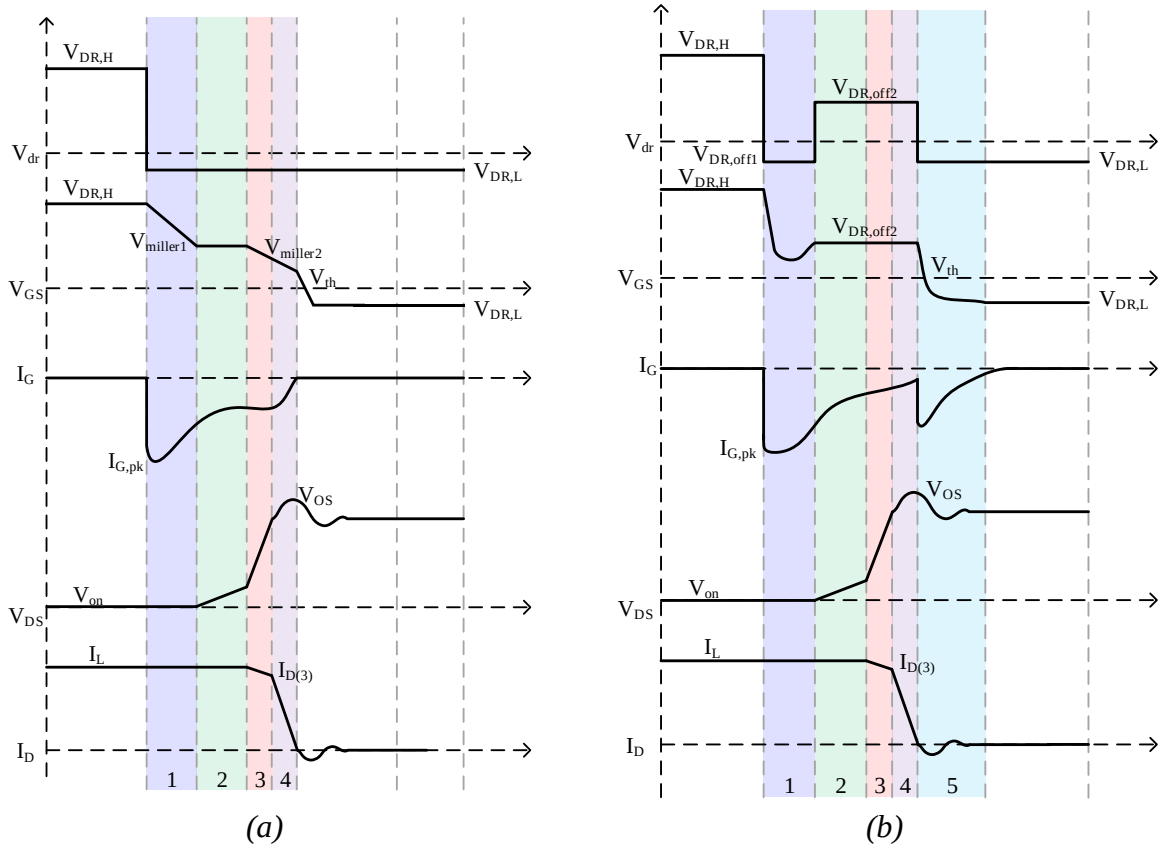


Figure 3.10. Transient waveforms for (a) conventional turn-off versus (b) ML turn-off.

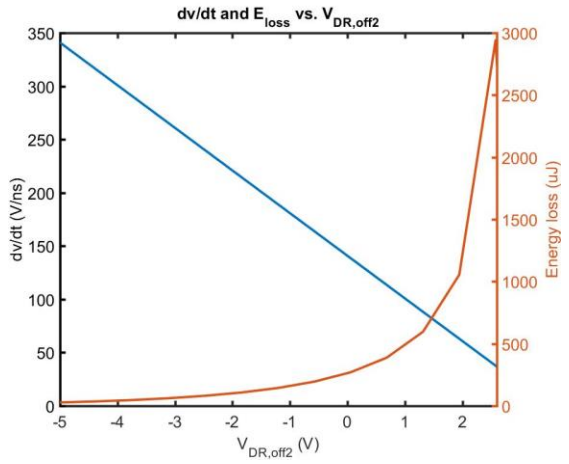


Figure 3.11. dv/dt and E_{loss} versus $V_{DR,off2}$.

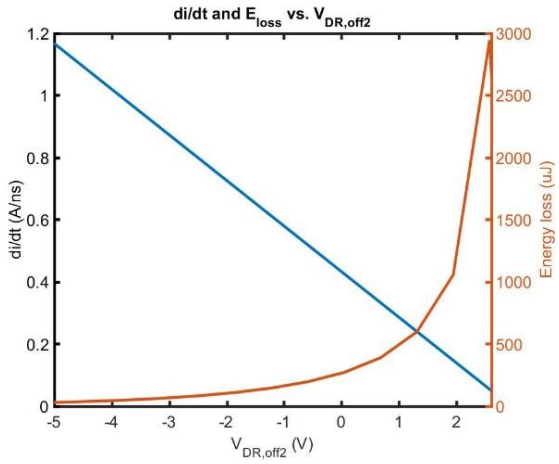


Figure 3.12. di/dt and E_{loss} versus $V_{DR,off2}$.

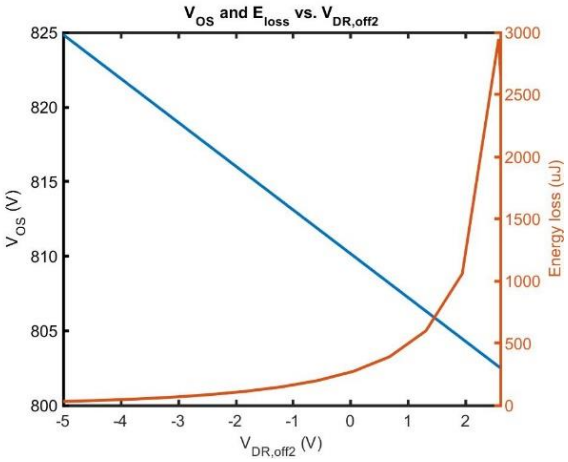


Figure 3.13. V_{OS} and E_{loss} versus $V_{DR,off2}$.

loop inductance, the voltage overshoot reduction is shown in Figure 3.13. Thus, the capability of the multi-level driver to decrease dv/dt and di/dt is shown in these figures, however, the tradeoff needs to be considered in order to minimize energy losses.

3.5 Conclusion

Each driver, voltage-mode, current-mode, and multi-level voltage-mode, were described and the theoretical analysis and equations were given to describe the main transient intervals. The

drivers each provide a methodology to tune the slew rate, being the gate resistance, gate current, or the voltage level. Each driver must be optimized based on the amount of control over *dv/dt* and *di/dt* versus the consequence of increased energy losses. In the following section, each method will be evaluated based on the analytical expressions given in this chapter. The optimal point for each driver will be given based on the analysis.

3.6 References

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CHAPTER 4

COMPARISON OF THE DRIVERS

4.1 Introduction

The acceptance of SiC devices by industry is dependent on the ability to control and utilize them effectively and reliably. As observed in the previous chapter, different gate driver methodologies and variations of the parameters can be used to mitigate the challenges as a result of high *dv/dt* and *di/dt* of these devices. Each provide a method to alter the slew-rates of the SiC MOSFET by changing their drive strengths. From the standpoint of the SiC MOSFET, each driver is doing the same thing; providing a current to charge and discharge its capacitors. However, the drivers themselves all achieve this control in different ways, some of which are influenced by the circuitry around it. This chapter will discuss the differences between these methodologies and their benefits and downfalls. Through the comparison of these methods from the theoretical analysis and simulations, the driver that provides the most control over the slew rates with minimal losses is determined. The simulated results are used to provide supplemental data for the actual performance of the device under test (DUT), as they utilize SiC MOSFET and Schottky diode models.

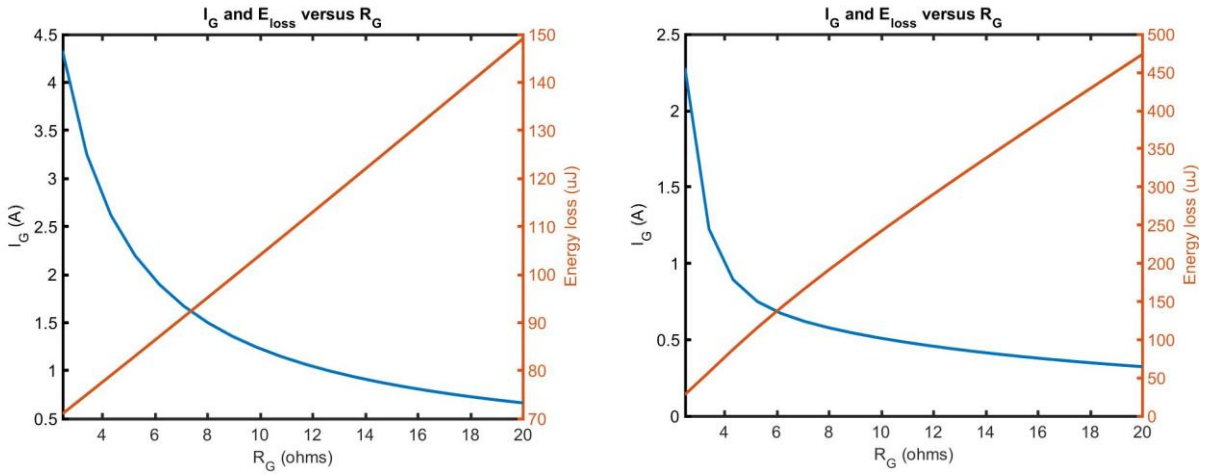
4.2 Comparison

4.2.1 The Conventional Voltage-Mode Driver

As mentioned before, the voltage-mode driver is the most widely used driver type due to its well-developed technology and simple control. However, there are many downfalls to this method and inconveniences when its utilized to drive SiC MOSFETs. The dependence of the voltage-mode driver on the impedance of the gate loop seriously reduces its performance because

of the dependence of drive strength on R_G and L_S, as shown in equations (9) and (33). This can be partially mitigated through board layout, but will not completely relieve the problem, especially if housed in discrete packages, which have additional inductance due to the leads, or even in wire-bonded modules which also introduce parasitic inductance. Uncontrolled resistances will be present in the gate loop aside from the external R_G due to the internal device resistance and gate driver output resistances, which set the maximum available gate current. In the following analysis, it is assumed that the external R_G is the only resistance in the path for the sake of evaluating it as the "control dial" to mitigate harmful *dv/dt* and *di/dt* slew rates. Figure 4.1 shows the average gate current and the energy losses versus R_G for both turn-on and turn-off.

The average gate current during the voltage and current transitions of the SiC MOSFET are affected by R_G, decreasing as R_G increases. As the gate current is reduced, the time at which the input capacitors charge and discharge increases, as shown in Figure 4.1. Subsequently, as the time increases, the energy losses increase, as well. A low gate resistance will result in low energy



(a) turn-on *(b) turn-off*

Figure 4.1. R_G influence on I_G and E_{loss}.

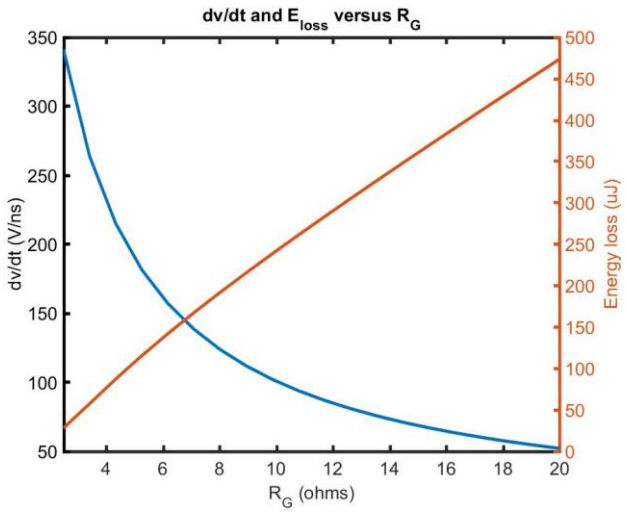


Figure 4.2. R_G influence on dv/dt and E_{loss} at turn-off.

losses, and fast slew rates. This means that the EMI will be higher due to large *dv/dt*, and the voltage overshoot will also be higher, as shown in Figure 4.2. One challenge in the design of this driver is to determine the optimal value for R_G at turn-off, which will reduce voltage overshoot, but will also be small enough to ensure the Miller current, due to high *dv/dt*, will not induce a voltage drop large enough to falsely turn-on the device. This is why an Active Miller Clamp is often used to bypass any large R_G that was designed to minimize the slew rate. According to the analytical results, when the *dv/dt* is reduced to values below 100 V/ns, the energy losses increase by a factor of 10 during the turn-off transition, which may be allowable depending on the application. According to these figures, an optimal R_G value is found somewhere between 6 and 8 ohms.

Although the gate resistor can effectively reduce the slew rates, it may not be the ideal method for the SiC MOSFET. Due to variations in temperature and current, some parameters such as the Miller plateau voltage and threshold voltage will change. In general, the gate resistor is an aspect of the circuit which is constant. Thus, a more variable solution would be better for SiC

MOSFETs. Voltage-mode drivers are beneficial because the control is simple, the technology is well-documented and utilized widely in industry, and gate driver ICs are readily available. However, the performance of the device will be greatly affected by the impedances in the gate loop, being the main downfall of the voltage-mode driver. Thus, the current-mode driver may be a feasible alternative to the voltage-mode driver for SiC MOSFETs, which is shown in the next section.

4.2.2 The Current-Mode Driver

The current-mode driver has some benefits over the voltage-mode driver by providing a constant drive strength throughout the switching transition. Theoretically, this enables the SiC MOSFET to switch at maximum performance with less dependence on gate-loop impedance than the voltage-mode driver [2]. A downside to this method, however, is the complexity of the circuit and the accuracy of the gate current level. It requires optimized control to set the gate current to

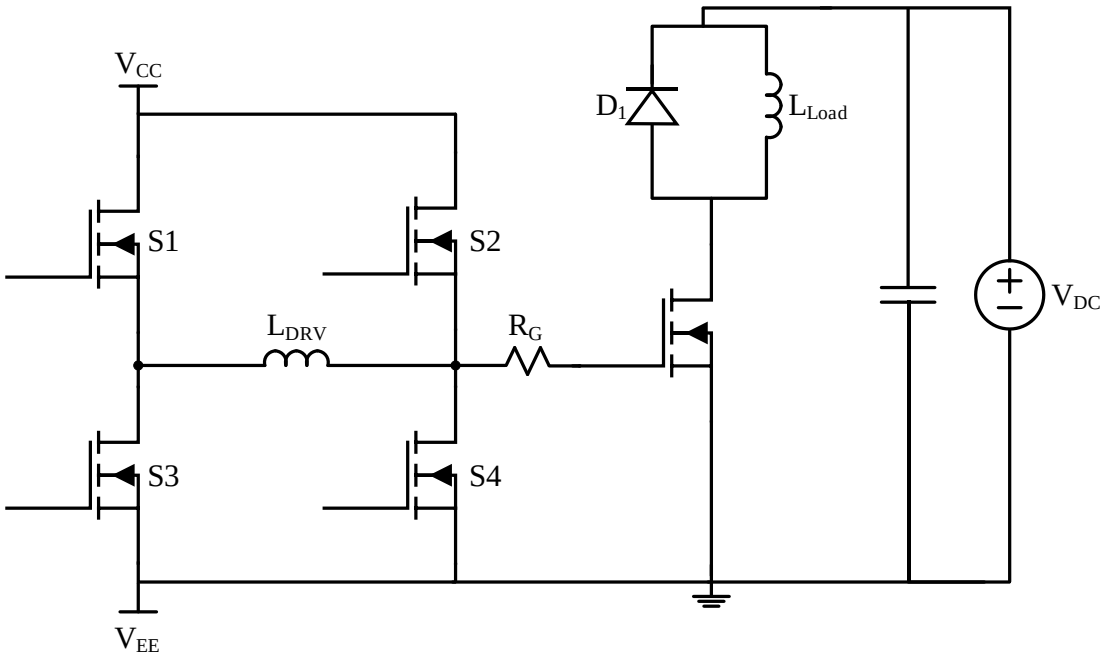


Figure 4.3. Current-source driver based on inductor [1].

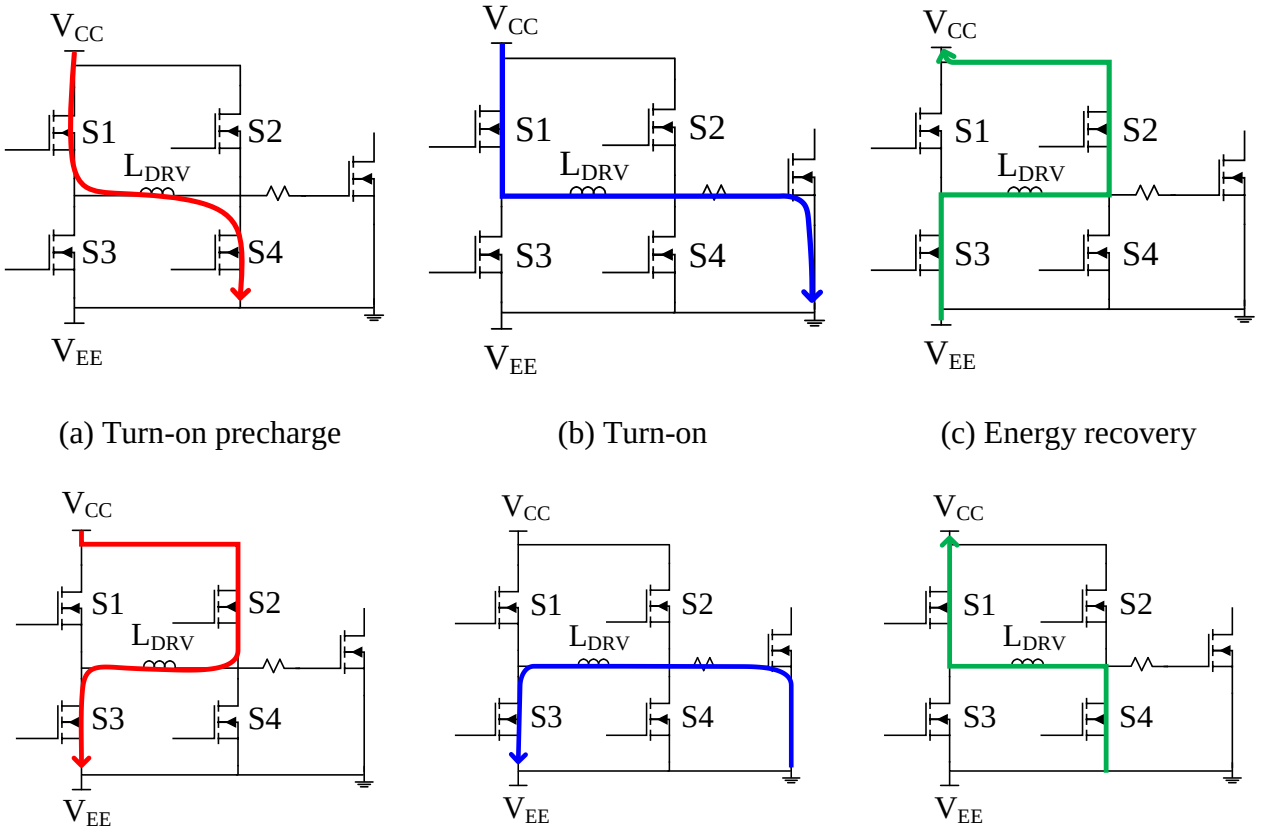
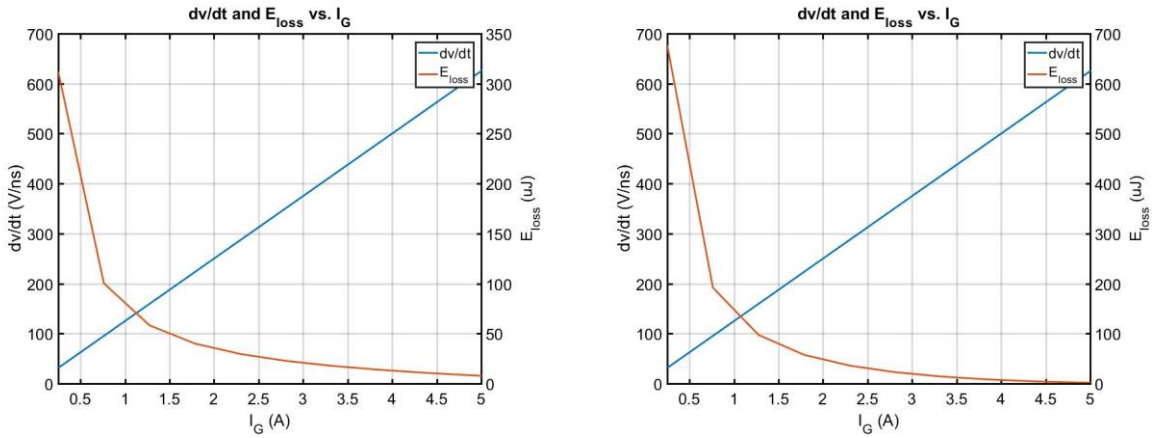


Figure 4.4. Current routes for current-mode driver [1].

drive the gate. An inductor-based topology may be used, as shown in Figure 4.3, because it allows the high and low drive voltage to be chosen by the designer, thus the voltage can be clamped at -5 V during turn-off to reduce the chance for false-turn-on [1].

S1 through S4 are used to control the charge and discharge of the driver inductor, L_{DRV}. V_{CC} and V_{EE} can be set as the recommended voltages shown on the SiC MOSFET's datasheet. The driver operates in discontinuous conduction mode to reduce the losses of L_{DRV}. The inductor must be sized appropriately to provide the necessary current to drive the device in a short period of time. This is called the pre-charging stage, which brings the inductor current up to the desired value.



(a) turn-on *(b) turn-off*

Figure 4.5. I_G influence on dv/dt and E_{loss}.

The amount of pre-charge time may increase the minimum allowable switching frequency. The control for this topology is not simple due to the number of switches and uncommon switching technique, thus a high-speed controller should be used to generate these pulses for best results. The current routes for this topology are shown in Figure 4.4.

Through the use of a constant current at the gate, the driver is able to switch the SiC MOSFET at consistent rates independently of variations in the Miller plateau due to changes in current [2]. This is the main difference between the current-mode and voltage-mode driver. Additionally, R_G and L_S do not affect the driver strength as they did with the voltage-mode driver. As shown in Figure 4.5, the energy losses are very low, and are similar to the levels observed from the voltage-mode driver in the same current range. The losses are further reduced as I_G increases, while *dv/dt* increases, and consequently EMI. To reduce *dv/dt*, the gate current must be reduced, and energy losses will increase. In this case I_G serves as the control dial of the current-mode driver, and the comparison of this method to the others will be further examined in Section 4.2.4.

4.2.3 The Multi-Level Voltage-Mode Driver

As discussed in the previous chapter, the multi-level voltage-mode driver provides a way to vary the drive strength by simply using the voltage level, V_{DR}, to control the transients and losses. A downfall of this method is that the energy losses are found to be much higher than the other two methods. Additionally, if the duration is not properly chosen, the driver may prevent very high switching frequencies. However, high-voltage applications utilizing 10 kV SiC MOSFETs are expected to switch in the range of 3 to 10 kHz, so switching losses may not be as much of a concern in comparison to the need to reduce EMI [3]. Thus, if the tradeoffs are carefully considered for this driver, the additional switching losses may be allowable with respect to the amount of slew rate control it provides.

Aside from the voltage and current levels, the main contributor to *di/dt* and *dv/dt* is the '*dt*' or duration of those voltage and current transitions, which is affected by the gate current. In this method, the gate current is controlled with the drive voltage, V_{DR}. As discussed in the previous chapter, the main transitions of interest during turn-on are the rise of I_D and the fall of V_{DS}. In these instances, the duration is controlled by $V_{DR,on1}$, as shown in the waveforms of Figure 3.7. For turn-on voltages beyond the typical 20 V, the gate current will increase and the losses will decrease. However, pushing the device past its maximum rating may cause additional stress on the gate oxide, and result in degradation over time. Additionally, though a lower turn-on voltage may be used to reduce slew rate, such as in the range from 15 to 20 V, it will increase the conduction losses. Thus, this study considered only the range of 20 to 25 V in order to minimize the conduction losses, and remain within the device's maximum ratings. Figure 4.6 shows the *dv/dt* and losses versus $V_{DR,on1}$ for the turn-on transition.

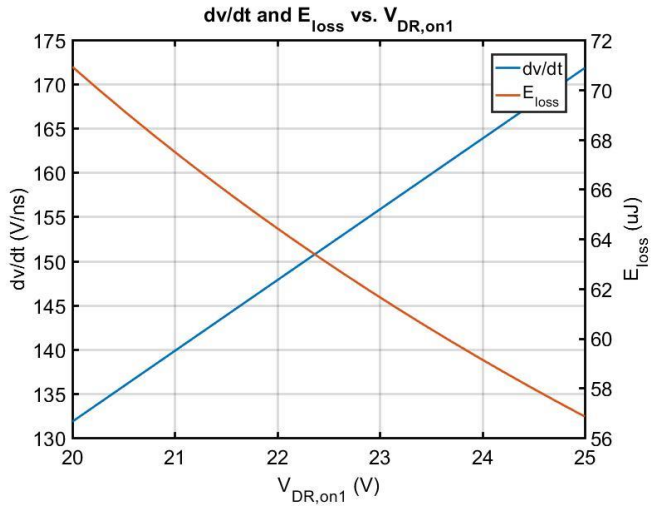


Figure 4.6. $V_{DR,on1}$ influence on dv/dt and E_{loss}.

For turn-off, there is a wide range of voltage levels which can be used to reduce the *dv/dt* and *di/dt* ranging anywhere from -5 V to 20 V. However, there are limitations to this voltage range due to the amount of losses incurred and the ability to turn-off the device. During a normal turn-off period, V_{GS} will have a plateau voltage around 3 or 4 V at 20 A, for the CREE® 1.2 or 1.7 kV SiC MOSFETs, according to equation (5). As shown in the previous chapter, the gate current for

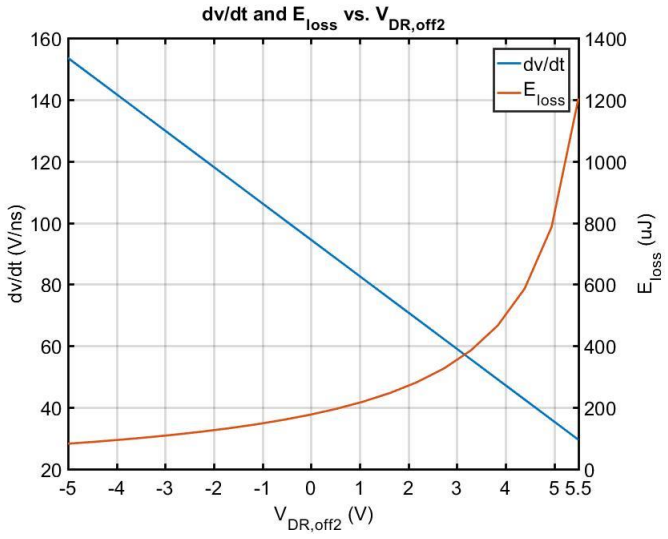


Figure 4.7. $V_{DR,off2}$ influence on dv/dt and E_{loss} during turn-off.

the conventional voltage driver is related to the voltage difference between the plateau voltage and $V_{DR,L}$. In the case of the multi-level driver, $V_{DR,L}$ is no longer constant, but is changed to an alternate voltage during the voltage rise time, called $V_{DR,off2}$. As $V_{DR,off2}$ increases from -5 V, the turn-off duration becomes longer, and energy losses will increase. $V_{DR,off2}$ should be set at a value between the Miller plateau voltage and the threshold voltage to minimize the time of turn-off and to maximize the reduction of *dv/dt*. For example, if the drain current is 20 A, the Miller plateau voltage is around 3.5 V, so $V_{DR,off2}$ should be between 2.6 and 3.5 V to minimize *dv/dt* while still minimizing E_{loss}.

The energy losses can be divided into two main periods, during the voltage rise time and the current fall time. During the current fall time, the gate current is affected by the source inductance due to the voltage drop across it. For every 1 nH of source inductance in the gate-loop and with a *di/dt* of 3 A/ns there is a 3 V drop. This drastically decreases the gate current, and increases energy losses. Additionally, with the same *di/dt*, the voltage overshoot across the device will increase based on the power loop inductance; where 20 nH would result in a voltage overshoot of 60 V. In order to decrease the *di/dt*, $V_{DR,off2}$ should be held during both the voltage rise and current fall times. However, it should be noted that when $V_{DR,off2}$ increases past 0 V, the energy losses increases much more, as shown in Figure 4.7. Thus, future designs should consider a dynamically varying $V_{DR,off2}$ in order to reduce the losses during the current fall time.

4.2.4 Comparison of the Drivers

The three drivers were all shown to provide slew-rate control over the transients of the SiC MOSFET. Each have benefits and downfalls with regards to the complexity of the circuit and control, as well as each driver's immunity to changes in temperature or load conditions. In this section, each driver's ability to control *dv/dt* and *di/dt* will be evaluated. The tradeoff between

Table 4.1. Effects of gating method on E_{loss}, dv/dt and di/dt.

Gating Method	**Variable**	**Effect on E_{loss}**	**Effect on *dv/dt* and *di/dt***
Voltage-Mode	$R_G \uparrow$	↑	↓
Current-Mode	$I_G \uparrow$	↓	↑
Multi-Level Voltage-Mode	$V_{DR} \uparrow$	↑	↓

higher switching losses and the slew rate minimization is the main concern. Energy losses should be minimally affected by each change in R_G, I_G, or V_{DR}. This section will define a ratio which will be utilized to describe how much E_{loss} changes with changes in the slew rate. From the above discussion, the relationships shown in Table 4.1 were found. Now, the dependence of these parameters will be discussed.

Using the equations given in Chapter 3, the parameters E_{loss}, *dv/dt* and *di/dt* were found for each driver with changes in their respective independent variable, being either R_G, I_G or V_{DR}, across a range of values. To compare the parameters side-by-side, each curve was normalized against the maximum value. The trends for turn-on are shown in Figure 4.8, Figure 4.9, and Figure 4.10 where the y-axis is the normalized value of the parameter and the x-axis is the range of values for a given driver. The turn-off trends for each driver are shown in Figure 4.11, Figure 4.12, and Figure 4.13. For the non-linear curves, the line was divided into multiple regions, indicated by a red triangle, and each region was linearized for comparison.

For the voltage-mode driver, the gate resistor was varied from 2.5 to 20 Ω as shown in Figure 4.8, with values shown in reverse order in a direct comparison to the other driver methods.

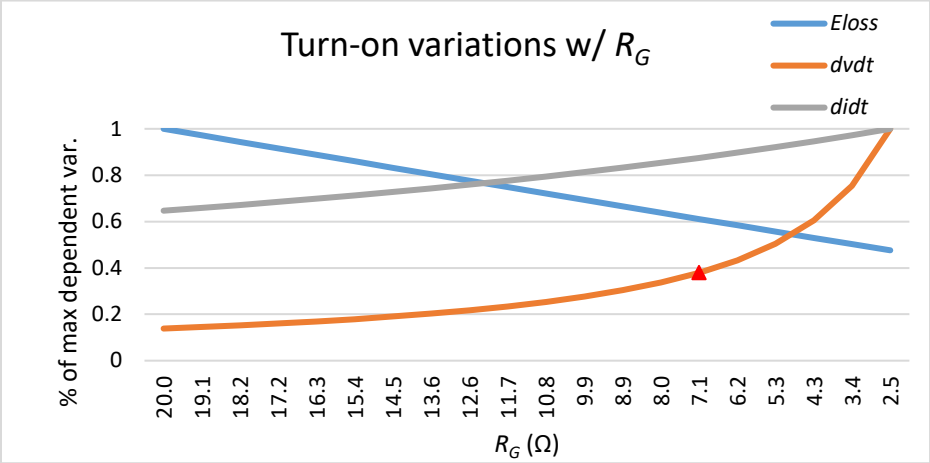


Figure 4.8. Turn-on variations dependent on R_G.

Table 4.2. Turn-on dependence on R_G.

Ratio	R_G = 2.5 – 7.1 Ω	R_G = 7.1 – 20 Ω
E_{loss} : *dv/dt*	-0.222	-1.40
E_{loss} : *di/dt*	-1.48	-1.48

The maximum values of the parameters in the plot for E_{loss}, *dv/dt* and *di/dt* are 96 µJ, -730 V/ns and 3.24 A/ns, respectively. The energy losses decrease linearly as R_G decreases, while *di/dt* increases linearly. The *dv/dt* rate of change was divided into two regions, before and after 7.1 Ω. When R_G is lower than 7.1 Ω, the *dv/dt* rate increases. This means that during the time between 2.5 Ω and 7.1 Ω, the energy losses will not increase much with respect to the amount of *dv/dt* reduction. As a result, the slopes of E_{loss} versus *dv/dt* and E_{loss} versus *di/dt* were introduced as ratios, which describe the amount of change in E_{loss} versus *dv/dt* and *di/dt*. The resulting values are

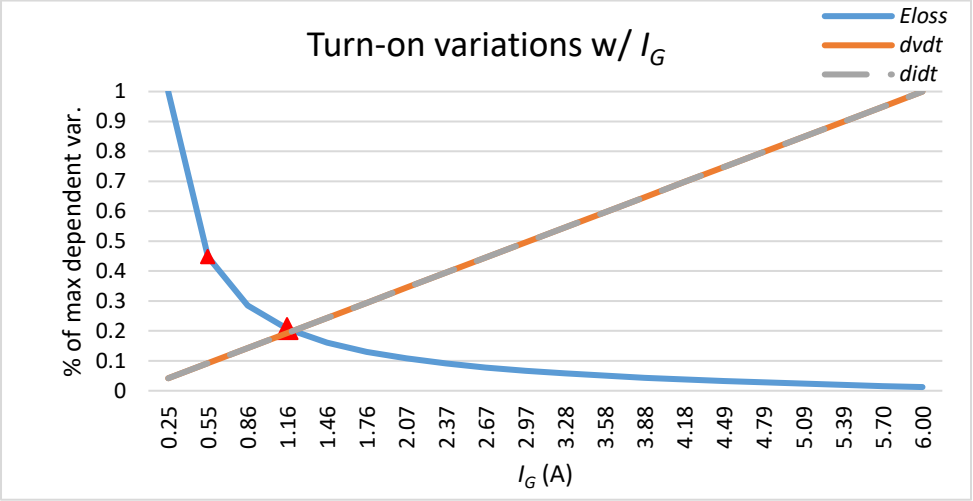


Figure 4.9. Turn-on variations dependent on I_G.

Table 4.3. Turn-on dependence on I_G.

Ratio	I_G = 0.25 – 0.55 A	I_G = 0.55 – 1.16 A	I_G = 1.16 – 6 A
E_{loss} : *dv/dt*	-10.95	-2.38	-0.241
E_{loss} : *di/dt*	-10.95	-2.38	-0.241

given in Table 4.2. In this case, it would be more beneficial to keep R_G within the range of 2.5 to 7.1 Ω to keep losses to a minimum.

The same methodology was applied to the current-mode driver. In this case, I_G ranges from 250 mA to 6 A. The maximum values for E_{loss}, *dv/dt* and *di/dt* are 192.04 µJ, 750 V/ns and 35 A/ns, respectively. In this case, the energy losses are non-linearly decreasing as I_G increases, shown

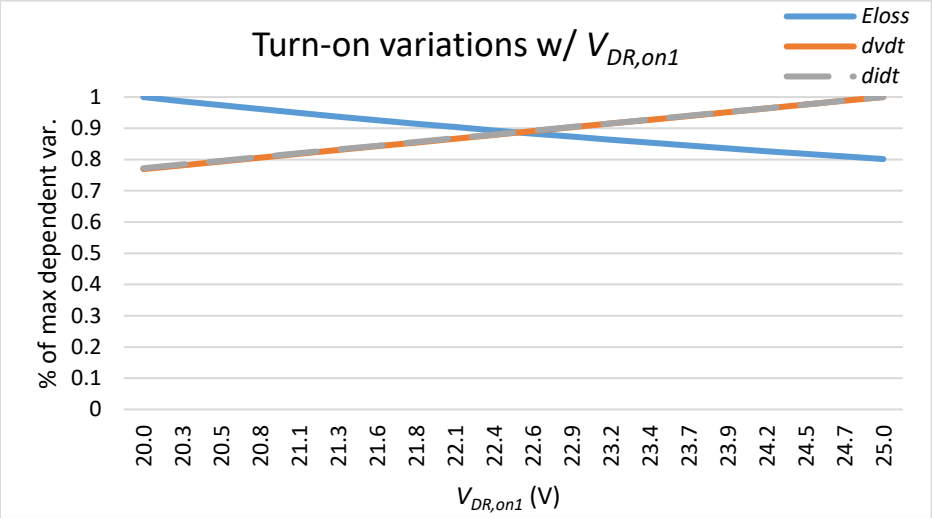


Figure 4.10. Turn-on variations dependent on $V_{DR,on1}$.

Table 4.4. Turn-on dependence on $V_{DR,on1}$.

Ratio	$V_{DR,on1}$ = 20 – 25 V
E_{loss} : *dv/dt*	-0.860
E_{loss} : *di/dt*	-0.870

in Figure 4.9. The slope was divided into three regions, as indicated by the red triangles in the figure, while *dv/dt* and *di/dt* increase at the same rate. The ratios are given in Table 4.3.

In this case, the energy losses will increase the most in the first region, below 550 mA. In the range of 1.16 to 6 A, the energy losses do not change much as *dv/dt* and *di/dt* change, so this would be the optimal region for controlling the slew rate.

Finally the multi-level voltage-mode driver for turn-on was evaluated in which $V_{DR,on1}$ ranges from 20 to 25 V, as shown in Figure 4.10. The maximum losses, *dv/dt* and *di/dt* are 47.93

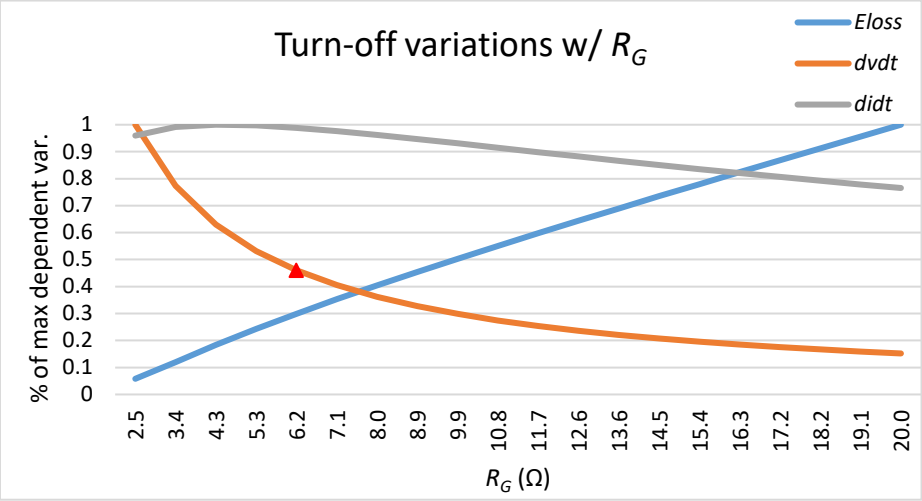


Figure 4.11. Turn-off variations dependent on R_G.

Table 4.5. Turn-off dependence on R_G.

	R_G = 2.5 – 6.2 Ω	R_G = 6.2 – 20 Ω
E_{loss} : *dv/dt*	-0.338	-2.52
E_{loss} : *di/dt*	-4.84	-4.84

µJ, 947.73 V/ns and 4.045 A/ns, respectively. All parameters vary linearly, and thus the ratios can be found directly, as shown in Table 4.4.

Due to the small range of values utilized here, for reasons mentioned in previous sections, the changes in losses and slew rates are almost the same, with change in loss being slightly smaller than the change in slew rates.

Next the turn-off parameters are evaluated for the three drivers. To begin with, the voltage-mode driver curves are shown in Figure 4.11. *dv/dt* and *di/dt* decrease as the gate resistance goes up, and *dv/dt* is divided into two regions due to the knee which occurs around 6.2 Ω. The ratios are shown in Table 4.5.

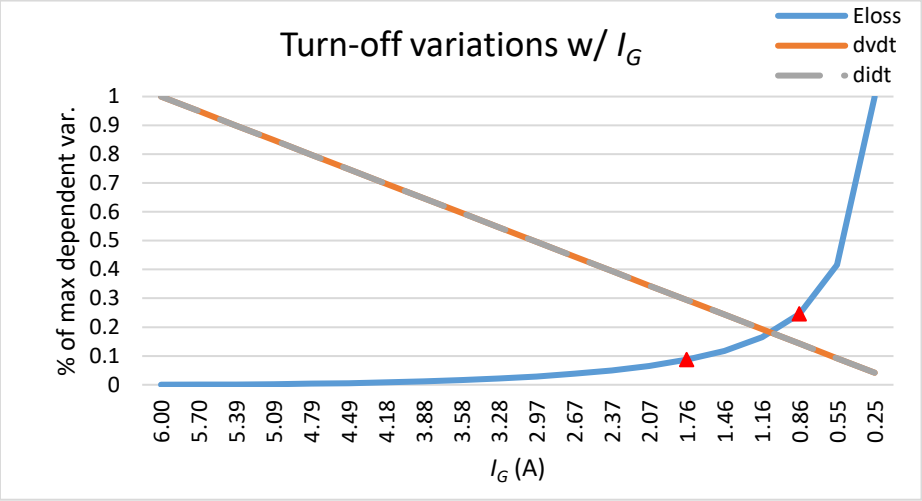


Figure 4.12. Turn-off variations dependent on I_G.

Table 4.6. Turn-off dependence on I_G.

	I_G = 1.76 – 6 A	I_G = 0.86 – 1.76 A	I_G = 0.25 – 0.86 A
E_{loss} : *dv/dt*	-0.155	-1.27	-7.48
E_{loss} : *di/dt*	-0.155	-1.27	-7.48

It is found that within the region from 2.5 Ω to 6.2 Ω, the *dv/dt* will decrease at a rate faster than energy losses increase. Thus, this region would be optimal region for slew rate control.

The gate current method was varied in the same range as turn-on as shown in Figure 4.12. Both *dv/dt* and *di/dt* decrease at the same rate as the gate current decreases. The energy losses are divided into three regions and are linearized. In the region below 860 mA, the losses increase at a high rate, so it is not suggested that current in this range be used. The ratios are given in Table 4.6. From the results it is obvious that the optimal values for I_G lie between 1.76 and 6 A.

Finally, the multi-level voltage-mode driver at turn-off was evaluated with $V_{DR,off2}$ ranging from -5 to 5.5 V. E_{loss}, *dv/dt* and *di/dt* are 291 µJ, 341.3 V/ns, and 1.16 A/ns, respectively. In this

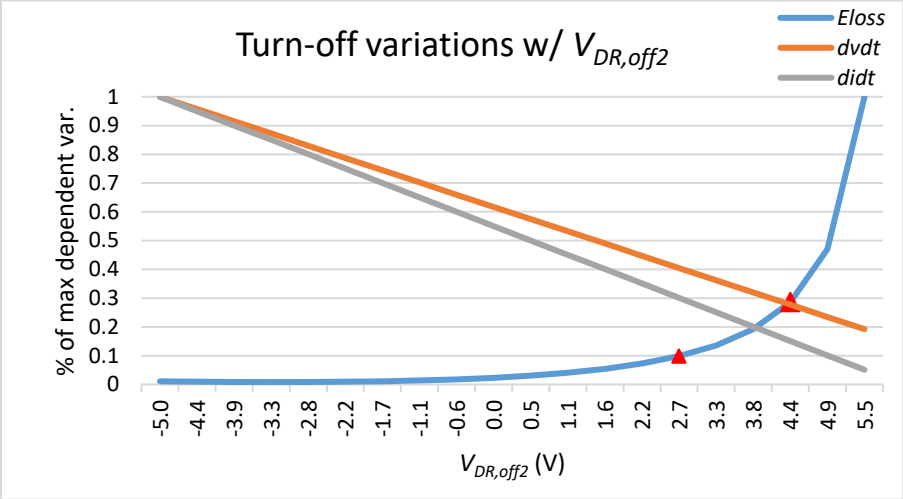


Figure 4.13. Turn-off variations dependent on $V_{DR,off2}$.

Table 4.7. Turn-off dependence on $V_{DR,off2}$.

	$V_{DR,off2}$ = -5 – 2.7 V	$V_{DR,off2}$ = 2.7 – 4.4 V	$V_{DR,off2}$ = 4.4 – 5.5 V
E_{loss} : dv/dt	-0.147	-1.76	-12.46
E_{loss} : di/dt	-0.125	-1.50	-10.62

case, E_{loss} and di/dt are described by linear changes while dv/dt is divided by two regions, signified by the red triangle in Figure 4.13. It is optimal that the value of $V_{DR,off2}$ be kept below 4.4 V in order to keep the energy losses as close to the base value as possible. The ratio results are given in Table 4.7.

Figure 4.14 shows the comparison between the ratios found for E_{loss} versus dv/dt for turn-on and turn-off in each driver category. For turn-on, the voltage mode and current mode drivers show the lowest change in E_{loss} compared to the multi-level driver. The current-mode driver also was able to reduce the dv/dt and di/dt the most when I_G is 1.16 A with both slew rates reducing to 19% of the maximum level.

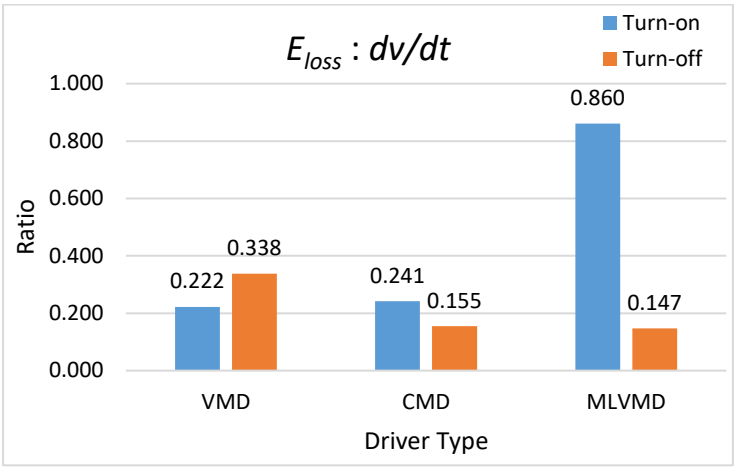


Figure 4.14. E_{loss}:dv/dt ratio comparison.

For turn-off, the multi-level driver shows the best performance next to the voltage-mode driver. The multi-level driver, when $V_{DR,off2}$ is at 2.7 V, reduced the *dv/dt* to 40% of the maximum, while the conventional method with R_G at 6.2 Ω, reduced the *dv/dt* to 45% of the maximum.

Figure 4.15 shows the comparison of ratios for E_{loss} to *di/dt* for each driver. The best performance at turn-on is the current-mode driver, which was able to reduce *di/dt* to 19% of its maximum. At turn-off, the multi-level voltage-mode driver reduced the *di/dt* to 30% of its maximum while the current-mode driver reduced it to 29% of its maximum. The voltage-mode driver is able to reduce the *di/dt*, but is not as effective as the other methods within the given range.

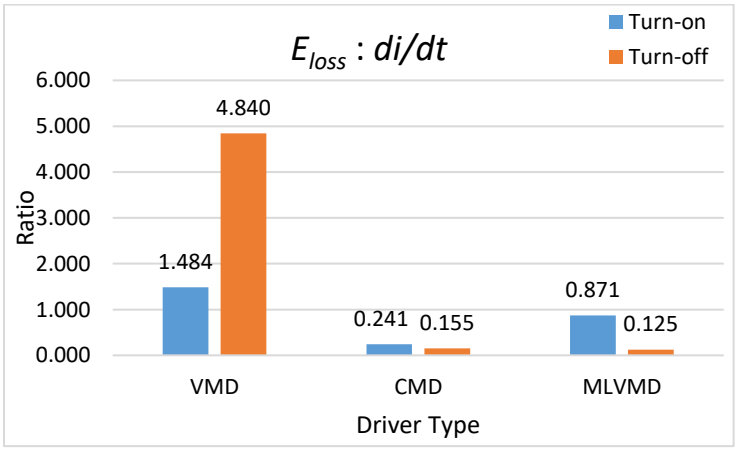


Figure 4.15. E_{loss}:di/dt ratio comparison.

Using this analysis, the optimal point for each driver has been given based on minimal energy losses and maximum reduction of *dv/dt*, and are given in Table 4.8. From the table, it is shown that at turn-on, the best driver is the current-mode driver, which has the lowest energy losses and *dv/dt* out of the three drivers. Although the *di/dt* is still higher at turn-on, the interaction with parasitic inductors can be mitigated through board layout.

For turn-off, the driver with the lowest losses is the current-mode driver, but the *dv/dt* and *di/dt* are still high. The voltage-mode driver and multi-level voltage-mode drivers have almost the same energy losses and similar *dv/dt* while the *di/dt* level is lower for the multi-level driver. The *dv/dt* reduction is important for EMI mitigation while reducing *di/dt* will help to reduce voltage

Table 4.8. Comparison of optimal operating points for each driver.

Turn-on				
Method	**Value**	E_{loss} **(µJ)**	***dv/dt*** **(V/ns)**	***di/dt*** **(A/ns)**
Voltage-Mode	R_G = 7.1 Ω	58.88	-276.9	2.83
Current-Mode	I_G = 1.76 A	39.77	-144.75	6.84
Voltage-Mode	$V_{DR,on1}$ = 20 V	47.3	-743.1	3.17
Turn-off				
Method	**Value**	E_{loss} **(µJ)**	***dv/dt*** **(V/ns)**	***di/dt*** **(A/ns)**
Voltage-Mode	R_G = 6.2 Ω	87.30	156.97	-1.14
Current-Mode	I_G = 1.76 A	34.72	220.43	-10.42
Voltage-Mode	$V_{DR,off2}$ = 2.7 V	88.74	210.77	-0.489

overshoot, as discussed previously. For turn-off voltage-mode drivers, the comparison between the conventional method and multi-level method will be further investigated.

Based on the trends at turn-on, through the ratio comparison, the current-mode driver showed the smallest change in E_{loss} and also has the smallest magnitude of E_{loss} and *dv/dt* when compared to the other methods at the optimal current value of 1.76 A. For turn-off, the voltage-mode drivers both reduced the *dv/dt* versus E_{loss} at similar rates, but in the comparison from Table 4.8, the conventional driver showed lower *dv/dt* at the chosen point. The initial conclusion from the theoretical standpoint is that the current-mode driver best serves turn-on, while the voltage-mode driver, either conventional or multi-level, best serve the turn-off.

4.3 Simulated Results

Through the use of device models, simulations can be used to investigate the expected performance of a device or circuit before physical implementation. This gives designers the ability to try multiple methods without the time spent fabricating circuits and testing. The theoretical model used to compare the drivers in the previous section offers an accurate portrayal of the performance of each driver. However, it is advantageous to use device models to develop a more accurate view of the effects of the driver on types of devices or converter topologies as there are some discrepancies between real and calculated values. Thus, the voltage-mode and current-mode drivers described in Chapter 3 were simulated using the double pulse test (DPT) circuit. The DPT is a clamped inductive load circuit which is used to characterize a device's switching transients. The MOSFET is switched on for a duration corresponding to the desired load current condition through the charging of the inductor, through the relationship: $V = L * \frac{di}{dt}$. The device is then switched off, showing the turn-off transition of interest, and is consequently switched back on

again to observe the turn-on transition at the same operating point. The device models for simulation were provided by CREE Wolfspeed™ and were chosen based on the devices utilized in the experimental verification. The simulation parameters are shown in Table 4.9.

For the voltage-mode drivers, both conventional and multi-level, the piecewise linear (PWL) function is used to generate the drive voltages. For the conventional driver, the gate driver was simulated using R_G ranging from 2.5 to 20 Ω. For the multi-level driver, the turn-on voltage, $V_{DR,on1}$, ranged from 20 to 25 V, while the turn-off voltage, $V_{DR,off2}$, ranged from -5 to 6 V. For the multi-level driver, an external gate resistor of 10 Ω was used.

The waveforms using multi-level turn-on are shown in Figure 4.16. During turn-on, the *dv/dt* and *di/dt* levels are controlled through the use of a high initial voltage level, $V_{DR,on1}$. If this level is chosen to be higher than 20 V, the energy losses are reduced and the slew rates increases. In Table 4.10 the results are compared against the conventional method, in which R_G is used.

Table 4.9. Simulation parameters.

DUT	C2M0045170D
Upper Device	C4D40120D
L_S	2.5 nH
L_D	4.5 nH
L_G	2.5 nH
$R_{G,ext}$	10 Ω
I_L	20 A
V_{DC}	600 V

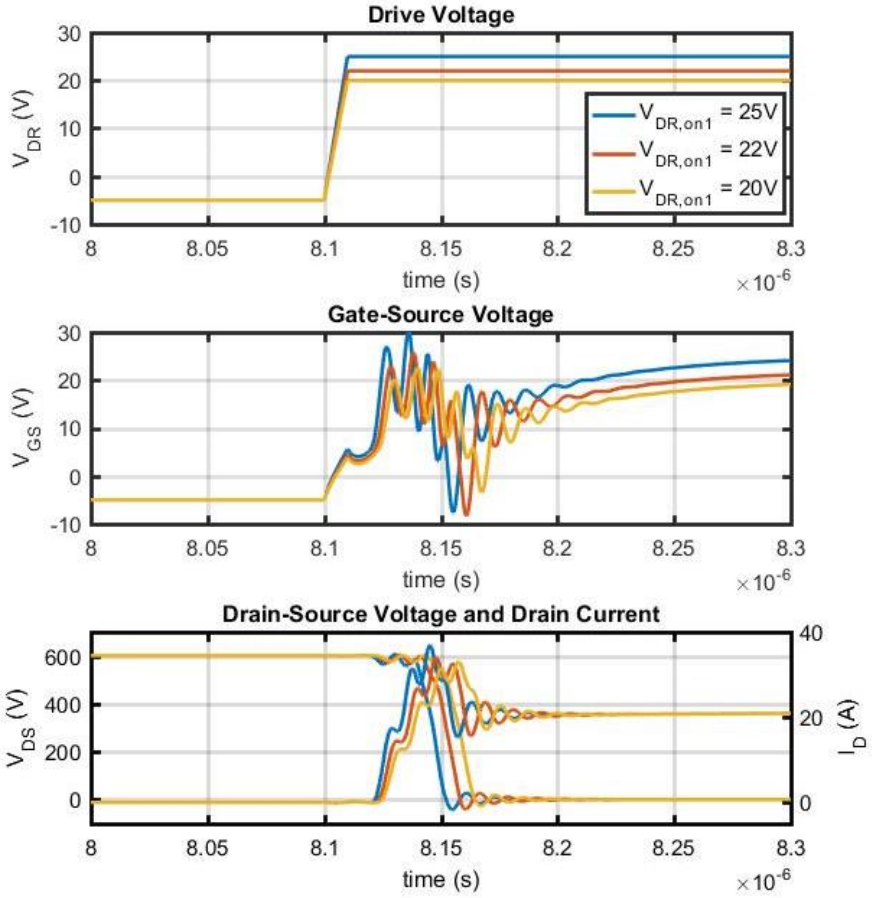


Figure 4.16. V_{DR}, V_{GS}, V_{DS} and I_D using ML turn-on.

The simulated drive waveforms using multi-level turn-off are shown in Figure 4.17. Three

Table 4.10. Turn-on comparison of voltage-mode drivers.

Turn-on			
Param.	***E_{loss}* (µJ)**	***dv/dt* (V/ns)**	***di/dt* (A/ns)**
R_G = 2.5 Ω	276.63	-87.92	4.98
R_G = 5 Ω	310.68	-51.13	3.95
R_G = 20 Ω	438.44	-35.20	0.803
$V_{DR,on1}$ = 20 V	369.53	-45.11	2.02
$V_{DR,on1}$ = 22 V	333.32	-51.44	2.49
$V_{DR,on1}$ = 25 V	301.75	-53.92	2.99

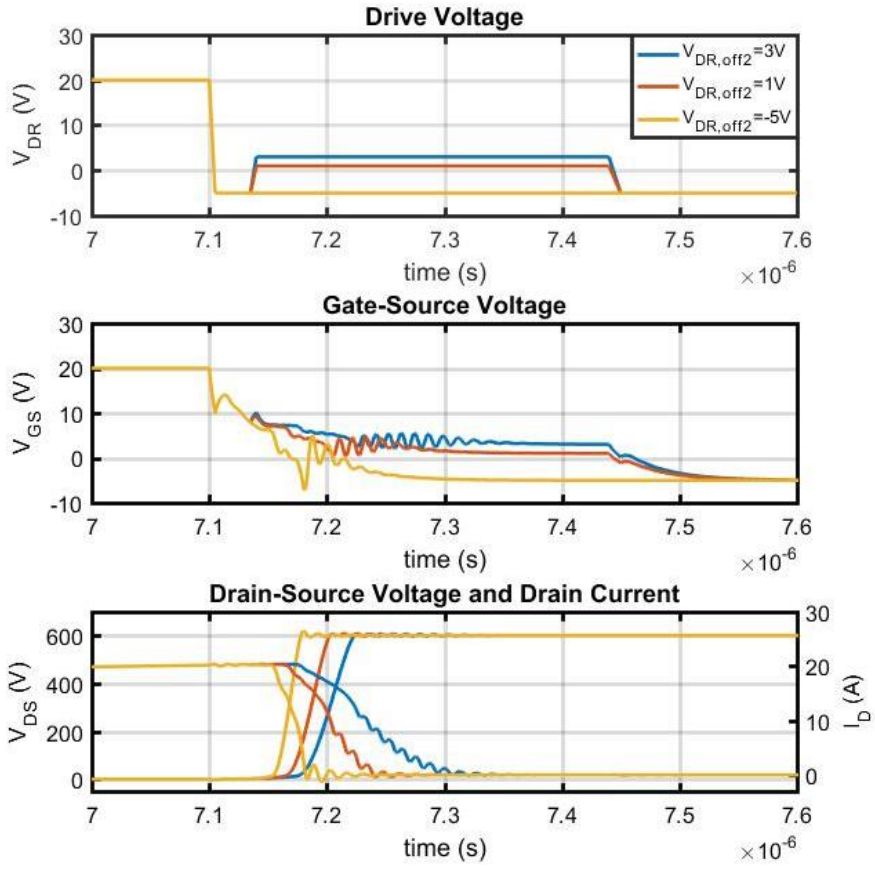


Figure 4.17. V_{DR}, V_{GS}, V_{DS} and I_D for ML turn-off.

cases are shown when $V_{DR,off2}$ is 3 V, 1 V and the conventional -5 V. Both the *dv/dt* and *di/dt* show

Table 4.11. Turn-off comparison of voltage-mode drivers.

Turn-off			
Param.	***E*$_{loss}$ (µJ)**	***dv/dt* (V/ns)**	***di/dt* (A/ns)**
R_G = 2.5 Ω	62.50	53.99	-3.28
R_G = 5 Ω	113.80	45.80	-1.34
R_G = 20 Ω	270.50	27.54	-0.299
$V_{DR,off2}$ = 0 V	169.57	23.38	-0.558
$V_{DR,off2}$ = 1.5 V	248.86	20.07	-0.562
$V_{DR,off2}$ = 3.5 V	490.49	14.68	-0.207
$V_{DR,off2}$ = 5.5 V	1467.80	8.36	-0.068

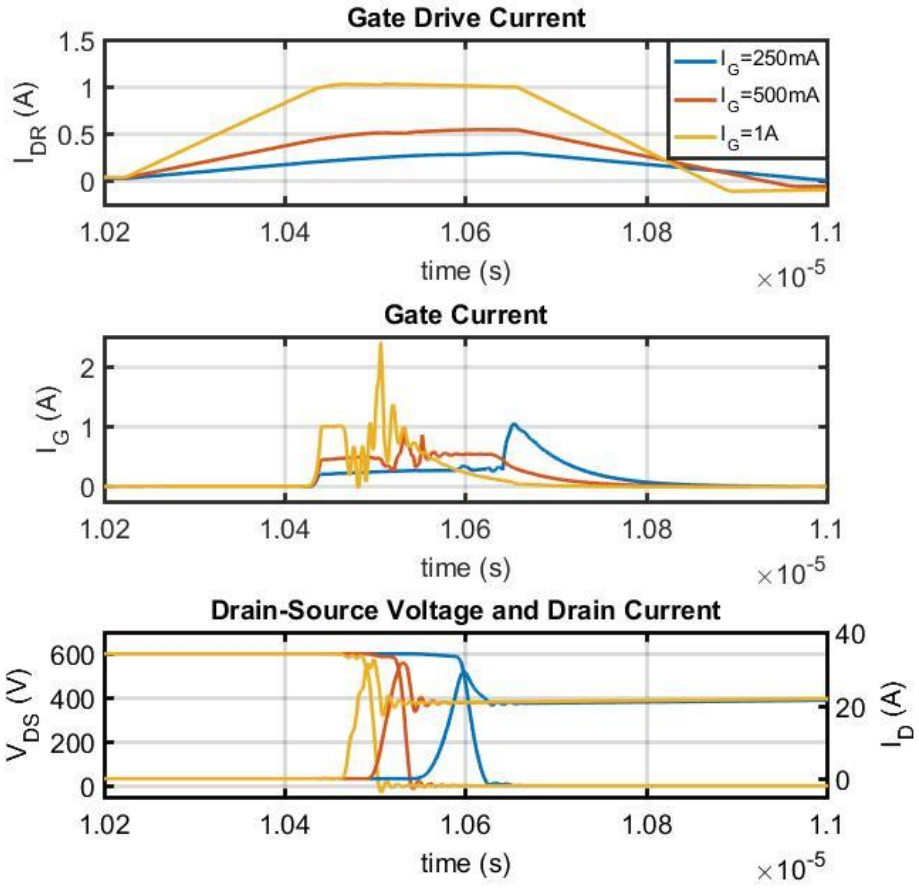


Figure 4.18. Current-mode driver at turn-on.

a visible reduction when $V_{DR,off2}$ is 1 V or 3 V versus the conventional case. The switching losses are shown to increase greatly just through observation of the area beneath the V_{DS} and I_D curves in the figure. The comparison of this method to variations in R_G is shown in Table 4.11.

The simulated current-mode driver is the inductor-based topology which was shown in Figure 4.3 and the operation is as described in the Section 4.2.2. The gate current was controlled by varying the driver inductance and was tested from 250 mA to 2 A. It was found through simulation that, using the topology from Figure 4.3, the control of gate current was no longer possible after 2 A due to the voltage drop across the external and internal gate resistors in the gate-

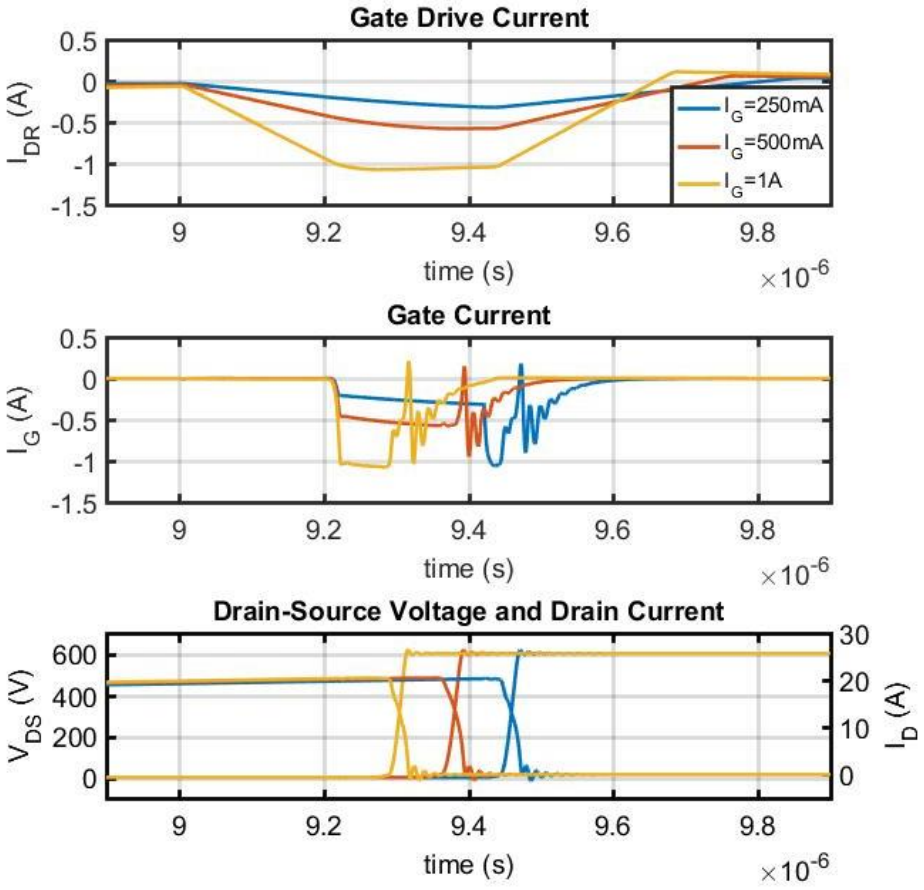


Figure 4.19. Current-mode driver at turn-off.

loop path. This is a deficiency of the current-mode driver topology because the voltage must be increased dynamically to provide a constant level of current throughout the transition.

Table 4.12. Current-mode driver simulated results.

	Turn-on			**Turn-off**		
I_G	E_{loss} **(µJ)**	***dv/dt* (V/ns)**	***di/dt* (A/ns)**	E_{loss} **(µJ)**	***dv/dt* (V/ns)**	***di/dt* (A/ns)**
250 mA	464.05	-22.32	0.516	78.70	31.65	-1.37
500 mA	366.07	-46.56	0.989	86.89	30.79	-1.37
1 A	357.34	-48.45	1.69	74.09	32.84	-1.44
2 A	352.02	-48.87	2.37	72.88	33.17	-1.41

The gate current is generated by charging and discharging a small inductor through the use of four switches. The gate current follows the inductor current when the control switches are activated for turn on or off as shown in the current paths in Figure 4.4. The current waveforms from the simulation are shown in Figure 4.18 for turn-on and Figure 4.19 for turn-off, where I_{DR} is the inductor current generated by the driver and I_G is the current at the gate of the MOSFET. Table 4.12 shows the values of *dv/dt* and energy losses due to the changes in I_G.

The variations in E_{loss}, *dv/dt* and *di/dt* were plotted to show the differences between the three drivers from the LTSpice simulation results. MLVD is the multi-level voltage driver for which V_{DR} is on the x-axis, VMD is the voltage-mode driver for which R_G is on the x-axis, and CMD is the current-mode driver for which I_G is on the x-axis. The best driver exhibits the lowest energy losses while still providing control over the slew rates. The best case has the lowest E_{loss} while still reducing *dv/dt* and *di/dt* to prevent EMI or other consequences of fast-switching.

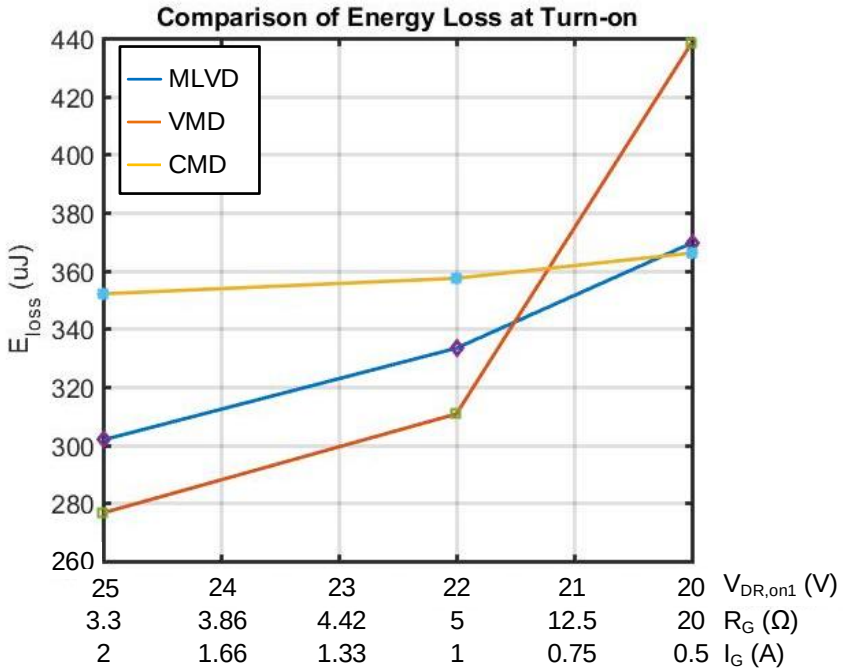


Figure 4.20. Comparison of E_{loss} at turn-on.

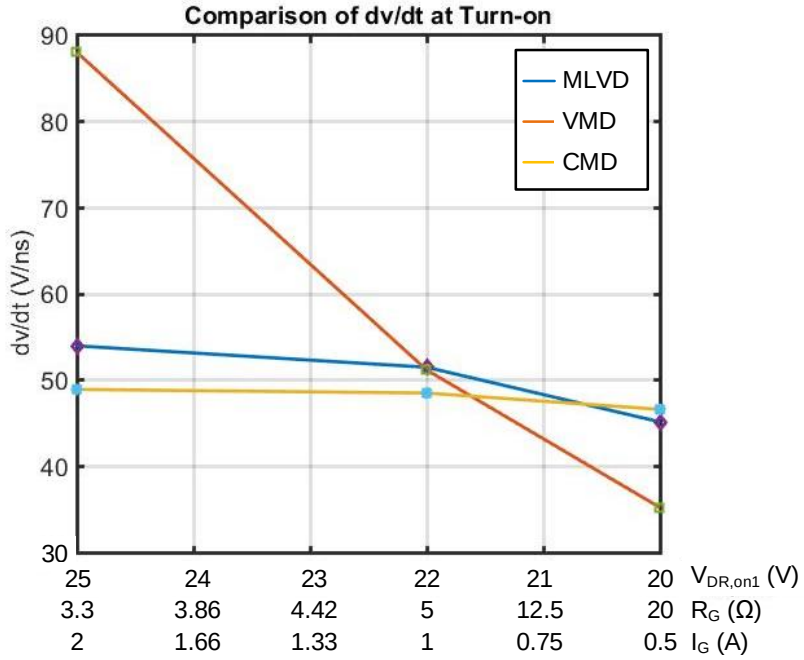


Figure 4.21. Comparison of dv/dt at turn-on.

The turn-on parameters, E_{loss}, *dv/dt*, and *di/dt* are shown in Figure 4.20, Figure 4.21, and

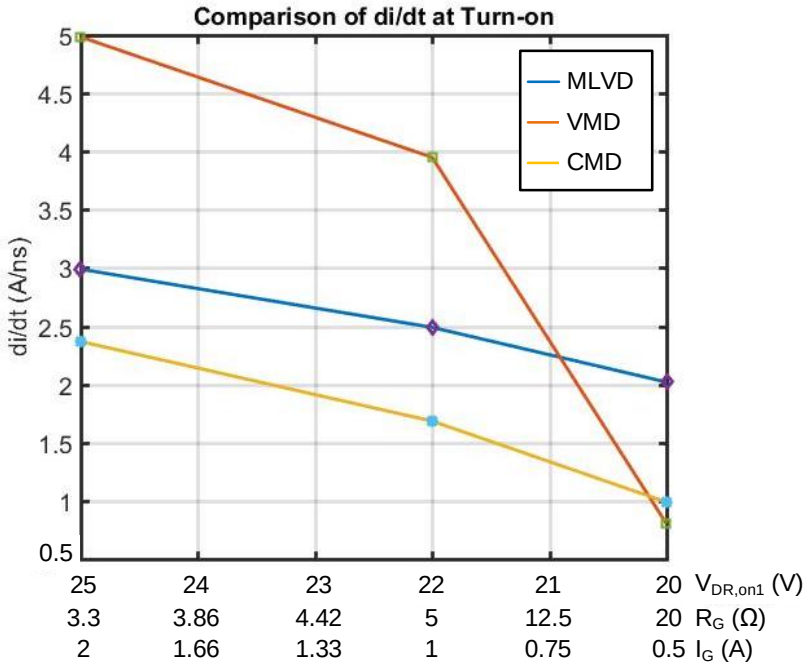


Figure 4.22. Comparison of di/dt at turn-on.

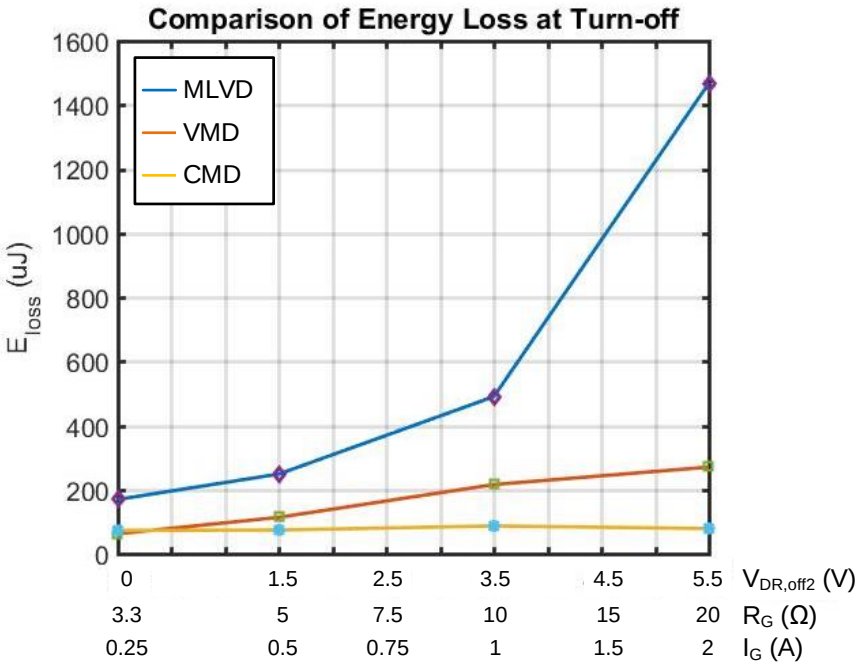


Figure 4.23. Comparison of E_{loss} at turn-off.

Figure 4.22, respectively. The energy losses for the current-mode driver are the most consistent across variations in the gate current. This is most likely due to the small range which was tested,

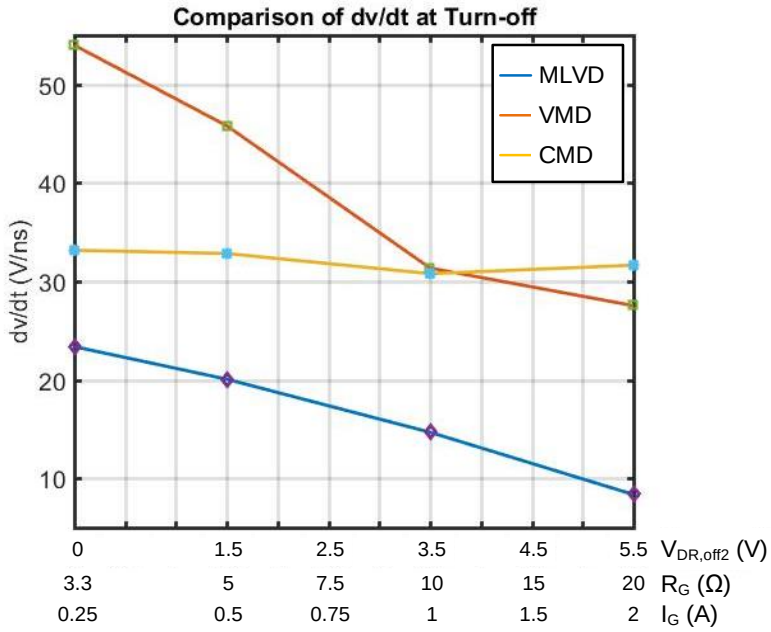


Figure 4.24. Comparison of dv/dt at turn-off.

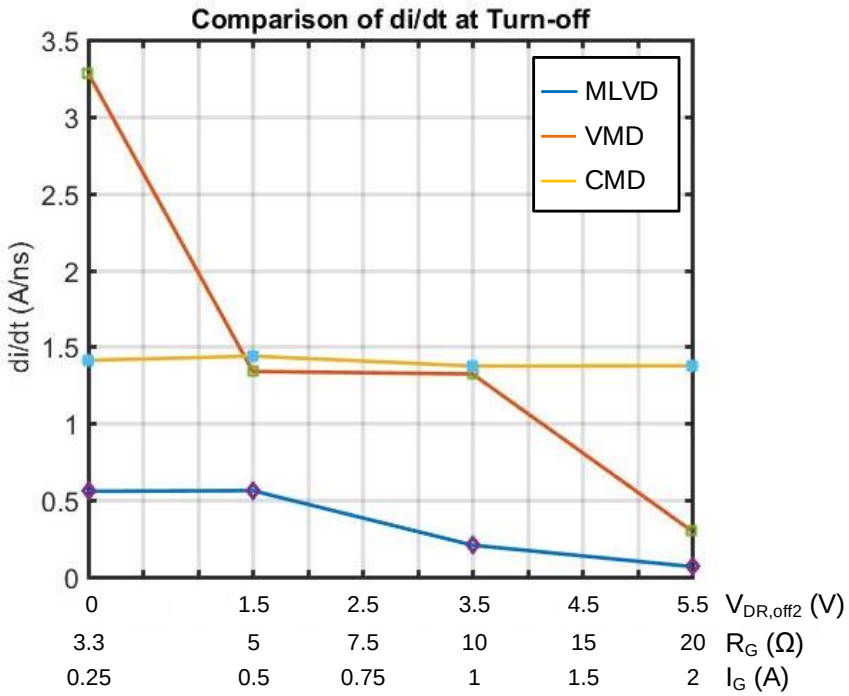


Figure 4.25. Comparison of di/dt at turn-off.

which was limited by the current-mode driver circuit topology. To reduce ringing and to increase ease of acquiring the simulation data, the MLVD had a gate resistance of 10 Ω, which is why the 25 V case on the far left of the x-axis has higher losses than the VMD case at 3.3 Ω. It can be assumed, then, that the MLVD may provide the lowest E_{loss} when R_G is reduced. In Figure 4.21, the *dv/dt* is shown and in Figure 4.22 the *di/dt* is given. For a *dv/dt* of around 50 V/ns, when $V_{DR,on1}$ is 22 V, R_G is 5 Ω and I_G is 1 A, the corresponding *di/dt* levels vary across drivers. The corresponding E_{loss} is smallest for the VMD while the CMD exhibits the highest loss.

The turn-off parameters, E_{loss}, *dv/dt*, and *di/dt* are shown in Figure 4.23, Figure 4.24, and Figure 4.25, respectively. The losses are highest for the MLVD for the entire range shown while the CMD has the lowest, and the VMD also provides relatively low loss. The *dv/dt* shown in Figure 4.24 shows a range of magnitudes for each method. However, if the lowest case is observed, being the point when $V_{DR,off2}$ is 0 V, R_G is 3.3 Ω and I_G is 0.25 A, the energy loss is quite close. When

comparing this same operating point on the *dv/dt* plot, the MLVD is shown to achieve much lower *dv/dt,* alleviating the EMI problems mentioned in previous chapters. Additionally, at this point, the *di/dt* for MLVD is also the lowest while the VMD is the highest.

4.5 Conclusion

In this chapter, the three gate drive methods were compared based on their performance and ability to provide slew-rate control while keeping energy losses minimal. The voltage-mode driver shows typical losses when using various gate resistors, and provides an ability to alter the *dv/dt* with small changes in E_{loss}. However, the gate resistance must be very finely tuned, and there must be some auxiliary circuitry included if the designer wants to change the slew rate online. On the other hand, the current-mode gate driver shows promise, with small variations in energy loss even with changes in slew rate. But this topology is complex, and fine-tuning of the gate current must also take time and effort. Controls of this driver will be complicated especially if the gate current is expected to change actively during various transitions of the MOSFET. Finally, if the application requires lower *dv/dt* slew rates and thus minimal EMI, the multi-level driver may be better suited for such applications because a small variation in the second-level voltage can greatly reduce it and the *di/dt*. This method also requires optimization, but the control is simple, like the conventional driver, and the complexity of the circuit is low. Thus, this driver will be examined in more detail through experimentation.

4.6 References

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[2] F. Wolfgang and Zheng Ziqing, “Turn-on performance comparison of current-source vs. voltage-source gate drivers,” *presented at 2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antionio, TX, March 2018.

[3] S. Madhusoodhanan et al., “Solid-State Transformer and MV Grid Tie Applications Enabled by 15 kV SiC IGBTs and 10 kV SiC MOSFETs Based Multilevel Converters,” *in IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3343-3360, July-Aug. 2015.

CHAPTER 5

TEST SETUP AND EXPERIMENTAL RESULTS

5.1 Introduction

The gate driver is a crucial aspect of any system aiming to utilize SiC devices. The gate driver can mitigate the challenges, as described in Chapter 2, due to the interactions between parasitics in the circuit and the SiC device's fast switching transients. In Chapter 3, different gate driver methodologies were investigated through an analytical approach, and in Chapter 4 their performance was compared through simulation. Each driver provides benefits to the system and each require their own tradeoffs. It was determined that the voltage-mode gate driver is the most common and well-developed method, providing ease of implementation. The current-mode driver was found to provide many performance benefits, but suffers from complex design and implementation. Finally, the multi-level voltage-mode driver was introduced as an alternative to the conventional voltage-mode driver, providing benefits via the amount of control over the slew rate. This method uses a second-level voltage to speed up or slow down the transitions of the device, instead of the conventional use of a gate resistor. In this chapter, the experimental results will be shown to compare the performance of the multi-level voltage-mode driver versus the conventional method. The development of the testbed for characterizing SiC MOSFETs, in itself, is a task that should not be taken carelessly, especially in the characterization of these fast-switching devices. This chapter will discuss the design considerations taken in the development of the double pulse test (DPT) platform. Then the experimental results are presented, with the board layout briefly described in the design of the driver. Finally, the conclusions will be drawn from the results.

5.2 Test Setup

5.2.1 Measurements

The DPT was used to experimentally verify the gate drivers designed for the high-voltage SiC MOSFETs. Due to the very fast rise and fall times of these devices – 10 to 20 ns for the discrete devices – attention must be given to the choice of measurement equipment. The board layout, bandwidth of probes and scopes, and the probe attachments are some of the main considerations. Previous research efforts have detailed some of the common measurement methodologies and describe board layout techniques to minimize parasitics [1].

With rise/fall times within tens of nanoseconds, and potential ringing due to parasitics at or above 200 MHz, the scope and probe must provide sufficient bandwidth. The bandwidth of the probe based on the measured rise/fall times is calculated using the equation

$$BW(GHz) = \frac{0.35}{risetime\ (ns)} \tag{57}$$

Typically, the bandwidth of the probe is suggested to be at least 3 to 5 times faster than the maximum expected measured frequency [2]. For the majority of the tests performed in this research, a high-voltage passive probe, the Tektronix P5120, with 200 MHz bandwidth was used to measure the V_{DS} of the lower MOSFET, the device under test (DUT) [3]. The drain current I_D was measured using two different methods: the Pearson current monitor and the coaxial shunt, as shown in Figure 5.1. The benefit of the Pearson current monitor is that it does not need to be inserted into the circuit. However, its bandwidth is limited to 70 MHz, and has a useable rise time of 5 ns [4]. This bandwidth is sufficient for these devices, but a higher bandwidth would be beneficial. On the other hand, the current viewing resistor (CVR) with a coaxial connector, from

Figure 5.1. Pearson current monitor and coaxial shunt current viewing resistor.

T&M research, can measure rise times as low as 0.3 ns, corresponding to a bandwidth of about 1 GHz [5]. The main drawback of the CVR is the added inductance by the insertion of the resistor into the current path. However, some additional inductance is introduced with the Pearson, as well, due to the insertion of a jumper wire to put the current transformer around. Finally, V_{GS} was measured using a 1X BNC cable connected to the board. All of these measurements share the same reference, so an isolated oscilloscope and differential probes were not necessary. To increase the bandwidth of such measurements while reducing the group loop inductance due to the probe connections, on-board measurements may be used through the use of a voltage-divider and high bandwidth operational amplifiers, such as the circuits shown in [10]. The control signals were generated using a function generator, the AFG3022B, to drive the gate driver, which can be controlled using a National Instruments™ LabView interface.

5.2.2 Board Layout

The board layout was optimized to provide ease for repeatable use and interchanging of gate drivers. Two versions of the DPT boards are shown in Figure 5.2, one being designed by the author and the other made by CREE™. The gate driver connectors were placed as close as possible

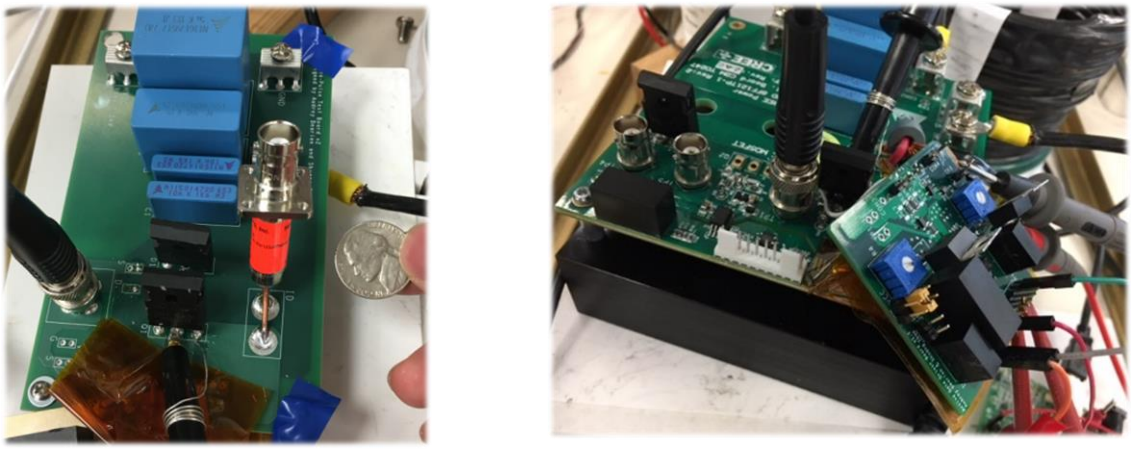

Figure 5.2. DPT experiment boards.

to the DUT in order to reduce the gate loop inductance. Additionally, a Kelvin connection on the board was designed to provide a short path from the MOSFET's source back to the driver. The gate and source planes were placed on separate layers to create a small gate loop vertically through the board. The upper Schottky diode and lower DUT were placed as close together as possible as well as the dc-link capacitors to minimize the power loop inductance, and consequently the ringing and voltage overshoot due to SCCLI, the power loop inductance.

The board was optimized to reduce the power-loop inductance by placing the DC power plane, HVDC, and the ground plane, GND, vertically on top of each other. Parasitic extraction tools can be useful in the optimization of the board layout. In this case, ANSYS® Q3D extractor was used to find and minimize the power loop and gate loop inductances. In the final board design, as shown in the rendering of Figure 5.3, the power and gate loop parasitic inductances were about 7 nH and 2.5 nH, respectively. The extraction process is documented in Appendix B. Additionally, higher creepage can be achieved through the use of board cutouts placed high-potential regions, such as between decoupling capacitors and the legs of the power MOSFET and Schottky diode.

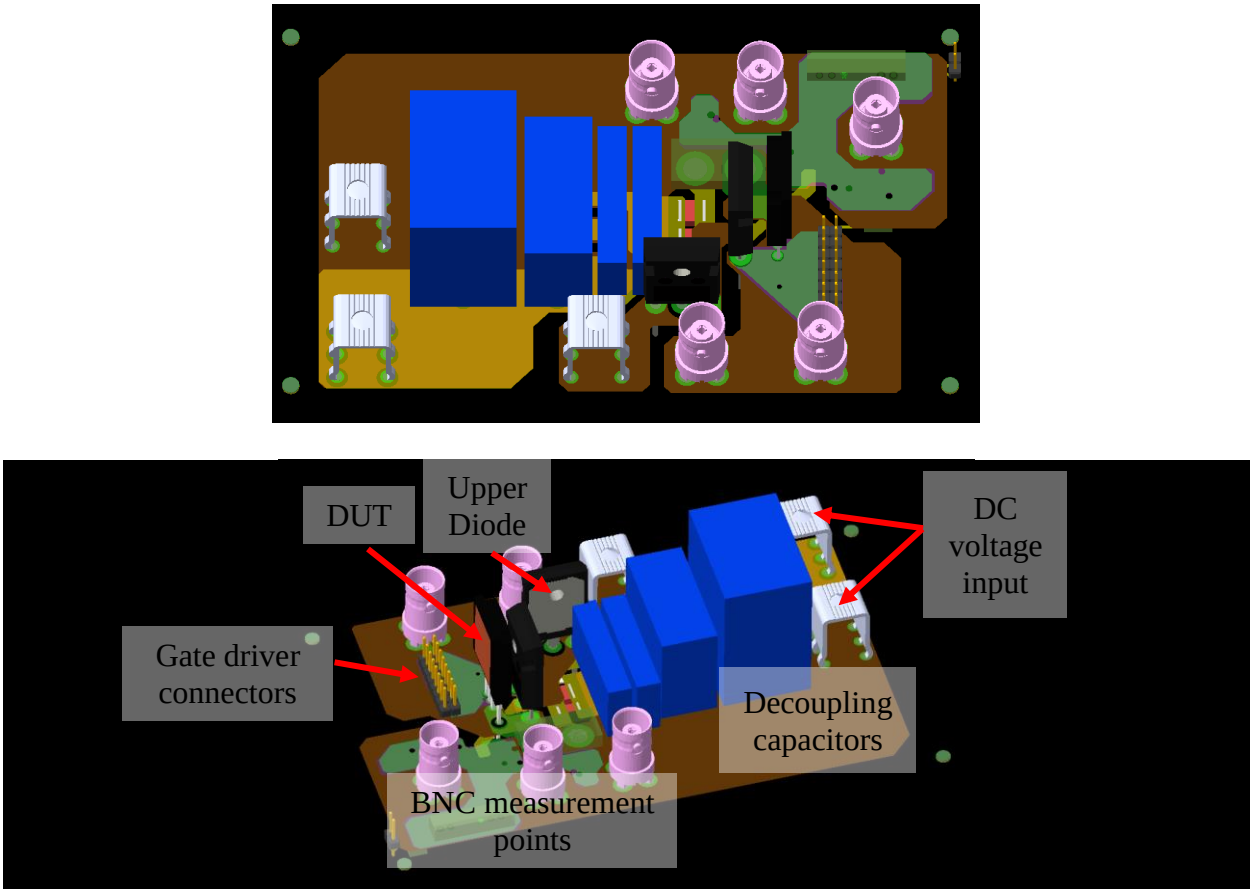

Figure 5.3. 3D Rendering of optimized DPT board.

5.2 Experimental Results

5.2.1 Test parameters

The DPT setup, Figure 5.4, was designed to test the SiC MOSFETs under different conditions and with various gate drivers. Specifically, the multi-level turn-off driver was found to be very valuable due to its ability to greatly reduce *dv/dt*. However, as shown in the theoretical analysis of Chapters 3 and 4, the energy losses increase when the switching speed is slowed down. The tradeoffs between slew rate reduction and increased energy losses were analyzed theoretically and through simulations. In this chapter, the performance based on experimental tests are found for the turn-off transition. The turn-off transition is important due to the high *dv/dt* and *di/dt* transitions that occur which result in EMI generation and voltage overshoot [11].

Table 5.1. Test parameters.

Lower DUT	C2M0045170D, 1.7 kV SiC MOSFET
Upper device	C4D40120D, 1.2 kV SiC Schottky Diode
Load inductor	Air core, 230 µH
DC link capacitors	2.35 mF
DC voltage, V_{DC}	100 – 600 V
Load current, I_L	5 – 20 A
$V_{DR,off2}$ range	3.5 – 5.5 V
Duration of $V_{DR,off2}$	*Dependent on $V_{DR,off2}$
R_G range	3.3 – 20 Ω

The test parameters are shown in Table 5.1. Both 1.2 kV and 1.7 kV SiC MOSFETs are used in experiments while the upper device is a SiC Schottky diode. Both the upper and lower devices are discrete, and are contained in TO-247 packages. As shown in Figure 5.4 the main

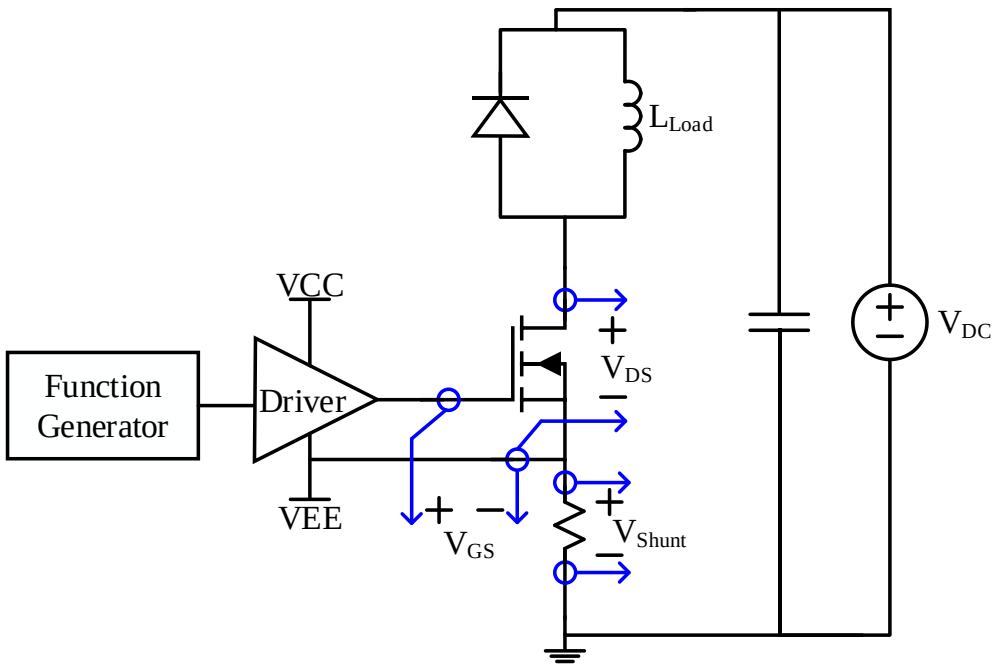

Figure 5.4. Double Pulse Test (DPT) circuit and measurement points.

measurement points of interest are V_{DS}, V_{GS} and I_D so that the transients and energy losses may be acquired in the post-processing stage.

5.2.2 Gate driver design

As mentioned before, there are some basic parameters of the gate driver that need to be considered to properly drive the SiC MOSFET. To begin with, the strength of the driver needs to be sufficient, meaning the gate charge of the device is considered along with the desired rise and fall times. The equation for gate current was given in Chapter 3 based on those parameters as shown:

$$i_{G,peak} = \frac{Q_{G,total}}{t_{rise/fall}} \tag{58}$$

Where Q_G is the total gate charge of the device and $t_{rise/fall}$ is the desired rise and fall time of V_{GS}. Q_G is found in the C2M0045170D's datasheet, which is 188 nC. For example, if the desired rise/fall time is 20 ns, then the gate current needs to be 9.4 A. The IXYS IXDN609SI was chosen as the main voltage buffer, providing a maximum drive current of 9 A [6]. This provides sufficient drive strength for a minimum datasheet recommended gate resistance of 2.5 Ω due to the following relationship:

$$i_{out} = \frac{\Delta V_{DRV}}{R_{G,min}} \tag{59}$$

Where the recommended current should be greater than 70% of i_{out} [7]. In this case, with a voltage swing of 25 V, the gate driver should provide >7 A. Thus, the IXYS driver is sufficient and also provides a low output impedance of 0.8 Ω and fast rise/fall times.

The Murata MGJ2D122005SC was chosen to supply the maximum drive voltage, V_{CC}, at 20 V and the minimum pull down voltage, V_{EE}, of -5 V. This is 2 W supply has isolation capability of 5.2 kV [8]. Additionally, Texas Instruments digital isolators were used to isolate the control signal, and has high common-mode transient immunity (CMTI) of 50 kV/μs [9]. The multi-level turn-off circuitry was achieved through the utilization of two IXYS drivers, where the lower driver provides a variable pull-town voltage based on the level set by the designer. This voltage level was set with a LDO (low dropout) regulator whose output voltage was variable based on a potentiometer. This driver was made such that the second-level turn-off does not have to be used if not desired. Thus, the tests without the multi-level turn-off were performed using the same driver, and thus have the same loop impedance.

The driver was designed using the Cadence® Allegro and PCB Editor software. The board is four layers, in which the power planes are kept on the internal layers, and the signals are kept on the top layer. The isolated power supplies and primary side of the digital isolators are separated physically from the secondary side with a cutout inserted in the isolation barrier to increase

Figure 5.5. ML gate driver board.

creepage. The signal routing is minimized by using the top/bottom layers and surface mount components. The final PCB design multi-level turn-off driver is shown in Figure 5.5.

5.3 Experimental Results

The multi-level turn-off driver is of interest due to its ability to mitigate the many negative effects of fast switching at turn-off, namely false-turn-on, voltage overshoot, and common-mode noise that are resultants of high *dv/dt*. Thus, the evaluation of this driver is compared to the conventional method experimentally. The conventional method utilizes a gate resistor to reduce the *dv/dt* and *di/dt* slew rates. The downfall of slowing the switching, however, is increased energy losses. This means that $V_{DR,off2}$ must be designed carefully based on the load conditions and the voltage level to produce the lowest energy losses. The same methodology goes for the use of R_G. The SiC MOSFET was tested under the conditions outlined in Table 5.1.

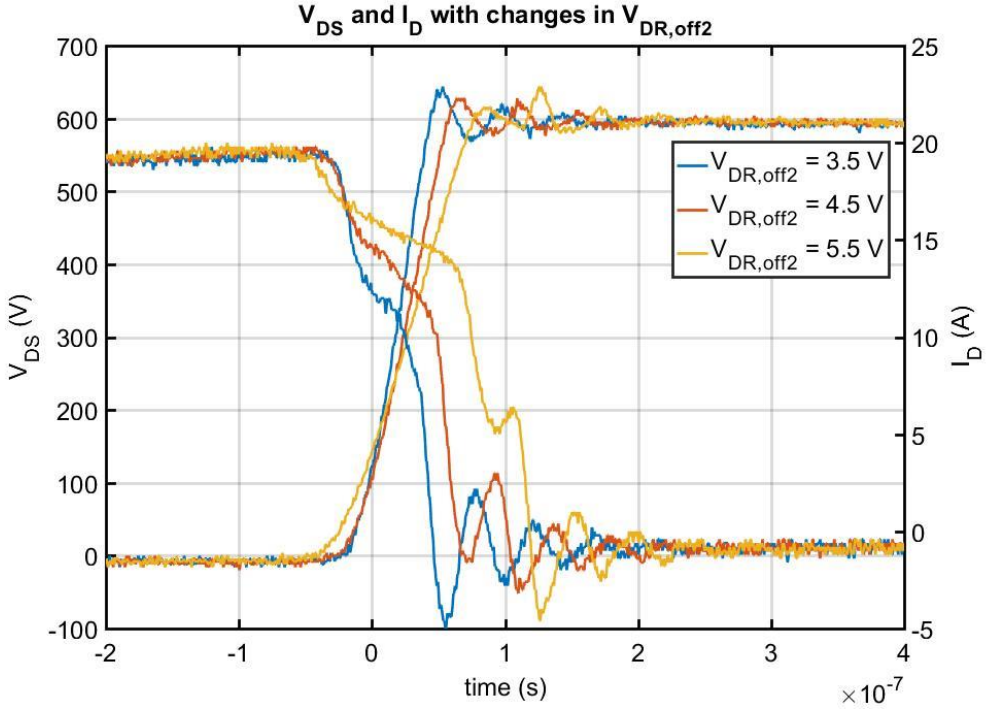

Figure 5.6. Experimental results where V_{DC}=600 V, I_L=20A.

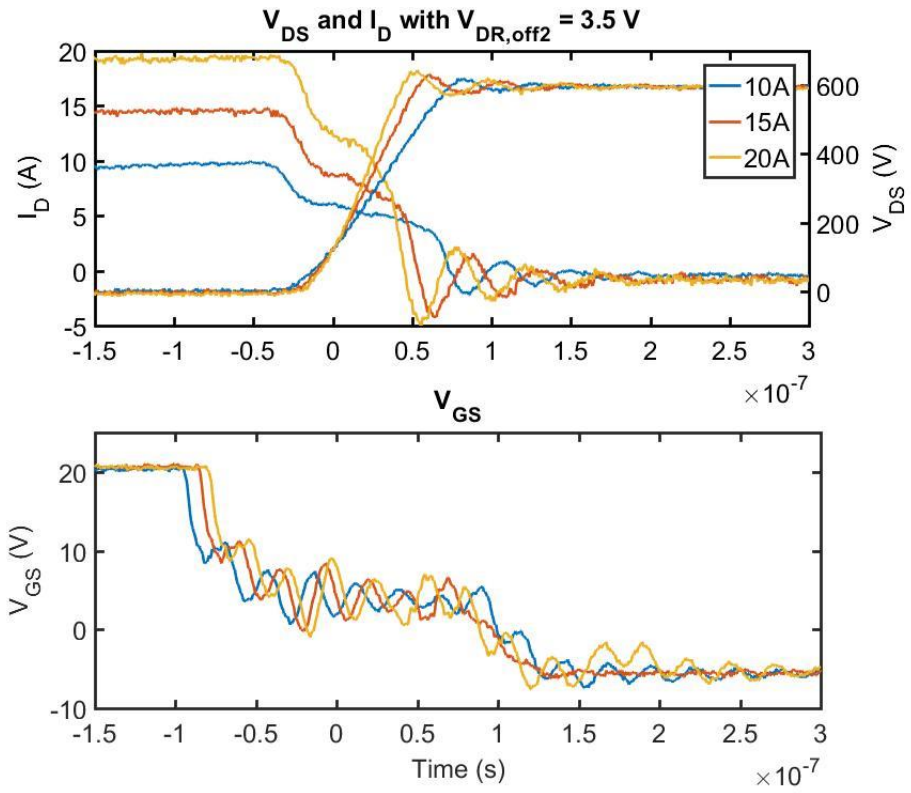

Figure 5.7. V_{DS}, I_D and V_{GS} vs. changes in I_L when $V_{DR,off2}$=3.5 V.

The experimental waveforms shown in Figure 5.6 show the change in slew rates of V_{DS} and I_D, due to $V_{DR,off2}$. The *dv/dt* slew rate shows obvious decrease, and has a constant slope throughout the transition. However, the *di/dt* does not behave in the same way. The current becomes divided into three main *di/dt* slew rates, the majority of which are still very steep. Each of the slew rates directly correspond to the voltage changes in V_{GS}. As $V_{DR,off2}$ increases, the current is held on for a longer period of time, resulting in increased power losses. After the current has been held at a certain value, it falls to zero at a fast rate similar to when it is driven by the conventional driver. The last *di/dt* transition seems consistent amongst all levels of $V_{DR,off2}$, and the resulting voltage overshoot on V_{DS} can be observed in the figure. As shown in Figure 5.8 and Figure 5.7, the gate voltage V_{GS} is shown along with V_{DS} and I_D. Although there are periods of time when *di/dt* is

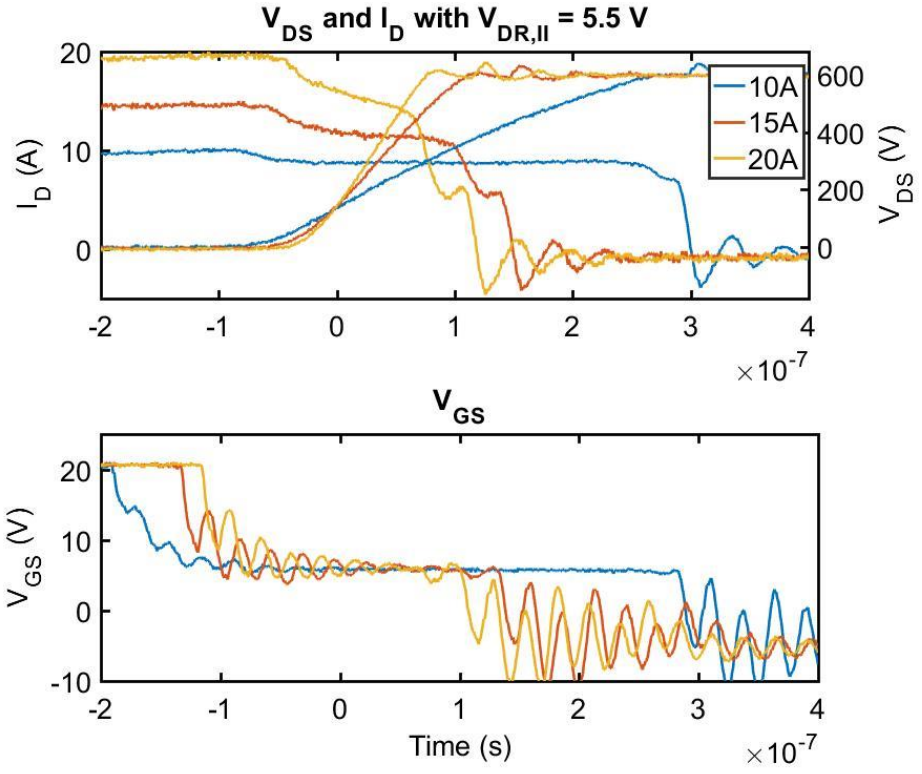

Figure 5.8. V_{DS}, I_D and V_{GS} vs. changes in I_D when $V_{DR,off2}$=5.5 V.

reduced, the maximum *di/dt* is consistent across all values of $V_{DR,off2}$. This is a downfall of the existing method of producing the $V_{DR,off2}$ voltage level due to the sharp transitions from $V_{DR,H}$ and to $V_{DR,L}$.

The level of $V_{DR,off2}$ mainly influences the *dv/dt* level, and proportionally reduces it, however the drain current has alternative effects that increase the losses. For example, if $V_{DR,off2}$ is 5.5 V when I_D is 10 A, the current remains high until V_{GS} is pulled down to -5 V, causing very high E_{loss}. Thus, I_L is a main variable in choosing the level of $V_{DR,off2}$. At higher levels of current, i.e. 20 A, it may be allowable to set $V_{DR,off2}$ at 5.5 V, while the lower current can utilize the 3.5 V. This directly corresponds to the relationship between V_{miller} and I_L as discussed in the theoretical

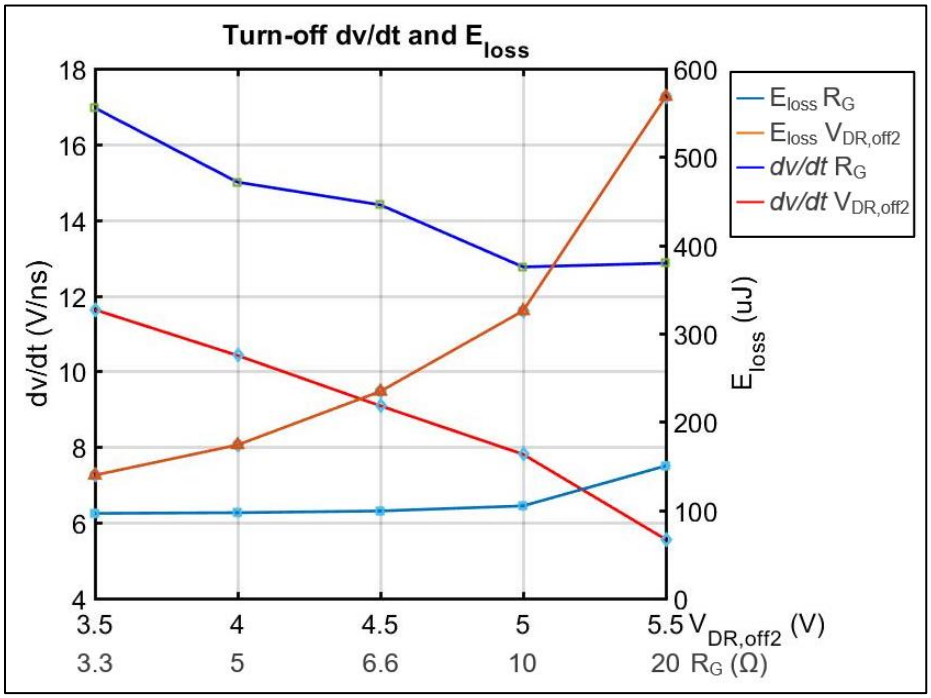

Figure 5.9. dv/dt and E_{loss} vs. $V_{DR,off2}$ when V_{DC}=600 V, I_L=20 A.

analysis. When I_L increases, so does V_{miller}, and thus if it is desired to reduce *dv/dt* which happens during this plateau region, then $V_{DR,off2}$ should be lower-than, but near that value.

The *dv/dt*, on the other hand, is controlled well by $V_{DR,off2}$ and has a single slope. The effect that the multi-level driver has on the *dv/dt* is much higher than that of the R_G method. Figure 5.9 shows the *dv/dt* and energy loss versus both $V_{DR,off2}$ and R_G, when V_{DC} is 600 V and I_L is 20 A. The *dv/dt* in the case of the multi-level driver can be reduced to less than 7 V/ns. On the other hand, a gate resistor of 20 Ω results in *dv/dt* still well above 10 V/ns. However, the energy loss is much higher for $V_{DR,off2}$ at 5.5 V versus when R_G is 20 Ω. In another case, when $V_{DR,off2}$ is 3.5 V, the *dv/dt* level is brought down to around 12 V/ns and has similar E_{loss} to the 20 Ω case, while *dv/dt* is only reduced to just below 14 V/ns. More improvements can be made to the multi-level driver with regards to the voltage level and other circuit components to improve these effects.

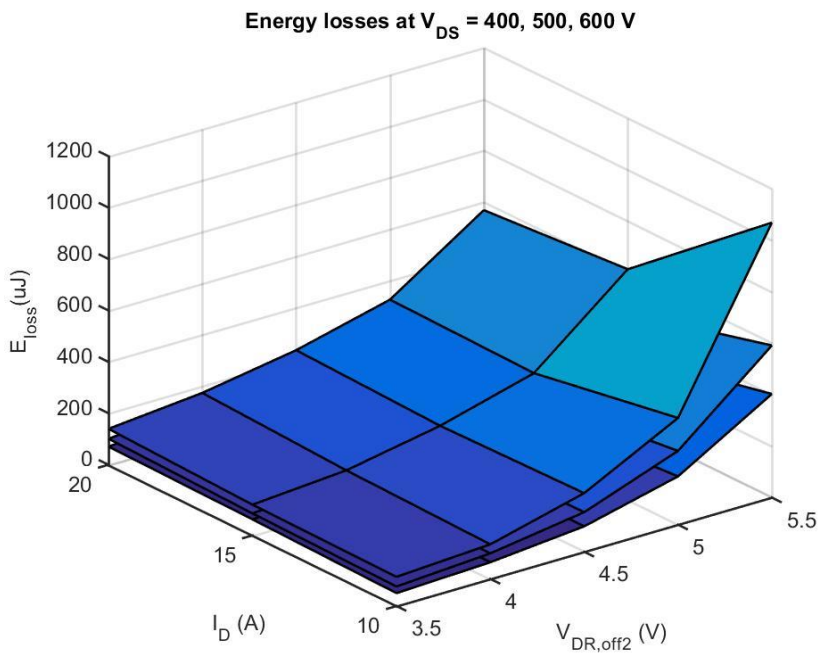

Figure 5.11. E_{loss} versus I_D and $V_{DR,off2}$.

The energy losses change with both I_L and $V_{DR,off2}$, as mentioned before. Figure 5.11 and Figure 5.10 show the variations in E_{loss} with both I_L and $V_{DR,off2}$ or R_G. Additionally, as the surface plots rise in the z-direction the voltage level increases from 400 V to 600 V. The energy losses in

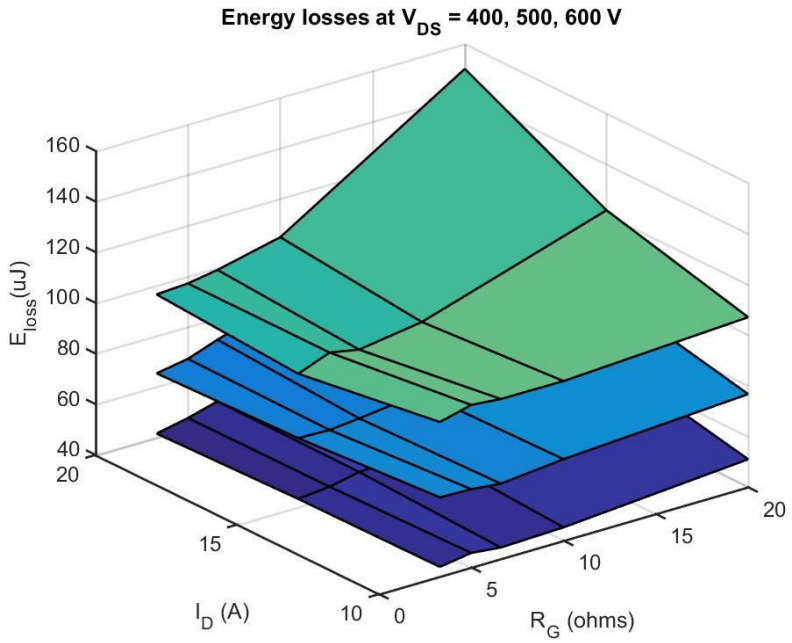

Figure 5.10. E_{loss} versus I_D and R_G.

all cases are significantly smaller for the R_G method than for the multi-level driver. This is mainly due to the effects on the drain current as shown in the waveforms above.

Although the energy losses are higher for the multi-level driver than for the conventional method, it is much more effective in reducing *dv/dt*. A notable discovery from the comparison is the duration of the turn-off period and the turn-off delay. The total turn-off duration comparing the two drivers is shown in Figure 5.12. Because the resistance is smaller when using $V_{DR,off2}$, there is a much faster transition between $V_{DR,H}$ to $V_{DR,off2}$ and from $V_{DR,off2}$ to $V_{DR,L}$. When the gate resistor is increased, it slows down every portion of the V_{GS} waveform. -5 V. This is a benefit of the multi-level driver. For applications requiring low *dv/dt* it may still be more beneficial for faster frequencies to use multi-level turn-off than the conventional method.

Although the energy losses for the conventional voltage-mode driver are much lower than that of the multi-level driver, there are some benefits with regards to control over *dv/dt* and the

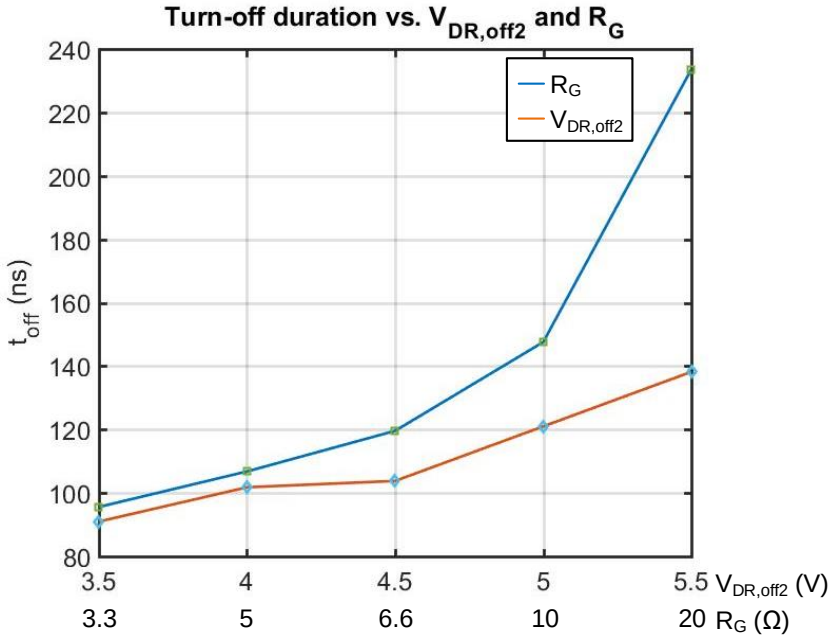

Figure 5.12. Turn-off duration comparison.

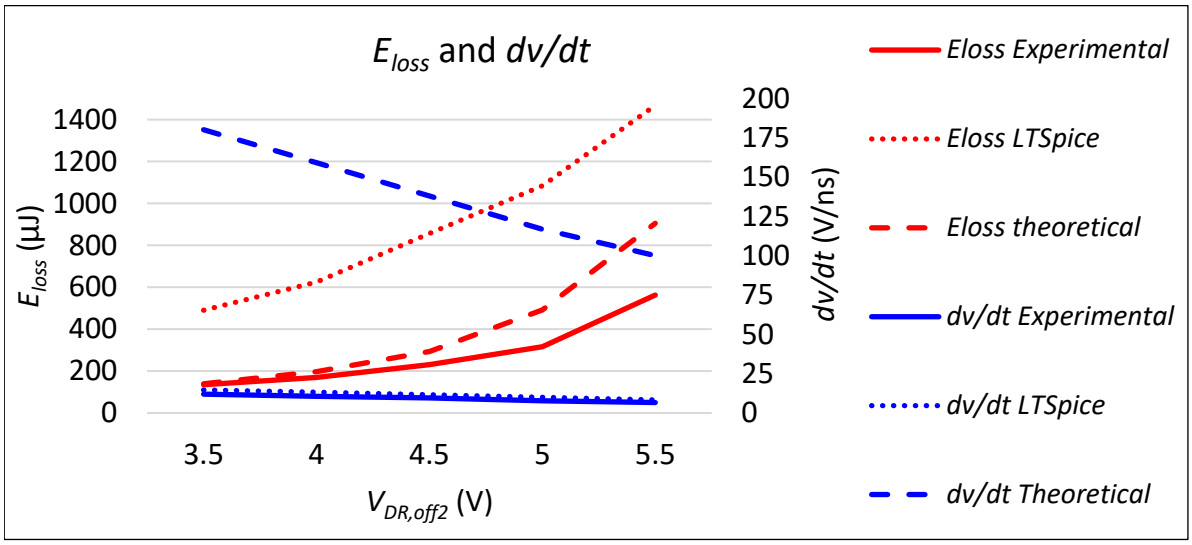

Figure 5.13. E_{loss} and dv/dt comparison of results.

shorter turn-off duration. With proper tuning, the multi-level driver can be optimized to reduce the *dv/dt* with minimal loss. This is especially important for applications, such as motor drives, which require lower levels of *dv/dt* and seek to utilize SiC MOSFET's other benefits. Additionally, if the driver is able to reduce the *dv/dt* through a driving technique such as this, then *dv/dt* filtering is reduced or removed, and thus the power density and weight of the system can be decreased.

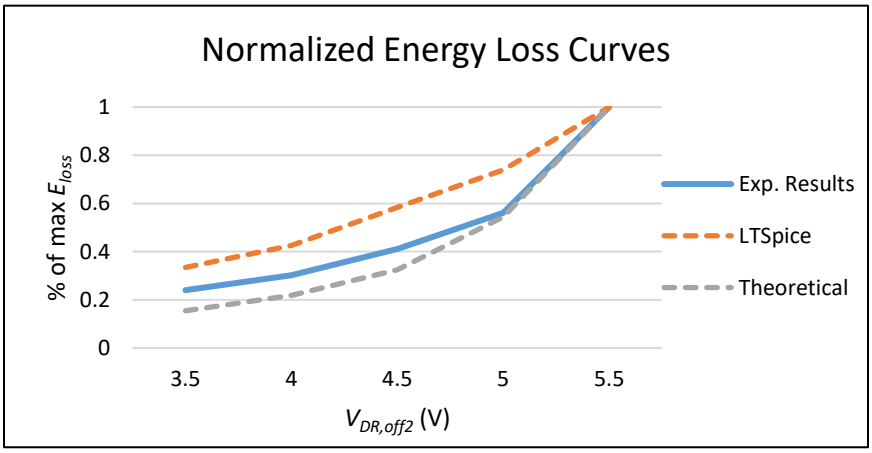

Figure 5.14. Experimental, LTpice and theoretical results comparison of E_{loss}.

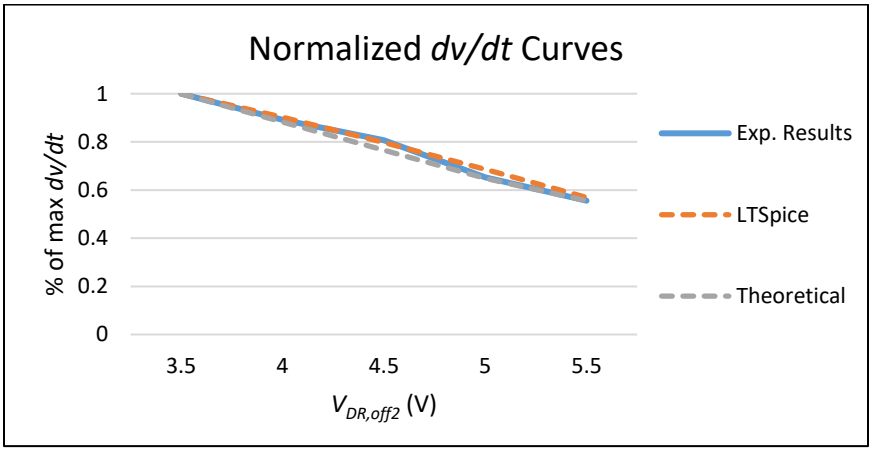

Figure 5.16. Experimental, LTSpice and theoretical results comparison of dv/dt.

Finally, the experimental data was compared with the theoretical and simulated results. The models must be tweaked to generate values which are closer to the actual experimental results. E_{loss} and *dv/dt* are shown in Figure 5.13 for each of the datasets. The values from the experimental and simulated results align closely in determining *dv/dt*. However, for energy loss comparison, the results from the theoretical analysis is closer to the experimental results. The purpose of this thesis was not to explain or perfect a model, but rather to find a way to compare them. Thus, through the normalization of the curves, the trends can be observed to be almost the same across all methods of comparison. The trends for E_{loss}, *dv/dt*, and *di/dt* using multi-level turn-off are shown in Figure

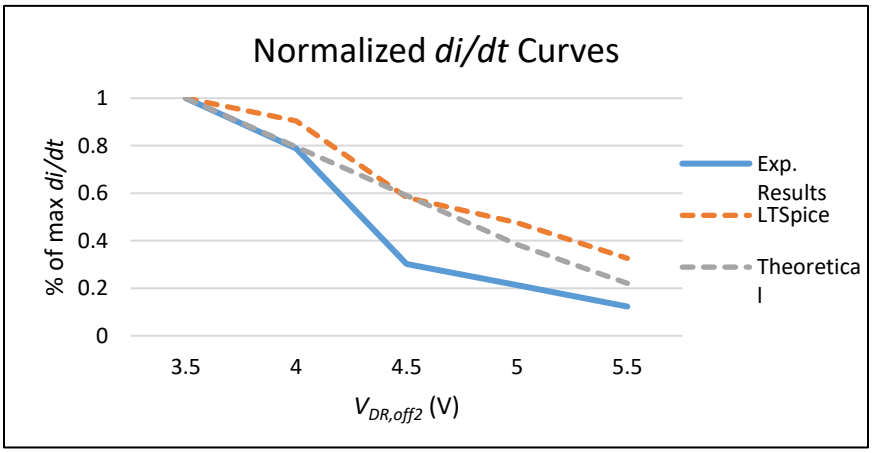

Figure 5.15. Experimental, LTSpice and theoretical results comparison of di/dt.

5.14, Figure 5.16, and Figure 5.15. This is useful to determine the validity of such analyses for predicting the actual behavior. The trend as a result of changing $V_{DR,off2}$ is reflected in the theoretical, simulated and experimental results. This agreement between methods of interpreting gate driver strategies can save design time to determine the best driver strategy. The trend lines can be easily fitted with a linear or polynomial function, and through the use of baseline experimental results, the performance may be predicted for the multi-level driver.

5.4 Conclusion

The design and implementation of SiC MOSFETs is not simple, and even the test setup itself requires careful design. The parasitics extraction was utilized to minimize inductance on the circuit board and the layout was optimized for this purpose. The gate driver designed provided a multi-level turn-off function which was compared to the conventional method. It was found through the experimental verification that the multi-level turn-off driver offers some advantages over the conventional voltage-mode driver. The multi-level driver can effectively reduce the *dv/dt* and has the ability to provide higher slew rate control and similar energy losses to the conventional driver. Additionally, the total duration of the turn-off was found to be smaller than the conventional method. The multi-level driver can be greatly improved, however, but has potential in applications where *dv/dt* is required to be low and the switching frequency is not extremely high. These systems can still benefit from the low conduction losses of SiC MOSFETs and their high breakdown voltage and high temperature operation. The gate driver is a highly important aspect of the system-level design, and can enable power electronics designs to achieve high efficiency and meet reliability requirements.

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CHAPTER 6

CONCLUSIONS AND RECOMMENDATION FOR FUTURE WORK

6.1 Summary and Conclusions

The improvements in SiC power device technology have been immense over the past decade and their performance benefits have been proven in a variety of applications [1, 2, 3]. However, the gate driver technology which enables these devices is still not fully developed. The driver should be able to provide the necessary functions to enable the performance of the SiC MOSFET while providing protection functions, as well. For many applications, the reliability of the device is of utmost importance, and some mitigation of the effects of *di/dt* with parasitic inductance can be achieved through the gate driver. Additionally, the *dv/dt* also introduces EMI and should be controllable by the designer based on their application needs. In Chapter 1, the background was given and the motivation for the work was described with a brief overview of the benefits of SiC devices, such as their operation at high temperatures and their high voltage-blocking capability.

In Chapter 2, the main challenges associated with using SiC MOSFETs were pointed out, and the common solutions were described. Above all the board layout should be optimized for both the gate driver and the converter. Parasitic inductances should be reduced, specifically the common-source inductance which serves as a main source of ringing and false-turn-on issues [4]. The minimization of parasitics in the board layout is achieved through small gate and power loops and by stacking the gate and source return path on layers atop one another to cancel out inductance. The use of a negative voltage rail in also necessary to cancel out the voltage spikes on the gate, thus reducing the chance of Miller turn-on [5]. An Active Miller clamp, or a package with a Kelvin

source connection, is strongly advised in whatever form is available to achieve this goal [6, 7]. Finally, the design of the isolation barrier, specifically with regards to the isolation transformer, is necessary due to its high isolation requirement and need for low coupling capacitance to prevent *dv/dt* from creating unwanted noise [8, 9].

In Chapter 3, three gate driver methodologies were described in detail through the analysis of the waveforms and the corresponding equations describing energy losses, *dv/dt*, and *di/dt* during the turn-on and turn-off transitions. The benefits and drawbacks of each method are pointed out. In Chapter 4, these driver methodologies were compared based on the theoretical equations and the simulated results [10]. The voltage-mode driver is the most conventional method and is commonly used, thus it is easy to implement. However, the control technique, namely the gate resistor, may not be the most effective method of control and cannot be actively changed without auxiliary circuitry. The current-mode driver was also investigated and provides benefits of constant current to enable consistent *dv/dt* and *di/dt* slew rates across a range of load current. It also provides low switching losses as compared to the other methods. However, the circuitry and control is complex and should be further investigated, and it is not clear if this method is suitable for high-voltage SiC MOSFETs. Finally, the multi-level voltage-mode driver was investigated, and provides control at both turn-on and turn-off using an intermediate voltage level. In this study, the turn-on voltage driver was able to change the slew rate using a range from 20 to 25 V in order to minimize conduction losses. Furthermore, the turn-off multi-level driver was also investigated and tested in the range of -5 to 5.5 V. It was shown to have similar switching losses to the voltage-mode driver, but provided better slew-rate reduction. This method can also be integrated as an active gate driver by using a control loop to change the voltage-level based on the load conditions, making this a good option for high-voltage SiC MOSFETs.

Chapter 5 described the experimental setup and some design considerations for the double pulse test and gate driver board. The results were given for the multi-level turn-off driver and was compared to the conventional voltage-mode driver. These experiments provided the comparison between using R_G and V_{DR} to change the slew rate. It was found that the multi-level turn-off driver produced much higher losses, but significantly reduced the *dv/dt*. Designers may consider this tradeoff depending on the *dv/dt* and *di/dt* levels required to minimize EMI per the system requirements. It was also found through the experimental results that the multi-level driver actually had lower turn-off time than the conventional method. It is important to note that the variations in E_{loss}, *dv/dt* and *di/dt* due to the changes in V_{DC} and I_L is similar for both the multi-level driver and the conventional driver. Thus, in the design of the gate driver circuit, the load conditions should always be a consideration. This is especially true for the multi-level driver, which may unnecessarily increase losses, or fail to turn off the device, if the V_{DR} is not chosen properly. With a developed current-mode driver, given the benefits found in the theoretical and simulated comparison, a hybrid gate driver could be beneficial in driving the SiC MOSFET. While the energy losses utilizing a multi-level driver at turn-off are tolerated due to the *dv/dt* and *di/dt* reduction resulting in lower EMI and voltage overshoot, the losses can be made up by reducing the turn-on losses utilizing a current-mode driver. Thus, during the total switching cycle, the overall losses are still low, and total switching losses are minimized. A multi-level driver at turn-on may also be used, but the small range of voltages allowable in order to minimize stress on the device may only reduce the losses to a certain extent. However, there is much work necessary to develop the current-mode driver, and thus a full multi-level voltage-mode driver may provide similar results to the aforementioned hybrid driver.

6.2 Recommendations

Due to the increase in energy losses and the inherent slowing down of the device transitions, the multi-level driver methodology should be considered for next-generation power electronics utilizing high-voltage devices like the 10 kV SiC MOSFET, which are expected to switch at frequencies in the range of 3 to 10 kHz and above [11]. In the applications in which these devices operate, it will not be necessary to switch at very high frequencies. However, the slew rate will be inherently larger due to the high voltage levels. Thus, the multi-level driver control may provide benefits to the system without hindering performance due to switching losses. One of the main advantages of this method is that it has the potential to be controlled digitally through feedback based on V_{DC} and I_D, temperature, or the slew rate. A feedback loop would provide the most efficient control of the SiC device under variations in operating conditions, and may protect and extended the device's lifetime by preventing unnecessary failures due to EMI and stress on the device. In the event of a short circuit, the multi-level driver also provides the means for soft turn-off to mitigate very high *di/dt* that results in large overshoot and potential device failure. Future considerations for the multi-level turn-off driver also include the control of transitions between the high-level voltage, intermediate voltage, and final turn-off voltage. When these V_{GS} transitions are fast, it was shown that the *di/dt* slew rates are also high, which cause voltage overshoot and additional ringing.

The multi-level driver is also of interest in systems which require high power density. Due to the minimization of the system, access to the gate loop, i.e. the gate resistor, may not be possible. In new packaging techniques, the gate driver can be positioned very close to the power device, as well as other components, such as through flip-chip packaging [12]. With electronics being in such close proximity to one another, the challenges of EMI and the *dv/dt* are heightened. To change the

slew rate in a conventional voltage-mode driver, it may be difficult for the designer to make changes to the gate resistor, being the main method of control. However, the mutli-level driver features may be integrated into an IC chip to provide digital control over the slew rate without having to make physical changes to the circuitry through the changing drive voltage. Thus, EMI mitigation is possible through the digital control, versus any physical circuit adjustments.

Finally, the benefits of the current-source driver are still under investigation in the research [13, 14]. Some downfalls of some of the current-mode topologies are the lack of a negative voltage rail to reduce the probability of a false turn-on and the complexity of the control. However, if this method, such as the one simulated in this work, is made to include a negative voltage rail as well as a positive on-voltage to reduce conduction losses, then it may be more beneficial than the voltage-mode driver. The benefits include consistent *dv/dt* and *di/dt* over variations in load current and the minimal effect of gate-loop resistance on the drive strength. However, in order to keep the current consistent across the entire switching transition, additional voltage provided at the supply of the driver must be considered to increase power after V_{GS} reaches 20 V. Thus, it is suggested that this method be investigated more thoroughly, and experimentally verified.

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APPENDIX A

MATLAB™ Code for Gate Driver Analytical Comparison

This appendix presents the MATLAB code utilized in the theoretical comparison of the voltage-mode, current-mode and multi-level voltage-mode gate drivers. This allows the user to input the DPT circuit, SiC MOSFET device, and SiC Schottky diode parameters to extract the energy losses, *dv/dt* and *di/dt* under various load conditions.

```
% Comparison of drivers
% Created by Audrey Dearien, Spring 2018
% Power MSCAD
%% Parameters of SiC MOSFET
% For equations, refer to "Analytical Loss Model for Power Converters with
SiC MOSFET and SiC Schottky Diode Pair" - Peng, Eskandari, Santi, ECCE 2015
clear all;
IL = 20; % Load current operating condition
VDC = 600; % DC bus voltage operating condition
Vth = 2.6; % MOSFET threshold voltage
gfs = 21.7; % MOSFET transconductance
rdson = 45e-3; % MOSFET on-resistance
Von = IL*rdson; % MOSFET on-state voltage drop
Vmiller = Vth+IL/gfs; % MOSFET miller plateau (may be required to change this
value manually for best results)
VDRH = 20; % Maximum drive voltage
VDRL = -5; % Minimum drive voltage
Ls = 5e-9; % Source inductance (in gate loop)
Ciss = 3672e-12; % MOSFET input capacitance
Vd = 1.5; % Schottky diode forward voltage drop
SCCLI = 20e-9; % Power loop inductance
Cd = 50e-12; % Schottky diode parasitic capacitance
Cl = 0; % Load inductor parasitic capacitance
Cgdmin = 8e-12; % MOSFET minimum value of Cgd (found in Cgd curve of
datasheet)
Cgdmax = 50e-12; % MOSFET maximum value of Cgd (found in Cgd curve of
datasheet)
Cdsmin = (171e-12)-Cgdmin; % MOSFET Cds minimum value (calculated)
Cdsmax = (171e-12)-Cgdmax; % MOSFET Cds maximum value (calculated)
%% TURN-ON Theoretical equations for all drivers
%% Voltage-mode Driver Turn-on Equations
% Only variable is Rg
Rg_x = linspace(2.5,20,20);
for n = 1:size(Rg_x,2)
    Rg = Rg_x(n);
    % Current rising period
    t_cur_rise = (Ciss*(Vmiller-Vth));
    t_cur_rise2 = (Ciss*Rg*IL + Ls*gfs*IL)/((VDRH-0.5*Vth-0.5*Vmiller)*gfs);
    Ig_cur_rise = (VDRH-0.5*(Vmiller+Vth)-Ls*(IL/t_cur_rise2))/Rg;
    didt_cur_rise = IL/t_cur_rise2;
    V_drop = VDC + Vd - SCCLI*didt_cur_rise;
    E_loss_cur_rise = 0.5*(t_cur_rise2*IL*(VDC+Vd))-(1/3)*(IL^2*SCCLI);
```

```
    % Voltage falling period I
    Vr = VDC+Vd-SCCLI*didt_cur_rise;
    t_v_fall1 = ((Vr-Vmiller+Vth)*Cgdmin*Rg + (Cd+Cl)*(VDC+Vd-
Vmiller+Vth)/gfs)/(VDRH-Vmiller);
    Ig_v_fall1 = (VDRH - Vmiller - (Cd+Cl)*(VDC+Vd-
Vmiller+Vth)/(gfs*t_v_fall1))/Rg;
    dvdt_fall1 = (Vmiller-Vth-Vr)/t_v_fall1;
    E_loss_v_fall1 = 0.5*t_v_fall1*IL*(Vr+Vmiller-Vth)+0.5*(Cd+Cl)*(VDC+Vd-
Vmiller+Vth)*(Vr+Vmiller-Vth);
    % Voltage falling period 2
    Ig_v_fall2 = (VDRH-Vmiller)/Rg;
    t_v_fall2 = (Vmiller-Vth-Von)*Cgdmax*Rg/(VDRH-Vmiller);
    dvdt_fall2 = (Von-Vmiller+Vth)/t_v_fall2;
    E_loss_v_fall2 = 0.5*IL*t_v_fall2*(Vmiller-Vth+Von)+0.5*(Cd+Cl)*(Vmiller-
Von-Vth)*(Vmiller+Von-Vth);
    % Save changing variables
    Ig_1(n,:) = Ig_cur_rise;
    Ig_2(n,:) = Ig_v_fall1;
    Ig_3(n,:) = Ig_v_fall2;
    Ig_avg(n,:) = (Ig_cur_rise + Ig_v_fall1 + Ig_v_fall2)/3;
    t_on_total(n,:) = t_cur_rise2+t_v_fall1+t_v_fall2;
    E_on_loss_total(n,:) = E_loss_cur_rise+E_loss_v_fall1+E_loss_v_fall2;
    didt_on(n,:) = didt_cur_rise;
    dvdt_on1(n,:) = dvdt_fall1;
    dvdt_on2(n,:) = dvdt_fall2;
end
% Normalize the datasets
tontot = (t_on_total)./max(abs(t_on_total));
Eonloss = (E_on_loss_total)./max(abs(E_on_loss_total));
didton = (didt_on)./max(abs(didt_on));
dvdton1 = (-dvdt_on1)./max(abs(dvdt_on1));
dvdton2 = (-dvdt_on2)./max(abs(dvdt_on2));

% Plots
figure(1);
subplot(5,1,1);
plot(Rg_x,t_on_total*10^6);
title('Turn-on duration in us');
subplot(5,1,2);
plot(Rg_x,E_on_loss_total*10^6);
title('Turn-on energy loss in uJ');
subplot(5,1,3);
plot(Rg_x,didt_on*10^-9);
title('Turn-on di/dt in A/ns');
subplot(5,1,4);
plot(Rg_x,-dvdt_on1*10^-9);
title('Turn-on dv/dt (1) in V/ns');
subplot(5,1,5);
plot(Rg_x,-dvdt_on2*10^-9);
title('Turn-on dv/dt (2) in V/ns');
%% Current-mode Driver Turn-on Equations
% Only variable is Ig
Ig = 1;
Igx = linspace(0.25,6,20);
for n = 1:size(Igx,2)
    Ig = Igx(n);
    % Current rising period
```

```
    t_cur_rise = (Ciss*(Vmiller-Vth))/Ig;
    t_cur_rise2 = IL*Ciss/(gfs*Ig);
    didt_cur_rise = IL/t_cur_rise;
    E_loss_cur_rise = 0.5*(t_cur_rise*IL*(VDC+Vd))-(1/3)*(IL^2*SCCLI);
    % Voltage falling period 1
    Vr = VDC+Vd-SCCLI*didt_cur_rise;
    t_v_fall1 = (Vr-Vmiller+Vth)*Cgdmin/Ig;
    dvdt_fall1 = Ig/Cgdmin;
    E_loss_v_fall1 = 0.5*t_v_fall1*IL*(Vr+Vmiller-Vth)+0.5*(Cd+Cl)*(VDC+Vd-
Vmiller+Vth)*(Vr+Vmiller-Vth);
    % Voltage falling period 2
    t_v_fall2 = (Vmiller-Vth-Von)*Cgdmax/Ig;
    dvdt_fall2 = -(Von-Vmiller+Vth)/t_v_fall2;
    E_loss_v_fall2 = 0.5*IL*t_v_fall2*(Vmiller-Vth+Von)+0.5*(Cd+Cl)*(Vmiller-
Von-Vth)*(Vmiller+Von-Vth);
    t_on_total(n,:) = t_cur_rise2+t_v_fall1+t_v_fall2;
    E_on_loss_total(n,:) = E_loss_cur_rise+E_loss_v_fall1+E_loss_v_fall2;
    if E_on_loss_total(n)<0
        E_on_loss_total(n)=0;
    end
    didt_on(n,:) = didt_cur_rise;
    dvdt_on1(n,:) = dvdt_fall1;
    dvdt_on2(n,:) = dvdt_fall2;
end

figure(2);
subplot(5,1,1);
plot(Igx,t_on_total*10^6);
title('Turn-on duration in us');
subplot(5,1,2);
plot(Igx,E_on_loss_total*10^6);
title('Turn-on energy loss in uJ');
subplot(5,1,3);
plot(Igx,didt_on*10^-9);
title('Turn-on di/dt in A/ns');
subplot(5,1,4);
plot(Igx,dvdt_on1*10^-9);
title('Turn-on dv/dt (1) in V/ns');
subplot(5,1,5);
plot(Igx,dvdt_on2*10^-9);
title('Turn-on dv/dt (2) in V/ns');
%% Multi-level Voltage-mode Driver Turn-on Equations
% Variable is VDR,II
Rg = 2.5;
VDRI = linspace(20,25,20);
for n = 1:size(VDRI,2)
    VDRH = VDRI(n);
    % Current rising period
    t_cur_rise = (Ciss*(Vmiller-Vth));
    t_cur_rise2 = (Ciss*Rg*IL + Ls*gfs*IL)/((VDRH-0.5*Vth-0.5*Vmiller)*gfs);
    Ig_cur_rise = (VDRH-0.5*(Vmiller+Vth)-Ls*(IL/t_cur_rise2))/Rg;
    didt_cur_rise = IL/t_cur_rise2;
    V_drop = VDC + Vd - SCCLI*didt_cur_rise;
    E_loss_cur_rise = 0.5*(t_cur_rise2*IL*(VDC+Vd))-(1/3)*(IL^2*SCCLI);
    % Voltage falling period 1
    Vr = VDC+Vd-SCCLI*didt_cur_rise;
```

```
    t_v_fall1 = ((Vr-Vmiller+Vth)*Cgdmin*Rg + (Cd+Cl)*(VDC+Vd-
Vmiller+Vth)/gfs)/(VDRH-Vmiller);
    Ig_v_fall1 = (VDRH - Vmiller - (Cd+Cl)*(VDC+Vd-
Vmiller+Vth)/(gfs*t_v_fall1))/Rg;
    dvdt_fall1 = (Vmiller-Vth-Vr)/t_v_fall1;
    E_loss_v_fall1 = 0.5*t_v_fall1*IL*(Vr+Vmiller-Vth)+0.5*(Cd+Cl)*(VDC+Vd-
Vmiller+Vth)*(Vr+Vmiller-Vth);
    % Voltage falling period 2
    Ig_v_fall2 = (VDRH-Vmiller)/Rg;
    t_v_fall2 = (Vmiller-Vth-Von)*Cgdmax*Rg/(VDRH-Vmiller);
    dvdt_fall2 = (Von-Vmiller+Vth)/t_v_fall2;
    E_loss_v_fall2 = 0.5*IL*t_v_fall2*(Vmiller-Vth+Von)+0.5*(Cd+Cl)*(Vmiller-
Von-Vth)*(Vmiller+Von-Vth);

    Ig_1(n,:) = Ig_cur_rise;
    Ig_2(n,:) = Ig_v_fall1;
    Ig_3(n,:) = Ig_v_fall2;
    Ig_total(n,:) = Ig_cur_rise+Ig_v_fall1+Ig_v_fall2;
    t_on_total(n,:) = t_cur_rise2+t_v_fall1+t_v_fall2;
    Eloss1(n,:) = E_loss_cur_rise;
    Eloss2(n,:) = E_loss_v_fall1;
    E_on_loss_total(n,:) = E_loss_cur_rise+E_loss_v_fall1+E_loss_v_fall2;
    didt_on(n,:) = didt_cur_rise;
    dvdt_on1(n,:) = dvdt_fall1;
    dvdt_on2(n,:) = dvdt_fall2;
end

figure(3);
subplot(5,1,1);
plot(VDRI,t_on_total*10^6);
title('Turn-on duration in us');
subplot(5,1,2);
plot(VDRI,E_on_loss_total*10^6);
title('Turn-on energy loss in uJ');
subplot(5,1,3);
plot(VDRI,didt_on*10^-9);
title('Turn-on di/dt in A/ns');
subplot(5,1,4);
plot(VDRI,-dvdt_on1*10^-9);
title('Turn-on dv/dt (1) in V/ns');
subplot(5,1,5);
plot(VDRI,-dvdt_on2*10^-9);
title('Turn-on dv/dt (2) in V/ns');

%% TURN-OFF Theoretical equations for all drivers
%% Voltage-mode Driver Turn-off Equations
% Only variable is Rg
Rg_x = linspace(2.5,20,20);
for n = 1:size(Rg_x,2)
    Rg = Rg_x(n);
    % Voltage rising period 1
    Ig_v_rise1 = (Vmiller-VDRL)/Rg;
    t_v_rise1 = (Vmiller-Vth-Von)*Cgdmax*Rg/(Vmiller-VDRL);
    dvdt_rise1 = (Vmiller-Vth-Von)/t_v_rise1;
    E_loss_v_rise1 = 0.5*IL*t_v_rise1*(Vmiller-Vth+Von);
    % Voltage rising period 2
```

```
    t_v_rise2 = (Cgdmin*Rg+(Cdsmin+Cgdmin+Cd+Cl)/(2*gfs))*(VDC-Vd-
Vmiller+Vth)/(Vmiller-VDRL);
    Id3 = IL - (Cd+Cl)*(VDC-Vmiller+Vd+Vth)/t_v_rise2;
    Vmiller2 = Vth + (Id3-((Cdsmin+Cgdmin)*(VDC-
Vmiller+Vd+Vth)/t_v_rise2))/gfs;
    Ig_v_rise2 = (0.5*(Vmiller2+Vmiller)-VDRL)/Rg;
    dvdt_rise2 = (VDC+Vd-Vmiller+Vth)/t_v_rise2;
    E_loss_v_rise2 = 0.5*(t_v_rise2*(VDC+Vd-
Vmiller+Vth)*(2*Id3+IL))+0.5*(t_v_rise2*(Vmiller-Vth)*(Id3+IL));
    % Current falling period
    Ig_cur_fall = (0.5*(Vmiller+Vth)-VDRL-Ls*Id3/t_v_rise2)/Rg;
    t_cur_fall = (Rg*Id3*Ciss+Ls*Id3*gfs)/((0.5*Vmiller2+0.5*Vth-VDRL)*gfs);
    didt_cur_fall = Id3/t_cur_fall;
    V_OS = VDC+Vd+SCCLI*didt_cur_fall;
    E_loss_cur_fall = 0.5*(t_cur_fall*(VDC+Vd))*Id3+SCCLI*Id3^2/2;

    Ig_1(n,:) = Ig_v_rise1;
    Ig_2(n,:) = Ig_v_rise2;
    Ig_3(n,:) = Ig_cur_fall;
    Ig_avg(n,:) = (Ig_v_rise1+Ig_v_rise2+Ig_cur_fall)/3;
    t_off_total(n,:) = t_v_rise1+t_v_rise2+t_cur_fall;
    E_off_loss_total(n,:) = E_loss_v_rise1+E_loss_v_rise2+E_loss_cur_fall;
    didt_off(n,:) = didt_cur_fall;
    dvdt_off1(n,:) = dvdt_rise1;
    dvdt_off2(n,:) = dvdt_rise2;
    Vos(n,:) = V_OS;
end

figure(4);
subplot(6,1,1);
plot(Rg_x,t_off_total*10^6);
title('Turn-off duration in us');
subplot(6,1,2);
plot(Rg_x,E_off_loss_total*10^6);
title('Turn-off energy loss in uJ');
subplot(6,1,3);
plot(Rg_x,didt_off*10^-9);
title('Turn-off di/dt in A/ns');
subplot(6,1,4);
plot(Rg_x,dvdt_off1*10^-9);
title('Turn-off dv/dt (1) in V/ns');
subplot(6,1,5);
plot(Rg_x,dvdt_off2*10^-9);
title('Turn-off dv/dt (2) in V/ns');
subplot(6,1,6);
plot(Rg_x,Vos);
title('Turn-off V overshoot');
%% Current-mode Driver Turn-off Equations
% Variable is Ig
Ig = 1;
Igx = linspace(0.25,6,20);
for n = 1:size(Igx,2)
    Ig = Igx(n);
    % Voltage rising period 1
    t_v_rise1 = (Vmiller-Vth-Von)*Cgdmax/Ig;
    dvdt_rise1 = Ig/Cgdmax;
```

```
    E_loss_v_rise1 = 0.5*IL*t_v_rise1*(Vmiller-Vth+Von);
    % Voltage rising period 2
    t_v_rise2 = (VDC-Vd-Vmiller+Vth)*Cgdmin/Ig;
    dvdt_rise2 = Ig/Cgdmin;
    Id3 = IL - (Cd+Cl)*(VDC-Vmiller+Vd+Vth)/t_v_rise2;
    E_loss_v_rise2 = 0.5*(t_v_rise2*(VDC+Vd-
Vmiller+Vth)*(2*Id3+IL))+0.5*(t_v_rise2*(Vmiller-Vth)*(Id3+IL));
    % Current falling period 1
    t_cur_fall = Id3*Ciss/(gfs*Ig);
    didt_cur_fall = Id3/t_cur_fall;
    E_loss_cur_fall = 0.5*Id3*(t_cur_fall*(VDC+Vd))+SCCLI*Id3^2/2;
    V_OS = VDC+Vd+SCCLI*Id3/t_cur_fall;
    t_off_total(n,:) = t_v_rise1+t_v_rise2+t_cur_fall;
    E_off_loss_total(n,:) = E_loss_v_rise1+E_loss_v_rise2+E_loss_cur_fall;

    didt_off(n,:) = didt_cur_fall;
    dvdt_off1(n,:) = dvdt_rise1;
    dvdt_off2(n,:) = dvdt_rise2;
    Vos(n,:) = V_OS;
end

figure(5);
subplot(6,1,1);
plot(Igx,t_off_total*10^6);
title('Turn-off duration in us');
subplot(6,1,2);
plot(Igx,E_off_loss_total*10^6);
title('Turn-off energy loss in uJ');
subplot(6,1,3);
plot(Igx,didt_off*10^-9);
title('Turn-off di/dt in A/ns');
subplot(6,1,4);
plot(Igx,dvdt_off1*10^-9);
title('Turn-off dv/dt (1) in V/ns');
subplot(6,1,5);
plot(Igx,dvdt_off2*10^-9);
title('Turn-off dv/dt (2) in V/ns');
subplot(6,1,6);
plot(Igx,Vos);
title('Turn-off V overshoot');
%% Multi-level voltage-mode Driver Turn-off Equations
% Variable is VDR,II
Rg = 2.5;
Vth = 6; % IMPORTANT TO MAKE VARIATIONS TO THIS TO GET ACCURATE RESULTS  in
this section
Vmiller = 8; % IMPORTANT TO MAKE VARIATIONS TO THIS TO GET ACCURATE RESULTS
in this section
VDRII = linspace(3.5,5.5,20);
for n = 1:size(VDRII,2)
    VDRL = VDRII(n);
    % Voltage rising period 1
    Ig_v_rise1 = (Vmiller-VDRL)/Rg;
    t_v_rise1 = (Vmiller-Vth-Von)*Cgdmax*Rg/(Vmiller-VDRL);
    dvdt_rise1 = (Vmiller-Vth-Von)/t_v_rise1;
    E_loss_v_rise1 = 0.5*IL*t_v_rise1*(Vmiller-Vth+Von);
    % Voltage rising period 2
```

```
    t_v_rise2 = (Cgdmin*Rg+(Cdsmin+Cgdmin+Cd+Cl)/(2*gfs))*(VDC-Vd-
Vmiller+Vth)/(Vmiller-VDRL);
    Id3 = IL - (Cd+Cl)*(VDC-Vmiller+Vd+Vth)/t_v_rise2;
    Vmiller2 = Vth + (Id3-((Cdsmin+Cgdmin)*(VDC-
Vmiller+Vd+Vth)/t_v_rise2))/gfs;
    Ig_v_rise2 = (0.5*(Vmiller2+Vmiller)-VDRL)/Rg;
    dvdt_rise2 = (VDC+Vd-Vmiller+Vth)/t_v_rise2;
    E_loss_v_rise2 = 0.5*(t_v_rise2*(VDC+Vd-
Vmiller+Vth)*(2*Id3+IL))+0.5*(t_v_rise2*(Vmiller-Vth)*(Id3+IL));
    % Current falling period
    Ig_cur_fall = (0.5*(Vmiller+Vth)-VDRL-Ls*Id3/t_v_rise2)/Rg;
    t_cur_fall = (Rg*Id3*Ciss+Ls*Id3*gfs)/((0.5*Vmiller2+0.5*Vth-VDRL)*gfs);
    didt_cur_fall = Id3/t_cur_fall;
    V_OS = VDC+Vd+SCCLI*didt_cur_fall;
    E_loss_cur_fall = 0.5*(t_cur_fall*(VDC+Vd))*Id3+SCCLI*Id3^2/2;
    Vmill2(n,:) = Vmiller2;

    Ig_1(n,:) = Ig_v_rise1;
    Ig_2(n,:) = Ig_v_rise2;
    Ig_3(n,:) = Ig_cur_fall;
    Ig_total(n,:) = Ig_v_rise1+Ig_v_rise2+Ig_cur_fall;
    t_off_total(n,:) = t_v_rise1+t_v_rise2+t_cur_fall;
    E1(n,:) = E_loss_v_rise2;
    E2(n,:) = E_loss_cur_fall;
    E_off_loss_total(n,:) = E_loss_v_rise1+E_loss_v_rise2+E_loss_cur_fall;
    didt_off(n,:) = didt_cur_fall;
    dvdt_off1(n,:) = dvdt_rise1;
    dvdt_off2(n,:) = dvdt_rise2;
    Vos(n,:) = V_OS;
end

figure(6);
subplot(6,1,1);
plot(VDRII,t_off_total*10^6);
title('Turn-off duration in us');
subplot(6,1,2);
plot(VDRII,E_off_loss_total*10^6);
title('Turn-off energy loss in uJ');
subplot(6,1,3);
plot(VDRII,didt_off*10^-9);
title('Turn-off di/dt in A/ns');
subplot(6,1,4);
plot(VDRII,dvdt_off1*10^-9);
title('Turn-off dv/dt (1) in V/ns');
subplot(6,1,5);
plot(VDRII,dvdt_off2*10^-9);
title('Turn-off dv/dt (2) in V/ns');
subplot(6,1,6);
plot(VDRII,Vos);
title('Turn-off V overshoot');
```

APPENDIX B

ANSYS Q3D Extraction tool

ANSYS Q3D was used to extract the parasitic inductances from the DPT board. This tutorial describes the process to perform parasitics extraction of the inductance of copper planes. The process begins in Cadence Allegro, assuming a PCB board has already been designed in that software. The process in ANSYS may be the same even if another PCB design software is used as long as a .dxf file is being imported.

*For simplicity, the original PCB layout, such as the one shown in Figure B.1, should be saved as another version in which all of the component symbols and unnecessary traces are removed. This will simplify the input file to ANSYS, however, these components may also be deleted once in ANSYS.

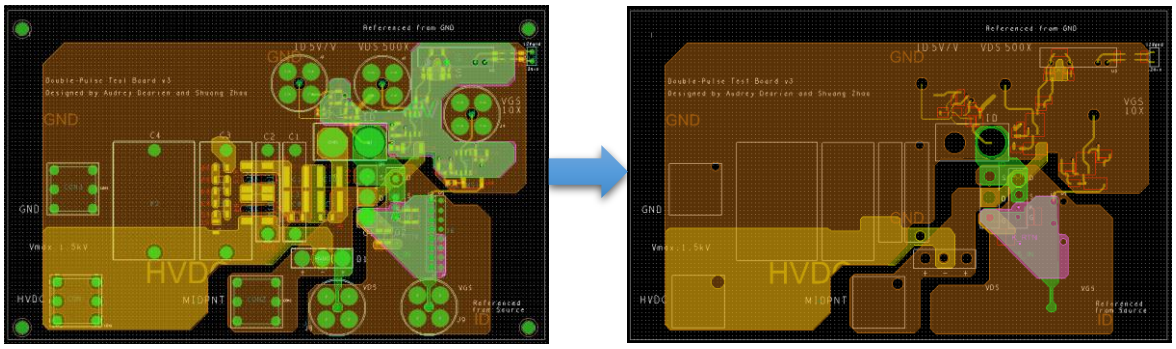

Figure B.1. PCB layout in Cadence Allegro.

- Export the .dxf (drawing exchange format) file of the PCB from Cadence Allegro, as shown in Figure B.2.

- In the 'DXF Out' window, make sure the output units are in the same units utilized in Allegro PCB editor, otherwise the units will be incorrect in ANSYS, Figure B.3.

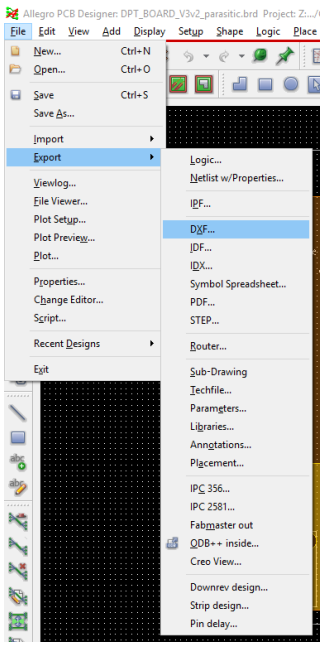

Figure B.2. Export the .dxf file.

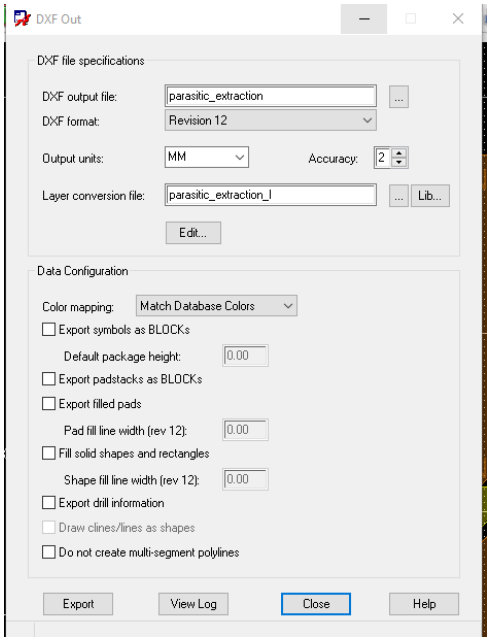

Figure B.3. Setup of DXF export.

- Make sure all the etch layers are selected, as shown in Figure B.4.
- Setup the desired file path and hit ‘Export’.

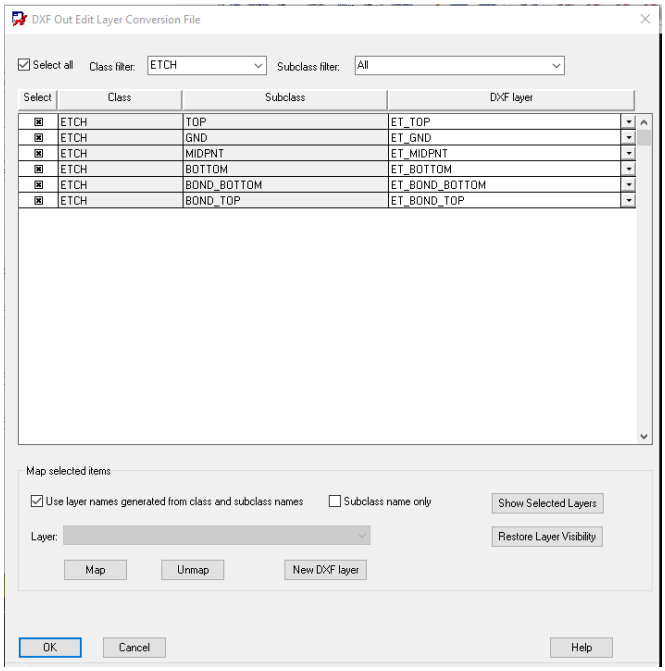

Figure B.4. Output DXF files by layer.

- Open ANSYS Electronics Desktop and insert a new Q3D Extractor design, Figure B.5.

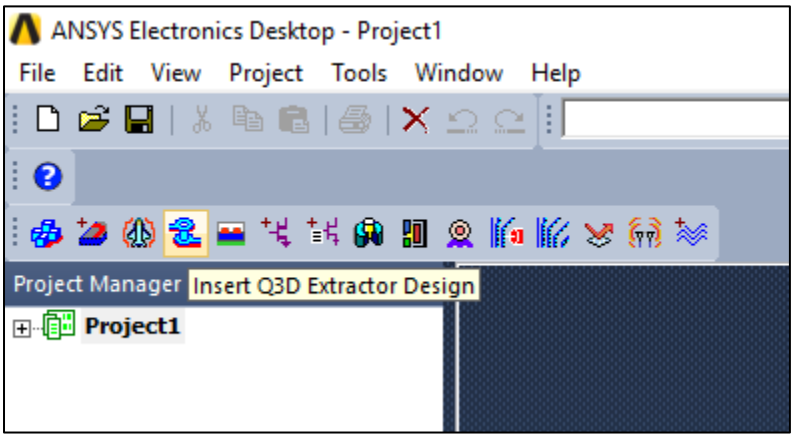

Figure B.5. Insert a Q3D design.

- In the tool bar, go to ‘Modeler’ -> ‘Import’
- Select the *.dxf* file from the folder path set in the previous steps Figure B.6.

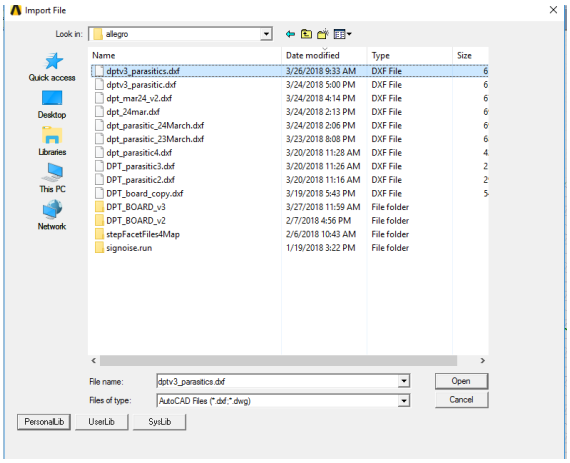

Figure B.6. Selecting the .dxf file.

- The window in Figure B.7 will appear. Select all of the layers and hit ‘OK’.

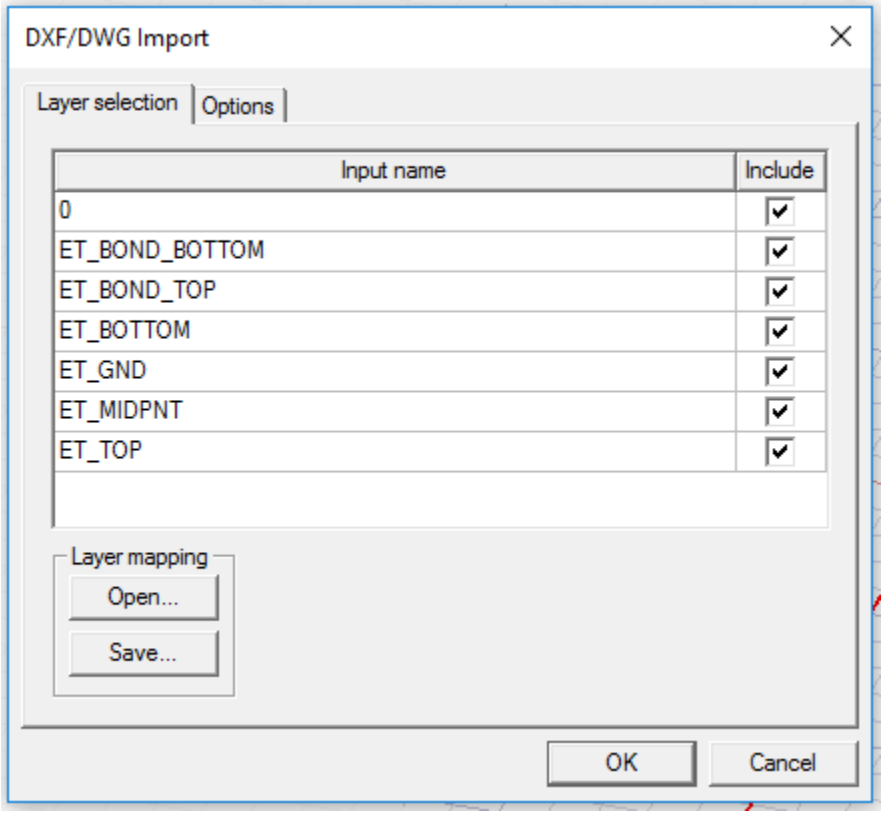

Figure B.7. Selecting the PCB layers from the .dxf file.

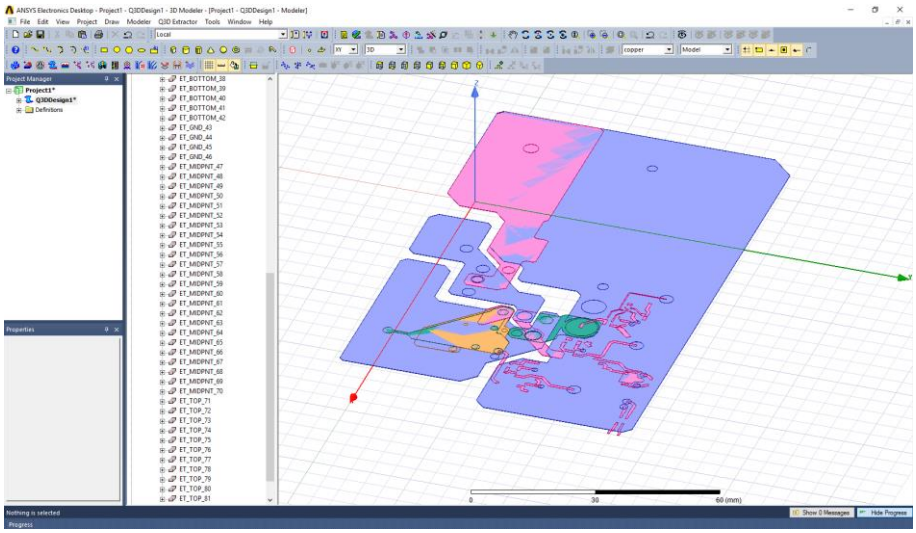

Figure B.8. PCB layers in ANSYS Q3D.

- The layers will be imported into the Q3D design, as shown in Figure B.8.

- All of the planes are on the same layer. They must be separated.

- The distances between layers of the PCB can be found by looking at the Cadence Allegro 'Cross Section Editor' to find the distances, as shown in Figure B.9. These are given in mils, while ANSYS is in mm, so unit conversion may be necessary.

Cross Section Editor

Export Import Edit View Filters

Primary

Objects		Types >>		Thickness >>	Physical >>		Embedded >>	Signal Integrity >>		
#	Name	Layer	Layer Function	Value mil	Layer ID	Material	Embedded Status	Conductivity mho/cm	Dielectric Constant	SI Ignore
*	*	*	*	*	*	*	*	*	*	*
		Surface							1	
1	TOP	Conductor	Conductor	1.2	1	Copper	Not embedded	595900	4.5	☐
		Dielectric	Dielectric	8		Fr-4		0	4.5	☐
2	GND	Conductor	Conductor	1.2	2	Copper	Not embedded	595900	4.5	☐
		Dielectric	Dielectric	8		Fr-4		0	4.5	☐
3	MIDPNT	Conductor	Conductor	1.2	3	Copper	Not embedded	595900	4.5	☐
		Dielectric	Dielectric	8		Fr-4		0	4.5	☐
4	BOTTOM	Conductor	Conductor	1.2	4	Copper	Not embedded	595900	4.5	☐
		Surface							1	

Figure B.9. Cross section editor in Allegro PCB Editor.

- In order to move the layers, such as MIDPNT in this example, from the bottom to 8 mils up, all of the planes on that layer are selected. Then right-click and go to ‘Move’ as shown in Figure B.10.

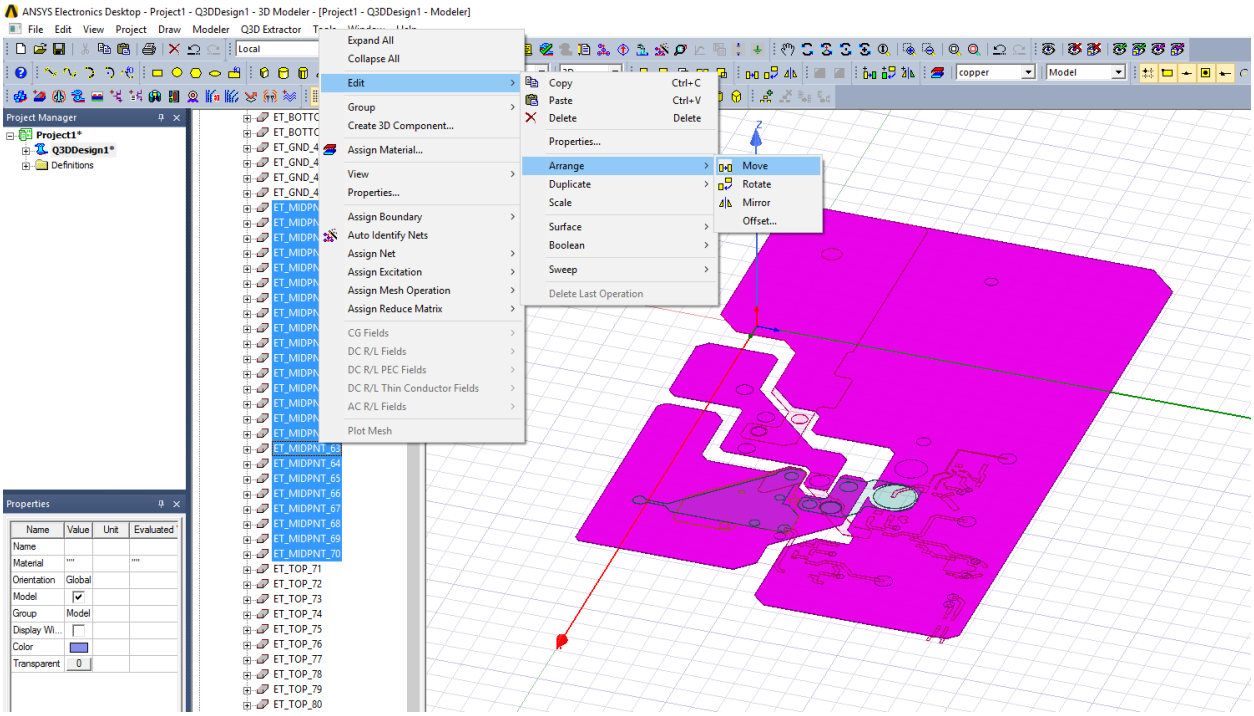

Figure B.10. Moving layers in the z-direction.

- The layers may be moved manually to any position because we can go back and edit the ‘Move’ command to be more precise, as shown in Figure B.11.

- Select all the ‘Move’ commands, and edit the position in the ‘Properties’ section.

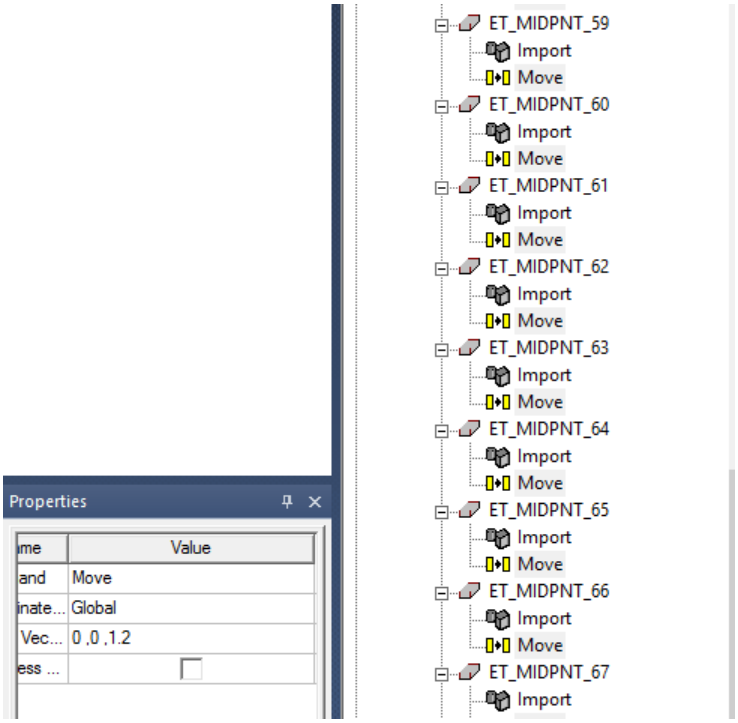

Figure B.11. Editing the move option.

- Repeat these steps for the number of layers in the board design. The bottom layer may be left in the same position, as it serves as the reference for the other layers movement.

- If cutouts were included on the board, or if cutouts are desired to set sources/sinks, the 'Boolean' function may be used to cut these out of the plane.

- The circle shown in Figure B.12 is cut out from the plane to use as a Source later in the analysis. The 'Subtract' window is shown in Figure B.13.

- The result is shown in Figure B.14 where there is now a hole where the circle was.

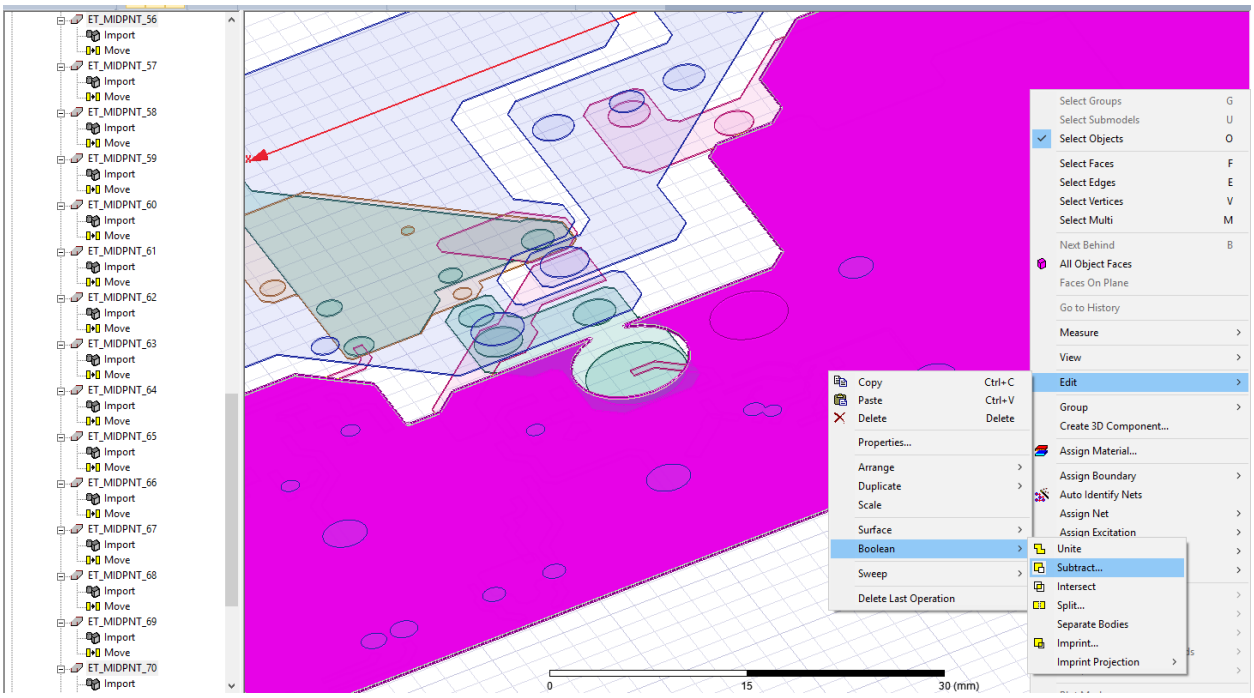

Figure B.12. Using the Boolean function to generate holes/cutouts.

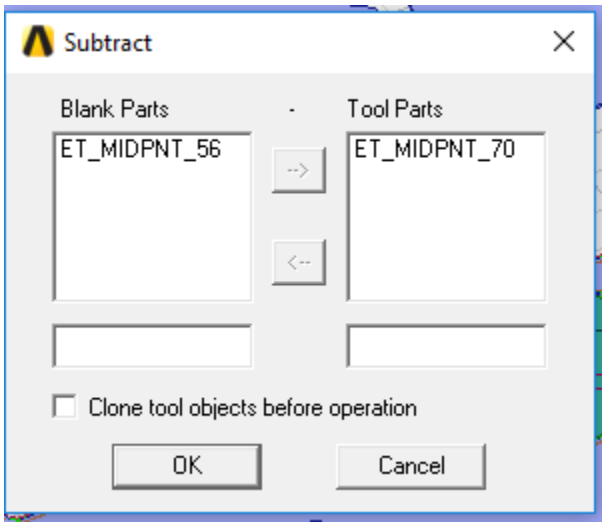

Figure B.13. Using the Boolean subtract function.

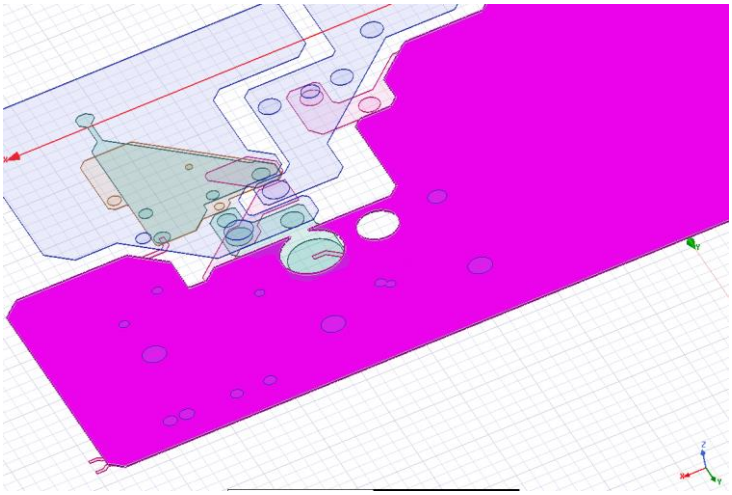

Figure B.14. Hole generated from Boolean subtract edit.

- For the parasitics analysis, the nets have to be detected. First, it is required to set the planes' material properties. In this case, they are all copper layers.

- The materials can be set by selecting all layers, right-clicking, and hitting 'Assign Material'. The copper is chosen as shown in Figure B.15 .

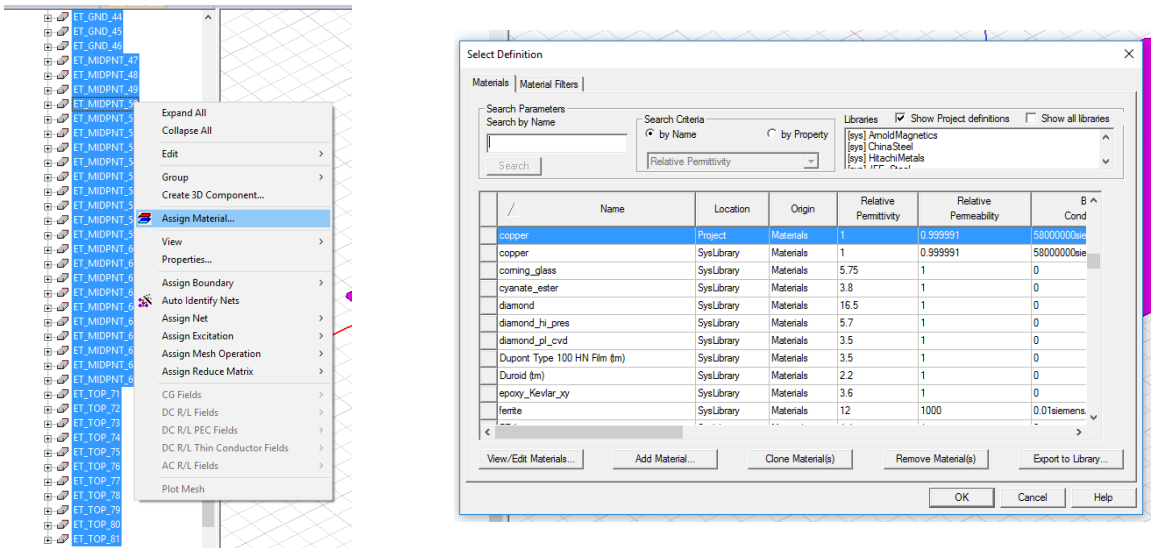

Figure B.15. Setting the material properties for the layers.

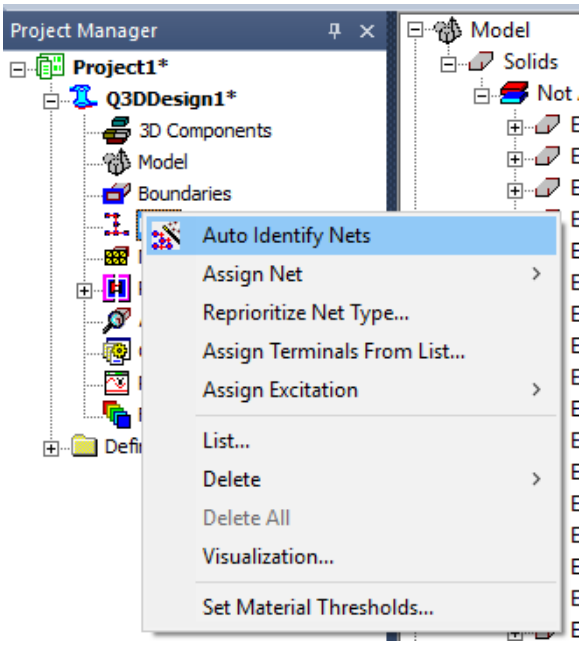

Figure B.16. Auto identifying nets of the copper layers.

- Now the nets can be Auto Identified, as shown in Figure B.16. Right-click ‘Nets’ in the ‘Project Manager’ and click ‘Auto Identify Nets’.

- Next, the sources and sinks for each plane can be set up (there is only one source and one sink allowed per layer, but there can be multiple positions for each by using CTL-select).

- The hole which was created in the previous steps was chosen as a ‘Source’ as shown in Figure B.17 by selecting the face.

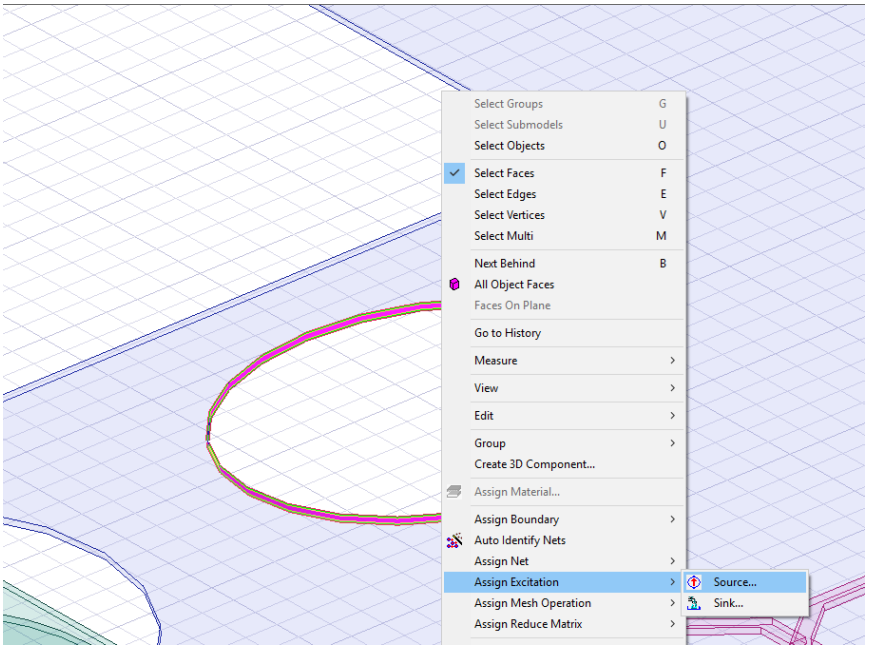

Figure B.17. Setting a 'Source' at the surface of the hole.

- Repeat this step for the desired ‘Sink’ selection on the same plane.

- These steps may be repeated for the number of planes in the PCB design.

- Finally, the analysis can be set up. Right-click ‘Analysis’ and click ‘Add solution step’.

- It is only desired to perform the ac R/L analysis at 1 MHz solution frequency, as shown in Figure B.18.

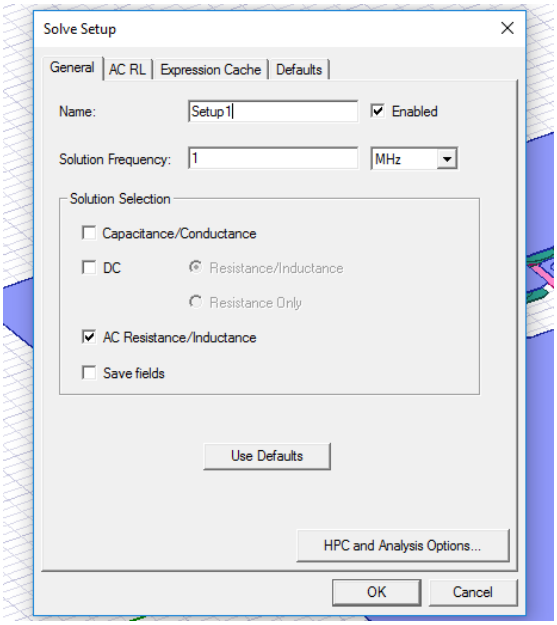

Figure B.18. Solver setup window.

- Hit ‘OK’. Now the solution may be analyzed as shown in Figure B.19. Right-click the solution setup and click ‘Analyze’.

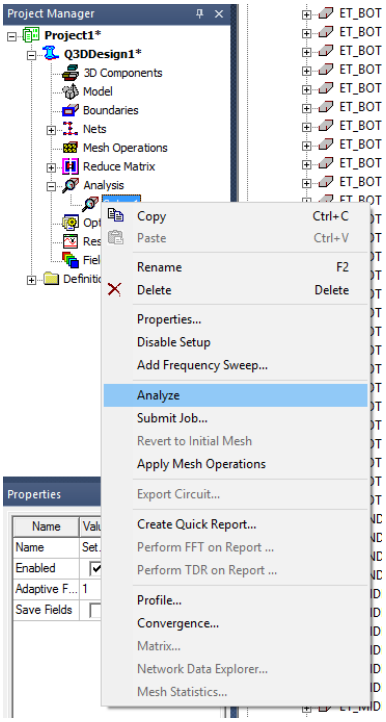

Figure B.19. Performing the analysis.

- After the analysis is completed, a solution matrix is generated including all of the R/L values between each net. This matrix can be accessed by right-clicking the Analysis Setup and clicking ‘Matrix’, as shown in Figure B.20.

- The self and mutual inductances are given in the matrix, as shown in Figure B.21. The matrix can be exported to MATLAB for further processing. The inductance of a particular loop can be found by adding the necessary net inductances together.

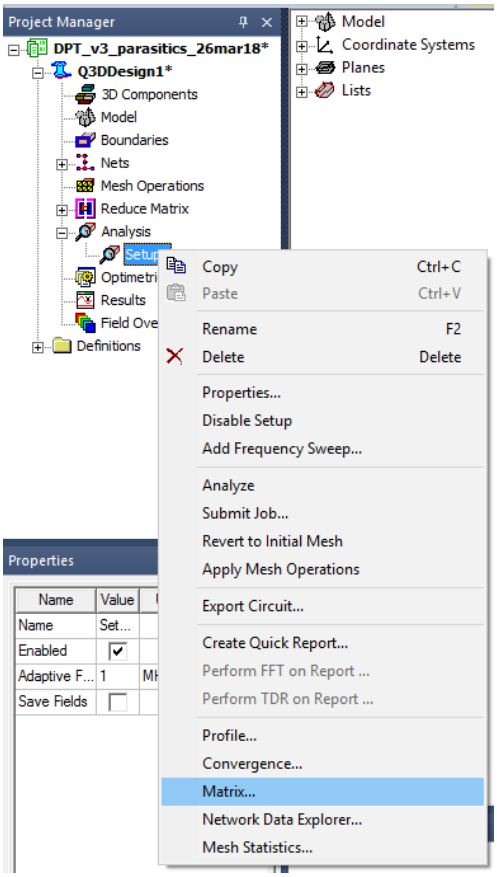

Figure B.20. Viewing the solution matrix.

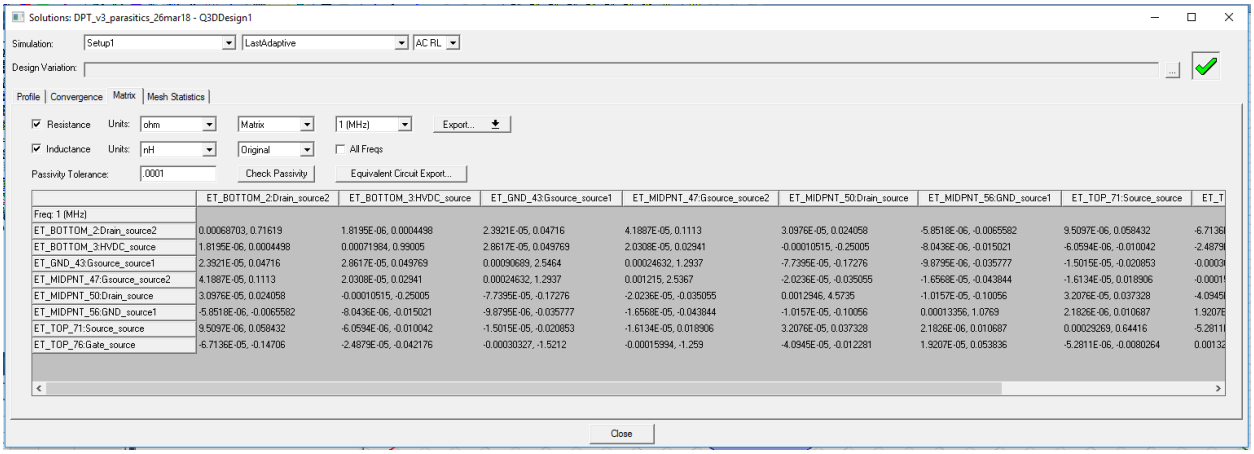

Figure B.21. The solution matrix with R/L values.