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Comparison of low-temperature co-fired ceramic and direct bonded copper for single ended primary inductance topology

Kristopher Cody Johnson
University of Arkansas, Fayetteville

Comparison of Low Temperature Co-fired Ceramic (LTCC) and Direct Bonded Copper (DBC) Substrate Implementation for Single Ended Primary Inductance Converter (SEPIC) Topology

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Kristopher Cody Johnson

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Abstract

This work examines the thermal dissipation characteristics of Low-Temperature Co-fired Ceramic (LTCC) and Direct Bonded Copper (DBC) with the implementation of a Single Ended Primary Inductance Converter (SEPIC) topology. The advantages and disadvantages of the two substrates will be explored in addition to a description of the design and control of the SEPIC. It will be shown that the DBC implementation is superior with regards to thermal dissipation, but that LTCC has advantages in high-density packaging, RF applications, and embedded components. These substrates and converters provide many advantages in industrial applications that include automotive and grid level implementations. Additional comments about best practices in the fabrication and design process are also included.

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Chapter 1 - Introduction

1.1 Opening Comments

Power electronics and the use of power converters in harsh environments and grid-connected applications are becoming more common as researchers attempt to make electrical applications more robust and efficient. Electric cars, DC power transmission, data storage, and battery powered personal electronic equipment all use power converters that must either withstand extreme temperatures and operating conditions or be reliable under constant use and thermal/electrical cycling for years at a time, or both. Ceramic substrates are a means of packaging and implementing power converters in a number of configurations that aid with thermal dissipation, do not corrode, can be packaged very tightly or in layers, and resist various types of shock. Different types of substrates have different advantages as the reader will soon discover, and this work will specifically examine the thermal dissipation characteristics of Low-Temperature Co-fired Ceramic (LTCC) and Direct Bonded Copper (DBC) substrates with respect to the operation of a single-ended primary inductance converter (SEPIC) topology.

1.2 Project Objectives

The basic goal of this project is to simulate, build, and observe the thermal dissipation characteristics of a power converter on both the LTCC and DBC substrates. The chosen power converter in this case is the SEPIC topology because of its ability to step up or step down voltage in addition to its higher part count in comparison to simpler converters such as the buck or boost converters. While a higher part count is not normally an advantageous characteristic of module design, it was thought that the increased part

count would allow for the observance of more points of heat transfer as components like the inductors and transistor began to dissipate power.

The thermal simulations for this project are built and run using Solidworks® Education Edition design software. A correlation is to be drawn between the maximum temperature observed on the devices in the simulation and the maximum temperature the devices actually exhibit on the completed physical module. These temperatures are measured using a thermal camera. After all of the measurements are gathered, a comparison of the thermal dissipation characteristics of both the LTCC module and the DBC module will be done and conclusions as to which substrate is more appropriate for power modules will be made.

Chapter 2 - Background

2.1 SEPIC and Boost Power Converters

The advantages of ceramic substrates are realized in the implementation of power modules, and the power module designed for this project is the (SEPIC) topology. However, an understanding of the operation of a boost converter is also important because of its use in the later stages of this work. These converters operate on similar principles, yet controlling the SEPIC is much more difficult than controlling the boost.

The SEPIC is a DC-DC switching power converter that has the ability to act as a constant voltage source to its load where its source is either at a higher *or* lower voltage potential than that load. This topology has a non-inverting output, a medium efficiency and cost compared to other step-up/step-down switching power converters such as the Cúk converter and has a continuous non-pulsating current sourcing characteristic that allows maximum power sourcing of a photovoltaic (PV) source [1]. In addition to these advantages in the application of a PV application DC-DC power converter, the SEPIC is more stable (and therefore desirable in this application) than the Cúk at maximum power point even though the Cúk responds faster to changes in an MPPT algorithm [2].

The circuit schematic for the SEPIC topology is shown in Figure 1. It requires the use of an input and output filtering capacitor (C1 and C3, respectively), an energy transfer capacitor (C2), two inductors (L1 and L2), a switch (M1, normally an n-type MOSFET), and a controller to control the switching device using a varying pulse width modulation (PWM). The inductors selected can be coupled such that they take up less space and have the same current ripple. The input capacitor reduces input ripple from the source, and the energy transfer capacitor blocks DC current in the event of a permanently

open switch thus protecting the load [3]. It is important to operate the converter in continuous-conduction mode, which occurs if there is current flowing through L2 throughout the entire switching cycle. Continuous-conduction mode is much easier to control than discontinuous mode because the response of the output to changes in the duty cycle is more stable and predictable in continuous mode [3].

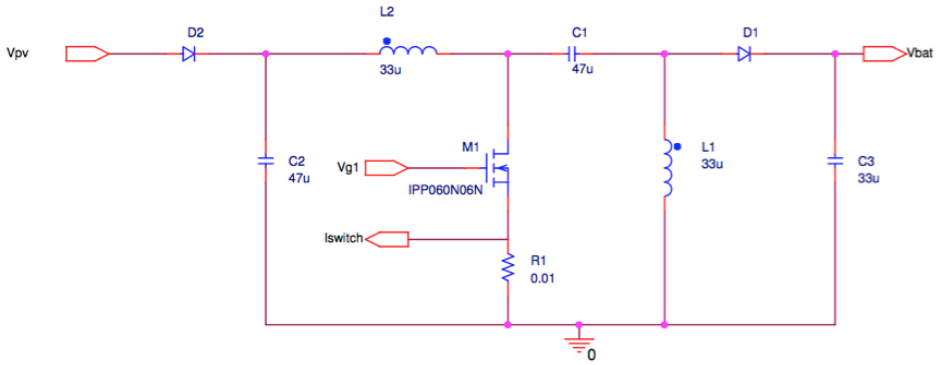

Figure 1: SEPIC Topology

Equation (1) describes the voltage conversion ratio for the SEPIC where V_s is the input voltage, V_a is the output voltage, and D is the duty cycle of the PWM.

$$\frac{V_s}{V_a} = \frac{D}{1-D} \tag{1}$$

This equation describes the ideal case, and the energy transfer would be decreased in actual implementation because of switching losses that include the parasitic resistances of the inductors and diodes, as well as the saturation resistance ($r_{ds(on)}$) of the MOSFET. Equations from application note AN-1484 describe how to size the inductors, capacitors, diode, MOSFET, and duty cycle given the frequency, input voltage, output voltage, and desired current ripple at the output [6].

The SEPIC can also be thought of a boost-buck converter since the first inductor and capacitor act as a boost converter, while the second stage is similar to buck converter

(except the output filter capacitor should be in series with the load as opposed to in parallel with it). A boost converter cannot step down voltage, but can effectively (although not as efficiently) step up voltage to the load [3]. This detail becomes very important in section 4.4 of this work.

Switching power converters need to be carefully controlled, and require the measurement and monitoring of the input and output voltages in order to successfully react to changes in the load or source. These variables are processed through a sensing network that controls a pulse width modulation (PWM) waveform that switches the transistor in the middle of the circuit to control the amount of energy transferred from the input to the output. The simpler topologies such as the buck and boost converters simply need a reference voltage to compare the output to, and then will adjust the PWM accordingly. Some applications require current sensing in addition to voltage sensing in order to calculate and execute a maximum power point tracker (MPPT) such as when using a solar panel as the source [7][8]. As mentioned above, the SEPIC topology in this application is controlled by a LM3478 switching controller that monitors the input and output voltages in addition to the current at the source of the transistor so it can shut down in the event of a high current condition in order to protect the components in the circuit [5][6].

The boost converter is limited to simply stepping up voltage from the input to the output. The circuit schematic for the boost converter can be seen in Figure 2 [3].

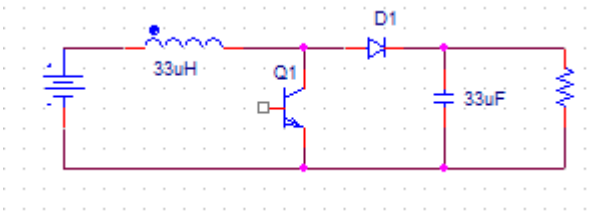

Figure 2: Boost Converter Topology

Equation 2 describes the voltage conversion ratio for the boost converter [3].

$$\frac{V_a}{V_s} = \frac{1}{1-D} \tag{2}$$

In addition to the inverted output characteristic of the boost converter, it is also less efficient as a means of transferring energy from source to load than the SEPIC. The boost is easier to control because it is only a second order system and therefore can be controlled by network that consists of a saw-tooth waveform and comparator that adjusts the PWM based on the output voltage. The LM3478 mentioned earlier can also control a boost converter and does so by monitoring the voltage at the input and output as well as the current at the source of the transistor for current protection. The monitoring of the input and output allows for faster response to load and line transients, which not only protects the components and sources from overvoltage, but also increases the efficiency of the system [3][5].

2.2 Properties of Ceramic Substrates

Designers use ceramic substrates in electronics manufacturing and packaging because they are chemically stable, have high thermal conductivity (similar to that of semiconductor devices), and are resistant to thermal and mechanical shock [9]. Ceramic substrates also have a low dissipation factor that minimizes capacitance and electrical

losses, a low dielectric constant that prevents breakdown at high voltage application, and they have physical and mechanical characteristics that prevent material distortion under high loading and high temperature applications. These substrates have higher compression strength than alloy steel, and a higher tensile strength than porcelain [9].

LTCC and DBC substrates have been around for some time, but have undergone continuous improvement over the years. DBC for instance, developed by General Electric, has been around for over 40 years. As is the case with many new products, adoption of DBC substrates was slow at first because of prohibitive costs, but manufacturers soon discovered the great benefits that DBC can provide. The major advantage to DBC is the "direct bonded copper" characteristic it is named for. The copper conductor of the substrate is directly bonded to a ceramic base which creates a strong bond between the copper and the ceramic base in place of the additional layers of solder and molybdenum to adhere the copper to the substrate in the traditional fabrication methods regarding ceramic substrates. The decrease in layers and material leads to a smaller height profile for the end product, in addition to better thermal cycling performance as a result of decreased thermal expansion of the copper (depending on thickness) because of the decreased thermal resistance in the absence of the molybdenum layer, and higher production yields due to the decreased number of layers to be fabricated [10]. Figure 3 shows a comparison of the traditional bonding method and the DBC method, where the ceramic base in this case is alumina (AlN) [10].

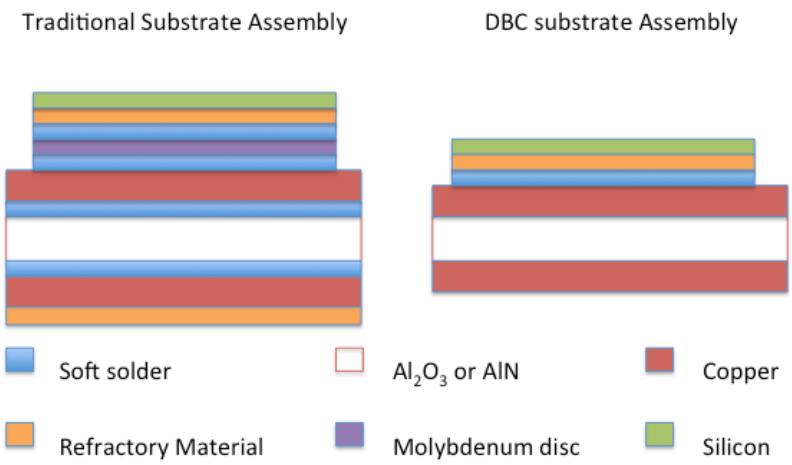

Figure 3: Traditional vs DBC substrate assembly

Because of the increased thermal performance of the DBC method, the substrates can withstand very high current. According to Visser and Snook, a copper foil of .25mm x 1 mm can withstand a continuous DC current of 100 amps with a temperature increase of less than 20 °C [11]. This is a particularly useful characteristic to have in high power modules that deal with fault current limiting or smart switching with grid level applications.

Due to the bonding characteristics of copper, specifically the eutectic bonding temperature of 1065 °C (and a melting point of 1084 °C), the most common ceramic substrates to use for DBC are alumina and beryllium oxide. Other options (such as that shown in Figure 1) is aluminum nitride, however, a thermal oxidation process must be used on the surface of the ceramic before attempting to bond the copper to it. This process can potentially produce a porous bauxite alumina interface between the copper and the substrate that degrades the thermal expansion characteristics as well as the thermal conductivity of the unit. The thermal characteristics of ceramic substrates can be calculated using Equation 3 [11]. Equation 3 describes thermal conductivity of a

compound substrate where **K** is the thermal conductivity of each material and **t** is the thickness of each material.

$$K_e = \frac{K_1 t_1 + K_2 t_2 + \ldots K_n t_n}{t_1 + t_2 + \ldots t_n} \quad (3)$$

DBC substrates are patterned using common printed circuit board techniques such as laser or chemical etching and dicing. Dry photoresist and chemical etching are common for small batch production [11]. Additional assembly and packaging options for DBC substrates include the addition of vias for hermetically sealed packages, integrated terminals and the possibility to liquid-cool the package using a combination of copper-ceramic and copper-copper bonding techniques to stack many layers of copper between the DBC substrates and cycling liquid between them. Liquid cooling is sometimes used to solve cooling problems in both industrial power electronics and automotive applications [10]. Vias can be added to the substrates by drilling holes in the ceramic prior to attaching the copper layer, then filling the via with a conductor in one of several methods including the use of a copper ball into the via after one copper layer is bonded and then adding the other copper layer, placing a copper blank into the via after one copper layer is already bonded then pressing the second copper layer down to it, or just pressing the front copper layer all the way to the back copper layer through the via. Integrated terminals are created by letting the copper layer extend past the ceramic layer, then interleaving it with another module or connection instead of soldering it. These integrated terminals help avoid solder failure between terminals, leave more space available on the substrate, and allow for high current through the interface because of the lack of solder [12].

LTCC substrates have not been around as long as DBC substrates have, but they have been used for couple of decades now and present a number of distinct advantages in

power electronics packaging and applications that need to withstand harsh environments, high temperatures, and/or various types of shock. Other advantages that LTCC substrates present to the power electronics manufacturer is the ability to create very dense packages because of the unlimited number of layers one can create with very reliable and easy to make vias (thickness of course becomes an issue), material properties that make the substrate conducive to RF applications like the low dielectric constant, and the ability to create very fine lines and spaces on the substrate with thick and thin film application of conductors and components [13].

The two thick-film compositions used for LTCC applications are metallizations and dielectrics. The metallizations are conductive pastes that are primarily used for traces and inductors, and are composed of four primary functional ingredients: 1.) a conductive metallic phase consisting of noble metal powders or alloys such as gold, silver, gold-palladium, platinum-gold, copper, aluminum, and nickel 2.) an inorganic binder phase/bonding agent composed of glass powders 3.) an organic carrier agent to suspend the inorganic binder and provide the correct consistency for the paste and 4.) an organic suspension medium. Different atmospheres in the firing environment are required depending on the metals used. For instance, the noble metals such as gold and silver can be fired in normal air, but copper requires a nitrogen environment to prevent oxidizing contamination [9].

Thick-film dielectric materials are used to insulate conductive patterns as well as create high dielectric constant (k) capacitors. These dielectric materials are comprised of crystallizing dielectrics and glass-filled ceramics such as barium titanate, lead titanate, and lead zirconate titanate. These compounds are heated to remove impurities, ball-

milled to 1-10μm and mixed with a carrier agent for the screen-printing process. The final processed products have dielectric constants of between 20-1200 [9].

Thick-film resistors are either resinate or cermet systems. These molecular compounds are described most concisely by Barlow and Elshabini as such: "Precious metal resinates are solutions of metal chlorides in organic solvents or organometallic compounds in which the metal atom is attached to an oxygen atom linked to a carbon atom. Cermets are materials resulting from a fused structure of conductive or resistive material in a vitreous nonconductive binder." The resistive pastes are comprised of resistive materials (normally selected from a number of metal-oxides), a glassy phase, an organic suspension medium, and diluted with another organic solution to be removed in the firing process. These resistors can be created with resistivities of 1Ω/square – 5MΩ/square sheet resistance. The thermal coefficient of resistance (TCR) of thick film resistors makes the conductivity of the materials complex in thin layers. Although metals normally have a positive TCR, when some of the active material is dissolved into the glass material during firing, the effect is similar to that of semiconductors with a negative TCR. The dimensions of the resistors affect TCR as well. Short and narrow resistors have a higher TCR than long wide resistors due to the diffusion of the active material across a wider area [9].

LTCC presents a distinct advantage over HTCC (high-temperature co-fired ceramic) substrates because LTCC can be fired at 875°C while HTCC must be fired at 1600°C and do not need to be plated by Ni or NiAu to bond or solder efficiently. The advantageous RF characteristics of LTCC substrates include the ability to integrate

passive RF functions on the substrate level between ceramic layers to perform functions such as a filter, a balun, or matching network [13].

The LTCC substrate process is a bit more complicated than the DBC process, but yields the distinct advantages mentioned in the previous paragraphs. One of the challenges to overcome in LTCC substrate fabrication and processing is the issue of shrinkage matching between the green tapes (the flexible LTCC substrate material before it is fired and hardened) and the metal inks (conductors) and components to be placed on the substrate. Early versions of the LTCC green tapes could shrink up to 16% in the firing process in the X and Y directions, and up to 25% in the Z direction [13]. However, current green tape products such as the pressure assisted zero-shrinkage sintering process for Murata's LFC® series tapes only shrink in the z direction leaving the pad size unchanged [15].

LTCC substrates yield additional advantages as well as some additional challenges when designed for RF and multi-layer applications. As the operating frequency of the circuit laid on the substrate increases, stray inductances increase in the traces used to connect components. Also, stray capacitances increase with the number of layers of substrate used and the voltages utilized in the modules. Since these substrates are well suited to use in high power applications, the voltages (and therefore capacitances between layers) can be quite significant.

Some methods have been developed in order to mitigate the effects of high frequency operation through improved deposition and fabrication techniques of embedded and printed passive components. One such method is to control the shape of embedded printed inductors so that their cross section is rectangular as opposed to

almond shaped. The almond shaped conductive material for these inductors have sharp edges in the cross sectional area that have larger leakage currents as opposed to rectangular conductors [16].

Additional options and developments for LTCC fabrication continue to come about as new materials and fabrication methods are researched and published. Inductors, capacitors, resistors, and transformers can be printed on substrates or embedded between layers in order to continually reduce overall package size. Ferrite and dielectric materials can be combined and co-fired with LTCC substrates to create highly reliable magnetically coupled inductors and transformers. The combination of ferrite and dielectric tapes and pastes also allow for the isolation of magnetic circuit components and conductive traces in different layers to prevent parasitic inductances. These fabrication techniques increase the appeal for using LTCC substrates to make system-in-package products that are compact with high circuit density [17].

Chapter 3 - Fabrication and Simulation

3.1 SEPIC Design

The SEPIC is a second order circuit with a left hand plane zero when used with closed loop feedback, so it is difficult to control where line and load transients may occur since it is not inherently stable in steady state. Using the equations from Hammerbauer and Stork, a Simulink® simulation of the ideal behavior of the converter was built in order to determine maximum operating conditions and adequately size the components [4]. The appendix contains many of the hands calculations done in order to solve for the component specifications such as maximum current and voltage experienced by the circuit based on the minimum and maximum input and output parameters for the system. The appendix also contains Matlab® code that was written in order to iteratively calculate the aforementioned component specifications based upon different input and output conditions possible in the test environment.

Figure 4 shows the Simulink® functional block diagram that was built using the equations from Hammerbauer and Stork. The switch and pulse generator blocks were used to simulate the PWM, but were limited to a constant duty cycle. The gain blocks with the "R" caption took the equivalent series resistance (ESR) of the inductors and capacitors into account. The gain blocks with "1/Cx" or "1/Lx" in the caption are the values of the various inductors and capacitors that were simulated. The sum and integrator blocks were used to complete the implementation of the state space equations from the Hammerbauer and Stork work. Figure 5 shows the voltage and current values observed in the simulation for each of the components of concern.

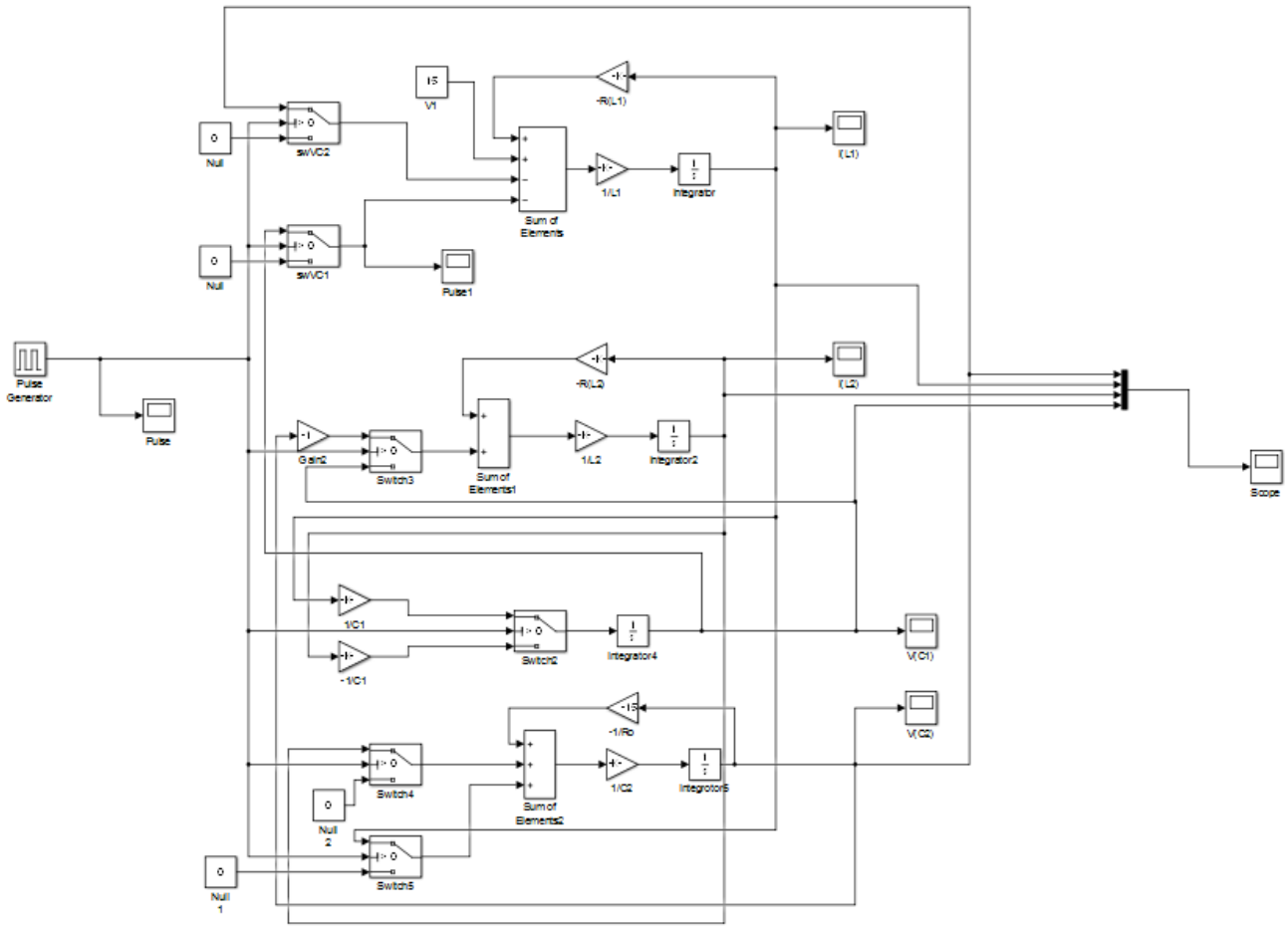

Figure 4: Simulink® Functional Block Diagram

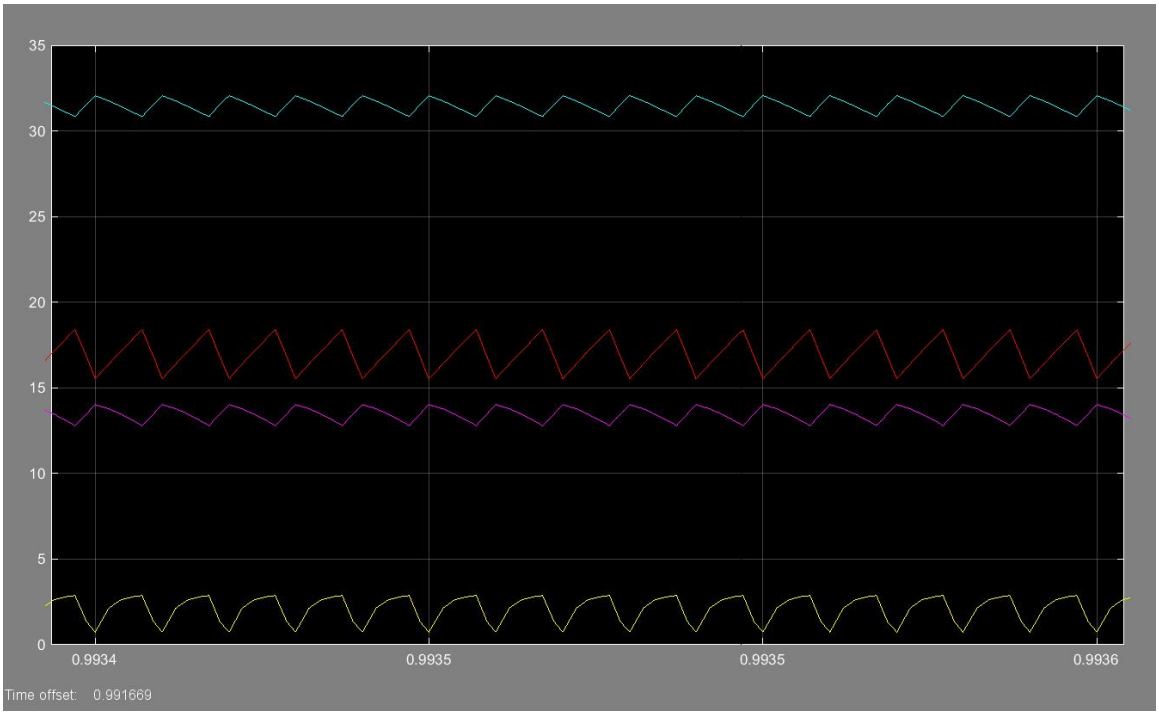

Figure 5: Simulink® Simulation of SEPIC- Purple=I(L1), Yellow=V(C2), Cyan=I(L2),Red=V(C1)

Figure 5 shows the maximum currents and voltages possible in an idealized system for the SEPIC topology. One should note that very high currents are possible in the inductors, but that the waveforms that appear to be steady state in this figure are actually peak values since the state space calculation was run with a fixed maximum duty cycle as opposed to a variable PWM controlled by input and output variables. The variable PWM regulates the energy transferred to the output, and if the output is a battery, the voltage is clamped to the battery voltage such that it is relatively constant but for the minor change in battery charge as the battery is charged.

3.2 Board Fabrication

The fabrication of the LTCC and DBC modules was accomplished with the help of many faculty, staff, and graduate students in the University of Arkansas Department of Electrical Engineering and the High Density Electronics Center (HiDEC) associated with

it (see acknowledgements). The LTCC module began with a blank green tape and a circuit trace layout built using AutoCAD® Student Edition software. The trace layout was sent to a third party manufacturer to be mounted as a negative mask in a screen mesh to be used on the screen-printing machine. The LTCC was layered and fired as a stack multiple green tapes in order to approximately match the thickness of the DBC board. After the green tape was fired, the traces were printed on it and the board was fired again in order to cure the traces.

The DBC module used the same traces design as the LTCC board in order to be as consistent as possible for comparison of thermal performance. The DBC traces were printed onto a negative transparency, zinc plated, then chemically etched in order to bring the traces out of the solid copper sheet of one side. There were some defects in the DBC production process because of the dry film coming away from the board to allow the chemical etching to erode the traces. However, multiple copies were produced in order to minimize risk. After the boards were fully fabricated, the components were placed on the boards with solder paste and put into a conveyor oven to complete the solder reflow process. Figures 6 and 7 show the fully fabricated LTCC and DBC (respectively) boards with the components attached.

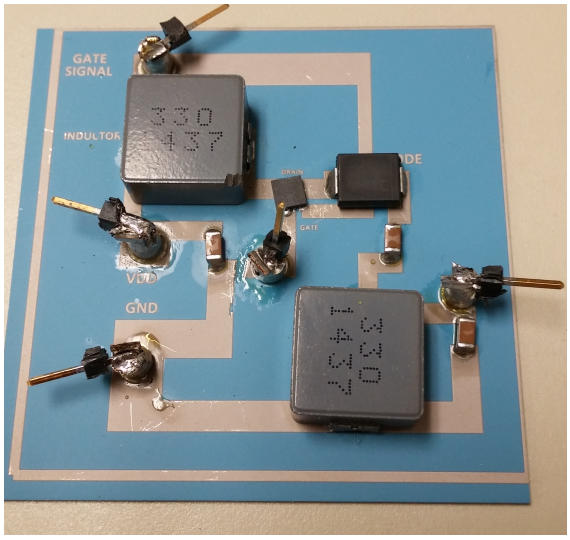

Figure 6:Fully Fabricated LTCC Board

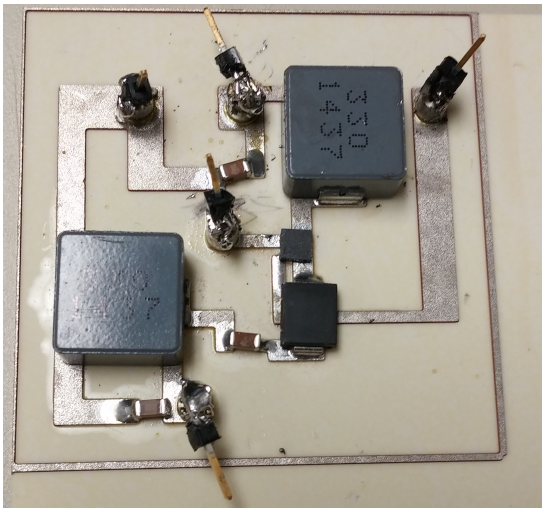

Figure 7: Fully Fabricated DBC Board

There were some problems with the reflow solder process because of the size of the traces on the MOSFET. The solder that was placed on the gate and source bled over the ceramic between the traces and shorted these two nodes on all but one of the LTCC boards. There were attempts to solve this problem by using a soldering iron and hotplate

to liquefy the solder between the traces, but this proved impossible because the substrate dissipated heat so quickly that the solder would not get to melting temperature on a large enough area to clear the short. A hot air gun was not used, but is an option that should have been explored.

Additional problems were encountered when it was realized that there were no physical points on the board that could be attached to probes to supply power, the gate signal for switching, nor the input, output, or ground signals for control and analysis. This lead to the creation of custom surface mount sockets and pins created from header pins and wire sockets that were attached to the surface of the board using the solder iron and hot plate method mentioned above. Again, this proved difficult because of the heat dissipation characteristics of the boards. In the end, however, solid solder bonds were created such that the circuit could function using off-board testing equipment and power sources.

3.3 LM3478 Implementation

The use of the LM3478 switching controller is an important step to testing, simulating, and operating the SEPIC converter for this project. The appendix contains the design schematic of the controller as well as many of the calculations and test bench observations for the design of not only the controller, but also for the sizing of the SEPIC components themselves. This controller was tested on the SEPIC with through hole components on a bread board in order to ensure the operation of the SEPIC converter with the initial calculated component sizes, and was then put onto a milled PCB milled in the University of Arkansas Senior Design Lab in order to make testing easier because of its modular implementation. Figure 8 below shows the final milled board with the

LM3478 mounted with pins along the right side for off-board connections to the converter module.

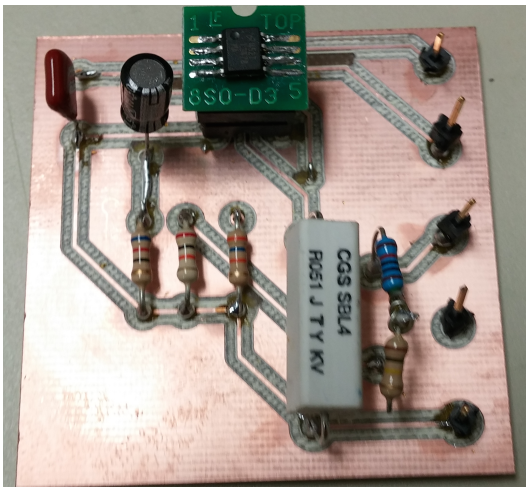

Figure 8: LM3478 Board Implementation

3.4 Circuit Modification

Immediately before testing began, it was realized that there was a fatal error in the trace layout of the SEPIC topology. Two of the critical components in the middle of the circuit were laid out in the wrong place. The diode was placed prior to the 47uF energy transfer capacitor and output inductor rather than after, so the energy transfer through the capacitor and inductor was blocked by the diode rather than the diode blocking back fed current from the load. This of course, was a serious and significant problem. Figure 1 shows the intended layout, and Figure 9 below shows the circuit that was actually fabricated.

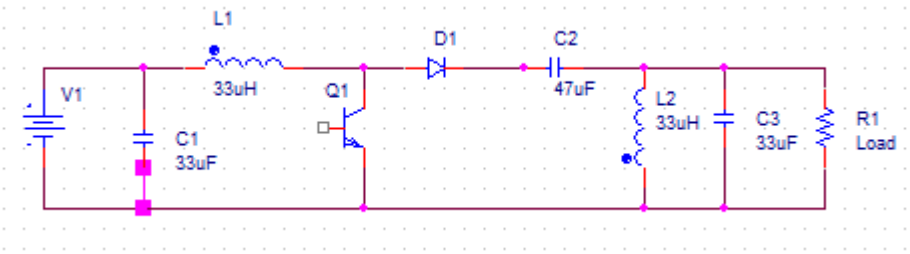

Figure 9: Schematic of Physical Circuit

By the time that this mistake was realized, there was no more time or funding to redesign another set of traces and then have them ordered and placed in a screen or transparency, then fabricate two more sets of boards. So, a modification of the circuit was made in order to rectify this mistake. In Figure 9, the output filter capacitor (C3) and the output inductor (L2) were removed and the node that they shared with the energy transfer capacitor (C2) was connected to ground. This meant that the schematic could now function as a boost converter where the output would now be the node shared by the diode (D1) and C2.

This solution was not ideal, but did allow for the operation of the circuit in order to observe the thermal characteristics that were the goal of this project. Additionally, the LM3478 was not needed after the purchase of a new function generator by the lab that had the ability to modify the duty cycle of the waveform generated. Since the boost converter is generally stable, it could be controlled by simply adjusting the duty cycle of the function generator as opposed to the need to control the SEPIC from unbounded operation by monitoring multiple variables with the LM3478, as mentioned earlier.

Figures 10 and 11 below show the final incarnation of the power converters that were tested. Notice that the output inductor and capacitor (bottom right two components from the boards in Figures 6 and 7) have been removed. One can see in Figure 10 that the

removal of these devices removed the traces that were screen printed onto the LTCC, so a solder trace had to be placed over where the component pad was. Both of the final boards appear worse for wear due to the reworking that was required to remove the original components, solder bridge over ripped off pads, and attach an additional pin at the new output node between the diode and C2.

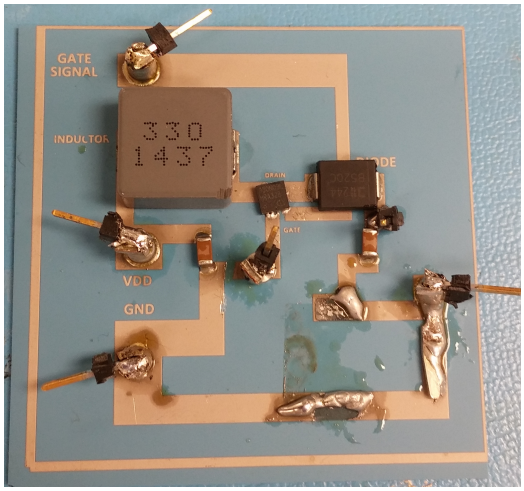

Figure 10: Final LTCC Module

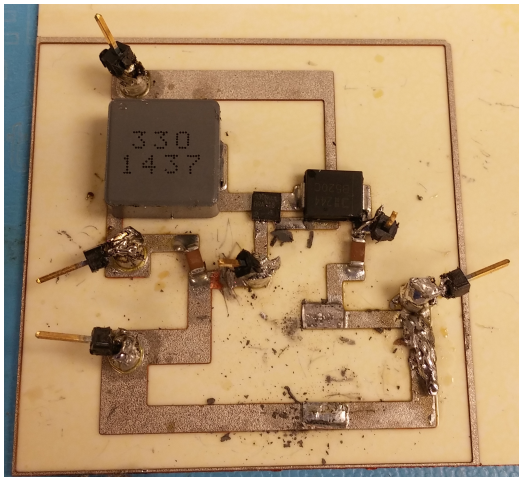

Figure 11: Final DBC Module

3.5 Thermal Simulation in Solidworks®

In order to obtain an idea of how the modules would perform under test conditions, a Solidworks® model was built of the module and a thermal simulation was performed. Due to the limitation of a Student Edition license for Solidworks® in addition to the lack of experience in the software, the models are simple yet demonstrate the key points of interest with regards to the thermal behavior substrates. The series of figures below show the results of the thermal study in Solidworks®. The figures are labeled both with captions and with notations in the upper left-hand corner of the figure, and the thermal scale in Kelvin can be seen on the right-hand side of each of the figures. The first set of images, Figures 12 and 13, show views of heat dissipation from the inductors on the LTCC, then a view of the heat dissipation from the MOSFET on the LTCC.

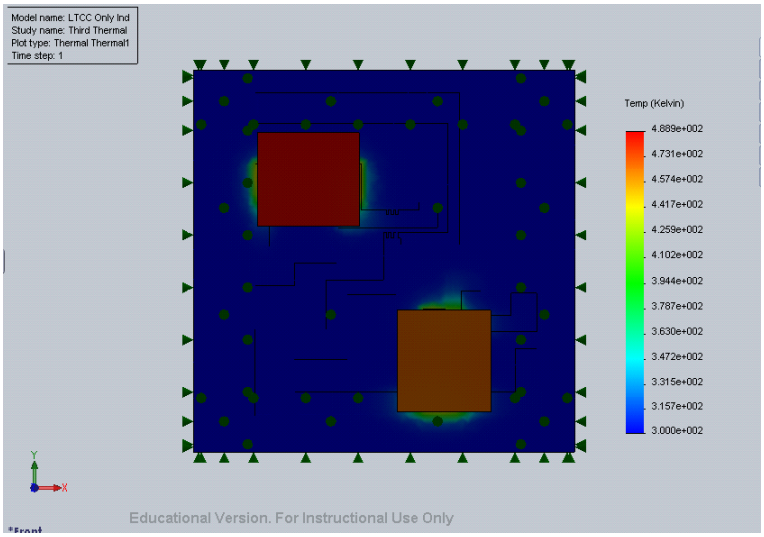

Figure 12: Inductor Heat Dissipation Simulation (LTCC)

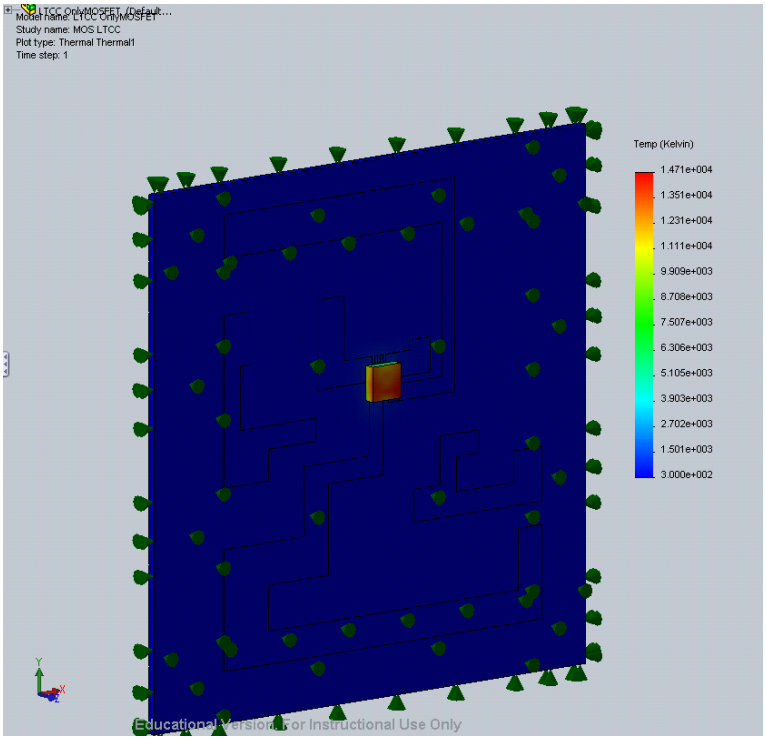

Figure 13: MOSFET Heat Dissipation Simulation (LTCC)

Figures 14 and 15 show the same views of the inductor and MOSFET heat dissipation, but with regards to the DBC module.

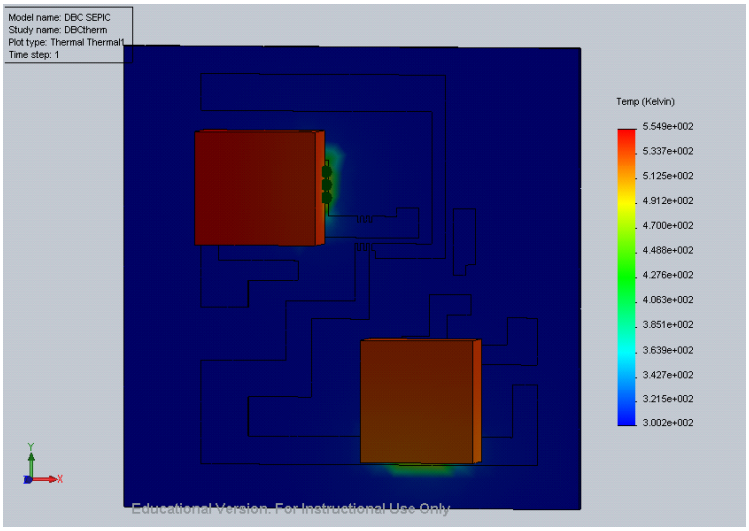

Figure 14: Inductor Heat Dissipation Simulation (DBC)

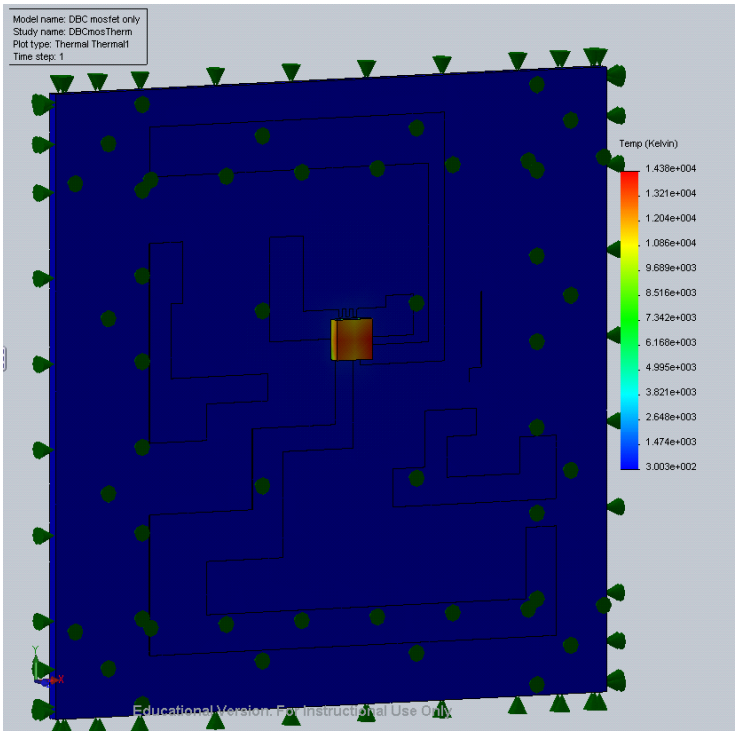

Figure 15: MOSFET Heat Dissipatoin Simulation (DBC)

The inductor simulations were run with a thermal load on the inductor of 25 watts. The MOSFET simulations were run with thermal load conditions increased to 50 watts since the 25W MOSFET simulations were difficult to observe due to lack of contrast between the part and the substrate. The maximum temperature shown in the simulation is markedly higher (by almost 70 Kelvin) on the DBC inductor simulation as opposed to the LTCC inductor simulation. However, the there is only a 30 K difference between the two MOSFET simulations, and the MOSFET temperature on the LTCC is actually hotter than when it is on the DBC. The simulations do not suggest that the substrates (simulated as ceramic porcelain) carry the thermal energy very far from the component before it is fully dissipated to room temperature. The simulations also suggest that the LTCC may be better suited to dissipating highly concentrated thermal loads better than DBC, while

DBC is may be better for dissipated loads with more surface area contact to the traces and substrates.

Chapter 4 - Analysis and Testing

The first tests performed were to confirm that the modified SEPIC into boost a converter actually worked and transferred energy from the input to the output in order to sufficiently heat up the components through power dissipation. The boost converters on both substrates were tested at a switching frequency of 100kHz and input voltage of 10V. As expected, the voltage at the output increased proportionally (inverted, of course) as the duty cycle increased according to the voltage conversion ratio in Equation 2. Figures 16 and 17 show the gate signal (in blue) and the drain to source voltage across the MOSFET (in yellow) for the LTCC and DBC implementations (respectively)

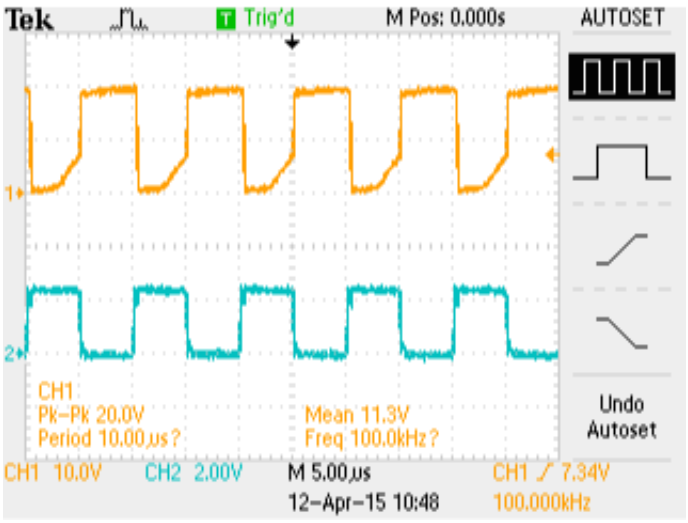

Figure 16: Test of Boost on LTCC

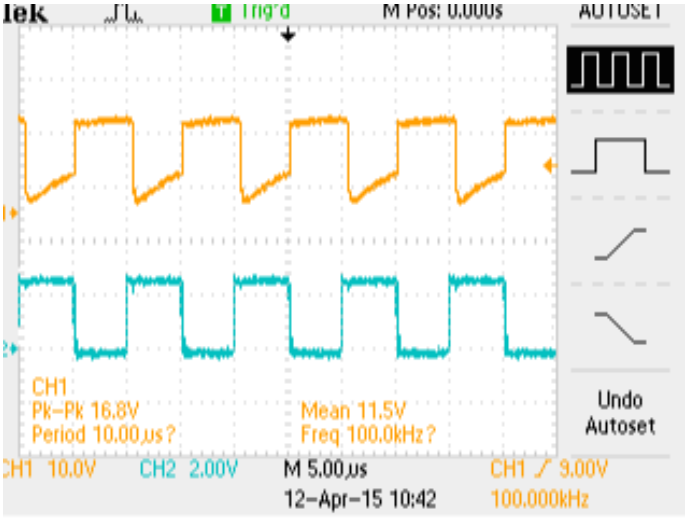

Figure 17: Test of Boost on DBC

One should note the voltage discharge curve in the yellow drain to source waveform in both of the figures above. This voltage tracks the voltage on the input capacitor as it transfers energy to the inductor. Since the circuit was modified from components designed for a different converter topology, there was a concern that the performance of the boost would not be ideal. However, as the next figures show, the converter performed very well and was sufficient to observe the thermal characteristics of the substrates.

Figures 18 and 19 below show an infrared image capture from a Flir® thermal camera. The circuits were connected to the source as mentioned above and discharged into a 20Ω power resistor for a minimum of 1 minute in order to build up a sufficient amount of heat in the components and the substrates. Figure 18 shows the LTCC infrared image, and Figure 19 shows the DBC infrared image.

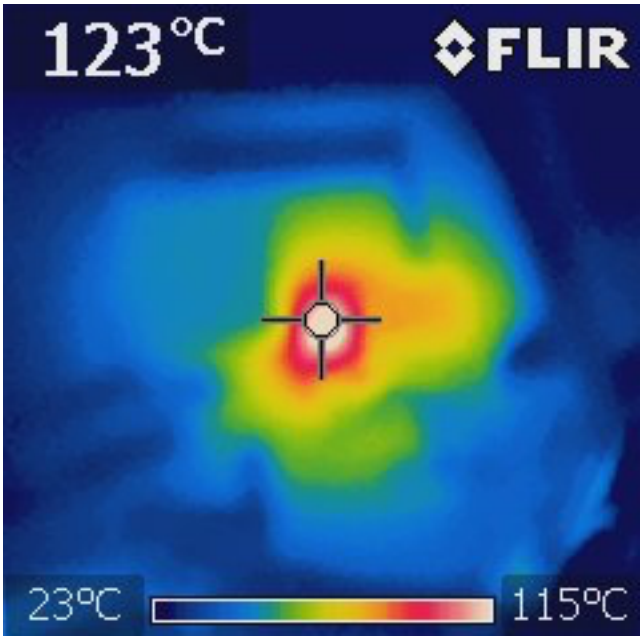

Figure 18: Infrared Image of LTCC Boost Converter During Operation

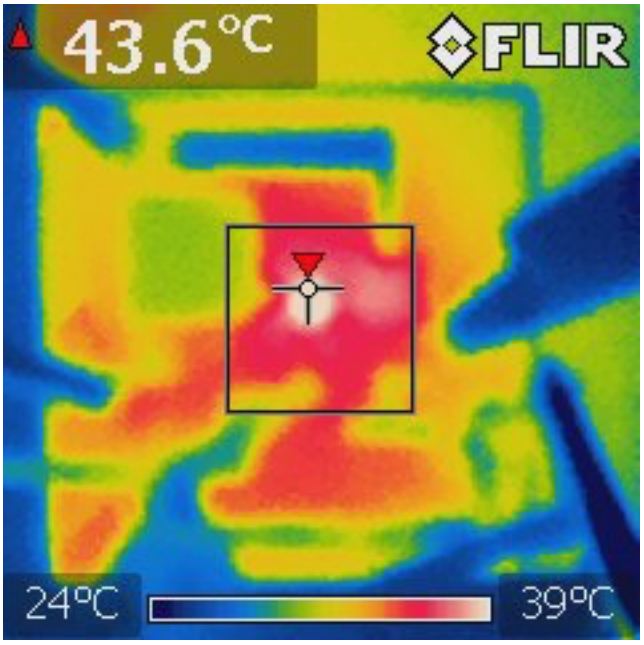

Figure 19: Infrared Image of DBC Boost Converter During Operation

In this application, the DBC performed much better than the LTCC in dissipating heat away from the components generating it and out to the substrate where it could escape by convection. Figure 18 shows how the heat generated by the MOSFET (the

white area) spreads out to toward the diode (the orange area to the right of the MOSFET), but does not extend to the edge of the board. However, one can identify almost all of the relevant components in Figure 19 by how the heat signatures surrounding them. The green-blue square to the right of the MOSFET is the inductor, and the red-white object to the right of the MOSFET is the diode. The alligator clips, oscilloscope probes, and the gate signal trace are all a cool blue at near room temperature because the ceramic substrate beneath them is dissipating the heat to its very edges.

Perhaps the most important thing to observe with regards to these thermal images is the maximum operating temperature of the components. During continuous operation, the DBC module never allowed the MOSFET temperature to rise above 50°C, whereas the LTCC module could not draw the heat away from the MOSFET and increased the temperature to the rated temperature of the component (150°C) at which time the circuit was shut down due to safety concerns. These observations contradict the simulation profiles observed in Solidworks®. However, further testing to determine whether thermal vias or increased component surface area on the LTCC implementation would allow it to match the thermal dissipation performance of the DBC may prove insightful.

Chapter 5 - Conclusion

The DBC substrate is a clear winner with regards to thermal dissipation for power converters based upon the findings shown in this paper. The advantages of the LTCC lie in the ability to create fine-line traces and multiple layers on a versatile substrate, and while it is made of a ceramic material, could not compete with the performance of the DBC with regards to heat dissipation. An LTCC module could have a heat sink attached to it in order to bolster its ability to wick heat away from its components, but this works against the benefit of LTCC to fit into small multi-chip modules (MCM) and perform well in the high-frequency applications it is becoming so popular for.

The success of the DBC in these tests is attributed to the dual copper layer on the substrates. The traces were only used on one side of the board, so the back side was simply a sheet of copper attached to the ceramic substrate layer that acted like a built-in heat sink. Performance of the DBC could improve in this application if heat sinks were soldered to the back of the module in order to increase the amount of surface area exposed to circulating air.

The actual performance of the boards with regards to the Solidworks® simulations was inconsistent at best. The thermal behavior of the substrate in the LTCC MOSFET simulation most closely resembled the actual performance of the substrates during the testing phase. Better simulation profiles could be built with component models that are more precise as opposed to cuboid representations of the material and size properties such as were used here. Also, more familiarity with the eccentricities of the software would aid in the accurate and custom simulation of more variables within the test environment that may contribute to the dissipation characteristics such as a manually

configuring the model meshing and thermal resistance between materials as opposed to running “automatic” or “default” settings for these variables.

In addition to the technical conclusions mentioned, there are a number of lessons learned with regards to the collaborative design process a whole that should be mentioned. The error in the trace layout evolved from a miscommunication and poor labeling of the design that led to this critical detail being overlooked before the fabrication process was initiated. Pressure to move to the fabrication stage because of approaching deadlines and an eagerness to begin testing led to restructuring of the scope of the project. It is fortunate that the project was salvaged, but a multi-layer board would not have been so easy to fix if a fix would have been possible at all. Finally, the communication required in order to coordinate the use of facilities, personnel, expertise, and diagnostic equipment is a daunting task that consumes at least as much time as the work itself does. It takes a tremendous amount of organization and cooperation with all parties involved in order to use the time and resources available effectively. Without the time, patience, and willingness to help of all of the people and organizations mentioned in the acknowledgments, this project would have been much more difficult than it was.

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Appendix

The following pages contain hand written calculations, design simulations, Matlab® code, and Simulink® code that were instrumental for this work to be a success.

LM3471

Implementation 33 μH

$V_{in\,min} = 5V - 7.5V$

Output Voltage: 9V

Output Current: 600mA

$$D_{max} = \frac{9V + 0.5V}{5V + 9V + 0.5V} = 0.655$$

$$\Delta I_L = 0.6A \times \frac{9V}{5V} \times 0.655 = 0.7A$$

$$I_{L,peak} = 600mA : \frac{9V + 0.5V}{5V} \cdot \left(1 + \frac{0.655}{2}\right)$$

$$= 1.5A$$

$$I_{L_2 peak} = 600mA\left(1 + \frac{0.655}{2}\right) = 0.79A$$

$$I_{Q_1 peak} = I_{L,p} + I_{L_2 p} = 1.5A + 0.79A = 2.29A$$

Feedback Resistors

$$R_2 = \frac{V_{ref}}{V_{out} - V_{ref}} \times R_1 = \frac{1.26V}{9V - 1.26V} \times 20k\Omega = 3.25k\Omega$$

sensing $$R_{SH} = \frac{130mV}{I_{Q_1 peak}} = \frac{130mV}{2.29A} = 56m\Omega$$

$$R_{FA} = (4.503 \times 10^{11})(100k\Omega)^{-1.26} = 226k\Omega$$

Compensation Network

$$f_{RHPZ} = \frac{(1-.655)^2 \times 9V}{2\pi \times 0.655 \times 33\mu H \times 0.5\times(.6A)}$$

$$= 26.3kHz$$

$$f_R = \frac{1}{2\pi\sqrt{33\mu H \cdot 47\mu F}} = 4kHz$$

$$f_c = \frac{4kHz}{6} = 673Hz$$

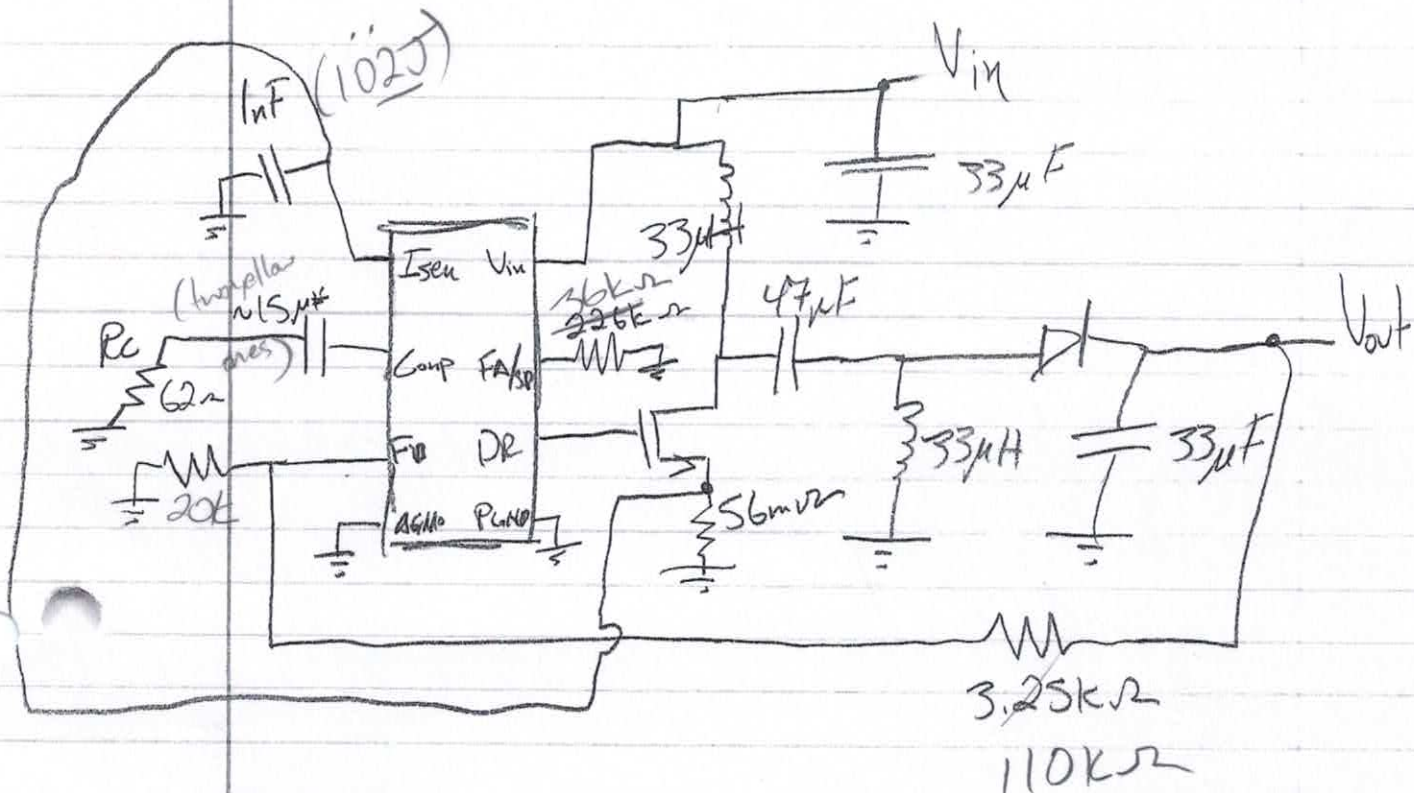
$$R_C = \frac{2\pi \times (673Hz)\times(33\mu F)\times(9V)^2\times(1+.655)}{(9V\times(800\mu)\times 1.26)\times(5V)\times(0.655)}$$

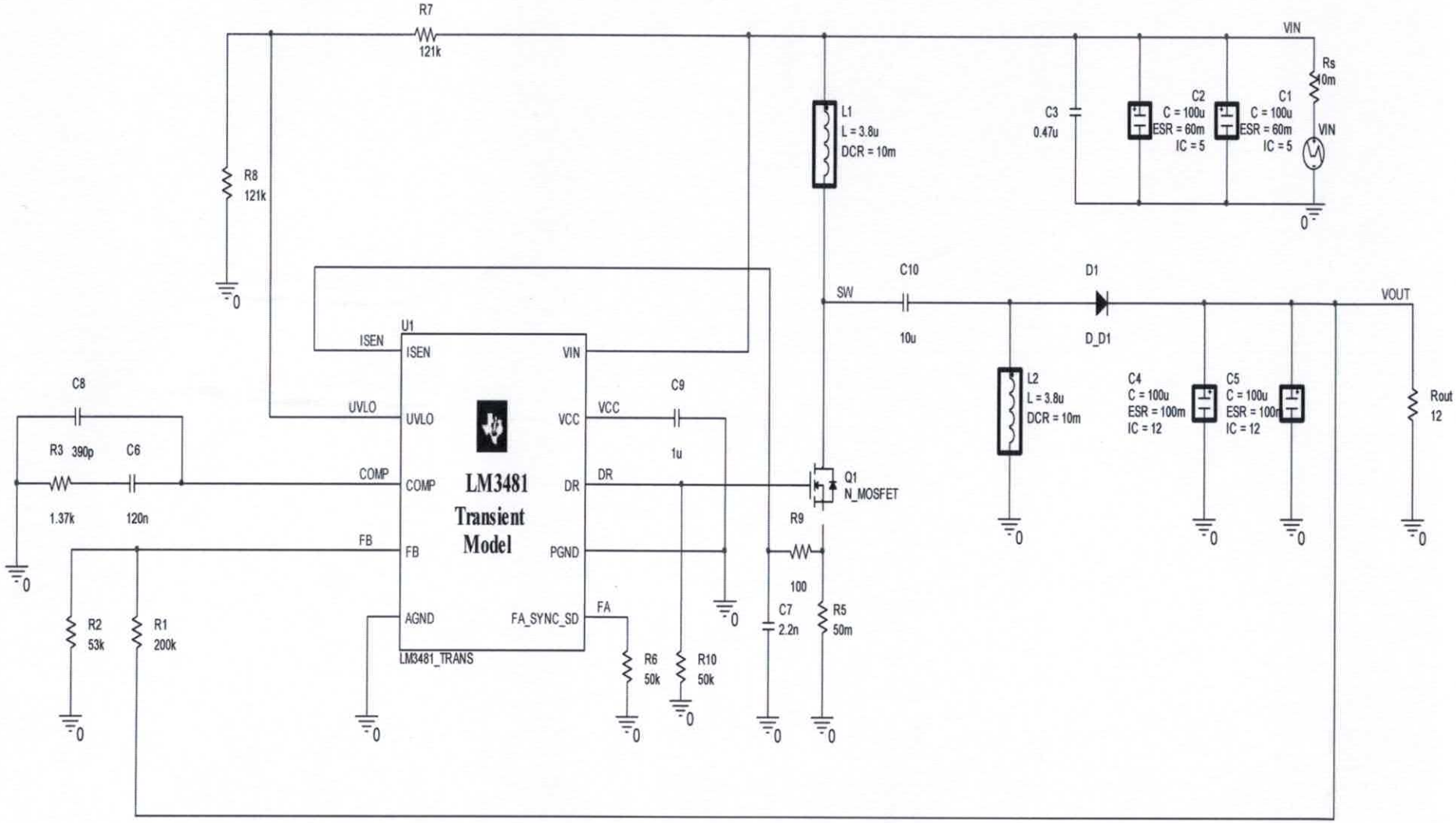
$$= 62\Omega$$

$$C_{C1} = \frac{4}{2\pi \times 673 \times R_C} = \frac{4}{2\pi(673Hz)(62\Omega)} = 15\mu F$$

$$C_{C2} = \frac{33\mu F \times 15m\Omega}{62\Omega} = 8pF$$

Schematic For SEPIC w/ LM3471




R7
121k
R8
121k
VIN
Rs
0m
L1
L = 3.8u
DCR = 10m
C3
0.47u
C2
C = 100u
ESR = 60m
IC = 5
C1
C = 100u
ESR = 60m
IC = 5
VIN
C10
10u
D1
D_D1
SW
VOUT
U1
ISEN
UVLO
COMP
FB
AGND
VIN
VCC
DR
PGND
FA_SYNC_SD
LM3481
Transient
Model
LM3481_TRANS
C8
R3 390p
C6
1.37k
120n
C9
1u
Q1
N_MOSFET
R9
100
C7
2.2n
R5
50m
FA
R6
50k
R10
50k
R2
53k
R1
200k
L2
L = 3.8u
DCR = 10m
C4
C = 100u
ESR = 100m
IC = 12
C5
C = 100u
ESR = 100m
IC = 12
Rout
12
0

1st

LM3481 Implementation

$$R_2 = \frac{V_{ref}}{V_{out} - V_{ref}} \times R_1 = \frac{1.275V}{6V - 1.275V} \cdot 20k\Omega = 5.4k\Omega$$

$$R_{SN} = \frac{160mV}{3A} = 53m\Omega$$

$V_{sense} = 160mV$
$V_{SL} = 90mV$

$$R_8 = \frac{1.43V}{I_{VALLO}}\left(1 + \frac{1.43V - 0.7}{V_{FM} - 1.43V}\right)$$

$R6 = R_{FA} = 45k\Omega$ For 400kHz

$R_1 + R_2$ (Feedback)

$$V_{out} = 1.275\left(1 + \frac{R_{F1}}{R_{F2}}\right)$$

$$\frac{6V}{1.275V} - 1 = \frac{R_{F1}}{R_{F2}} = 3.706$$

$$R_{SEN} = \frac{(V_{sense} - D) \times V_{SL}}{I_{SW,Peak}} = \frac{(160mV) - (0.25)(90mV)}{16A} = 8.5m\Omega$$

$V_{SL} = 90mV$
$V_{sense} = 160mV$
$D = 0.25$
$I_{SWPeak} = 16A$

2/9/15

1st test of SEPIC @ $V_{in} = 6.5 - 7.5V$

Output voltage: 1.5V

Ripple is either transient or ~1V @ 13 MHz

2/10/15

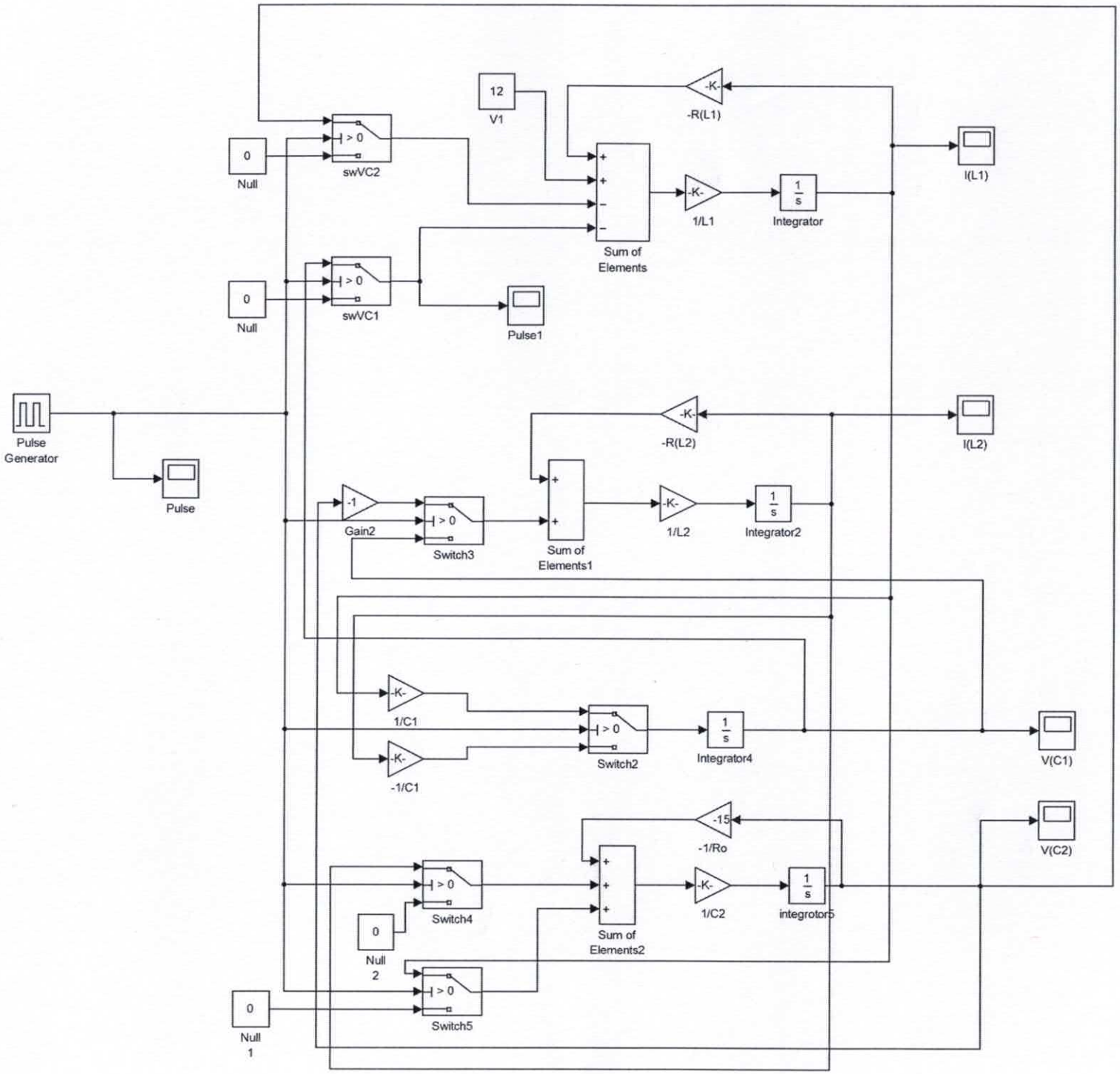
Output voltage @ 8.4V w/ $R_2 = 110k\Omega$

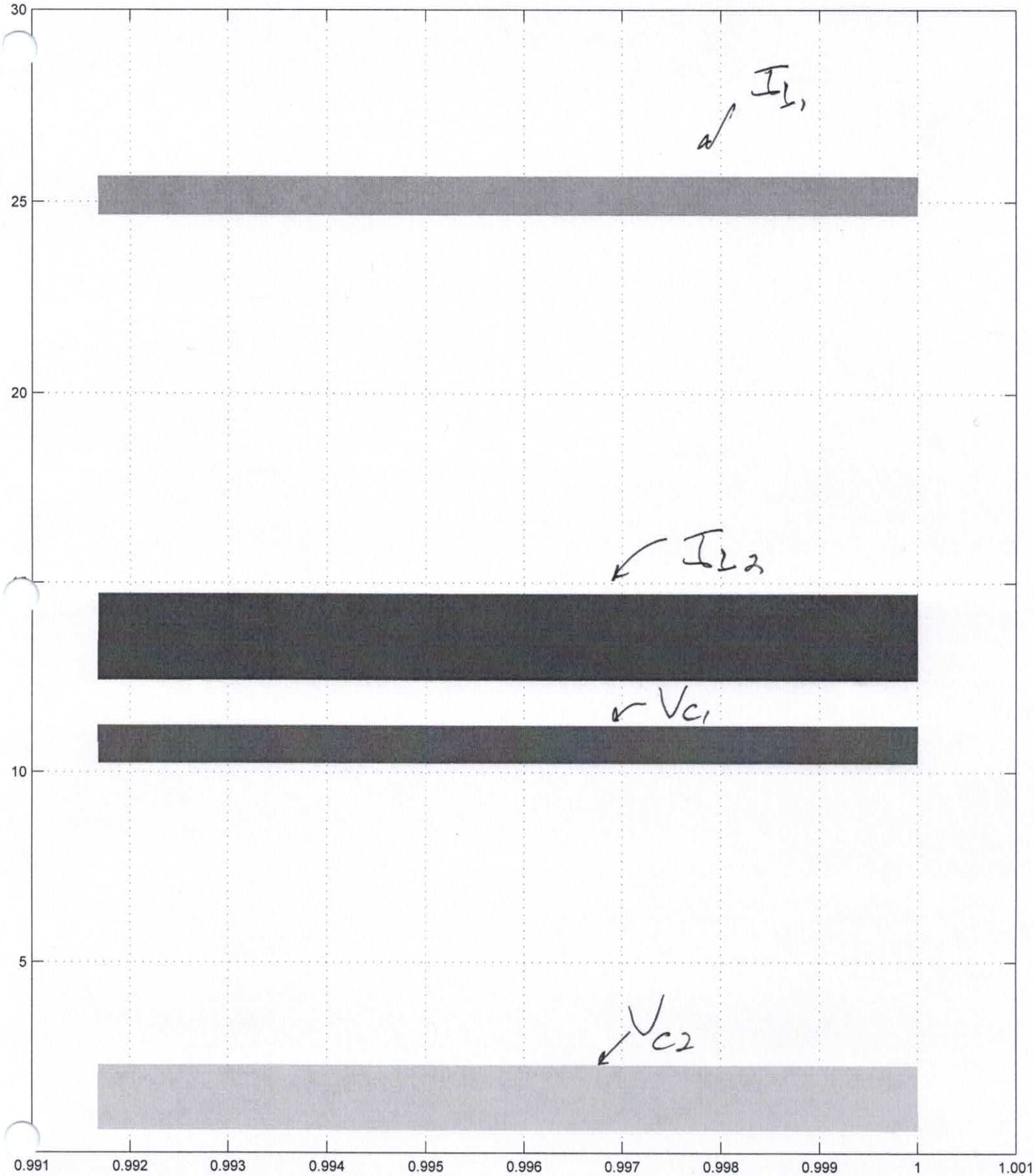
Observed Gate frequency of 12kHz

$(4.503 \times 10^{11})\{(12kHz)^{-1.26}\} = 226k\Omega$

$\frac{226k\Omega}{(12kHz)^{-1.26}} = 3.11 \times 10^{10}$

$(3.11 \times 10^{10})(100kHz)^{-1.26} = 15.6k\Omega$


12
V1
-K-
-R(L1)
I(L1)
0
Null
> 0
swVC2
Sum of
Elements
1/L1
Integrator
0
Null
swVC1
Pulse1
Pulse
Generator
Pulse
-K-
-R(L2)
I(L2)
-1
Gain2
Switch3
Sum of
Elements1
1/L2
Integrator2
-K-
1/C1
-K-
-1/C1
Switch2
Integrator4
V(C1)
-15
-1/Ro
V(C2)
Switch4
0
Null
2
Sum of
Elements2
1/C2
integrotor5
0
Null
1
Switch5



Time offset: 0

Ton

① $\frac{dI_{L_1}}{dt} = \frac{1}{L_1}\left(-R_{L_1} I_{L_1} + V_1\right)$

$I_{L_1} = \int \frac{1}{L_1}\left(-R_{L_1} I_{L_1} + V_1\right) dt$

② $\frac{dI_{L_2}}{dt} = \frac{1}{L_2}\left(-R_{L_2} I_{L_2} + V_{C_1}\right)$

$I_{L_2} = \int \frac{1}{L_2}\left(-R_{L_2} I_{L_2} + V_{C_1}\right)$

③ $V_{C_1} = \int \left(\frac{1}{C_1} I_{L_2}\right) dt$

④ $V_{C_2} = \int -\frac{1}{C_2 R_0} V_{C_2}\, dt$

Toff

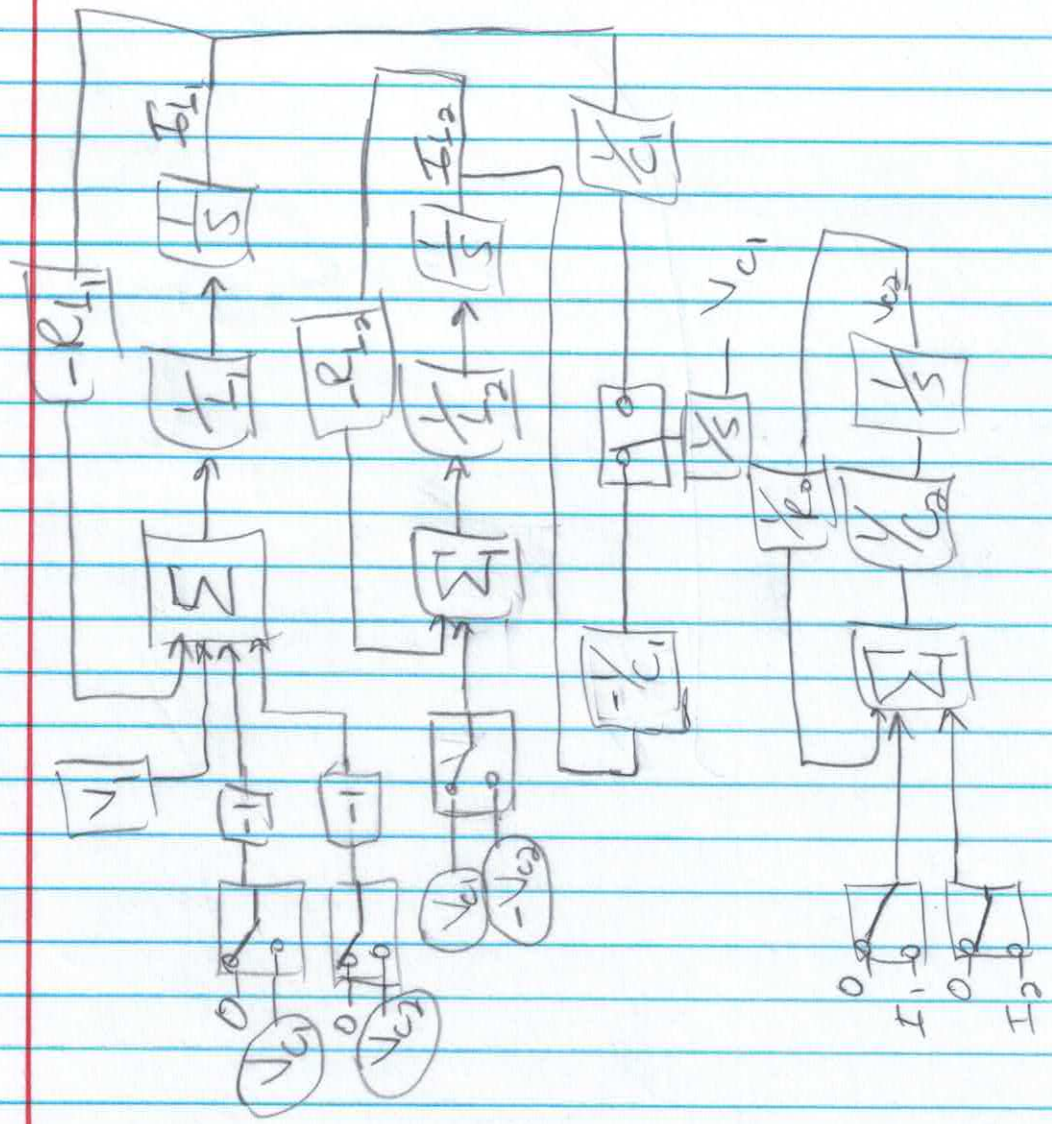
① $I_{L_1} = \int \frac{1}{L_1}\left[-R_{L_1} I_{L_1} - V_{C_1} - V_{C_2} + V_1\right] dt$

② $I_{L_2} = \int \frac{1}{L_2}\left[-R_{L_2} I_{L_2} - V_{C_2}\right] dt$

③ $V_{C_1} = \int \frac{1}{C_1} I_{L_1}\, dt$

④ $V_{C_2} = \int \frac{1}{C_2}\left[I_{L_1} + I_{L_2} - \frac{1}{R_0} V_{C_2}\right.$

State Space Simulation in Simulink.



SEPIC component design equations

① Equ 1

$$D = \frac{V_{out} + V_D}{V_{IN} + V_{out} + V_D} = \frac{6V + 0.3V}{12V + 6V + 0.3V} = 0.34$$

① Equ. 2

$$D_{max} = \frac{V_{out} + V_D}{V_{in(max)} + V_{out} + V_D} = \frac{6V + 0.3V}{6V + 0.3V + 2V} = 0.75$$

From AN-1484 (1) p.34 # Designing DC/DC converters based on SEPIC topology (2)

(2) $\Delta I_L = 30\% \times \frac{I_{IN}}{\eta}$ equ. 3

(1) $L_1 = L_2 = L = \frac{V_{in(min)}}{\Delta I_L \times f_{sw}} \times D_{max}$ $V_D = 0.5$

equ. 4

$V_{in(min)} = (\text{Operating Voltage of PV}) \times 10\% \approx 2V$

$D_{max} = 75\%$ $\eta = 90\%$ $I_{IN} = 1.35A$ (operating current)

$I_{out} = 3A$

$\Delta I_L = 30\% \times \frac{1.35A}{0.9} = 600mA$

$L = \frac{2V}{(600mA)(40kHz)} \times 0.75 = 62.5\mu H = L$

(1) $I_{L_1(peak)} = I_{out}\left(\frac{V_{out}+V_D}{V_{in(min)}}\right)\left(1+\frac{40\%}{2}\right)$

equ. 5

$= 3A\left[\frac{6V+0.3V}{2V}\right]\left[1+0.2\right] = 11.34A$

(1) $I_{L_2(peak)} = I_{out} \times \left(1+\frac{40\%}{2}\right) = 3A[1.2] = 3.6A$

equ. 6

(1) $I_{Q_1} = I_{L_1(peak} + I_{L_2(peak)} = 11.34A + 3.6A = 14.94A$

equ. 8

* reverse biased condition of diode

① $V_{RD} = V_{IN(Max)} + V_{out(MAX)} = 17.5V + 6V = 23.5V$

eqn. 11

* (coupling capacitor)

① $I_{CS(rms)} = I_{out}\sqrt{\frac{V_{out}+V_D}{V_{IN(min)}}} = 3A\sqrt{\frac{6V+0.3V}{2V}} = 5.3A$

eqn. 12

① $V_{CS(max)} = V_{IN(max)} = 17.5V$

$C_S =$

① $\Delta V_{CS} = \frac{(I_{out})(D_{max})}{C_S \times f_{SW}} =$

eqn. 13

① $I_{C_{out}(rms)} = I_{out}\sqrt{\frac{V_{out}+V_D}{V_{in(min)}}} = 3A\sqrt{\frac{6V+0.3V}{2V}} = 5.3A$

eqn. 14

① $ESR \leq \frac{V_{ripple} \times 0.5}{I_{L_1(peak)} + I_{L_2(peak)}} = \frac{600mV(0.5)}{14.94A} = 20m\Omega$

eqn. 15

① $C_{out} \geq \frac{I_{out} \times D}{V_{ripple} \times 0.5 \times f_{sw}} = \frac{3A \times 0.75}{600mV(0.5)(40kHz)} = 187.5\mu F$

eqn. 16

① $I_{C_{in(rms)}} = \frac{\Delta I_L}{\sqrt{12}} = \frac{600mA}{\sqrt{12}} = 173mA$

eqn. 17

$C_{in} = 10\mu F + ?$

SEPIC Converter Design Calculations

Caclulations based on AN-1484 "Designing a SEPIC Converter"

```
Vinmax = 18.2;
Iin = 1.1;
n=.9;
Iout = 3;
Vd = .3;
Vin = 17.5;
Vout = 6;
Cs = 10e-6;
Cin = 10e-6;
Vinmin= Vin*.1;
fsw = 400e3;
T = 1/fsw;
Vripple = 600e-3;
Voc=22;
Isc=1.21;

%Nominal and Max Duty Cycle
D = (Vout+Vd)/(Vin+Vout+Vd);
Dmax = (Vout+Vd)/(Vinmax+Vout+Vd);
%Current Ripple
Iripple = .3*(Iin/n);
%Inductor Size
L1 = (Vinmin/(Iripple*fsw))*Dmax;
L2 = L1;
L = L2;
%Max Inductor Current
IL1peak= Iout*((Vout+Vd)/(Vinmin))*(1+(.4/2));
IL2peak= Iout*(1 + .4/2);
%Max Transistor Current
Iq= IL1peak + IL2peak;
%Transistor Power Dissipation
% Pq = (Iqrms^2)*Rdson*Dmax+(Vinmin+Vout)*Iq*((Qgd*fsw)/Ig);
%Max Diode Voltage
Vrd = Vinmax + Vout;
%Max Coupling Capacitor Current and Voltage
Ics = Iout*sqrt((Vout+Vd)/Vin);
Vcs = Vinmax;
%Coupling Current Ripple
Vcsripple = (Iout*Dmax)/(Cs*fsw);
%Output Capacitor Requirments
ESR = (Vripple*.5)/(IL1peak+IL2peak);
Coutmin = (Iout*D)/(Vripple*.5*fsw);
%Max Input Capacitor Current
ICin = Iripple/sqrt(12);
%Shunt Resistance for PV
Rsh= Voc/Isc;
```

```
fsw
D
Dmax
Rsh
Iripple
L
L1
IL1peak
IL2peak
Iq
Vrd
Ics
Vcs
Vcsripple
ESR
Coutmin
ICin
```

```
fsw =

      400000

D =

    0.2647

Dmax =

    0.2571

Rsh =

   18.1818

Iripple =

    0.3667

L =

   3.0682e-06

L1 =
```

```
    3.0682e-06

ILlpeak =

   12.9600

IL2peak =

    3.6000

Iq =

   16.5600

Vrd =

   24.2000

Ics =

    1.8000

Vcs =

   18.2000

Vcsripple =

    0.1929

ESR =

    0.0181

Coutmin =

   6.6176e-06

ICin =

    0.1058
```