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Digital Systems for On-Site Collection for Water Quality Analysis

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DIGITAL SYSTEMS FOR ON-SITE DATA COLLECTION FOR WATER QUALITY ANALYSIS

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ABSTRACT

DIGITAL SYSTEMS FOR ON-SITE DATA COLLECTIONS FOR WATER QUALITY ANALYSIS

A prototype system has been developed for recording and transmitting digital data at a remote water quality monitoring station in an unattended manner. As many as eight analog signals from transducers, which measure water quality characteristics such as dissolved oxygen, temperature, pH, chlorides, conductivity, redox, and turbidity, are converted to digital signals and recorded in binary coded decimal format on magnetic tape. This unit may be contacted from a central station for playback of the day's recording. The transmitted data can be recorded at the central station by teletype.

Each data record includes a time-of-day "word" so that all data is identifiable. The techniques developed during this contract period have possible application in many areas of water resource research, particularly for use in making water quality measurements in remote areas or at numerous sites reporting to one central station.

ACKNOWLEDGEMENT

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This research was performed, under the supervision of M. K. Testerman, Principal Investigator, by:

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I. SUMMARY OF RESEARCH PERFORMED

This report describes the design and construction of a device for recording and transmitting data from transducers which measure water quality especially at unattended locations. The monitor has the capability of recording water quality information and presenting this information on command. For the purposes of this investigation, it is assumed that line power and telephone facilities are available at the monitor site. The scope of the investigation includes the design and construction of a bread-board monitor and some central processor equipment. It does not include transducers, transducer signal conditioning, or data reduction techniques. Figure 1 is a view of the monitor which has been constructed.

A. Design Objectives

The function of the system is to monitor water quality parameters at a remote unattended site for periods of up to 30 days. This necessitates a system design which has a high degree of inherent reliability.

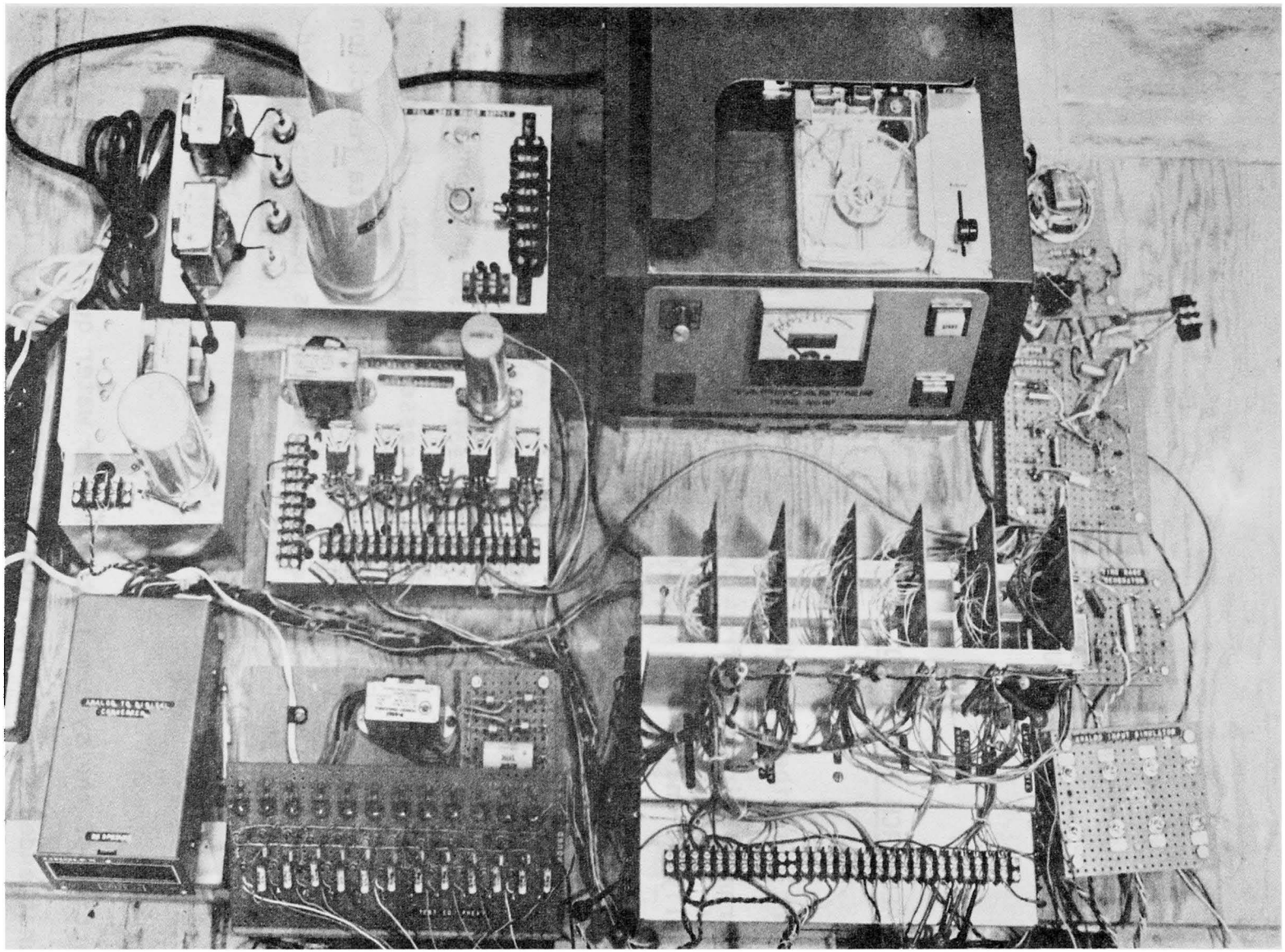


Figure 1

Overall View of Water Quality Monitor

To achieve this reliability, integrated circuits and other solid state circuits were used extensively. The number of moving parts was kept to a minimum consistent with economy and other objectives.

A preliminary investigation based on information obtained from the Arkansas Pollution Control Commission has shown that a realistic system for use in this state should consist of approximately sixty remote monitor points throughout the state and one central processor.[1] Almost all of these points are sufficiently near roads along which electrical and telephone facilities would be available.

In view of the fact that there would be sixty field units and one central processor, it is obvious that the minimum system cost will be affected primarily by the cost of the field units. With this in mind, the system was designed for minimum cost of field units, even at the expense of making the central processor more complex than would be the case in normal design procedure.

B. Additional Advantages

In the event central system interrogation is not desired, the same field system can be used to record on-site data for manual pickup and subsequent processing. The tape cartridge will hold enough tape for one hour of playback time. Since a record of eight variables including time of recording occupies only 3½ seconds of playback time, hourly recordings could be taken for as much as 40 days on a single cartridge of tape. The only changes required would be moving one connection in the command wiring to generate hourly commands, and the insertion of the cartridge with larger

tape capacity.

It is anticipated that the wide area dialing service would be used during off-peak hours to collect the information from all the stations. Consequently, cost of data transmission would not be prohibitive. In the event of severe weather disturbances or other unusual conditions, any station may be interrogated at any time. The information available will be the information collected since the last interrogation command was received. An additional benefit is obtained if daily readings are available, since failure of transducers or measuring equipment will be quickly detected, so that maintenance measures may be instituted.

C. Functional Description of the Monitor

Functionally, the monitor consists of nine parts (see Figure 2). The outputs of various water quality transducers are fed into the analog multiplex switch which sequentially transfers one input at a time into the analog-to-digital (A to D) converter.

The A to D converter chosen for this system is a digital panel meter. This device converts analog input voltages to a binary-coded-decimal (BCD) output on command. The numeric display of the analog value of voltage is actually unnecessary for A to D conversion and the conversions occur too rapidly for reading of the individual values. However, the cost of the device is less than that for most A to D converters without a display. Also, the display function is quite useful for trouble-shooting. A digital panel meter was chosen for temperature stability,

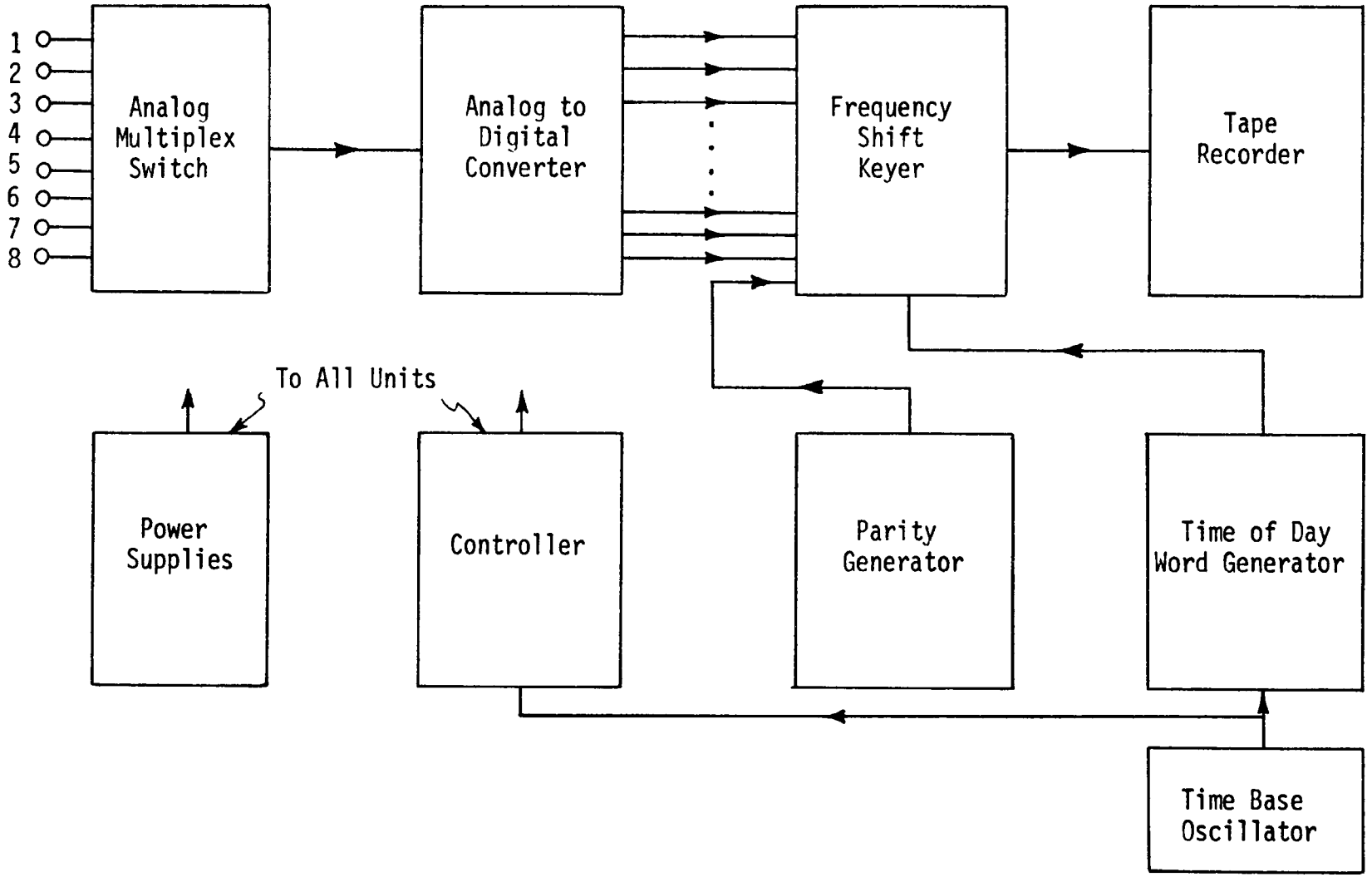


Figure 2

Monitor Block Diagram

availability, and its ability to make conversions on external command. The primary disadvantage of the digital panel meter for this application is that the digital BCD outputs are in parallel form.

Parallel output means that the output (consisting of bits) is on 16 lines, each line representing one bit in the digital word format (see Figure 3). For this application it is necessary for the digital information to be in serial form. The serialization is accomplished in the frequency-shift-keying (FSK) circuitry.

The frequency shift keyer in this system performs two separate functions. First, the information from the A to D converter is serialized by a commutation process which is similar to the analog multiplexing of the inputs; that is, the parallel outputs of the A to D converter are sequentially switched to a common line to form a serial equivalent of the parallel inputs. The second function of the FSK circuitry is taking the serial train of digital "1's" and "0's" and converting them into two tones; 2300 Hz for a "1" and 2000 Hz for a "0". The output of the frequency shift keyer then is a series of two tones which can be recorded by a magnetic tape recorder.

The recorder incorporated into the system for digital information storage is of the type designed for commercial broadcasting. It is an endless loop cartridge type which can record on a single track for any period of time up to 1 hour. It is completely electrically controlled; that is, the start, stop, record and playback command are electrical signals. The unique feature of this recorder is that the second track is used to identify the position of the tape. In this application, the second

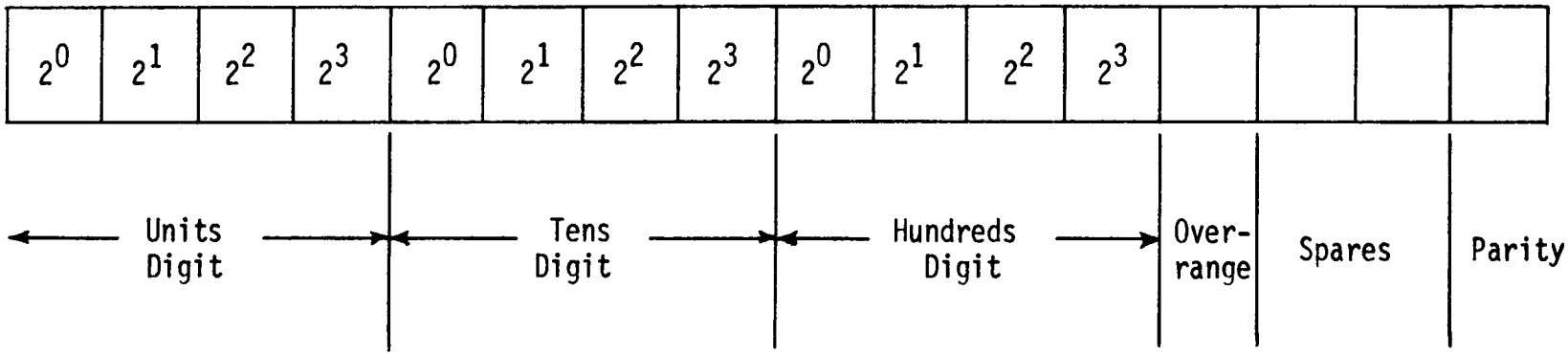


Figure 3

Digital Word Format

track marks the beginning of the recorded material. Upon command the recorded material is played once and the machine stops. Repeated interrogation is possible if desired.

Each group of eight readings and the time of day take approximately 2 seconds of recording time so that slightly over 3 minutes of tape records 1 day's data taken four times each hour. When played back, this data rate is compatible with low cost telephone circuits.

After each water quality reading has been recorded on the tape, the time of day is also recorded in digital manner. The time of day "word" is multiplexed into the frequency shift keyer in the same way as the data "word". The time of day generator consists of an integrated circuit frequency divider which has the output of the time base oscillator as an input. After successive binary divisions, the time of day is registered as a 16-bit binary word. The least significant bit is indicative of a 15 minute time period and the period of the most significant bit is 8192 hours (almost one year).

A highly stable time base oscillator serves as the input to the time of day generator as well as providing synchronization information to all of the control functions for the field unit. The oscillator is a Colpitts type utilizing a quartz crystal resonator operating at a frequency of 149.131 kHz. The oscillator operates from a separately regulated power supply for maximum frequency stability.

A parity generator is incorporated in the monitor as an error detection device. When digital information is transferred in a system such as

the monitor, there is a probability that an error will be made. With digital information in BCD format, the only error possible is the interchange of a "1" and a "0".

Since the probability of this error is small, then the probability of two such errors in one digital word is extremely small. In the monitor, the parity generator supplies an additional bit to the word if the original word has an even number of "1's" unless an error has been made in transmission, storage, or processing of the information. A choice can be made between odd parity or even parity. Odd parity was chosen so that a distinction can be made between a word which is all "0's" and a word which is "no information".

In Figure 4, the block labeled "control logic" represents the most complex section of the monitor. The control logic supplies all of the control signals for the other parts of the monitor. The function of the control circuitry is best described with the aid of timing charts. Table 1 describes the commands given during the record phase and Table 2 describes the playback sequence.

The monitor requires 115 volts AC 60-cycle power for operation. During the record and playback operations, tape recorder motor on, the power consumption is approximately 100 watts. The idle power is much less. The allowed temperature range of the solid state components used is from $0^{o}C$ to $70^{o}C$. The A to D converter, however, must be within a 20 degree range of ambient for rated accuracy. This could be accomplished with a simple oven arrangement if wide temperature ranges were encountered.

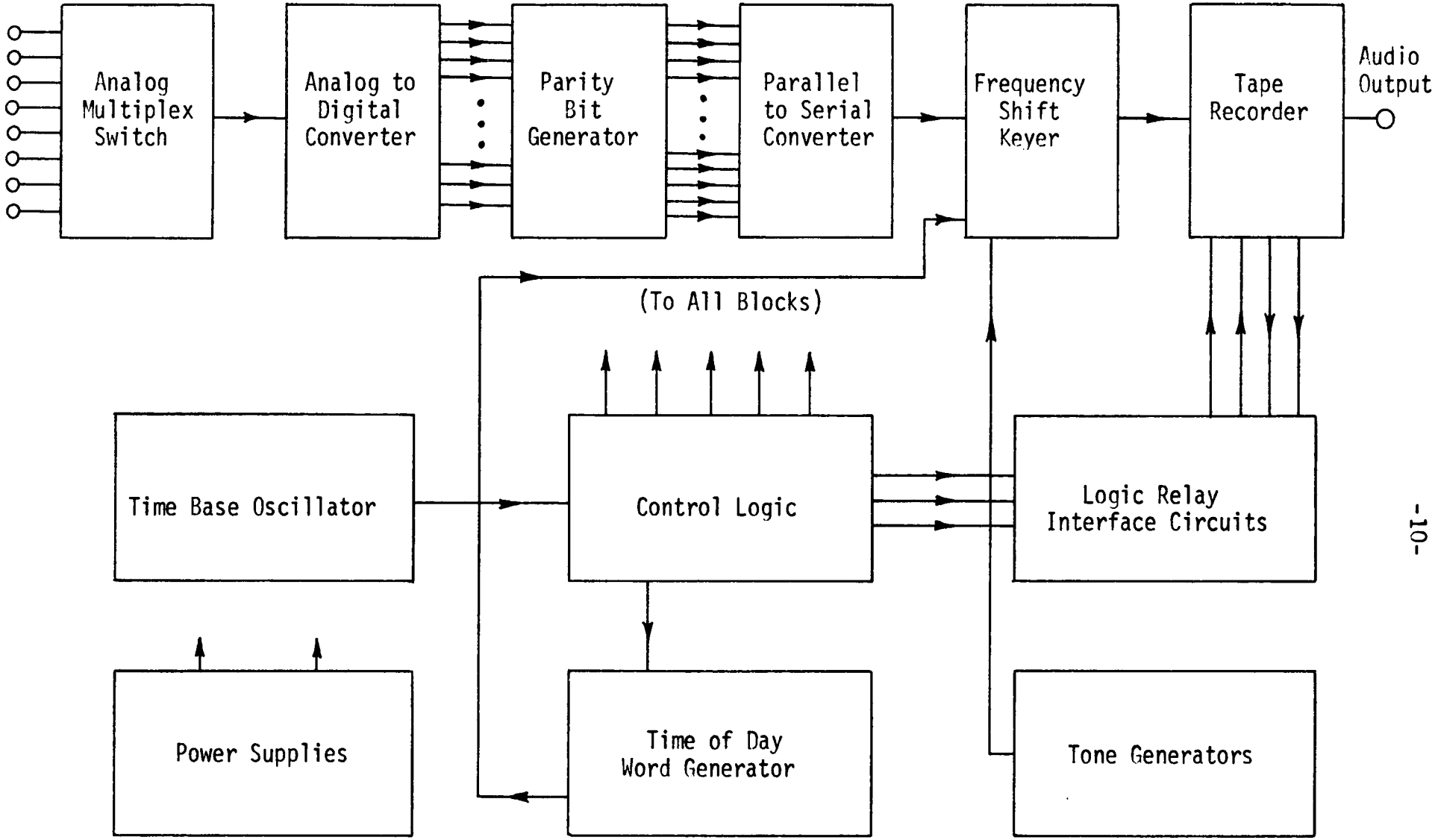


Figure 4

Electrical Block Diagram

Table 1

Timing Diagram - Record Sequence

A. Turn on recorder motor and electronics.

B. Engage recorder clutch (start tape).

C. Turn on analog input number 1.

D. Supply conversion command to the D to A converter.

E. Commutate the output of the D to A converter through the FSK.

F. Commutate the "time-of-day" word through the FSK.

G. Switch off input number 1 and turn on input number 2.

H. Supply conversion command to the A to D converter.

..

..

.. (repeat this sequence through all eight analog channels)

..

..

W. ......

X. ......

Y. Disengage recorder clutch (stop tape).

Z. Turn off recorder motor and electronics.

This sequence is repeated every 15 minutes and takes 3.516 seconds.

Table 2

Timing Diagram - Playback Sequence

A. Switch recorder from record mode to playback mode.

B. Turn on recorder motor and electronics.

C. Engage recorder clutch.

D. Advance the tape to the beginning of the recorded material.

E. Turn on audio output from the tape recorder.

F. Play the entire tape once.

G. Stop the tape (disengage clutch) at the end of the material.

H. Turn off recorder motor and electronics.

I. Switch the recorder back into the record mode.

This sequence is initiated after the reception of the playback command.

The effects, if any, of temperature extremes on the tape transport have not been established. A finalized design for the field unit would probably have all of the equipment contained in a moisture proof case with a thermostatically controlled heater for low temperature operation.

II. DESIGN AND DEVELOPMENT OF MONITOR HARDWARE

Since the beginning of the contract period, several advances in certain areas have occurred which would have a pronounced effect on design if the project were started at the time of this writing. Also, the cost of performing certain functions would be reduced as state-of-the-art concepts were incorporated. For example, new lost cost cassette digital tape recorders are now available which would permit direct digital recording at a reasonable cost. One could also use a new integrated circuit modem after the digital recorder for frequency-shift-keying.

The design objectives stated in the summary eliminated the use of exotic hardware because of cost considerations. The reliability and, particularly, the availability of such hardware over a period of time is also an important consideration. The resultant design was thus a compromise of many factors. All of the components used in the monitor are available as off-the-shelf items and at reasonable prices.

Figure 4 is an electrical block diagram of the monitor which defines the unit in parts that can be physically identified rather than as functional blocks. Detailed discussions of each item in the diagram are presented in the remainder of this report.

A. Analog Multiplex Switching

The first operation performed on the input signals is the sequential switching of the inputs to the analog-to-digital converter. It is assumed

that the analog information on the inputs will be continuously available during the measurement period. The general electrical requirements of this switching function are:

1. A low "on" resistance
2. A high "off" resistance
3. A minimum voltage offset through the switch
4. Negligible circuit loading (resistance to ground high).

There are a number of practical methods of performing this switching function. The advantages and disadvantages of each method are discussed below.

With a multiple relay technique, each channel of information would be gated to the A to D converter when the relay for that channel is energized. If this method had been chosen, mercury wetted reed relays would have been used because of their low "on" resistance, high "off" resistance, and ability to function reliably under the dry switching conditions of the circuit. The major disadvantages of this method are that each relay would need an electrical driver stage and the eight drivers would have to be operated from some additional decoding logic circuits to obtain the desired sequential switching.

To eliminate the need for decoding logic, a stepping relay was considered. This device will switch from one channel to the next by the application of a current pulse to a single relay coil. In this case, only one driver stage would be needed and the control logic could be greatly simplified. This technique was not chosen for the final design because of the many disadvantages of electromechanical devices in uncontrolled environments. Another disadvantage is that the operating logic does not indi-

cate the active channel so an ambiguity could arise if the stepping relay missed a command.

There are several good solid state switching techniques. A conventional junction transistor is a good switching device except that the collector-to-emitter voltage (across the switch) is not zero and worse, it is temperature dependent. If this potential were constant, its effect could be eliminated by calibration; but since it is a function of temperature, compensation networks would be required. This system rapidly becomes impractical.

A MOS (Metal-Oxide-Silicon) transistor has no inherent offset potential between the drain and source when the device is turned on. By using a MOS device, the offset problem is eliminated but the "on" resistance is higher than that of a junction transistor. The relatively high "on" resistance of the switch is not a serious problem in this application because the input impedance of the A to D converter is sufficiently high to prevent a significant voltage drop across the switch. However, the drive requirements for a MOS switch are almost as complex as that required for a relay. An independent negative supply voltage is required for proper biasing of field effect transistors and at least one stage of amplification for the 5-volt control logic would be needed in addition to the decoding logic.

The method chosen for analog multiplexing of inputs utilizes a Fairchild MOS Monolithic 8-Channel Multiplex Switch type 3705 (Fairchild Semiconductor, Mountain View, California). The 3705 is an 8-channel multiplex switch with the output enable control and one-of-eight decoder included on the chip. It is a monolithic integrated circuit utilizing

P-channel enhancement mode MOS technology. The logic input lines are directly compatible with the DTL (Diode Transistor Logic) used in the control circuitry without any level-shifting interface circuits. The only special requirement of the device is an isolated negative 20-volt supply.

The actual electrical circuit of the 3705 is quite complex and can be found in the Fairchild literature. A logic diagram is given in Figure 5 and a truth table in Figure 6. Notice in the truth table that the three control inputs (2_0, 2_1, and 2_3) go through a binary counting sequence. If these three lines are connected to a three stage binary counter, the decoder will select one input at a time through the eight inputs, provided the output enable (OE) line is in the high state. The control section of the monitor contains a three stage counter for this device and is described in detail in another section of the report.

The availability of 3705 made the difficult task of analog multiplex switching quite easy. At the time of construction, these devices were quite new on the market and somewhat expensive, but no more expensive than other means of doing the same job.

B. Analog To Digital Conversion

The selection of a method for analog to digital conversion for the monitor proved a greater problem than anticipated. It was found early in the investigation that no suitable A to D converters as such were available for this application. It was therefore necessary to design

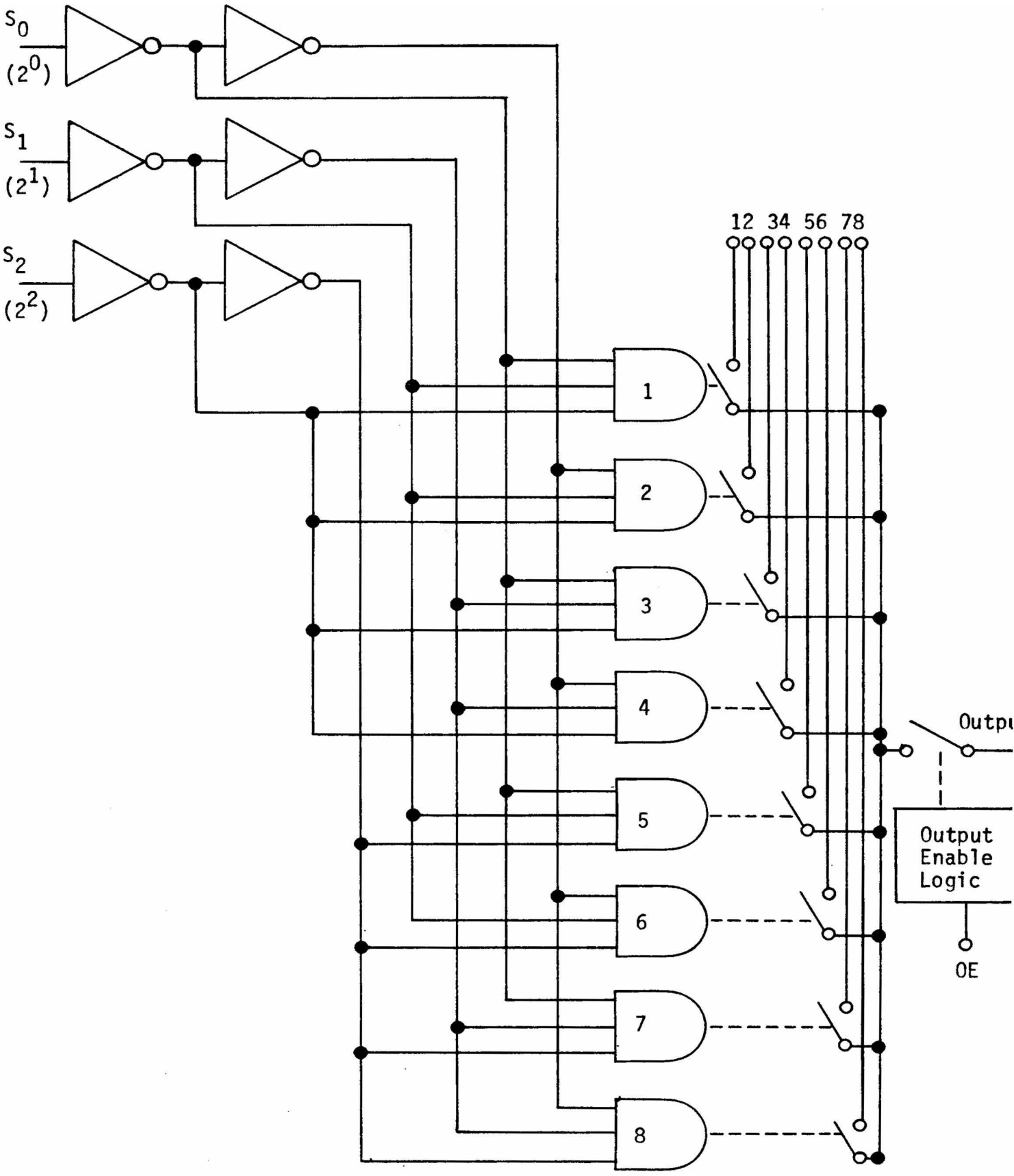


Figure 5

Logic Diagram of 3705 and 9312 Multiplex Switches

Logic Inputs				
2^2	2^1	2^0	OE	Channel "On"
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8
X	X	X	0	All Off

X = Does not affect output

Figure 6

Truth Table of 3705 and 9312 Multiplex Switches

and build an appropriate converter or to find a suitable substitute. The requirements for the A to D converter can be summarized as follows:

1. 3 digit accuracy and resolution (0.1%)
2. Capable of making a conversion on external command
3. Accuracy unaffected by changes in environment temperature
4. Output compatible with the DTL used in the system
5. Reasonable cost.

There are many commercially available A to D converters which fulfill all of the above requirements except the last. For most applications, high speed, high resolution and accuracy are necessary but in the monitor system these qualities are unnecessary. At the present time, there are many more low cost converter components available which would make the construction of an A to D converter more practical. In particular, low cost thick film ladder networks and voltage references are available which, in conjunction with a comparator, compromise a basic A to D converter. This component approach allows one to tailor the converter to the application with fewer compromises than with a purchased sub-system.

During the design phase of the monitor development the choice of a practical A to D converter was more limited and resulted in the purchase of a digital panel meter (DPM) which contains an A to D converter. The unit purchased was a Gralex Model DM-31A Digital Panel Meter (Gralex Industries Inc., Copiague, New York). This unit is a 3 1/2 digit (1.500 volt) model and has a stated accuracy of 0.1% at room temperature. Some other pertinent specifications include: a 16 2/3 millisecond conversion time, conversion on external command, and binary coded decimal (BCD)

output compatible with the diode-transistor-logic (DTL) used in the rest of the monitor system. A complete functional description of the DPM can be found in Appendix I. The only compromise involved in the use of the DPM in the monitor is that the electrical BCD output is in parallel form; that is, there is one connection for each bit of information. In this application it is necessary to serialize the information for storage on the magnetic tape. The display part of the DPM is unnecessary for operation but has proven to be quite valuable for calibration and trouble-snooting.

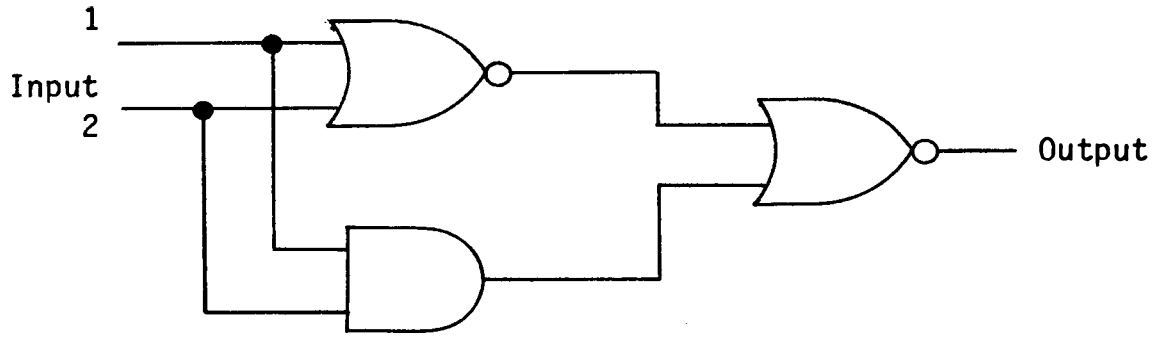
C. Parity Bit Generation

Errors in the storage and transmission of digital information can be far more serious than analog errors, particularly when the information is processed before evaluation. To protect against digital errors, a parity bit generator was designed, built, and installed in the monitor. The only error possible in a binary word is the interchange of "0" and "1". If the probability of one of these errors is small, the probability of two errors in the same word is very small. A single error will cause the number of "1's" to change from an odd to an even number or vice versa. The parity generator supplies a "1" or a "0" to the word to make the word always contain an odd number of "1's". This is odd parity. Examination of each word will indicate if a single error has been made. Odd parity was chosen so that a digital word of all "0's" will have a parity bit "1" to distinguish it from "no information". The parity generator in the monitor takes the entire word in parallel form from the A to D converter and

generates a "1" or a "0" on the output line depending on whether the number of "1's" in the word is even or odd. Figure 7 is the functional logic diagram for the Exclusive OR gate used along with the truth table for the gate. Figure 8 is the logic diagram for the parity tree used by the monitor. The Exclusive OR gates used in the monitor are integrated circuits which have four gates per package. They are Motorola MDTL MC1812P devices and are available from Motorola Semiconductor Products Inc., Phoenix, Arizona.

D. Parallel To Serial Conversion

When the parity bit has been added to the output of the A to D converter, the entire word is serialized so that the information can be processed by the Frequency Shift Keyer (FSK). The problem of serialization of the digital information is much the same as the multiplexing of the analog inputs. In this case there are sixteen lines which must be commutated or switched in sequence. A device is available from Fairchild Semiconductor which performs the same function as the analog multiplex switch and has the same truth table. The only difference is that the Digital Multiplexer can only accept digital information for transmission through the device. The device is known as an 8-Input Digital Multiplexer type 9312. Two of these devices are used since sixteen lines must be commutated. Commands for the control of the multiplexer are generated by the control logic. The reader is referred to Figures 5 and 6 for a logic diagram and truth table for the 9312 multiplex switch since they are the same as the analog multiplex switch. The identical technique is used in



Inputs		
1	2	Output
0	0	0
0	1	1
1	0	1
1	1	0

Figure 7

Logic Diagram and Truth Table for Exclusive OR Gate

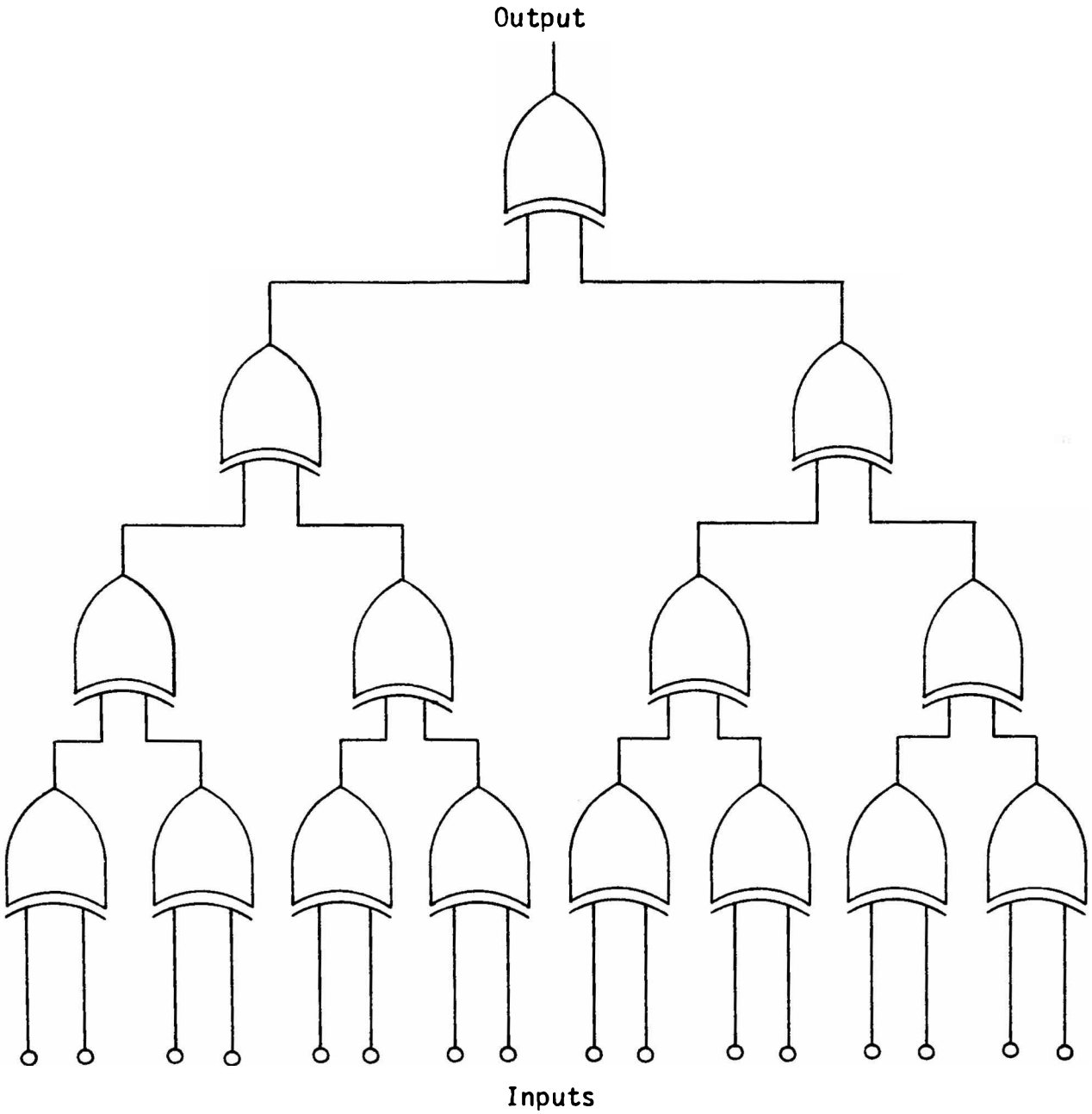


Figure 8

Parity Tree Logic Diagram

the time-of-day information. The time-of-day word generation is discussed in the section on clock functions.

E. Frequency Shift Keying

At a point just after the digital multiplex switches in the monitor, the measured variables and the time of day appear in serial form. The tape recorder used in the monitor is not capable of recording digital information directly and it is not desirable to transmit digital logic levels over communications circuits. The function of the Frequency Shift Keyer (FSK) is to change the digital information to a form more compatible with the recorder and the telephone circuits. The frequency shift keyer has three inputs. The logic input accepts the 0 and 5 volt logic levels from the digital multiplex switches. The other two inputs accept two continuously supplied AC voltages or tones. The two tones, one for the logical "0" and the other for the logical "1", are supplied by two frequency stable unijunction oscillators (see Figure 9). The frequencies of these two oscillators are adjustable and arbitrarily set at 2.0 and 2.3 kHz. The outputs of these oscillators are gated to the input of the recorder as the logical "0's" and "1's" appear at the input of the FSK. In other words, the output of the FSK is 2.0 kHz if a "0" is on the logic input line and 2.3 kHz if a "1" is on the line. A logic diagram of the FSK appears in Figure 10. The Nand gates used are contained in one Motorola Type MC846P Quadruple Two Input Gate.

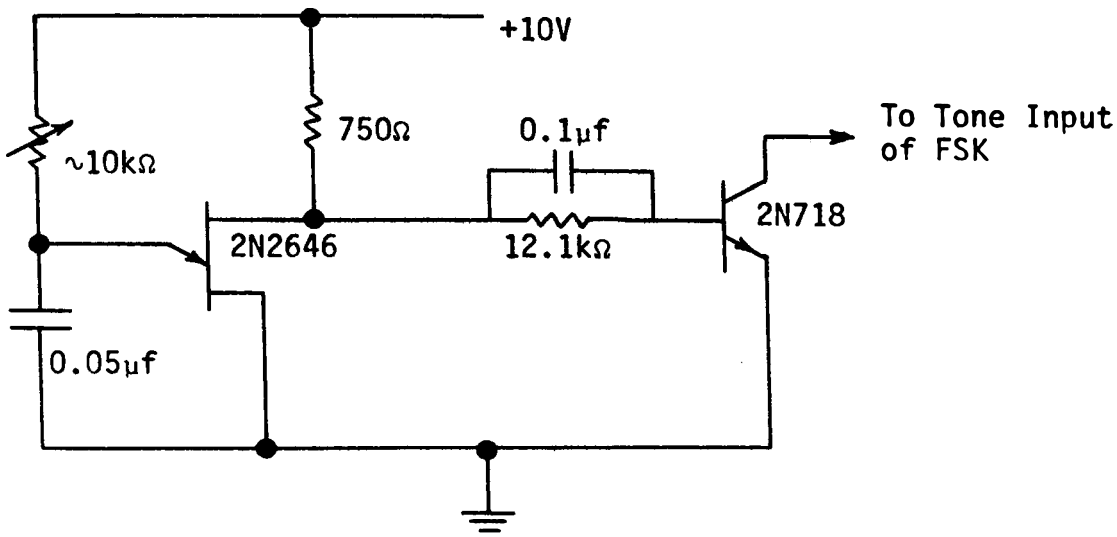


Figure 9

Diagram of Oscillators for FSK (Two Used)

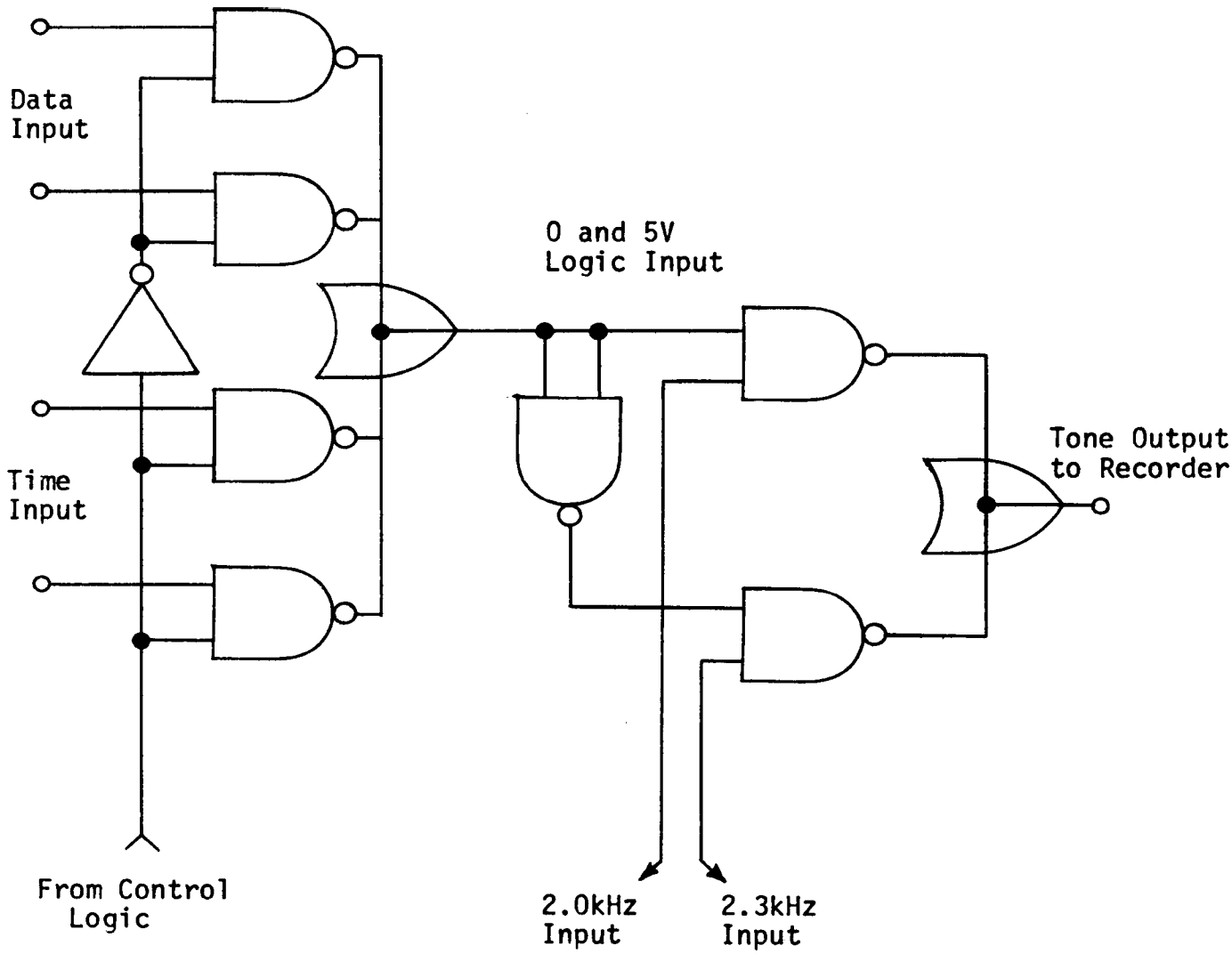


Figure 10

Logic Diagram of FSK

F. Tape Recorder

The tape recorder used to store information in the monitor was selected as a compromise between the very expensive digital instrumentation recorders and low cost home entertainment types. The recorder selected is a Model 700-RP cartridge tape recorder manufactured by Tapecaster Corporation of Rockville, Maryland. This is a commercial grade machine intended for use by broadcasters for spot announcements. The recorder is an endless loop cartridge type which can record on one channel for periods of up to 1 hour. The control of the recorder is completely electrical; that is, the start, stop, record and play commands are electrical switching functions and not manual mechanical operations. The unique feature of this recorder is that a second track on the tape is used to identify the beginning of the tape, which is an arbitrary point since the tape is an endless loop.

The recorder was originally designed to play random length announcements and stop at the end of each one. The stop signal is derived from a tone burst on the control channel at the very beginning of each section of recorded material. This built-in logic is not desired in the monitor application so some minor modifications were made. The modifications consisted mostly of defeating the built-in logic and the bringing out of all pertinent control lines for manipulation by the control logic section of the monitor. A controlled erase bias oscillator and an erase head were also added. The points in the circuits brought to external terminations are:

1. Audio input } Information channel
2. Audio output }
3. Tone marker control } Control channel
4. Relay contacts of tone identification circuit }
5. Motor power control
6. Clutch control
7. Playback enable
8. Record enable
9. Erase oscillator enable.

The tape recorder was preserved as a self-contained unit. All power supplies are inside the recorder case and the entire unit can be removed from the monitor by disconnecting four plug-in cables. In actual field service this would be a highly desirable feature since the majority of the moving parts of the monitor are in the tape recorder. This, therefore, eliminates the need for field servicing of the recorder if spares were kept on hand. Complete schematics showing modifications of the tape recorder are given in Figure 11.

G. Time Base Oscillator

A time base oscillator has been incorporated in the monitor for two purposes. First, the time-of-day word generator requires a frequency-stable train of pulses for operation and second, the control requires a pulse train for the synchronization of the monitor control functions. The time base oscillator constructed for this application is a quartz crystal resonator with appropriate circuits for drive and interface with the Diode

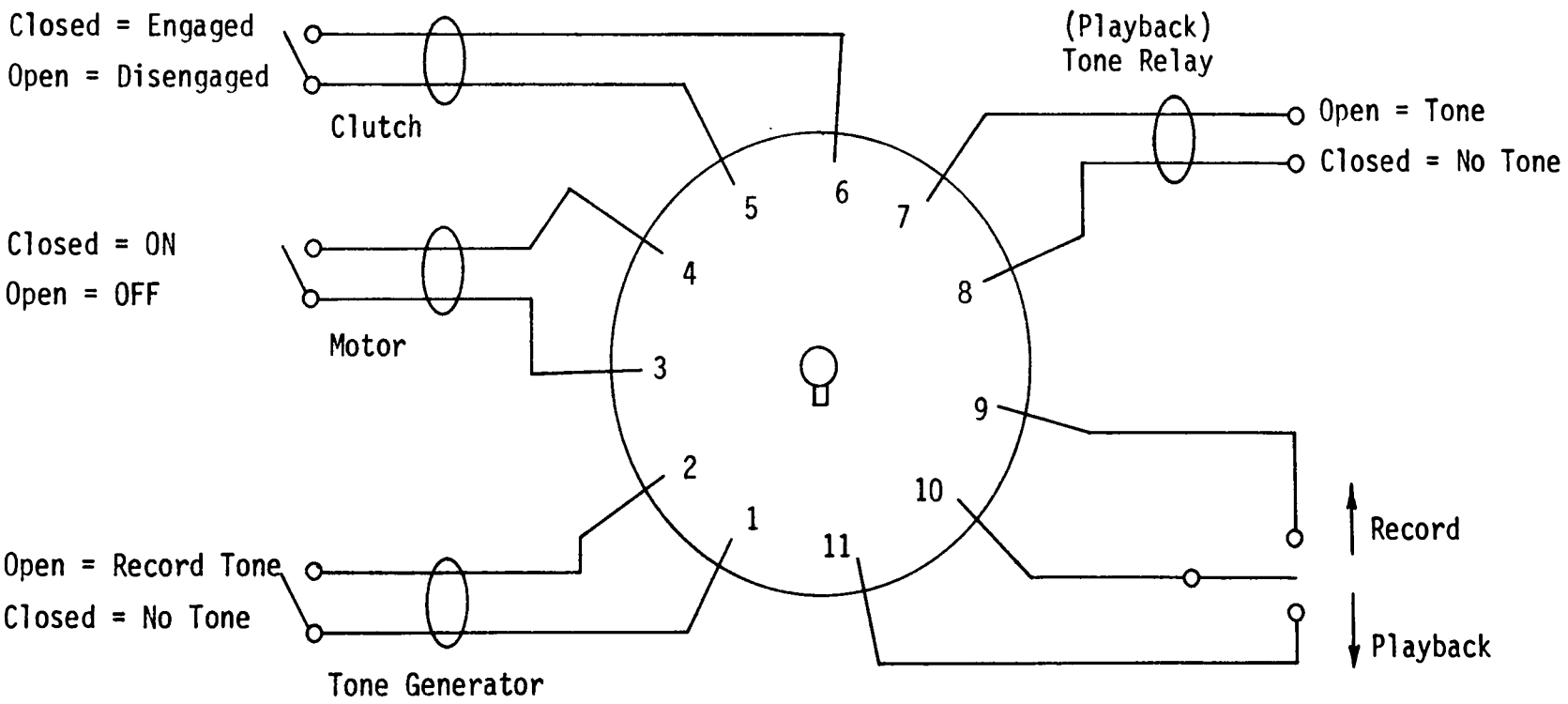


Figure 11

Tape Recorder Control Modification

Transistor Logic used in the monitor. The oscillator is a Colpitts type operating at a frequency of 149.131 kHz which is an even multiple of 1 cycle per minute. The oscillator is operated from its own temperature-compensated voltage regulator to insure good frequency stability. The output stage is an amplifier which serves to decouple the oscillator from the load. Figure 12 is a schematic of the oscillator.

In actual field use, it would probably be desirable to operate the oscillator in a temperature controlled environment or else re-design the oscillator with some form of temperature compensation, since the frequency of resonance of the crystal is somewhat temperature dependent. Also, in field use it might be desirable to operate the oscillator and the time-of-day circuits from a power supply which is not dependent on outside power for operation. This would insure against the loss of time-of-day if the source of outside power should fail.

As stated above, the output of the oscillator is 149.131 kHz. The highest frequency used by the control logic is 36.4089 Hz. This lower frequency is obtained by the division of the high frequency output of the oscillator by a factor of 16, three consecutive times. Division by 16 is accomplished in a Motorola MC839P integrated circuit. Within the integrated circuit the division is performed by dividing by two in four J-K flip-flops. Further frequency division is performed by Motorola MC853P dual flip-flops operated within a period of 15 minutes which is the recording interval for which the monitor is presently set. The recording interval is easily adjusted by a multiple or submultiple of 15 minutes.

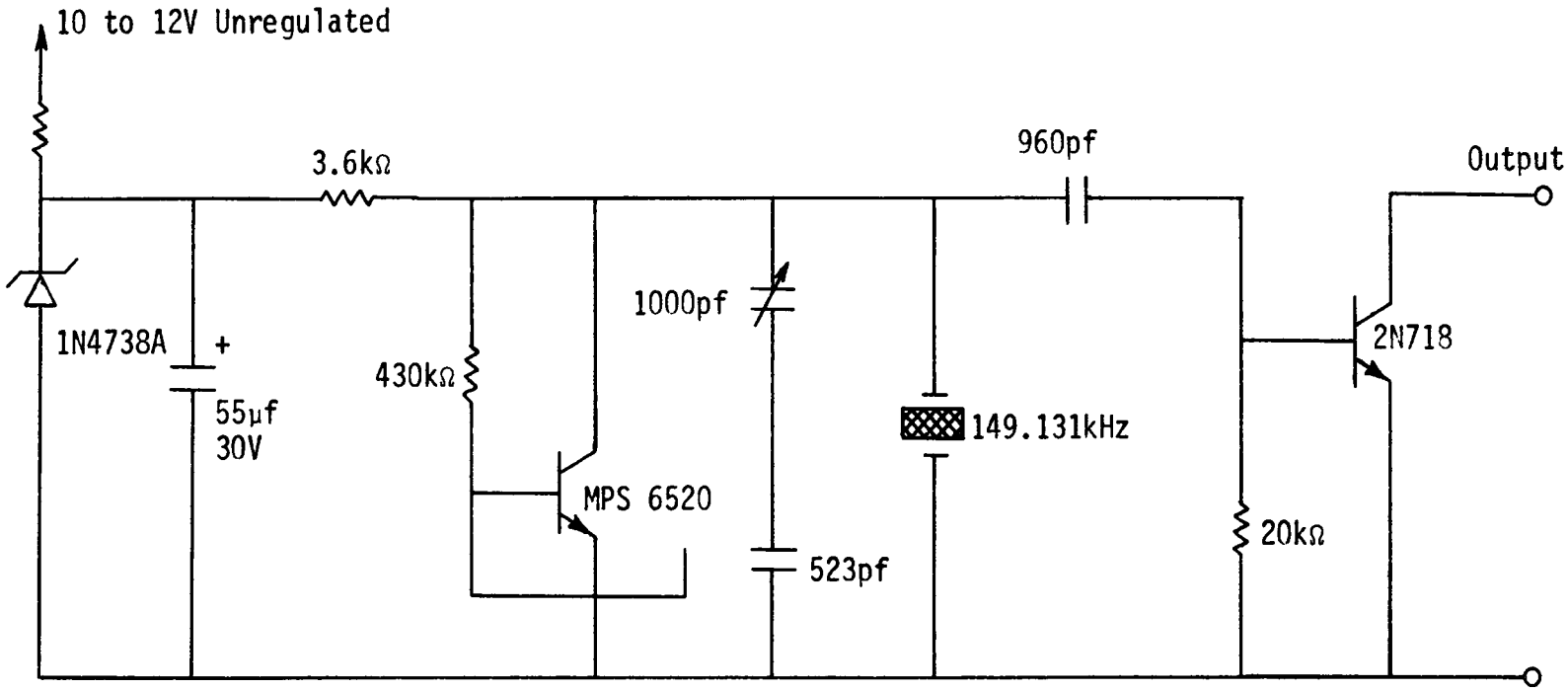


Figure 12

Time Base Oscillator Schematic

H. Time-Of-Day Word Generation

The 15 minute period of the last flip-flop in the control logic section is the first bit in the time-of-day word generator. Division by 16 in four MC839P's is done in the time-of-day word generator. The output of each stage in these dividers is fed into the inputs of two Fairchild 9312 digital multiplexers. The period of the last flip-flop is 8192 hours which is almost one year. The outputs of the two 9312's are fed into the frequency shift keyer as shown in Figure 10. A block diagram of the complete frequency division is given in Figure 13.

I. Control Logic

The most extensive design work in the construction of the monitor was required by the control logic section. The function of this section of the monitor is to provide all of the necessary electrical commands of the operation of the monitor in both record and playback modes. The principle of operation of the controller is the recognition of patterns generated by a sixteen stage binary counter. This counter is also part of the clock frequency division circuits and is labeled as "control logic" in Figure 13. The outputs of the logic pattern recognition circuits are connected to the various control points in the monitor. The outputs are electrical pulses of different periods and durations. The first part of the control logic discussion concerns the operation of the control logic derived from the first eight bits of the sixteen bits in the counter.

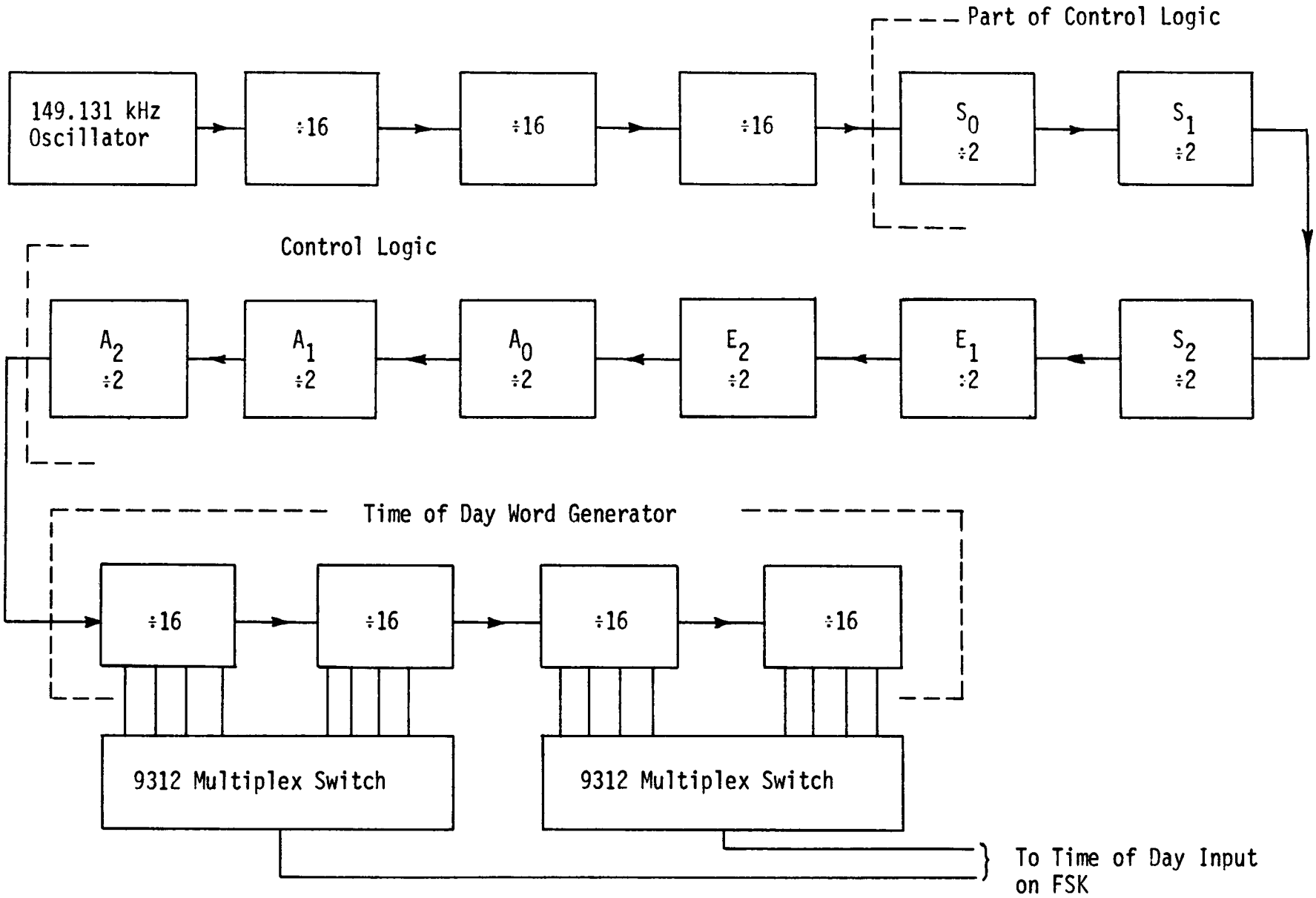


Figure 13

Block Diagram of Clock System

These are the least significant bits; i.e., those which change the fastest. Figures 14a and 14b are two views of the control logic and other circuits of the monitor.

Figure 15 shows the timing diagram for the first 32 counts of the control logic counter. This is the period required for one analog reading and one time-of-day reading. This sequence is repeated seven more times for each data recording period. In the figure, the groups of "1's" and "0's" which are circled are the patterns which are recognized by the control logic. The columns labeled A_2, A_1, and A_0 control the analog multiplex switch. The three counter stages whose outputs are A_2, A_1, and A_0 are connected directly to the control inputs of the analog multiplex switch. When all three columns are "0", the first analog channel is gated "on". When these columns read "0, 0, 1", the second analog channel is gated "on" and when they read "0, 1, 0", the third channel is turned "on", etc. The columns labeled S_0, S_1, and S_2 are the controls for the digital multiplex switches that follow the A to D converter. These "S" columns function in the same way for the digital switches as the "A" columns for the analog switch. The E_1 and E_2 columns are the output enable controls for the digital multiplex switches. When the E_1 column is "1" the first digital multiplex switch functions and when the E_2 column is "1" the second multiplex switch functions.

Four counts after the first analog line is gated "on", the pattern 0,0,1,0,0 appears in columns E_2, E_1, S_2, S_1, S_0. This pattern is repeated every 32 counts for a period of one count. It occurs four counts after each analog channel is gated "on". This pattern is recognized and used to trigger the A to D converter; that is, it is

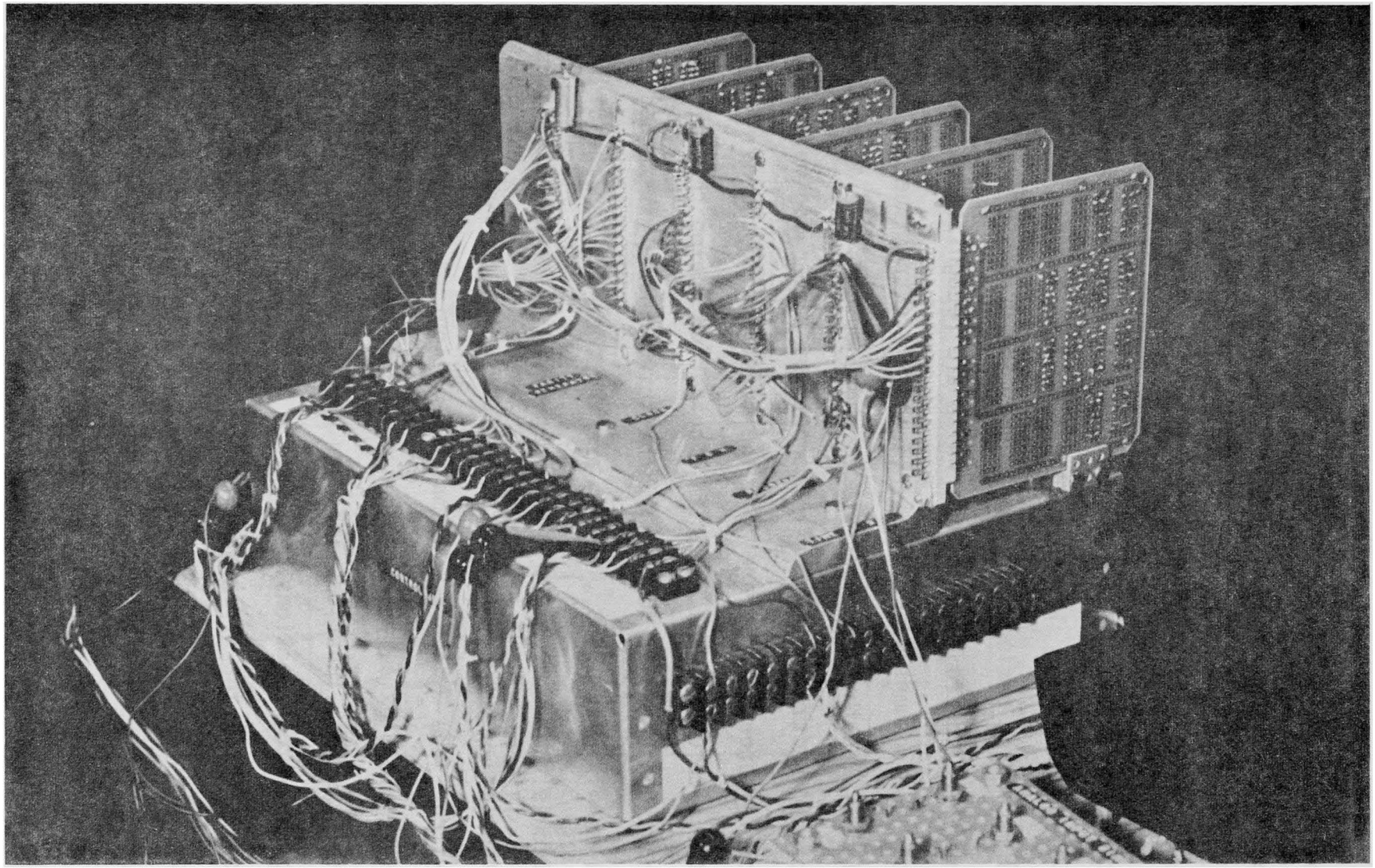


Figure 14a

Monitor Control Logic - Rear View

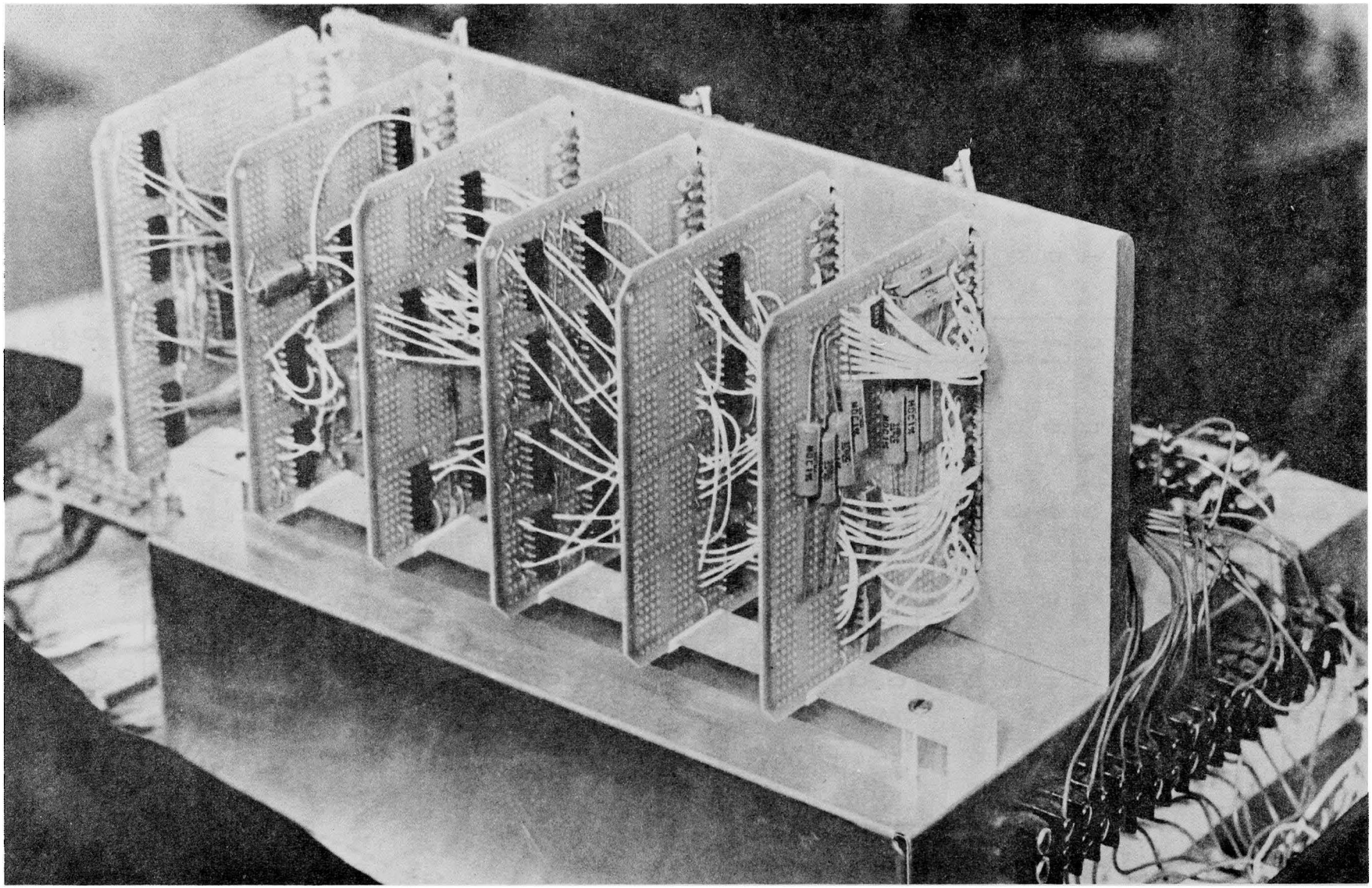


Figure 14b

Monitor Control Logic - Front View

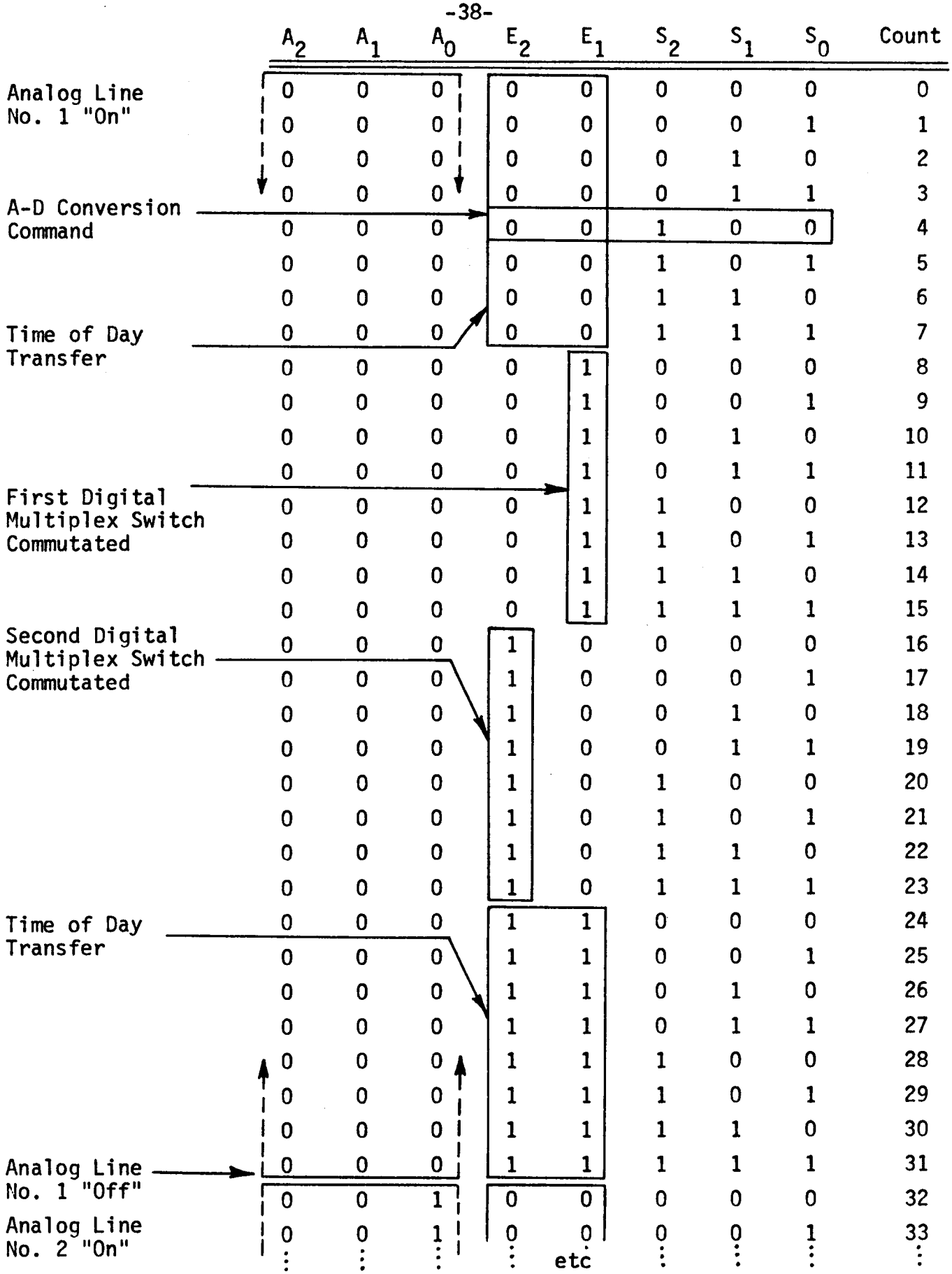


Figure 15

Timing Diagram of First Section of Control Logic

used to initiate an A to D conversion. The conversion is made four counts after the analog switching to allow any transients to subside before the A to D conversion is made. Figure 16 is a logic diagram of the conversion command recognition circuit.

Between analog readings, the time of day information is gated to the FSK. This occurs when the E_2 and E_1 columns are either both "0" or both "1". This pattern is recognized by an Exclusive OR circuit. The logic diagram and truth table for this circuit are shown in Figure 17. The pattern of both "0" or both "1" on the E_2, E_1 columns occurs between counts 0 through 7 and 24 through 31 on the timing diagram (Figure 15).

The eight most significant bits of the control logic counter serve to control the operation of the recorder in the record mode. A timing diagram of this operation is given in Figure 18. Two cycles are shown and the period between cycles is 15 minutes (256 counts). After count number 3, the tape transport motor in the recorder is started. The motor continues to run through count number 7. The motor is started two counts before it is used to allow it to reach operating speed. During the 6th count, the data and time information are recorded. Figure 19 shows the logic diagram for the pattern recognition circuit used to control the motor and clutch. In addition to the counter inputs to the control logic, there is a line which is labeled "record disable input". The function of this line is to prevent the monitor from attempting to record and playback data if the two commands happen to be given at the same time. The playback command overrides the record command.

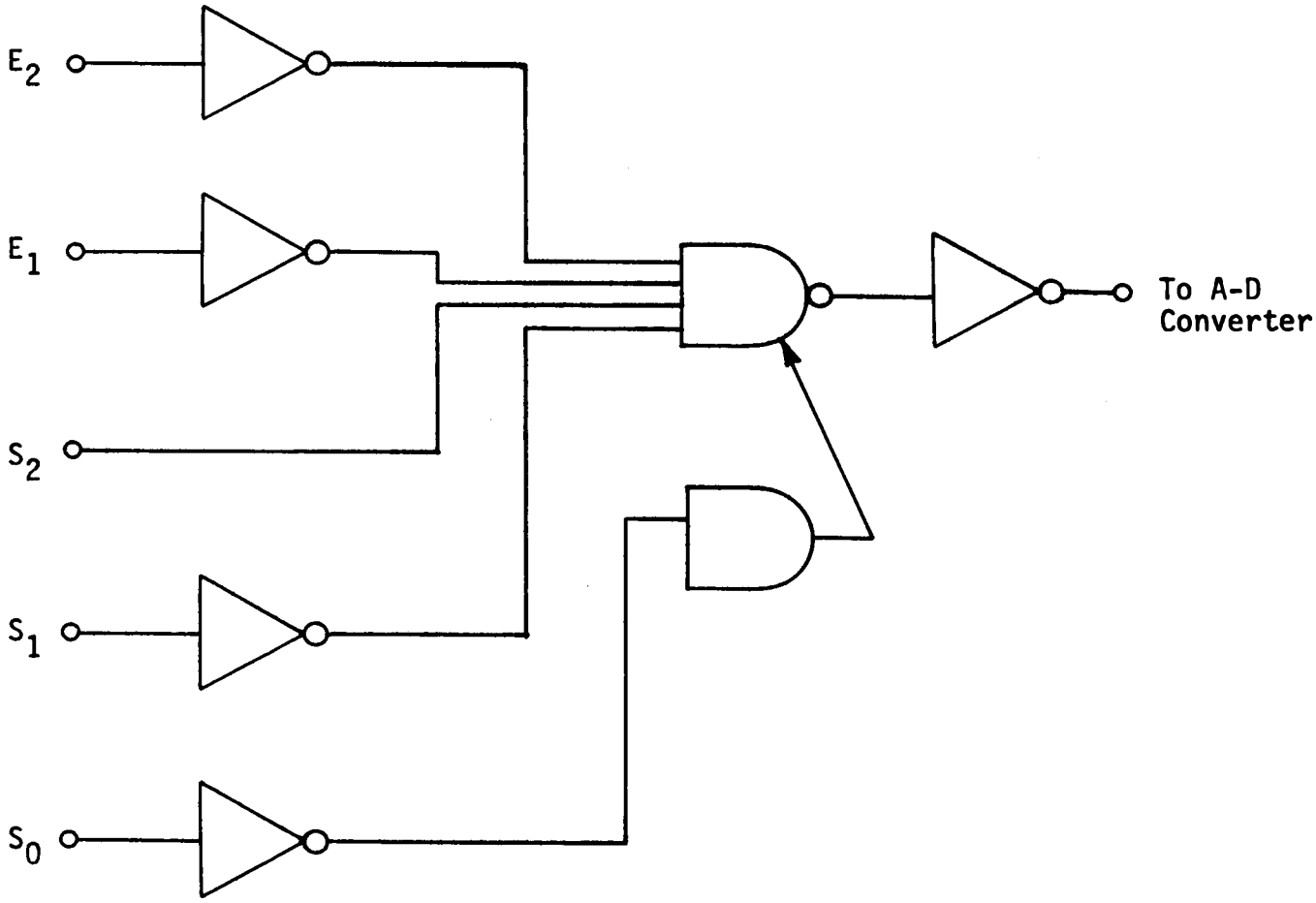
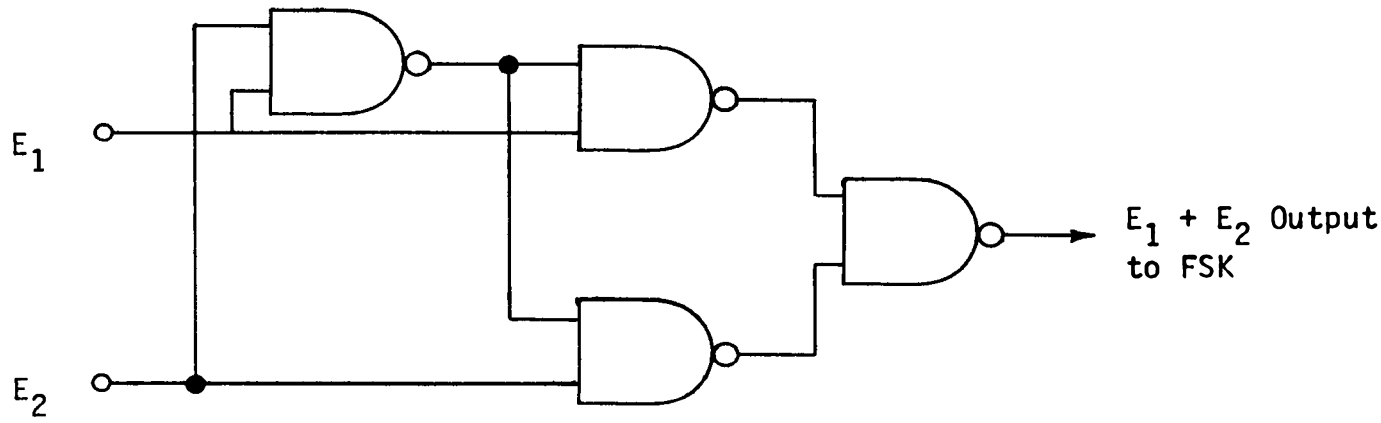


Figure 16

Logic Diagram of Conversion Command Circuit



E_1	E_2	Output
0	0	1
0	1	0
1	0	0
1	1	1

Figure 17

Exclusive "OR" Circuit and Truth Table

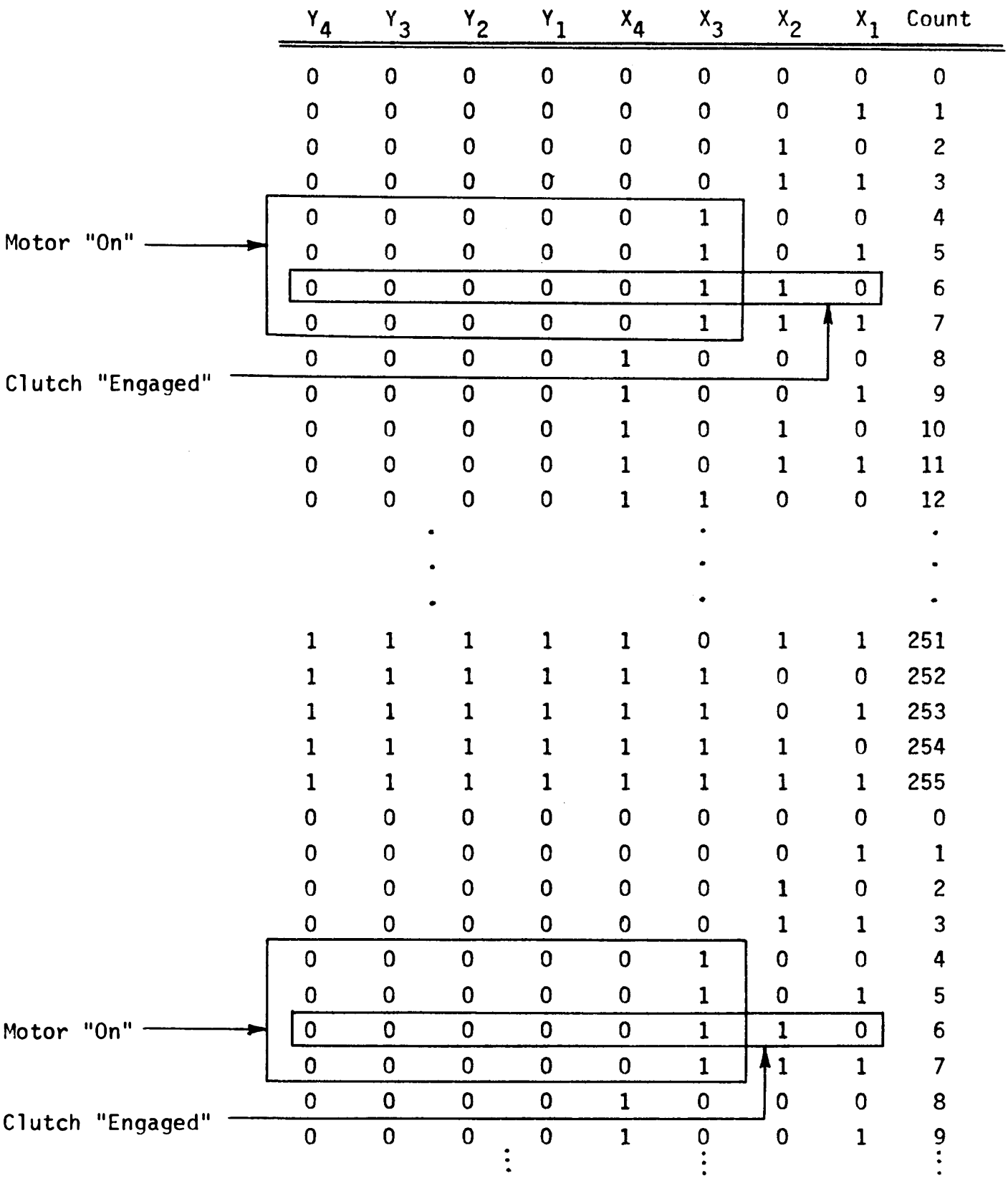


Figure 18

Timing Diagram of Second Section of Control Logic (Recorder Operation)

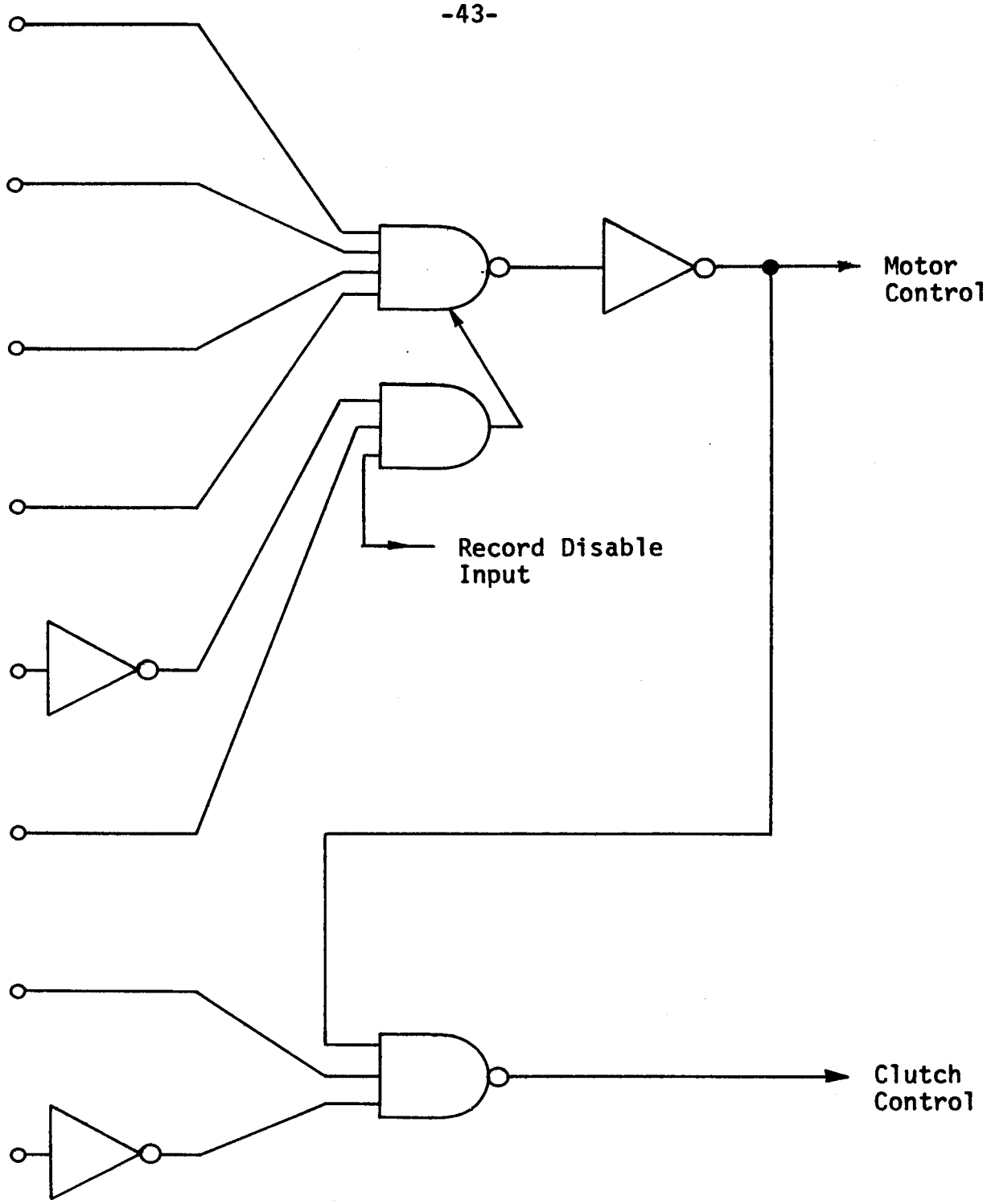


Figure 19

Logic Diagram of Recorder Control Circuits

In the playback mode of operation, the tape recorder motor and clutch are controlled by logic circuits completely separate from the record control circuits. Playback of data is initiated by a switch closure which resets two flip-flops. When playback is initiated; the motor is started, the clutch is engaged, the electronics in the recorder is switched from "record" to "playback", and the audio output is muted. All of this occurs simultaneously and directly after the reception of the playback command. The tape is now running and proceeds until the marker (cue) on the second track of the tape is reached. At this point, the audio is turned on and the recorded data are played back. When the tape has made one complete cycle and the marker is reached for the second time, the motor is shut off, the clutch is disengaged, and the electronics is switched back into the record mode. The monitor is now ready to continue to accept data. If a data point is supposed to be taken during a playback period, it is skipped. That is, the playback command overrides. Figure 20 is a logic diagram and schematic of the playback mode control logic. The extra circuitry after the control inputs is for the suppression of spurious signals. Switch contact bounce, line transients, etc. must be carefully guarded against for proper logic circuit operation. The output terminals for the motor and clutch are preceded by "OR" circuits to allow operation of the motor and clutch by either the record mode logic or the playback mode logic.

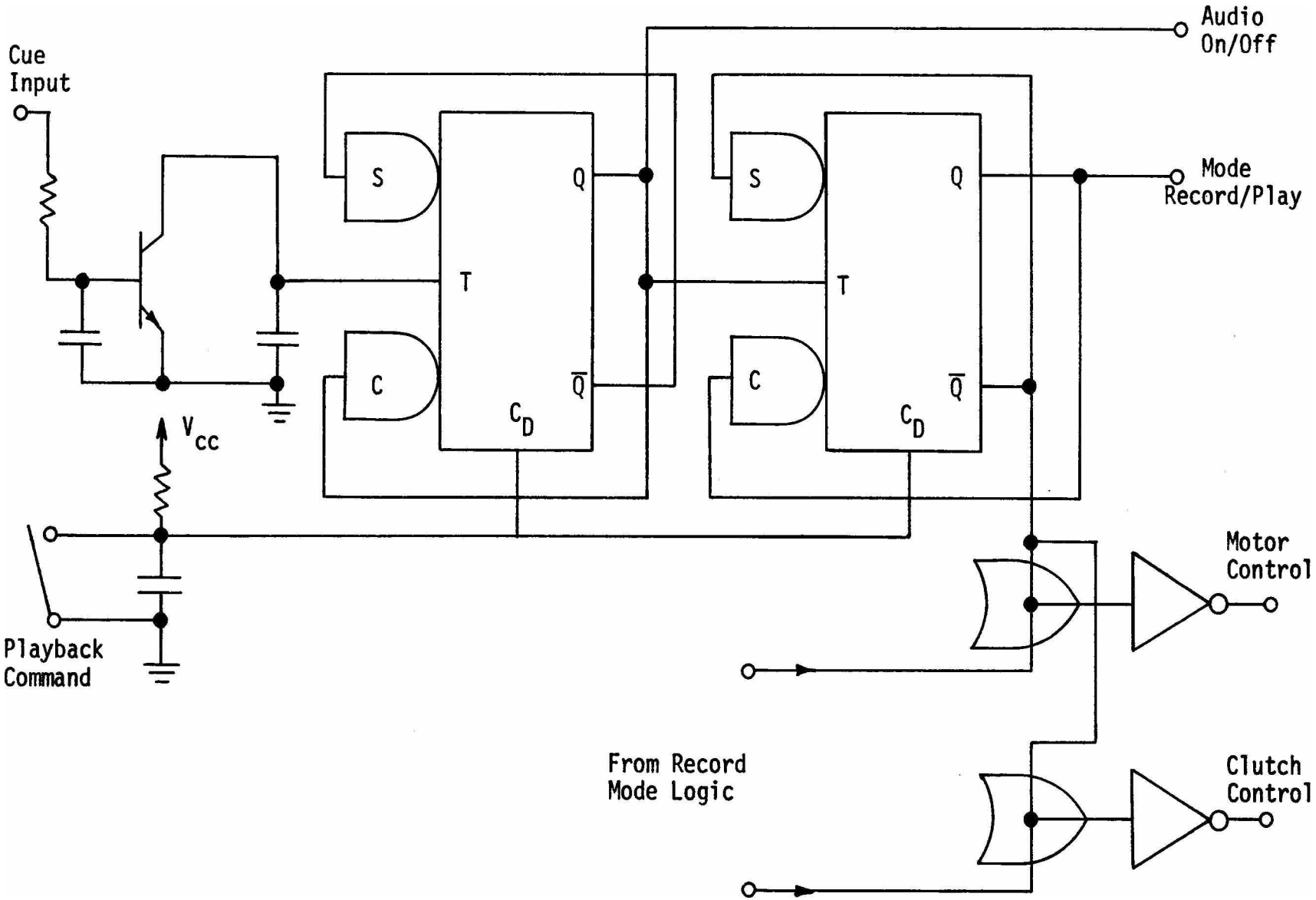


Figure 20

Logic Diagram of Playback Mode Circuits

J. Relay Interface Circuits

During the design and construction of the monitor, one of the principal design goals was high reliability. To achieve this objective, solid state components were used and the number of moving parts kept to a minimum. The tape recorder has most of the moving parts but it was also necessary to use relays in several applications. Certain switching functions are best done with relays. At the present time it is possible to control the power circuits for the tape recorder motor and clutch with solid state devices but the relays were used because of the design problems encountered with inductive load switching. The supply voltages for the tape recorder electronics are also relay switched.

The control functions which are generated by the control logic are available as 0 and 5 volt outputs from DTL integrated circuits. The integrated circuits can sink a reasonable amount of current in the logical "0" state and can supply a 5 volt output through a 6,000 ohm resistor in the logical "1" state. Since very few relays can operate from this type of supply, some interface circuits were designed to operate the relays from the control logic levels. Figure 21 is a schematic of one relay driver stage and power supply. The circuit has negligible loading on the integrated circuits. Equally important is that the relay, with its inductive and switching transients, is removed from the logic circuits by two stages of amplification. The diode across the relay coil serves to further suppress transients. All of

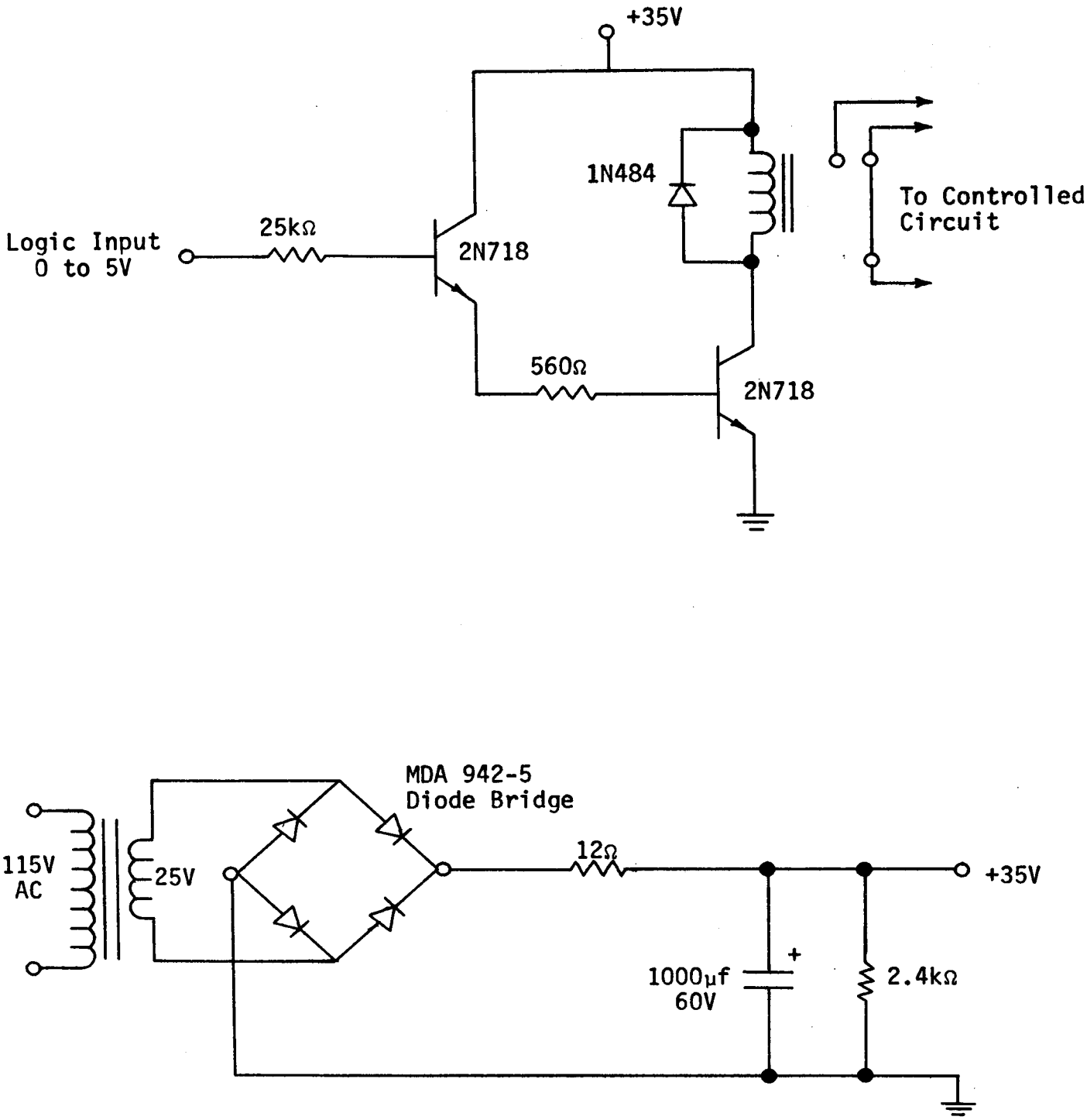


Figure 21

Relay Interface Circuit and Power Supply

the relays are operated from a common power supply which is not used for any other function in the monitor. This isolation of the power supply is also to guard against switching transients entering other parts of the monitor.

K. Power Supplies

In addition to the relay power supply, 5 volt and 20 volt supplies are needed for monitor operation. The 5 volt supply is used for the DTL integrated circuits used in the monitor. In the initial design stages of the monitor, the complexity of the control functions could not be easily judged and, as a result, a much larger than necessary power supply was built. Figure 22 is a schematic of the 5 volt supply. A unique feature of this supply is that all of the regulation circuitry is contained in the integrated circuit (Motorola MC 1461) except for a series pass transistor and a few passive components. This design has proven to be highly successful in this application because of the stability and low output impedance of the supply. An unregulated output from the 5 volt supply is used to supply the FSK tone generators and the time base oscillator which has its own regulation circuitry.

Figure 23 is a schematic of the 20 volt supply used for the MOS multiplex switch. Like the 5 volt supply, the 20 volt supply uses a Motorola MC1461 integrated circuit regulator. Very little current is required for the operation of the multiplex switch so that a series pass transistor is not necessary.

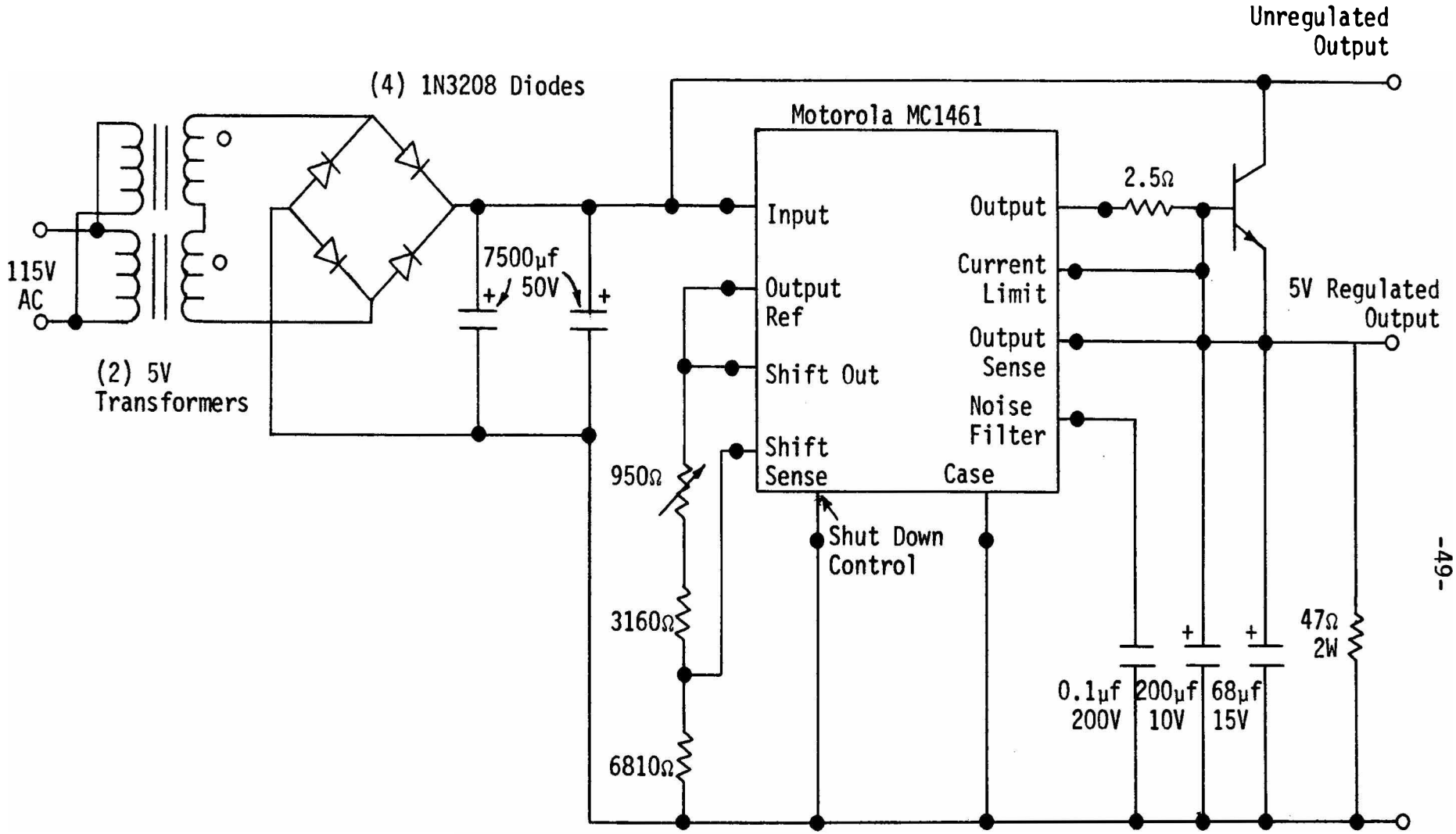


Figure 22

5 Volt Logic Power Supply Schematic

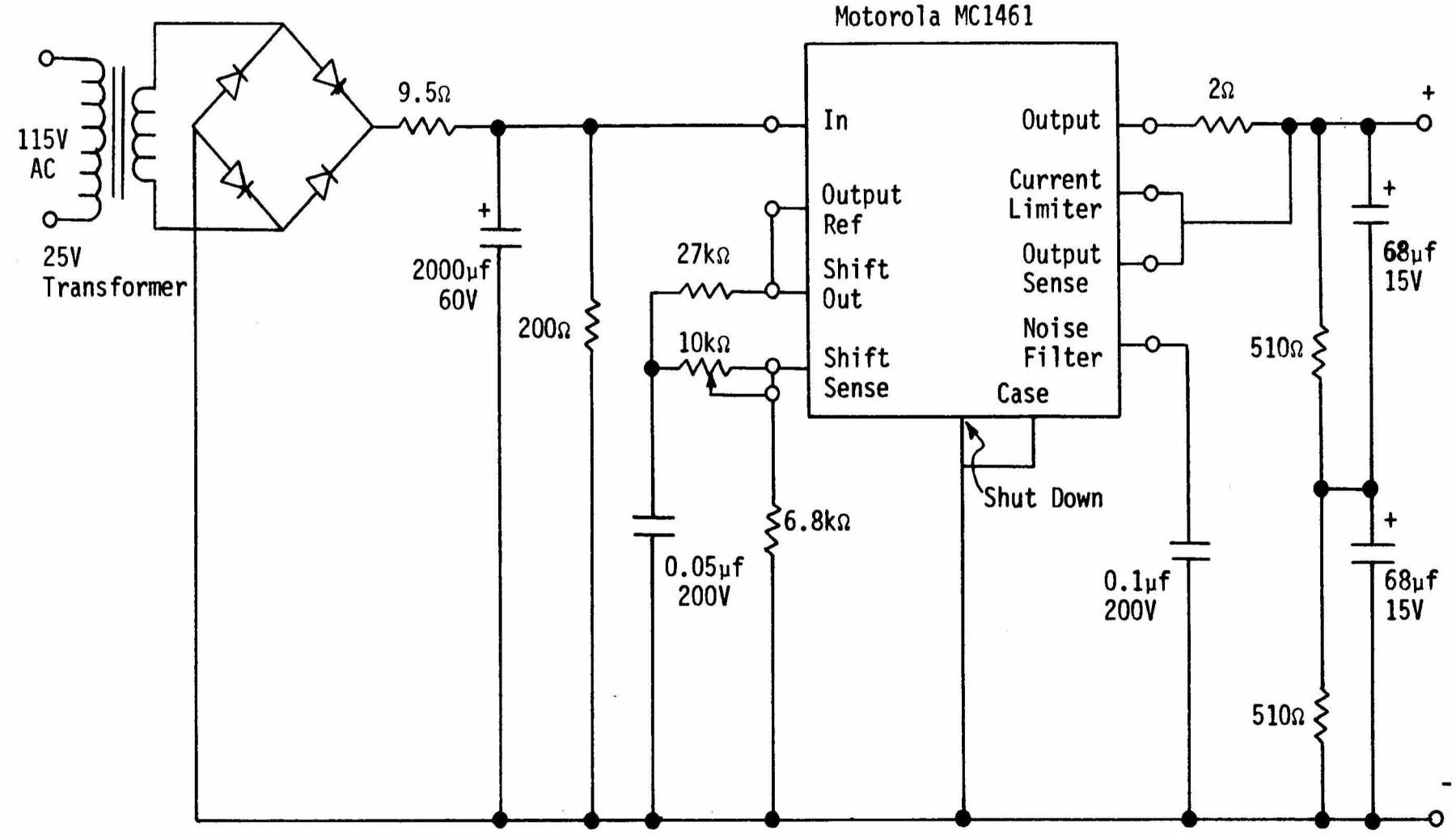


Figure 23

20 Volt Multiplex Switch Power Supply Schematic

III. CENTRAL PROCESSER

The information stored on magnetic tape in the monitor can be played back at any time by a command from the central processer. The water quality data is in BCD and the time of day is in pure binary format. Both are frequency shift keyed. Before any of the data can be processed or displayed, it is necessary to convert from the FSK signals on a telephone circuit to a form compatible with a computer or printer. Figure 24 is the schematic of the unit which can take FSK inputs and convert them to 0 to 5 volt logic levels. Three channels are available in this device in case it should become necessary to use the third channel to identify the beginning of each word. The circuit consists of an operational amplifier in an adjustable gain configuration connected to an emitter follower. The function of the emitter follower is to provide a low impedance drive for the three filter networks.

The filters used in this device are a simple one-stage LC type which are heavily damped. The high damping and high drive level assures rapid response and decay of the network. An undesirable result of this high damping is broad frequency response. The proper compromise between fast response and channel bandwidth will need to be determined by actual field trials. The center response frequency of each channel is adjusted by the variable inductors.

The output of each filter section is converted to DC and filtered to operate the driver stages before the invert gates. The inverter output is now a DTL compatible signal which can be coupled to a computer or

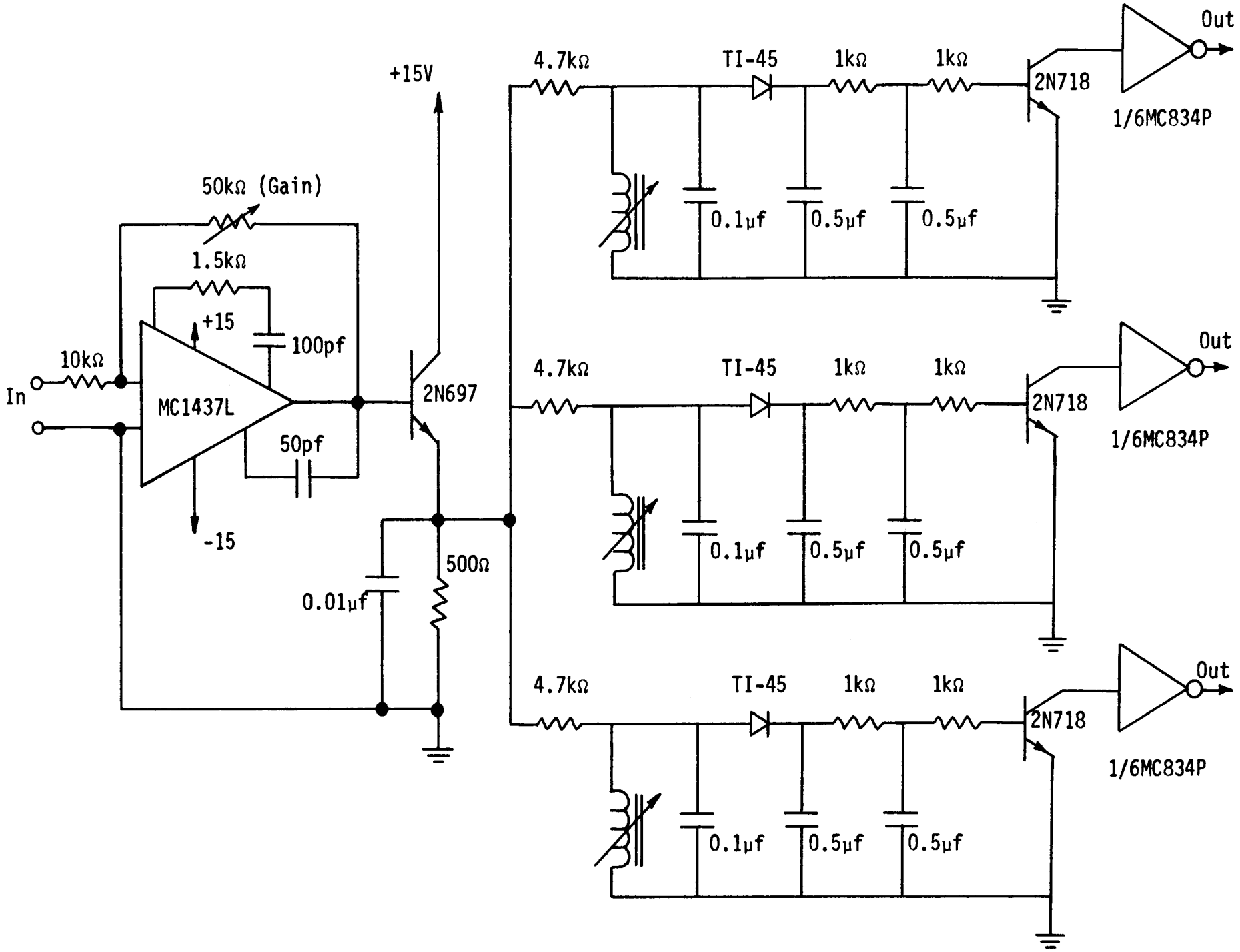


Figure 24

FSK to DTL Converter

readout device.

To prevent the monitor from playing back information when it is not required, a tone encoder and decoder has been designed. The decoder would supply the playback command to the monitor in response to a relatively long duration (several seconds) tone from the central processer. Figure 25 is the schematic of the encoder and Figure 26 is the schematic of the decoder.[2] Both units make use of resonant reed relays for frequency reference. The incorporation of this system into the monitor network will make the monitors insensitive to transient noises on the telephone circuits and will allow the operator of the central processing station to call for the field information when it is desired.

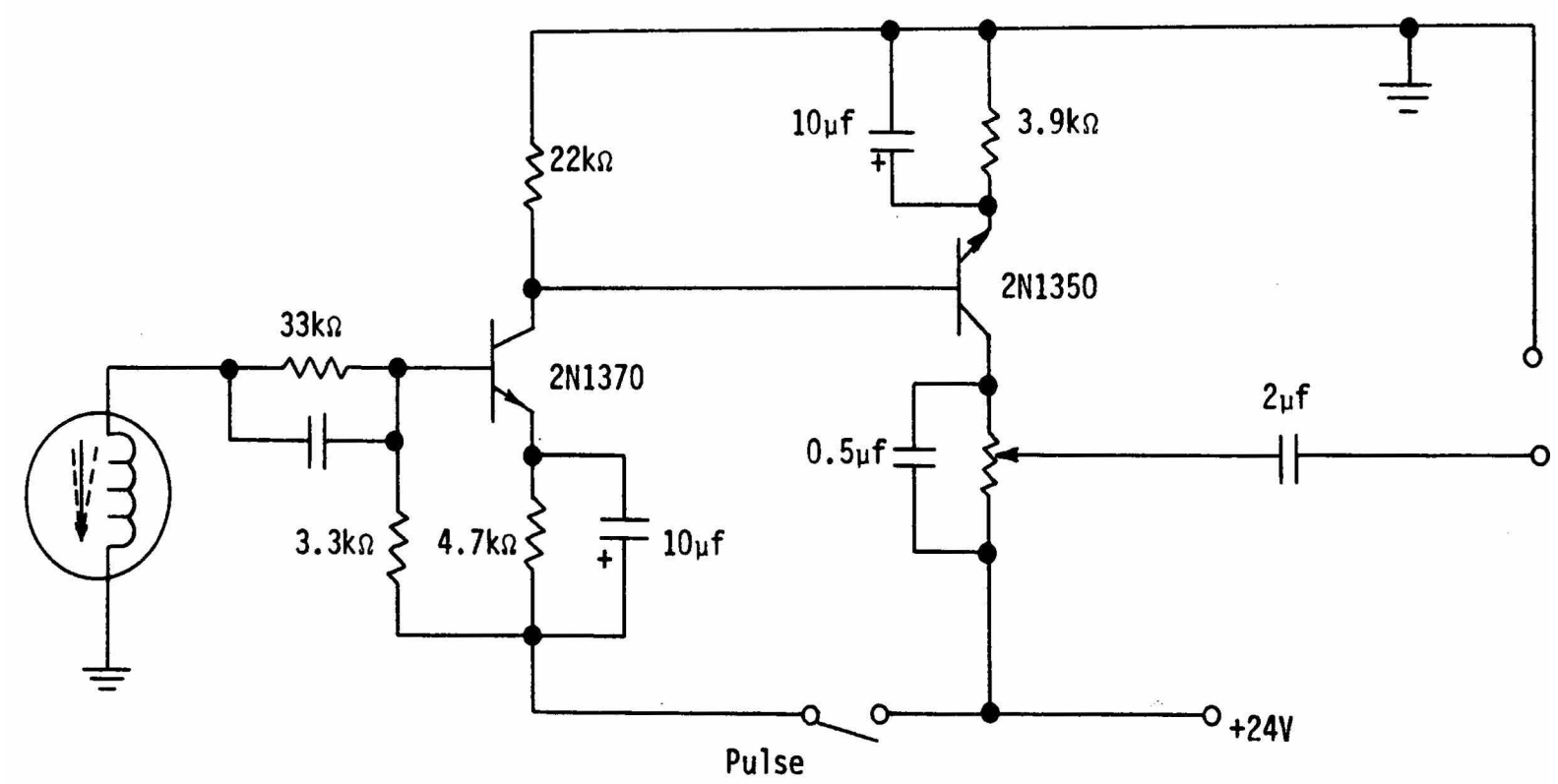


Figure 25

Tone Encoder

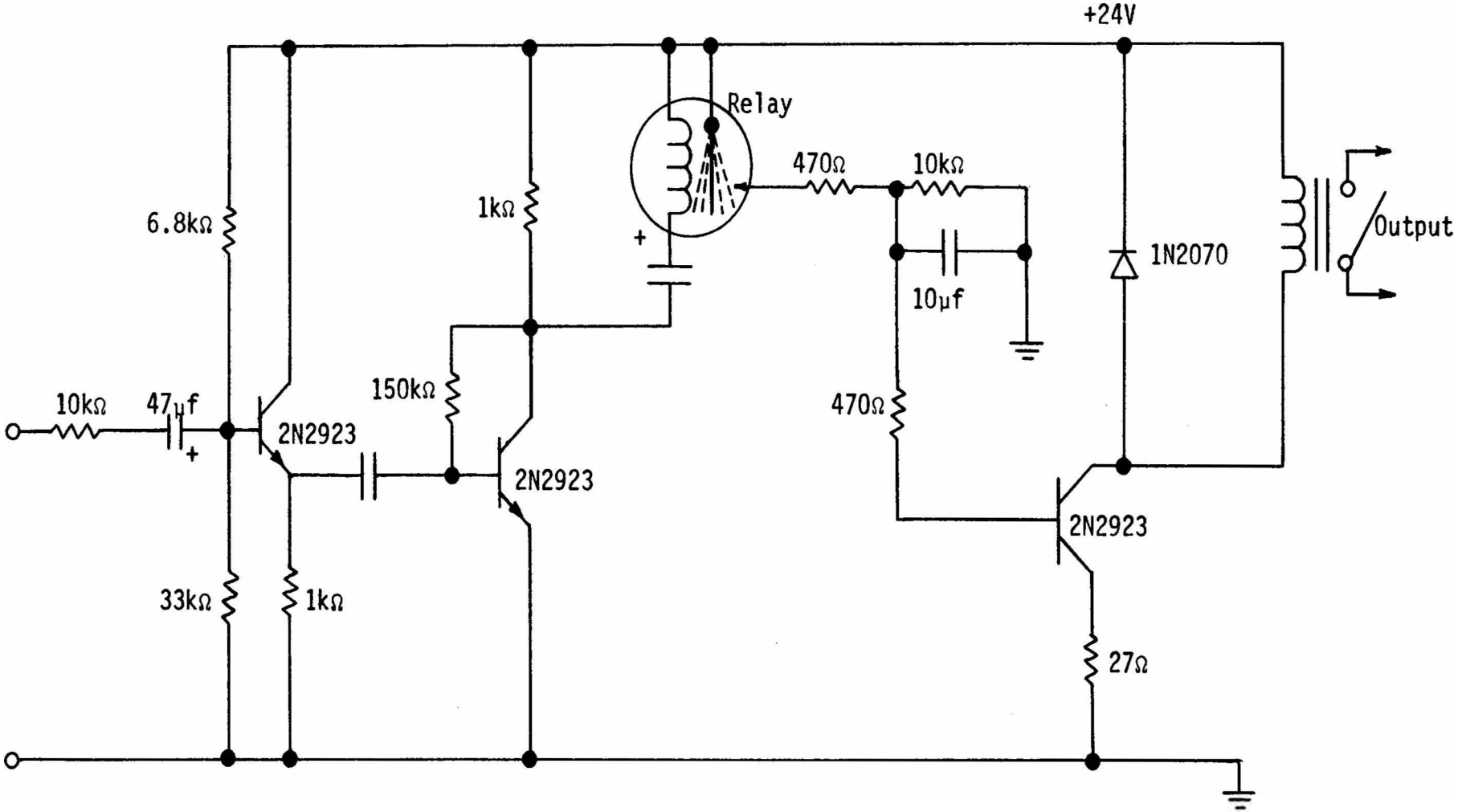


Figure 26

Tone Decoder

APPENDIX I

Theory of Operation[3]

The Gralex Digital Panel Meters employ an integrating technique to provide "3-1/2" digit decimal outputs representing input voltages. The basic integration process is a result of employing the relationship:

$$V = \frac{1}{C} \int i dt$$

where V represents the voltage reached when a current, i, is impressed on a capacitor C for an interval dt. The current (s) resulting from the impression of an input voltage V_{in} across series resistors is fed to the input of an operational integrator with capacitor C in the feedback loop. The input source current i_s is allowed to enter the summing junction of the integrator for an interval t_1. The resultant excursion of the ramp observed at the output of the integrator is directly proportional to the magnitude of the input source current i_s. At the conclusion of charging period t_1, a reverse i_R is impressed across discharge resistors. This causes capacitor C to discharge. The length of time expended in discharge capacitor C is directly proportional to the magnitude of the input voltage. A comparator sensed the time at which the ramp is completely discharged during interval t_2. At this time, a clock that was initiated at the start of period t_1 is stopped and the resultant count accumulated in the three decade counters is the digital equivalent of the input voltage.

The integration process is controlled by the use of a measurement rate clock and 10 kHz counting clock. The measurement rate clock initiates the 10 kHz counting clock. After 1,000 counts have been received by the decade counters a carry is generated and fed to the control section to generate signal t_2. During the time the initial 1,000 counts are being accumulated (t_1) a clamp at the junction of the input resistors is opened to allow the source current i_s to charge the integrating capacitor C to a voltage V for 100 milliseconds.

At the end of t_1 the source current is inhibited and the reverse reference current i_R is impressed on the integrator. The length of time required to discharge C, t_2, is proportional to the magnitude of the input voltage V_{in}. When the comparator senses the zero-crossing, the counting clock is stopped. The resultant accumulated count appearing in the three decade counters is now directly proportional to the magnitude V_{in}.

At the conclusion of t_2 the contents in the decade counters are strobed and transferred to the output BCD decoder drivers for the display.

At the conclusion of t_2 an electronic switch is closed across integrating capacitor C, holding the output of the integrator at a zero clamp level. This insures that with each measurement the output of the integrator will start from the same reference level thereby affording essentially drift free operation.

References

1. Arkansas Pollution Control Commission, Annual Progress Report, 1968-1969.

2. Control Technique with Resonant Reed Relays, Bramco Control Division, Ledex Inc., Piqua, Ohio, 1968

3. Instruction Manual, Digital Panel Meters, Model DM-31A, Gralex Industries Inc., Copiageu, New York, 11726