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Silicon Wafers with Different Functional Layers Embedded by Direct Bonding for Sensors and Power Devices

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Silicon Wafers with Different Functional Layers Embedded by Direct Bonding for Sensors and Power Devices

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Silicon Wafers with Different Functional Layers Embedded by Direct Bonding for Sensors and Power Devices
（直接接合によって異なる機能層を埋め込んだセンサー・パワーデバイス用シリコンウェーハ）

A dissertation submitted for the degree of Doctor of Philosophy (Engineering)

Department of Robotics

by

Yoshihiro KOGA

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Silicon Wafers with Different Functional Layers Embedded by Direct Bonding for Sensors and Power Devices

Yoshihiro KOGA

Abstract

Public facilities have been installed with many security cameras to reduce the occurrence of crime and traffic accidents. It is most important for the night vision of cameras to decrease the dark current. Because the dark current is generated by impurities such as metal and oxygen in the device fabrication region, impurities must be decreased. A gettering technology that can capture impurities is important to decrease impurities. The gettering capability must be set higher than that of current technology of the cameras for night vision. However, the gettering capability of current technologies is less than 1×10^{13} atoms/cm^2, and cannot be improved more than 1×10^{13} atoms/cm^2. On the other hand, since oxygen out-diffuses from the silicon substrate contained oxygen more than 1×10^{17} atoms/cm^3 during high temperature treatment of the wafer fabrication process such as an epitaxial growth or an anneal, there are more than 1×10^{17} atoms/cm^3 of oxygen in the device fabrication region of an epitaxial or denuded zone-intrinsic gettering (DZ-IG) wafer. Thus, the wafer for the cameras for night vision must have the gettering capability more than 1×10^{13} atoms/cm^2 and oxygen in device fabrication region less than 1×10^{17} atoms/cm^3.

It has become especially important to counter environmental problems such as global warming and air pollution. Automobiles have been changing from gasoline cars to hybrid and fully electric cars, which contain various power devices. The electrical isolation regions of the devices were used by pn junction. However, they have been used by SiO_2, in order to decrease leakage currents in power devices. These devices are formed on silicon-on-insulator (SOI) wafers and shallow trench isolation (STI) are buried around devices. Since a buried oxide (BOX) layer of the current SOI wafers is formed by thermal oxidation, the BOX layer has a fixed charge and the resistivity of the silicon layer on the BOX layer is consequently varied. In addition, a device formed on the SOI wafer is completely surrounded by SiO_2 that are the BOX layer and STI; therefore, the self-heating of the device is accelerated, which in turn increases the leakage current. Moreover, the process of fabricating an SOI wafer involves a long treatment at temperatures above 800°C. Since the coefficient of thermal expansion of the BOX layer is different from that

of a silicon wafer (substrate) made of a silicon single crystal, the SOI wafer has the membrane stress around the BOX layer. The membrane stress causes the warping of devices such as micro-electromechanical systems (MEMS) after the BOX layer under MEMS is etched. Current SOI wafers are plagued by at least these three issues that are the fixed charge of the BOX layer, the membrane stress around the BOX layer, and the poor thermal conductivity of the BOX layer.

In my research, silicon-based bonding wafers with different functional layers for sensors and power devices were studied to resolve the above issues. Surface-activated bonding (SAB) in an ultrahigh vacuum at room temperature was used to reduce thermal stress to the wafer as much as possible and to avoid contamination by metallic impurities during wafer bonding.

In Chapter 1, some kinds of semiconductor devices (imaging, MEMS, and power devices) and the wafer bonding technologies needed for fabricating these semiconductors are described. Finally, the purpose of this thesis is described.

In Chapter 2, I describe the silicon-bonded wafers with oxygen less than 1×10^{17} atoms/cm^3 in a device fabrication region and a gettering capability exceeding 1×10^{13} atoms/cm^2 for complementary metal oxide semiconductor (CMOS) image sensors. Two types of silicon-bonded wafer were studied. One type is composed of an epitaxial wafer bonded to a molecular-ion-implanted wafer for fabricating high-sensitivity CMOS imaging sensors of security cameras. The epitaxial layer is less than 15 µm thick. The other type is a floating zone (FZ) wafer bonded to a Czochralski (CZ) wafer at room temperature and is utilized for producing IR-detecting sensors for avalanche photodiode (APD) devices used in light detection and ranging (LiDAR) systems. The device fabrication region is thicker than 100 µm. The bonding region has a high gettering capability exceeding 1×10^{13} atoms/cm^2 for metallic impurities, and oxygen does not out-diffuse from CZ wafer, resulting in less than 1×10^{17} atoms/cm^3 of oxygen in the device fabrication region.

In Chapter 3, three types of SOI wafer for power devices and MEMS are described. They are fabricated by chemical vapor deposition (CVD) and SAB. One type has a BOX layer formed by plasma-enhanced chemical vapor deposition (PE-CVD), in order for the resistivity in the silicon layer to remain unchanged by the fixed charge in the BOX layer made of the thermal oxide film. The second type has a deposited and annealed BOX layer to increase the density and breakdown electric field of the BOX layer. The third type is formed with a BOX layer made of SiO_x ($x < 2$) to decrease the membrane stress around the BOX layer. The BOX layer formed by PE-CVD has no fixed charge and there is no change in the resistivity of the silicon layer on the BOX layer. The occurrence of the accidental

B-mode breakdown electric field of the BOX layer could be reduced by annealing the deposited BOX layer at a temperature higher than that of deposition. When the BOX layer made of SiO_x, where x was less than 0.7, the membrane stress decreased from that of the reference sample ($x = 2$).

In Chapter 4, SOI wafers with a high-thermal-conductivity BOX layer are described for power and RF devices. The SOI wafer could be fabricated with the BOX layer made of polycrystalline diamond or amorphous silicon carbide (SiC) to prevent the self-heating of devices fabricated on the BOX layer during operation. The thermal conductivity of the polycrystalline diamond layer was one hundred times higher than that of the SiO_2 layer. The breakdown electric field of the amorphous SiC layer is 10–11 MV/cm, the same as that of a SiO_2 layer.

Finally, the studied wafers described in Chapters 2–4 are concluded in Chapter 5.

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Chapter 1 Introduction

1.1 Silicon device technologies

1.1.1 Sensor device technologies

To reduce the occurrence of crime and traffic accidents, public facilities such as airports, stations, sports stadiums, shopping malls, and police boxes have been installed with many security cameras to deter crime. Living spaces such as apartments and houses have also been equipped with security cameras. The use of cameras is becoming increasingly widespread in society. These cameras have imaging devices based on a pn-junction and a metal oxide semiconductor (MOS) capacitor, as shown in Fig. 1.1 When the p-type region is applied with zero voltage while the n-type region is applied with some amount of voltage, the pn-junction has a depletion layer between the n-type and p-type regions, as shown in Fig. 1.1 (a).[1] On the other hand, when the p-type region is zero voltage and the gate is applied some amount of voltage, the MOS capacitor has a depletion layer under the SiO_2 layer, as shown in Fig. 1.1 (b).[2] When light is illuminated into the pn-junction, holes, and electrons are generated in the depletion layer of the pn-junction. These generated electrons can be transferred from the pn-junction to the MOS capacitor by controlling the input voltages of the n-type region and gate, as shown in Fig. 1.1 (c).[3]

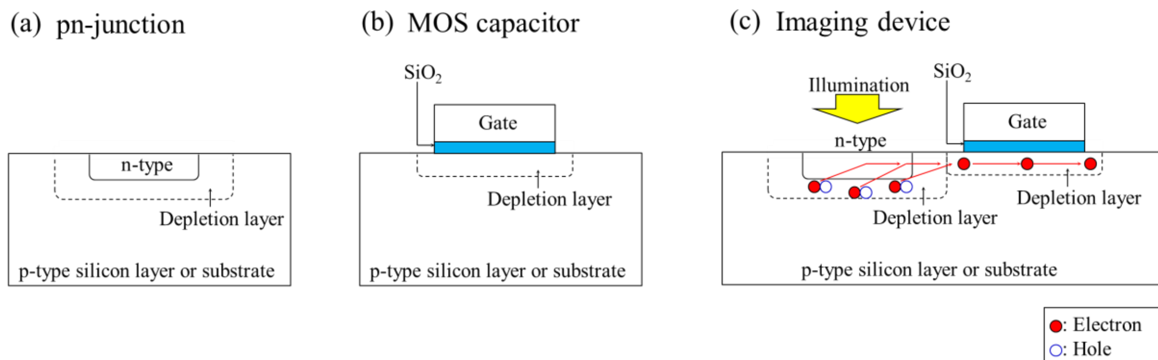


Fig. 1.1. Structure of imaging device.

Imaging devices are of two types, as shown in Fig. 1.2. One type is the charge coupled device (CCD) and the other type is the CMOS image sensor (CIS).[4,5] In the CCD, the electrons generated in a photodiode are transferred to an output terminal through numerous gates, as shown in Fig. 1.2 (a). Thus, this device is easily affected by electrical noise generated between the photodiode and the output terminal. On the other hand, in the CIS, the electrons generated in a photodiode are immediately transferred to an output terminal through a gate near the photodiode, as shown in Fig. 1.2 (b). Thus, The CIS is negligibly affected by electrical noise.

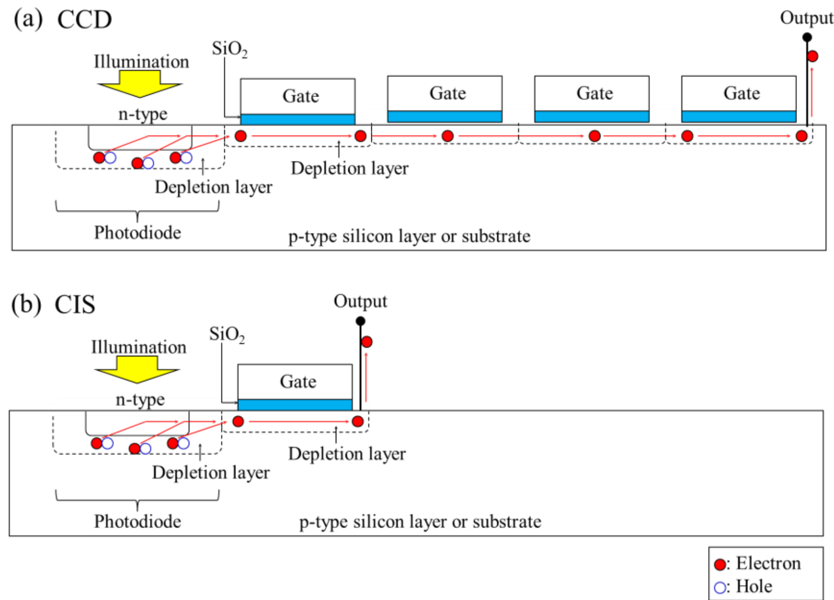


Fig. 1.2. The mechanisms of imaging devices.

Figure 1.3 shows the operation principle of an imaging sensor. When light is illuminated onto a chip, the photodiode formed by the pn-junction detects the light and generates electrons and holes. Then, electrons are then transferred through the MOS transistor, as shown in Fig. 1.3 (a). Figure 1.3 (b-1) shows the process of detecting the light and generating electrons using an energy band diagram of the electrons. When the light illuminates the photodiode, an electron in the valence band (E_v) receives the energy of the illuminated light and transfers to the conduction band (E_c). If, owing to a defect in the photodiode, an electron exists at the trap level (E_t) between E_v and E_c, the light illuminated to the photodiode causes this trapped electron to also transfer to E_c, as shown in Fig. 1.3 (b-2). This extra electron generates a photoelectric phenomenon that results in an error known as a smear.[6)] On the other hand, when the light is not illuminated to the photodiode, the photodiode still detects a small amount of light and may cause an electron at E_t to transfer to E_c, as shown in Fig. 1.3 (c-2). This photoelectric phenomenon also results in an error known as a white spot.[7,8)] Figure 1.4 shows the temperature dependence of the dark current in CMOS image sensors.[9)] It is classified by generation and diffusion currents. The generation current originates from the defects or impurities in the photodiode. The diffusion current flows from the defects or impurities in a silicon substrate below the photodiode to the photodiode. The generation current is much higher than the diffusion current at less than 53°C. If the generation current does not arise at all, the dark current can be reduced to one-tenth at less than 53°C. Because cameras are generally used at room temperature, which is less than 53°C, to decrease the dark current, it is more effective to reduce not the diffusion current but the generation current.

The dark current originates from crystal defects or impurities such as metal or oxygen in the photodiode, as shown in Fig. 1.5. Therefore, the fabrication of imaging devices has two requirements. One is that there should be no defects in the device fabrication region. This is satisfied by growing an epitaxial layer on the silicon wafer or by forming a denuded zone through the annealing of the wafer at a high temperature above 1000°C. The other requirement is that there should be no impurity such as metal or oxygen in the device fabrication region. Device fabrication processes are optimized by cleaning to remove metallic impurities introduced during sputtering, annealing, or etching in which treatment equipment made of metallic parts are used. However, since the electrodes of devices are formed of silicide-containing nickel or copper and wires are made of copper, aluminum, and titanium, these metals remain in the device fabrication region. Therefore, a gettering sink that can

capture the metals must be formed in the silicon wafer to remove the metals from the region for fabricating CMOS image sensors.

Gettering technologies have long been studied to resolve this issue. When a gettering sink is formed on the wafer outside the device formation region, it can capture impurities such as metal and carbon and hence reduce the concentrations of impurities in the device formation region. The first-generation gettering sink was formed at the back of the silicon wafer and was called an external gettering (EG) sink, as shown in Fig. 1.6 (a).[10] There are two methods of forming an EG sink. A polysilicon layer is deposited at the back of the silicon wafer or phosphorus is doped into the back of the silicon wafer. The second-generation gettering sink was formed in the silicon wafer to improve the yields of logic and memory devices and was called an internal gettering (IG) sink, as shown in Fig. 1.6 (b).[11] Oxygen precipitates called bulk microdefects (BMDs) are formed in a silicon wafer upon heat treatment during wafer and device fabrications. With the development of wafers for a system in package (SiP) in which chips are laminated in one module to shrink the module size, the number of laminated chips increased, and the thickness of each chip became less than 100 μm. The number of bonded wafers increased before the dicing of the wafer and the assembly of the chips in the SiP module. Such a thin wafer cannot accommodate any gettering sinks that improve the yield of the SiP module. Thus, the EG method was again considered, and crystal defects were formed at the back of a silicon wafer during grinding or polishing to make the wafer thin, as shown in Fig. 1.6 (c).[12] However, when the thickness of the wafer or chip became less than 50 μm, the wafer or chip cracked. On the other hand, as the heat treatment in device fabrication has evolved to have a lower temperature and a shorter processing time, metals contaminated in the device fabrication region could not diffuse until the IG or EG sink, and cause the degradation of the device yield. Therefore, it was proposed to form the gettering sinks close to the device fabrication region; this is called proximity gettering (PG), as shown in Fig. 1.6 (d).[13,14] Crystal defects are formed directly under the device fabrication region by ion implantation into the silicon wafer.

Epitaxial and annealed wafers with IG sinks have been used for CMOS image sensors.[11,15,16] These wafers have gettering capabilities of less than 1×10^{13} atoms/cm^2 for nickel, copper, and iron, and oxygen more than 1×10^{17} atoms/cm^3. Because dark current (generation current) is generated by metallic impurities and oxygen in the device fabrication region, as shown in Fig. 1.4, these impurities must be reduced as much as possible in order for CMOS image sensors to be used for the night vision of security cameras and anticollision sensors. Thus, the wafers for them must have gettering capabilities of more than 1×10^{13} atoms/cm^2 for nickel, copper, and iron, and oxygen less than 1×10^{17} atoms/cm^3.

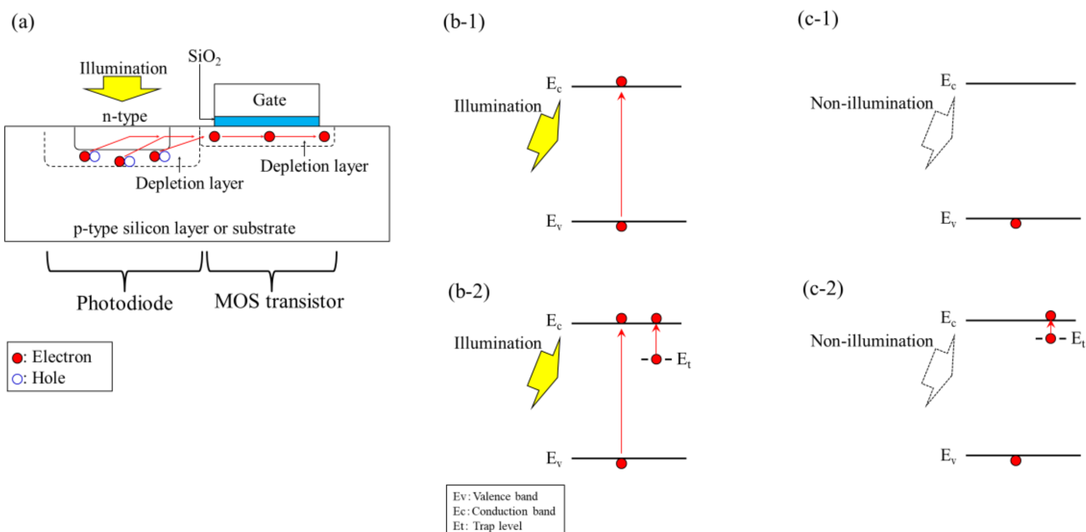
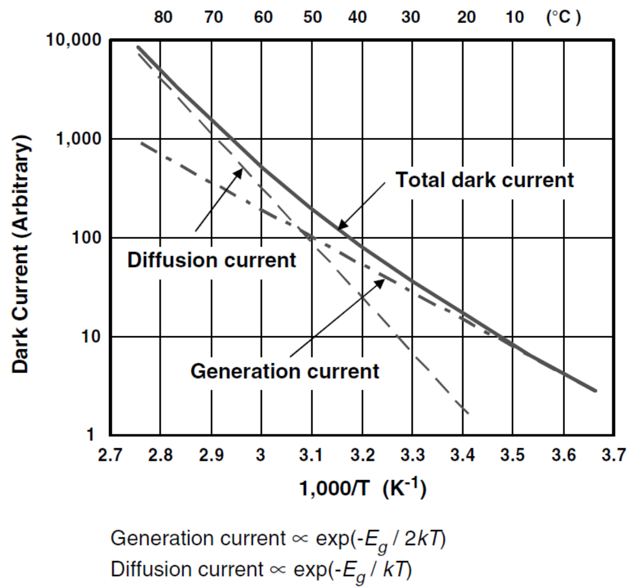


Fig. 1.3. Operation principle of imaging sensor.



Generation current ∝ $\exp(-E_g / 2kT)$
Diffusion current ∝ $\exp(-E_g / kT)$

Fig. 1.4. Temperature dependence of dark current.[9)]

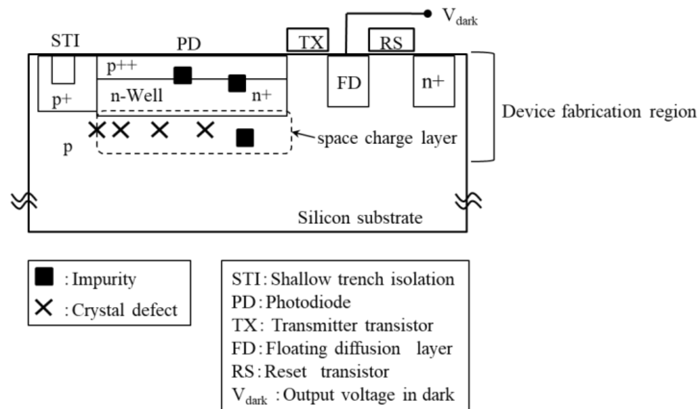


Fig. 1.5. Cross-sectional diagram of the imaging sensor for a security camera.

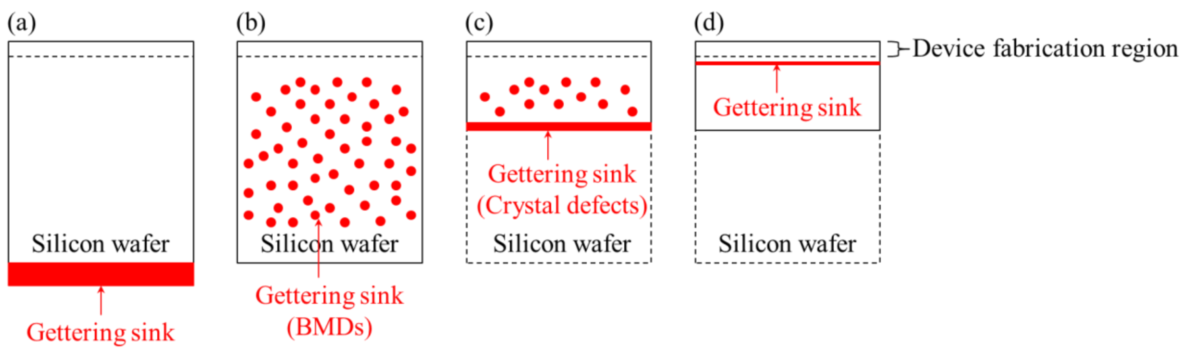


Fig. 1.6. Gettering technologies.

Since an imaging device changes light to an electric signal, it is most important to focus much light. The light is focused on the photodiode. Figure 1.7 (a) shows the CIS with front-side illumination (FSI). Since metal wiring reflects the illuminated light, it is difficult for this device to focus all the illuminated light. To resolve this issue, the light should be illuminated from the back of the silicon substrate to the photodiode while avoiding the metal wiring. Figure 1.7 (b) shows the CIS with back-side illumination (BSI).[17)] The silicon substrate is ground and polished from the back to the photodiode after fabricating devices in the silicon substrate. The device is then rotated, and the silicon substrate is bonded to another substrate. This structure for BSI has been produced in recent years. For this device, it is important to form a gettering sink near the device fabrication region. In addition, the wafer bonding technology that does not introduce impurities at low temperatures after fabricating devices is also important for this device.

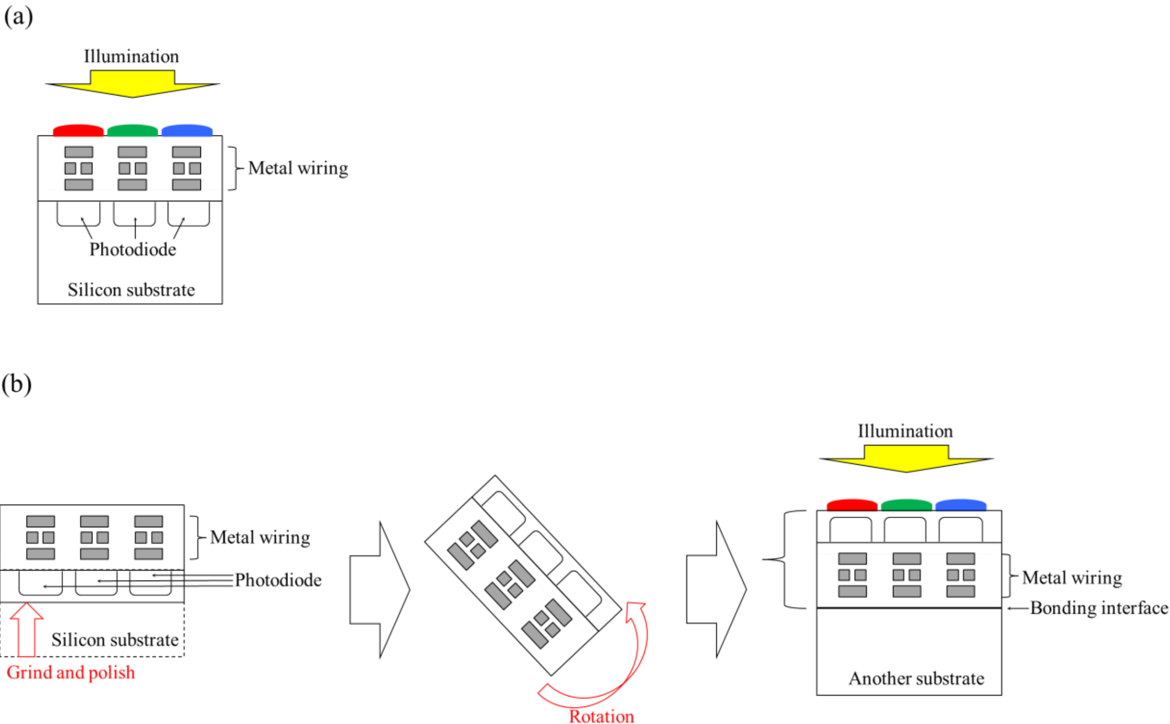


Fig. 1.7. CMOS image sensor technologies.

Micro-electromechanical systems (MEMS) move mechanically and can change this mechanical motion to an electrical signal, as shown in Fig. 1.8. Their sensors detect the movement of an object and change this mechanical motion to an electrical signal. Then, CMOS-FETs process this electrical signal and feed back the object information as an electrical signal or a mechanical motion. MEMS become especially important for automobile and smartphone applications.

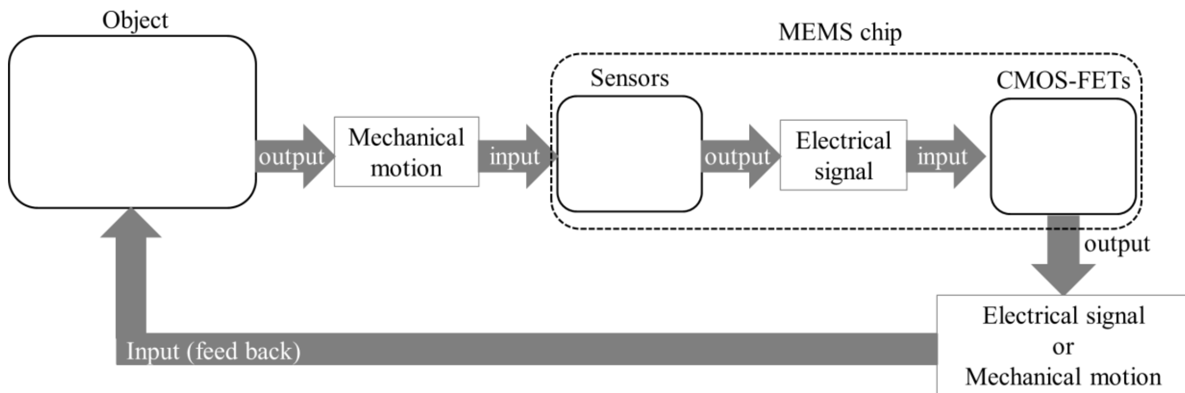


Fig. 1.8. Structure of MEMS.

Figure 1.9 shows the trend of MEMS. A cavity is formed in Substrate 1 in order for the pressure sensor to move vertically, and Substrate 1 is bonded onto another substrate (Substrate 2), as shown in Fig. 1.9 (a). The pressure sensor is bent by external pressure. Because sensors, such as an accelerometer and a gyro sensor, are highly sensitive, the structures of these sensors are complicated. These sensors are formed on silicon-on-insulator (SOI) wafers that have a SiO_2 layer called a buried oxide (BOX) layer, as shown in Fig. 1.9 (b).[18] Since the etching rate of the SiO_2 layer is different from that of a silicon layer, the complicated device patterns can be formed on this wafer by selective etching. The wafer bonding technology is also important for this device. In addition, a sensor is formed above a silicon substrate in order for the freedom of sensor design to be wide, as shown in Fig. 1.9 (c).[19] MEMS can be simply formed in an SOI wafer, as shown in Fig. 1.9 (b). However, because the process of fabricating an SOI wafer is carried out at a temperature above 800°C and requires a long time, the wafer has membrane stress around the BOX layer. Because the membrane stress consequently affects the MEMS on a cavity after etching the BOX layer, the membrane stress in the SOI wafer must be decreased. Since a silicon oxide layer on a silicon substrate has compression stress and a SiN layer on a silicon substrate has tensile stress, the use of the SiO_xN_y layer has been studied to decrease the membrane stress in the layer.[20] However, the etching rate of the SiO_xN_y layer in hydrofluoric acid (HF) could not be evaluated, and there will be a problem that the etching rate by HF is lower than that of a SiO_2 layer. In addition, in this method, it is difficult to balance compression and tension stresses by varying the x and y values, and the process cost is higher than that for a SiO_2 layer because a nitrogen-based gas must be added.

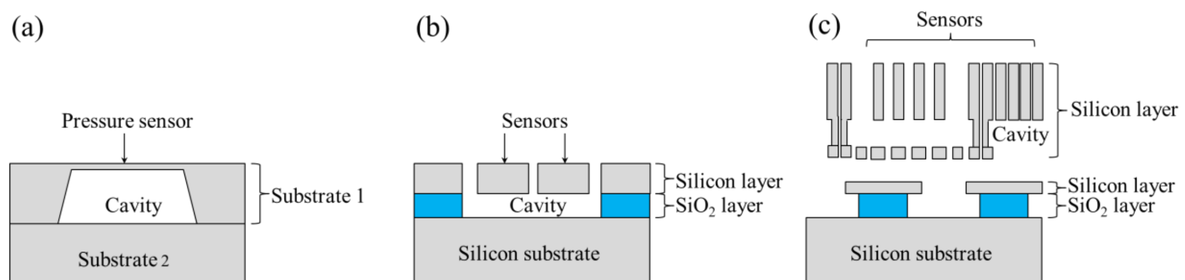


Fig. 1.9. MEMS technologies.

1.1.2 Power device technologies

In recent years, it has become especially important to counter environmental problems such as global warming and air pollution. Automobiles have been changing from gasoline cars to hybrid and fully electric cars, which contain various power devices.[21,22] Power devices are mounted in products powered by batteries. Figure 1.10 shows the power device technologies.[23] Power devices were first based on planar CMOS field-effect transistors (CMOS-FETs), as shown in Fig. 1.10 (a). This type of CMOS-FET has a long p-type (p^-) region between the gate and the drain to achieve a high breakdown voltage between the source and the drain. The area of this power device is large. Next, a vertical structure was suggested to solve this problem, as shown in Fig. 1.10 (b). Because the electrical current flows vertically, the breakdown voltage can be optimized by adjusting the thickness of the n-type region in the silicon substrate and the power device size can be further reduced. Subsequently, the gate was also formed vertically to further shrink the power device, as shown in Fig. 1.10 (c). The gate is formed as a trench structure, and the electrical current flows along the two sides of the trench gate. Finally, the electric current is speedily turned off by the annihilation of the bipolar operation involving electrons and holes, allowing the speedy operation of the power device, as shown in Fig. 1.10 (d). This device is called an insulated gate bipolar transistor (IGBT). The p-type (p^+) region is formed under the n-type (n^+) region and injects holes into the n-type region. The electrons emitted from the n^+-region of the emitter are recombined with the holes injected from the p^+-region of the corrector; consequently, the electrons do not reach the back of the wafer substrate, causing this device to speedily turn off.

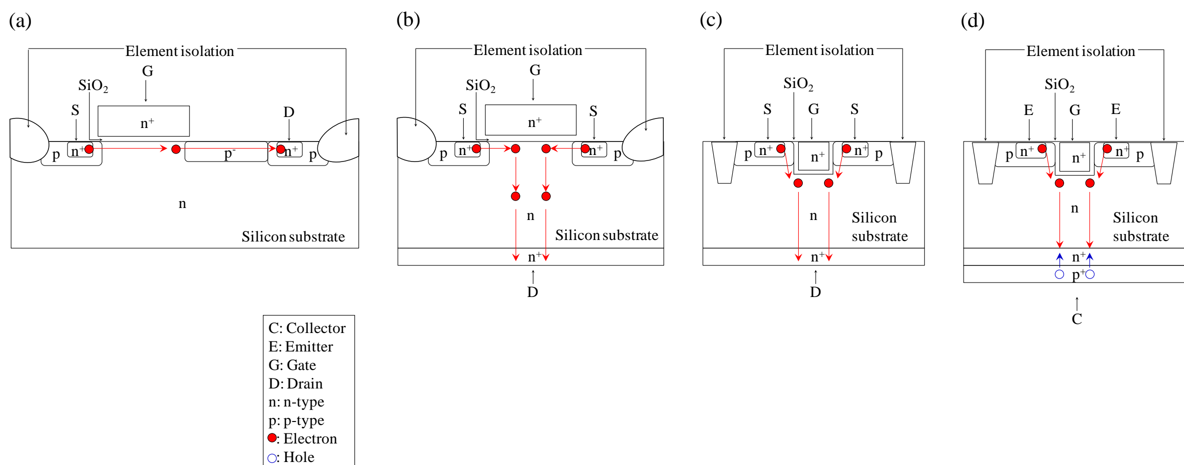


Fig. 1.10. Power device technologies.

Figure 1.11 shows a cross-sectional diagram of power devices fabricated on a silicon wafer. Devices 1, 2, and 3 are surrounded by electrical isolation regions. When the isolation regions are formed by a pn junction, boron and phosphorus are implanted into the silicon wafer to dope carriers of p-type and n-type in the isolation region. After such implantation, annealing is carried out to recrystallize the silicon wafer to repair the damage generated by implantation and to electrically activate the implanted boron and phosphorus. However, because the implanted silicon wafer cannot be perfectly recrystallized, the implanted elements cannot perfectly activate electrically. In result, a leakage current generates between the devices through the pn junction at high temperatures and votages.[24,25] Thus, such isolation is not useful for conventional power devices. The most efficient way to decrease the leakage current through an isolation region without the damage caused by implantation is to replace the pn junction with silicon dioxide (SiO_2).[26–31] Therefore, it is important to know how to form electrical isolation regions to decrease the leakage current to fabricate power devices in

a silicon wafer.

To realize convenience and comfort, Internet of things (IoT) is desired to connect wireless communication products such as smartphones, tablets, high-definition multimedia interfaces, automobiles, and robots.[32–34] Since RF devices have been widely used in wireless communication applications, it will be necessary, in these applications, to send larger amounts of data-to-data centers in the future. Since RF devices are high-frequency devices, they must operate at high speeds. In addition, since wireless communication applications are powered by batteries, RF devices must also operate at low powers. Therefore, it is also important to know how to form electrical isolation regions to decrease the leakage current to fabricate RF devices in a silicon wafer.

When electrical isolation regions are formed in SiO_2 without a pn junction, isolation region 1 is formed between devices by shallow trench isolation (STI), as shown in Fig. 1.11.[35] However, when devices are formed in a silicon wafer, isolation region 2 shown in Fig. 1.11 must still be formed using a pn junction. To form this pn junction, boron or phosphorus must be implanted deeply using high energy. This high-energy implantation generates many end-of-range (EOR) defects around the implantation region, and the generated defects cannot be perfectly recrystallized by heat treatment.[36–39] Consequently, an electric current flows from devices to the silicon wafer through the defects remaining in the pn junction. In addition, an electric current also flows from one device to other devices through the pn junction and silicon substrate. To resolve this issue, SOI wafers have been used to fabricate devices.[40,41] Figure 1.12 (a) shows a cross-sectional image of an SOI wafer. This wafer has a SiO_2 (BOX) layer as the insulator layer in the wafer. This BOX layer replaces the pn junction as isolation region 2 in Fig. 1.11. Figure 1.12 (b) shows an SOI wafer containing isolation region 1 formed by STI.[35] The devices in an SOI wafer are completely surrounded by SiO_2, which makes up a BOX layer and an STI region. The BOX layer is formed by thermal oxidation. Because the BOX layer formed by thermal oxidation has a fixed charge, the resistivity in the silicon layer on the BOX layer changes.[42–44] The electrical characteristics such as leakage current and subthreshold voltage degrade when the resistivity in the silicon layer changes. Thus, for the devices formed on the SOI wafer, it is important that the resistivity in the silicon layer in which the devices are fabricated is constant. However, in the SOI wafer, whether or not the resistivity in the silicon layer is constant has not yet been studied.[45–47]

Because it takes more than one day to fabricate the SOI wafer at a high temperature such as 800°C, the SOI wafer is contaminated by metallic impurities during the formation of the BOX layer and the bonding of the silicon layer to the BOX layer.[48–52] Because it is also important to reduce the number of metallic impurities introduced during the fabrication of the SOI wafer, the metallic parts of heat treatment devices have been coated with carbon. However, this method has had a limited effect in reducing the amount of contaminated metallic impurities. The fabrication process must be performed by other methods involving low temperatures and short processing times.

On the other hand, the length of their devices is shrunk to increase their productivity of the devices. As the current is increased by shrinking the device length, the electrical energy of the device consequently increases, which ultimately increases the heat generation of the device. Thus, for the devices formed on the SOI wafer, it becomes important to release the heat generated near them. However, no SOI wafer with thermal conductivity has been fabricated.[45–47] Therefore, the SOI wafer has at least three issues to be resolved: reduction in fixed charge in a BOX layer, reduction in wafer fabrication process time, and achieving the thermal conductivity of the BOX layer.

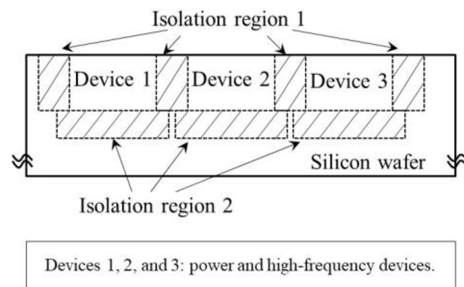


Fig. 1.11. Cross-sectional diagram of power and high-frequency devices fabricated on a silicon wafer.

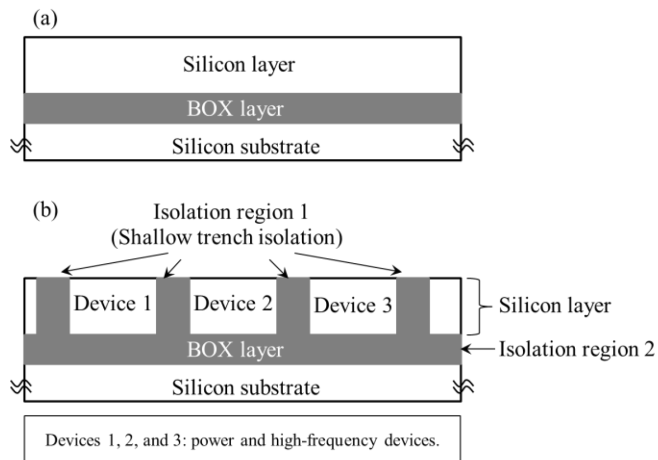


Fig. 1.12. Cross-sectional diagram of SOI wafer fabricated for producing devices.

1.2 Wafer bonding technologies

Wafer bonding is one of the important processes for fabricating a bonding wafer. Table 1-I shows the bonding technologies that have been used for fabricating semiconductor chips, modules, and wafers.

Thermocompression bonding is the bonding technology wherein two metal layers are bonded by the mutual diffusion of metal elements upon compression and heating at 200–400°C and has been used to bond metal substrates.[53)] In atomic diffusion binding, two substrates are deposited with thin metal layers in a vacuum and then bonded by the atomic diffusion of the deposited metal at room temperature. This has been used for packaging chips in three dimensions.[54)] In anodic bonding, two substrates are heated at 250–500°C by coulomb power by applying a voltage between substrates. This technology has been used for MEMS fabrication.[55)] Fusion bonding is a bonding technology in which OH groups are formed on the substrate surface to prebind them; then, H_2O is vaporized from the bonding interface by heat treatment at 150–1200°C. This method has been used in SOI wafer fabrication.[56)]

Surface-activated bonding (SAB) directly bonds two substrates at a temperature lower than 150°C in an ultrahigh vacuum, as shown in Fig. 1.13.[57,58)] Substrates such as semiconductors and metals can be bonded. Substrates 1 and 2 are irradiated with argon ions to remove impurities and the native oxide layer on their top surfaces in an ultrahigh vacuum of less than 1×10^{-5} Pa, as shown in Fig. 13 (a). Then, dangling bonds are formed at their top surfaces, as shown in Fig. 13 (b). Next, the surface of Substrate 2 is brought into contact with that of Substrate 1 in an ultrahigh vacuum. Consequently, the dangling bonds of Substrate 1 are strongly connected to those of Substrate 2. Because this bonding process can be carried out at a temperature lower than 150°C, bonding is possible even if the thermal conductivities of the two substrates are different. In addition, the wafers fabricated into devices, such as memory, power, CIS, and MEMS devices, can also be bonded without heat treatment.

The wafer to be boned (bonding wafer) might be contaminated with metallic impurities when using thermocompression bonding, atomic diffusion binding, or anodic bonding. On the other hand, the bonding wafer has thermal stress when using fusion bonding. These cause problems in the wafer fabrication process. The bonding of the wafer for device fabrication has mainly been carried out in two steps. In the first step, the bonded wafer is temporarily bonded at a low temperature. Then, in the second step, the bonded wafer is strongly bonded at a high temperature over a long time without the peeling of the wafer bonded on the substrate during wafer fabrication processes such as grinding and polishing. Figure 1.14 shows the time sequence of the heat treatment in the fabrication of the SOI wafer by fusion bonding and device fabrication.[47)] Two wafers (bonded and base wafers) are weakly bonded at temperatures below 600°C in the first step (Step 1) during the wafer fabrication process. Then, in the second step (Step 2), bonding above 800°C for a few hours can strongly bond the two wafers without the peeling of the wafer bonded on the substrate during wafer fabrication processes such as grinding and polishing. On the other hand, the device fabrication process also includes heat treatment as gate oxidation or drive-in heat treatment for diffusing doped elements into a silicon substrate such as wafer bonding above 800°C. If the bonding wafer can be bonded below 800°C and ground without the peeling of the wafer bonded on the substrate, because the bonding wafer is strongly bonded during the device fabrication process above 800°C, the long, high-temperature bonding process might not be necessary. Thus, it is preferable to use SAB to bond wafers for fabricating semiconductors above 800°C without the contamination of metallic impurities or thermal stress.

Table 1-I. Bonding technologies.

Method	Bonding substrate	Temperature
Thermocompression bonding	Metal	200–400°C
Atomic diffusion bonding	Semiconductor Glass	RT
Anodic bonding	Semiconductor Metal Glass	250–500°C
Fusion	Semiconductor SiO_2	150–1200°C
Surface activated bonding	Semiconductor Metal	RT–150°C

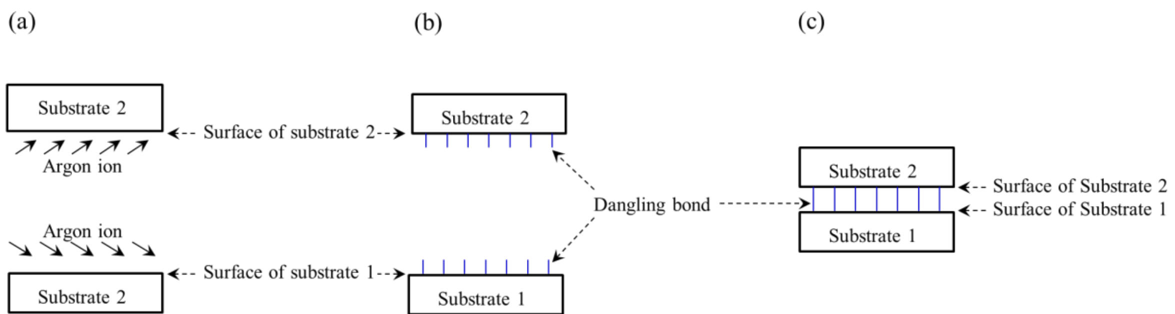


Fig. 1.13. Surface-activated bonding.

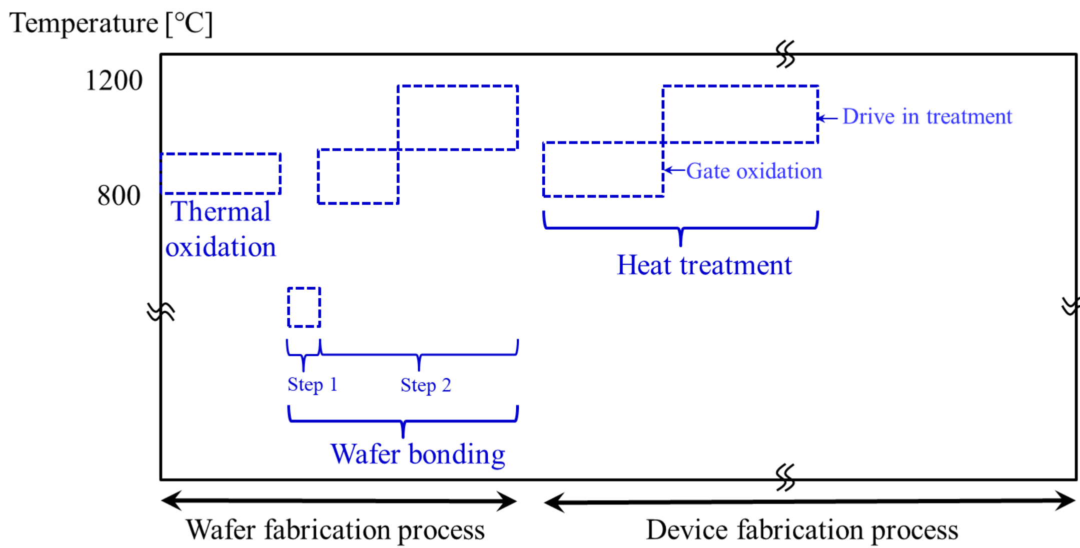


Fig. 1.14. Time sequence of heat treatment in wafer and device fabrications.

1.3 Purpose of this research

Wafers for sensors and power devices have some issues that have not yet been resolved, as presented in Section 1.2. In Chapter 2, the silicon bonded to silicon wafers with a gettering capability of more than 1×10^{13} atoms/cm^2 and an oxygen concentration of less than 1×10^{17} atoms/cm^3 are presented to decrease the generation current of the high-sensitivity CIS. In Chapter 3, SOI wafers with no fixed charge in the BOX layer and a low membrane stress for use in power and MEMS device fabrication are discussed. In Chapter 4, SOI wafers with a thermal conduction layer instead of a SiO_2 layer to inhibit the self-heating of devices surrounded by silicon oxide layers are presented. In this research, bonding was carried out by SAB in an ultrahigh vacuum at a room temperature in order for the wafer not to be contaminated by metallic impurities and to have as little thermal stress as possible during wafer bonding. Finally, Chapter 5 is a summary of the results of these studies.

Chapter 2 Silicon bonded to silicon wafers with low oxygen concentration and high gettering capability

2.1 Introduction

Imaging devices have been widely used in applications such as digital cameras, security cameras, and anticollision sensors, as presented in Section 1.1, and their performance has been continuously improving. Since IR light is less diffused in the air than other types of light, IR light has a higher straightness than other types of light. Thus, IR light is best for reaching an object a few tens of meters away and being reflected from it; consequently, anticollision sensors such as a light detection and ranging (LiDAR) system use IR light detectors.[59] Since IR light is easily transmitted through a silicon crystal,[60] the silicon crystal in a sensor for detecting IR light must be more than a few tens of micrometers in size. Thus, the image sensor for anticollision sensors comprises an avalanche photodiode (APD) that can be formed vertically and deeply in a silicon substrate.[61] Figure 2.1 shows an anticollision sensor with an APD in the silicon substrate. Electrons and holes are generated in a silicon substrate by IR light radiation. Then, they are accelerated by an electric field between the surface and back of the silicon substrate, and an avalanche phenomenon of electrons and holes consequently occurs. Thus, the APD can detect the irradiated IR light with high sensitivity. Because the avalanche phenomenon of electrons and holes is the driving mechanism of this device, the region of device formation must have no crystal defects or impurities such as metal or oxygen.

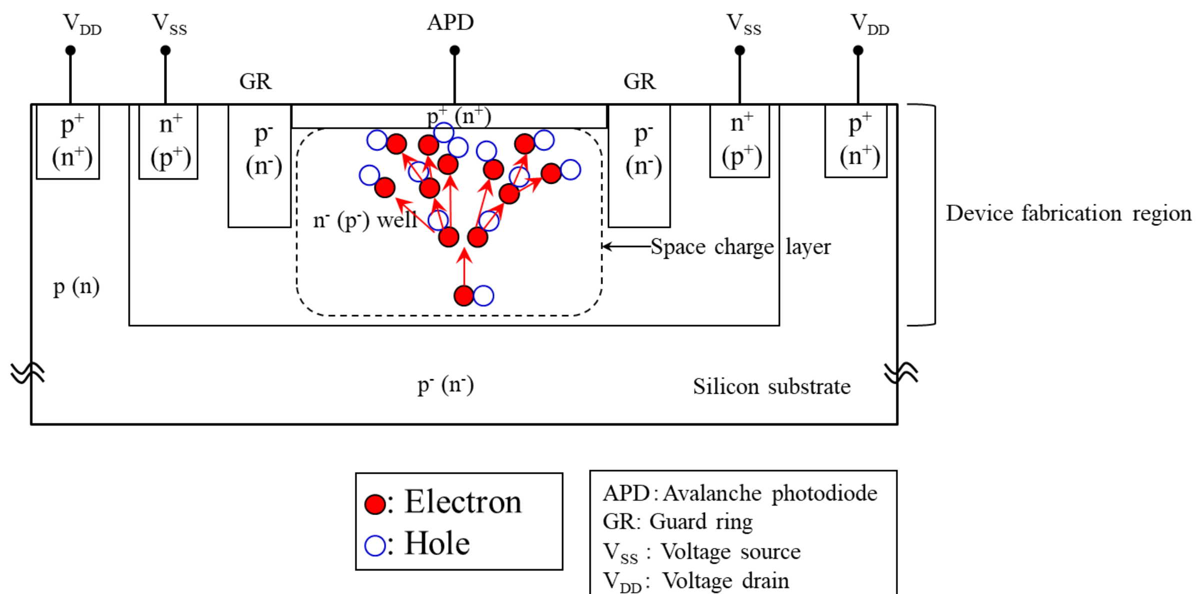


Fig. 2.1. Cross-sectional image of APD for anticollision sensor.

In the detection of IR radiation with a wavelength larger than 1120 nm in a silicon wafer, the thickness of the detection region must be greater than 100 μm. However, epitaxial silicon layer growth takes a long time, requiring more than 30 h at high temperatures above 1000°C to form an APD in an epitaxial layer on a silicon crystal substrate.[62] Consequently, the silicon substrate may be bent, have some slip, or be contaminated with metallic impurities from the equipment during the process of growing the epitaxial layer. In addition, oxygen dissolved in the silicon substrate diffuses out to the epitaxial layer during the growth process at high temperatures above 1000°C.[63,64]

Figure 2.2 shows a cross-sectional image of the chip with devices in the silicon wafer, fabricated for a LiDAR system. When CMOS-FETs and a detector (APD) are fabricated in a

silicon wafer, their size can be reduced and formed in a system on a chip (SoC).[65)]

Figure 2.3 shows the detailed cross-sectional structure of the detector region fabricated in an epitaxial wafer. Because the image sensor must be supersensitive to IR radiation, which is easily transmitted through the silicon wafer, the sensor is made of an APD formed vertically and deeply.[61)] When metallic impurities contaminate in the epitaxial layer, they form deep energy levels in the contaminated region.[66,67)] These deep energy levels act as generation or recombination centers, which mostly affect the electrical characteristics of the imaging sensor, such as dark current and white-spot defect density.[68,69)] Thus, they degrade the yield and reliability of the sensors. When oxygen diffuses out from the silicon substrate to the epitaxial layer after fabricating the devices, this oxygen also forms deep-level defects in the diffusion region.[70)] These oxygen-related defects cause an incomplete transfer of the electrical charges that accumulated in the APD when detecting IR radiation; consequently, fixed-pattern noise occurs in the detected signal.[71)] That is, these metallic impurities and oxygen-related defects strongly affect the performance of the LiDAR system. Therefore, the epitaxial layer on the silicon substrate should be grown at a low temperature to inhibit out-diffusion from the Czochralski-grown (CZ) silicon substrate to the epitaxial layer during its growth on the silicon substrate. Since epitaxial layers do not grow on the silicon crystal substrate below 900°C, a layer grown at less than 900°C is not epitaxial but polycrystalline or amorphous.[62)] There is a limit to the minimum temperature at which an epitaxial layer can be grown on the CZ silicon wafer substrate shown in Fig. 2.3. Kurita and his co-workers studied the epitaxial wafer with a gettering capability of less than 1×10^{13} atoms/cm^3 for high-sensibility cameras. In this wafer, less than 1×10^{18} atoms/cm^3 of oxygen diffused out from the silicon substrate to the epitaxial layer, which is the device fabrication region.[15,16)] However, the dark current for the high-sensibility cameras is still not low enough to use for night vision in security cameras and anticollision sensors. Thus, the generation current due to metallic impurities and oxygen in the device fabrication region, as mentioned in Chap. 1.1, must be reduced from that of the high-sensibility cameras, in order for CMOS image sensors to be used in high-sensibility security cameras and anticollision sensors.

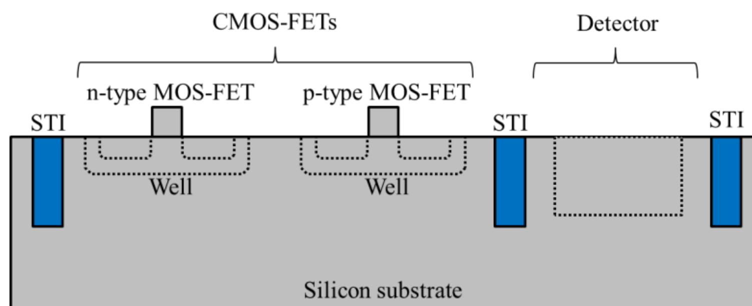


Fig. 2.2. Cross-sectional image of the chip with CMOS-FETs and detector.

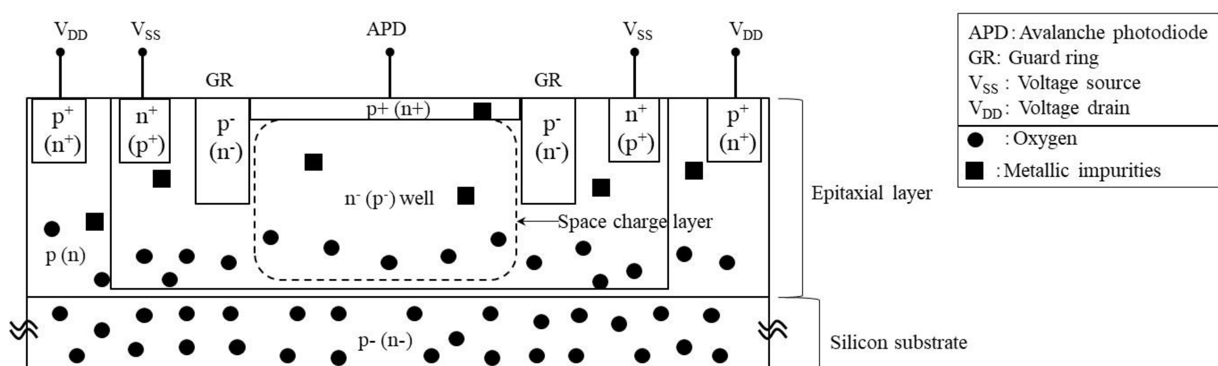


Fig. 2.3. Detailed cross-sectional structure of the detector region.

Figure 2.4 (a) shows the epitaxial wafer for CMOS imaging sensor devices. Because oxygen diffuses from the silicon substrate to the epitaxial layer [shown as the buffer layer in Fig. 2.4 (a)] during the growth of the epitaxial layer, an additional epitaxial layer must be grown. Oxygen also diffuses from the silicon substrate to the epitaxial layer during the heat treatment of the device fabrication process. Thus, it is difficult for the concentration of oxygen in the device fabrication region to be reduced after fabricating the devices. A strong gettering sink for oxygen must be formed directly below the device fabrication region in the epitaxial layer (directly above the buffer layer) to inhibit the diffusion of oxygen from the silicon substrate to the epitaxial layer.

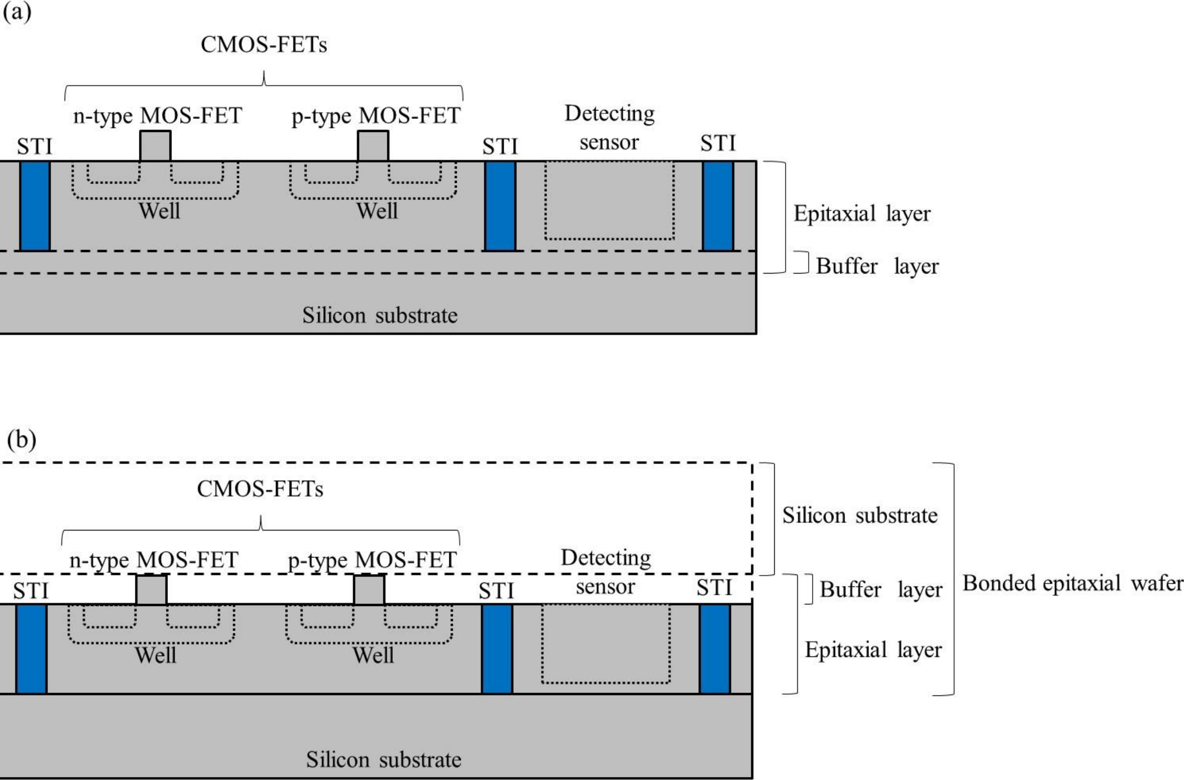


Fig. 2.4. Cross-sectional images of the chip formed in (a) epitaxial and (b) bonded epitaxial wafers.

2.2 Objectives

Security cameras and anticollision sensors must have a higher sensitivity than high-sensibility cameras, especially at night. For night vision, it is most important to decrease the dark current, as described in Chap. 1.1. There are typically more than 1×10^{17} atoms/cm^3 of oxygen in a CZ silicon substrate for a denuded zone-intrinsic gettering (DZ-IG) wafer or an epitaxial wafer; these oxygen atoms diffuse to the device fabrication region and consequently form defects in it during device fabrication. In addition, metallic impurities such as nickel, copper, and iron might also be introduced during the device fabrication processes. The gettering capability of the epitaxial or DZ-IG wafer for high-sensibility cameras is less than 1×10^{13} atoms/cm^3.

Since the wafer bonding region acts as a strong gettering sink[72)], a silicon layer was proposed to be directly bonded to a silicon substrate at room temperature by SAB. Two types of silicon-bonded wafer were studied to achieve a device fabrication region with less than 1×10^{17} atoms/cm^3 of oxygen and a gettering capability exceeding 1×10^{13} atoms/cm^2 for nickel, copper, and iron. One type comprises an epitaxial wafer bonded to the silicon substrate with molecular ion implantation and is applied to security cameras using FSI that is less than 15 µm thickness of the device region (Chapter 2.3). Since it is difficult to grow an epitaxial layer that is thicker than 100 µm on a silicon substrate, the second type comprises an FZ wafer bonded to a CZ wafer and is applied to anticollision sensors with an APD that is thicker than 100 µm (Chapter 2.4).

2.3 Silicon epitaxial layer bonded to silicon wafer with molecular-ion-implanted layer

2.3.1 Experimental methods

The fabrication process for this epitaxial-layer-bonded wafer is illustrated in Fig. 2.5. C_3H_5 ions were implanted into a base wafer at a high dose using a molecular ion implanter (Nissin Ion Equipment Co., Ltd., CLARIS).[73,74] C_3H_5 was used because carbon can form a gettering sink in silicon crystals.[75–77] The epitaxial layer was grown on the bonding wafer, which was a CZ silicon substrate.

The bonding wafer grown the epitaxial layer was then bonded to the base wafer implanted molecular ions in an ultrahigh vacuum at room temperature (EVG 580 ComBond/MWB-08-ST). Because it is not necessary to grow an epitaxial layer on a molecular-ion-implanted wafer, it is possible to implant a silicon substrate at a high dose to generate an amorphous layer in the ion-implanted region. It is also not necessary to recrystallize an amorphous layer generated by implantation at a high dose.

After bonding the two wafers, the bonding wafer was ground and polished down to the epitaxial layer formed at the back, which is opposite the wafer-bonding region. By these steps, an epitaxial layer on an amorphous layer generated by implantation at a high dose can be obtained. For the epitaxial layer deposition on a silicon substrate with ion implantation, because the epitaxial layer cannot grow on an amorphous layer, the generated defect density during the deposition of the epitaxial layer is in a trade-off relationship with the ion implantation dose or energy. Because the developed combination fabrication process does not grow an epitaxial layer on a molecular-ion-implanted wafer, there is no limitation regarding the dose or energy.

Table 2-I lists the conditions in experiments using 200-mm-diameter wafers polished to a thickness of 725 μm. These wafers were made of (100) phosphorus-doped CZ silicon single crystals. Their resistivity was 10 Ω·cm and their oxygen concentration was 0.8×10^{18} atoms/cm^3. As shown in Fig. 2.5, the base substrate wafer was implanted from the surface with C_3H_5 ions at 80 keV at a dose of 1×10^{16} atoms/cm^2. The bonding wafer was grown on an epitaxial layer of 8 μm thickness using a Si_3HCl gas source at 1100°C. These two wafers were bonded by SAB in an ultrahigh vacuum of less than 1×10^{-5} Pa at room temperature. Dangling bonds were formed on the top surfaces of the two wafers by irradiating argon ions at 1–2 keV to activate the surfaces. After bonding the two wafers, the bonding wafer was ground and polished to the 4-μm-thick epitaxial layer formed at the back, which is opposite the wafer-bonding region. A reference sample was fabricated by growing an epitaxial layer of 4 μm thickness on a silicon substrate without molecular implantation.

As shown in Fig. 2.6, the existence of voids after bonding the epitaxial layer to the silicon substrate with molecular ion implantation was investigated by an infrared-transmission observation method to evaluate the quality of the epitaxial layer [step (a)]. Then, the depth profile of oxygen was evaluated by SIMS analysis [(step (b)] and the bonding interface was observed after heat treatment, such as that during device fabrication, by cross-sectional TEM observation [step (c)]. Next, the capability of gettering to remove transition metals was evaluated by SIMS analysis after actual device fabrication [step (d)]. Finally, the depth profile of carbon was evaluated by SIMS analysis [step (e)].

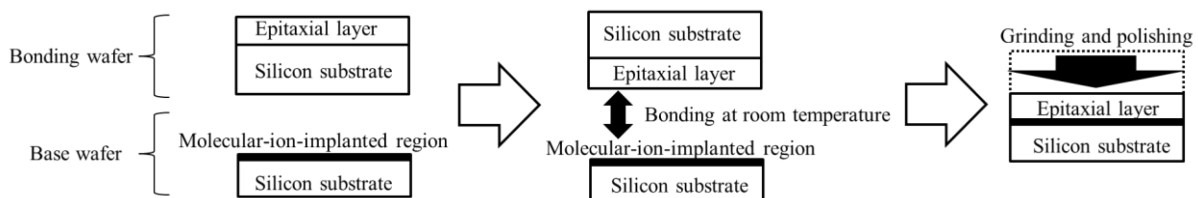


Fig. 2.5. Fabrication flow of the studied bonding wafer.

Table 2- I. Specifications of work samples.

Studied sample	
Substrate wafer	Bonding wafer
silicon wafer n-type 10 Ω·cm Oi: 0.8 $\times 10^{18}$ atoms/cm^3 200 mm diameter	silicon wafer n-type 10 Ω·cm Oi: 0.8 $\times 10^{18}$ atoms/cm^3 200 mm diameter
carbon-cluster ion implantation condition Ion element: C_3H_5 Enargy: 80 keV Dose: 1 $\times 10^{16}$ atoms/cm^2	epitaxial layer n-type 60 Ω·cm 8 μm
Reference sample (Epitaxial wafer)	
silicon wafer n-type 10 Ω·cm Oi: 0.8 $\times 10^{18}$ atoms/cm^3 200 mm diameter	epitaxial layer n-type 60 Ω·cm 4 μm

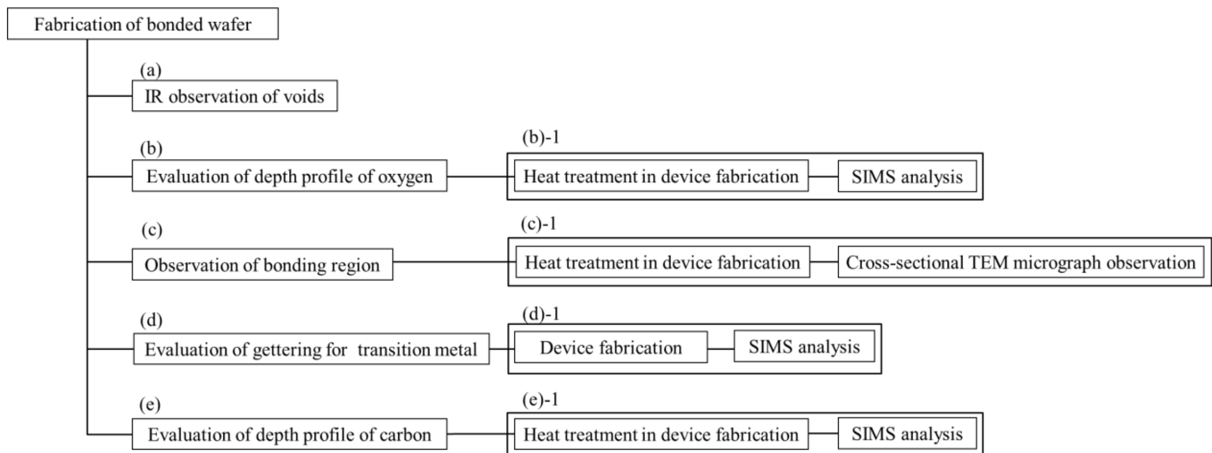


Fig. 2.6. Flowchart of the experiment.

2.3.2 Experimental results

2.3.2.1 Evaluation of voids formed during bonding of epitaxial layer to molecular-ion-implanted silicon substrate in ultrahigh vacuum at room temperature

Figure 2.7 shows the result of infrared-transmission observation of a 200-mm-diameter sample after bonding the epitaxial layer to the silicon substrate implanted with molecular ions at room temperature under 1×10^{-5} Pa. There were no voids in the wafer. The epitaxial layer was successfully bonded to the silicon substrate with high-dose molecular ion implantation (dose: 1×10^{16} atoms/cm^2) in an high vacuum at room temperature.

Because ion implantation knocks substitutional silicon ions into a silicon crystal, both vacancies and interstitial silicon are generated.[78–82] Consequently, high-dose implantation generates many defects of vacancies and interstitial silicon in the silicon crystal. Thus, it is difficult to grow an epitaxial layer with high-dose implantation on the silicon wafer surface. Although high-dose implantation (dose: 1×10^{16} atoms/cm^2) was performed at 80 keV, which is not a high ion-implantation energy, the room-temperature-bonded wafer did not have any extended defects or voids after bonding the two wafers (bonding and ion-implanted base wafers) nor were there any extended defects on the surface of the base wafer implanted with a high dose of molecular ions.

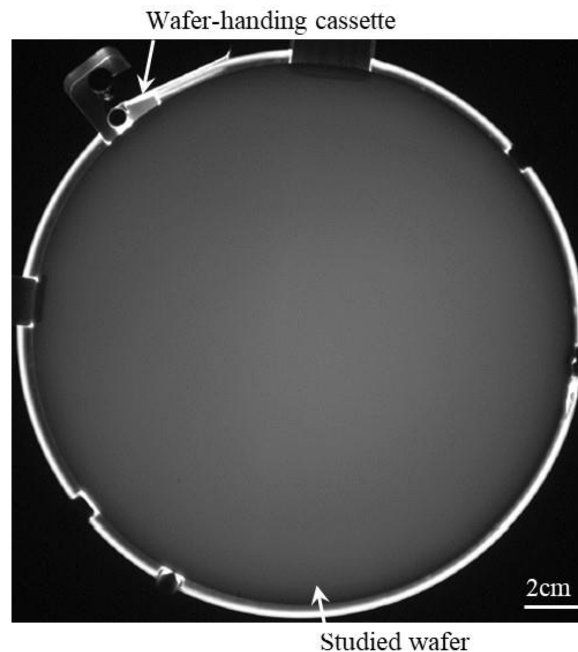


Fig. 2.7. Result of infrared transmission observation of 200-mm-diameter wafer after bonding of epitaxial layer at room temperature.

2.3.2.2 Depth profile of oxygen concentration after wafer fabrication and heat treatment

The depth profile of oxygen concentration was evaluated by the SIMS analysis of the samples with an epitaxial layer bonded to the silicon substrate implanted with molecular ions and a reference sample with an epitaxial wafer without molecular ions.

Figure 2.8 (a) shows the depth profile of the oxygen concentration after wafer fabrication, and Fig. 2.8 (b) illustrates that after heat treatment at 1100°C for 2 h in a nitrogen atmosphere, which are typical conditions of device fabrication. For the reference sample (epitaxial wafer), more than 1.0×10^{17} atoms/cm^3 of oxygen was detected in the epitaxial layer. Oxygen out-diffused to the epitaxial layer from the CZ silicon substrate during the growth of the epitaxial layer. On the other hand, for the room-temperature-SAB wafer, the concentration of oxygen in the epitaxial layer was less than 1.0×10^{17} atoms/cm^3. Because oxygen was out-diffused during the growth of the epitaxial layer, an additional 4-μm-thick epitaxial layer was grown to enable bonding to the silicon substrate. Thus, oxygen did not diffuse to the epitaxial layer from the CZ silicon substrate after wafer fabrication.

Furthermore, this room-temperature-bonded wafer contained a high concentration of oxygen (more than 3.0×10^{19} atoms/cm^3) between the epitaxial layer and the silicon substrate. On the silicon substrate and the epitaxial layer, oxygen from the native oxide on the silicon wafer surface was knocked into the silicon wafer bulk, when argon ions were irradiated onto the silicon wafer surface to activate surface bonding at both the base wafer and the epitaxial layer of the bonding wafer.[79,80,83)]

For the epitaxial wafer, the oxygen concentration at the surface increased by one order of magnitude from 3.5×10^{16} to 4.0×10^{17} atoms/cm^3 after heat treatment at 1100°C for 2 h, which are typical conditions of device fabrication. However, for the room-temperature-bonded wafer, the oxygen concentration of the epitaxial layer surface increased from 3.0×10^{16} to only 1.0×10^{17} atoms/cm^3 after heat treatment. Therefore, in the room-temperature-bonded wafer, the concentration of oxygen in the device fabrication region is reduced to less than 1×10^{17} atoms/cm^3 after wafer fabrication, which is less than that in the reference epitaxial wafer.

In addition, Figs. 2.9 (a) and 2.9 (b) show expanded depth profiles of the oxygen and carbon concentrations determined by SIMS analysis for the room-temperature-bonded wafer after wafer fabrication and the following heat treatment at 1100°C for 2 h in a nitrogen atmosphere, respectively. As illustrated in Fig. 2.9 (a), the oxygen concentration profile after wafer fabrication was symmetrical about the wafer-bonding region. Because oxygen is introduced from the native oxide on the silicon wafer into the silicon wafer bulk, that is, the silicon substrate and epitaxial layer, argon ions were irradiated onto the silicon wafer surface to activate the bonding surfaces of both the bonding wafer and the epitaxial layer of the base wafer. Additionally, there was a high concentration of carbon in the silicon substrate after wafer fabrication. This profile was in agreement with that of the molecular-ion-implanted sample in the experiment of Kurita and co-workers.[15,16)] During the fabrication of the room-temperature-bonded wafer, carbon was implanted into the base wafer. The epitaxial layer was then bonded on this implanted base wafer at room temperature. Thus, because the room-temperature-bonded wafer did not undergo any heat treatment after carbon was implanted into the base wafer, this profile result is reasonable.

As illustrated in Fig. 2.9 (b), the oxygen concentration profile after heat treatment was not symmetrical around the wafer-bonding region and was related to that of carbon distributed in the wafer-bonding and molecular-ion-implanted regions.

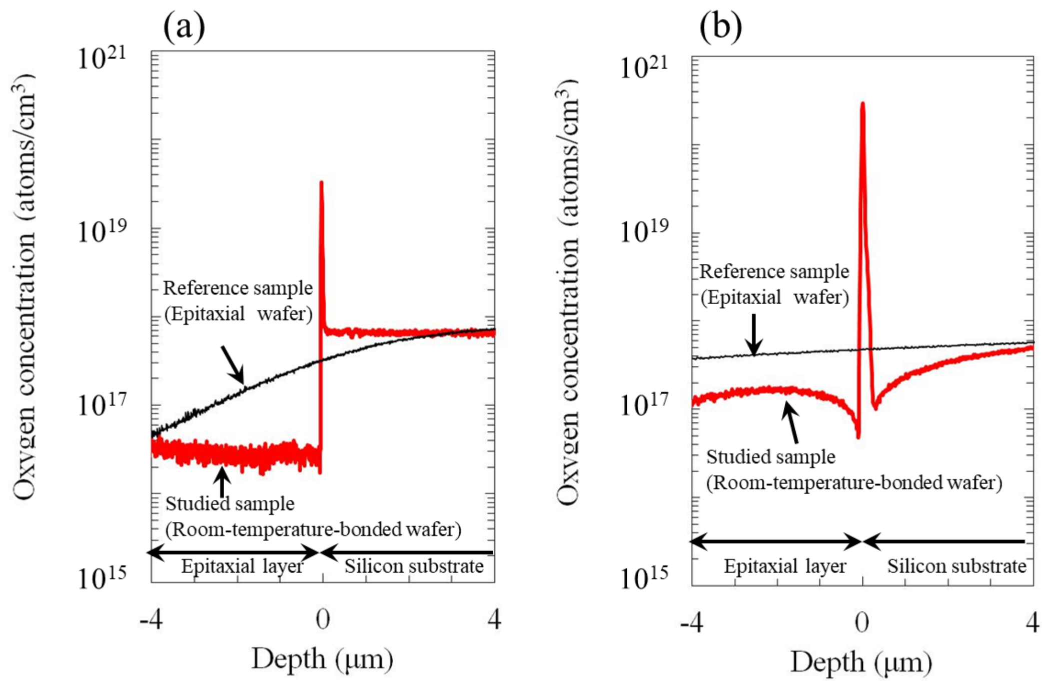


Fig. 2.8. Depth profiles of oxygen concentration measured by SIMS analysis.
(a) After fabrication of bonded wafer and (b) after heat treatment (1100°C for 2 h).

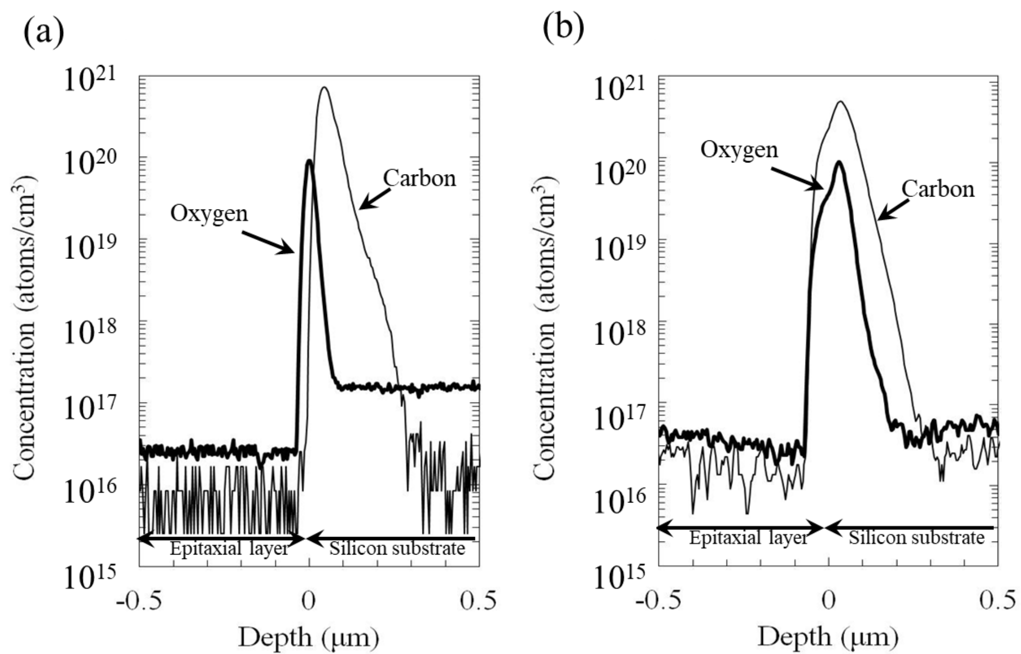


Fig. 2.9. Depth profiles of oxygen and carbon concentrations measured by SIMS analysis.
(a) After fabrication of bonding wafer and (b) after heat treatment (1100°C for 2 h).

2.3.2.3 Defects around bonding interface

Defects in this room-temperature-bonded wafer were observed near the wafer-bonding region by cross-sectional TEM. Figures 2.10 (a) and 2.10 (b) show cross-sectional TEM images of the room-temperature-bonded wafer after wafer fabrication and heat treatment (1100°C for 2 h), respectively. As shown in Fig. 2.10 (a), there was an amorphous layer in the wafer-bonding region between the epitaxial layer and the molecular-ion-implanted region of the CZ silicon substrate. The amorphous layer in the epitaxial layer was formed by argon-ion irradiation during SAB, and the amorphous layer in the CZ silicon substrate was formed by molecular ion implantation into the silicon substrate.

As illustrated in Fig. 2.10 (b), no defects expanded to the epitaxial layer from the bonding interface. The amorphous layers recrystallized during heat treatment (1100°C for 2 h), and two types of defect remained in these amorphous layer regions, namely, misfit dislocations in the wafer-bonding region between the epitaxial layer and the CZ-grown silicon substrate, and dots in the molecular-ion-implanted region in the CZ-grown silicon substrate. We call these dot defects black point defects.

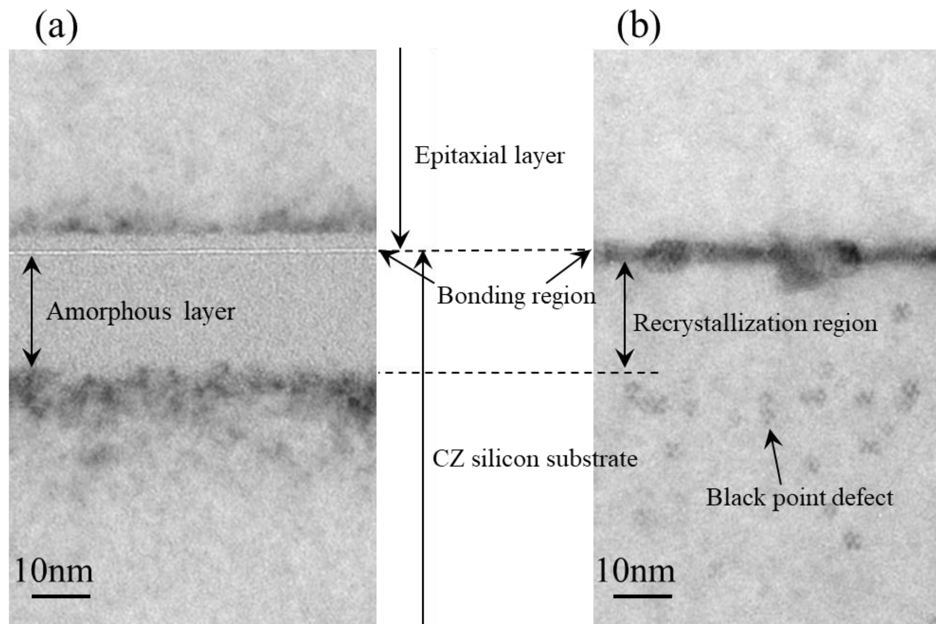


Fig. 2.10. Cross-sectional TEM images of bonded wafers with molecular ion implantation. (a) After fabrication of bonded wafer and (b) after heat treatment (1100°C for 2 h).

2.3.2.4 Transition-metallic-impurity gettering behaviors after actual device fabrication

Figure 2.11 shows the depth profiles of the concentrations per volume for nickel, copper, and iron obtained by SIMS analysis after actual device fabrication and the concentration per area on the room-temperature-bonded wafer after actual device fabrication obtained by integration. By integrating the concentration per volume in Fig. 2.11 to obtain the concentration per unit area, it was found that nickel, copper, and iron existed under the epitaxial layer at concentrations higher than 1×10^{14} atoms/cm^2 per unit area. Therefore, this room-temperature-bonded wafer has a gettering capability of more than 1×10^{14} atoms/cm^2.

In addition, Fig. 2.12 shows the expanded SIMS analysis results of the bonded wafer with molecular ion implantation after actual device fabrication, including the solid solubility of metallic impurities (nickel, copper, and iron) in the silicon crystal, as denoted by the dotted lines.[84)] The concentrations of these metallic impurities were above the solid solubility limit in the silicon crystal after actual device fabrication. These metallic impurities were distributed in the wafer-bonding interface and the molecular-ion-implanted region.

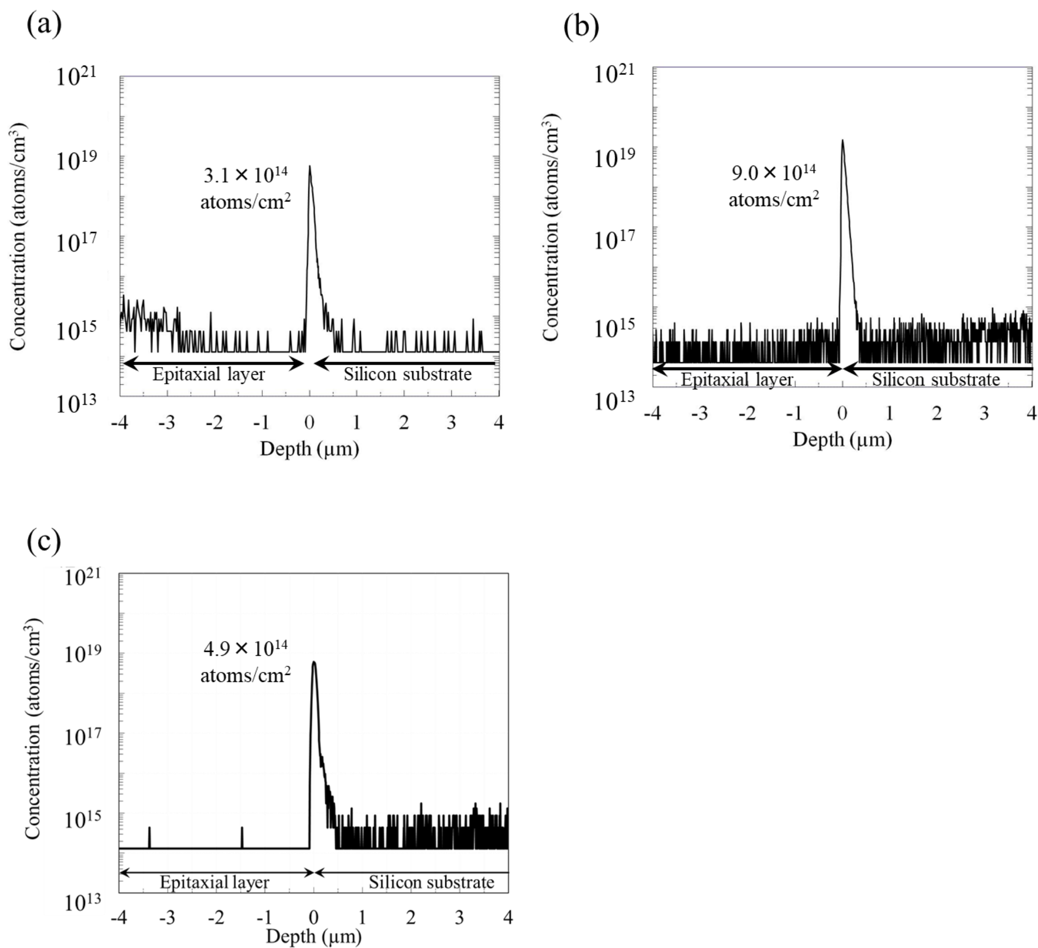


Fig. 2.11. Depth profiles of metallic impurity concentrations determined by SIMS analysis after actual device fabrication: (a) nickel, (b) copper, and (c) iron.

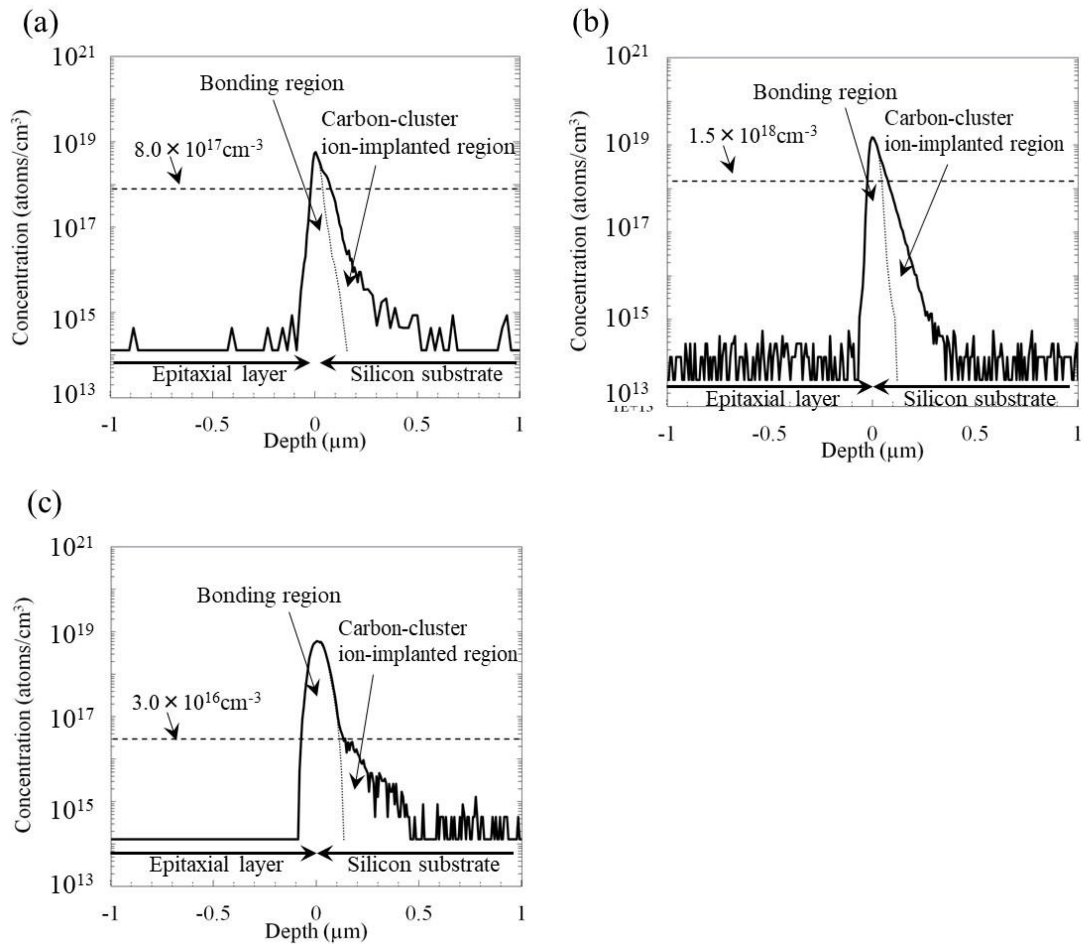


Fig. 2.12. Expanded depth profiles of metallic impurity concentration measured by SIMS analysis after actual device fabrication with solid solubility of metallic impurities: (a) nickel, (b) copper, and (c) iron.

2.3.3 Discussion

The two types of defect (misfit dislocations and black point defects) remaining in the amorphous region were assumed to act as gettering sinks for oxygen out-diffusing to the epitaxial layer from the silicon substrate, as shown in Fig. 2.8 (b). In general, a misfit dislocation acts as a gettering sink,[85)] and carbon can getter oxygen[75,76,86–88)].

According to Fig. 2.9 (b), because this high carbon concentration was above the solid solubility limit (3.3×10^{19} atoms/cm^3)[89)] in the silicon crystal after heat treatment, carbon existed not only at the substitutional site but also the interstitial site and precipitated into this region where the carbon concentration was above the solid solubility limit in the silicon crystal. Kurita and co-workers argued that black point defects in the molecular-ion-implanted region are composed of carbon that can getter oxygen;[15,16)] therefore, this room-temperature-bonded wafer, which also has black point defects, as shown in Fig. 2.10 (b), is considered to be able to getter oxygen. On the other hand, Yu et al. showed that the misfit defect at the wafer-bonding interface acts as a gettering sink,[90)] so my wafer-bonding region should also act as a gettering sink, as shown in Fig. 2.12. Therefore, because oxygen was gettered at misfit dislocations in the wafer-bonding interface and black point defects in the molecular-ion-implanted region, the concentration of oxygen in the epitaxial layer could also be decreased after heat treatment, for example, during device fabrication processes.

In general, there are two types of gettering sink: relaxation and segregation.[91,92)] For the relaxation type, because a gettering sink is effective only below the supersaturated solid solubility limit, the gettered-metal-impurity concentration is below the solid solubility limit in the silicon crystal. For the segregation type, because it is not always necessary for the atmosphere of a gettering sink to be below the supersaturated solid solubility limit, the gettered-metal-impurity concentration is above the solid solubility limit in the silicon crystal. Thus, a segregation-type gettering sink is more stable than a relaxation-type gettering sink in the silicon crystal regardless of the temperature. Because the concentrations of metallic impurities were determined above the solid solubility limit in the silicon crystal in the studied wafer after actual device fabrication, this wafer had at least one segregation-type gettering sink.

As seen in the cross-sectional TEM image [Fig. 2.10 (a)] taken after wafer fabrication, amorphous layers were formed in the bonding and molecular-ion-implanted regions. An amorphous layer generally acts as a gettering sink similarly to a polysilicon back seal.[93)] Thus, the amorphous layers in this bonding wafer act as segregation-type gettering sinks.

As shown in the cross-sectional TEM image [Fig. 2.10 (b)] taken after heat treatment in device fabrication, this bonding wafer had misfit dislocations in the wafer-bonding region and black point defects in the molecular-ion-implanted region. When a silicon wafer has misfit dislocations, impurities are captured around these dislocations in the silicon crystal. In accordance with the Cottrell effect, the solid solubility limit of the impurity increases to relieve the strain in the silicon crystal.[85,94)] This region near the dislocations acts as a segregation-type gettering sink.[85)] Yu et al. showed that copper segregated above the solid solubility limit in the wafer-bonding region after quenching the heat treatment temperature from 800°C to room temperature.[90)] Aucouturier et al. showed that copper segregated into twins after heat treatment at 700°C,[80)] and Maurice and Colliex showed that copper and iron segregated into grain boundaries after heat treatment at 900°C.[95)] Pizzini et al. showed that oxygen and carbon segregated near grain boundaries.[96)] In my bonded wafer, oxygen, carbon, and metallic impurities (nickel, copper, and iron) were segregated in the wafer-bonding region, as shown in Figs. 2.11 (b) and 2.12. Thus, my bonding wafer has a segregation-type gettering sink in the wafer-bonding region.

The molecular-ion-implanted region also captured metallic impurities (nickel, copper, and iron), which were at concentrations above the solid solubility limit in the silicon crystal, as illustrated in Fig. 2.12. As illustrated in Fig. 2.9, because the carbon concentration was

above the solid solubility limit (3.3×10^{19} atoms/cm^3) in the silicon crystal in the implanted region,[89)] carbon was located at substitutional sites (C_s) and interstitial sites (C_i) in this implanted region. Shirasawa et al. indicated that the binding energy of metallic impurities at C_i was higher than that of metallic impurities at C_s or O_i (oxygen located at the interstitial sites) in the silicon crystal.[97,98)] Thus, C_i in the ion-implanted region must act as the dominant and stable gettering sink in the silicon crystal. Because my bonded wafer captured nickel, copper, and iron, which were at concentrations above the solid solubility limit in the silicon crystal in the molecular-ion-implanted region, as illustrated in Fig. 2.12, C_i in this implanted region acted as a segregation-type gettering sink. Therefore, my bonding wafer has at least segregation-type gettering sinks in the wafer-bonding and molecular-ion-implantated regions, and a gettering capability exceeding 1×10^{14} atoms/cm^2.

2.3.4 Summary

The bonding characteristics and gettering performance for oxygen and metallic impurities in the case of an epitaxial layer bonded to a C_3H_5-ion-implanted silicon substrate were demonstrated for the first time. The epitaxial layer can be bonded to an amorphous layer of the silicon substrate with high-dose molecular ion implantation. The wafer has two gettering sinks in the wafer-bonding and molecular-ion-implanted regions for oxygen and metallic impurities. Consequently, the concentration of oxygen in the epitaxial layer was less than 1×10^{17} atoms/cm^3 after wafer fabrication, and the wafer had a gettering capability exceeding 1×10^{14} atoms/cm^2.

2.4 Floating-zone silicon wafer bonded to CZ silicon substrate

2.4.1 Experimental methods

Figure 2.13 shows the method of fabricating the bonded silicon wafer made of an active FZ wafer and a base CZ wafer. The active FZ and base CZ wafers were fabricated and bonded by SAB in an ultrahigh vacuum at room temperature to form a silicon layer in which devices are fabricated. After bonding the two wafers, the active FZ wafer was ground and polished from the back, which is the side opposite the bonding interface, to the desired thickness.

Table 2-II lists the characteristics of the 200-mm-diameter wafer that was polished to a silicon layer of 725 μm thickness. The active wafer was (100) phosphorus-doped FZ single-crystal silicon, and the base wafer was (100) phosphorus-doped CZ single-crystal silicon. The resistivities of the FZ and CZ wafers were 60 Ω·cm and 10 Ω·cm, and their oxygen concentrations were less than 0.1×10^{17} atoms/cm^3 and 8.0×10^{17} atoms/cm^3, respectively.

As shown in Fig. 2.13, the active FZ wafer was bonded by SAB to the base CZ wafer in an ultrahigh vacuum of less than 1×10^{-5} Pa at room temperature (Nidec Machine Tool Corporation, MWB-08-AX) to form the device-fabricating region. The top surfaces of these wafers were activated by argon-ion irradiation with argon ion energies of 1–2 keV for 3 min. After bonding the two wafers with a force of 100 kN, the active FZ wafer was ground from the back and polished to a thickness of 5 μm. A reference sample with an epitaxial layer grown on a CZ wafer was also prepared. This CZ wafer was (100) phosphorus-doped CZ single-crystal silicon. Its resistivity was 10 Ω·cm and its oxygen concentration was 3.0×10^{17} atoms/cm^3. The CZ wafer was grown on a 5-μm-thick n-type epitaxial layer using Si_3HCl and PH_3 gas sources at 1100°C.

As shown in Fig. 2.13, voids and defects were investigated after bonding the active FZ wafer to the base CZ wafer [steps (a) and (b)] and after the heat treatment in device fabrication [step (c)]. Figure 2.14 illustrates the heat treatment process in the fabrication of the APD. The heat treatment was carried out at above 900°C in nitrogen atmosphere, and the sample stage was loaded and unloaded at 900°C in ambient nitrogen gas in a furnace. Then, the concentration of oxygen in the bonded FZ wafer was evaluated after grinding and polishing to the thickness of the device-fabricating region and after the heat treatment in device fabrication [steps (d) and (e)]. In addition, the capability of gettering of transition metals was evaluated [steps (f) and (g)]. Finally, the characteristics of real devices were evaluated and the bonded wafer was studied after fabricating actual devices [steps (h), (i), (j), and (k)]. Figure 2.15 illustrates the process of fabricating the pn-junction diode as the basic device of the APD in order to understand the efficacy of the studied bonded wafer compared with that of the epitaxial wafer. Firstly, the protective oxide layer was formed on the surfaces of samples. Secondly, the p-type well was formed in the n-type layer by patterning using photolithography, boron implantation, and annealing at 900°C for 1 h after forming the protective oxide layer at 1050°C for 14 min. Thirdly, STI was formed by the photolithography, RIE, and embedding of SiO_2. Fourthly, the interlayer insulator was deposited on the surfaces of samples by CVD. Fifthly, a through-hole via was formed by photolithography and RIE. Then, the samples were implanted with boron and phosphorus and annealed at 900°C for 30 min for low resistance of the silicon layer. Finally, a metal connecter was formed by sputtering, photolithography, etching, and sintering at 400°C for 30 min. The diode fabrication was carried out between 400°C and 1050°C in oxygen or nitrogen atmosphere, and the sample stage was loaded and unloaded at 400°C when the heat treatment temperature was 400°C or at 900°C when the heat treatment temperature was above 900°C in ambient nitrogen gas in a furnace.

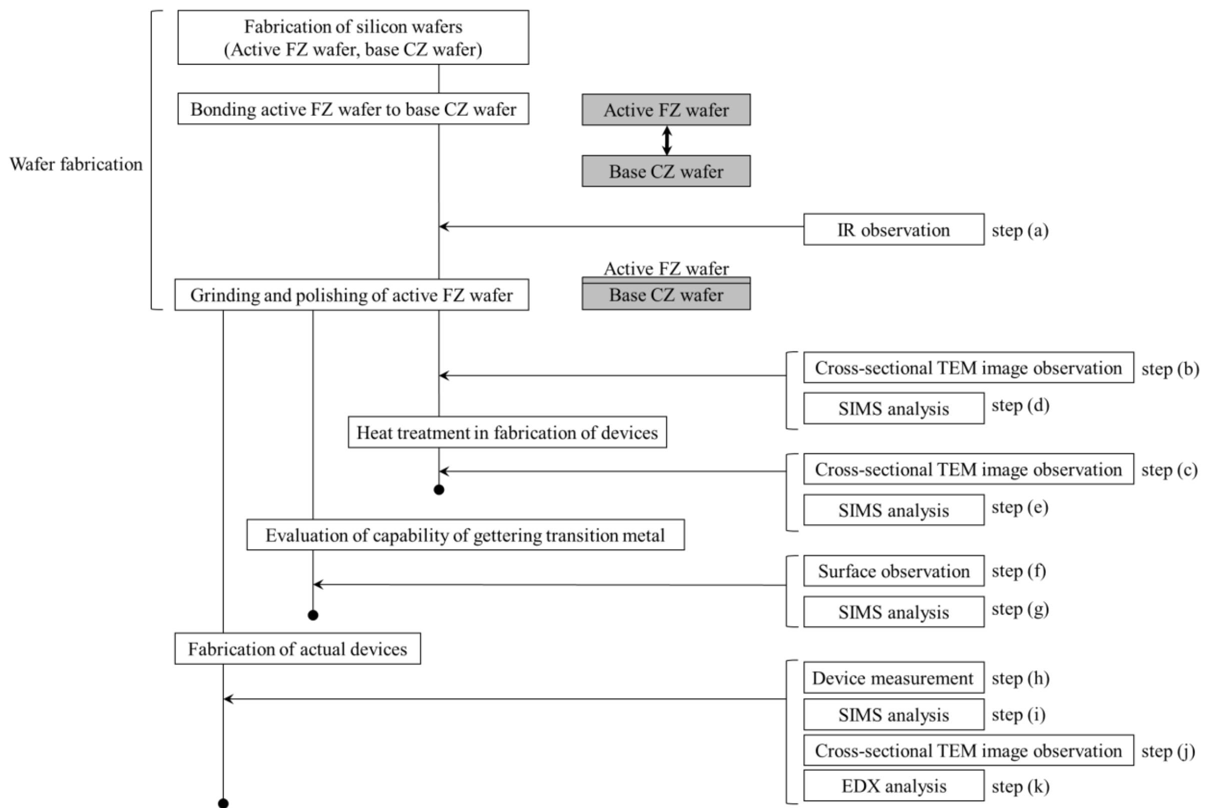


Fig. 2.13. Flowchart of experiment.

Table 2-II. Samples used in this study.

	Substrate wafer	Activate layer
Studied sample (Bonded wafer)	CZ-silicon wafer n-type (phosphorus-doped) 10 Ω·cm Oi: 8.0 $\times 10^{17}$ atoms/cm^3	Bonded FZ wafer n-type (phosphorus-doped) 60 Ω·cm Oi $\leqq$0.1 $\times 10^{17}$ atoms/cm^3
Reference sample (Epitaxial wafer)	CZ-silicon wafer n-type (phosphorus-doped) 10 Ω·cm Oi: 3.0 $\times 10^{17}$ atoms/cm^3	Epitaxial layer n-type (phosphorus-doped) 60 Ω·cm 5 μm

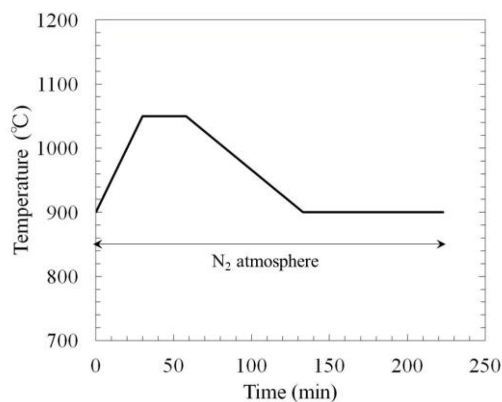


Fig. 2.14. Time sequence of heat treatment in device fabrication.

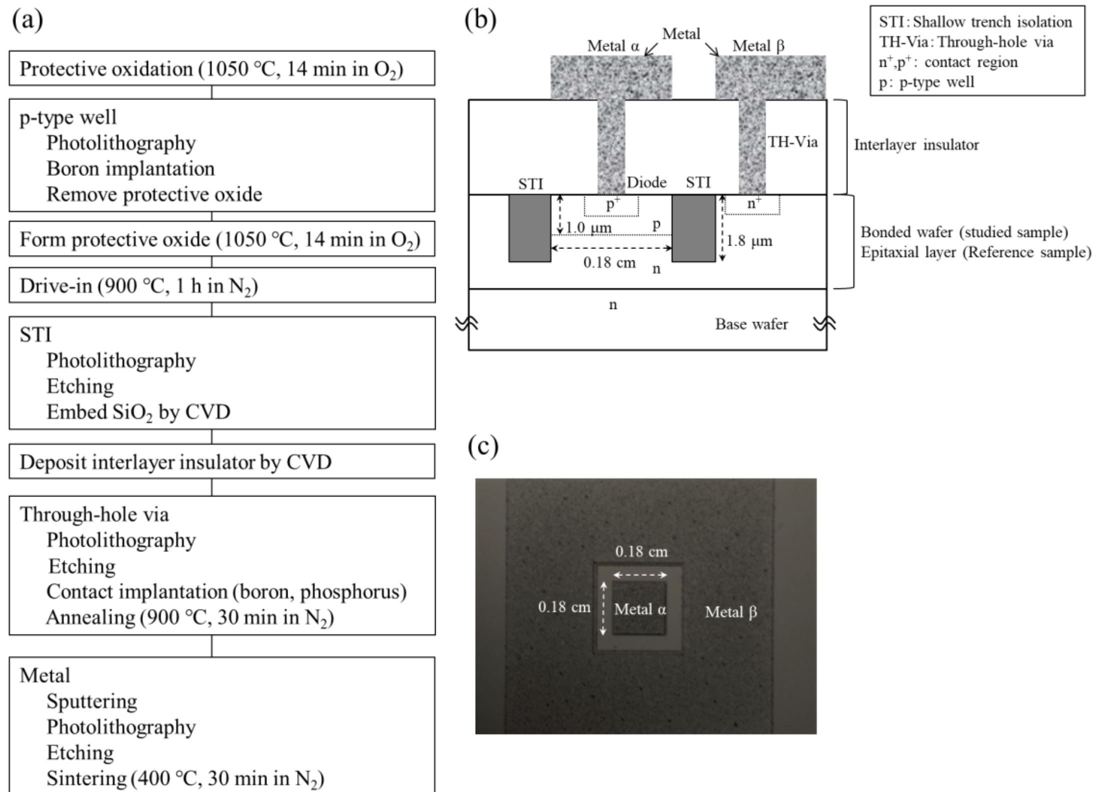


Fig. 2.15. Fabrication of device in silicon layer. (a) Device fabrication processes, (b) cross-sectional image of fabricated device, and (c) photograph of fabricated device.

2.4.2 Experimental results

2.4.2.1 Evaluation and observation of voids at bonding interface

Voids remaining at the bonding interface were evaluated by IR transmission imaging after the SAB of the FZ wafer to the CZ wafer at room temperature under a pressure of 1×10^{-5} Pa. Figure 2.16 shows an IR transmission image after SAB. The IR transmission image shows a lattice-like pattern. There are no defects in the bonding wafer. The 200-mm-diameter wafer sample does not have any voids.

The bonded interface was also observed on a cross-sectional TEM image of the chip obtained after dicing the bonded wafer at its center. Figure 2.17 (a) shows a cross-sectional HR-TEM image of the fabricated wafer. The bonding interface was flat and there were no microvoids at the bonding interface between the active FZ wafer and the base CZ wafer. Amorphous layers of 3 nm thickness were observed at the bonding interface of the active FZ and base CZ wafers.

The bonded interface on a cross-sectional TEM image was also observed to evaluate the thermal stability after the heat treatment in device fabrication shown in Fig. 2.14. The cross-sectional HR-TEM image in Fig. 2.17 (b) shows that the bonding interface was again flat and no new microvoids were generated at the bonding interface. No 6-nm-thick amorphous layer was observed in the bonding interface. The amorphous layer had recrystallized to a silicon crystal during the heat treatment. In addition, a white line, marked by red arrows, and strain regions, enclosed by blue dotted lines, were observed in the bonding interface. Because the amorphous layer was recrystallized in the bonding interface from a single-crystal region of the base CZ wafer toward the bonded FZ wafer, lattice mismatch occurred, and the strain was generated at the bonding interface.

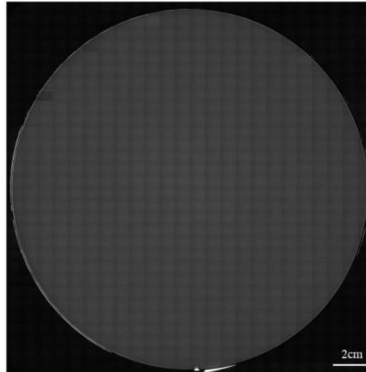


Fig. 2.16. IR transmission image of 200-mm-diameter wafer after bonding FZ wafer to CZ wafer.

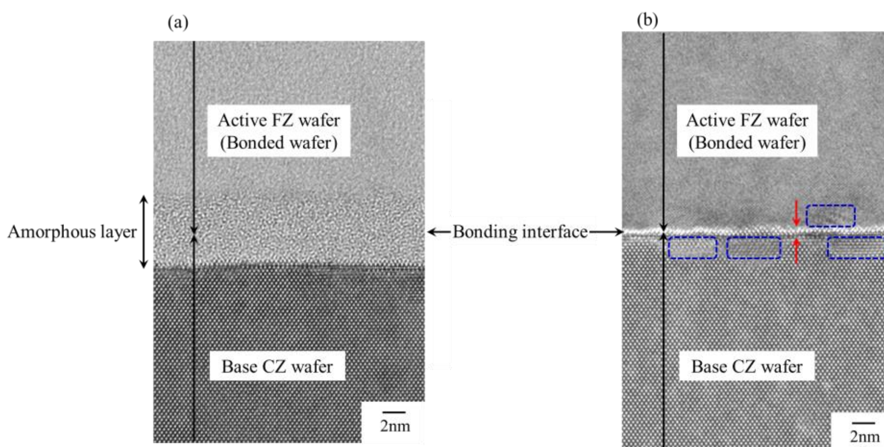


Fig. 2.17. Cross-sectional TEM images (a) after bonding FZ wafer to CZ wafer and (b) after heat treatment.

2.4.2.2 Depth profile of oxygen concentration

For the studied bonded and reference epitaxial wafers after wafer fabrication and heat treatment in device fabrication processes, the depth profiles of oxygen concentrations were evaluated by SIMS. Figures 2.18 (a) and 2.18 (b) respectively show the depth profiles of oxygen concentrations after wafer fabrication and heat treatment. The x-axis is the depth from the surfaces of samples, and the y-axis is the concentration of oxygen obtained by SIMS analysis. The detection limit of oxygen in SIMS is about 3×10^{16} atoms/cm^3.

Figure 2.18 (a-i) shows the results for the reference epitaxial wafer after wafer fabrication. The oxygen concentration was more than 1×10^{17} atoms/cm^3 at depths from 4 μm to 5 μm in the epitaxial layer. Figure 2.18 (a-ii) shows the results for the studied bonded wafer after wafer fabrication. The concentration of oxygen in the bonded FZ Si layer from the surface to the bonding interface is constant at 3×10^{16} atoms/cm^3, which is the detection limit of SIMS analysis. The concentration of oxygen in the region of the bonding interface near 5 μm is high, greater than 1×10^{20} atoms/cm^3. Oxygen was knocked into the surface of the silicon substrate during SAB and exists at a high concentration at the bonding interface.[63) The concentration of oxygen in the bonded FZ Si layer can be less than that in the epitaxial layer of the device fabrication region despite the silicon substrate containing a higher concentration of oxygen (8×10^{17} atoms/cm^3) than the silicon substrate of the epitaxial wafer (3×10^{17} atoms/cm^3).

Figure 2.18 (b) shows the depth profile of the oxygen concentration after the heat treatment in device fabrication shown in Fig. 2.14. Figure 2.18 (b-i) shows the results for the reference epitaxial wafer. The concentration of oxygen increased to a value above 1×10^{17} atoms/cm^3 at depths from 1 μm to 5 μm in the epitaxial layer after heat treatment. Compared with that before heat treatment shown in Fig. 2.18 (a-i), the region in which the oxygen concentration was greater than 1×10^{17} atoms/cm^3 expanded by 4 μm. On the other hand, Fig. 2.18 (b-ii) shows the results for the studied bonded wafer. The concentration of oxygen in the bonded FZ Si layer from the surface to the bonding interface after heat treatment was also constant at 3×10^{16} atoms/cm^3, which is the detection limit of SIMS analysis. Thus, the concentration of oxygen in the bonded FZ Si layer can be kept below 3×10^{16} atoms/cm^3 after heat treatment. By comparing the results for the reference epitaxial wafer shown in Fig. 2.18 (b-i) and those for the studied bonded wafer shown in Fig. 2.18 (b-ii), it was found that the concentration of oxygen in the bonded FZ Si layer of the bonded wafer is one order lower than that in the epitaxial layer of the reference epitaxial wafer after heat treatment.

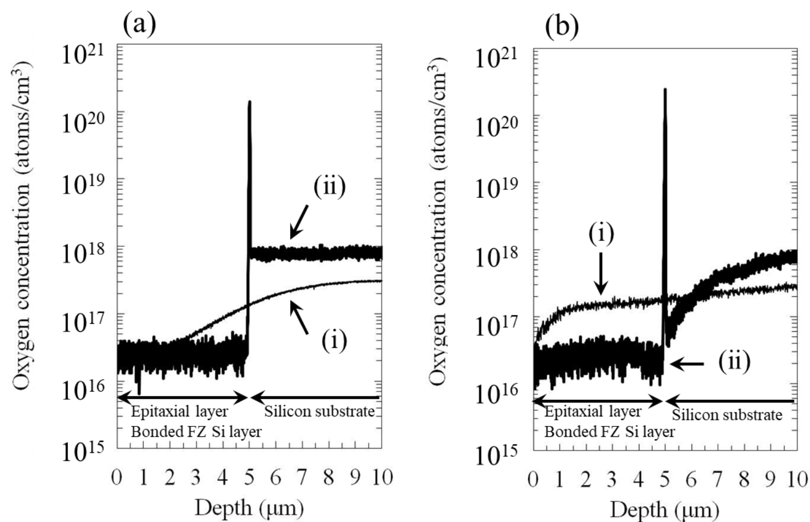


Fig. 2.18. Depth profiles of oxygen concentrations measured on (i) reference epitaxial and (ii) studied bonded wafers by SIMS analysis: (a) after fabricating wafers (before heat treatment) and (b) after heat treatment in device fabrication.

2.4.2.3 Gettering behaviors of transition metal

Figure 2.19 shows the optical microscopy images of the pits made by nickel silicide on the surfaces of two samples (studied bonded and reference epitaxial wafers) after nickel contamination at 2×10^{13} atoms/cm^2 and Wright etching. Figure 2.19 (a) shows the result for the reference sample (epitaxial wafer). Many pits were observed on the surface of the chip. Figure 2.19 (b) shows the result for the studied sample (bonded wafer). No pits were observed on the surface of the chip. Because Wright etching etches not the nickel silicide but only the silicon layer, the silicon layer of the studied sample did not contain any nickel silicide. On the other hand, the reference sample had a large amount of nickel silicide. Therefore, this studied bonded wafer has a gettering capability of at least 2×10^{13} atoms/cm^2 for nickel, whereas the reference sample does not.

Next, the depth profiles of the concentrations per volume of nickel, copper, and iron for the studied sample were obtained by SIMS analysis after contamination with these metals. Figure 2.20 shows the depth profiles of the concentrations of nickel [Fig. 2.20 (a)], copper [Fig. 2.20 (b)], and iron [Fig. 2.20 (c)] obtained by SIMS analysis. The approximate SIMS detection limits are 2×10^{15} atoms/cm^3 for nickel, 2×10^{15} atoms/cm^3 for copper, and 6×10^{14} atoms/cm^3 for iron. Nickel, copper, and iron were each detected to be greater than 4×10^{17} atoms/cm^3 at the bonding interface, but not detected in other regions. Therefore, the bonding interface of the studied bonded wafer acted as a gettering sink of at least 2×10^{13} atoms/cm^2 for nickel, copper, and iron.

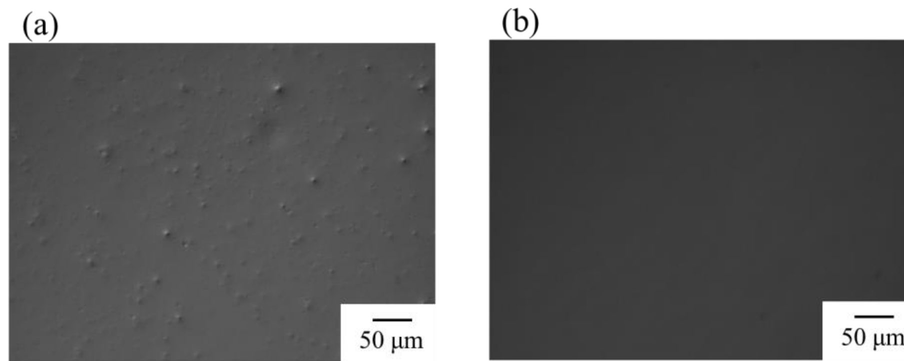


Fig. 2.19. Optical microscopy (OM) images of the pits made by nickel silicide on the surfaces of the (a) reference epitaxial and (b) studied bonded wafers after contaminating nickel at 2×10^{13} atoms/cm^2 and Wright etching.

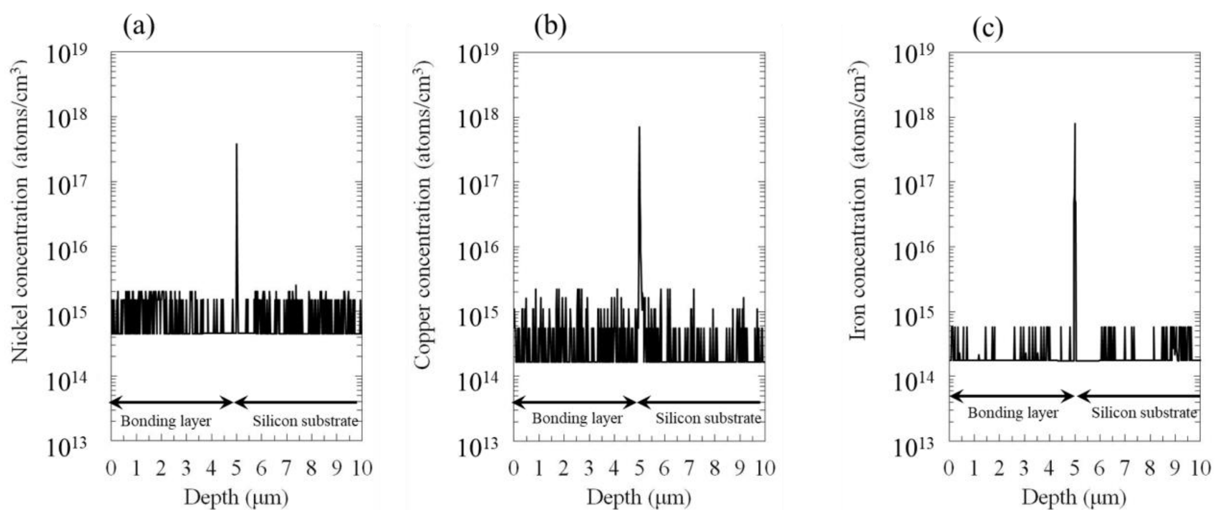


Fig. 2.20. Depth profiles of metallic impurity concentrations measured by SIMS analysis after contamination of 2×10^{13} atoms/cm^2 (a) nickel, (b) copper, and (c) iron.

2.4.2.4 Characteristics of actual devices

The characteristics of the pn-junction diode fabricated as an actual device in two samples (studied bonded and reference epitaxial wafers) by the process and with the structure shown in Fig. 2.15 were measured. Figure 2.21 shows the results of the measurement of the pn-junction diode. The dotted (i) and solid (ii) lines in Fig. 2.21 respectively show the results for the reference epitaxial and studied bonded wafers. They had a reverse current of -3 V to 0 V and a forward current of 0 V to 3 V. Because both showed the characteristics of a pn-junction diode,[24)] the successful fabrication of pn-junction diodes in the samples was confirmed. The reverse electrical current of the studied sample was below 1×10^{-9} A/cm^2, as shown by the solid line (ii) in Fig. 2.21. On the other hand, that of the reference sample was higher than 1×10^{-6} A/cm^2, as shown by the dotted line (i). The leakage current of the studied sample decreased to one-thousandth that of the reference sample.

The leakage current of the pn-junction diode is increased by contamination with transition metals or oxygen.[99,100)] The depth profiles of the concentrations per volume of transition metals (nickel, copper, and iron) and oxygen were analyzed in the studied and reference samples by SIMS after removing the metal and interlayer insulator of the samples with a pn-junction device fabricated as an actual device. Nickel, copper, and iron were detected at high concentrations, as shown in Figs. 2.22 (a-1), 2.22 (a-2), and 2.22 (a-3), respectively. In the studied bonded wafer, these transition metals were detected at concentrations greater than 5×10^{17} atoms/cm^3 at the bonding interface. Thus, the wafer could obtain more than 5×10^{17} atoms/cm^3 of transition metals during the fabrication of the pn-junction diode. The concentrations of gettered metals are higher than those of contaminants, as shown in Fig. 2.20. Therefore, the studied wafer has a gettering capability of at least 2×10^{13} atoms/cm^2 at the bonding interface. On the other hand, in the reference epitaxial wafer, no nickel, copper, or iron was detected. Since the reference wafer has no gettering sink, this is reasonable.

Figure 2.22 (b) shows the profiles of oxygen concentration. The oxygen concentration in the reference sample was more than 7×10^{16} atoms/cm^3, and oxygen diffused from the silicon substrate to the epitaxial layer with the fabricated devices, as shown in Fig. 2.22 (b-i). This result is the same as that in Fig. 2.18 (b-i) obtained after the heat treatment in device fabrication. On the other hand, the oxygen concentration in the studied sample was kept below 5×10^{16} atoms/cm^3, and oxygen did not diffuse from the silicon substrate to the bonded FZ Si layer with the fabricated devices, as shown in Fig. 2.22 (b-ii). This result is the same as that in Fig. 2.18 (b-ii) obtained after the heat treatment in the fabrication of actual devices. Thus, the concentration of oxygen in the bonded FZ Si layer of the studied sample was lower than that in the epitaxial layer of the reference sample after fabricating the pn-junction diode.

Next, the bonded interface of the studied sample was observed on a cross-sectional TEM image after fabricating the pn-junction diode. Figure 2.23 shows the cross-sectional HR-TEM image. The bonding interface was flat and there were no microvoids. Again, no amorphous layer of 6 nm thickness was observed in the bonding interface. This result is the same as that in Fig. 2.17 (b) obtained after the heat treatment in the fabrication of actual devices. In addition, defect A was observed in the strain regions, as indicated by the blue dotted line in Fig. 2.23. Because defect A was observed in the region in which an amorphous layer existed after wafer fabrication, as shown in Fig. 2.17 (a), this defect A was formed as a result of the lattice mismatch and strain of the silicon crystal after recrystallization during device fabrication.

When the concentration of an element in a silicon crystal is more than 1×10^{20} atoms/cm^3, EDX analysis can yield a concentration map of that element.[101,102)] Because the concentration of oxygen detected at the bonding interface by SIMS analysis exceeded 1×10^{20} atoms/cm^3 [Fig. 2.22 (b-ii)], the concentration map of elemental oxygen around the bonding interface was analyzed by EDX analysis. Figure 2.24 (a) shows the analyzed area, and Fig.

2.24 (b) shows the concentration map of elemental oxygen in the studied sample. A high concentration of oxygen was detected at defect A. In addition, the depth profile of oxygen is shown in Fig. 2.24 (c). Oxygen was detected at concentrations much higher than the detection limit at defect A and was maximum at the bonding interface.

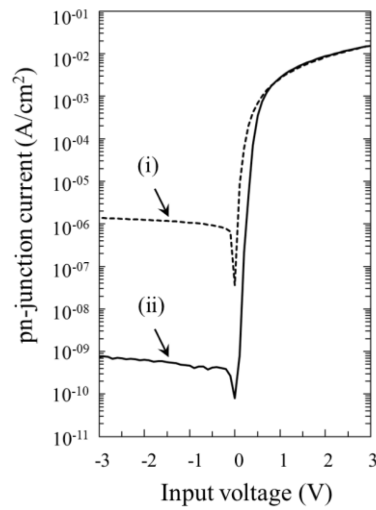


Fig. 2.21. Characteristics of the pn-junction diode fabricated on the (i) reference epitaxial and (ii) studied bonded wafers.

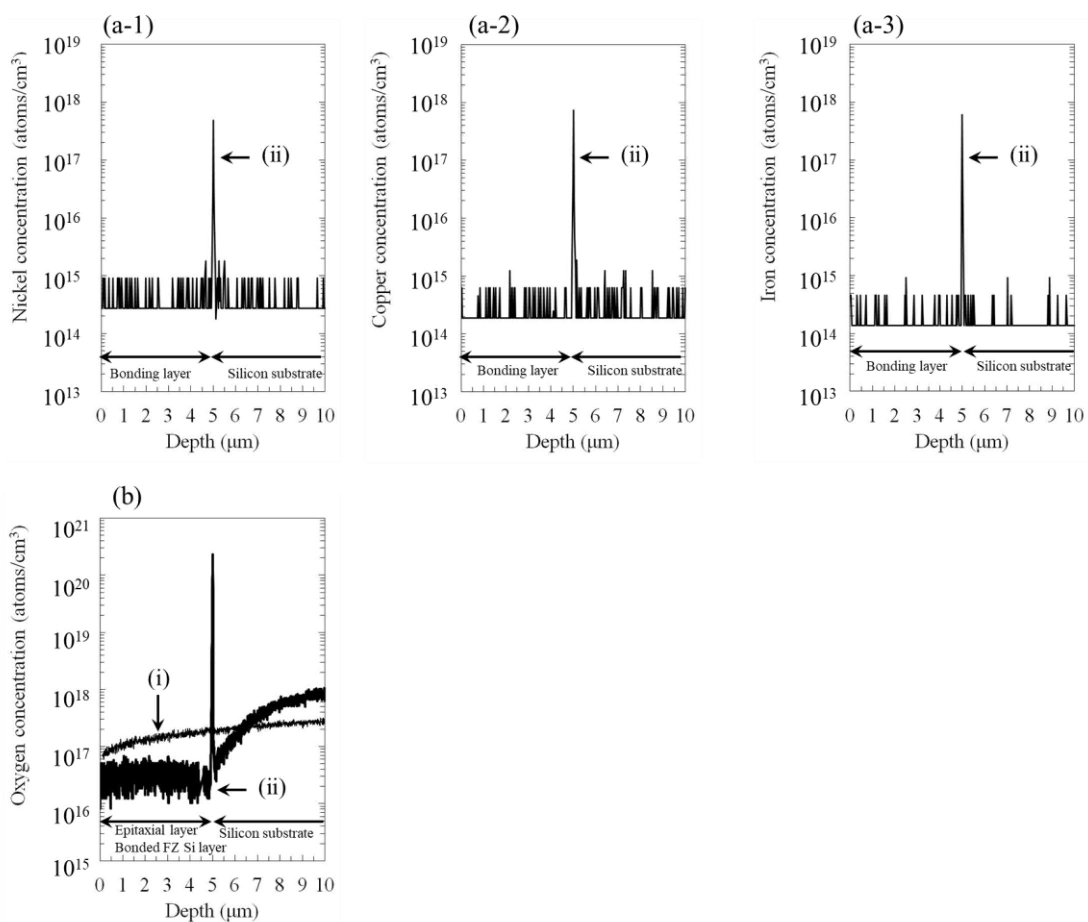


Fig. 2.22. Depth profiles of metallic impurity and oxygen concentrations measured on (i) reference epitaxial and (ii) studied bonded wafers by SIMS analysis after device fabrication: (a-1) nickel, (a-2) copper, (a-3) iron, and (b) oxygen.

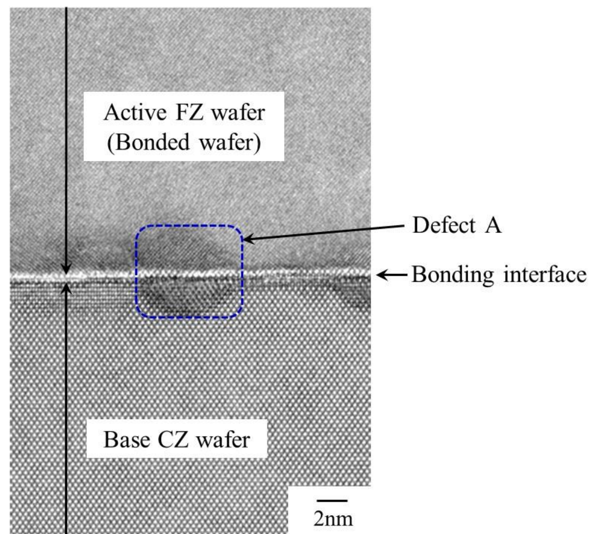


Fig. 2.23. Cross-sectional TEM image of the studied bonded wafer after fabricating pn-junction diode.

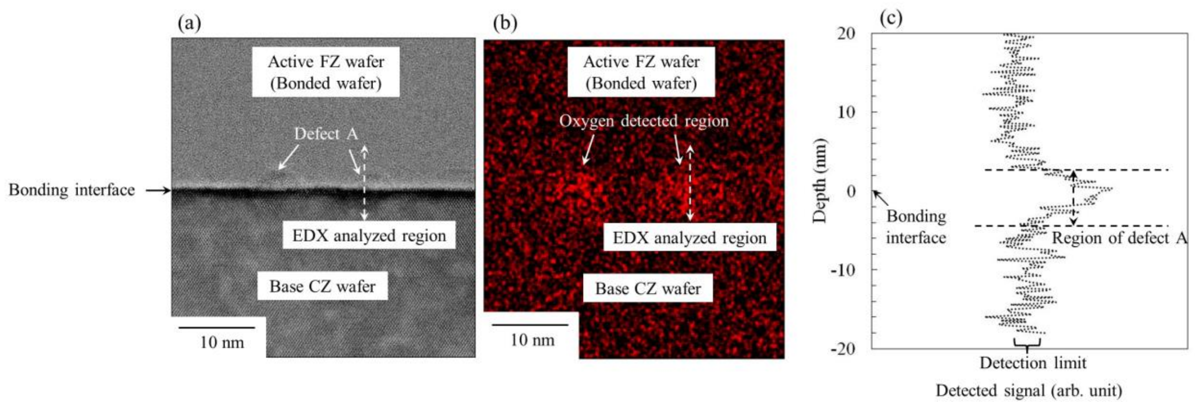


Fig. 2.24. Map and depth profile of elemental oxygen for the studied bonded wafer, obtained by EDX analysis after fabricating pn-junction diode: (a) cross-sectional TEM image of the analyzed region, (b) map of elemental oxygen concentration, and (c) depth profile of elemental oxygen.

2.4.3 Discussion

According to Figs. 2.17 and 2.23, lattice mismatch existed at the bonding interface. In addition, according to Fig. 2.24, the strains shown as defect A existed at the bonding interface. Oxygen was distributed at the bonding interface shown in Figs. 2.18 and 2.22 (b) and at defect A in the bonding interface shown in Fig. 2.24. In accordance with the Cottrell effect, impurities segregate to relieve strain in the silicon crystal[85,94)] and the strain region acts as a gettering sink. Therefore, defect A with strain and the bonding interface with lattice mismatch acted as gettering sinks for oxygen.

On the other hand, nickel, copper, and iron were detected at the bonding interface by SIMS analysis, as shown in Figs. 2.20 and 2.22. Yu et al. showed that copper segregated at the bonding interface.[90)] Aucouturier et al. showed that copper segregated into twin defects,[80)] and Maurice and Colliex showed that copper and iron segregated into grain boundaries.[95)] Because my studied bonding wafer has defect A with strain and a bonding interface with lattice mismatch at the bonding interface, as shown in Figs. 2.17 and 2.23, these defects also act as gettering sinks for the metals. Therefore, in the studied bonding wafer, the concentrations of oxygen and metallic impurities in the device-fabricating region could be reduced by gettering oxygen and metallic impurities at the bonding interface; this also decreased the leakage current of the pn-junction diode formed in the bonded FZ Si layer.

2.4.4 Summary

The bonding characteristics and oxygen- and transition-metal-impurity gettering performance of a wafer comprising an FZ wafer and a CZ substrate bonded by SAB were demonstrated for the first time. This bonded wafer has an amorphous layer of 6 nm thickness in the bonding interface. This amorphous layer is recrystallized during device fabrication, and the strain remained in the recrystallized region. Areas of strain act as gettering sinks for oxygen and metallic impurities. Consequently, the concentration of oxygen in the device fabrication region is less than 1×10^{17} atoms/cm^3 after device fabrication, and the wafer has a gettering capability of at least 2×10^{13} atoms/cm^2.

2.5 Conclusions

Two types of silicon-bonded wafer fabricated by SAB for use in high-sensitivity imaging sensors were studied in this chapter. One type was a silicon epitaxial wafer bonded to a molecular-ion-implanted silicon substrate with a total thickness of 15 µm for high-sensitivity CMOS imaging sensors of security cameras. The other type was an FZ silicon wafer bonded to a CZ silicon wafer with a total thickness greater than 100 µm used in IR-detecting sensors with an APD device of the LiDAR system. With these bonded wafers, a device fabrication region (the bonding layer) with a concentration of less than 1×10^{17} atoms/cm^3 and a gettering capability of more than 2×10^{13} atoms/cm^2 for metallic impurities was formed for the first time in the world. The results are summarized below.

1. The concentration of oxygen in the bonding layer (an epitaxial layer or an FZ wafer) of the fabricated imaging devices decreased to less than 1×10^{17} atoms/cm^3.

2. The bonding interface between the bonding wafer (an epitaxial wafer or an FZ wafer) and the silicon substrate has a gettering capability of more than 2×10^{13} atoms/cm^2 for metallic impurities such as nickel, copper, and iron.

3. The leakage current of the pn-junction diode, which was the dark current of the studied wafer, decreased to one-thousandth that of the reference wafer.

Chapter 3 SOI wafers with low fixed charge or low membrane stress

3.1 Introduction

Two types of SOI wafer have been produced. Figure 3.1 shows the correlation between the thicknesses of the BOX and silicon layers of an SOI wafer.[47] The type A SOI wafer has BOX and silicon layers that are more than 1 μm thick. This SOI wafer has been used for the fabrication of power devices. Recently, it has also been used for fabricating MEMS. The type B SOI wafer has BOX and silicon layers that are less than 1 μm thick. Figure 3.2 shows the MOS structure fabricated in this SOI wafer. When the silicon layer is thick, it is depleted by a high voltage, as shown in Fig. 3.2 (a). On the other hand, when the silicon layer is thin, it is easily depleted by a low voltage, as shown in Fig. 3.2 (b). Therefore, the type B wafer has been used for fabricating RF devices that operate at low power with a high speed at a high frequency.

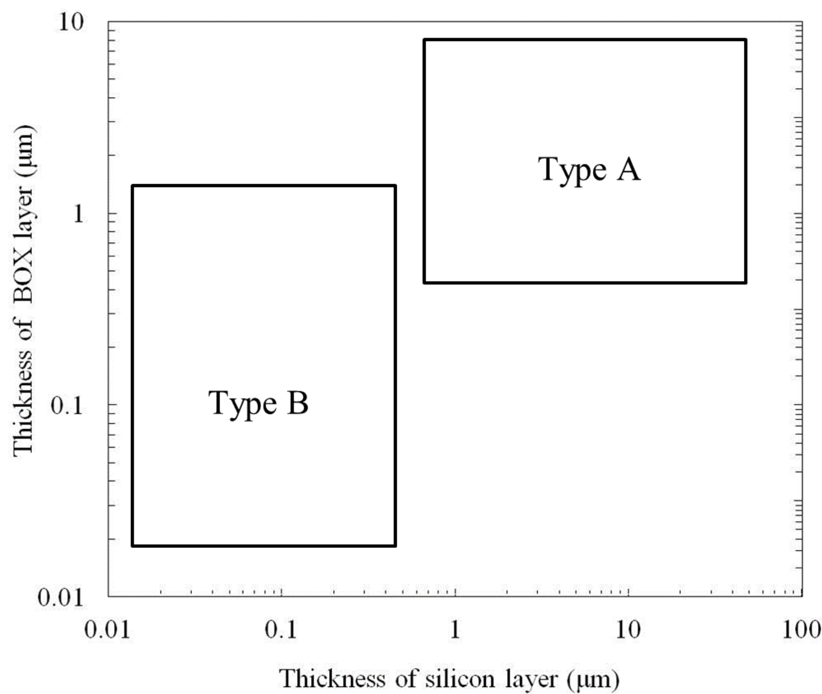


Fig. 3.1. Correlation between thicknesses of BOX and silicon layers of SOI wafer.

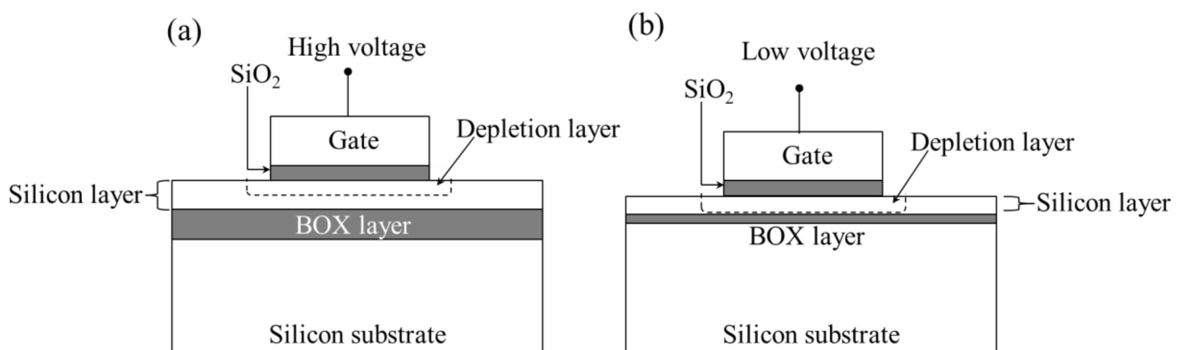


Fig. 3.2. MOS structure fabricated on SOI wafer.

Because the thicknesses of the silicon and BOX layers of the type A SOI wafer are different from those of the type B SOI wafer, the production methods of the type A and type B SOI wafers are also different. Figure 3.3 shows the method of producing the type A wafer. Two silicon substrates are first produced, as shown in step (1). A SiO_2 layer is then formed on silicon substrate 2 by thermal oxidation at a temperature higher than 800°C, as shown in step (2).[103] Third, silicon substrate 1 is bonded to silicon substrate 2 with the SiO_2 layer by thermal heat treatment at a temperature above 1000°C, as shown step in (3).[56] Finally, silicon substrates 1 and 2 are each ground and polished from the back.

Figures 3.4–3.6 show the method of producing type B SOI wafers. Figure 3.4 shows a UNIBOND wafer.[47] Two silicon substrates are first produced, as shown in step (1). Secondly, hydrogen ions are implanted into silicon substrate 1, and then a SiO_2 layer is formed in silicon substrate 2 by thermal oxidation, similarly to the type A wafer, as shown in step (2). Next, silicon substrate 1 is bonded by thermal heat treatment at 300–400°C through the smart cut process to silicon substrate 2 with the SiO_2 layer separated from the hydrogen-implanted region. Then, a silicon layer is strongly bonded to silicon substrate 2 by thermal heat treatment, similarly to the type 1 wafer, as shown in step (3). Finally, silicon substrates 1 and 2 are each ground and polished from the back, as shown in step (4). When the silicon layer is very thin, chemical mechanical polishing (CMP) cannot be used to flatten the surface of a separated bonding wafer that requires a small polishing allowance. Thus, plasma-assisted chemical etching (PACE) has been used to optimize the thin layer.[104] In this flattening method, the thickness of the separated silicon layer is first measured over the entire wafer. Then, the separated silicon layer is plasma-etched while feeding back the measured thickness point by point. Silicon substrate 1 can be recycled.

Next, Fig. 3.5 shows an epitaxial layer transfer (ELTRAN) wafer, which has been suggested as a high-quality silicon layer on the BOX layer.[46] Two silicon substrates are first produced, as shown in step (1). Secondly, a porous silicon layer is formed on the surface of silicon substrate 1 by anode formation, as shown in step (2). In this anode formation, voltage is applied to silicon substrate 1 while dipping it in hydrofluoric acid and ethanol. The epitaxial silicon layer is then grown on the porous silicon layer after the recrystallization of the surface of the porous silicon layer by baking at a temperature above 1000°C in a hydrogen atmosphere, as shown in step (3). A SiO_2 layer is additionally formed on the epitaxial silicon layer by thermal heat treatment such as that used for the type A and UNIBOND wafers, as shown in step (4). Next, silicon substrate 1 is bonded to silicon substrate 2 by thermal heat treatment, similarly to the type A and UNIBOND wafers. A porous layer is then separated by the wafer pressure of the wafer jet method. Finally, the porous layer is completely ground away and the surface of the epitaxial layer is then slightly polished. This silicon substrate 1 can also be recycled, similarly to that of the UNIBOND wafer.

Finally, Fig. 3.6 shows separation using an implanted oxygen (SIMOX) wafer, which was suggested for fabricating an SOI wafer at a low cost.[45] One silicon wafer is first produced, as shown in step (1). Next, oxygen ions are implanted into the silicon wafer, as shown in step (2). Finally, the implanted silicon wafer is annealed by thermal heat treatment at a temperature above 1300°C in an oxygen atmosphere to form the BOX layer in the region with implanted oxygen, as shown in step (3).

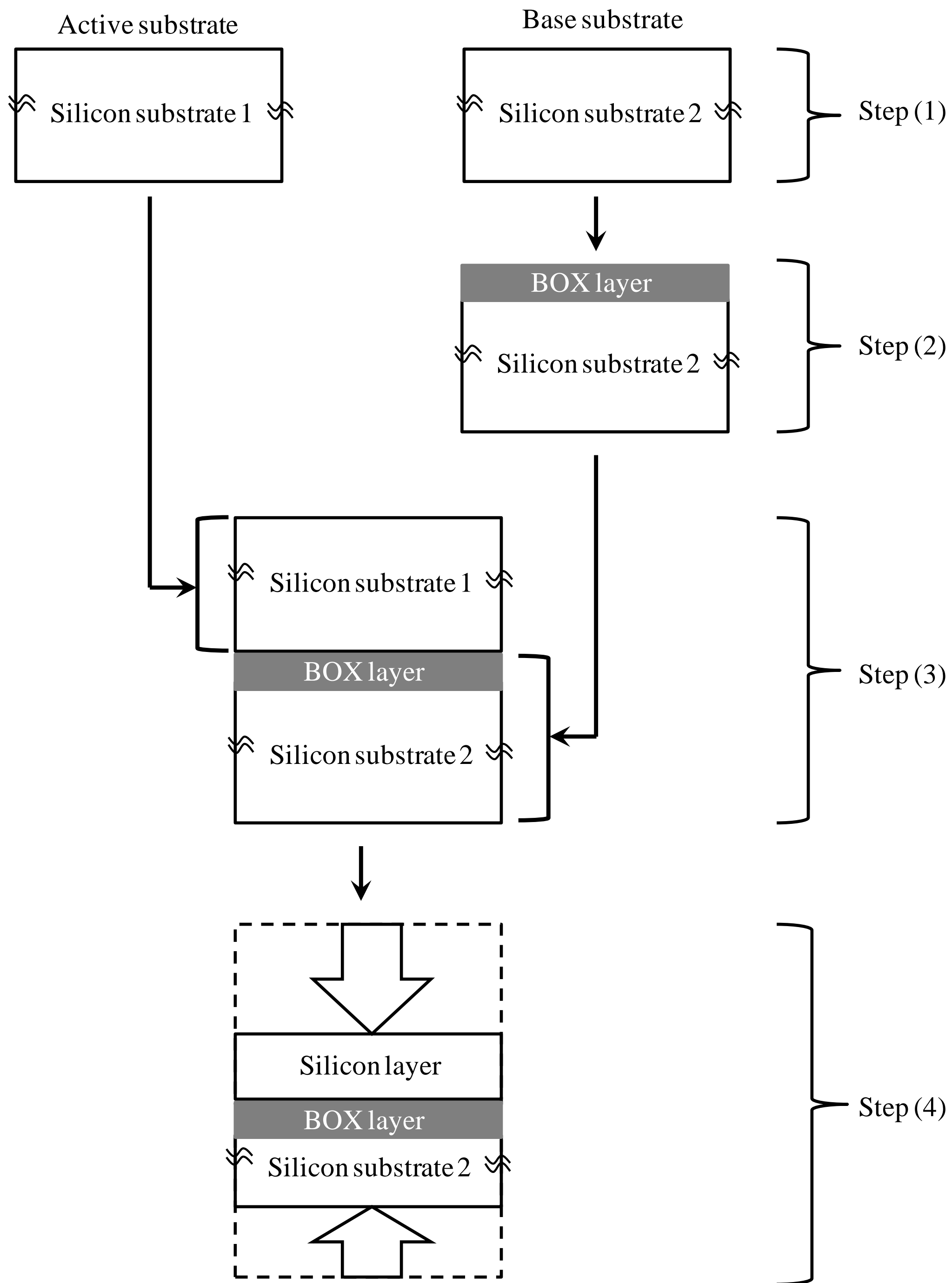


Fig. 3.3. Method of producing type A wafer (silicon and BOX layers: thicker than 1 μm).

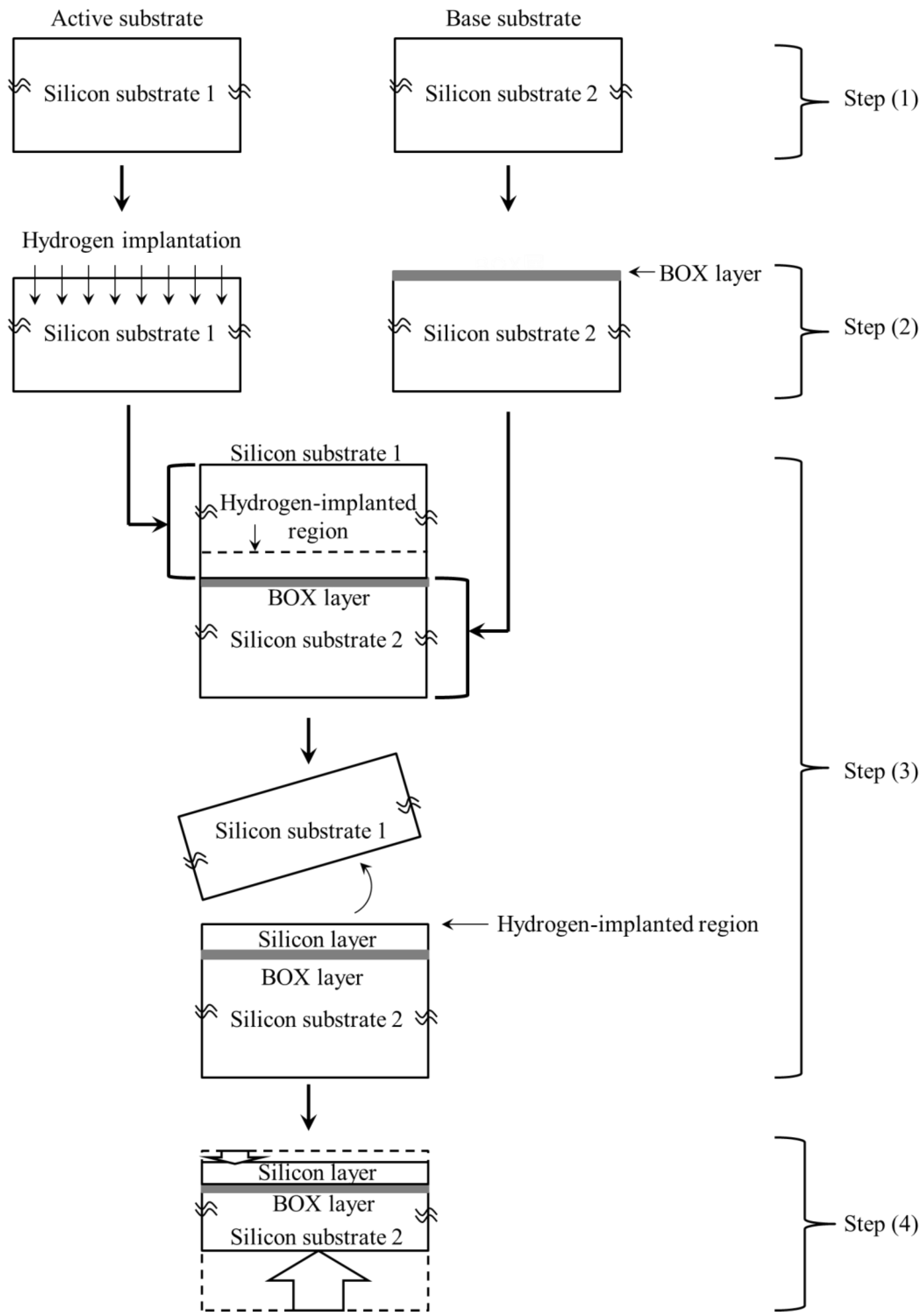


Fig. 3.4. Method of producing type B UNIBOND wafer (silicon and BOX layers: thinner than 1 μm).

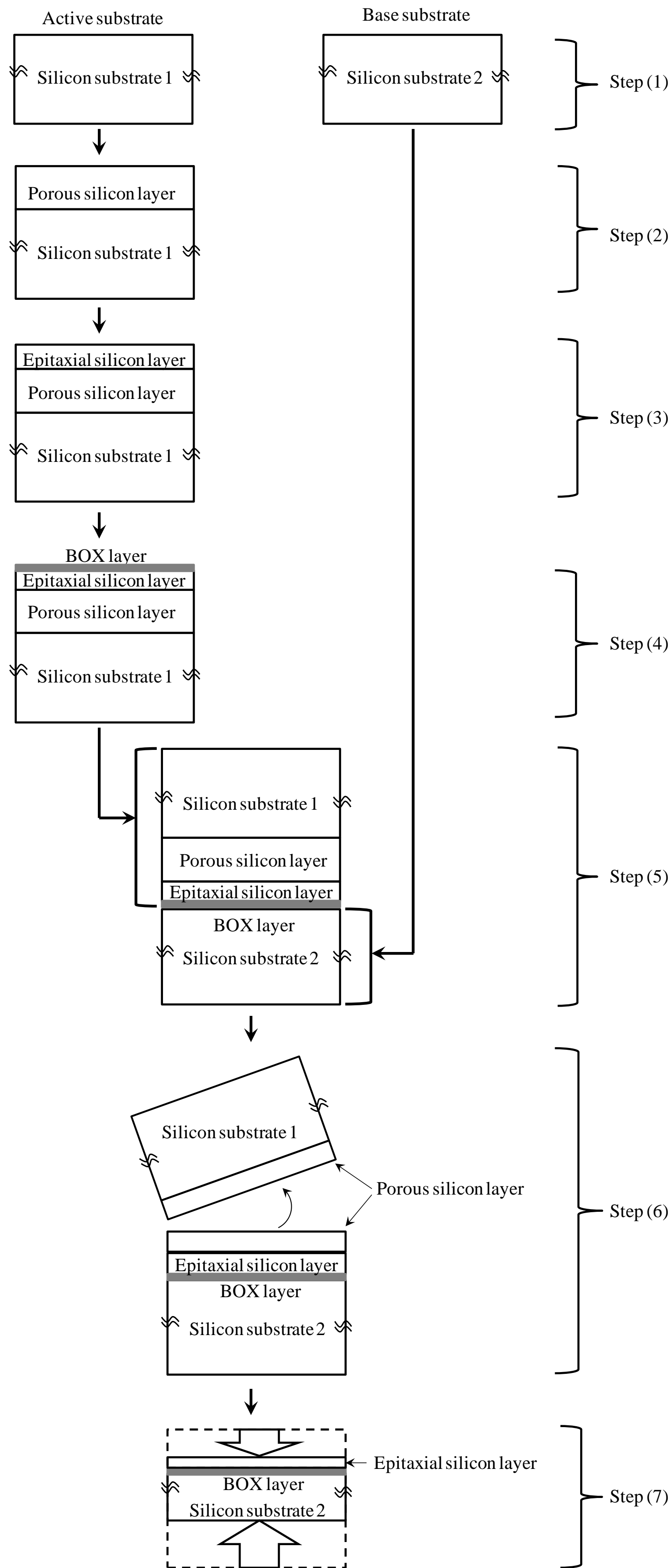


Fig. 3.5. Method of producing type B ELTRAN wafer (silicon and BOX layers: thinner than 1 μm).

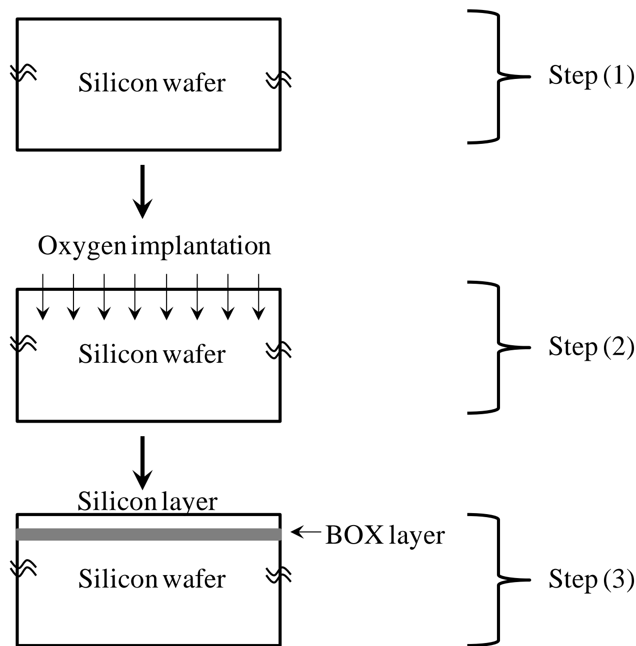


Fig. 3.6. Method of producing type B SIMOX wafer (silicon and BOX layers: thinner than 1 μm).

For fabricating these SOI wafers, a BOX layer has been formed by thermal oxidation[103] and a silicon layer has been bonded to the BOX layer by thermal oxidation at a temperature above 800°C for 3–4 h.[56] Because thermal oxidation occurs through the reaction of diffused oxygen with the silicon substrate, it takes a long time to form a thick thermal oxide film. A BOX layer that is more than 10 μm thick must be oxidized for more than 30 days, making the wafer fabrication process highly costly. In addition, there is a transition layer between the thermal oxide film and the silicon substrate, and this transition layer has a fixed charge.[42–44] This fixed charge is not neutral but positive. Thus, the resistivity of the silicon layer on the BOX layer changes and the leakage current consequently increases in the well region of power or RF devices in the silicon layer. It is a problem that the leakage current is increased more than 1×10^5 times by the fixed charge in the BOX layer.[105] In addition, dopant elements such as boron and phosphorus out-diffuse during the long thermal bonding process at high temperatures, and the resistivity in the silicon layer on the BOX layer consequently changes. Thus, for the devices formed on the SOI wafer, it is important for the resistivity in the silicon layer where devices are fabricated to be constant. However, the SOI wafer in which the resistivity of the silicon layer is constant has not been studied.[45–47]

On the other hand, the coefficient of thermal expansion of the SiO_2 BOX layer is 0.5×10^{-6}/°C and that of a bonding wafer made of a silicon single crystal is 2.3×10^{-6}/°C.[105] Since they are different, membrane stress of about 300 MPa remains around the BOX layer in an SOI wafer,[106] and the MEMS devices fabricated in such wafers become warped.[107] Since a silicon oxide layer on a silicon substrate has compressive stress and a SiN layer on a silicon substrate has tensile stress, the SiO_xN_y layer has been studied to decrease the membrane stress in the layer.[20] However, in this method, it is difficult to balance the compressive and tensile stresses by setting x and y, and the process margin is poor. The process cost becomes higher than that of fabricating the SiO_2 layer because of the addition of nitrogen-based gas. In addition, there is the problem that the etching rate of the SiO_xN_y layer by hydrofluoric (HF) acid is lower than that of a SiO_2 layer.

Therefore, the current SOI wafers have at least three issues that must be resolved: reduction in fixed charge in the BOX layer, reduction in membrane stress around the BOX layer, and reduction in the duration of the wafer fabrication process.

3.2 Objectives

Here, I look at three types of SOI wafer that have an extra-thick BOX layer of 10 μm thickness fabricated by chemical vapor deposition (CVD)[108,109] and SAB in less than one-tenth the time required by the reference method (thermal oxidation and thermal bonding). Such wafers would enable the fabrication of power devices at high voltages. The first type is an SOI wafer in which the resistivity in the silicon layer is not changed by forming the thick BOX layer without a fixed charge (Chapter 3.3). The second type has a thick BOX layer without a fixed charge that was annealed to increase its density and breakdown electric field (Chapter 3.4). The third type has a SiO_x ($x < 2$) BOX layer to investigate the possibility of reducing the membrane stress around the BOX layer after the fabrication of the SOI wafer and heat treatment (Chapter 3.5).

3.3 SOI wafer with extra-thick SiO_2 BOX layer

3.3.1 Experimental methods

The resistivity of the silicon layer of the SOI wafer was studied to determine whether or not it was changed by forming the BOX layer without a fixed charge. Figure 3.7 illustrates the method of fabricating an SOI wafer with an extremely thick BOX layer. Two silicon wafers were fabricated: the base wafer and the bonding wafer. The BOX layer was deposited on the base wafer by plasma-enhanced chemical vapor deposition (PE-CVD) at 500°C to achieve a strong bonding to the base wafer.[108,109] After depositing the BOX layer, only its top surface was polished by CMP for bonding to the bonding wafer without void generation. The bonding wafer was then bonded to the base wafer with the polished BOX layer by SAB at room temperature in an ultrahigh vacuum for a short time. After bonding the two wafers (bonding wafer and base wafer with the BOX layer), the bonding wafer was ground and polished down to the active layer of the device from the back, which is opposite the wafer-bonding region.

Table 3-I lists the experimental conditions adopted in polishing 2-inch-diameter silicon wafers to a thickness of 500 μm. These wafers were made of (100) CZ silicon single crystals. Their n- and p-type resistivities were 2–6 Ωcm, and their oxygen concentration was $1.0–1.2 \times 10^{18}$ atoms/cm^3. The n-type crystals are doped with phosphorus, and the p-type crystals are doped with boron. As illustrated in Fig. 3.7, the base wafer was deposited on a 10-μm-thick SiO_2 BOX layer at 500°C for 4 h by PE-CVD (Tsukishima Kikai Co., Ltd.). The surface of this BOX layer was polished by CMP. Then, as the silicon layer, the bonding wafer was bonded to the polished BOX layer of the base wafer by SAB in an ultrahigh vacuum of less than 1×10^{-5} Pa at room temperature for 5 min (Nidec Machine Tool Corporation, MWB08-AX). The top surface of the bonding wafer was irradiated with argon ions of less than 1 keV. After bonding the two wafers (bonding wafer and base wafer with the BOX layer), the bonding wafer was ground and polished from the back to a thickness of 2 μm. A reference sample comprising a 1.2-μm-thick BOX layer formed by thermal oxidation at 1100°C and a bonding wafer bonded to the BOX layer by high-temperature treatment at 800°C for 2 h followed by 1200°C for 1 h was fabricated for the comparative evaluation of a currently available SOI wafer and the studied SOI wafer.

As illustrated in Fig. 3.7, to search for voids after bonding the bonding wafer to the deposited BOX layer [steps (a) and (b)] and after heat treatment during device fabrication [steps (c)], IR and cross-sectional TEM observations were carried out. Then, the breakdown electric field of the deposited BOX layer was evaluated by TZDB measurement[110] [step (d)] and the concentration of doping elements in and the resistivity of the bonded bonding wafer were determined by SIMS analysis and SR measurement [steps (e) and (f)] after grinding and polishing the bonded bonding wafer to be as thin as the active layer of the device.

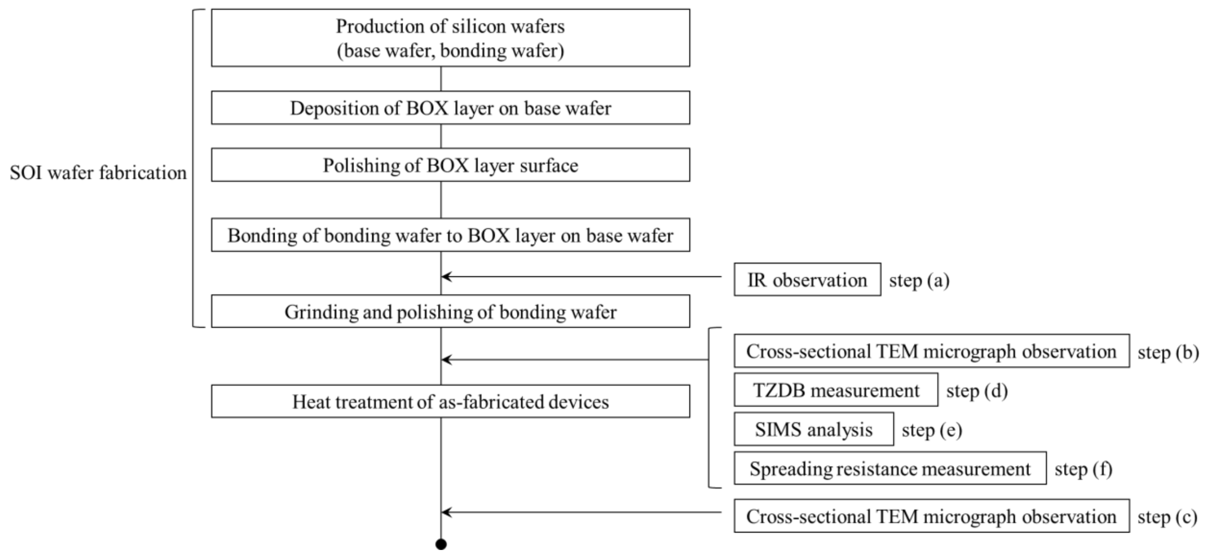


Fig. 3.7. Flowchart of experiment.

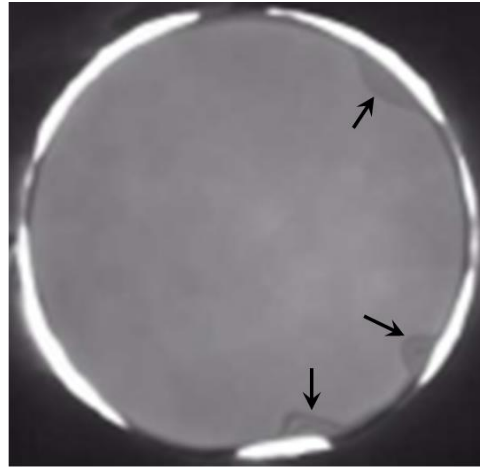
Table 3-I. Specifications of samples used in this study.

	Silicon layer (bonding wafer)	BOX layer	Silicon substrate
Studied sample	silicon wafer n-type (phosphorus-doped) 2–6 Ω·cm Oi: 1.0–1.2 $\times 10^{18}$ atoms/cm^3 2 μm (500 μm before grinding) 2 inch diameter	PE-CVD 10 μm	silicon wafer p-type (boron-doped) 2–6 Ω·cm Oi: 1.0–1.2 $\times 10^{18}$ atoms/cm^3 500 μm 2 inch diameter
Reference sample	silicon wafer n-type (phosphorus-doped) 2–6 Ω·cm Oi: 1.0–1.2 $\times 10^{18}$ atoms/cm^3 2 μm (500 μm before grinding) 2 inch diameter	Thermal oxidation 1.2 μm	silicon layer p-type (boron-doped) 2–6 Ω·cm Oi: 1.0–1.2 $\times 10^{18}$ atoms/cm^3 500 μm 2 inch diameter

3.3.2 Experimental results

3.3.2.1 Evaluation and observation of voids at bonding interface

The remaining voids were evaluated by IR transmission imaging after bonding a silicon wafer to the deposited and polished BOX layer by SAB. Figure 3.8 shows an IR transmission image. There were voids in the wafer only in three regions (indicated by arrows). These three regions were where tweezers were used to place the base wafer and the bonding wafer into the bonding equipment. These results indicate that the silicon wafer could be bonded to the deposited BOX layer by SAB at room temperature under a high vacuum.



→: Region pinched with tweezers

Fig. 3.8. IR transmission image of 2-inch-diameter wafer after bonding silicon wafer to deposited BOX layer of base wafer.

The bonded interface was also observed on a cross-sectional TEM image of the chip obtained after dicing the bonded wafer at its center. Figure 3.9 (a) shows the cross-sectional TEM images taken after SOI-wafer fabrication. The bonded interface was flat and had no microvoids.

In addition, the cross section of the bonding interface after heat treatment such as that in power-device production was observed to evaluate the thermal stability of the bonding region. This heat treatment was carried out at 1100°C for 4 h in an ambient gas of nitrogen in a furnace. Figure 3.9 (b) shows the cross-sectional TEM image taken after such heat treatment. There were no extended defects, such as punch-out dislocations, or new voids at the bonded interface. Therefore, the bonding interface between a silicon layer and the BOX layer deposited by SAB was thermally stable.

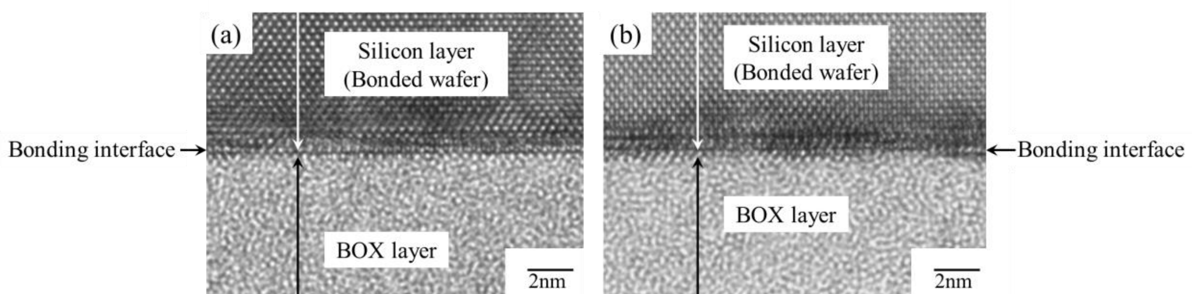


Fig. 3.9. Cross-sectional TEM images of bonding interface. (a) After bonding a silicon layer to a BOX layer and (b) after heat treatment such as that in device fabrication (1100°C for 4 h).

3.3.2.2 Evaluation of breakdown electric field of deposited BOX layer

The breakdown electric field of the BOX layer was determined for the studied and reference SOI samples by TZDB measurement.[110] When 0 V is applied to the silicon substrate under the BOX layer, the silicon layer on the BOX layer is supplied with an additional input voltage of 0.1 V. The electric field of the BOX layer is generally defined as the input voltage divided by the BOX layer thickness. When the leakage current from the silicon layer to the silicon substrate through the BOX layer was more than 1×10^{-4} A/cm^2, the intrinsic breakdown electric field was defined as being in the C mode.

Figure 3.10 shows the results of TZDB measurement for the (a) studied (deposited BOX layer, SAB) and (b) reference (oxidized BOX layer, thermal bonding) samples. The breakdown electric field of both samples was 11–12 MV/cm. Since the breakdown electric field of a thermal oxide film is generally 8–15 MV/cm, these results are reasonable.[110] As illustrated by curve (a), the leakage current of the studied sample was higher than that of the reference sample [curve (b)] when the input electric field was 0–10 MV/cm. Metallic impurities contaminating the BOX layer originated from the PE-CVD equipment used to deposit the BOX layer on the base wafer.[111,112] Therefore, the deposited BOX layer has an intrinsic breakdown electric field as well does a thermal oxide film.

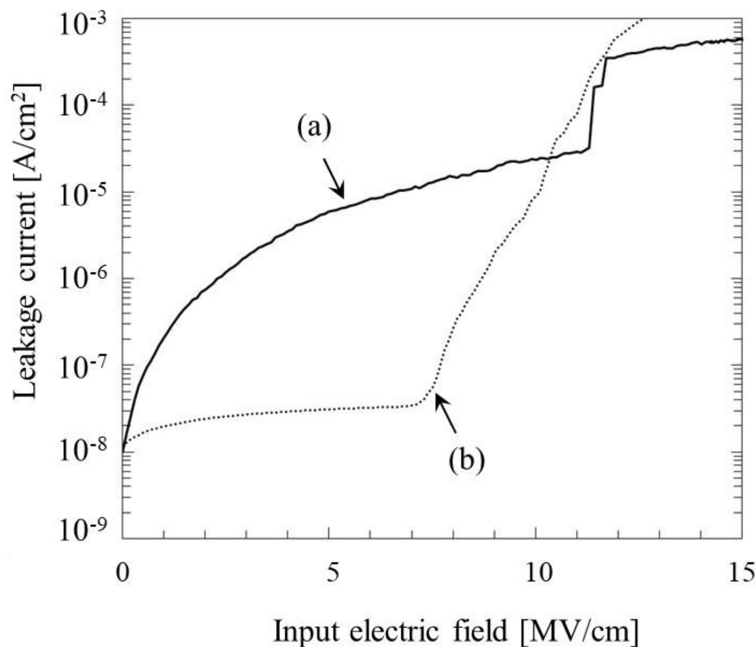


Fig. 3.10. TZDB measurement results for BOX layer. (a) Studied (deposited BOX layer, SAB) and (b) reference (oxidized BOX layer, thermal bonding) samples.

3.3.2.3 Evaluation of depth profile of concentration of doping element in bonded silicon layer on BOX layer

When devices are fabricated in an SOI wafer, the doping element concentration must be constant in the bonded silicon layer, in order that the resistivity in it is constant. In this study, the silicon layer as the n-type conductor was doped phosphorus, and the depth profile of phosphorus in the silicon layer was analyzed by SIMS analysis.

Figure 3.11 illustrates the results of the SIMS analysis for the studied and reference samples. The x-axis is the distance from the bonding interface and the y-axis is the phosphorus concentration determined by SIMS analysis. The concentration of phosphorus in the studied sample was constant from the top surface of the silicon layer to the bonding interface, as illustrated by curve (a). Thus, the silicon layer was bonded to the BOX layer at room temperature without the out-diffusion of phosphorus. On the other hand, the concentration of phosphorus in the reference sample decreased from a depth of 0.3 μm to the bonding interface, as illustrated by curve (b). These results show that, in the studied sample, the silicon layer was bonded to the BOX layer at room temperature without the out-diffusion of phosphorus.

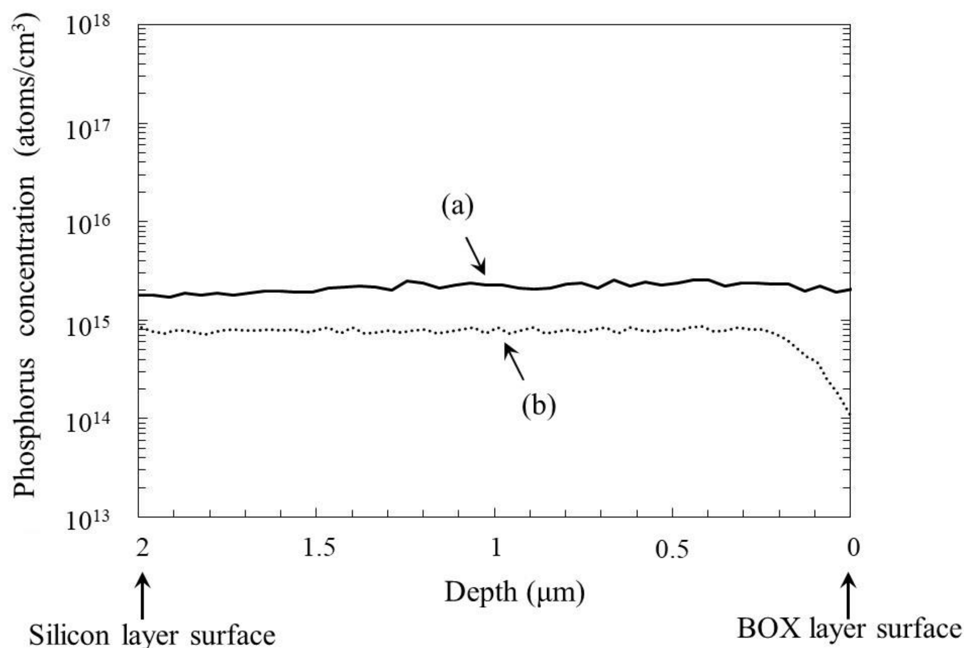


Fig. 3.11. SIMS depth profiles of phosphorus concentrations in silicon layer after fabricating SOI wafer. (a) Studied (deposited BOX layer, SAB) and (b) reference (oxidized BOX layer, thermal bonding) samples.

3.3.2.4 Evaluation of depth profile of resistivity in bonded silicon layer on BOX layer

Because devices are fabricated in the silicon layer of an SOI wafer, the resistivity of the silicon layer must be constant. Thus, the resistivity profiles of the studied and reference samples were evaluated by SR measurement.

Figure 3.12 shows the results of the SR measurement. The x-axis is the distance from the bonding interface and the y-axis is the resistivity obtained by SR measurement. The resistivity of the studied sample was constant from the top surface of the silicon layer to the bonding interface, as illustrated by curve (a). On the other hand, the resistivity of the reference sample [curve (b)] increased from a depth of 0.8 μm to the bonding interface between the silicon layer and the BOX layer. The resistivity at the bonding interface was about 1×10^4 times the constant resistivity in the region from a depth of 0.8 μm to 2.0 μm. Therefore, for the SOI wafer with the BOX layer deposited by PE-CVD and the silicon layer bonded by SAB, the resistivity of the silicon layer on the BOX layer was constant.

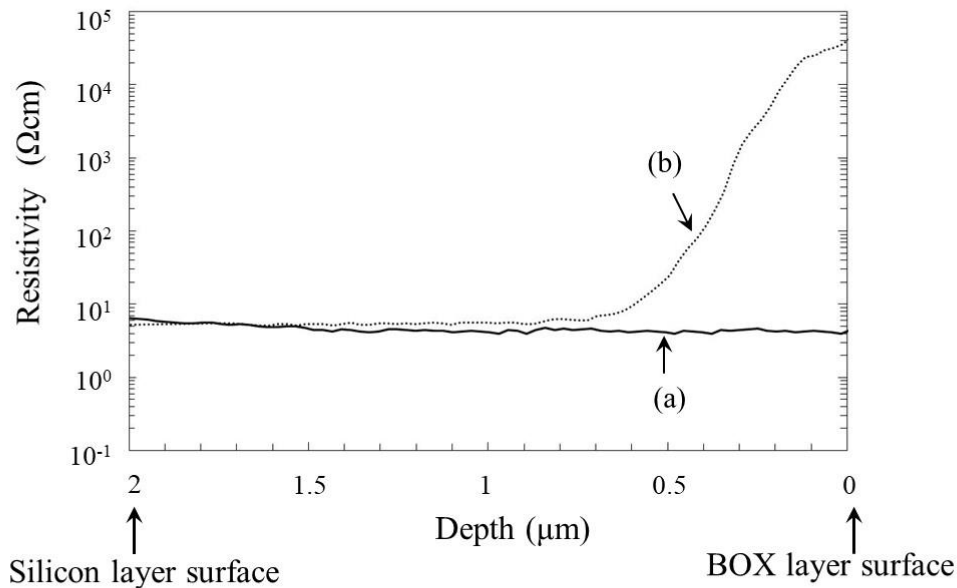


Fig. 3.12. Depth profiles of resistivity in silicon layer obtained by SR measurement after fabricating SOI wafer. (a) Studied (deposited BOX layer, SAB) and (b) reference (oxidized BOX layer, thermal bonding) samples.

3.3.3 Discussion

For the reference sample (oxidized BOX layer, thermal bonding), according to the results of SIMS analysis [Fig. 3.11 (b)], the phosphorus concentration decreased to 0.3 μm in the bonding region between the silicon and BOX layers. When the phosphorus concentration decreases to 1×10^{14} atoms/cm^3 from 1×10^{15} atoms/cm^3, the resistivity of this region will increase tenfold. However, according to the SR measurement results [Fig. 3.12 (b)], the resistance in this region increased more than 1×10^4 times those in the other regions. This increase in resistance cannot be explained by only the decrease in phosphorus concentration.

I hypothesized that a positive fixed charge in this BOX layer might affect the n-type-silicon layer. When the n-type region contacts with the p-type region, such as at the pn-junction, the carrier concentration in the n-type region is balanced by that in the p-type region, and the real carrier concentration in the n-type region decreases.[1] Figure 3.13 illustrates the carrier concentration in the silicon layer of the reference sample (oxidized BOX layer, thermal bonding). Curve (a) shows the depth profile of the carrier concentration calculated using the results of SR measurement, and curve (b) illustrates the depth profile of the phosphorus concentration determined by SIMS analysis. The notation D_{ref} represents the sum of the phosphorus concentrations in region 1 for the reference sample after fabricating the SOI wafer, D_{dep} is the sum of the carrier concentrations calculated using the resistivity determined by the SR measurement in region 1, and D_{BOX} is the positive fixed charge in the BOX layer. Because the silicon layer is of the n-type and the fixed charge in the BOX layer is positive (p-type), the following equation is used to investigate the effect of the fixed charge:

$$D_{BOX} = D_{ref} - D_{dep}, \quad (3\text{-}1)$$

where D_{ref} is the product of multiplying the phosphorus concentrations at depths from 0 to 0.8 μm in the silicon layer (1.66×10^{16} atoms/cm^3) and D_{dep} is the sum of the concentrations at depths from 0 to 0.8 μm calculated using the SR measurement data (7.28×10^{15} atoms/cm^3). D_{BOX} calculated using equation (3-1) was 7.46×10^{11}/cm^2 per unit area. The fixed charge is generally 1.0×10^{11}–1.0×10^{12}/cm^2.[43,44] The estimated fixed charge (D_{BOX}) was close to this general value. Thus, I concluded that a fixed charge existed in the thermally oxidized BOX layer of the reference sample but not in the deposited SiO_2 layer of the studied sample. Therefore, the fixed charge generated in the thermally oxidized BOX layer of the reference sample caused the resistance of the silicon layer on this BOX layer to increase.

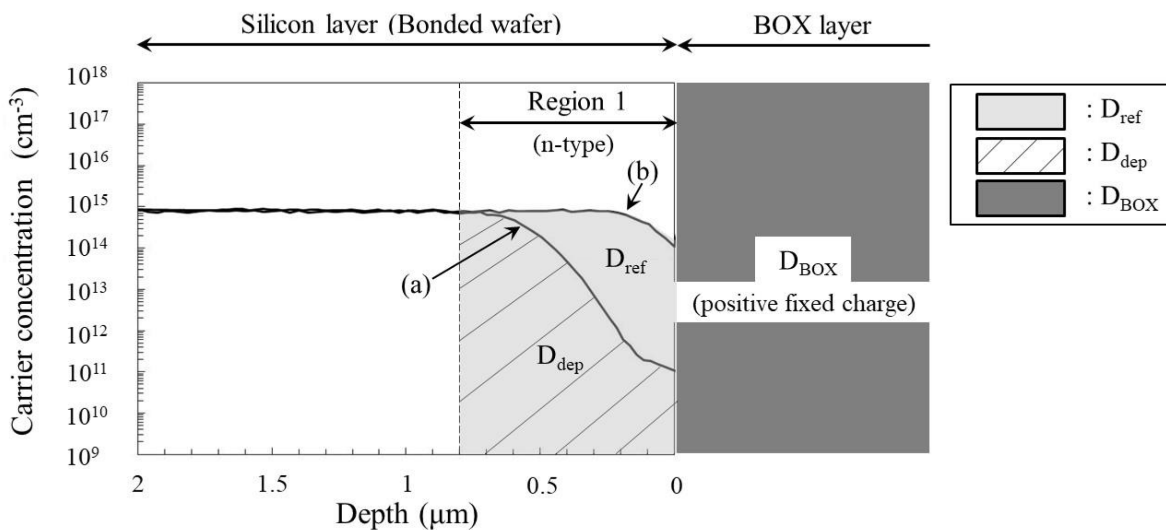


Fig. 3.13. Depth profiles of carrier concentration in silicon layer of reference sample (oxidized BOX layer, thermal bonding). (a) Carrier concentration calculated using the resistivity determined by SR measurement and (b) phosphorus concentration determined by SIMS analysis.

3.3.4 Summary

An SOI wafer with a 10-µm-thick BOX layer deposited by PE-CVD at 500°C for 4 h on which a silicon layer was bonded by SAB for 5 min was fabricated for the first time. A BOX layer with no fixed charge could be formed; thus, the resistivity of the silicon layer remains unchanged on the BOX layer. In addition, the bonding region has no voids and no extended defects after bonding and heat treatment such as that in device fabrication processes.

3.4 SOI wafer with deposited and annealed SiO_2 BOX layer

3.4.1 Experimental methods

The SOI wafer was studied to increase the density and breakdown electric field of the BOX layer without a fixed charge. Figure 3.14 shows the method of fabricating an SOI wafer with an extremely thick BOX layer. Two silicon wafers were fabricated: a base wafer and a bonding wafer. A BOX layer was deposited on the base wafer by PE-CVD at 300°C. Then, this BOX layer was annealed at a temperature above 300°C in an oxygen atmosphere to make it dense. After annealing the deposited BOX layer, only its top surface was polished by CMP to bond the bonding wafer on the deposited BOX layer by SAB at room temperature in an ultrahigh vacuum without forming voids. After bonding the bonding wafer on the BOX layer of the base wafer, the bonding wafer was ground and polished from the back, which is opposite the wafer-bonding region, to the desired thickness of the device formation region.

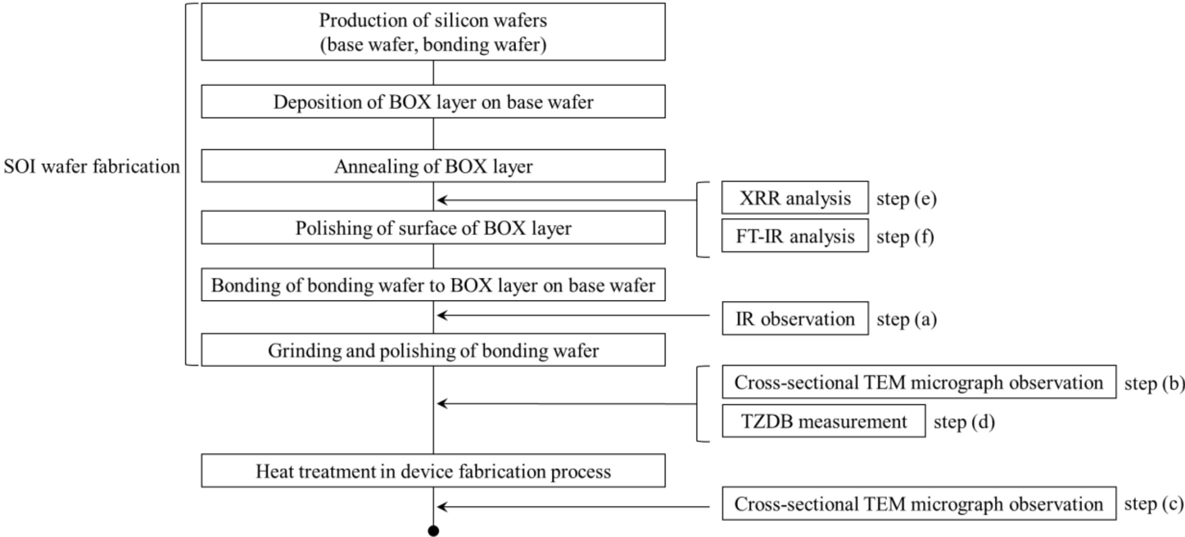


Fig. 3.14. Flowchart of experiment.

3.4.1.1 Sample fabrication

Table 3-II lists the specifications of 2-inch-diameter silicon wafers polished to a thickness of 500 μm. These wafers were made of (100) CZ silicon single crystals. The conductivity of these wafers was of the p-type doped with boron, their resistivity was 2–6 Ω·cm, and their oxygen concentration was 1.0–1.2 × 10^{18} atoms/cm^3.

A BOX layer of a 10-μm-thick silicon oxide film was deposited on the base wafer by PE-CVD at 300°C for 3 h (Tsukishima Kikai Co., Ltd.). Then, the deposited BOX layer was annealed in an oxygen atmosphere in a furnace at a temperature between 300°C and 1050°C for 1 h. Table 3-III lists the annealing conditions for the samples. The top surface of the BOX layer was polished by CMP. Then, the bonding wafer was bonded by SAB to the polished BOX layer of the base wafer as the silicon layer in an ultrahigh vacuum of 1 × 10^{-5} Pa at room temperature (Nidec Machine Tool Corporation, MWB08-AX). The top surface of the bonding wafer was irradiated with argon ions with an energy of less than 1 keV for 5 min. After bonding the bonding wafer to the base wafer with the BOX layer, the back of the bonding wafer was ground and polished until its thickness was 30 μm.

Table 3-II**.** Specifications of samples.

	Silicon layer (bonding wafer)	BOX layer	Base wafer
Studied sample	2 inch diameter Silicon wafer p-type (boron-doped) 2–6 Ω·cm Oi: 1.0–1.2 × 10^{18} atoms/cm^3 30 μm (500 μm before grinding)	PE-CVD 100 nm 10 μm	2 inch diameter Silicon wafer p-type (boron-doped) 2–6 Ω·cm Oi: 1.0–1.2 × 10^{18} atoms/cm^3 500 μm
Reference sample	2 inch diameter Silicon wafer p-type (boron-doped) 2–6 Ω·cm Oi: 1.0–1.2 × 10^{18} atoms/cm^3 30 μm (500 μm before grinding)	Thermal oxidation 100 nm	2 inch diameter Silicon layer p-type (boron-doped) 2–6 Ω·cm Oi: 1.0–1.2 × 10^{18} atoms/cm^3 500 μm

Table 3-III. Annealing conditions for silicon oxide film of base wafer of studied samples.

	Annealing temperature (°C)	Annealing time (hours)
Sample 1	NA	NA
Sample 2	300	1
Sample 3	500	1
Sample 4	700	1
Sample 5	900	1
Sample 6	1050	1

3.4.1.2 Experimental procedure

The presence of voids and defects was after bonding the bonding wafer to the BOX layer on the base wafer [Fig. 3.14 steps (a) and evaluated (b)] as well as after the heat treatment in the device fabrication process [step (c)]. Then, the breakdown electric field was measured after grinding and polishing the bonding wafer to the desired thickness of the device fabrication region [step (d)]. Finally, the density of the deposited BOX layer was evaluated after annealing the BOX layer on the base wafer [steps (e) and (f)].

3.4.1.2.1 Evaluation of remaining voids after bonding a bonding wafer to BOX layer deposited on base wafer

The sample was examined for voids by IR observation after bonding the silicon wafer to the BOX layer deposited on the base wafer. Because the IR radiation is transmitted through the silicon wafer and reflected at voids, any voids remaining at the bonding interface in a wafer can be detected.

3.4.1.2.2 Observation of cross section of bonding region between bonding wafer and BOX layer deposited on base wafer

Next, the sample was examined by TEM observation for wafer-bonding-induced defects in the bonding region between the bonding wafer and the BOX layer deposited on the base wafer. Cross-sectional TEM and high-resolution TEM (HR-TEM) images show wafer-bonding-induced defects generated during the fabrication of the SOI wafer and the heat treatment in the device fabrication process. Figure 3.15 illustrates the sequence of heat treatments in the fabrication of CMOS-FETs.[16] These heat treatments were at temperatures above 700°C in a nitrogen atmosphere, and the sample stage was loaded and unloaded at 700°C in nitrogen ambient gas in the furnace.

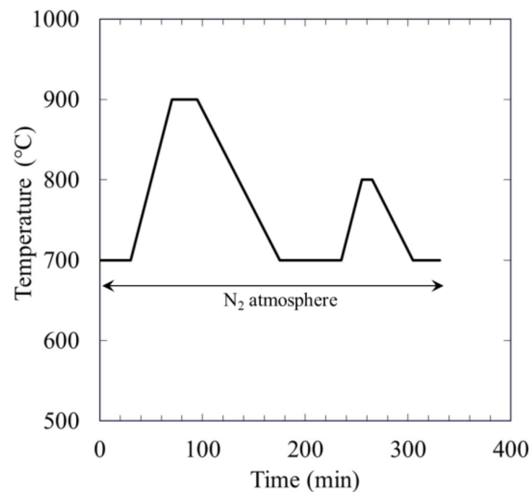


Fig. 3.15. Time history of heat treatment in device fabrication.

3.4.1.2.3 Evaluation of breakdown electric field of BOX layer

To evaluate the electrical insulation characteristic of the BOX layer, the breakdown electric field of the BOX layer of the studied samples was evaluated by TZDB measurement after patterning and fabricating a test element group (TEG) in the silicon layer on the BOX layer.[110] Although a voltage of 0 V was supplied to the base wafer under the BOX layer, an additional input voltage of 0.1 V was supplied to the silicon layer on the BOX layer. The electric field of the BOX layer, as an evaluated parameter, is defined as the input voltage divided by the BOX layer thickness. In this study, samples of a 100-nm-thick BOX layer were fabricated to investigate the intrinsic breakdown electric field within the 200 V limit of the measurement device.

3.4.1.2.4 Analysis of density of BOX layer

The density of the BOX layer was evaluated by XRR. Small chips were cut from the annealed BOX layer on the base wafer for XRR analysis. The BOX layer was analyzed by irradiating X-rays on its surface. The X-ray used in this analysis was the Cu Kα1,2 line at 0.15046 nm and the irradiation angle ranged from 0 deg to 2 deg in steps of 0.002 deg.

3.4.1.2.5 Analysis of binding density in BOX layer

The density of Si–O bonds in the BOX layer was evaluated by the FT-IR method. Small chips were cut from the annealed BOX layer on the base wafer for FT-IR analysis. The BOX layer was analyzed by irradiating light from a SiC light source to its surface. A DTGS detector, a Ge/KBr beam splitter, a resolution of 8 cm^{-1}, and an accumulation number of 2500 were used.

3.4.2 Experimental results

3.4.2.1 Evaluation of remaining voids after bonding a bonding wafer to BOX layer on base wafer

A 10-μm-thick BOX layer was deposited on the base wafer. A thickness of approximately 20 nm of the surface of the deposited BOX layer was then polished, and the bonding wafer was bonded to the polished BOX layer by SAB at room temperature under a pressure of 1×10^{-5} Pa. This sample was examined for any remaining voids by IR transmission imaging. Figure 3.16 shows the IR transmission image, which shows a lattice-like pattern. The image does not show any defects in the bonding wafer. Therefore, this studied sample has no voids in the wafer.

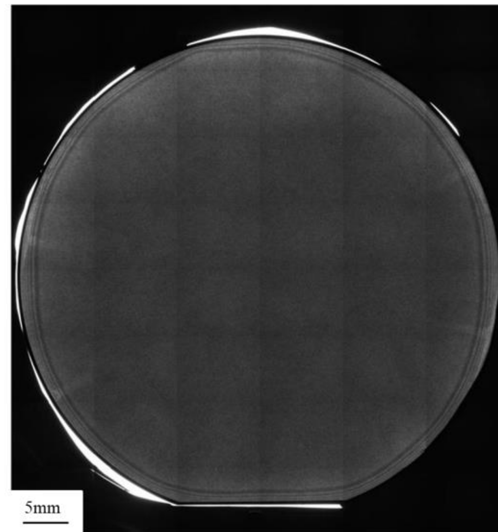


Fig. 3.16. IR transmission image of 2-inch-diameter wafer with a silicon wafer bonded to the BOX layer on the base wafer.

The studied SOI wafer was diced and the bonding interface of the chips taken from the center of the wafer was observed by cross-sectional TEM. Figure 3.17 (a) shows the cross-sectional TEM image of the fabricated SOI wafer. The bonding interface was flat and had no microvoids. In addition, at the bonding interface of the bonded silicon layer of the bonding wafer, there was a 5-nm-thick amorphous layer. This amorphous layer was generated by irradiating argon ions to activate the surface of the silicon layer of the bonding wafer during the SAB process.[36] In addition, there was a 1-nm-thick white layer under this amorphous layer at the bonding interface. Figure 3.18 shows the SAB process for bonding the bonding wafer (silicon layer) to the BOX layer on the base wafer.[113] First, a bonding wafer and a base wafer with a BOX layer are set in the bonding device, as shown in step (1) in Fig. 3.18. Argon ions are then irradiated onto the surface of the bonding wafer, and silicon atoms are sputtered from the surface of the bonding wafer, as shown in step (2). Consequently, the sputtered silicon atoms are deposited on the top surface of the BOX layer, as shown in step (3). Finally, the deposited silicon layer acts as an adhesive layer that bonds the bonding wafer to the BOX layer, as shown in step (4). Therefore, the white layer at the bonding interface is the silicon layer deposited on the top surface the BOX layer by the sputtering of silicon atoms at the surface of the bonding wafer during the SAB process.

The cross section of the bonding interface after heat treatment was also observed to evaluate the thermal stability of the bonding interface during device fabrication processes. This heat treatment was carried out at a temperature above 700°C in an ambient atmosphere of nitrogen gas in a furnace as a device fabrication process, as shown in Fig. 3.15. Figure 3.17 (b) shows the cross-sectional TEM image obtained after this heat treatment. Extended defects

such as punch-out dislocations were not generated at the bonded interface nor were any new microvoids formed. On the other hand, the amorphous layer at the bonding interface was not observed as it was recrystallized during this heat treatment. Therefore, the bonding interface between the bonding wafer and the deposited BOX layer was thermally stable during the device fabrication processes.

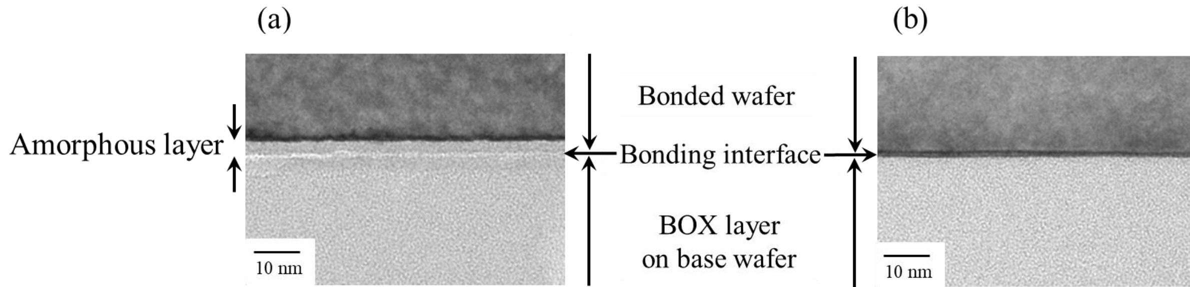


Fig. 3.17. Cross-sectional TEM images of bonding interface. (a) After fabricating the SOI wafer (before heat treatment) and (b) after the heat treatment in device fabrication.

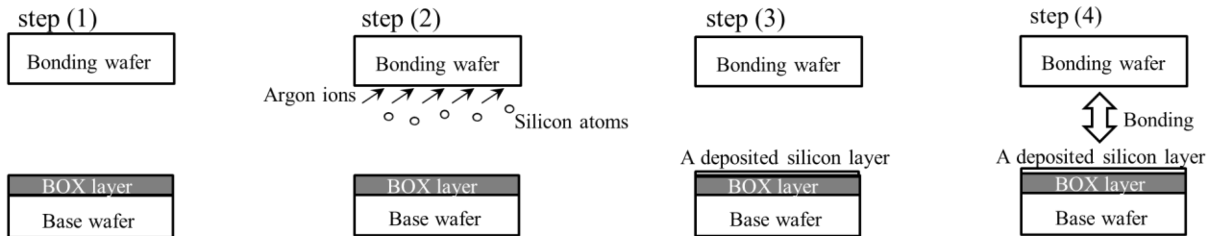


Fig. 3.18. Flow of SAB of a bonding wafer to the base wafer with a BOX layer.

3.4.2.2 Evaluation of breakdown electric field of deposited BOX layer

The breakdown electric field of the BOX layer of the studied and reference SOI samples was measured by TZDB.[110)] The reference sample was fabricated by oxidation at 1050°C for 23 min in an oxygen atmosphere.

Figure 3.19 shows the results of TZDB measurement for the studied samples 1 (deposited silicon oxide film without annealing) and 2–7 (deposited silicon oxide film with annealing at 300, 500, 700, 900, 1050°C) and the reference sample (thermal oxide film). The x-axis is the effective electric field calculated as the voltage divided by the thickness of the silicon oxide film, and the y-axis is the electrical current flowing into the silicon oxide film. When the leakage current from the silicon layer to the base wafer through the BOX layer was higher than 1×10^{-4} A/cm^2, the breakdown electric field was considered intrinsic in this study. The breakdown electric fields are shown in Fig. 3.19 (1–7) for the reference sample and samples 1–6. The breakdown electric field of the samples was 11–14 MV/cm.

On the other hand, the leakage current of the samples varied up to 1×10^{-4} A/cm^2. When the leakage current was higher than 5×10^{-6} A/cm^2, the breakdown electric field was considered to be in accident mode. The breakdown electric field was determined to be 12.5 MV/cm for the reference sample, 6.5 MV/cm for sample 1, 9.0 MV/cm for sample 2, 10.05 MV/cm for sample 3, 11.5 MV/cm for sample 4, 12.5 MV/cm for sample 5, and 8.95 MV/cm for sample 6. The accident-mode breakdown electric field of the deposited silicon oxide film was less than that of the thermal oxide film.

Figure 3.20 shows the relationship between the annealing temperature and the effective electric field for the intrinsic mode [Fig. 3.20 (a), C mode] and the accidental mode [Fig. 3.20 (b), B mode]. According to Fig. 3.20 (a), the effective electric field of the intrinsic mode for

the deposited silicon oxide film was 13–14 MV/cm, which is similar to that for the thermal oxide film. However, it decreased to a value of less than 12 MV/cm after annealing at 1050°C. According to Fig. 3.20 (b), the effective electric field of the accident mode for the deposited silicon oxide film was one-half that for the thermal oxide film and increased upon annealing treatment up to 900°C, but after annealing at 1050°C, it decreased to become the same as that at 300°C. Therefore, the deposited silicon oxide film initially might not be dense, similar to the thermal oxide film, but it became dense upon annealing in an oxygen atmosphere.

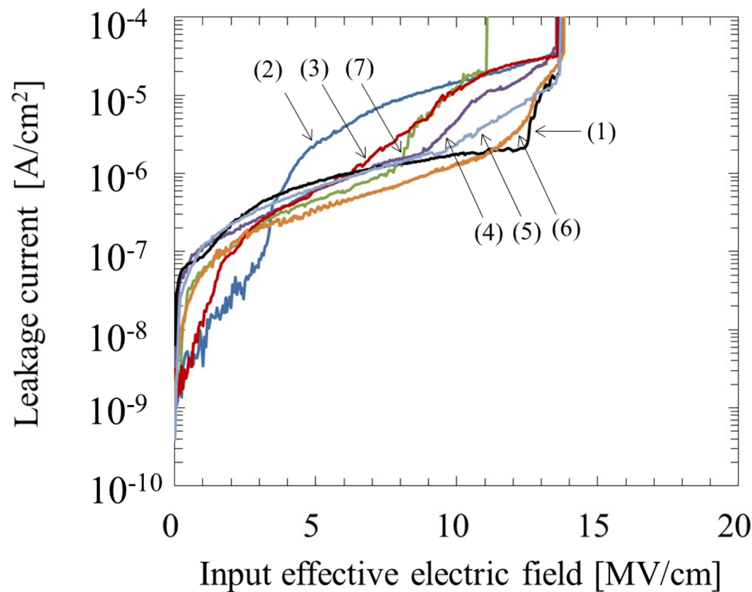


Fig. 3.19. TZDB measurement results for BOX layer. (1) Thermal oxide film (reference sample), (2) deposited silicon oxide film without annealing (sample 1), and deposited silicon oxide film with annealing at (3) 300, (4) 500, (5) 700, (6) 900, and (7) 1050°C (samples 2, 3, 4, 5, and 6, respectively).

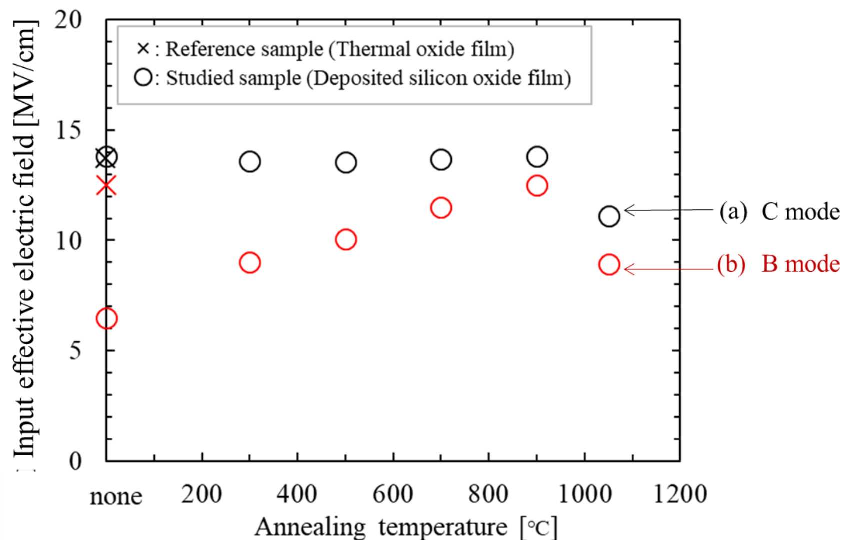


Fig. 3.20. Relationship between annealing temperature and effective electric field as determined by TZDB measurement. (a) Intrinsic mode (C mode) and (b) accidental mode (B mode).

3.4.3 Discussion

Figure 3.21 shows the electric current flowing into the insulator layer, determined by TZDB measurement.[110] An electric current generally flows into the insulator layer in three modes, A, B, and C, as shown in Fig. 3.21 (a). The A-mode electric current is mainly generated by metallic impurities contaminated in the insulator layer, as shown in Fig. 3.21 (b-1). Since the impurities act as low-resistivity spots in the isolator layer, electric current flows through the contaminated region at a low electric field. The B-mode electric current is unintentionally generated in the insulator layer because of the degradation of the quality of the layer owing to, for example, defects in the layer, as shown in Fig. 3.21 (b-2). The C-mode electric current is an intrinsic quality of the layer and is unaffected by metallic impurities in the isolator layer or the degradation of the quality of the layer, as shown in Fig. 3.21 (b-3).

Figure 3.20 shows the (a) C-mode and (b) B-mode electric currents. As can be seen in Fig. 3.20 (b), the effective electric field of the B-mode was increased by annealing in an oxygen atmosphere because annealing caused the density of the deposited layer to increase. However, after 1050°C annealing, the effective electric fields of the B- and C-modes decreased from those of the sample annealed at 900°C. Because each annealing treatment in this study was carried out using the same heat treatment furnace, the difference in the concentration of the contaminating impurities during each heat treatment would be small. Then, the deposited layer becoming less dense upon annealing at 1050°C might be explained as follows. Because the BOX layer is deposited at a low temperature of 300°C, the binding energy between silicon and oxygen atoms in the deposited silicon oxidation layer is low. Consequently, because silicon and oxygen atoms might diffuse from the deposited silicon oxide film at high temperatures such as 1050°C, the density of the silicon oxide film would decrease.

To verify the above hypothesis, the density of the silicon oxide film was analyzed by XRR. Figure 3.22 shows the results of the XRR analysis. The x-axis shows the annealing temperature, and the y-axis shows the density of the silicon oxide film. The density of the reference sample was 2.26 g/cm^3. This is the same as the density of a conventional thermal oxide film.[114,115] For the studied sample, the density of the deposited silicon oxide film was 2.27 g/cm^3, and those of the samples annealed at 300–900°C were 2.25–2.27 g/cm^3. These values are the same as that for the conventional thermal oxide film.[114,115] Because the error of this analysis is about ±1%, the densities of the deposited silicon oxide films with and without annealing can be considered to be the same as that of the thermal oxide film of the reference sample. However, the density of the deposited BOX layer annealed at 1050°C was 2.19 g/cm^3, which is a 3.5% decrease from that of the deposited BOX layer before annealing (2.27 g/cm^3). Therefore, the deposited BOX layer became less dense upon annealing at 1050°C.

Figure 3.23 shows the model of this phenomenon. In general, SiO_2, which forms the silicon oxide film, comprises Si^{4+} and O^{2-} in the form of tetrahedral structures of $(SiO_4)^{4-}$, as illustrated in Fig. 3.23 (a).[116] Since the silicon oxide film is connected by bridging oxygen and forms a network structure, as illustrated in Fig. 3.23 (b-1), this film has ionic bonds. When the quality of the silicon oxide film decreases, other than the oxygen in the contaminating metallic impurities, the tetrahedral structure of $(SiO_4)^{4-}$ lacks oxygen. This oxygen insufficiency is replenished by annealing in an oxygen atmosphere, as illustrated in Fig. 3.23 (b-2). On the other hand, oxygen is lost from the tetrahedral structure of $(SiO_4)^{4-}$ by annealing at high temperatures such as 1050°C and a new lack of oxygen is generated, as illustrated in Fig. 3.23 (b-3).

To verify the above model, the Si–O bond in the BOX layer was analyzed by the FT-IR method. Figure 3.24 shows the results of the FT-IR analysis. The x-axis shows the annealing temperature, and the y-axis shows the signal strength of the Si–O bond at 1050–1100 cm^{-1} divided by the thickness of the silicon oxide film.[117–122] The signal strength of the Si–O bond was increased by annealing the deposited BOX layer, and it was maximum after annealing at

900°C. This trend is similar to that of the breakdown electric field in the B-mode shown in Fig. 3.20 (b). Therefore, the oxygen in the deposited BOX layer was replenished by annealing in an oxygen atmosphere, and the layer became denser than before annealing. However, when annealing at 1050°C, oxygen diffuses from the deposited BOX layer, and the density of the layer becomes less than that after annealing at 900°C; consequently, the breakdown electric field in the B mode decreases.

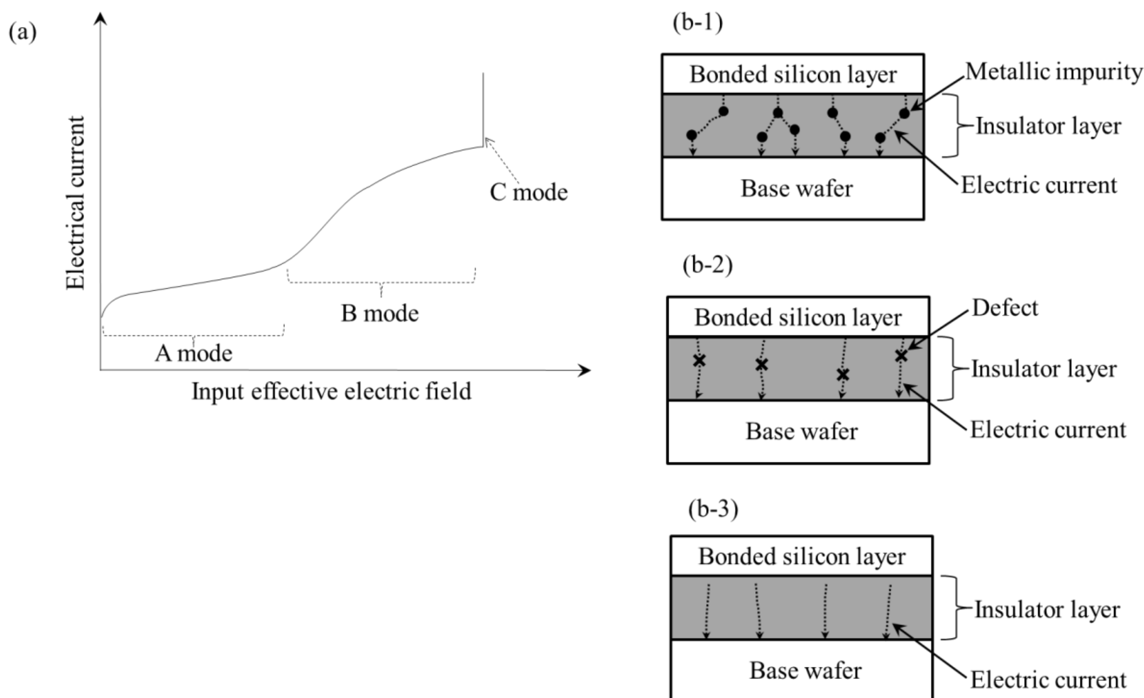


Fig. 3.21. Leakage current modes for an insulator layer. (a) Electric current flows into the insulator layer. (b-1) Metallic impurities contaminate the isolator layer. (b-2) Defects form in the isolator layer. (b-3) Intrinsic mode of isolator layer.

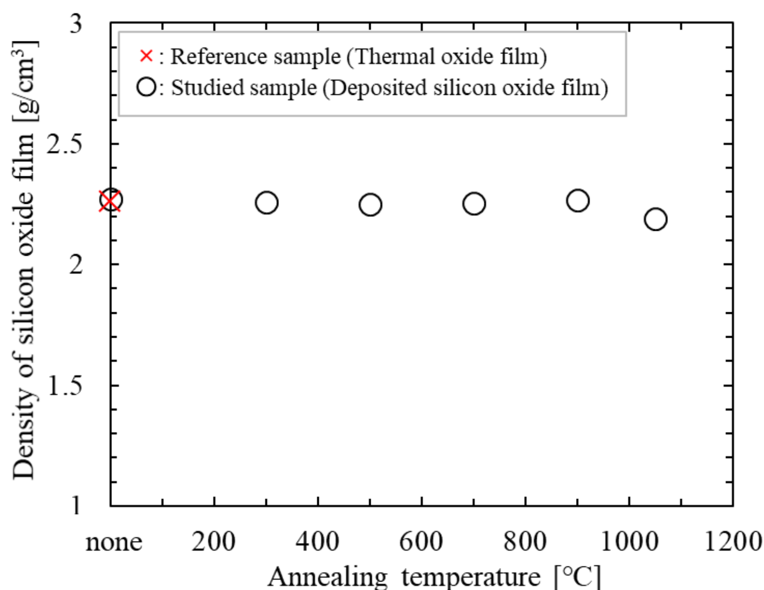


Fig. 3.22. Relationship between annealing temperature and density of silicon oxide film determined by XRR analysis.

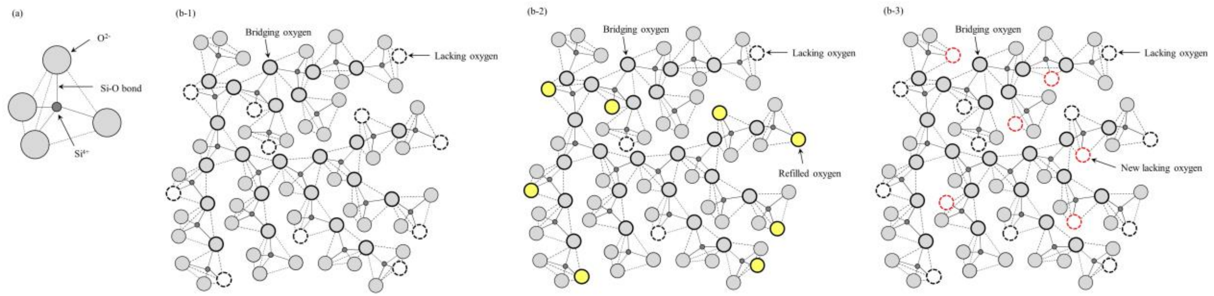


Fig. 3.23. Model of the structure of silicon oxide film with annealing. (a) Unit structure, (b-1) silicon oxide film, (b-2) replenishing of oxygen atoms to silicon oxide film by annealing in oxygen atmosphere, and (b-3) lack of oxygen atom in silicon oxide film after annealing at high temperature.[123)]

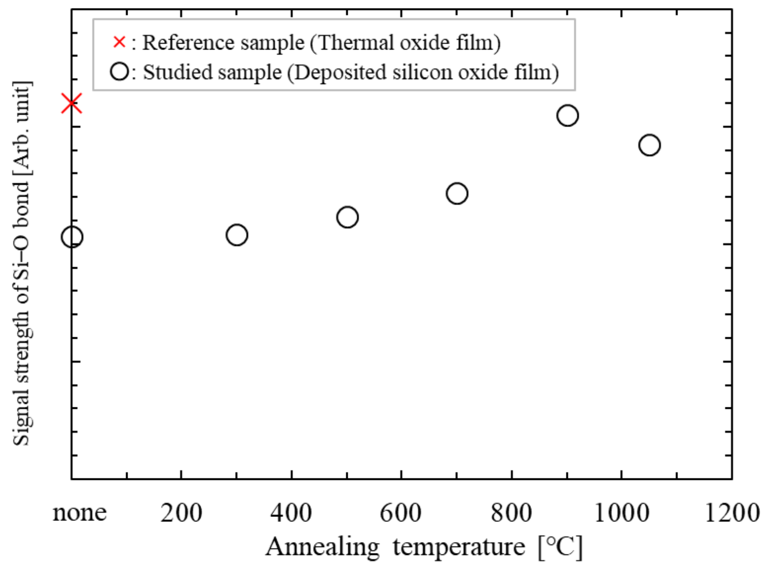


Fig. 3.24. Relationship between annealing temperature and signal strength of Si–O bond, determined by FT-IR analysis.

3.4.4 Summary

In this section, the SOI wafer with a deposited and annealed BOX layer was studied to increase the density and breakdown electric field of the BOX layer. The BOX layer of 10 μm thickness was deposited by PE-CVD at a low temperature of 300°C and made dense by annealing at a temperature above 300°C in an oxygen atmosphere. The intrinsic C-mode breakdown electric field of the BOX layer is the same as that of the thermal oxide film. In addition, the problem of the occurrence of the B mode is alleviated by annealing at a temperature higher than 300°C.

3.5 SOI wafer with SiO*x* BOX layer

3.5.1 Experimental methods and results

An SOI wafer with a SiO_x ($x < 2$) BOX layer was studied to investigate the possibility of reducing the membrane stress around the BOX layer after the fabrication of the SOI wafer and heat treatment. Figure 3.25 shows the experimental procedure for fabricating an SOI wafer with decreased stress of the BOX layer. Table 3-IV shows the specifications of the two types of sample used in this study. Sample A is a silicon wafer with the SiO*x* layer on the top and is used for evaluating and analyzing the deposited SiO*x* layer, as in steps (b-1–5) in Fig. 3.25. Sample B is an SOI wafer and is used for the evaluations in steps (b-6–10).

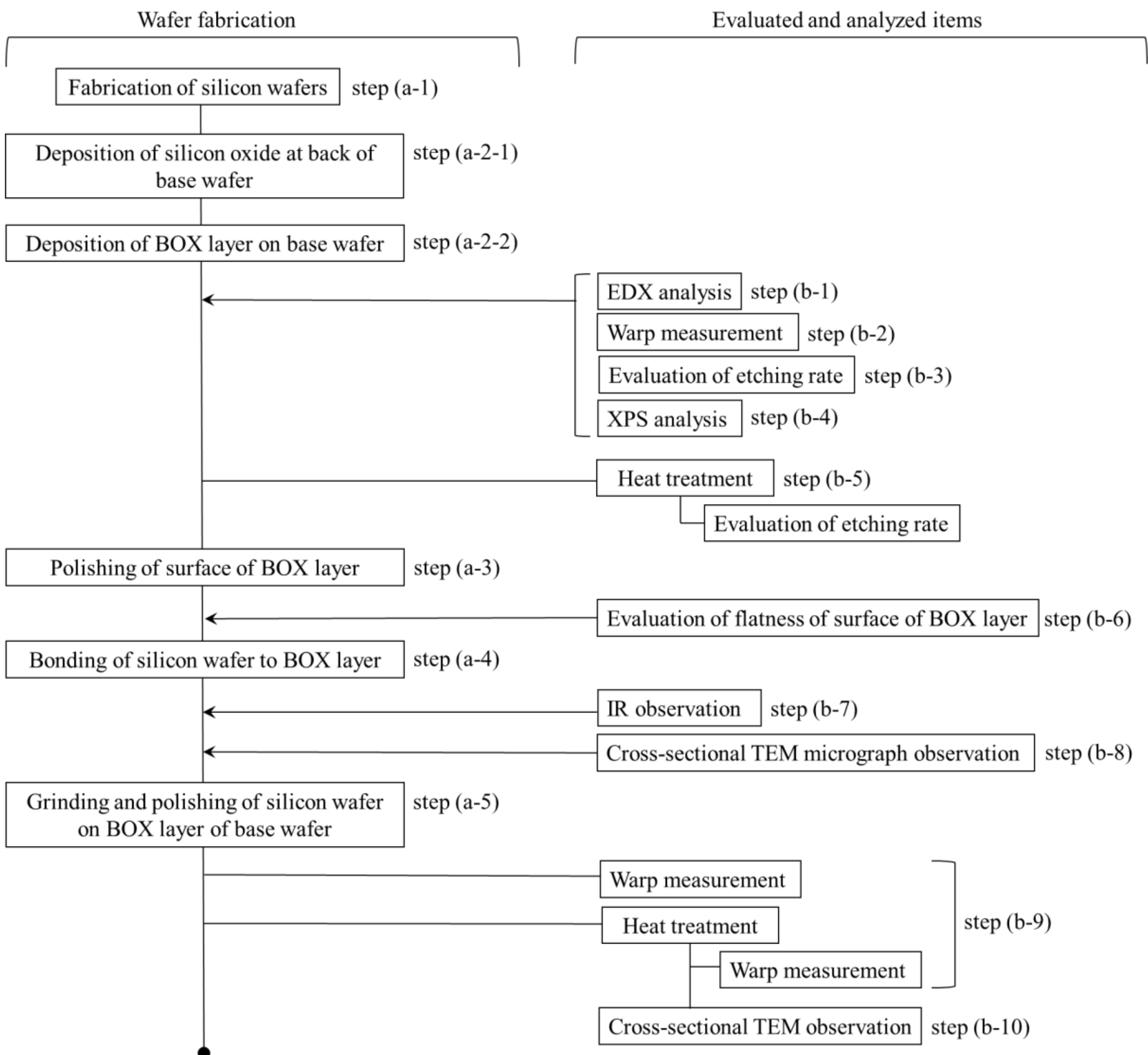


Fig. 3.25. Flowchart of experiment.

Table 3-IV. Specifications of samples used in this study.

	Base wafer	BOX layer	Bonding wafer (Silicon layer)	Bottom-side silicon oxide film	
Sample A	p-type (boron-doped) 5 Ω·cm Oi: 1.2 × 10^{18} atoms/cm^3 4 inch diameter , 525 μm	2.5 μm	NA (0 μm)	NA (0 μm)	BOX layer Silicon substrate
Sample B	p-type (boron-doped) 5 Ω·cm Oi: 1.2 × 10^{18} atoms/cm^3 4 inch diameter , 525 μm	2.4 μm	p-type (boron-doped) 5 Ω·cm Oi: 1.0 × 10^{18} atoms/cm^3 4 inch diameter 525 μm (before grinding) 10–17 μm (after grinding)	2.5 μm	Silicon layer BOX layer Silicon substrate Silicon oxide film

3.5.1.1 Deposition of BOX layer on base wafer

Four-inch (100) boron-doped CZ silicon wafers of p-type with a thickness of 525 μm were prepared as the base and bonding wafers [step (a-1) in Fig. 3.25]. Their resistivity was 5 Ω·cm and their oxygen concentration was 1.0–1.2 × 10^{18} atoms/cm^3. First, a SiO_x film was simultaneously deposited on both the top and bottom sides of the silicon wafer by PE-CVD. Tetramethylsilane [$Si(CH_3)_4$], oxygen (O_2), and argon (Ar) were used. The deposition was carried out at a high temperature of 500°C for 1 h so that the deposited layer was highly dense, under 10 Pa with a 13.56 MHz RF power of 700 W using a parallel-plate 6-inch PE-CVD tool (Tsukishima Kikai Co., Ltd.) [steps (a-2-1) and (a-2-2) in Fig. 3.25]. As summarized in Table 3-V, the amounts of $Si(CH_3)_4$ and O_2 gases were varied to change the component ratio of silicon to oxygen atoms in the deposited BOX layer.

The components of the deposited BOX layer were analyzed by EDX (Genesis APEX2, Country) [step (b-1) in Fig. 3.25]. Figure 3.26 shows the results of the EDX analysis. The x-axis shows the ratio of oxygen gas to $Si(CH_3)_4$ and the y-axis the ratio of oxygen to silicon (O/Si). The O/Si ratio was varied between 0.36 and 2.0 by changing the amounts of $Si(CH_3)_4$ and O_2 gases. As the ratio of gases increased, O/Si also increased.

Table 3-V. Conditions of gas flow into the CVD chamber during BOX layer deposition.

	$Si(CH_3)_4$ [sccm]	O_2 [sccm]	Ar [sccm]
Condition 1	25	100	0
Condition 2	25	68	0
Condition 3	25	57	20
Condition 4	25	50	40
Condition 5	25	25	40
Condition 6	25	16	40
Condition 7	25	10	40
Condition 8	25	7	40
Condition 9	25	5	40

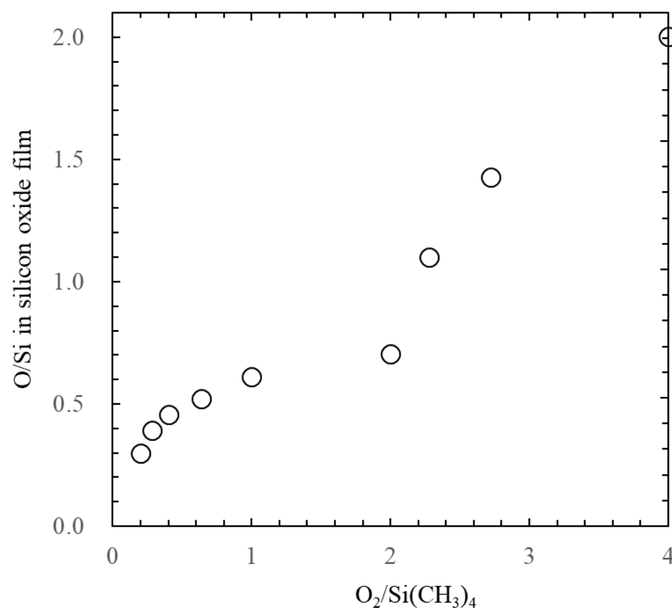


Fig. 3.26. Relationship between ratio of gases [$O_2/Si(CH_3)_4$] and O/Si.

3.5.1.2 Measurement of warpage of deposited wafer

The warpage of Sample A was measured at room temperature in air using an optical wafer morphology analyzer (FLX-2320-S, Toho Technology Corporation, Japan) [step (b-2) in Fig. 3].[124–126] Figure 3.27 shows the in-plane map of warpage of a reference sample (O/Si = 2.0, condition 1). The morphology of the wafer is concentric, suggesting that the stress of the SiO_x layer is fairly uniform throughout the surface. This is also the case with other samples, and thus, the center deflection can be used as the amount of warpage.

Figure 3.28 shows the center deflection plotted against O/Si in a silicon oxide film. The calculated stress of the SiO_x layer is also shown. As O/Si decreased, the amount of warpage decreased. When O/Si was less than 0.59, the amount of warpage decreased to less than one-half that when O/Si was 2.00. The calculated results are shown on the right y-axis. Because the membrane stress was negative, the deposited layer had compressive stress. As O/Si decreased, the absolute value of membrane stress decreased. The membrane stress with O/Si = 0.36 was one-half that with O/Si = 2.00. Therefore, the compressive stress can be decreased by using a silicon-rich oxide film.

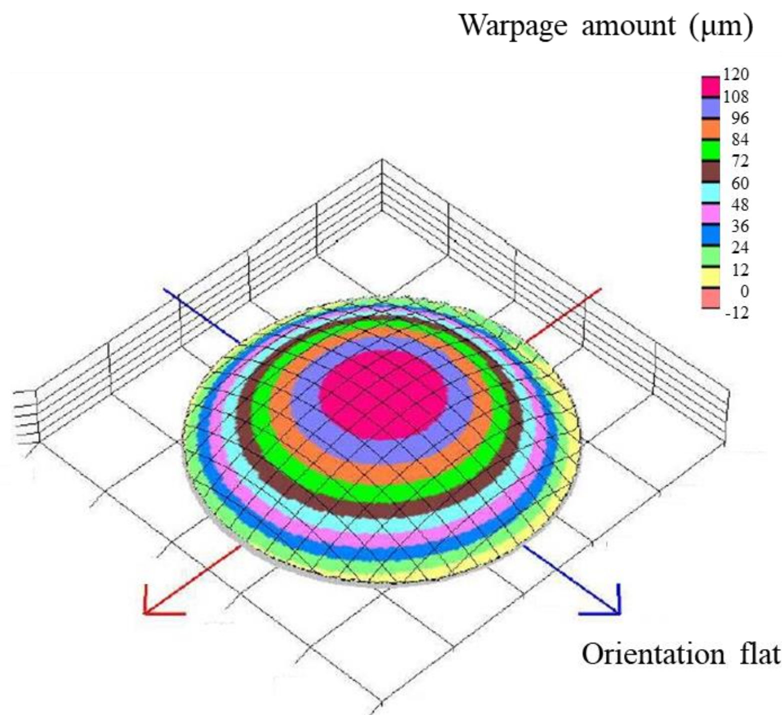


Fig. 3.27. In-plane map of warpage of reference sample (O/Si = 2.00, Condition 1).

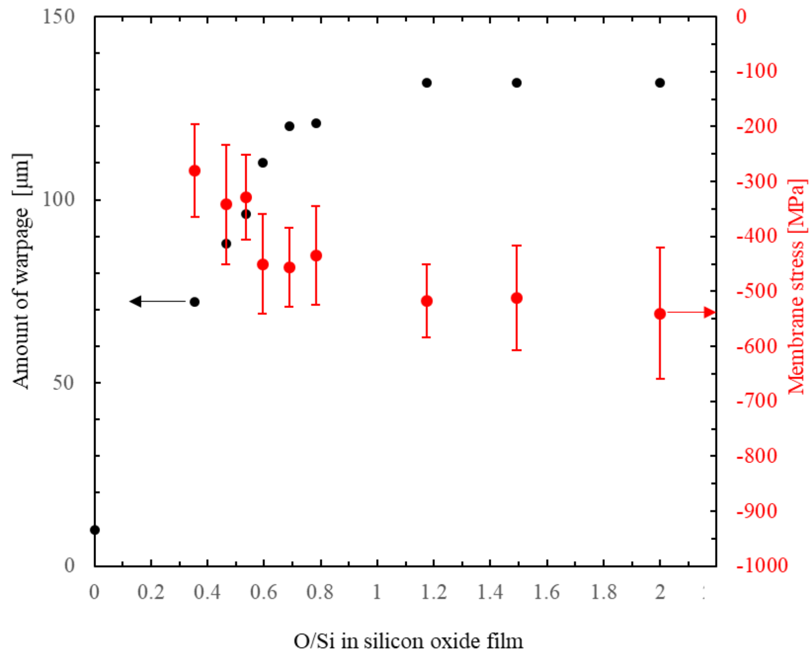


Fig. 3.28. Relationship between O/Si and amount of warpage and membrane stress of deposited BOX layer.

3.5.1.3 Evaluation of etching rate of deposited BOX layer on base wafer

The etching rate of the BOX layer was evaluated using HF [step (b-3) in Fig. 3.25]. After masking half of the area of the chip diced from sample A using acid-resistant tape, the chip was dipped into an aqueous HF solution of 30% weight concentration of HF at room temperature. Figure 3.29 shows the relationship between O/Si and the etching rate. As O/Si decreased, the etching rate decreased. In particular, when O/Si = 0.69, the etching rate decreased to one-half that when O/Si = 2.00. In addition, when O/Si was less than 0.54, the etching rate decreased to one-tenth that when O/Si = 2.00.

The thermal stability of the etching rate of the SiO_x layer was evaluated. Figure 3.30 shows the time history of heat treatment in the gate oxidation or annealing process after doping elements such as boron and phosphorus as carriers. This heat treatment was carried out at 1050°C for 15 min in an oxygen or nitrogen atmosphere, and the wafers were loaded and unloaded in the heat treatment furnace at 900 °C in a nitrogen atmosphere using a Model 200 device (ULVAC) [step (b-5) in Fig. 3.25]. The results are additionally plotted in Fig. 3.29. When O/Si was less than 0.79, the etching rate markedly decreased. The results showed the same trend as that before heat treatment.

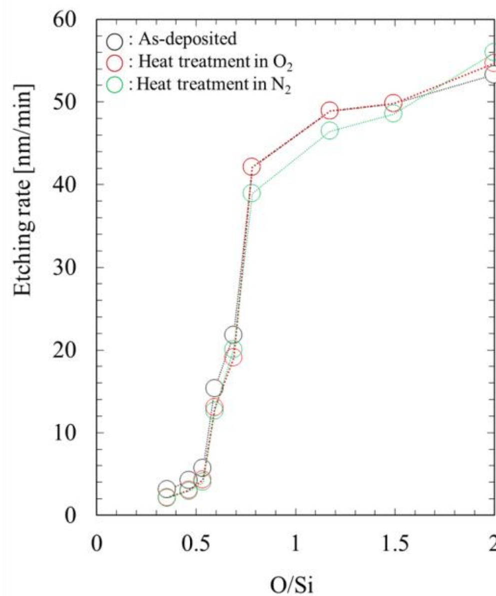


Fig. 3.29. Relationship between O/Si and etching rate of deposited BOX layer.

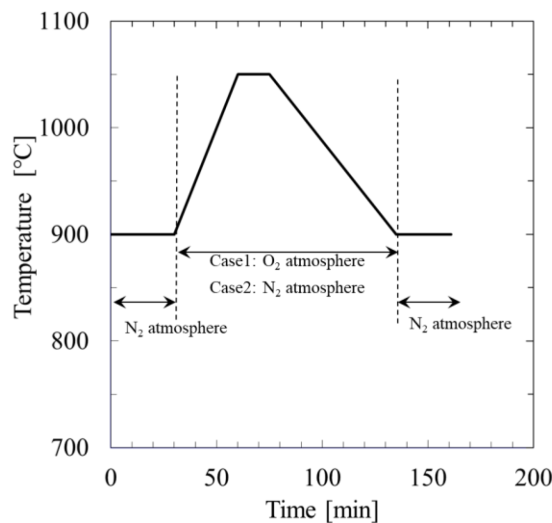


Fig. 3.30. Time history of heat treatment showing the maximum temperature for the device fabrication process.

3.5.1.4 Polishing of surface of deposited BOX layer on base wafer

The top surface of the deposited layer of 100 nm thickness was polished from 2.5 μm to 2.4 μm by CMP to reduce the roughness [step (a-3) in Fig. 3.25], and the flatness of the top surface was then measured by atomic force microscopy (AFM) using the Dimension Icon system (Bruker) [step (b-6) in Fig. 3.25]. The average roughness (Ra) decreased from 0.14 nm to 0.13 nm over an area of 100 μm^2. The roughness after depositing the BOX layer was good. Since Ra should generally be less than 1 nm for SAB, this Ra is sufficient for bonding a silicon layer to the polished BOX layer by SAB.[57,58,127-129)]

3.5.1.5 Bonding of wafer to polished BOX layer

A base silicon wafer was bonded to the polished BOX layer by SAB at room temperature in an ultrahigh vacuum of less than 1×10^{-5} Pa (Nidec Machine Tool Corporation, MWB-08-AX) [step (a-4) in Fig. 3.25]. The surface of the silicon wafer and the BOX layer were activated by argon ion irradiation. The following were the bonding conditions: applied voltage, 1.5 kV; plasma current, 100 mA; argon ion irradiation time, 5 min; and load, 100 kN.

To evaluate whether voids exist in the bonding region, IR transmission observation was carried out after SAB. An IRise (Moritex) system was used for this observation [step (b-7) in Fig. 3.25]. Figure 3.31 shows the representative results of the IR transmission observation of a reference sample (condition 1). The lattice pattern in the IR transmission image does not show any defects in the bonded wafer. No white spots were observed in the wafer and there were no voids.

In more detail, a cross section of the bonded region was observed by TEM using an H9000UHR-I microscope (Hitachi) to characterize structural defects such as microvoids or SAB-induced defects formed during the fabrication of the SOI wafer [step (b-8) in Fig. 3.25]. Figure 3.32 (a) shows a TEM cross-sectional image of the bonded interface in a diced sample of the SOI wafer at its center. There were no microvoids, and an amorphous layer of 3.7 nm thickness was formed on the side of the bonded wafer in the bonding region. In the SAB process, argon ion irradiation to activate the surface of the silicon wafer for bonding to the BOX layer transforms the silicon crystal to an amorphous layer at the surface of the bonded wafer.[123,130–133)] The transformation of the amorphous layer under the bonding wafer from a silicon crystal upon irradiation enables the bonding of a wafer to the BOX layer deposited on the base wafer without the generation of voids.

In addition, the fabricated SOI wafer was heat-treated at 1050°C for 15 min in an oxygen atmosphere using a Model 200 device (ULVAC) [step (b-10) in Fig.3.25], as shown in Fig. 3.30. Figure 3.32 (b) shows the cross-sectional TEM image taken after this heat treatment. No new voids or extended defects such as punch-out dislocations were observed in the bonding region. On the other hand, the amorphous layer observed at the bonding interface before heat treatment disappeared, and moiré patterns were observed in the region where the amorphous layer was observed before heat treatment. The amorphous layer was recrystallized during heat treatment.

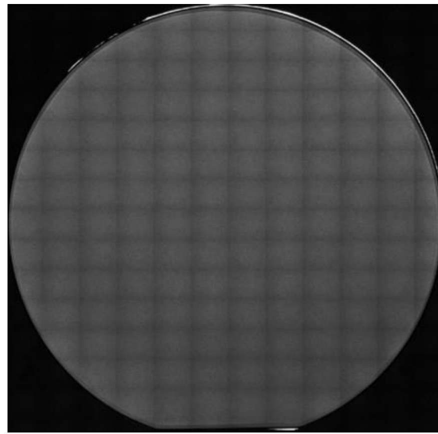


Fig. 3.31. IR transmission image of 4-inch-diameter wafer after bonding wafer to BOX layer of base wafer by SAB.

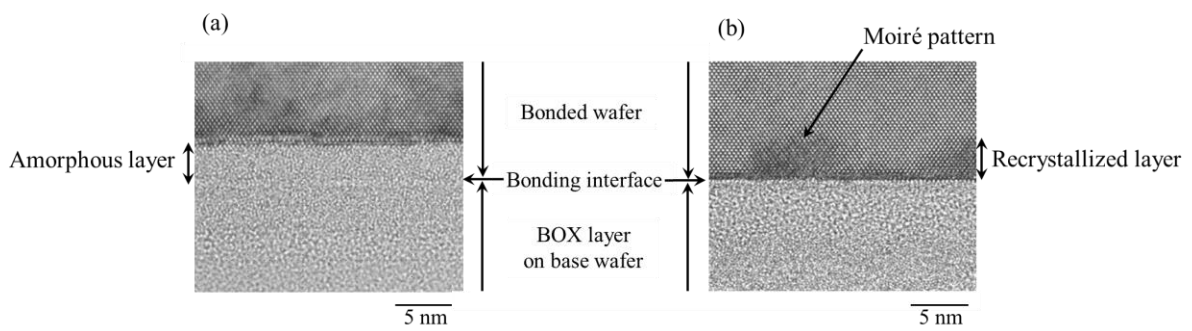


Fig. 3.32. Cross-sectional TEM images (a) after bonding wafer to BOX layer by SAB and (b) after heat treatment in device fabrication.

3.5.1.6 Measurement of warpage of SOI wafer after heat treatment

The bonded wafer was ground and polished until a silicon layer of 10 μm thickness was formed [step (a-5) in Fig. 3.25]. After fabricating the SOI wafer (sample B), it was heat-treated at 1050 °C for 15 min in an oxygen atmosphere using a Model 200 device (ULVAC), as shown in Fig. 3.30. Then, the amount of warpage of the heated SOI wafer was measured [step (b-9) in Fig. 3.25]. Figure 3.33 shows the amount of warpage and stress of the silicon layer on the BOX layer after fabricating the SOI wafer [(a) black] and after heat treatment [(b) red]. As O/Si decreased, the amount of warpage decreased after fabricating the SOI wafer. In addition, the amount of warpage decreased after heat treatment. The reference SOI wafer was formed by thermal oxidation and thermal bonding. Then, heat treatment was performed, and the sample was evaluated. The data of this sample were also plotted as (c) in Fig. 3.33. The amounts of warpage of studied samples were less than those of their wafers.

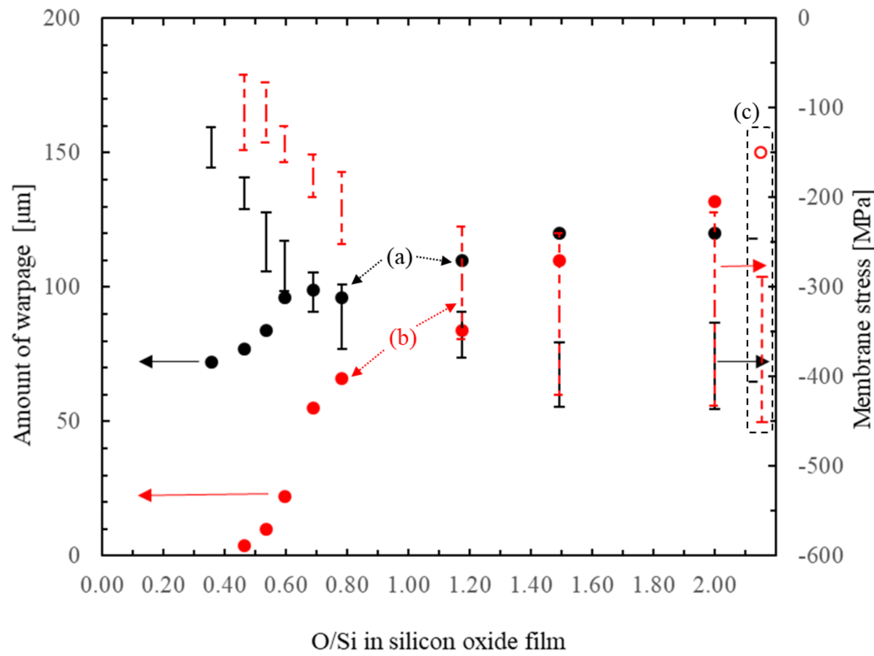


Fig. 3.33. Relationship between O/Si and amount of warpage or membrane stress of SOI wafer. (a) After fabricating SOI wafer, (b) after heat treatment, and (c) reference sample after heat treatment.

3.5.2 Discussion

Silicon oxide has a SiO_4 tetrahedral structure.[116] The mechanism of etching SiO_2 using HF aqueous solution is explained by the following reactions:[134]

$$SiO_2 + 4HF \rightarrow SiF_4 + 2H_2O, \qquad (3\text{-}2)$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6. \qquad (3\text{-}3)$$

Reactions (3-2) and (3-3) are summarized as

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O. \qquad (3\text{-}4)$$

The detailed etching reactions are shown in Fig. 3.34. First, according to Reaction (3-2), four HF molecules come into contact with SiO_4 in the silicon oxide film, as shown in Fig. 3.34 (a). Then, four oxygen ions (O^{2-}) are replaced with four fluorine ions (F^-) and two H_2O molecules are generated, as shown in Fig. 3.34 (b). In addition, according to Reaction (3-3), two additional HF molecules come into contact with SiF_4 [Fig. 3.34 (c)] and H_2SiF_6 is consequently formed as an octahedral structure [Fig. 3.34 (d)]. Figure 3.35 shows the etching phenomenon in the silicon oxide film through these reactions. Four HF elements first come into contact with SiO_4 [Fig. 3.35 (a)], four O^{2-} ions are replaced with four F^- ions and SiF_4 is formed in the silicon oxide film [Fig. 3.35 (b)]. Other HF molecules additionally come into contact with SiF_4 [Fig. 3.35 (c)], and H_2SiF_6 is consequently formed [Fig. 3.35 (d)] and dissolved into the aqueous solution [Fig. 3.35 (e)]. This process is repeated, and the etching of the silicon oxide film progresses. Because of step (b), the etching rate of the silicon oxide film is affected by the concentration of SiO_4 units in the film.

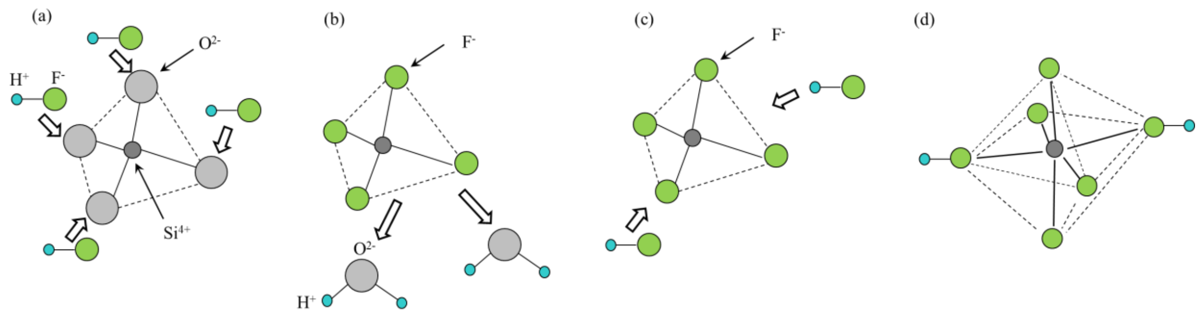


Fig. 3.34. Etching reaction between SiO_4 in silicon oxide film and HF aqueous solution.

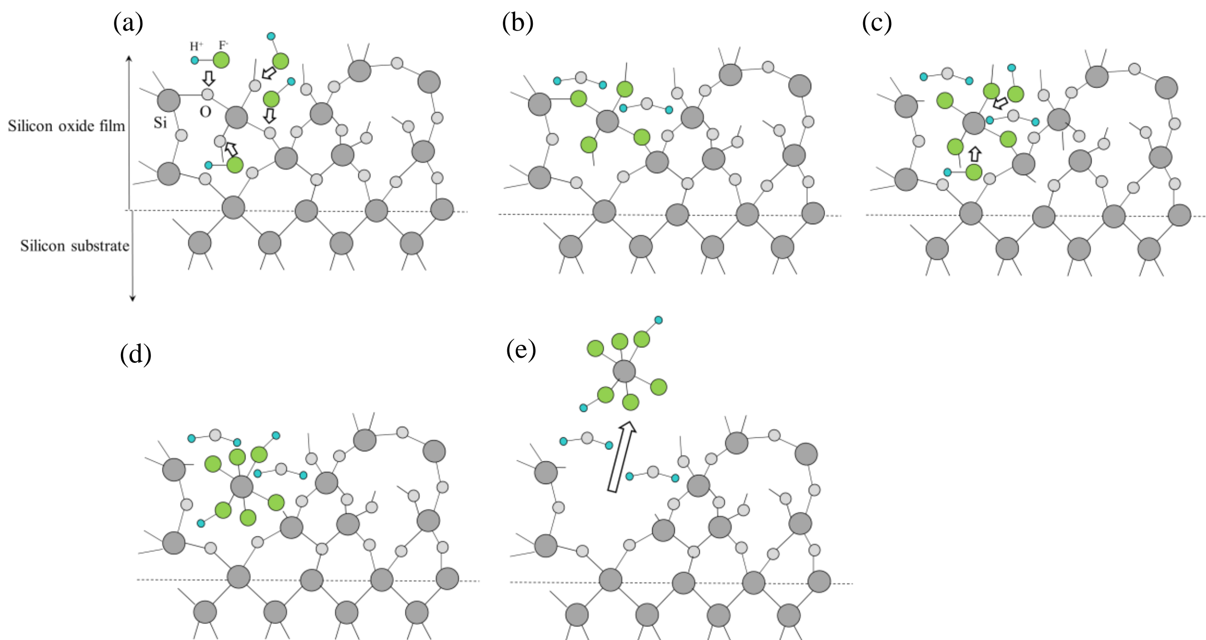


Fig. 3.35. Etching of silicon oxide film with HF aqueous solution.

Figure 3.36 shows schematics of the silicon oxide film made of SiO_x ($x \leqq 2$). When x is less than 2, the oxygen atom is replaced with the silicon atom in the film. Figures 3.36 (b-1), (b-2), and (b-3) show the schematics of SiO_2, $SiO_{1.57}$, and SiO_1, respectively. When x is 2 or 1.57, SiO_4 is made of more than two bridging oxygen atoms, as shown in Figs. 3.36 (b-1) and (b-2). The concentration of SiO_4 in the SiO_x layer will be less than one-half that of oxygen atoms in this layer. On the other hand, when x is 1, SiO_4 is made of not bridging oxygen but an oxygen atom, as shown in Fig. 3.36 (b-3). The concentration of SiO_4 in the SiO_x layer will be one-fourth that of oxygen atoms in this layer. Therefore, when x is from 1 to 2, the concentration of SiO_4 is assumed to be one-half that of oxygen atoms detected by EDX analysis, and when x is less than 1, the concentration of SiO_4 is assumed to be one-fourth that of oxygen atoms detected by EDX analysis. In addition, the concentration of SiO_4 in the SiO_x layer is normalized by that of SiO_2, and the etching rate of SiO_x is multiplied by that of SiO_2. Figure 3.37 shows the relationship between O/Si (x) and the calculated etching rate. When O/Si is less than 1, the etching rate markedly decreases. This is similar to the experimental result.

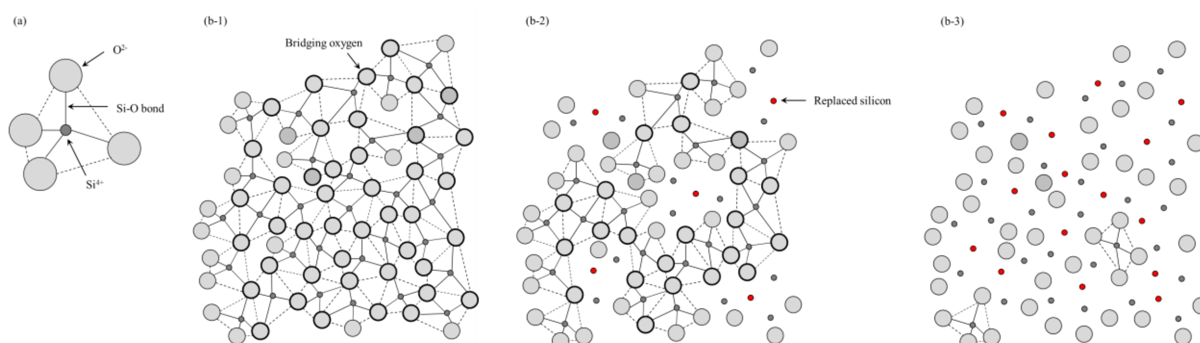


Fig. 3.36. Schematics of the silicon oxide film made of SiO_x ($x \leqq 2$). Structures of (a) SiO_4, (b-1) SiO_2, (b-2) $SiO_{1.57}$, and (b-3) SiO_1.

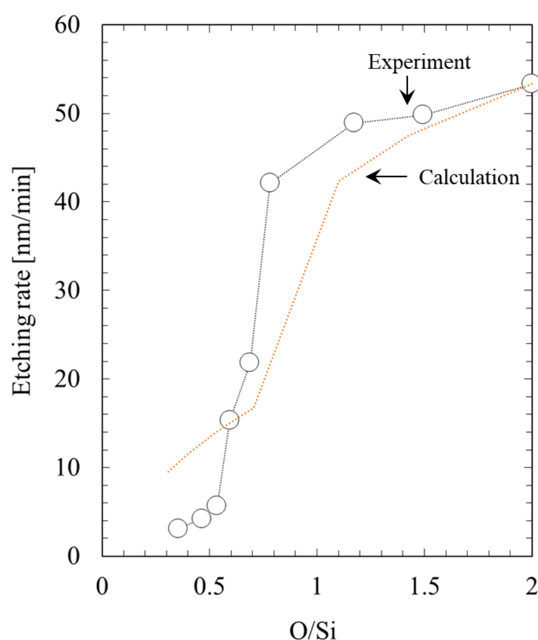


Fig. 3.37. Relationship between O/Si and etching rate of deposited BOX layer.

3.5.3 Summary

In this section, the membrane stress around the SiO_x ($x < 2$) BOX layer of the SOI wafer was reduced. The SiO_x BOX layer was deposited by PE-CVD. When x was less than 1.2, the membrane stress was decreased by more than 10% of that when $x = 2$. On the other hand, when x was less than 0.79, the etching rate markedly decreased.

3.6 Conclusions

Three types of SOI wafer fabricated using CVD and SAB technologies were studied in this chapter. They could be fabricated in less than one-tenth the time required for the reference method (thermal oxidation and thermal bonding). In the first type of SOI wafer, the BOX layer was formed to have no fixed charge without changing the resistivity in the silicon layer on the BOX layer. The second type was made to have increased density and breakdown electric field of the BOX layer by depositing and annealing the BOX layer. In the third type of SOI wafer, the stress around the BOX layer was reduced by forming the BOX layer of SiO_x ($x < 2$). These SOI wafers were the first of their kind, and these studies were the first on the respective issues. The results are summarized below.

1. In the first type of SOI wafer, the 10-μm-thick BOX layer in the SOI wafer was deposited by PE-CVD at 500°C for 4 h, and a silicon layer was bonded to the deposited BOX layer by SAB for 5 min. The BOX layer could be formed with no fixed charge, and the resistivity of the silicon layer on the BOX layer does not change. In addition, the bonding region has no voids or extended defects after bonding and heat treatment such as that in device fabrication processes. Therefore, this method can eliminate the fixed charge in the BOX layer.

2. In the second type of SOI wafer, the BOX layer was deposited by PE-CVD at 300°C for 4 h and then made dense by annealing at a temperature above 300°C in an oxygen atmosphere for 1 h. The intrinsic C-mode breakdown electric field of the BOX layer was the same as that of the thermal oxide film. In addition, the accidental B-mode breakdown electric field of the BOX layer could be improved by annealing the deposited BOX layer at a temperature higher than 300°C.

3. In the third type of SOI wafer, the BOX layer was made of SiO_x ($x < 2$) by PE-CVD at 500°C for 4 h. When x was less than 1.2, the membrane stress decreased by more than 10% from that of the reference sample ($x = 2$). Moreover, the etching rate markedly decreased when x was less than 0.79. Therefore, this method can reduce the membrane stress around the BOX layer.

Chapter 4 SOI wafers with heterogeneous layer

4.1 Introduction

SOI wafers have been used to fabricate power and high-frequency devices.[40,41] An SOI wafer has a BOX layer made of SiO_2 as the insulator layer in the wafer, as shown in Fig. 1.12 (a). Isolation regions are made of SiO_2 by STI, as shown in Fig. 1.12 (b).[35] The devices in the SOI wafer are completely surrounded by SiO_2, which comprises a BOX layer and an STI region. Since SiO_2 has a low thermal conductivity, these devices are self-heating,[135] and thus their electrical characteristics deteriorate owing to their self-heating, adversely affecting their performance. It is most important for the devices formed on the SOI wafer to release the heat generated near a device. However, the SOI wafer has not been changed from SiO_2 to an alternative material with a higher thermal conductivity than the SiO_2 layer.[45–47] The thermal conductivity of the solid conformed laminated layers (λ_{all}), as seen in Fig. 4.1 (a), is shown by

$$\lambda_{all} = \frac{t_{all}}{t_1/\lambda_1 + t_2/\lambda_2 + \ldots + t_n/\lambda_n}, \tag{4-1}$$

where t_{all} is the total thickness of the solid-conformed laminated layers, t_n the thickness of one laminated layer, and λ_n the thermal conductivity of a laminated layer.

When the devices are fabricated in the SOI wafer and the silicon substrate under the BOX layer is removed by grinding, polishing, and etching to package devices in a module, the silicon-layer-fabricated device and the BOX layer remain as the two solid formed layers. This structure is shown in Fig. 4.1 (b) and its thermal conductivity is described by

$$\lambda_{all} = \frac{t_{all}}{t_{Si}/\lambda_{Si} + t_{BOX}/\lambda_{BOX}}, \tag{4-2}$$

where t_{Si} is the thickness of the silicon-layer-fabricated device, λ_{Si} is the thermal conductivity of a silicon crystal, t_{BOX} is the thickness of the BOX layer, and λ_{BOX} is the thermal conductivity of the BOX layer. When $t_{si} = t_{BOX}$, for example, t_{si} and t_{BOX} are 10 μm, the thermal conductivity of this structure is shown by

$$\lambda_{all} = \frac{2}{1/\lambda_{Si} + 1/\lambda_{BOX}}. \tag{4-3}$$

When the BOX layer is made of SiO_2, λ_{Si} is 157 W/mK and λ_{BOX} is 1.4 W/mK.[136] Then, λ_{all} is calculated to be 2.8 W/mK. If λ_{BOX} is more than twice that of SiO_2, λ_{all} can also be more than twice 2.8 W/mK. Therefore, λ_{all} was set to be more than twice 2.8 W/mK as much as possible.

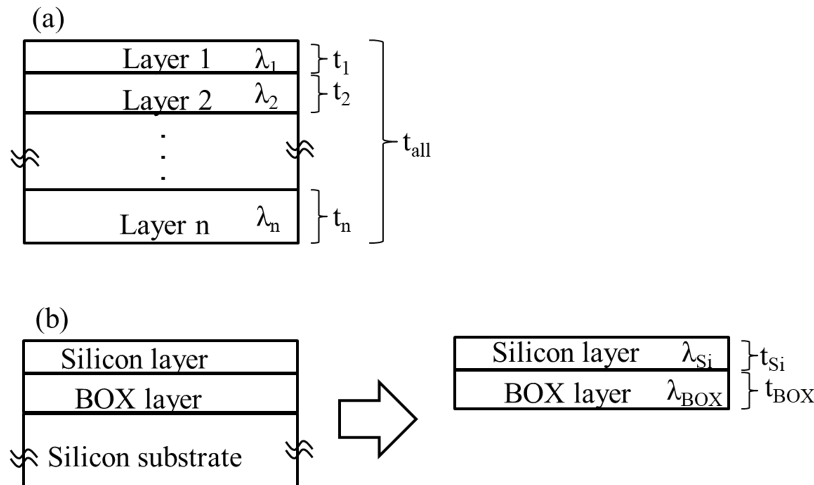


Fig. 4.1. Cross-sectional images of laminated wafer.

Wide-band-gap semiconductor materials generally have a high breakdown electric field.[137] When a BOX layer is made of a metallic compound such as GaN or Ga_2O_3, metal atoms diffuse to the device fabrication region during the fabrication of the device and the leakage currents at the pn junction and the gate layer are consequently generated. Thus, metallic compound materials cannot be used for the BOX layer. Diamond and silicon carbide (SiC) have no metal elements; thus, their breakdown electric field and thermal conductivity are high.[137] However, since the lattice constant of the single-crystalline diamond is different from that of silicon, it is impossible to deposit a single-crystalline diamond layer directly on a silicon wafer without forming crystal defects. Polycrystalline diamond can be deposited by scratching diamond powder.[138] However, in this seeding technology, the seeding density cannot be fixed and is more likely to be suited to a chip, not a wafer. In addition, the bonding of single-crystalline diamond and a single-crystalline silicon layer has been performed,[139] but the bonding of polycrystalline diamond to a silicon layer has not yet been accomplished.

On the other hand, since single-crystalline SiC is grown above 1300°C, which is near the melting point of a silicon crystal,[140] it is also difficult to deposit a single-crystalline SiC layer on a silicon wafer. In addition, the SiC layer deposited on a silicon substrate has not yet been bonded to a single-crystalline silicon layer.

4.2 Objectives

The purpose of this study is to realize a method of fabricating an SOI wafer with a BOX layer formed with a metal-free alternative material to SiO_2. I endeavored to fabricate SOI wafers with polycrystalline diamond or an amorphous SiC layer on a silicon substrate by CVD. Since diamond has the highest thermal conductivity among semiconductor materials, polycrystalline diamond is applied in devices in which reducing self-heating is the top priority. On the other hand, an amorphous SiC layer is used in devices that require a high breakdown electric field.

In addition, since the thermal expansion of BOX layers made of the above materials differs from that of a silicon wafer, the bonding of the SOI wafer cannot be carried out by a long thermal treatment above 800°C. Thus, wafer bonding by SAB at room temperature was used to bond these BOX layers without thermal stress.

4.3 SOI wafer with diamond layer

4.3.1 Experimental methods

The process of fabricating the SOI wafer with a diamond-BOX layer is shown in Fig. 4.2. Two silicon wafers, a base wafer and a bonding wafer, were fabricated. The base wafer was coated with diamond nanocrystals by spin-coating. After baking the base wafer, a diamond layer was deposited on the base wafer by microwave-plasma-enhanced chemical vapor deposition (MW-CVD). The top surface of this diamond layer was polished by CMP. Then, the bonding wafer was bonded to the polished diamond layer by SAB at room temperature in ultrahigh vacuum. Finally, the bonding wafer was ground and polished until a silicon layer was formed at the back as the active layer of the device, opposite the wafer-bonding interface.

(100) Czochralski (CZ) 2-inch-diameter silicon wafers were used. The base wafer was polished to 3 mm thickness, and the bonding wafer, used as a silicon layer, was polished to 500 μm thickness. When another material layer is deposited on a base wafer, the base wafer might become warped. Thus, the base wafer thicker than standard wafer was used. These wafers were made of a phosphorus-doped CZ silicon-single crystal of n-type. Their resistivity was 5 Ω·cm and their oxygen concentration was 1.2×10^{18} atoms/cm^3. The base wafers were coated with diamond nanocrystals in water by spin-coating. The size of these nanocrystals was below 10 nm, and they made up 5% of each coated base wafer.[131, 141] This coated base wafer was baked at 80°C for 3 min in air ambient in a clean room using a hot plate. Then, a diamond layer was deposited as the BOX layer on the base wafer between 900°C and 1200°C by MW-CVD (NIHON KOSHUHA Co., Ltd., MDD-2016). Only the top surface of this diamond layer was polished by CMP. The bonding wafer was then bonded to the polished diamond layer by SAB at room temperature in an ultrahigh vacuum under 1×10^{-5} Pa, by which the dangling bonds at the surfaces of the two wafers were connected (Nidec Machine Tool Corporation, MWB-08-AX). These dangling bonds were formed at the top surface of the two wafers by irradiating argon ions at 1–2 keV to activate the surface of the two wafers. After bonding the two wafers, the bonded wafer was ground and polished until a silicon layer of 2 μm thickness formed at the back, which is opposite the wafer-bonding interface. A reference SOI wafer was fabricated by thermal oxidation and thermal bonding. A 1.5-μm-thick BOX layer was formed on the base wafer by thermal oxidation above 900°C. The bonding wafer was bonded to the BOX layer of the base wafer by a high-temperature treatment at 800°C for 2 h and 1150°C for 1 h.[56)]

As shown in Fig. 4.2, the binding at the surface of the nanocrystalline-diamond-coated base wafer was investigated by XPS analysis after baking [step (a)]. Then, the surface of the diamond layer was observed [step (b)] and its structure was analyzed by XRD and XPS analyses [steps (c) and (d)]. The thermal conductivity of the diamond layer was then evaluated [step (e)]. Next, the flatness of the diamond layer was evaluated by AFM measurement after deposition and polishing [step (f)], and IR and cross-sectional TEM observations were performed after bonding the silicon wafer to the diamond layer to search for voids [steps (g) and (h)]. Then, the concentration of doping elements and the resistivity in the silicon layer were determined by SIMS analysis and SR measurement, and the diamond layer was analyzed by XPS analysis after grinding and polishing the bonding silicon wafer to the thickness of the active layer of the device [steps (i)–(k)]. Finally, the breakdown electric field of the diamond layer was evaluated by TZDB measurement after fabricating actual devices in the silicon layer [steps (l) and (m)]. The device fabrication process shown in Fig. 4.3 was used to fabricate a test-element group (TEG) for TZDB measurement.

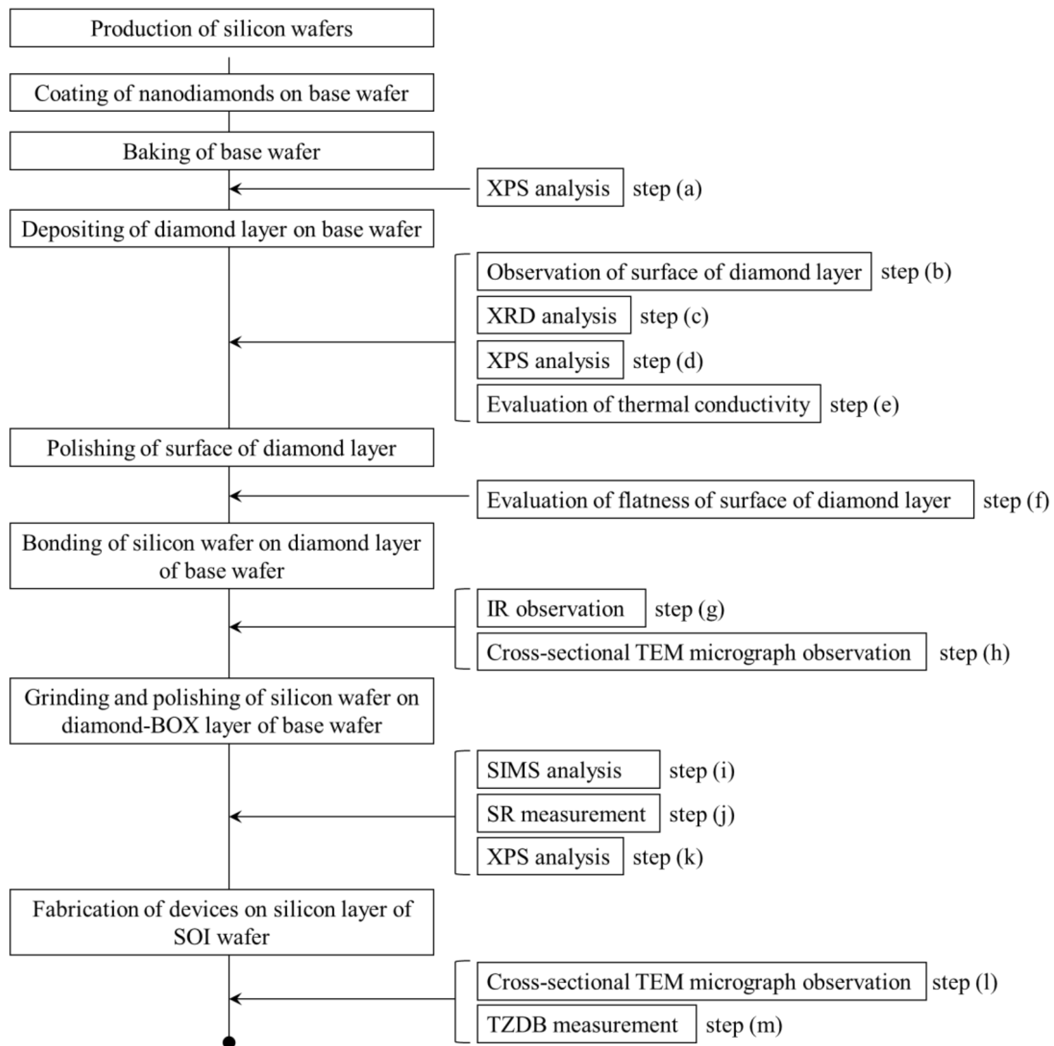


Fig. 4.2. Flow of experiment.

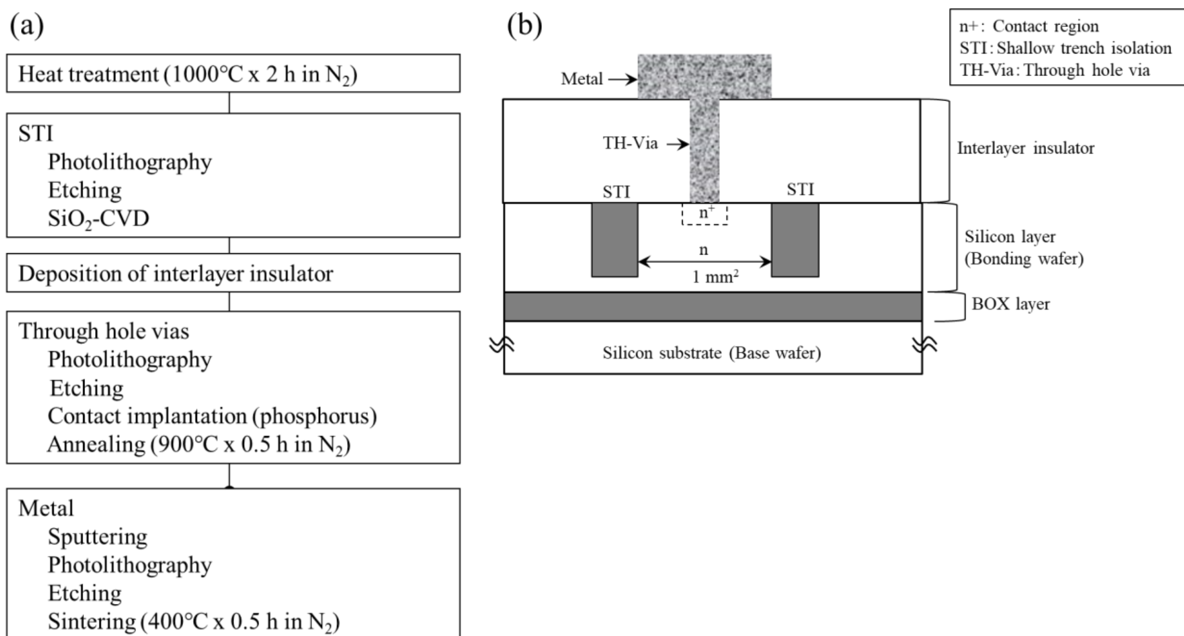


Fig. 4.3. Process of fabricating device in silicon layer of SOI wafer. (a) Device fabrication process and (b) cross-sectional image of fabricated device.

4.3.2 Experimental results

4.3.2.1 Analysis of base wafer surface before diamond deposition

The surface of the nanodiamond-coated base wafer was analyzed by XPS after baking, and the results are shown in Fig. 4.4. Figure 4.4 (a) shows the Si 2p spectra and Fig. 4.4 (b) shows the C 1s spectra. According to Fig. 4.4 (a), Si–O bonds were detected at binding energies of 101 eV (SiO_x) and 103 eV (SiO_2).[142] The Si–O bonds existed at the surface of the base substrate after baking. According to Fig. 4.4 (b), C–O bonds at a binding energy of 286.5 eV were detected and C=O bonds at a binding energy of 288 eV were detected.[142,143] C–O and C=O bonds also existed at the surface of the base substrate. However, C–Si bonds at a binding energy of 283 eV were not detected.[142] The carbon in the nanodiamonds did not directly bind to the silicon substrate.

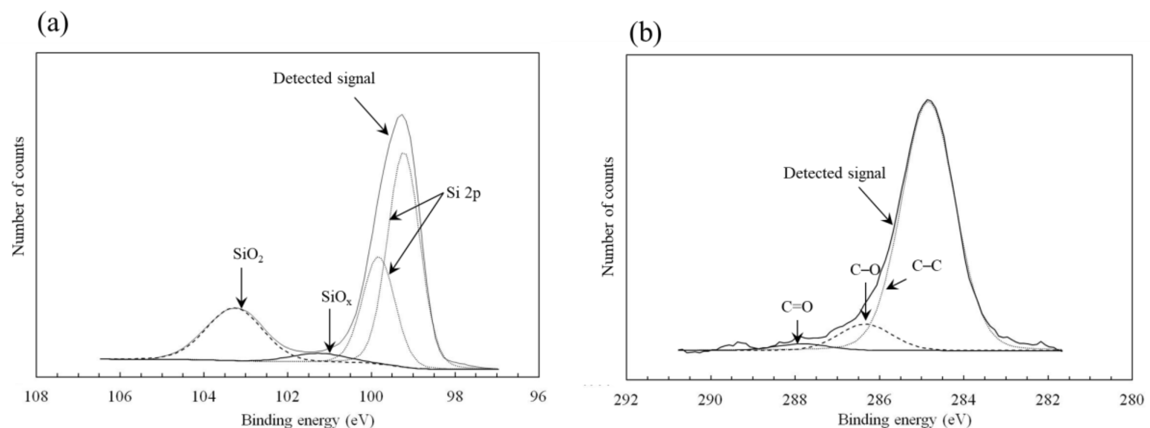


Fig. 4.4. Results of XPS analysis after baking nanodiamond-coated base wafer. (a) Si 2p and (b) C 1s spectra.

4.3.2.2 Observation and analysis of diamond layer deposited on base wafer

Figure 4.5 shows the OM observation results for the base wafer surface after depositing the diamond layer on the nanodiamond-coated base wafer. The thickness of the deposited diamond layer was 10 µm. Figure 4.5 (a) shows a photograph of the base wafer. Diamonds were deposited over the entire wafer. Figure 4.5 (b) shows the OM image. Diamond grains were densely deposited, and the diamond grain size was below 10 µm. These grains were smaller than those of the diamond layer deposited by scratching using diamond powder.[144]

Figure 4.6 shows the results of XRD analysis for the deposited diamond layer. (111), (220), and (311) diffraction peaks were detected.[145] Because the deposited diamond layer mainly consisted of (111) and (220) single crystals, the polycrystalline diamond could be deposited on the base wafer. In addition, Fig. 4.7 shows C1s photoemission spectra for the surface of the deposited diamond layer obtained by XPS analysis. The sp^3 peak at 285.4 eV was mainly detected.[146] Because native oxide was formed on the diamond layer, C–O bonding was also detected. Therefore, the polycrystalline diamond layer could be deposited on the base wafer following the flow shown in Fig. 4.2.

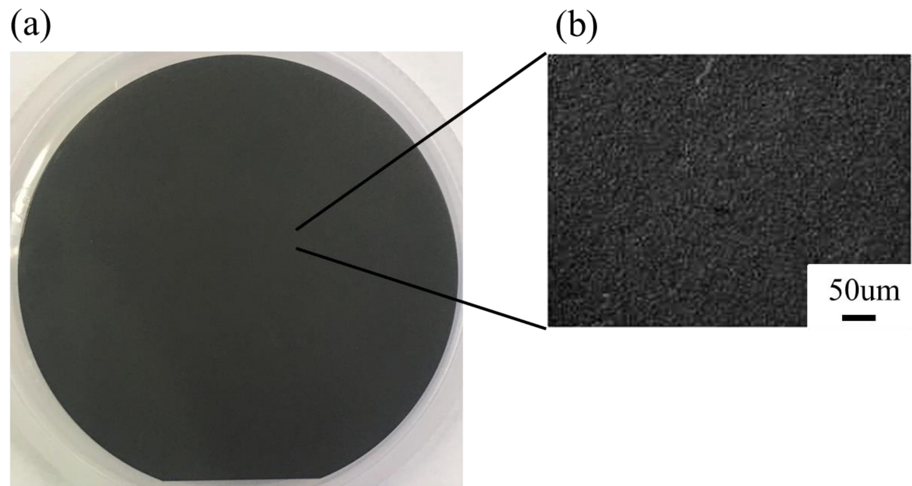


Fig. 4.5. Results of observing surface of 2-inch-diameter sample after depositing diamond on nanodiamond-coated base wafer. (a) Photograph of 2-inch-diameter wafer and (b) OM image.

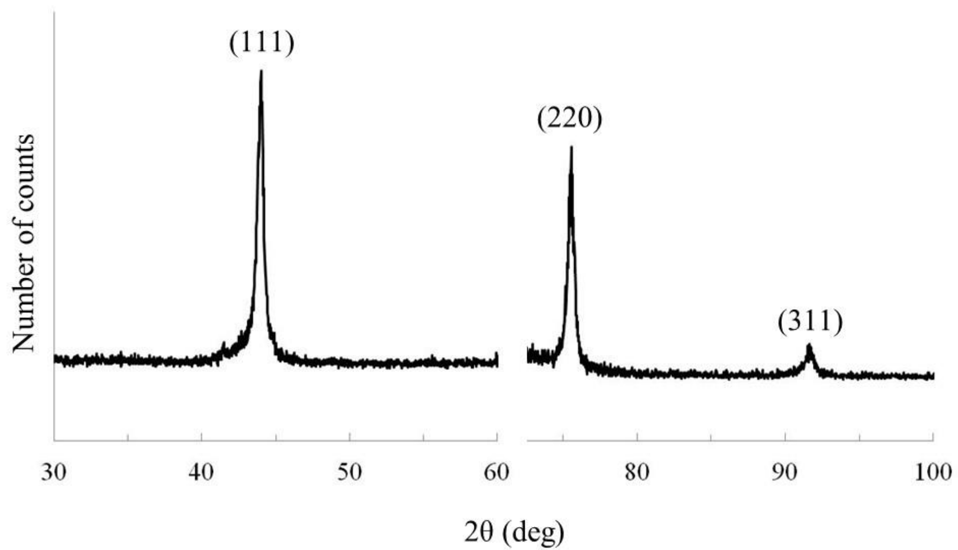


Fig. 4.6. Results of XRD analysis of diamond layer deposited on base wafer.

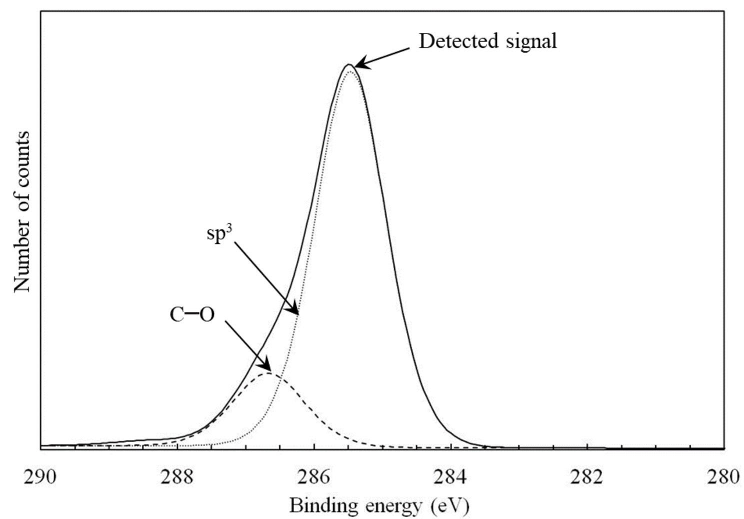


Fig. 4.7. C 1s spectra for diamond layer deposited on base wafer obtained by XPS analysis.

4.3.2.3 Evaluation of thermal conductivity of diamond-BOX layer

The thermal conductivity of a base wafer with a diamond-BOX layer was evaluated using a TCi thermal conductivity analyzer to transiently measure the resistivity at the surface of the sample after it was heated.[147,148] Two samples were evaluated: a diamond layer deposited on a silicon substrate as the studied sample and a SiO_2 layer deposited on a silicon substrate as a reference sample. The total thickness of the base wafers and the silicon substrate was 500 μm and the thickness of the BOX layer was 4 μm.

The thermal conductivity was determined to be 146 W/mK for the studied sample (the diamond layer on the silicon substrate), 85 W/mK for the reference sample (the SiO_2 layer on the silicon substrate), and 145 W/mK for the silicon substrate without any deposited layer. According to equation (4-2), the thermal conductivity of the deposited diamond layer was 2100 W/mK and that of the deposited SiO_2 layer was 1.6 W/mK, as shown in Fig. 4.8. When using equation (4-3), the thermal conductivity of the silicon and BOX layers removed the silicon substrate of the studied sample with the diamond layer was calculated to be almost one hundred times higher than that of the reference sample with the SiO_2 layer. Therefore, the studied sample has a high thermal conductivity.

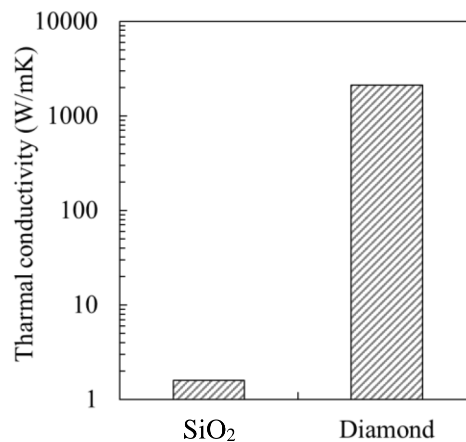


Fig. 4.8. Thermal conductivities of the two samples.

4.3.2.4 Evaluation of roughness of polished diamond layer on base wafer

After the diamond layer was polished by CMP until its thickness was reduced from 10 μm to 8 μm, the flatness of the polished surface was evaluated by the AFM method. The average roughness (Ra) was 2–3 nm over the area of 400 μm^2.

4.3.2.5 Evaluation and observation of voids formed during SAB of silicon wafer to diamond layer deposited on base wafer

Figure 4.9 shows an IR transmission image of the above-mentioned sample after bonding a silicon wafer to the polished diamond layer by SAB at room temperature under a pressure of 1 $\times 10^{-5}$ Pa. There were no voids in the wafer. Thus, the silicon wafer was successfully bonded to the diamond layer on the base wafer by SAB.

The bonded interface was also observed in cross-sectional OM and TEM micrographs of the chips obtained after dicing the bonded wafer at its center. Figures 4.10 shows the cross-sectional images obtained by (a) OM and (b) TEM observations. There were no voids over a wide area, as shown in Fig. 4.10 (a), and there were no microvoids in the bonding region, as shown in Fig. 4.10 (b). Therefore, a silicon wafer can be bonded to a diamond layer of a base wafer without voids.

In addition, amorphous layers of 5 nm thickness existed above and below the bonding interface. The amorphous layer above was formed by irradiating argon ions to the single-crystal silicon layer, and the amorphous layer below was formed by irradiating argon ions to the polycrystalline diamond layer during an activated treatment before bonding a silicon wafer to a base wafer with a polycrystalline diamond layer.

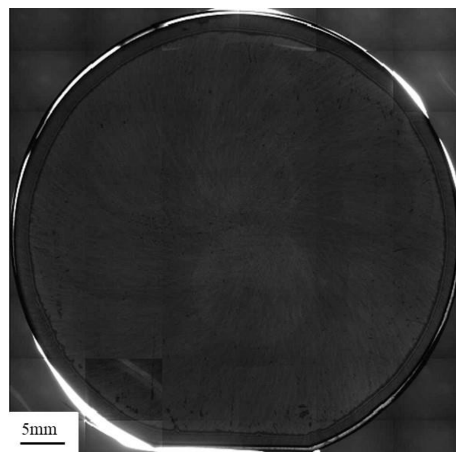


Fig. 4.9. IR transmission image of 2-inch-diameter wafer after bonding silicon wafer to diamond layer of base wafer.

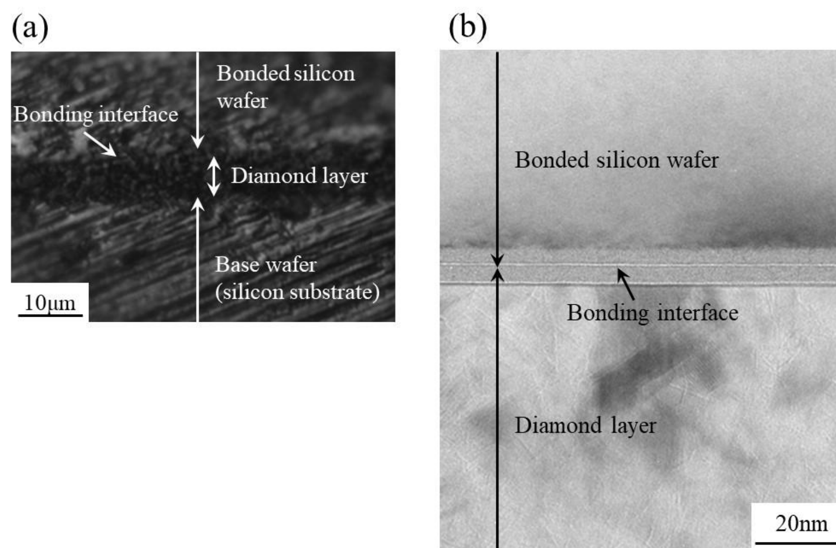


Fig. 4.10. Cross-sectional images of bonded silicon wafer on diamond layer of base wafer. Cross-sectional (a) OM and (b) TEM images.

4.3.2.6 Evaluation of depth profile of doped element in silicon layer on BOX layer

Because the devices were fabricated in a silicon layer on a BOX layer, the concentration of a doped element must have a constant depth profile in the silicon layer. Thus, the depth profile of the concentration of phosphorus in an n-type conductor was analyzed from the surface of the silicon layer to the bonding interface (the surface of the BOX layer) in the studied and reference (SOI wafer) samples by SIMS analysis.

Figure 4.11 shows the results of the SIMS analysis. The x-axis is the distance from the bonding interface, and the y-axis is the phosphorus concentration obtained from the SIMS analysis. For the studied sample [Fig. 4.11 (a)], the concentration of phosphorus was constant from the top surface of the silicon layer to the bonding interface. On the other hand, for the reference sample [Fig. 4.11 (b)], the concentration of phosphorus decreased from a depth of 0.2 μm to the bonding interface. Phosphorus diffused out from the silicon layer to the BOX layer during the bonding of the silicon wafer to the BOX layer at above 800 °C.

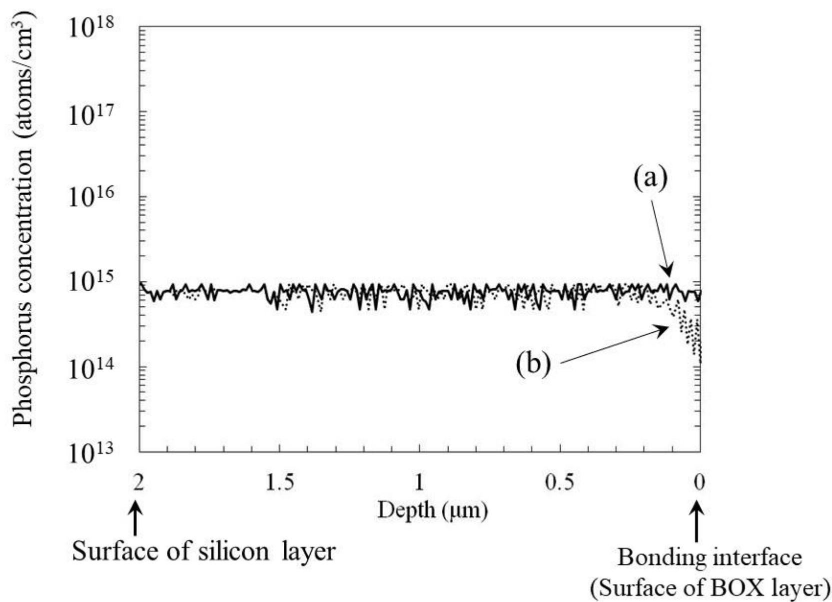


Fig. 4.11. Depth profiles of phosphorus concentration in silicon layer for studied and reference samples, obtained by SIMS analysis, after fabricating SOI wafer. (a) Studied and (b) reference samples.

4.3.2.7 Evaluation of depth profile of resistance in silicon layer on BOX layer

Because devices are fabricated in a silicon layer on a BOX layer, it is also important that the depth profile of the resistivity in the silicon layer is constant. The resistivity profiles of the studied and reference (SOI wafer) samples were investigated from the surface of the silicon layer to the bonding interface (the surface of the BOX layer) by SR measurement.

Figure 4.12 shows the results of the SR measurement. The x-axis is the distance from the bonding interface, and the y-axis is the resistivity obtained by SR measurement. For the studied sample [Fig. 4.12 (a)], the resistivity was constant from the top surface of the silicon layer to the bonding interface. On the other hand, for the reference sample (SOI wafer) [Fig. 4.12 (b)], the resistivity increased from a depth of 0.8 μm to the bonding interface between the silicon layer and the BOX layer. The resistivity at the interface was about 1×10^4 times that in the region of constant resistivity between the depths of 0.8 μm and 2.0 μm. This increasing resistivity cannot be explained by the concentration of the doped element, as shown in Fig. 4.12 (b), but can be explained by the positive fixed charges in thermal oxidation, as presented in Sect. 3.3.3.

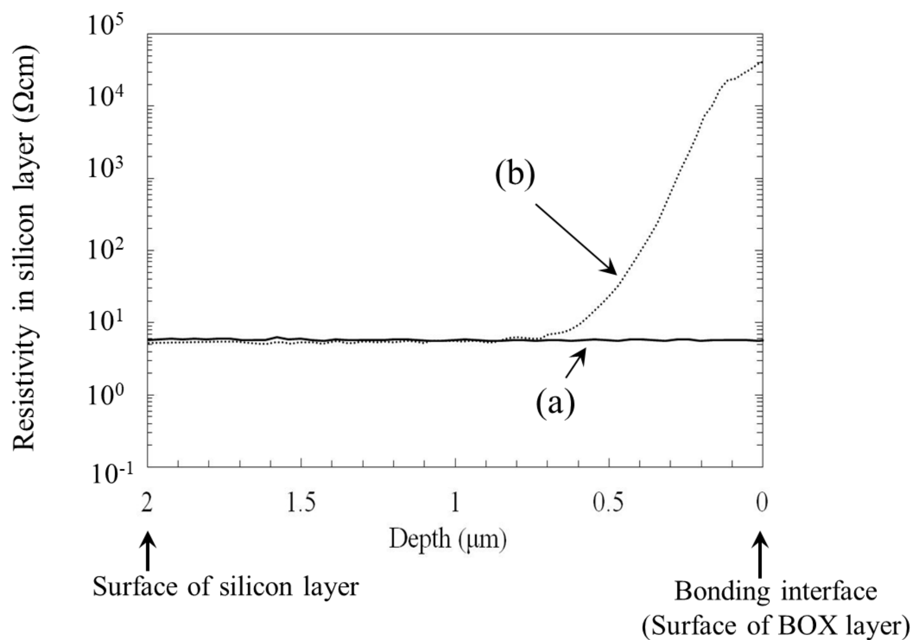


Fig. 4.12. Depth profiles of resistivity in silicon layer for (a) studied and (b) reference samples, obtained by SR measurement after fabricating SOI wafer.

4.3.2.8 Evaluation of breakdown electric field of diamond-BOX layer

Figure 4.13 shows a photograph of the studied sample after devices were fabricated on it by the processes shown in Fig. 4.3. Although the maximum temperature was 1000 °C, the silicon layer was not removed from the diamond layer during the device fabrication. Figure 4.14 shows a cross-sectional TEM image of the studied sample after devices were fabricated on it. Gaps were not generated at the bonding interface. In addition, amorphous layers at the bonding interface shown in Fig. 4.10 were not observed and recrystallized after fabricating the devices.

The breakdown electric field of the BOX layer of the studied sample and the reference SOI sample was measured by TZDB, which is a voltage-step-stress method. When a silicon substrate under the BOX layer is supplied with 0 V, the metal connected to the silicon layer has an additional input voltage of 0.1 V. Figure 4.15 shows the equivalent circuit schematic for the SOI wafer, where R_{Si} is the resistance of the silicon layer, R_{BOX} is that of the BOX layer, R_{Sub} is that of the base wafer, and R_{All} is that from the top surface to the back of the base wafer. Because R_{Si}, R_{BOX}, and R_{Sub} are connected serially,

$$R_{all} = R_{Si} + R_{BOX} + R_{Sub} . \qquad (4\text{-}4)$$

As V_{BOX} is the voltage applied to the BOX layer and V_{In} is the voltage input to the silicon layer, V_{BOX} can be calculated using Ohm's law,[149]

$$V_{BOX} = V_{In} * \frac{R_{BOX}}{R_{Si} + R_{BOX} + R_{Sub}} . \qquad (4\text{-}5)$$

R_{Si} and R_{Sub} can be calculated by multiplying the resistivity and thickness. For calculating R_{BOX}, it is necessary to measure the resistivity of the diamond layer. However, the contact resistivity between the probe of the measuring equipment and the diamond layer increases when using the four-terminal and SR methods. Thus, it is difficult to measure the resistivity of the diamond layer.

From equation (4-4),

$$R_{BOX} = R_{All} - (R_{Si} + R_{Sub}) . \qquad (4\text{-}6)$$

Figure 4.16 shows the breakdown voltage and electric field for the studied and reference samples obtained by TZDB measurement. The measured area of the silicon layer was 1 mm^2, as shown in Fig. 4.16 (b). R_{All} was calculated using the data of the I–V curve in Fig. 4.16 (a). When the current density exceeds 2×10^{-10} A/cm^2, R_{All} is defined by the following equation in terms of the input voltage V_{In} and current I:

$$R_{All} = \frac{V_{In}}{I} . \qquad (4\text{-}7)$$

Consequently, R_{All} is 4.6×10^{11} Ω, R_{Si} is 1.0×10^{-3} Ω, and R_{Sub} is 1.5 Ω.

When R_{BOX} is much larger than R_{Si} and R_{Sub}, R_{BOX} satisfies

$$R_{BOX} \fallingdotseq R_{All} \qquad (4\text{-}8)$$

from equation (4-4). V_{BOX} can be calculated from equations (4-4), (4-5), and (4-8) as

$$V_{BOX} \fallingdotseq V_{In} . \qquad (4\text{-}9)$$

In addition, the electric field was calculated by dividing V_{BOX} by the thickness of the BOX layer, the results of which are shown in Fig. 4.16 (b). The breakdown electric field was defined as the input voltage at which the leakage current reached 1×10^{-4} A/cm^2. The breakdown electric field of the studied sample was 1 MV/cm. Since the breakdown electric field of polycrystalline diamond is about 1 MV/cm,[150,151] this result is reasonable. On the other hand, the breakdown electric field of the reference sample was 8.0 MV/cm. Since the breakdown electric field of thermal oxide is generally 8–15 MV/cm,[110] this result is also reasonable. Since an electrical current flows at the grain boundaries in the polycrystalline diamond layer,[111] the breakdown electric field of the studied sample was lower than that of the reference sample.

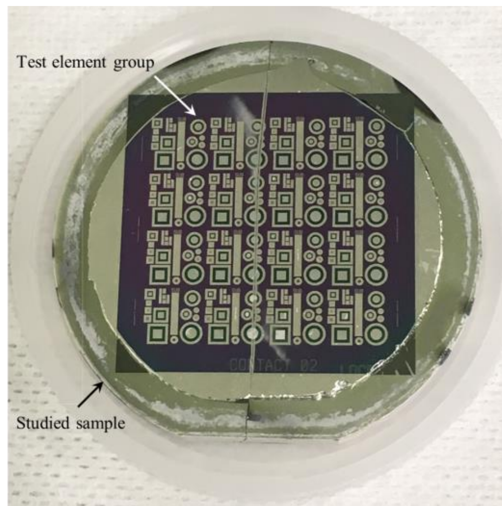


Fig. 4.13. Photograph of studied sample after fabricating devices.

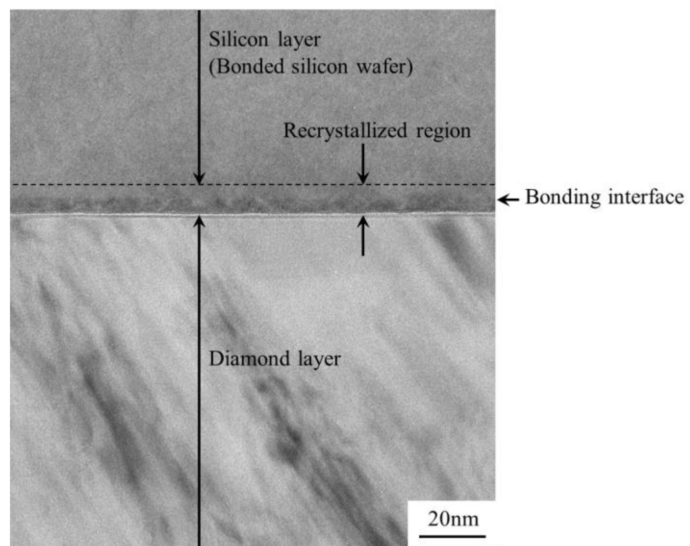


Fig. 4.14. Cross-sectional TEM image of bonding interface after fabricating devices on studied sample.

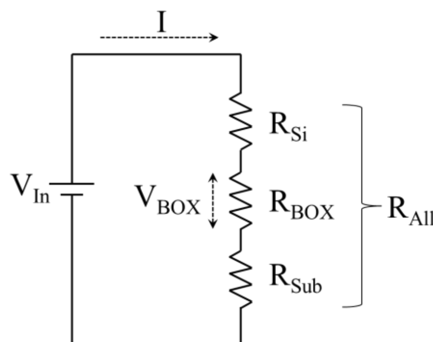


Fig. 4.15. Schematic of equivalent circuit for SOI wafer.

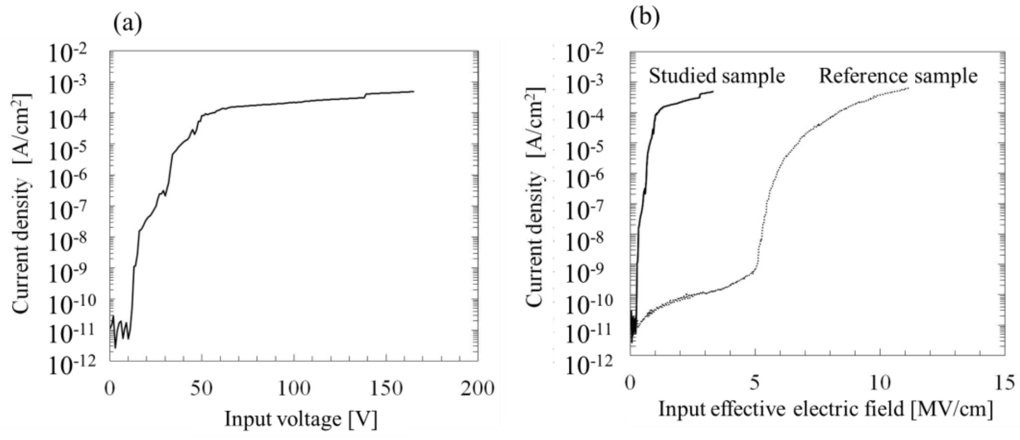


Fig. 4.16. TZDB measurement results for diamond-BOX layer. (a) Result for studied sample and (b) results for studied and reference samples.

4.3.3 Discussion

Diamond cannot be grown on a substrate of a different material without seeding elemental carbon. The seeding techniques generally involve scratching the substrate with diamond powder[138,152,153)] and implanting carbon ions into the substrate by BEN.[154)] In this work, these seeding techniques were not used to avoid damaging the surface of the base wafer. As an alternative, nanodiamond was spin-coated[155)] on the base wafer, followed by the baking of the spin-coated base wafer.

According to the XPS results for the base wafer surface after baking the spin-coated base wafer shown in Fig. 4.4, C–Si bonds do not exist on the base wafer and the elemental carbon in nanodiamond does not connect directly to the elemental silicon in the base wafer. Then, C–O and Si–O bonds were found to exist at the surface of the base wafer after baking the spin-coated base wafer. Thus, it was assumed that the elemental carbon at the surface of the base wafer bonded with the elemental silicon at the surface of the base wafer through the elemental oxygen, and this seeding mechanism of thermal-treatment-wafer bonding[156-160)] through the elemental oxygen after the vaporization of H_2O was proposed.

Figure 4.17 shows the mechanism of diamond seeding. In step (a), the nanodiamonds contained in water are spin-coated on a base wafer. Because water exists around each nanodiamond, the nanodiamond does not come into direct contact with the base wafer in this process. In step (b), the base wafer is baked at 80 °C. Only the water (H_2O) coating the nanodiamonds is vaporized, and the carbon in the nanodiamonds is weakly bonded to the oxygen in the native oxide layer. In step (c), polycrystalline diamond is deposited on the base wafer between 1000 °C and 1200 °C. In this process, the carbon is strongly bonded to the oxygen in the native oxide layer on the base wafer.

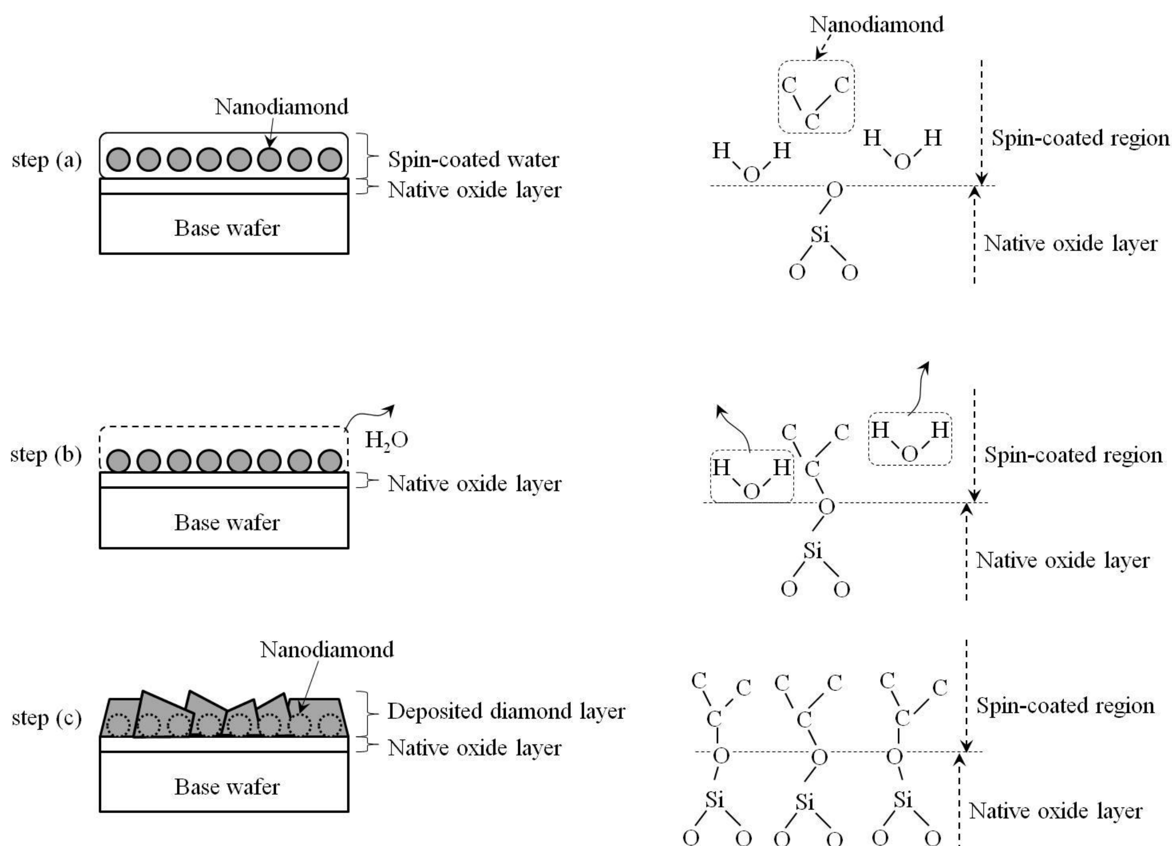


Fig. 4.17. Mechanism of diamond seeding on base wafer.

According to the results of the cross-sectional HR-TEM observation of the interface bonded by SAB, as shown in Fig. 4.10 (b), amorphous layers existed above and below the bonding interface. The thickness of these layers formed by argon ion irradiation during SAB was about 5 nm.[139,161–163] This argon ion irradiation generated dangling bonds at the surfaces of the polycrystalline diamond layer and bonding wafer at the same time. Figure 4.18 shows the mechanism of bonding between the polycrystalline diamond layer and the bonded wafer for the studied sample (diamond-BOX-SOI wafer). In step (a), the surfaces of the bonded wafer and polycrystalline diamond layer are sputtered by argon ion irradiation in an ultrahigh vacuum, and the dangling bonds stable in an ultrahigh vacuum are generated at these surfaces. Thus, in step (b), when these bonds come close to each other, the dangling bonds at the elemental silicon in the bonded wafer and the elemental carbon in the polycrystalline diamond layer become connected.

Liang et al. reported the bonding of a single-crystal silicon substrate to a single-crystal diamond substrate by SAB.[139] They showed, by electron energy loss spectroscopy (EELS), that the argon-ion-irradiated region of the single-crystal diamond substrate had σ- and π-connected ions. By XPS analysis, they showed that this region also had sp^3 and sp^2 bonds and no C–O bonds. The σ-connected ions and sp^3 bonds showed that single-crystal diamond was a cubic crystal system, and the π-connected ions and sp^2 bonds showed that graphite had dangling bonds. The lack of C–O bonds indicated the removal of the native oxide layer on the diamond layer. Thus, the argon ion irradiation removed the native oxide layer on the diamond layer, maintained single-crystal diamond, and formed dangling bonds on the diamond layer. These results clarified that the dangling bonds of the irradiated diamond substrate were connected to those of the irradiated silicon substrate.

The crystal condition and bonding states in the bonding region of the polycrystalline diamond layer were investigated by EELS and XPS. Figure 4.19 shows the results of the EELS analysis of the polycrystalline diamond layer and its bonding interface. Figure 4.19 (a) shows the analyzed points. As shown in Fig. 4.19 (b-1), a σ* peak at 292 eV for the polycrystalline diamond layer was detected, whereas a σ* peak at 292 eV was detected and a π* peak at 286 eV was detected near the bonding interface of the polycrystalline diamond layer, as shown in Fig. 4.19 (b-2).

To evaluate how the silicon layer bonded to the polycrystalline diamond layer, only the silicon layer on the polycrystalline diamond layer of the studied sample was removed by CMP and etching. Then, the top surface of the diamond layer after the SAB process was analyzed by XPS. Figure 4.20 shows the results of the XPS analysis. According to the spectra in Fig. 4.20 (a), sp^3 bonds were mainly detected, although sp^2 and C–Si bonds were also detected.[147,151] Figure 4.20 (b) shows the additional spectra obtained after depositing a diamond layer on the base wafer (before the SAB process, Fig. 4.7). The surface of the diamond layer does not have sp^2 or C–Si bonds but has sp^3 and C–O bonds.

These results are the same as those reported by Liang et al.[139] In this work, it was clarified that the native oxide layer on the diamond layer was removed and that the sp^2 structure was generated at the surface of the diamond layer by irradiating argon ions to the surface of the diamond layer. In addition, C–Si bonds were generated by connecting the activated elemental silicon in the silicon wafer to the activated elemental carbon in the diamond layer. Therefore, the mechanism shown in Fig. 4.18 is reasonable.

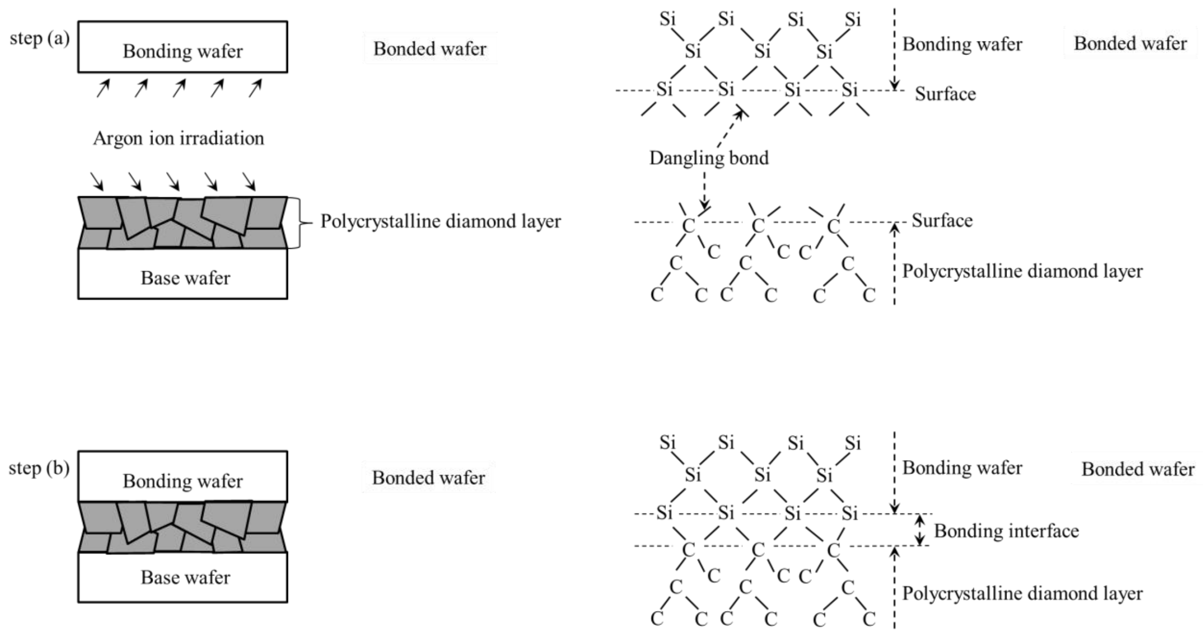


Fig. 4.18. Mechanism of SAB between polycrystalline diamond layer and bonding wafer.

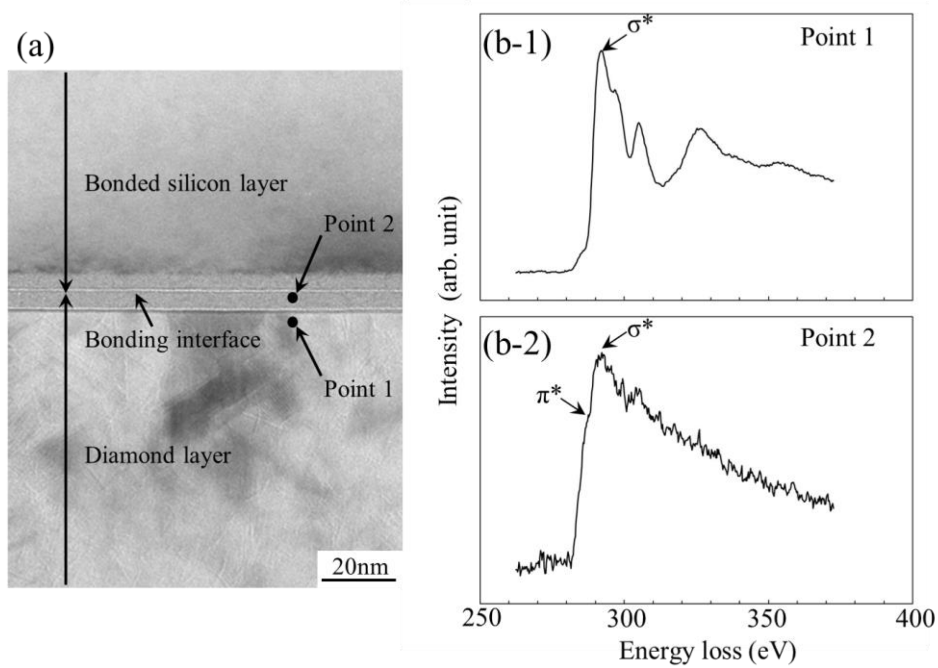


Fig. 4.19. Results of EELS analysis near bonding interface after fabricating SOI wafer.
(a) Analysis points, (b-1) result of EELS analysis for point 1, and (b-2) result of EELS analysis for point 2.

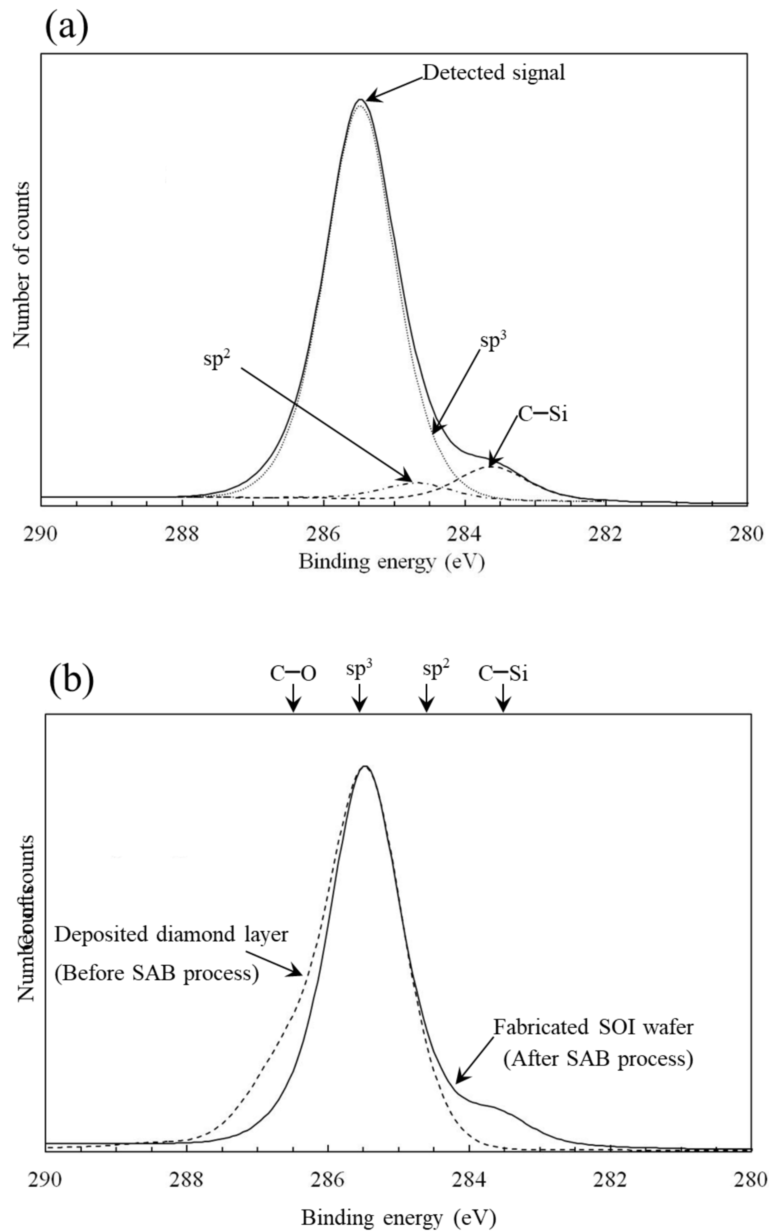


Fig. 4.20. C 1s spectra of surface of diamond layer after fabricating SOI wafer, obtained by XPS. (a) Result for fabricated SOI wafer and (b) results for deposited diamond layer (Fig. 6) and fabricated SOI wafer.

4.3.4 Summary

In this section, the fabrication of an SOI wafer with a polycrystalline diamond layer as a BOX layer was described. Diamond could be seeded on a base wafer by spin-coating nanodiamonds, and a dense diamond layer could be deposited on the seed nanodiamonds by MW-CVD. In addition, a silicon wafer was bonded to the diamond layer by SAB at room temperature without forming any voids. The thermal conductivities of the silicon and BOX layers removed the silicon substrate of the studied sample with the diamond layer were calculated to be almost one hundred times higher than that of the reference sample with the SiO_2 layer.

4.4 SOI wafer with silicon carbide layer

4.4.1 Experimental methods

Figure 4.21 shows the method of fabricating an SOI wafer with a SiC layer. Three silicon wafers were fabricated: a base wafer, a bonding wafer, and another wafer. The SiC layer was deposited on the base wafer by PE-CVD with flows of CH_4 and CH_3SiH_3 at 300 °C. After depositing the SiC layer on the base wafer, its top surface was polished by CMP.

The bonding wafer was then fixed to the base wafer with the polished SiC layer by SAB. Figure 4.22 illustrates this SAB process. It is generally necessary for the temperature to be above 1300°C to grow a single-crystal SiC layer.[140] Because a silicon wafer was used in my study and the temperature study was less than 1300°C, the deposited SiC layer is not a single crystal and has many stable dangling bonds, making it difficult to attach to a silicon layer and thus connect two substrates. Therefore, an ultrathin silicon layer as an adhesive layer was deposited on the SiC layer to bond the bonding wafer to the SiC layer on the base wafer. The ultrathin silicon layer deposition was carried out by irradiating another silicon wafer with argon ions and sputtering the silicon atoms of the other silicon wafer before bonding the bonding wafer to the SiC layer on the base wafer [step (2)]. Then, the bonding wafer was activated by irradiating argon ions and bonded to the SiC layer through this ultrathin silicon layer (step (3)).[113,164] After bonding the two wafers (the bonding wafer and the base wafer with the SiC layer), the bonding wafer was ground and polished from the back, which is opposite the wafer-bonding region, to the thickness of the active layer of the device. In addition, a reference SOI wafer was fabricated using SiO_2, instead of SiC, as an insulator layer deposited by PE-CVD.

Boron-doped (100) CZ 2-inch-diameter single-crystal silicon wafers were used in this study. The base wafer and the bonding wafer making up the silicon layer were each polished to a thickness of 500 μm. Their resistivity was 5 Ω·cm and their oxygen concentration was 1.2×10^{18} atoms/cm^3. A SiC insulator layer was deposited on the base wafers at 300°C by PE-CVD at flow rates of 130 sccm for CH_4 and 25 sccm for CH_3SiH_3 (Tsukishima Kikai Co., Ltd.). The thickness of this layer was varied from 140 nm to 6 μm depending on the results of evaluation; the thicknesses used to evaluate the thermal stability, thermal conductivity, and breakdown electric field of the insulator layer were 6 μm, 4 μm, and 140 nm, respectively. The top surface of this insulator layer was polished by CMP. Then, an ultrathin silicon layer as an adhesive layer was deposited on the insulator layer of this base wafer, and the base wafer was fixed to the bonding wafer by SAB in an ultrahigh vacuum of less than 1×10^{-5} Pa at room temperature (Nidec Machine Tool Corporation, MWB08-AX). The three silicon wafers (the bonding wafer, the base wafer with the SiC insulator layer, and another wafer for the deposition of the ultrathin silicon layer) were irradiated with argon ions at an energy of 1–2 keV for 5 min. After bonding the bonding wafer and the base wafer with the insulator layer, the back of the bonding wafer was ground and polished to a thickness of 20 μm. A reference sample was fabricated by the PE-CVD of SiO_2 as the insulator layer at 500°C and fixed by SAB at room temperature, as shown in Sect. 3.3.1.

As shown in Fig. 4.21, the SiC layer was deposited on the base wafer as the insulator layer. The surface of the base wafer with the SiC layer was then observed to evaluate its thermal stability after heat treatment (step (a)). The thermal conductivity of the SiC layer on the base wafer was continuously measured (step (b)). Next, voids and defects were searched for using IR and cross-sectional TEM observations after bonding the silicon layer to the SiC layer (steps (c) and (d)). Finally, after the bonding wafer was ground and polished as the active layer of devices, actual devices were fabricated on the silicon layer for TZDB measurement, and the breakdown electric field of the SiC layer was measured using these fabricated devices (step (e)).

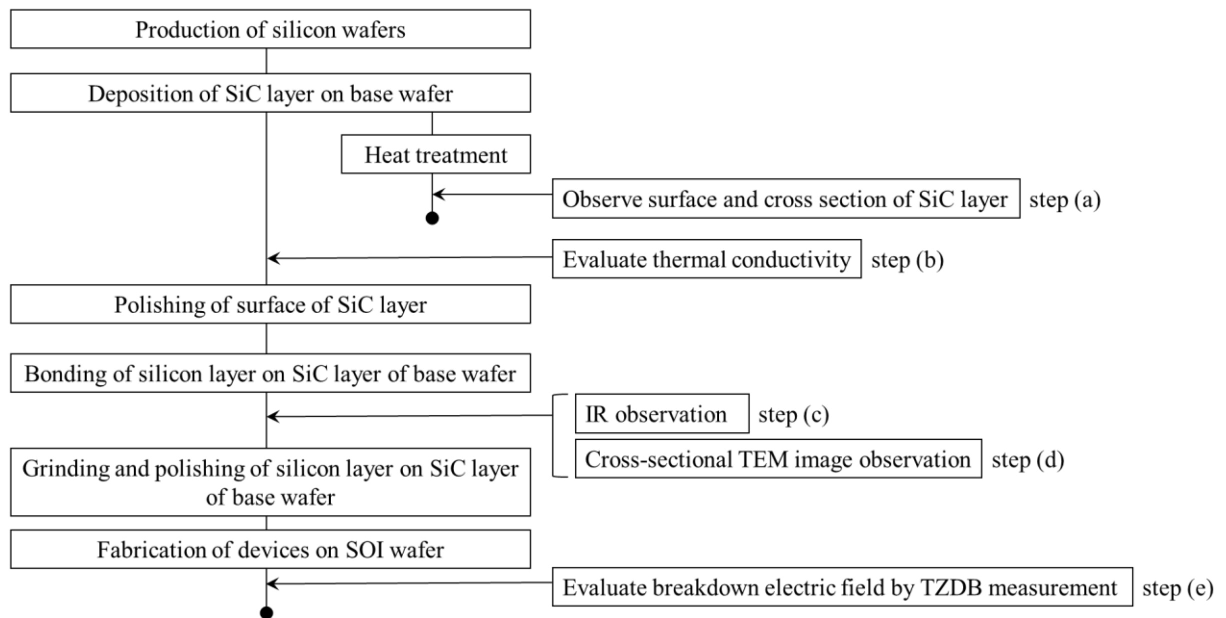


Fig. 4.21. Flow of experiment.

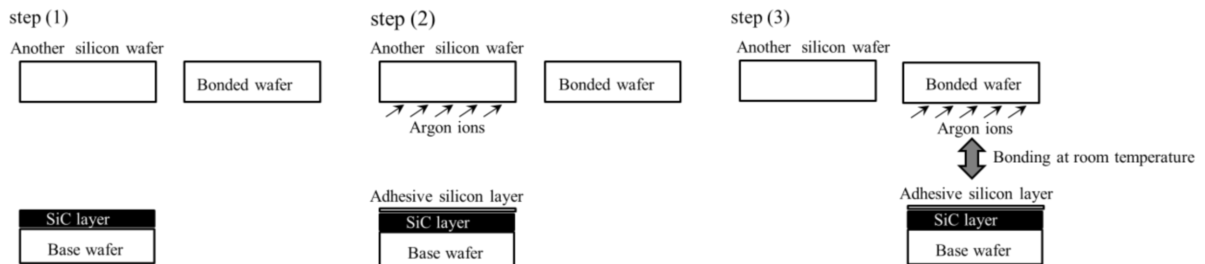


Fig. 4.22. Flow of fixing bonding layer on SiC layer by SAB.

4.4.2 Experimental results

4.4.2.1 Evaluation of thermal stability of deposited SiC layer on base wafer

The surface of the deposited SiC layer of 6 μm thickness on the base wafer after heat treatment at 1100°C for 4 h in nitrogen was observed. Figure 4.23 (a) shows a photograph of one-quarter of the wafer before heat treatment (after depositing the SiC layer on the base wafer). The SiC layer was deposited on the wafer from the center to 3 mm from the edge; the remaining area was where the sample holder of the deposition equipment held the silicon wafer, so the SiC layer was not deposited in this area. Figure 4.23 (b) shows a photograph of the wafer after heat treatment. The entire wafer was gray and similar to the base wafer before depositing the SiC layer. Therefore, the deposited SiC layer on the base wafer was removed during heat treatment, and this SiC layer had low thermal stability.

A sample with a SiC layer having thermal stability was next fabricated. A thin silicon nitride (SiN) layer was formed on the SiC layer as a capping layer by PE-CVD at flow rates of 25 sccm for CH_3SiH_3 and 120 sccm for N_2. The thickness of the SiN layer was 20 nm. Figure 4.24 (b) shows a cross-sectional OM image of this sample capped with the SiN layer after heat treatment at 1100°C for 4 h. This SiC layer remained after heat treatment. Therefore, this SiC layer had thermal stability by capping the SiN layer.

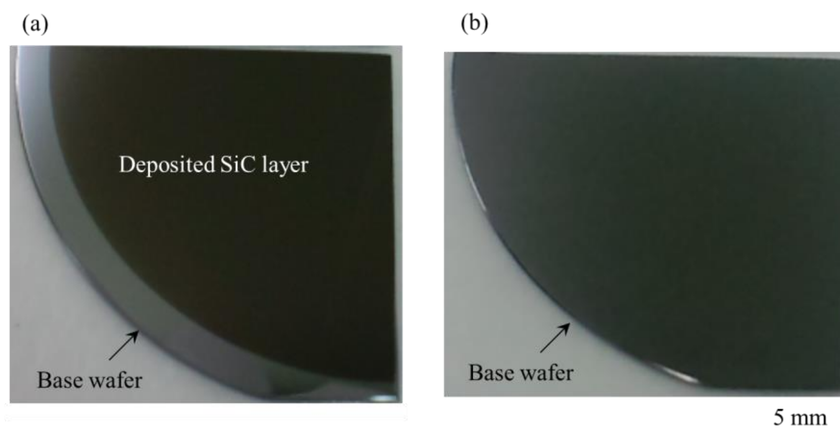


Fig. 4.23. Images of the surface of the SiC layer on a base wafer. (a) Before and (b) after heat treatment.

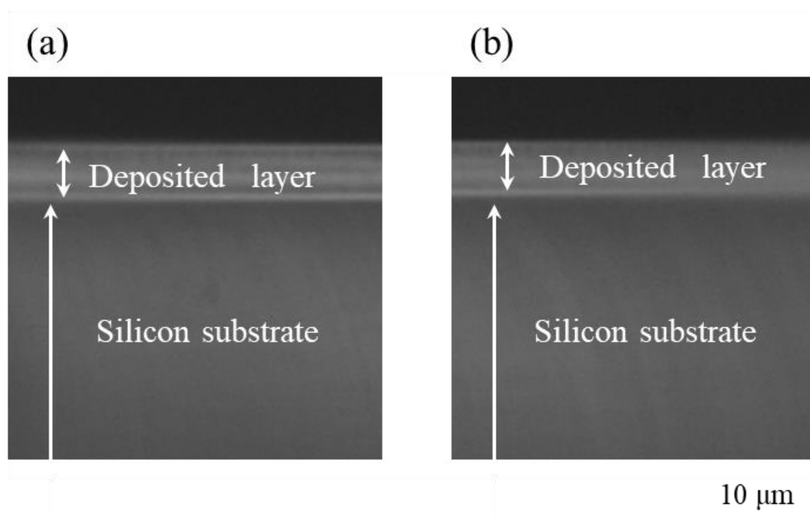


Fig. 4.24. Cross-sectional OM images. (a) Before and (b) after heat treatment.

4.4.2.2 Evaluation of thermal conductivity of SiC layer on base wafer

A base wafer with a SiC layer of 4 μm thickness and a capping SiN layer of 20 nm thickness was fabricated, and the thermal conductivity of this SiC layer with the capping SiN layer was measured using the TCi thermal conductivity analyzer to transiently measure the resistivity at the surface of the sample after heating.[147,148] The two samples were evaluated: the SiC layer with a capping SiN layer on a silicon substrate as the studied sample and a SiO_2 layer with a thickness of 4 μm deposited on a silicon substrate. Both the base wafer and the silicon substrate had a thickness of 500 μm.

The thermal conductivity was determined to be 119 W/mK for the studied sample (SiC layer on the silicon substrate), 85 W/mK for the reference sample (SiO_2 layer on the silicon substrate), and 145 W/mK for the silicon substrate without a deposited layer. According to equation (4-2), the thermal conductivity of the deposited SiC layer was 5.1 W/mK and that of the deposited SiO_2 layer was 1.6 W/mK, as shown in Fig. 4.25. According to equation (4-3), the thermal conductivities of the silicon and BOX layers removed from the silicon substrate of the studied sample with the SiC layer were calculated to be almost three times higher than that of the reference sample with the SiO_2 layer. Therefore, the studied sample has a high thermal conductivity.

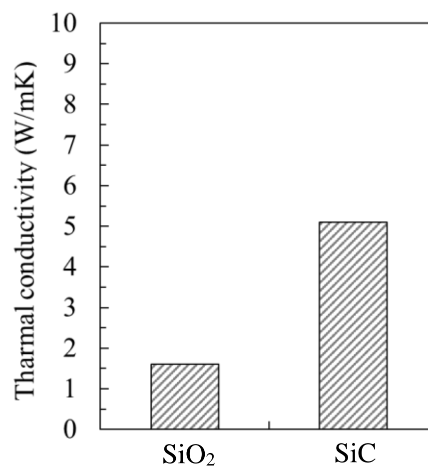


Fig. 4.25. Thermal conductivities of the two samples.

4.4.2.3 Evaluation and observation of voids formed when fixing silicon wafer to deposited layer of base wafer by SAB

Figure 4.26 shows an IR transmission image of the above-mentioned sample after the SAB of a silicon wafer to the polished SiC layer of 140 nm thickness with a capping SiN layer of 20 nm thickness at room temperature and a pressure of 1×10^{-5} Pa. There were no voids in the wafer except in three regions (shown by arrows in Fig. 4.26). These regions were generated by impurities on the SiC layer introduced during the polishing of the top surface of the SiC layer before fixing the silicon layer to the SiC layer.

The bonded interface was also observed on a cross-sectional TEM image of the chip obtained after dicing the bonded wafer at its center [Fig. 4.27 (a)]. The bonding surface was flat and there were no voids or defects at the bonding interface between the silicon and insulator (SiC with capping SiN) layers over a wide area. Figure 4.27 (b) shows a cross-sectional HR-TEM image of the same sample. There were no microcavities or punch-out dislocations at the bonding interface. An amorphous layer of 10 nm thickness was observed at the bonding interface. This amorphous layer was formed with two layers of 5 nm thickness, namely, the silicon wafer (layer) and the SiN insulator layer. As shown in the SAB process illustrated in Fig. 4.22, the argon-ion-sputtered silicon atoms at the surface of the silicon wafer (layer) and the sputtered silicon atoms were adsorbed on the top surface of the SiN layer on the SiC layer. Therefore, a silicon wafer (layer) could be fixed to a SiC layer with a capping SiN layer of a base wafer without voids or punch-out dislocations by depositing an amorphous adhesive layer containing silicon before bonding.

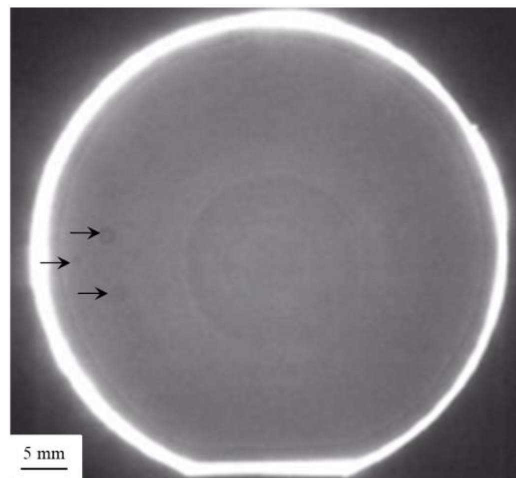


Fig. 4.26. IR transmission image of 2-inch-diameter wafer after bonding silicon wafer on the SiC layer of base wafer.

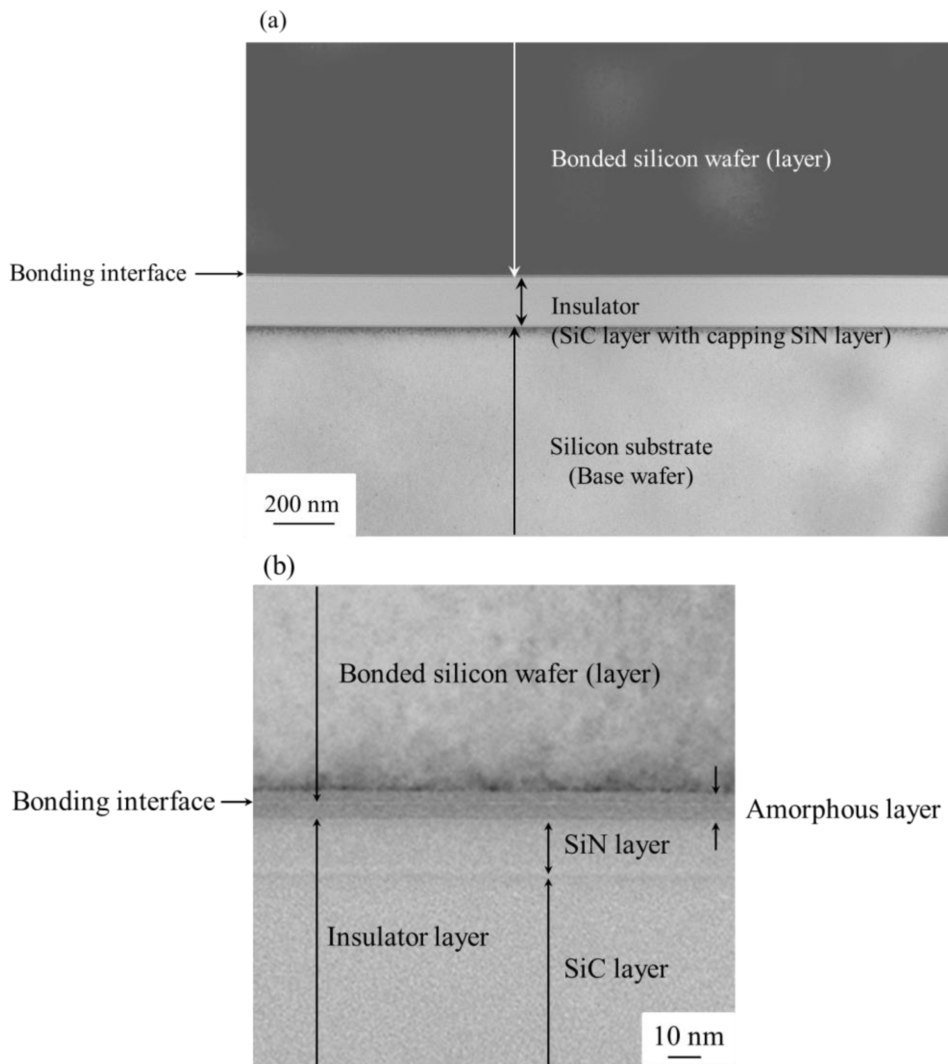


Fig. 4.27. Cross-sectional TEM images after bonding silicon layer on the SiC layer of base wafer. (a) TEM and (b) HR-TEM images.

4.4.2.4 Evaluation of breakdown electric field of SiC layer into SOI wafer

Figure 4.28 shows the breakdown electric fields for the studied sample (insulator layer: SiC) and reference sample (insulator layer: SiO_2) obtained by TZDB measurement. When the leakage current through the BOX layer from the silicon layer on the BOX layer to the silicon substrate under the BOX layer was larger than 1×10^{-4} A/cm^2, the intrinsic breakdown electric field as the C mode was defined. The breakdown electric field of the reference sample was 10.2 MV/cm, as illustrated by the dotted line (a) in Fig. 4.28. The breakdown electric field of the studied sample was 10.8 MV/cm, as shown by the solid line (b) in Fig. 4.28. This value was the same as that of SiO_2. Therefore, the studied SiC layer had the characteristic of an insulator with sufficient thermal conductivity for an SOI wafer.

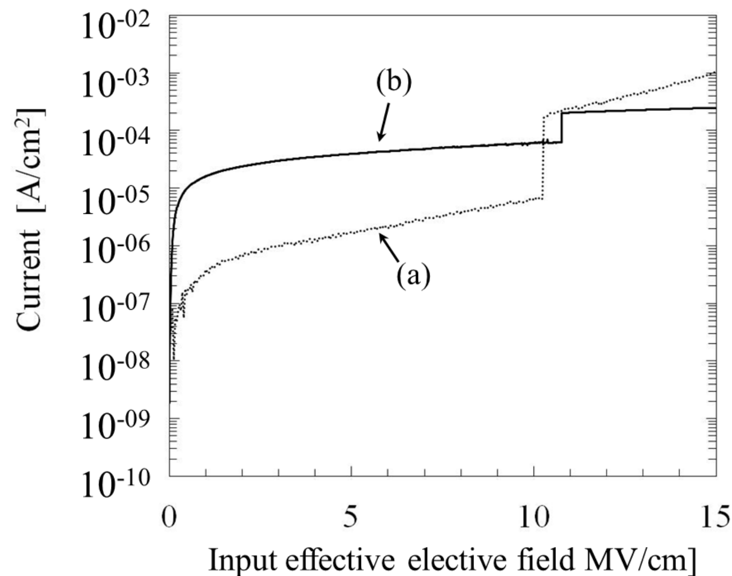


Fig. 4.28. TZDB measurement results for insulator layer. (a) Reference (SiO_2 layer) and (b) studied (SiC layer) samples.

4.4.3 Discussion

With the exception of the intrinsic leakage current of the insulator layer, leakage currents into the isolator layer are mainly generated in three modes,[110,111,165–168] as shown in Fig. 4.29. In the first mode [Fig. 4.29 (a)], when metallic impurities are contaminated into an isolator layer, since they act as low-resistivity spots in the insulator layer, an electric current flows in the contaminated region.[165,166] In the second mode (Fig. 4.29 (b)), when the top surface of the insulator layer is roughened since a strong electric field is generated in the concave regions in the roughened isolator layer, an electric current flows into the hollow regions.[167] In the third mode (Fig. 4.29 (c)), when cavities and grain boundaries exist in the insulator layer since a local electric charge is generated at the cavities and grain boundaries, an electric current flows near them.[168]

In general, a SiC layer is formed as a single crystal above 1300°C.[169–171] Because the SiC layer was deposited at 300°C in this study, it was not a single-crystal layer but a polycrystalline or amorphous layer. Because there were no grain boundaries in the SiC layer, as shown in Fig. 4.27 (b), the deposited SiC layer was not polycrystalline but amorphous.

When the insulator layer is polycrystalline, the leakage current in the insulator layer is lower than that in a single-crystal layer. Figure 4.30 shows a schematic of the leakage current paths in the polycrystalline layer. Dangling bonds are formed at grain boundaries between single crystals. Since a dangling bond has unpaired electrons and is negatively charged, an electric current is generated at the dangling bonds. Thus, in terms of the insulation characteristic, a polycrystalline insulator with dangling bonds is electrically leakier than a single-crystal insulator without dangling bonds.

In Sect. 4.3.2.8, I discussed the breakdown electric field of a polycrystalline diamond layer as a wide-band-gap semiconductor material. This breakdown electric field was 1 MV/cm, which is much lower than that of a single-crystal diamond layer.[131,137] The breakdown electric field of a single-crystal SiC layer is generally 2–3 MV/cm.[137] When the studied SiC layer were polycrystalline, the breakdown electric field would be lower than 2 MV/cm, which, however, was not the case. As mentioned above, the SiC layer does not have any grain boundaries, as shown in Fig. 4.27 (b). Therefore, the studied SiC layer was made of not polycrystalline but amorphous.

On the other hand, the leakage currents of the two samples (reference and studied) were above 1×10^{-7} A/cm^2 at 0–10 MV/cm, as illustrated in Fig. 4.28. Metallic impurities were contaminated into the insulator layer from the deposition equipment during depositing the layer on the base wafer. The leakage current of the studied sample (insulator layer: SiC) was greater than that of the reference sample (insulator layer: SiO_2), as shown in Fig. 4.28. Because the PE-CVD equipment differed for the SiC and SiO_2 layers, the concentration of metallic impurities in these layers might differ and the SiC layer might have a higher concentration of contaminated metallic impurities than the SiO_2 layer.

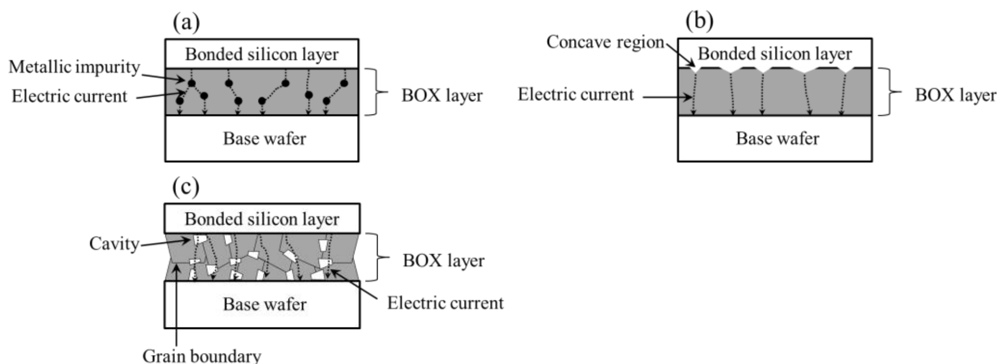


Fig. 4.29. Leakage current modes for insulator, excepting intrinsic leakage current.
(a) Metallic impurities contaminating an insulator layer, (b) roughening of an insulator surface, and (c) cavities and grain boundaries in an insulator layer.

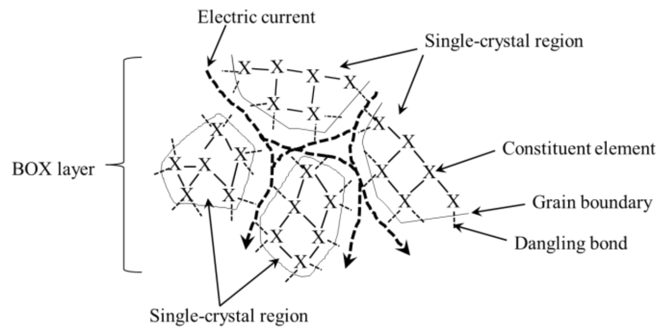


Fig. 4.30. Leakage current paths in the polycrystalline insulator layer.

4.4.4 Summary

In this section, I proposed a fabrication process for an SOI wafer with a SiC layer as a BOX layer with a higher thermal conductivity than the SiO_2 layer. The amorphous SiC layer was formed by PE-CVD at 300°C, and a silicon layer was bonded to the deposited SiC layer with the capping SiN layer by SAB with no voids or punch-out dislocations at the bonding interface after bonding a silicon layer to the deposited SiC layer as an insulator layer. The thermal conductivities of the silicon and BOX layers removed from the silicon substrate of the studied sample with the SiC layer were calculated to be almost three times higher than that of the reference sample with the SiO_2 layer. The breakdown electric field of this layer was 10–11 MV/cm, the same as that of a SiO_2 layer.

4.5 Conclusions

In this chapter, the purpose of the work described was to develop a method of fabricating an SOI wafer with a BOX layer, both of which have a high breakdown electric field and a high thermal conductivity. The SOI wafer with a BOX layer made of polycrystalline diamond or amorphous SiC that had a high thermal conductivity was fabricated for the first time. The results are summarized as follows:

1. For a BOX layer made of polycrystalline diamond, the diamond layer is deposited on a base wafer by spin-coating nanodiamonds and MW-CVD. Then, a silicon wafer could be bonded to the diamond layer by SAB without forming any voids, and the SOI wafer with a polycrystalline diamond layer could be fabricated. The thermal conductivity was one hundred times higher than that of the SiO_2 layer.

2. For a BOX layer made of amorphous SiC, the SiC layer is formed by PE-CVD at 300°C, and a silicon layer was bonded to the deposited SiC layer with a capping SiN insulator layer by SAB without the formation of voids or punch-out dislocations at the bonding interface. The thermal conductivity was three times higher than that of the SiO_2 layer. The breakdown electric field of this layer was 10–11 MV/cm, the same as that of a SiO_2 layer.

3. The SOI wafer with a polycrystalline diamond layer is suitable for devices that require reduced self-heating, and the SOI wafer with an amorphous SiC layer is suitable for devices that require a high breakdown electric field.

5. Conclusions

In this thesis, silicon wafers with different functional layers embedded by direct bonding for the fabrication of sensors (CMOS imaging sensors and MEMS) and power devices are described. The wafer bonding process was SAB, whereby a silicon wafer can be bonded to another wafer at room temperature in an ultrahigh vacuum. Table 5-I shows the list of studied wafers.

In Chapter 2, two types of bonded silicon wafer with proximity gettering were demonstrated for fabricating imaging sensors. One type was an epitaxial wafer bonded to a molecular-ion-implanted wafer for high-sensitivity CMOS imaging sensors of security cameras. The other type was an FZ wafer bonded to a CZ wafer at room temperature for LiDAR system IR-detecting sensors that use an APD device. The concentration of oxygen in the bonding layer (an epitaxial layer or an FZ wafer), which is the region where devices are formed, decreased to below 1×10^{17} atoms/cm^3, which was one-tenth that of current epitaxial wafers. In addition, the bonding region between the bonding wafer and the silicon substrate has a gettering capability of more than 2×10^{13} atoms/cm^2 for contaminated metallic impurities such as nickel, copper, and iron. The leakage current of the pn-junction diode, which is the dark current of the studied wafer, decreased to one-thousandth that of the reference wafer.

In Chapter 3, three types of SOI wafer were demonstrated for fabricating power and MEMS devices. These wafers could be fabricated for less than one-tenth that of the reference method (thermal oxidation and thermal bonding). One type was deposited on a BOX layer of 10 μm thickness by PE-CVD at a high temperature of 500°C. This wafer had no fixed charge in the BOX layer, which existed in a thermal oxide film. The second type had a BOX layer formed by PE-CVD at a low temperature of 300°C and made dense by annealing at a temperature above 300°C in an oxygen atmosphere. The accidental B-mode breakdown electric field of the BOX layer can be improved by annealing the deposited BOX layer at temperatures higher than 300°C. The third type had a BOX layer made of SiO_x ($x < 2$) deposited by PE-CVD at 500°C to decrease the membrane stress around the BOX layer. When x was less than 1.2, the membrane stress was decreased by more than 10% compared with that of the reference sample (x: 2).

In Chapter 4, SOI wafers with a high-thermal-conductivity BOX layer were demonstrated. The wafers had a BOX layer made of polycrystalline diamond or amorphous SiC, so that devices on the BOX layer do not self-heat during operation. The SOI wafers could be fabricated with a BOX layer comprised of an insulator and a thermal-conductivity layer made of polycrystalline diamond or an amorphous SiC layer. The thermal conductivity of polycrystalline diamond was one hundred times higher than that of the SiO_2 layer. The breakdown electric field of the amorphous SiC layer was 10–11 MV/cm, the same as that of a SiO_2 layer.

All these wafers could be fabricated without voids or thermal stress by SAB in a short time. From the work described in this thesis, the feasibility studies of the suggested wafers could be mostly completed, and the suggested wafers could resolve the issues plaguing current wafers. As the next step, their wafers must have the test of devices more than 100°C for long-term reliability. In the future, it will be most important and necessary to put the studied wafers to practical use.

Table 5-I. List of wafers studied in this thesis.

Target device	Studied wafer	Base wafer	Intermediate layer	Bonding wafer	Advantage	Section	Chapter
CMOS imaging sensor	Silicon epitaxial layer bonded to silicon wafer with molecular-ion-implanted layer	Molecular-ion implanted CZ wafer	Molecular ion-implanted layer	Epitaxial wafer	(1) Low concentration of oxygen in device fabrication region (2) Proximity and high gettering	2.3	2
	Floating-zone silicon wafer bonded to Czochralski silicon substrate	CZ wafer	NA	FZ wafer	(1) Thick device region (2) Low concentration of oxygen in device fabrication region (3) Proximity and high gettering	2.4	
Power device and MEMS	SOI wafer with extra-thick SiO_2 BOX layer	CZ wafer	Deposited SiO_2 layer	CZ wafer	(1) Thick BOX layer (2) No fixed charge in BOX layer	3.3	3
	SOI wafer with deposited and annealed SiO_2 BOX layer	CZ wafer	Deposited and annealed SiO_2 layer	CZ wafer	(1) Thick BOX layer (2) B-mode improvement for BOX layer	3.4	
	SOI wafer with SiOx BOX layer	CZ wafer	Deposited SiO_x layer	CZ wafer	Reduced membrane stress around BOX layer	3.5	
Power and radio frequency devices	SOI wafer with diamond layer	CZ wafer	Polycrystalline diamond layer doped boron	CZ wafer	High thermal conductivity of BOX layer	4.3	4
	SOI wafer with silicon carbide layer	CZ wafer	Amorphous SiC layer	CZ wafer	High thermal conductivity of BOX layer	4.4	

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