Study of Integration Technology with 3D-stacked Heterogeneous Dielets for Flexible Hybrid Devices

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Abstract

This thesis focuses on integration technology research and development for a healthcare monitoring and vain viewer device called Smart Skin Display as a Flexible Hybrid Electronics (FHE) that combines the performance of rigid single crystalline semiconductors with flexible organic substrates. So far, structurally new FHE is proposed with embedded heterogeneous chips using fan-out wafer-level packaging (FOWLP). Conventional flexible devices are limited to so-called flexible printed circuits (FPC), where only limited parts without any components surface-mounted on polyimide substrates are flexible. In contrast, highly flexible devices have been developed using organic semiconductors. However, the performance of the organic semiconductors is low compared to Si and III-VI semiconductors. On the other hand, ultrathin Si dies themselves used in conventional FHE are flexible. In previous studies, the ultrathin dies thinned to less than several tens of micrometers are surface-mounted on polymeric substrates and interconnected with printable wirings. However, the conventional FHE has a severe problem caused by mechanical stress to give characteristics fluctuation when bending. The FHE used in this research consists of several tiny chips called “dielet” and embeds them in an extremely flexible elastomer substrate PDMS at the wafer-level. Recently, “chiplet” has been attracting attention in the semiconductor field. A chiplet is a tiny chip designed to separate several functions previously combined into a monolithic system on a chip (SoC). The advantage of chiplet is that each chiplet can be manufactured using the appropriate technology nodes at a low cost. The concept of the dielets in this study encompasses a broader spectrum of initially tiny devices such as optical devices, MEMS, and passive devices, in addition to the chiplets mentioned above. Smart Skin Display, as a highly integrated FHE device, consists of mini-LEDs, micro-LEDs, and 3D-ICs with photodiodes and LED drivers. The micro-LEDs are stacked on the 3D-ICs having TSV (through-silicon via). The mini-LEDs emit red and IR light to human skin, and the 3D-ICs receive the reflected light from the blood vessel and drive the micro-LEDs used as micro-LED display components. This highly integrated wearable flexible hybrid device can diagnose conditions like arteriosclerosis obliterans more easily since it can simultaneously visualize blood vessels and acquire biological information. This thesis mainly describes five key integration technologies to fabricate Smart Skin Display. The first one is high-precision tiny dielet assembly. The second one is highly bendable multi-level wiring formation on an elastomer PDMS, the third one is room-temperature micro-LED bonding on a wafer, the fourth one is TSV barrier and seed layer deposition using standard PVD tool, and the last one is micro-LED stacking on thin 3D-ICs. I will develop these key technologies required to implement Smart Skin Display in each chapter.

Process integration and flexible redistributed multi-wiring layer design/formation of Smart Skin Display are the main topics of Chapter 2. In the highly integrated Smart Skin Display, heterogeneous dielets are temporarily fixed on a thermal rerelease tape attached to a support substrate, followed by filling and molding with a biocompatible and flexible PDMS. A critical issue for tiny dielet positioning within ±10 μm in the integration process integration is die shift, which refers to the movement of the dielet caused by the fluidic force of the resin

and thermomechanical stress. In this study, an anchor layer is proposed as a method to suppress die shift regardless of the size of the dielets. By introducing the anchor layer, suppressing the die shift of mini-LEDs with a side length of 300 μm down to several micrometer ranges is succeeded. To construct the mechanically robust Smart Skin Display, I then focus on the fabrication of flexible redistributed two-layer interconnects on an elastomer PDMS. The flexible multilayer wiring is structurally designed based on a stress neutral axis concept. When Smart Skin Display is bent, more significant stress is applied at the outermost wiring layer from the stress neutral axis. The stress neutral axis is, therefore, to be located in the middle of the two-layer wires in this study by designing the thickness and Young's moduli of the materials. Since conventional polyimide flexible substrates have high Young's moduli around 3-4 GPa, such a stress-neutral axis control is challenging, and low-Young's-modulus PDMS can achieve the structural design. I accomplish the flexible wiring formation with a width of 50 μm or smaller required for Smart Skin Display. Furthermore, the mechanical durability of the flexible multilayer wiring is evaluated by bending tests. The flexible multilayer wiring can survive the severe conditions of a 1-mm radius of curvature during the bending test. This result suggests that the flexible multilayer wiring can be endured by mechanical stress when folding Smart Skin Display.

Low-thermomechanical-stress bonding and interconnect technologies for heterogeneous dielets on the wafer are discussed in Chapter 3. Conventional bonding used for 3D integration requires thermocompression bonding. However, the 3D-IC would be damaged when a high-temperature point load is applied, making it difficult to attach micro dielets to the 3D-IC. As a result, I create room-temperature electroplated Cu direct bonding and show that it could be done using sapphire wafers as a host substrate. Micro-LEDs, which are expected to be used in next-generation displays, are used as tiny dielets and successfully bonded. For Smart Skin Display, an electroluminescence yield of about 100% is required. A failure analysis is underwent to enhance the yield of electroplated Cu direct bonding. Finally, the prospect of achieving 100% luminescence yield is obtained. This bonding method can vertically stack and electrically interconnect dielets that are not suitable for thermocompression bonding in one batch. Furthermore, it is a fantastic bonding method that can attach multiple heterogeneous components at once.

The processability of dielet-on-wafer 3D integration based on Via-last TSV formation is described in Chapter 4. The TSV barrier and seed layer sputtering is an important process that determines the success or failure of 3D-IC fabrication. In industry, a specialized sputtering apparatus such as ionized sputtering and long-throw sputtering is used for the deposition of TSV barrier/seed layers; however, their usefulness is constrained for TSV with large aspect ratios. In this investigation, I optimize the process utilizing standard sputtering by controlling rotation, tilting, and positioning conditions between target metals and wafer samples and challenge the maximum aspect ratio that can be fabricated. The results of this research are significant in that they expand the range of 3D-IC that can be fabricated using standard sputtering equipment. Based on this outcome, I design the TSV geometry and fabricate 3D-IC at the die-level. Micro-LEDs are successfully bonded onto the thinned 3D-IC by room-temperature electroplated Cu direct bonding without any cracks. Therefore, micro-LEDs are successfully operated. The 3D-IC dielets can be integrated by the highly integrated FHE techniques, which significantly enhance the performance of flexible devices. The FHE in this research gives a breakthrough against the constraints of traditional flexible devices and can greatly contribute to the development of the mechanical and electrical systems engineering and biomedical engineering fields.

Finally, Smart Skin Display integration technologies described in Chapters 2–4 are summarized in Chapter 5.

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Chapter 1
Introduction

1.1 Background

Over the years since the invention of the transistor, a large-scale integrated circuit (LSI) has continued to get smaller, according to Moore's Law [1]. Today, 3nm processes are in production [2]-[4], while 2 nm [5][6] and 16Å processes are also developing. Process node shrinking leads to improved LSI performance and lower power consumption. However, Moore's law has decreased since 2000, and the gap between Moore's law projection and actual chip performance has grown 15-fold by 2008. Spurring this slowdown is the declining cost-effectiveness associated with the shrinking of LSI manufacturing processes. The post-Moore era is anticipated to begin in the future [7], and a strategy is being taken to boost performance that combines miniaturization and functionalization, as shown in Fig. 1-1.

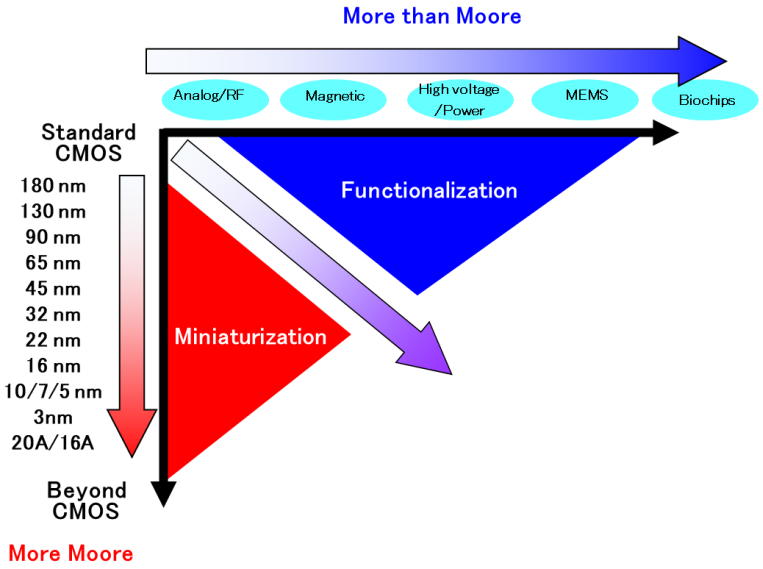


Fig. 1-1 LSI performance improvement approach.

1.2 Heterogeneous integration

Monolithic stacking of III-V device layers on Si or GaAs wafers for optoelectronic applications has kicked off investigations on heterogeneous integration [8]. At that time, multichip modules were the term used [9][10]. Until the late 1990s, conventional heterogeneous integration had been restricted to the fabrication of heterojunctions, such as., GaAs/GaAlAs, and heterostructures with multi-wavelength LEDs. Over the past two decades, flip-chip bonding technology for even small chips has been employed extensively in industry, and heterogeneous integration research has been extended to include additional areas, such as microelectromechanical systems (MEMS) [11] and sensors [12]. Meanwhile, heterogeneous integration works have been moving beyond 2D structures to 3D [1].

At first, fully 3D-integrated IC (3D-IC) attracted attention as a high-performance and multipurpose heterogeneous integration [2]-[6]. 3D-ICs require chips thinner than a few tens of m, because of their limited mechanical strength they are prone to warpage and residual stress problems and Joule heat [7]-[9].

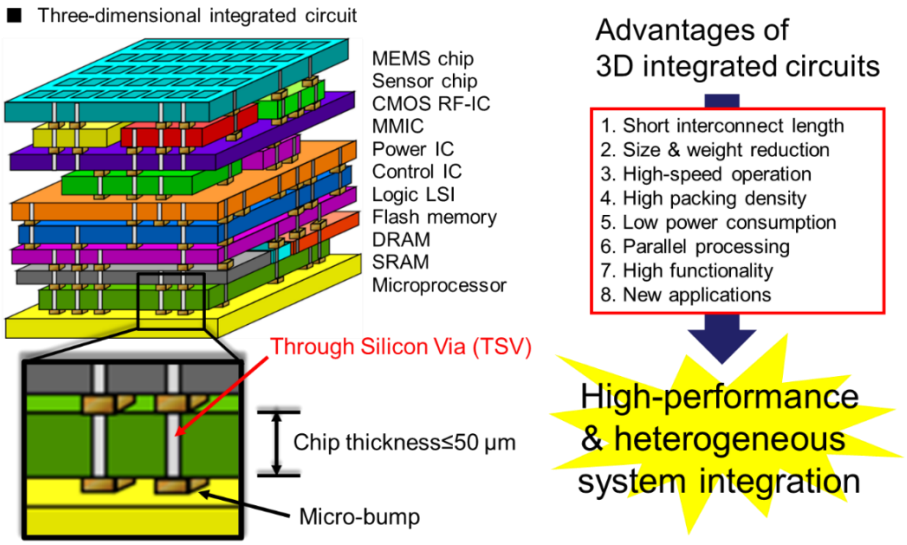


Fig. 1-2 Features of 3D-IC

3D-IC is undoubtedly a very promising technology, but it also has many difficulties. Because of this, current research has focused heavily on heterogeneous integration, which is based on 3D-IC technology. More recently, 3D-DRAM [10][11] has been divided into several high-bandwidth memory (HBM) [12]-[15] and heterogeneously integrated with CPUs. A comparison of high-bandwidth memory (HBM) and conventional DRAM is given in Fig. 1-3; HBM uses 3D stacking To dramatically increase the number of inputs and outputs, resulting in a very wide overall bandwidth. The most recent standard, HBM3, has a bandwidth of 896 GB/s [16]. As seen in Fig. 1-4, silicon interposers connect the HBM and logic, as described below.

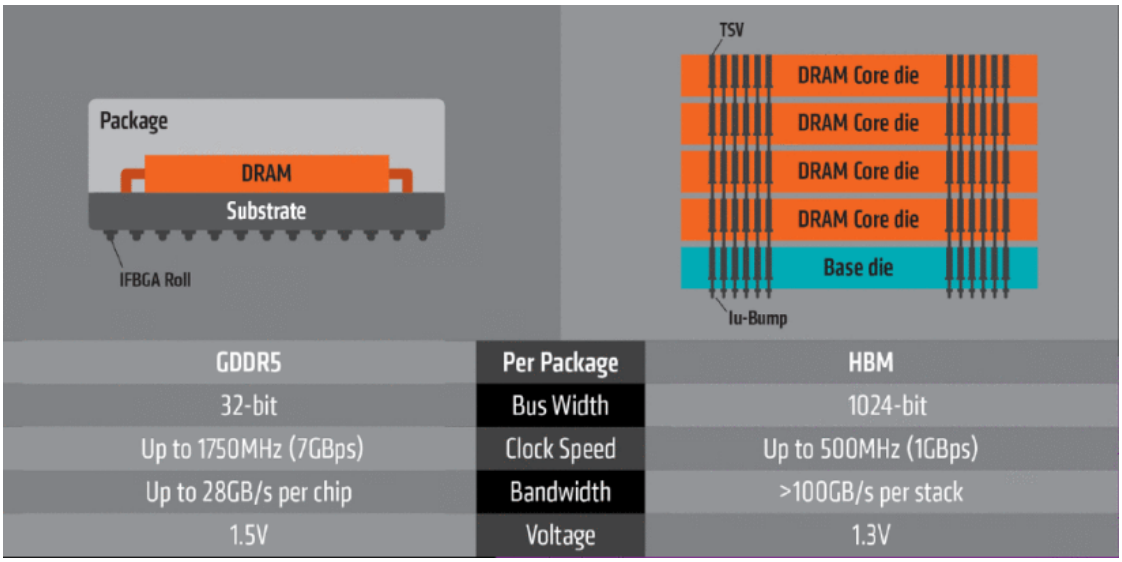


Fig. 1-3 Comparison of conventional DRAM and HBM [14]

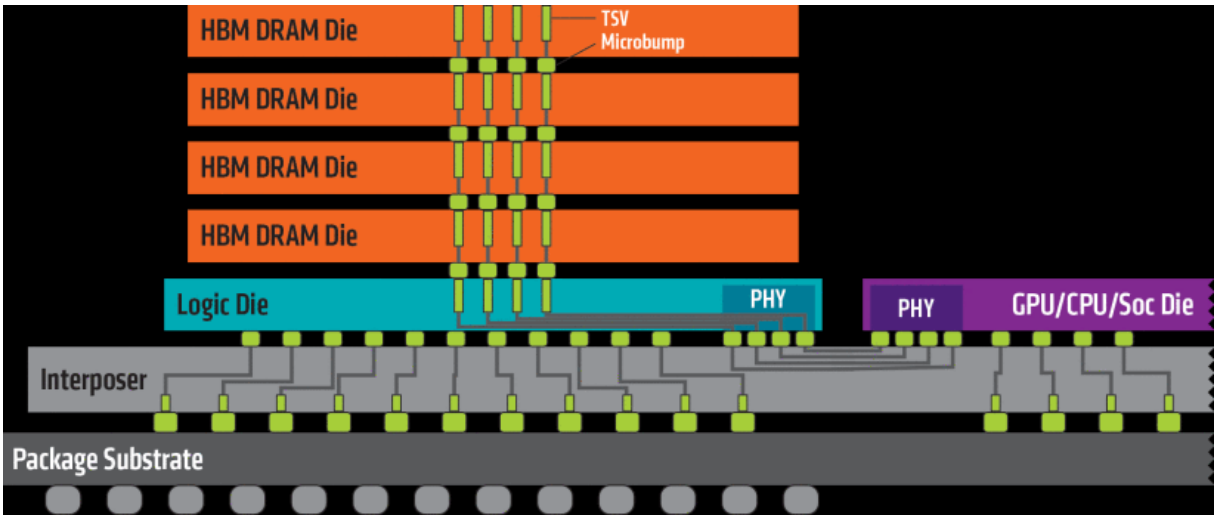


Fig. 1-4 Cross-section of HBM package [14]

Such a heterogeneous integration architecture is also increasingly used to three-dimensionally stack logic chips manufactured at different technology nodes [17] as shown in Fig. 1-5.

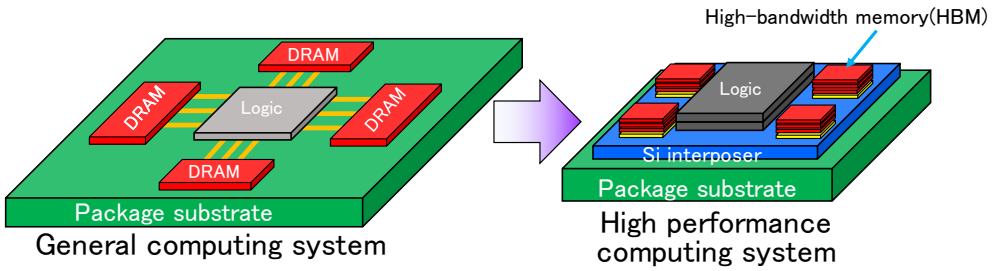


Fig. 1-5 Schematic of heterogeneous integration

The 2.5D package, which incorporates the aforementioned Si interposer and interconnects the chips, is known as a 2.5D package. Chip on Wafer on Substrate (CoWoS) technology, created by TSMC, served as the foundation for 2.5D packages [18]-[22], CoWoS is displayed in Fig. 1-6. The Si interposer is the key component of CoWoS, which preserves the advantages of integrating numerous dies while avoiding the problems that 3D-ICs have, such as heat

difficulties [23]. Si interposer has the following benefit : (1) Smaller form factor (total circuitry size) in comparison to PCB-board integration, (2) much higher bandwidth between memory and logic dies, (3) lower power consumption because there are fewer large IOs among chips on a PCB board, and (4) quicker turn-around time to integrate multiple-node chips without implementing cutting-edge technology from scratch[24]. For these reasons, Si interposers attracted much attention [25][26].

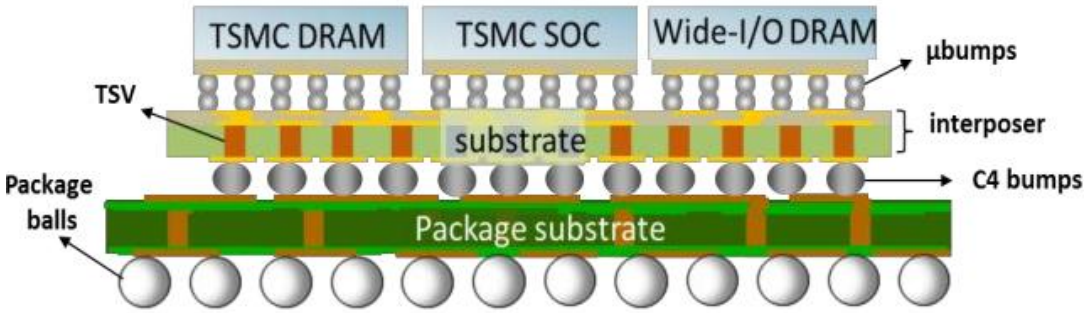


Fig. 1-6 Schematic of CoWoS [22].

Furthermore, organic interposers have attracted attention in recent years [27]-[29]. The size of Si interposers that can be produced using the wafer process is limited by the size of the reticle used for lithography. This precludes the integration of big ASICs with high functionality that need lots of HBMs. Organic interposers, on the other hand, can be used in greater sizes because they are made at the panel level. Table 1-1 shows a comparison of the Si interposer and the organic interposer.

Table 1-1 A comparison of the organic interposer and Si interposer [30]

Features	Organic Interposer	Silicon Interposer
Cu Wiring (Dielectric)	SAP Pattern Plating (Organic)	Damascene (Oxide)
Front Side UBM or pad size / pitch (min.)	30 / 55 μm	25 / 55 μm
Front Side wiring line / space / thickness (min)	6 / 6 / 10 μm	0.5 / 0.5 / 1.0 μm
Number of routing layers (typical)	10	4
Wiring layer via size	20 μm	1.0 μm
PTH or TSV size / pitch / depth	57 / 150 / 200 μm	10 / 50 / 100 μm
Back Side UBM or pad size / pitch	100 / 150 μm	100 / 150 μm
Back Side wiring line / space / thickness (min)	6 / 6 / 10 μm	10 / 10 / 1.0 μm

1.3 Fan Out Wafer Level Packaging (FOWLP)

FOWLP is a packaging method created by Infinion in 2005 [31]. There are two types of FOWLP: RDL-first, in which the chip is bonded after wiring is created, and die-first, in which the chip is enclosed in hard resin before wiring is created.

The corresponding process flows are shown in Fig. 1-7 [31]. Die-first method, in particular, does not necessitate bumps, thus allowing for a low-profile package and streamlining the procedure. Due to these characteristics, FOWLP, including integrated fan-out (inFO) [32]-[34], which is a derivative of die-first FOWLP, is employed in the production of mobile processors, where space-efficiency and cost-efficiency are crucial considerations.

However, it is now also being utilized for packaging for heterogeneous integration, due to its capacity to combine many types of chips [35]-[37]. FOWLP is applied to applications where performance is critical, such as the production of processors for Tesla's Dojo supercomputer [38],

which does machine learning for automatic driving. The technology is also being used in situations where performance is crucial.

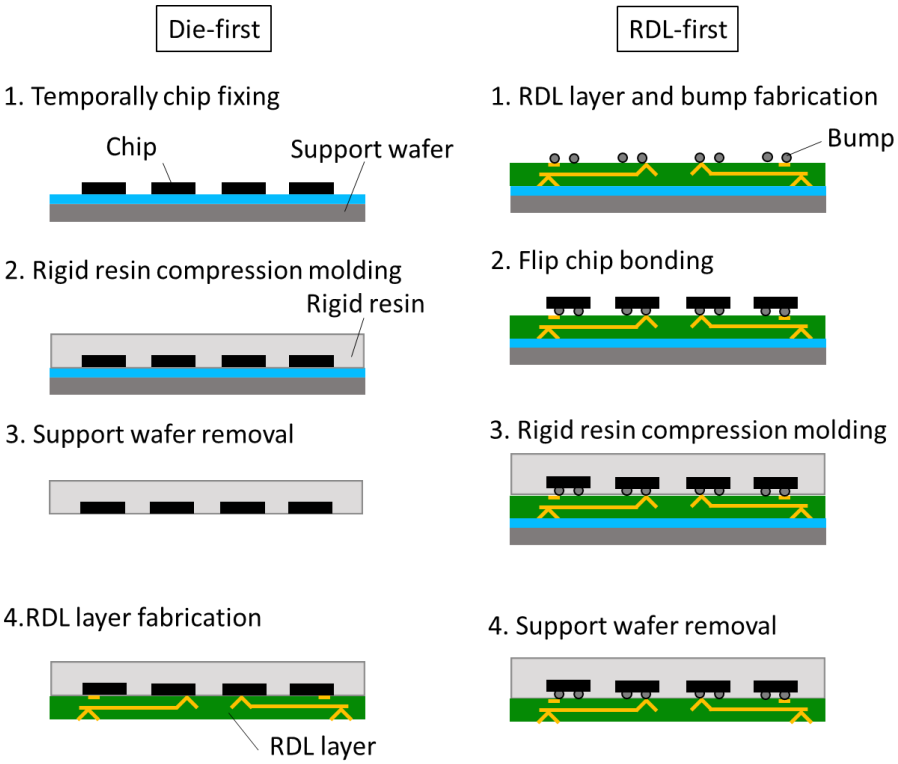


Fig. 1-7 Process flow of two type FOWLP

1.4 Flexible hybrid electronics

In recent years, wearable devices, implantable devices, and the Internet of Things have become increasingly popular as devices have become smaller and lighter, and the development of wireless communications made it easier for device-to-device connections, thus diversifying the applications of electronic devices. However, conventional devices are limited by the shape of their internal printed circuit boards, making them impossible to bend. Because of this, flexible devices using flexible substrates instead of rigid printed circuit boards have recently been developed, and

many flexible devices based on organic semiconductors [42][43][44] and thin film transistors (TFT) [45][46]have been reported. However, there are several problems with conventional flexible devices using organic semiconductors: First, the electron mobility of organic semiconductors is lower than that of inorganic single-crystal semiconductors such as Si. The hole electron mobility of organic semiconductors has been increasing year by year, and some organic semiconductors with electron mobility exceeding 30 cm2V-1s-1 have been reported in hole-transporting semiconductor polymers [47]-[51], However, it falls short of the 450 cm^2/Vs hole electron mobility of single-crystal silicon. Since electron mobility is an important factor in determining the processing speed and power consumption of a circuit, it is challenging to construct high-performance devices that perform high-speed operations in organic semiconductors as it is with inorganic single-crystal semiconductor devices. The switching frequency of organic transistors is several MHz [52][53], which is significantly slower than the GHz switching frequency of inorganic semiconductor transistors.

The second problem is that it is challenging to produce printed wiring. The wiring width of ordinary printed electronics is several millimeters to several tens of millimeters [54][55], making it challenging to achieve high circuit integration and construct compact, high-performance devices. Since conventional printing methods such as inkjet and gravure are difficult to miniaturize, methods such as self-assembling metallic nano ink by combining hydrophobic and hydrophilic patterns have been proposed 0. Although this method can construct finer wiring than current methods, it is not yet practical because the resistance increases rapidly below 1 m[57].

The third problem is involved in the roll-to-roll procedure [58]. It is a method of creating circuits wherein rolled flexible boards are fed from one side of the production line and processed as shown in Fig. 1-8. It is then rolled up again on the other side of the production line before moving on to the next process. It costs money to transport distinct substrates that have been

separated from the start of the operation in the traditionally manufacturing process that uses rigid substrates The Roll-to-Roll method is expected to lower costs by connecting several manufacturing lines for continuous processing. However, it has been shown that during large-area sheet processing, the roll-to-roll operation results in sheet deformation [60]. This decreases yields and results in severe alignment errors. These problems issues have prevented, conventional flexible devices from performing as well as inorganic single-crystal semiconductor devices.

The field of flexible hybrid electronics (FHE) has been attracting attention [61][62]. FHE blends standard inorganic semiconductor device production with flexible electronics employing organic semiconductors. Devices with both high flexibility and high performance can be produced through FHE. A conceptual diagram of FHE is shown in Fig. 1-9. The FHE is a flexible substrate with a printed wiring system. Therefore, FHE can create flexible devices with the performance of traditional LSI chips. Flexible and biocompatible organic materials can be attached to or attached to the human body. Inorganic semiconductor chips with high-speed calculation capabilities are also suitable for processing complicated biological signals. For these reasons, FHE has attracted considerable interest in the medical and healthcare fields.

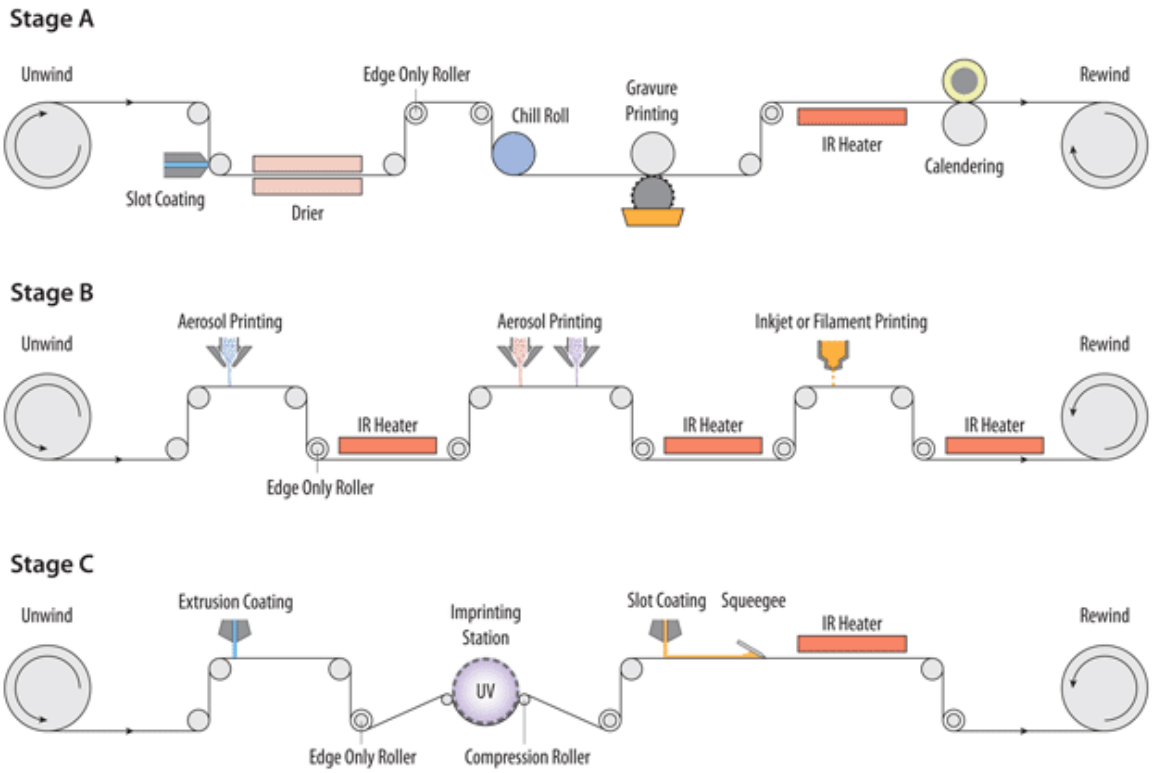


Fig. 1-8 Roll-to-roll process [59]

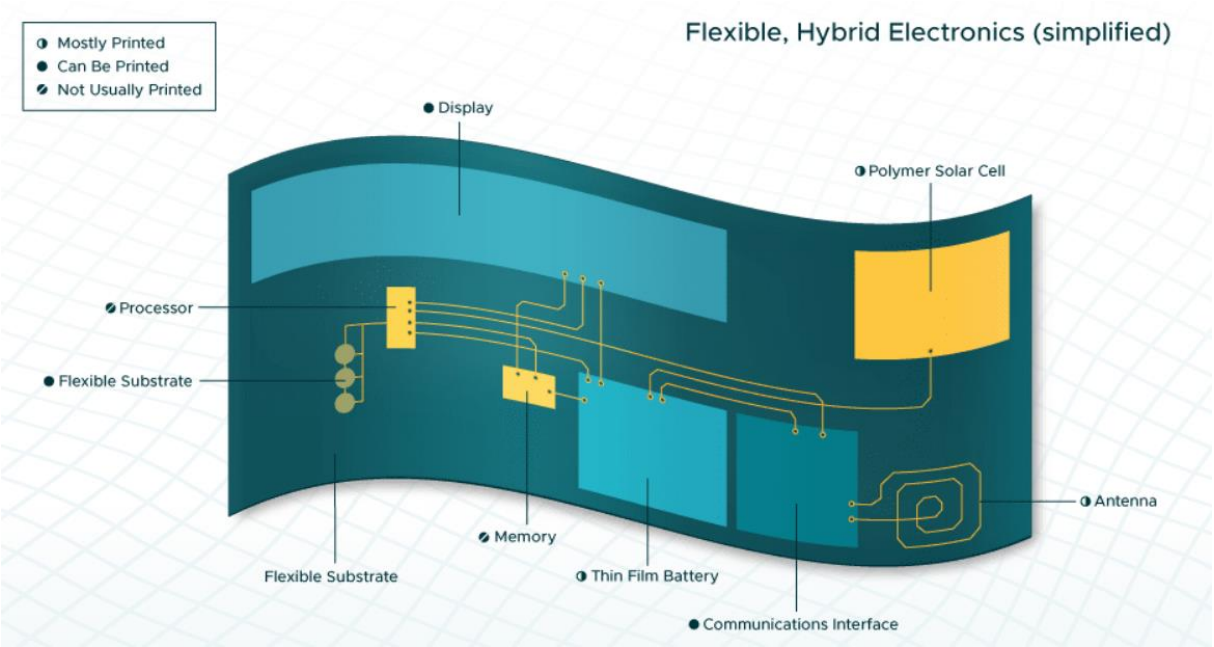


Fig. 1-9 Conceptual images of FHE [63]

1.4.1 Conventional FHE

It has been discovered that single-crystalline Si exhibits flexibility when manufactured extremely thin (ア). As illustrated in Fig. 1-10, when Young's modulus of a Si wafer is assessed using a nano indenter, Young's modulus rapidly decreases at a thickness of 50 μm or less. As seen in Fig. 1-11, it becomes so flexible that it can be easily bent by a finger. For the typical FHE process ultrathin dies (20 μm or less in thickness) must be created by backside grinding so they can be bent and follow curved profiles 0-[66]. The ultrathin dies can be technologically fabricated down to 7 μm or less [67][68]. The manufacture of flexible electronics using this property has been suggested [69]. Fig. 1-12 shows the concept of FHE using an ultrathin Si wafer. By embedding an LSI chip with an ultrathin Si chip in a flexible resin, flexibility is given to the entire device. However, one of the issues with devices using ultrathin Si chips is reported to be the degradation of device properties due to the thinning of Si (ア). A Young's modulus falls as DRAM chips with planar capacitors get thinner, as seen in Fig. 1-13, However, retention time gets shorter. This is hypothesized to be caused by the lattice structure distortion when the Si wafer becomes ultrathin. In addition, the durability against repeated bending has not been adequately evaluated, and the reliability is low.

Another issue is that the mechanical strength of the ultrathin dies is determined by thinning processes (chemical mechanical polishing, plasma etching, dry polishing, kai-dry polishing, poly grinding, ultra-poly grinding, #2000, etc.) [70]. Simple saw dicing and cost-effective mechanical grinding with dry polishing are not enough to relieve the mechanical stress and remove microcracks at the chip edges. Other intriguing methods to create ultrathin dies without using mechanical thinning procedures include a spalling technology [71] and transfer technologies from SOI wafers [72]-[74].

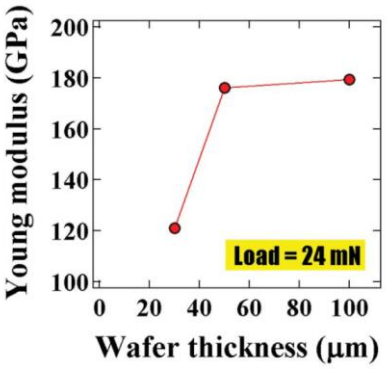


Fig. 1-10 Young's modulus variation versus wafer thickness

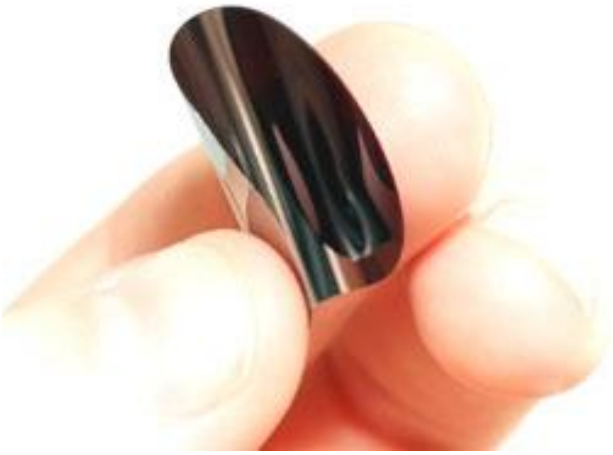


Fig. 1-11 Ultrathin Si wafer

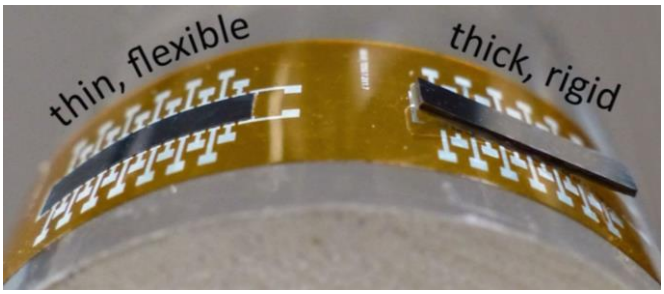


Fig. 1-12 FHE using ultrathin Si

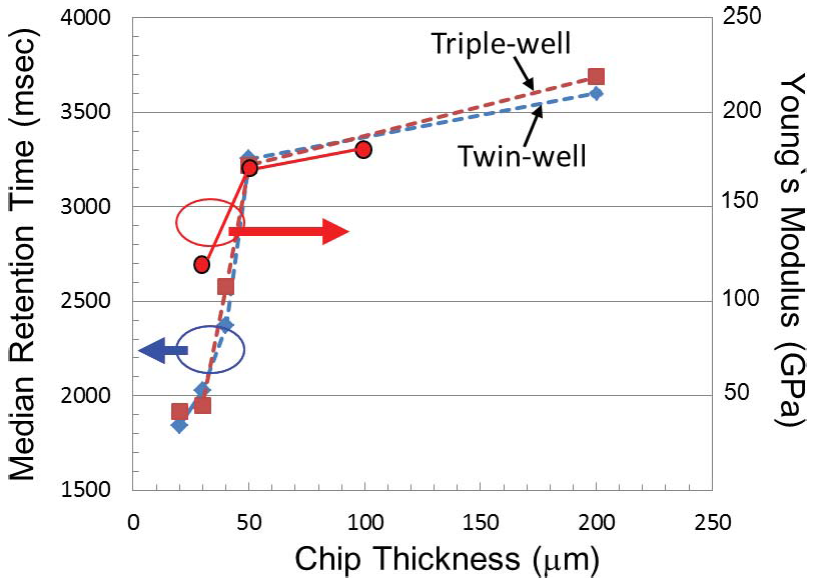


Fig. 1-13 Median retention time of DRAM cell array at 50% failure versus chip thickness.

FHE uses flexible wiring to connect the mounting region of semiconductor chips known as an island [75]. The flexible wiring absorbs bending stress in this technique, so no stress is placed on the semiconductor chip. Therefore, stress-related fluctuations in chip properties can be reduced. However, because of the extensive flexible wiring in this device, performance improvement cannot be anticipated despite the high integration.

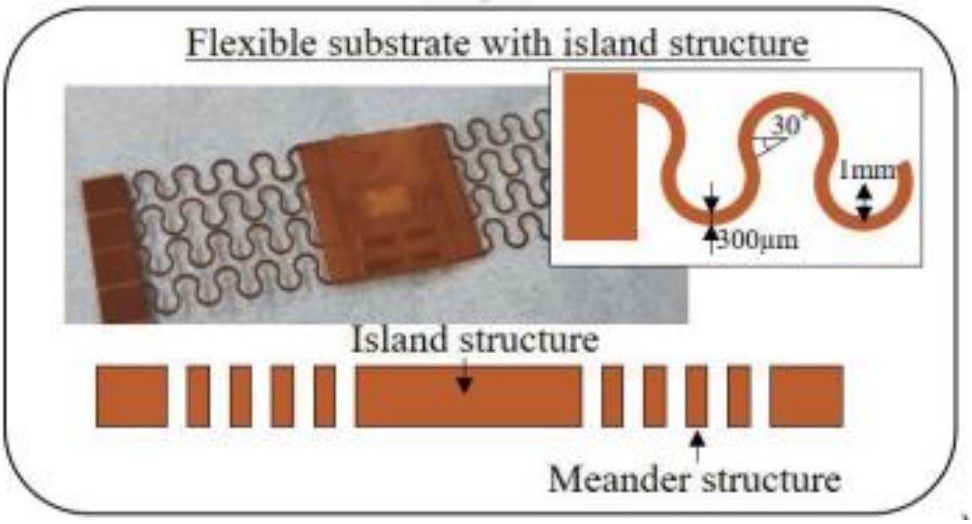


Fig. 1-14 FHE device with island structure [75]

1.4.2 New FHE in this study

I have talked about the problems with traditional FHE. Our laboratory has suggested a new flexible device structure [75][77]. Table 1-2 compares traditional flexible device technologies. The FHE devices in this research aim to solve the with traditional technologies and create high-performance flexible devices. This device uses inorganic single-crystal semiconductors, especially Si, and does not use organic, amorphous, or polycrystalline semiconductors. Additionally, the system can be highly flexible without bending Si itself and can achieve high performance. This highly integrated FHE applies the fan-out wafer-level packaging (FOWLP) procedure [78], in which several small LSI chips are embedded in a flexible substrate and connected with fine wiring created by a wafer-level process. The suggested procedure is to achieve high integration of FHE by embedding several small LSI chips in a flexible substrate and connecting them with fine wiring created by a wafer-level process as illustrated in Fig. 1-15. several moderately thin, rigid, small LSI chips are embedded in a flexible organic substrate, and the organic substrate between the chips bends to create high flexibility in the entire system. Since the chips are not very thin, devices can be made without affecting the performance of traditional LSI chips. In addition, wiring formation at the wafer level, which is a comparable step to the traditional Si device fabrication process connects chips tightly. Fig. 1-16 shows an actual FHE with 625 Si chips implanted in a flexible substrate.

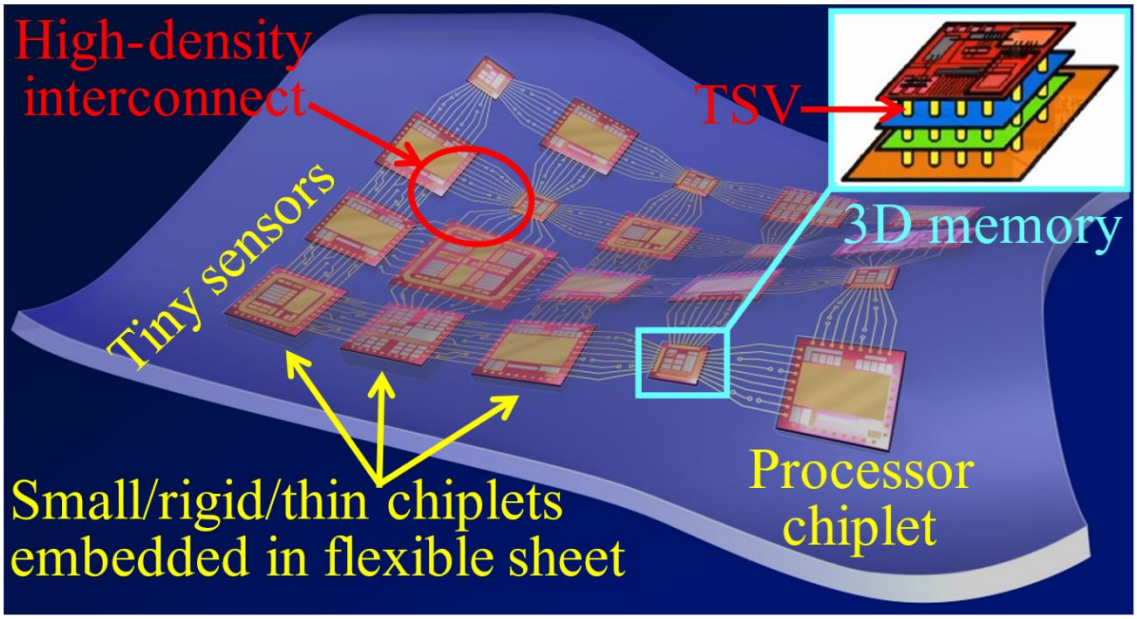
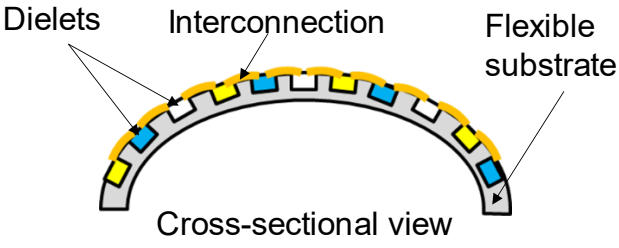


Fig. 1-15 Schematic illustrations of advanced FHE with embedded 3D-IC and heterogeneous dielets.



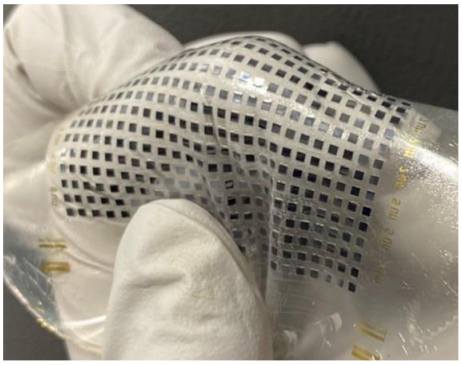
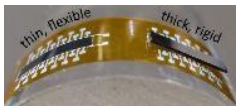


Fig. 1-16 Highly integrated FHE with 625 Si dielets

Table 1-2 Comparison of flexible device fabrication technology

	Si Electronics	Organic electronics	Conventional FHE	New FHE in this work
				
Device materials	Inorganic single crystalline semiconductors	Organic semiconductors	Inorganic and organic semiconductors	Inorganic single crystalline semiconductors
Interconnects	Photolithography	Printing	Printing	Photolithography
Processing	Sheet-level	Sheet-level	Sheet-level	Wafer-level
Performance	**High**	**Low**	**High**	**High**
Reliability	**High**	**Low**	**Low**	**High**
Flexibility	**Low**	**Extremely high**	**Midium**	**High**

1.5 Chiplet

Chiplets are system design techniques that integrate numerous module chips into a single package to create hetero-integrated systems [79]-[83]. According to Moore's law, the chiplet is expected to be a potential driver for advancing performance scaling as well as size scaling in the future. The figure illustrates a conceptual diagram of a chiplet. Chiplets are individually constructed functioning blocks. With the aforementioned 3D/2.5D packaging technologies, chiplets are joined by cutting-edge microelectronic packaging techniques such as redistribution layers (RDLs), solder micro bumps, and TSVs. Products incorporating the chiplet are already being sold as high-end processors as shown in Fig. 1-18 [84].

Fig. 1-17 Schematic of chiplet [85]

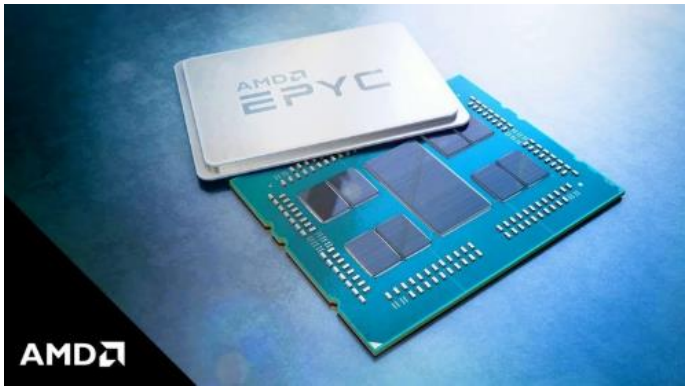


Fig. 1-18 Chiplet-based processor [84]

As shown in Fig. 1-19, development costs are increasing rapidly as technology nodes become smaller [86]. Therefore, it is getting more and more challenging to continue with traditional monolithic integration. Chiplet may reuse individually made chips, thus efficiently addressing issues such as development cost and time. Chiplets are Si's intellectual property subsystems and not s smaller SoC-partitioned chip (system on a chip). Therefore, standardization is required to integrate chiplets more successfully. The Common Heterogeneous Integration and IP Reuse Strategies (CHIPS) program of the Defense Advanced Research Projects Agency served as the first impetus for the chiplet ecosystem [87]. Standardization is currently being promoted by industry associations led by Intel [88]. Standardized chiplets helped to effectively accelerate the

speed of development but also reduce the development expenses and threshold while also speeding up development., Chip R&D will therefore concentrate on algorithms and basic technologies, greatly increasing the overall level of innovation and capability.

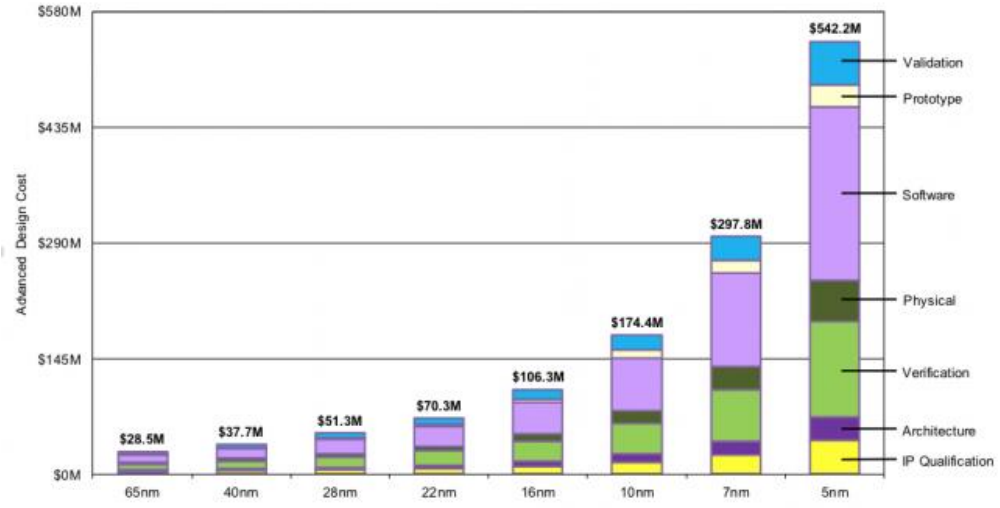


Fig. 1-19 Chip Design and Manufacturing Cost under Different Process Nodes [86]

1.6 Definition of dielet

The collection of little die that will be used in the FHE in this investigation is called “dielet.” Chiplet is a system design methodology that interconnects chips manufactured in different technology nodes utilizing cutting-edge packaging techniques such as 2.5D packaging To produce a high-throughput, high-performance package. Chiplet is a function-focused idea that considers which technological node to build each functional block. On the other hand, dielet is a concept that emphasizes only geometry. A dielet is a die that is only a few millimeters in size that can be used to build a flexible system using the FHE technology in this research [39]-[41]. Fig. 1-20, a dielet's notion is depicted. In general, chips designed based on chiplets are functional blocks such as logic, memory, and analog circuits that are typically separated from conventional SoC. These chips along with other chips such as sensors, MEMS, passive devices, and optical devices like

VCSELs, LEDs, and mirrors are all included in dielets. This research aims to develop flexible systems with significantly higher integration than traditional flexible devices by incorporating dielets.

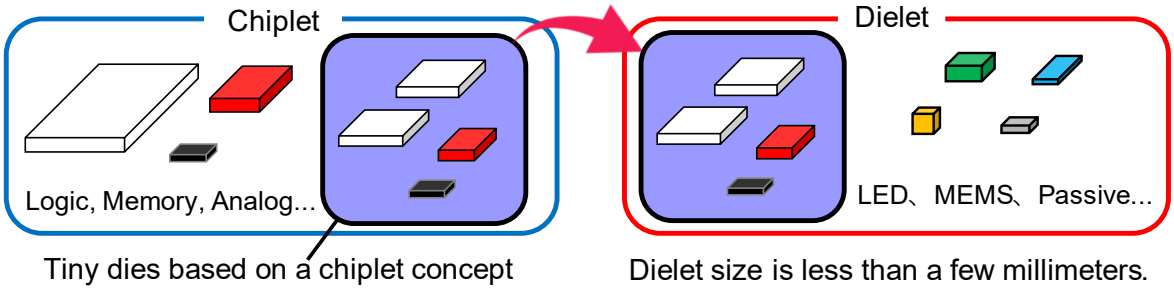


Fig. 1-20 Concept of dielet.

1.7 Blood vessel visualization device

Arteriosclerosis causes stenosis or blockage of blood vessels in the arteries throughout the body. For instance, blocked arteries in the brain can result in cerebral infarction and blocked coronary arteries in the heart can result in angina pectoris or myocardial infarction. When arteries in the limbs get blocked and are unable to deliver nutrients and oxygen sufficiently, symptoms such as coldness at the tips of the limbs and aching muscles occur. This condition is called arteriosclerosis obliterans (ASO). It is crucial to take care of the foot every day because, in the worst-situation, ASO might result in the amputation of the foot. Echocardiography and Computed Tomography (CT) are used to diagnose ASO. The figure displays a CT scan image of an ASO-induced stenosis. These tests require a hospital visit.

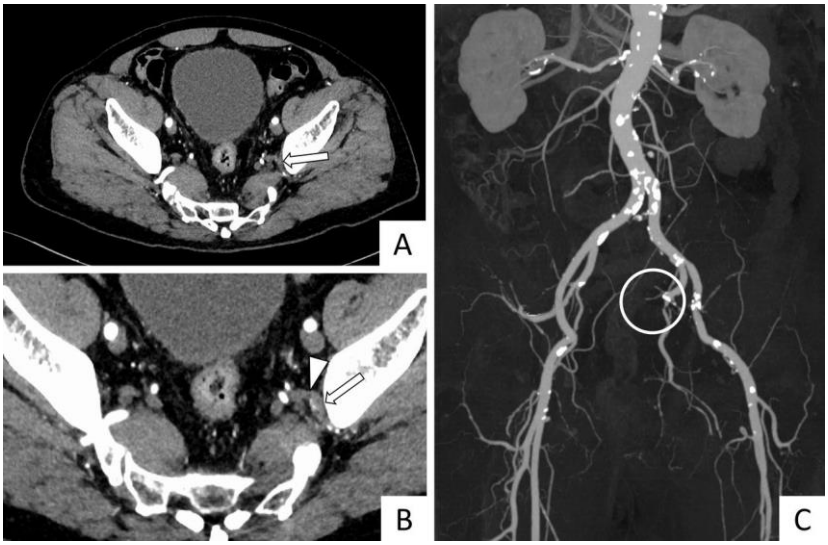


Fig. 1-21 Abdominal CT with contrast enhancement. (A) Axial view, (B) an enlarged axial view, and (C) a three-dimensional image of the arteries. The site of occlusion was the left superior gluteal artery (A and B, arrows; C, circle). The low-density area in the enlarged axial view was suspected to be a thrombus (B, arrowhead)[89].

Currently, a portable tool that can visualize blood vessels is in practical use in the medical industry as a vascular imaging tool to help with punctures. Fig. 1-22 shows an illustration of the use of this device. This device can be used at home because it does not require a physician or nurse expertise, like an echo or CT scan, this gadget can be utilized at home. Fig. 1-23 The hemoglobin in red and infrared light absorption spectra is depicted. Hemoglobin in blood vessels tends to absorb infrared light and thus reflects less infrared light than other living tissues. Using this method, the gadget illuminates the skin with infrared light and measures how much light is reflected light to detect blood vessels. However, the device must be utilized at a proper angle and distance from the skin, and the hand-held nature of the device has the drawback that one hand is occupied. Foot care, techniques for preventing foot disease, requires checking blood circulation as well as visually inspecting and palpation of the skin and nail condition of the toes. Therefore, for the vascular visualization device to be a wearable type that allows both hands to be free so that patients can check the blood circulation in their feet as part of foot care.

Fig. 1-22 Hand-held vascular visualization device. (Upper) Accu Vein[90]. (Lower) Vein Viewer Flex[91].

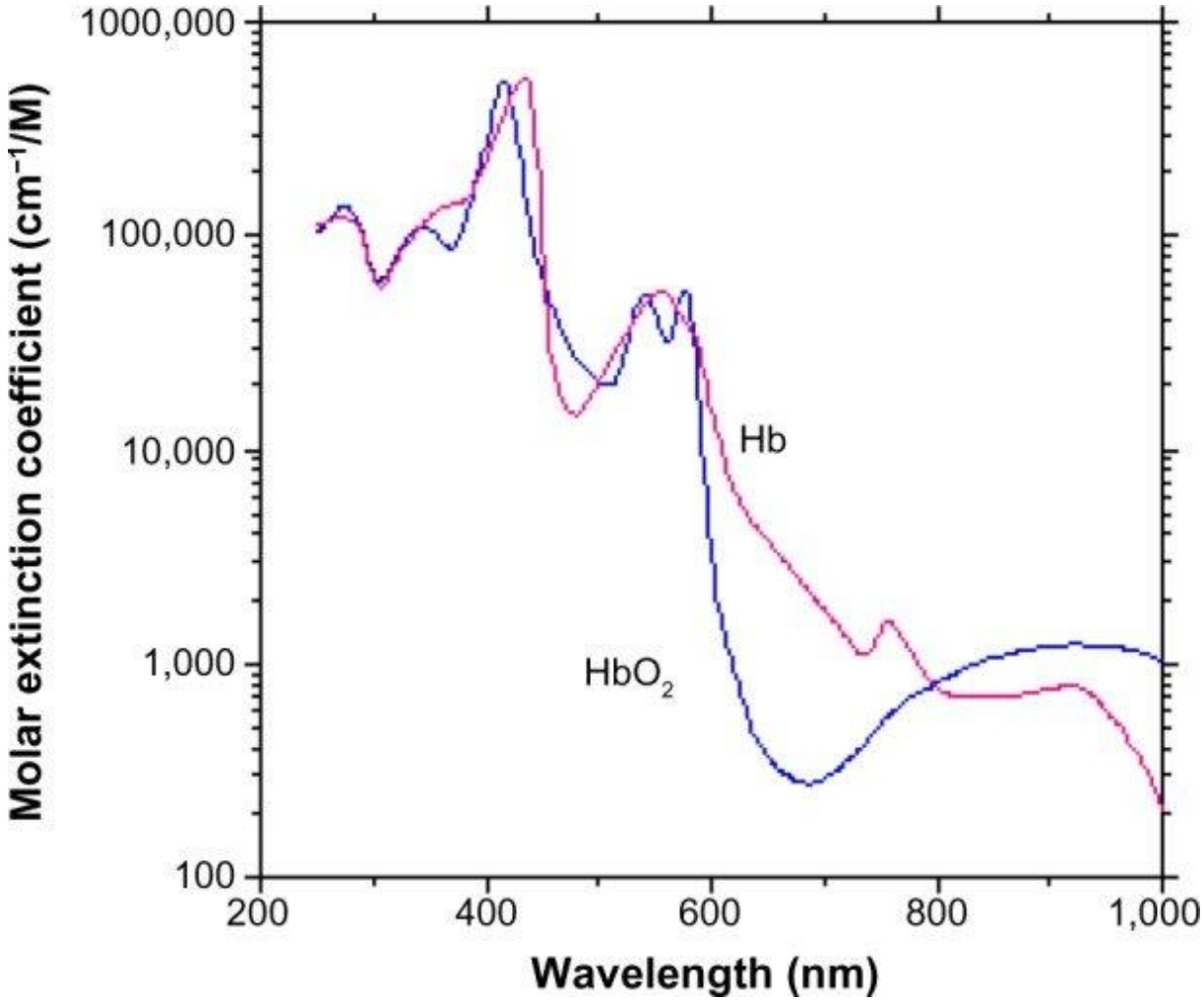


Fig. 1-23 Absorption spectra of the oxygenated and deoxygenated hemoglobin molecules[92].

1.8 Smart Skin Display

A display that can be affixed to the skin has been proposed [93]. However, the function of skin displays in past research is limited to displaying information. I am suggesting Smart Skin Display, which is depicted in Fig. 1-25. The IR/Red mini-LED, 3D-IC, and micro-LED components of this gadget. The operation flow of Smart Skin Display is shown in Fig. 1-26. Because this device is wearable, it can be palpated with both hands, which is not possible with traditional hand-held devices. As a result, the technology makes it easier for healthcare professionals can use the device

to diagnose ASO. In addition, the device can assist with a puncture in the same way as conventional devices. A puncture is invasive and carries risks such as infection. In addition, the blood vessels' appearance differs from person to person. The strain on the patient is reduced because puncture may be performed reliably, even in patients with poor blood vessel visibility, because of the device's ability to visualize blood vessels. Furthermore, Smart Skin Display also has functions for measuring heart rate and oxygen saturation (SpO_2) that are not available with conventional devices. Therefore, Smart Skin Display alone can complete the collection of biometric information required for diagnosis.

IR and red light are irradiated onto the human arm, and a photodiode measured the intensity of the reflected light from the subcutaneous tissue and hemoglobin in the 3D-IC chip to monitor pulse wave and SpO_2. These signals are processed in the 3D-IC and transferred through an LED driver included in the 3D-IC to a blue micro-LED that is stacked vertically on the 3D-IC. In the end, the device will show visual blood information. As previously mentioned, the result information is visualized by a flexible micro-LED display called Smart Skin Display. In this study, a highly functional flexible display that can acquire and interpret biological information was created by combining the dielets with the FHE technology. The specifications for Smart Skin Display are inTable 1-3. For bending durability, the bending radius was set at 2 cm, given that the average human wrist is approximately 5 cm, wide [94]. 1,000 bending cycles were designed to endure bending for more than one year, even when used once a day. designed to endure durability to withstand severe bending of 1 mm is also necessary due to the potential for bending during handling.

There are four key technologies to accomplish the advanced FHE integration, as depicted in Fig. 1-27. 1) Multi-level metallization on a flexible substrate 2) Die shift reduction, 3) Room-temperature bonding of micro-LED, and 4) assembly, bonding, and interconnection of tiny micro-

LED on 3D-IC.

This thesis aims to develop these key technologies and create a fabrication process for Smart Skin Display.

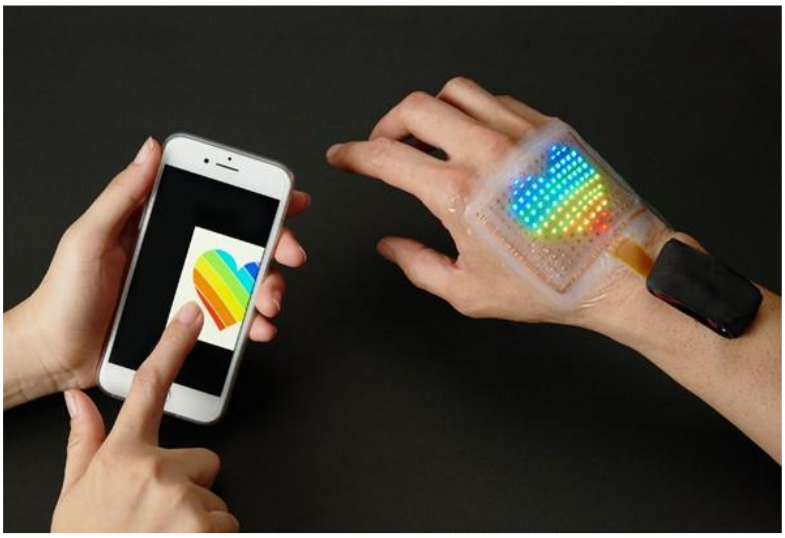


Fig. 1-24 Conventional skin display[93]

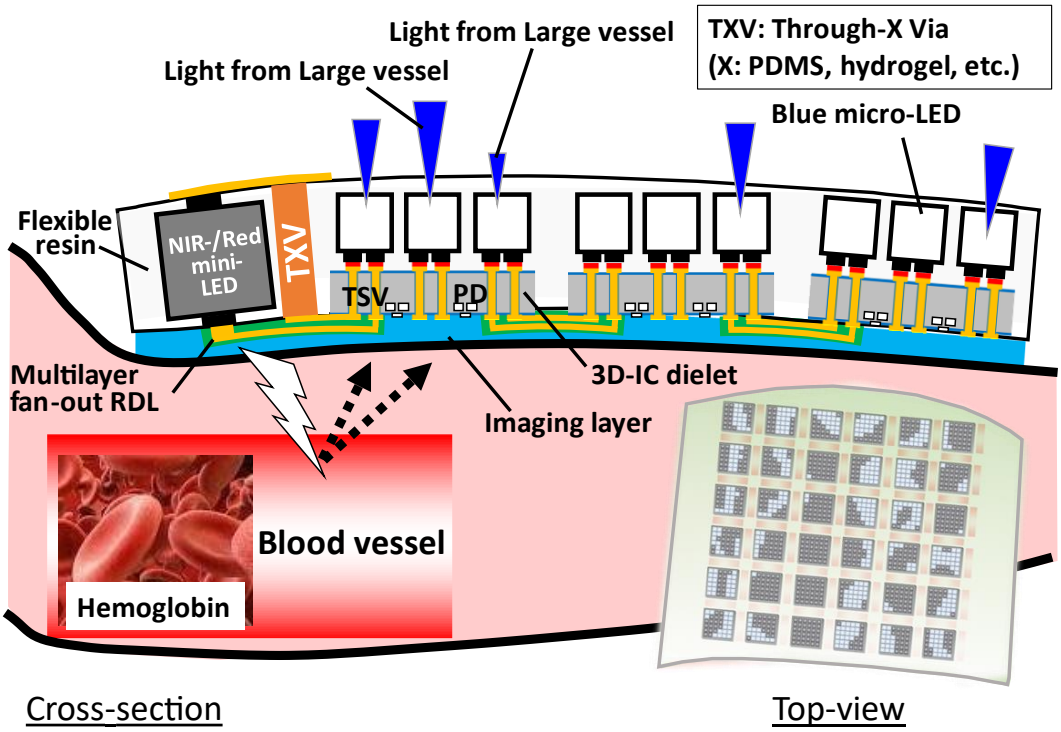


Fig. 1-25 Concept of Smart Skin Display

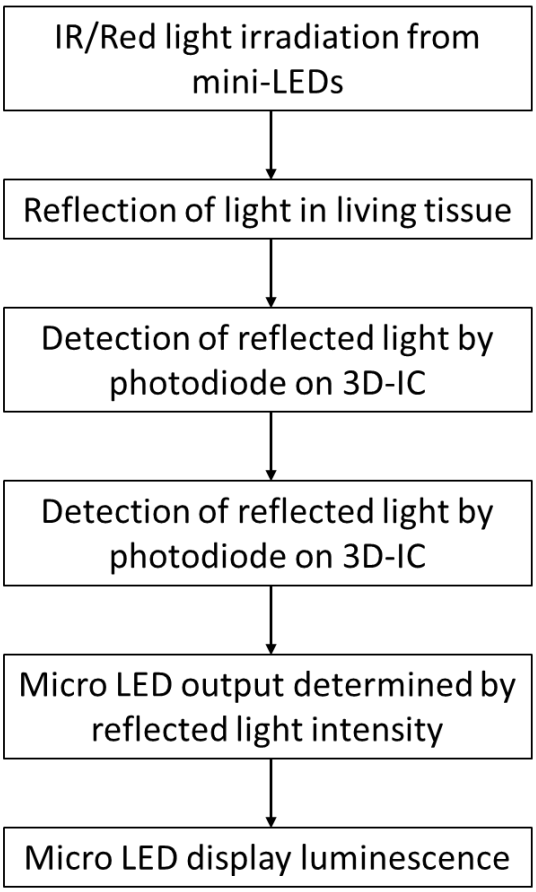


Fig. 1-26 Operation flow of Smart Skin Display

Table 1-3 Specification and requirements for Smart Skin Display

Display	resolution	Approx. 60 ppi
Multilayer flexible wiring	Wiring width	50 μm
	Wiring pitch	80 μm
	Number of layers	2
	Bending durability in wearing	1000 times at a radius of curvature of 20 mm
	Folding durability in handling	100 times at a radius of curvature of 1 mm
Mini-LED	Size	IR LED:330 μm (L) x 330 μm (W) x 300 μm (H) Red LED: 370 μm (L) x 370 μm (W) x 300 μm (H)
	Dieshift tolerance	±10 μm
Micro-LED	Size	100 μm (L) x 100 μm (W) x 100 μm (H)
	Bonding temperature	Room-temperature
	Bonding pitch	300 μm
3D-IC	Size	2.5 mm (L) x 2.5 mm (W) x 40 mm (H)
	TSV diameter	8 μm
	TSV depth	30μm

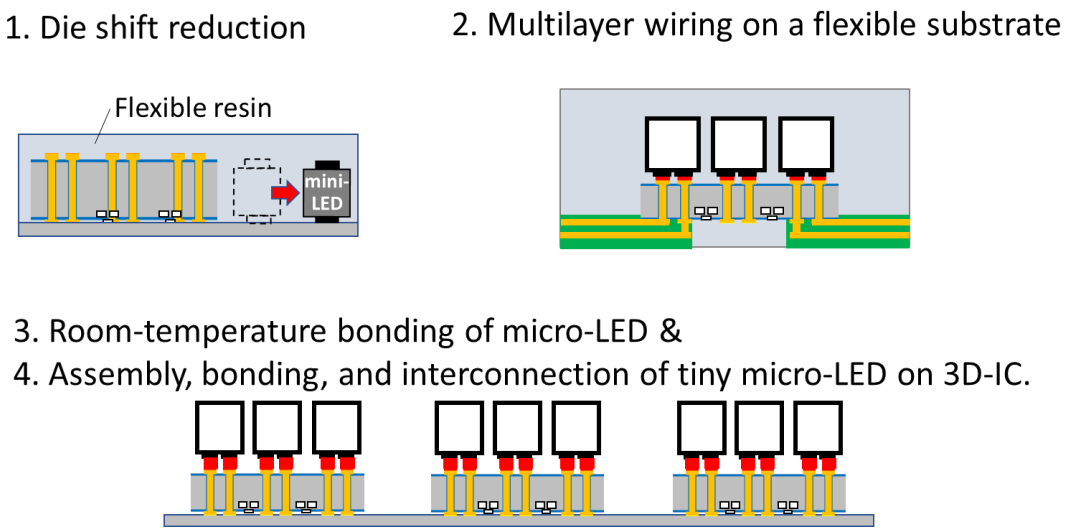


Fig. 1-27 Key technology of Smart Skin Display

1.9 Objectives and organization of the dissertation

This thesis contains five chapters. The contents of each chapter are as follows.

The structural design and manufacturing procedure of a highly integrated FHE device fabrication process are covered in Chapter 2. The design and fabrication process for flexible multilayer wafer-level interconnections is discussed in this chapter. Additionally, multilayer interconnects need to be bending-resistant mechanically. A structural design based on the stress-neutral axis is offered as a solution to this issue to reduce the stress on the interconnections. Additionally, a technique to prevent die shift is presented in this chapter. Alignment errors are brought on by die shift, which happens during the compression molding of resin wafers. The steps to take to address this issue are discussed.

The development of room-temperature electroplating direct bonding for heterogeneous dielet stacking is discussed in Chapter 3. When mounting small micro LEDs to 3D-ICs, in particular, conventional bonding of 3D-ICs necessitates thermocompression bonding, which may result in

3D-IC's destruction. I created a technique that permits bonding at room temperature and conducted a failure analysis to address this issue.

In Chapter 4, a via-last TSV formation methodology is used to fabricate 3D-IC dielets. High-aspect-ratio Cu-TSVs are needed for 3D-IC prototyping because small diameters give low TSV capacitance to demonstrate high signal transfer, and long TSVs mean relatively thick Si enough for mechanically tough chips. I compared the step coverage between long-through and standard PVD. By boosting the production of high-energy sputtering flux, low-frequency substrate RF vias were installed into the former PVD to re-sputter the bottom Cu and deposited the Cu at the bottom sidewall. Finally, I used the usual PVD to produce void-less via-last Cu-TSV and confirmed the maximum aspect ratio needed to fill deep Si holes with electroplated bottom-up Cu. Additionally,0.1-mm-squre blue micro-LEDs were stacked on the 3D-IC having the Cu-TSVs that were interconnecting to the micro-LEDs, and the usefulness of room-temperature electroplated direct bonding was verified by the heterogeneous 3D integration based on dielet-on-wafer stacking technology.

The conclusions to this theory are shown in Chapter 5.

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Chapter 2
Structure design and fabrication of new flexible hybrid electronics

2.1 Introduction

2.1.1 Conventional flexible wiring

Flexible printed circuits (FPC) are flexible wiring employed in conventional silicon electronics. FPC is indicated in Fig. 2-1. FPC refers to substrates in which circuits are created by metals such as copper foil on an insulating, thin, soft base film such as polyimide. Because they can be arranged three-dimensionally, taking advantage of small gaps in electronic devices, FPC is frequently utilized in portable and wearable electronics due to its lightweight and flexibility. Additionally, numerous devices have been reported in which semiconductor components are incorporated utilizing printing and other techniques into the base material [1]-[9]. But this flexible wiring only provides a little amount of flexibility. Flexible substrates cannot form fine wiring at the wafer level since they are formed through sheet-level procedures. Contact holes connecting the layers are created by laser processing, but the alignment accuracy of laser processing can deviate by several tens of μm, so taking into account the minimum wiring width and alignment accuracy of contact holes, the minimum wiring pitch of multilayer wiring that can realistically be formed is about 100 μm. Recent advances in flexible electronics have resulted in contact hole diameters as small as 70 μm, and multilayer interconnections with a wiring pitch of fewer than 100 μm are on the horizon. Flexible electronics multilayer interconnects technology in flexible electronics is still in its infancy, nonetheless, given the nanoscale size of semiconductors as of

right now.

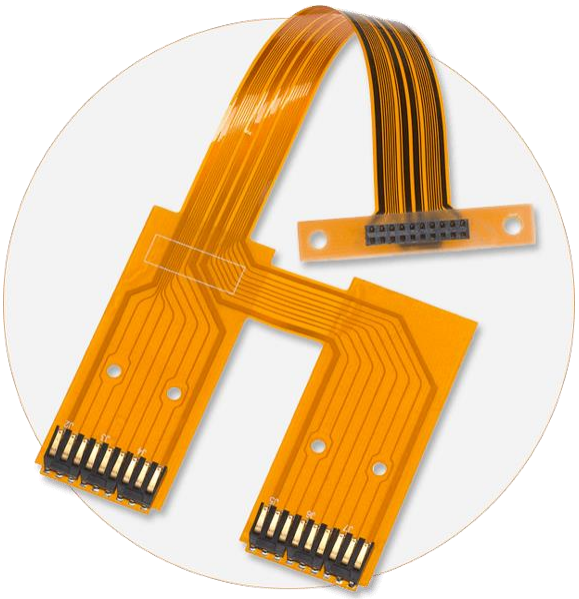

Fig. 2-1 Flexible printed circuit [10]

Flexible wiring with higher flexibility has been reported at the research level. the two approaches to improving wiring flexibility are: one is to introduce complex structures such as horizontal wavy wiring [11]-[17][16] or vertical wavy wiring [18]-[24][23]. Horizontal wavy wiring is depicted in Fig. 2-2, and vertical wavy wiring is in Fig. 2-3. Despite their high stretchability, these have issues of low wiring density and long wiring length. Another approach is to form circuits using conductive materials that are inherently stretchable. For instance, stretchable wiring is created using conductive inks or liquid metals [25]-[34] as seen in Fig. 2-4. These materials have higher resistivity than solid metals such as Cu and Au. Additionally, the printing technique makes it difficult to create precise wiring.

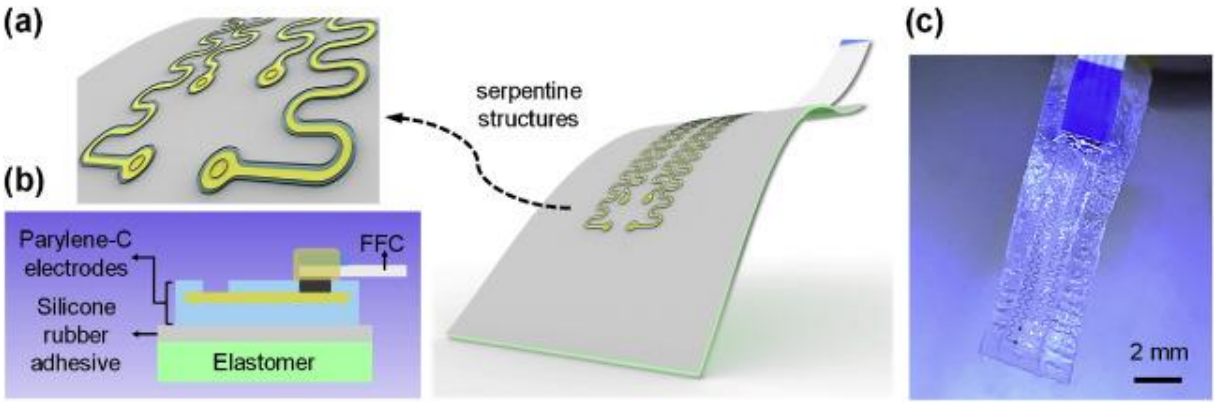

Fig. 2-2 Horizontal wavy wiring [25]

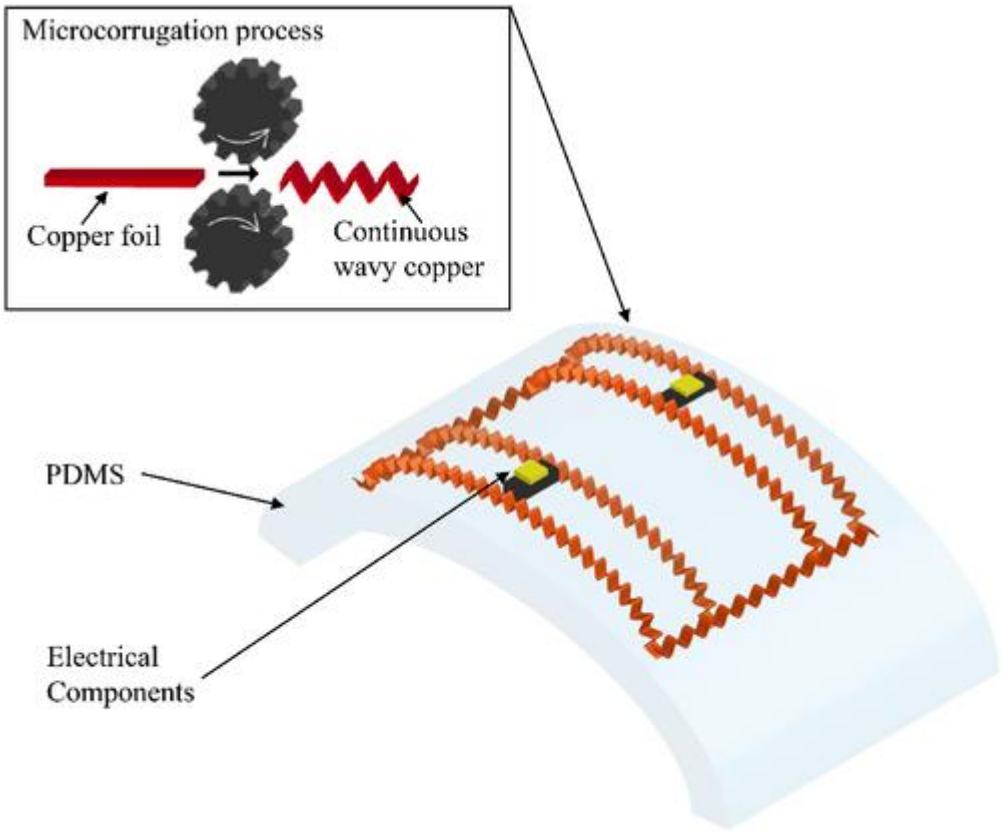

Fig. 2-3 Vertical wavy wiring [19]

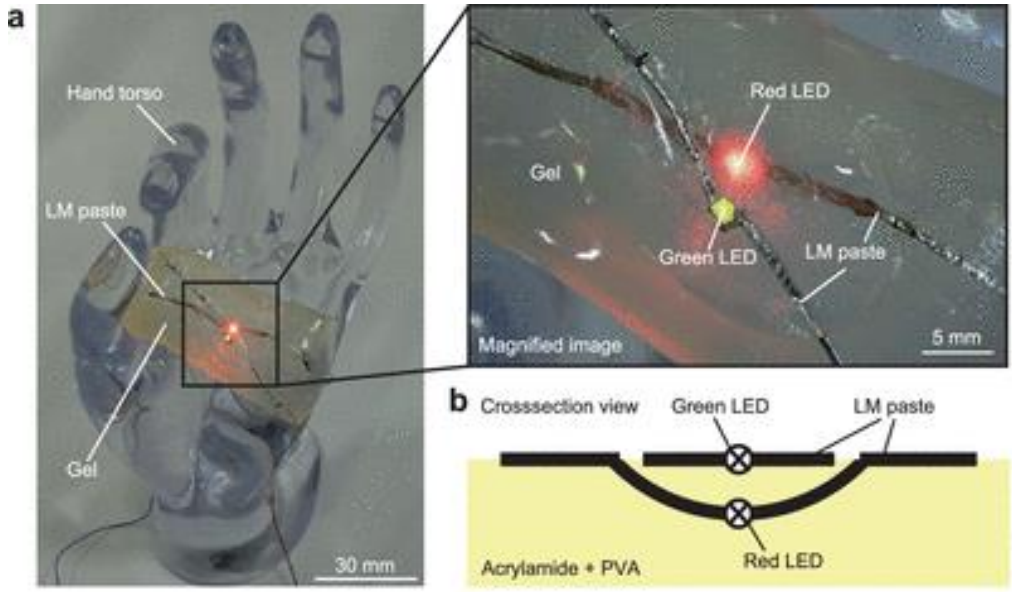

Fig. 2-4 Construction of the system on a gel substrate using LM paste [34].

2.1.2 Flexible wiring in this work

Metal wiring on flexible substrates was fabricated in this work using wafer-level photolithography. Consequently, finer wiring than conventional flexible wiring can be formed. Low resistance is also a result of the wiring material's solid metal construction and great conductivity. Up to this point, I have reported on this flexible wiring [35][36]. However, issues still exist.

The resistance of the interconnects rises with the number of bending cycles until eventually current cannot flow through them. As observed from Fig. 2-5, the metal wiring fabricated on the flexible substrate is peeled off from the substrate and broken by the stress of repeated bending.

The need to significantly enhance wiring density is another problem. The flexible wiring I have reported so far is a single layer. However, to link the parts of Smart Skin Display, multilayer wiring is essential. This study will create a two-layer wiring with a width of 50μm, which is needed for Smart Skin Displays.

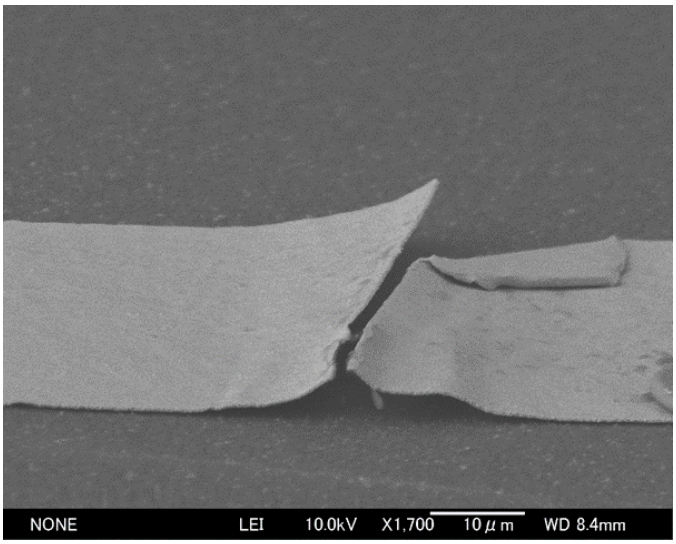

Fig. 2-5 SEM image of broken Au wiring on PDMS

2.1.3 Die shift issue

As depicted in Fig. 2 6, “die shift” is the term for chip migration during the resin compression molding process. Die shift is believed to be brought on by thermomechanical (TM) effects caused by differences in coefficient of thermal expansion (CTE) and fluidic-force (FF) effects caused by resin flowability. Die shift is a severe issue in conventional FOWLP, and various approaches have been used to address it.

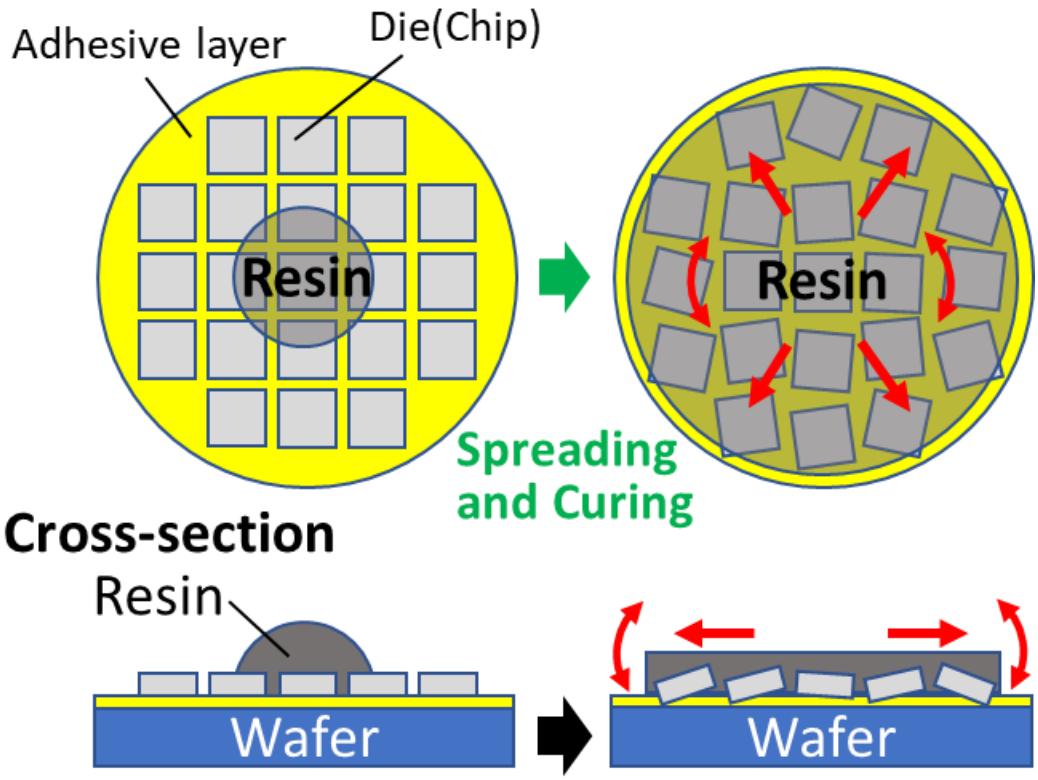

Fig. 2-6 Schematic diagram of die shift.

Table 1 lists previously documented "die shift" works using hard epoxy mold compositions. Die-shift phenomena have been explored in depth since 2009[37] where die shift at the outermost dies of wafers were exceeding 100 μm. The die-shift of the thicker dies is 8% less than that of the 700- and 300-μm-thick dies. The maximum die shift in a wafer was reduced from 633 μm to 79 μm [38] by the use of carrier wafers and pre-shift procedures. According to several studies, using a die with more surface area, enhancing chip insertion load and adhesion between dies and temporary adhesives/tapes, selecting lower viscosity molding compound material, increasing the mold compound thickness, and lowering compression speed can all help prevent die-shift[39]-[44]. Die size has a remarkably large impact71[45]. Nevertheless, the die shift and die protrusion (stand-off height) triggered by high die-placement load is a tradeoff [44]: they had attained a die shift of ±15μm at ±10μm die protrusion. Wafer warpages and all other process conditions,

particularly their temperatures, have an impact on the die shift as well [43]. According to Ling et al., 85% of die-shift is from thermal and mechanical (TM) effects such as Young's moduli and a CTE mismatch between the mold and carrier wafers, whereas the rest 15% is due to the FF such as shear force [47]. By lowering the mold compound thickness and carrier CTE, and increasing the die pitch and thickness, it is possible to reduce the TM-induced die shift [47]. However, by lowering the compression speed, mold curing temperature, preheating time, die pitch, inter-die space, and die thickness as well as raising the mold thickness, the die shift brought on by the FF effect may be minimized [47]. Additionally, studies on the effects of the properties of mold compounds (granular/liquid/sheet) on die-shift have been conducted, but they are quite complex [48][49].

Table 2-1 Thermomechanical and fluidic force effects on die shift described in previous

FOWLP works with rigid epoxy mold compounds.

	Thermo -Mechanical (TM) effect	Fluidic-Force (FF) effect
 Die-Shift increase	High compression speed [37] Large warpage [51] (large CTE mismatch between carrier wafers and mold) High curing temp. [39] High Young's modulus [43][44]* High CTE from r.t to T_g [42][43] Thick mold [39] ← → Thin mold [37] The outermost dies [38][49][52]	Thin [52]and small [53]dies High-density die pitch [37] Low placement load [54] Low adhesion between dies and adhesions/tapes [54] High viscosity mold [53] The outermost dies [38][49][52]
 Die-Shift decrease	Low compression speed [37] Small warpage [39] (small CTE mismatch between carrier wafers and mold) **Low curing temp. [39]*** **Low Young's modulus [43][44]*** **Low CTE (r.t. <T<T_g) [42][43]** Thin mold [37] ← → Thick mold [55] The central dies [38][49][52]	Thick [52]and large [53]dies Low-density die pitch [37] High placement load [54] High adhesion between dies and adhesions/tapes [54] Low viscosity mold [53] The central dies [38][49][52]

***PDMS is effective to reduce die shift**

I have created a structurally new FHE based on die-first/face-down FOWLP technology with dielets applying PDMS that possessed a low-Young's modulus like rubber and is curable at low temperatures even at room temperature. The die-shift assessment has been given by UCLA [50] where die shift was able to be lowered to 6 μm. As well as using a mask-less lithography approach to create small patterns on shifted dielets, they are also attempting to predict the die-shift using deep learning techniques. According to IMEC, a new temporary adhesive BrewerBOND® C1301 with a low Young's modulus, similar to PDMS, can lower die-shift [51]. To maintain component connectivity in Smart Skin Display, die shift must be limited below 10 μm.

2.2 Experimental

2.2.1 Structural design of multilayer wiring FHE based on stress-neutral axis

The interlayer dielectric used was SU-8. The interlayer dielectric film's thickness was chosen to place the stress-neutral axis in the middle of the two-layer wiring. When a bending force is applied to a material, it is neither pushed nor compressed at the stress-neutral axis. It is possible to reduce the load on the wire in each layer during bending by positioning the stress-neutral axis at the center of the two-layer wiring. The stress neutral axis was determined by the following equation.

$$\lambda = \frac{\sum_{i=1}^{n} E_i({h_i}^2 - {h_{i-1}}^2)}{2\sum_{i=1}^{n} E_i(h_i - h_{i-1})}$$

λ is the distance from the bottom to the stress-neutral axis, E is Young's modulus, and h is the distance from the bottom to the top of each layer. Fig. 2-7 displays an image of the stress-neutral axis. shows Young's modulus of each material. The thickness of SU-8 was determined using this formula to be approximately 4.12 μm, so the actual fabrication process targeted 4 μm for the deposition of SU-8. Since conventional polyimide flexible substrates have high Young's moduli around 3-4 GPa, such a stress-neutral axis control is challenging, and low-Young's-modulus PDMS can achieve the structural design.

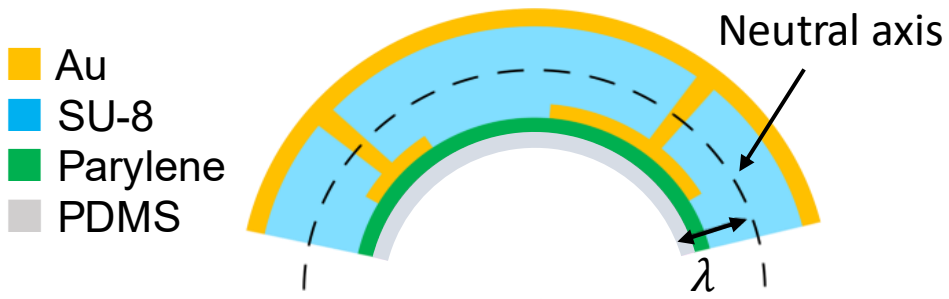

Fig. 2-7 Image of a neutral axis

Table 2-2 Young's modulus of each material in the multilayer wiring

Layer	Material	Young's modulus (GPa)	Thickness (μm)
Interlayer dielectric	Parylene	2.0	4.0
Wiring layer	Au	78	0.5
Stress buffer layer	Parylene	2.73	1
Substrate	PDMS	0.0005	500

2.2.2 Fabrication of multilayer FHE

The fabrication process of multilayer wiring is depicted in Fig. 2-8. A first handler was used to pour PDMS onto, and a second handler was used to sandwich it with, a high-temperature thermal release sheet that thermally foams at 200°C. After that, PDMS was cured at 70°C for 3 hours with a 360 g weight on it. The thickness of PDMS was 500 μm. The adhesion between PDMS and parylene was then increased with an excimer UV treatment following the removal of the initial handler. 1 μm thick parylene was deposited by vapor deposition as a stress buffer layer. The parylene surface was treated with excimer and spin-coated with an adhesion promoter to improve the adhesion between the parylene and the Ti/Au wire. The first layer of wire was created by photolithography and wet etching after which Ti 15 nm and Au 500 nm were coated by sputtering. 4 μm thick SU-8 was spin-coated as the interlayer dielectric. SU-8 is a constant

negative resist. The second layer of wiring was formed in the same way as the first layer. Finally, the PDMS was eventually peeled off from the second handler.

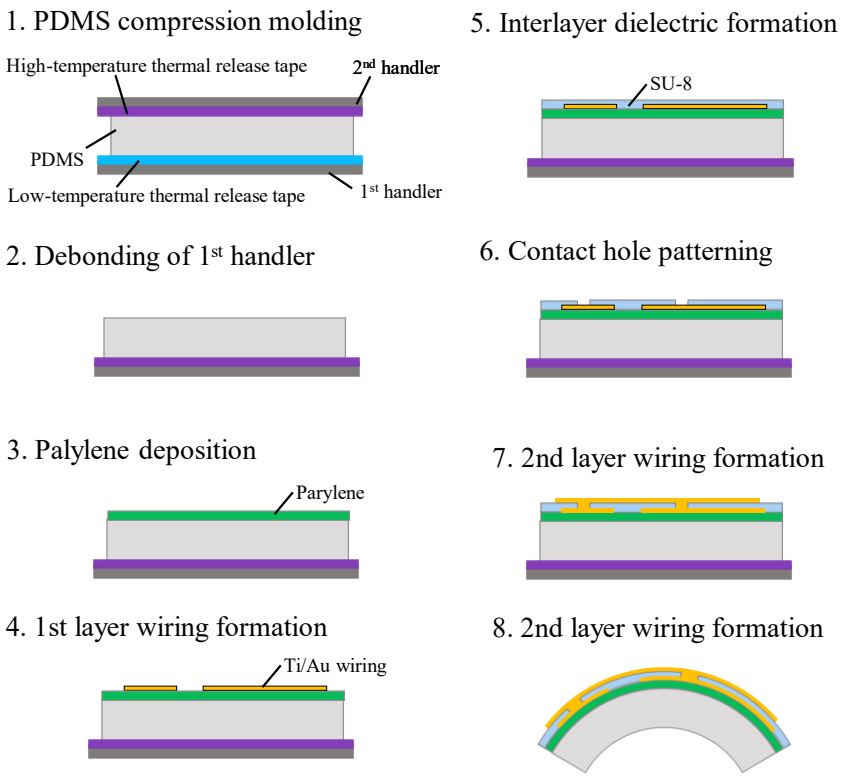

Fig. 2-8 Process flow of flexible multilayer wiring

2.2.3 Bending test of the flexible multilayer wiring

As seen in Fig. 2-9, and Fig. 2-10, repeated bending tests were performed by attaching the evaluation sample was fastened to a PET film and fixing the film to the bending test apparatus. The radius of curvature was set to 20 mm, assuming that the film would be attached to the arm. \depicts the actual repetitive bending test apparatus seen in Figure 3 3. The resistance of each wire was assessed using the four-terminal approach at 0, 1, 5, 10, 50, 100, 500, and 1000 bending cycles. To prevent the PET film from changing the location of the stress-neutral axis, the PET film just beneath the wiring was cut off for the test.

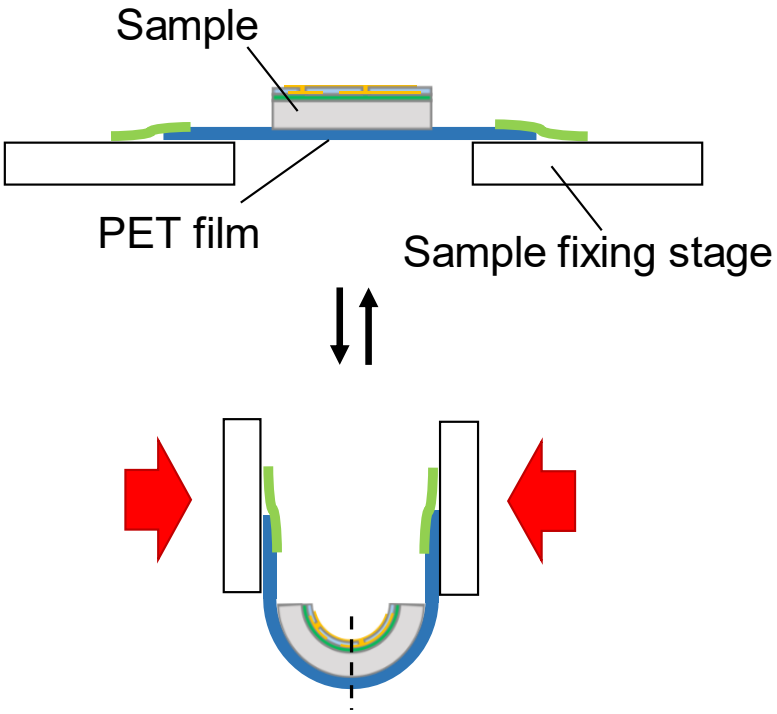

Fig. 2-9 Schematic diagram of repeated bending test

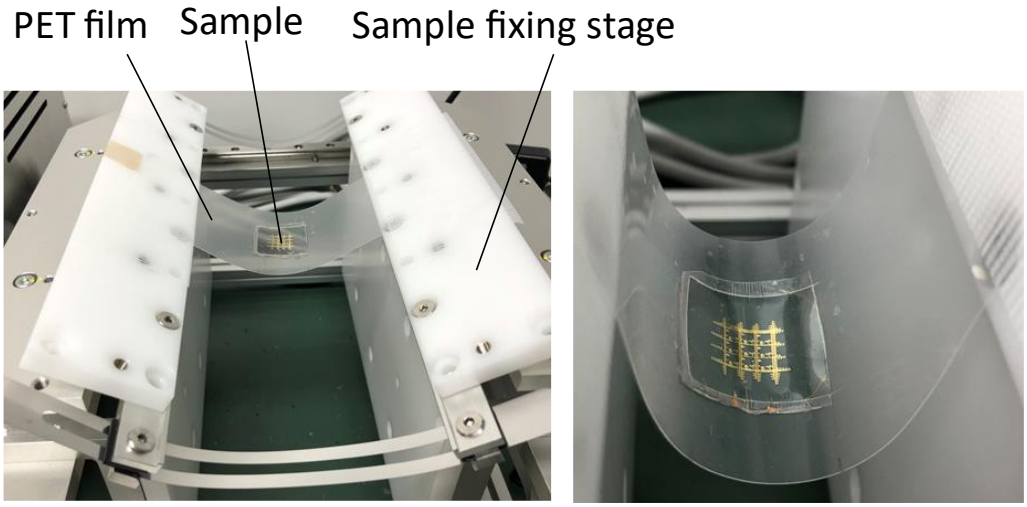

Fig. 2-10 Photo of repeated bending test

2.2.4 Passivation layer design

A cross-sectional schematic diagram of flexible wiring with a passivation layer is illustrated

in the figure. The surface barrier was made of biocompatible Parylene C. The thickness of the surface protective film was intended so that the position of the stress-neutral axis aligns with the center of the wiring, and the thickness was 7.3μm. summarizes the physical characteristics of each material used in the calculations and the cross-section of flexible wiring with a passivation layer is seen in Fig. 2-11.

Depicts the process flow of flexible wiring with passivation layer in Fig. 2-12. 1 mm square dummy Si chip is inserted PDMS, SBL is placed on PDMS, and metal wiring is created over the chip. The wiring width is 50 m, with three wires passing over four chips. The pitch of the interconnects is 300 μm, and the pitch of the chips is 1.8 mm. The chips are 50 microns thick, the PDMS is 500 μm, and the stress buffer layer is 1 μm. The stress buffer layer is made of Parylene. Parylene was deposited by vapor deposition.

Table 2-3 Young's modulus of each material in flexible wiring with the passivation layer

Layer	Material	Young's modulus (GPa)	Thickness (μm)
Passivation layer	Parylene	2.73	7.3
Wiring layer	Au	78	0.5
Stress buffer layer	Parylene	2.73	1
Substrate	PDMS	0.0005	500

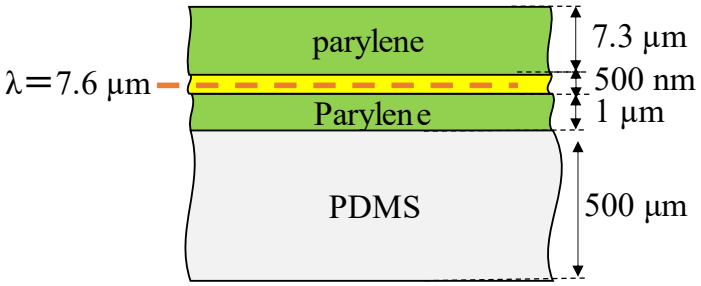

Fig. 2-11 Cross-section of flexible wiring with a passivation layer

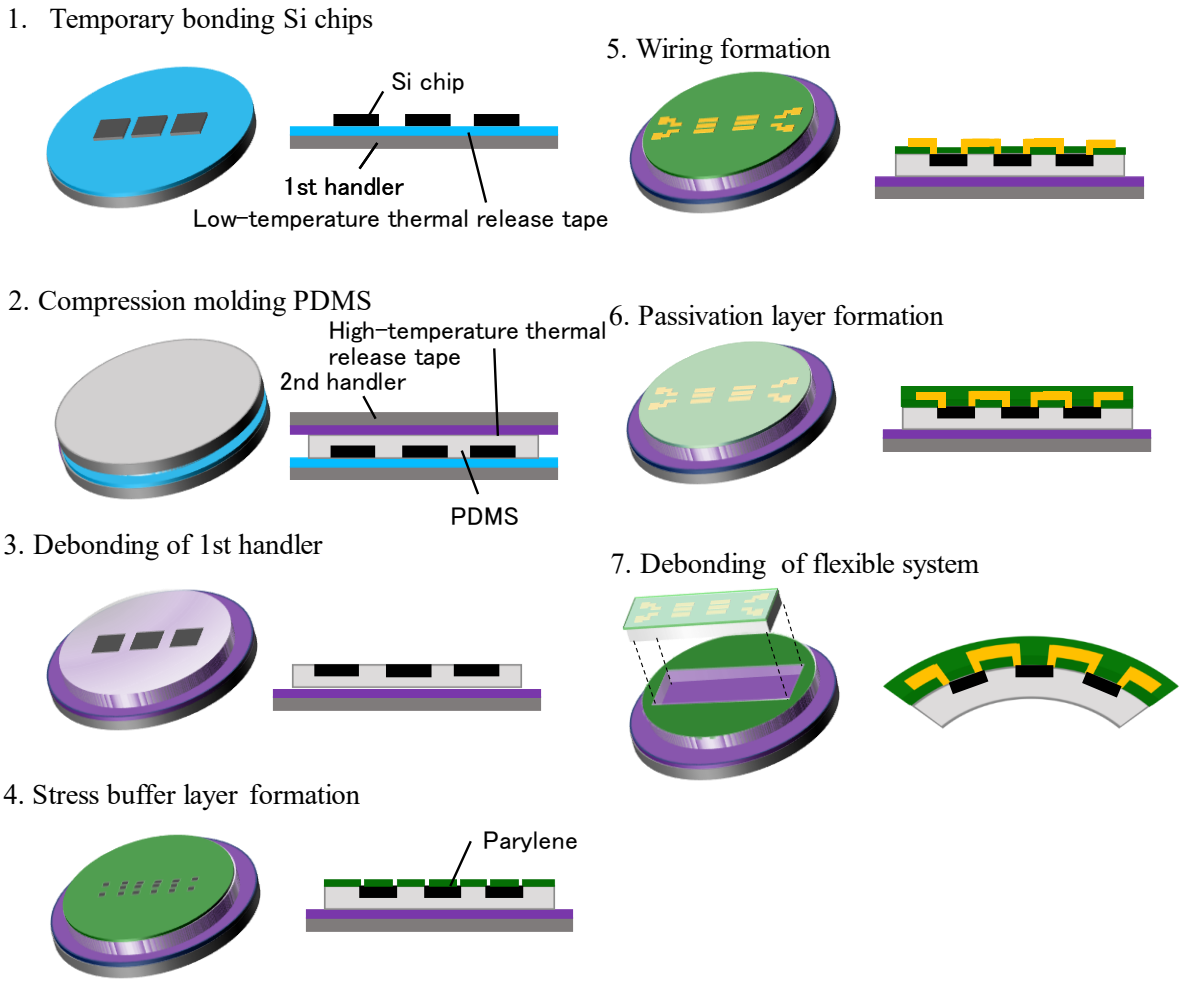

Fig. 2-12 Process flow of flexible wiring with a passivation layer

2.3 Evaluation of flexible multilayer wiring

A photograph of the multilayer wiring on PDMS is displayed in Fig. 2-13. On the first layer, wires were formed with widths of 30, 40, and 50 μm and on the second layer, wires with widths of 20, 30, and 50 μm were formed Fig. 2-14 shows a picture of the flexible multilayer wiring on a human arm may be seen. The flexible multilayer wiring has been bent along the curvature of the arm.

In addition, SU-8 serves not only as an interlayer dielectric but also to reduce the unevenness brought by the development of the first-layer interconnections. The degree of the first layer wiring before and after the SU-8 coating was measured using a surface profiler. Fig. 2-15 shows a cross-sectional view of the measurement and the measurement finding, it reveals that the first layer wiring was uneven by between 0.5 μm and 1.2 μm before the application of the SU-8 coating. After the SU-8 application, the unevenness is reduced to about 0.2 μm, and the flatness is significantly improved.

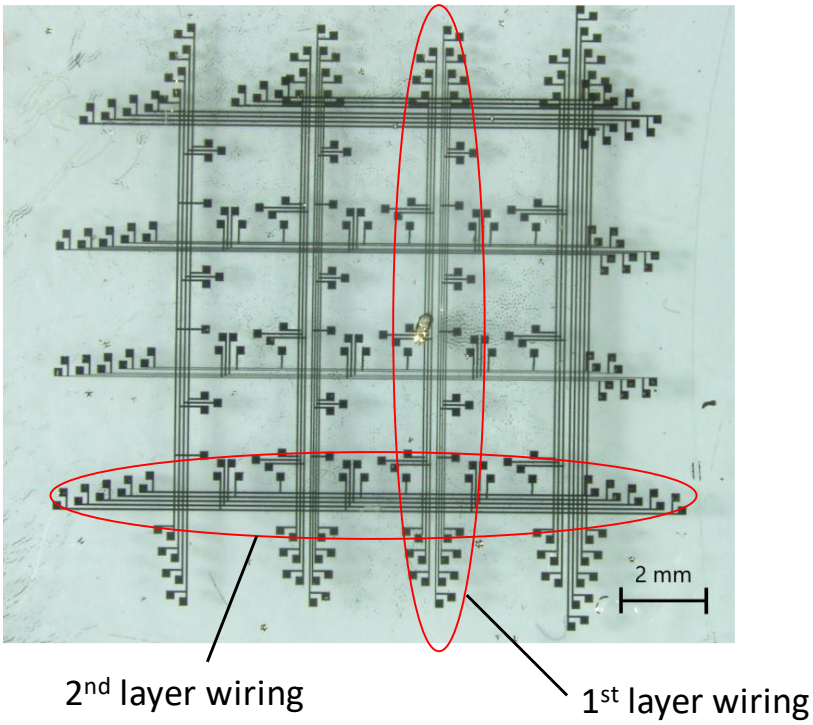

Fig. 2-13 A photo of the fabricated multilayer wirings on PDMS

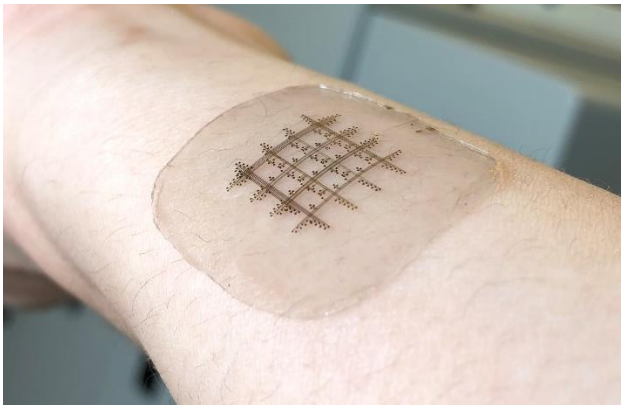

Fig. 2-14 Flexible multilayer wiring on a human arm

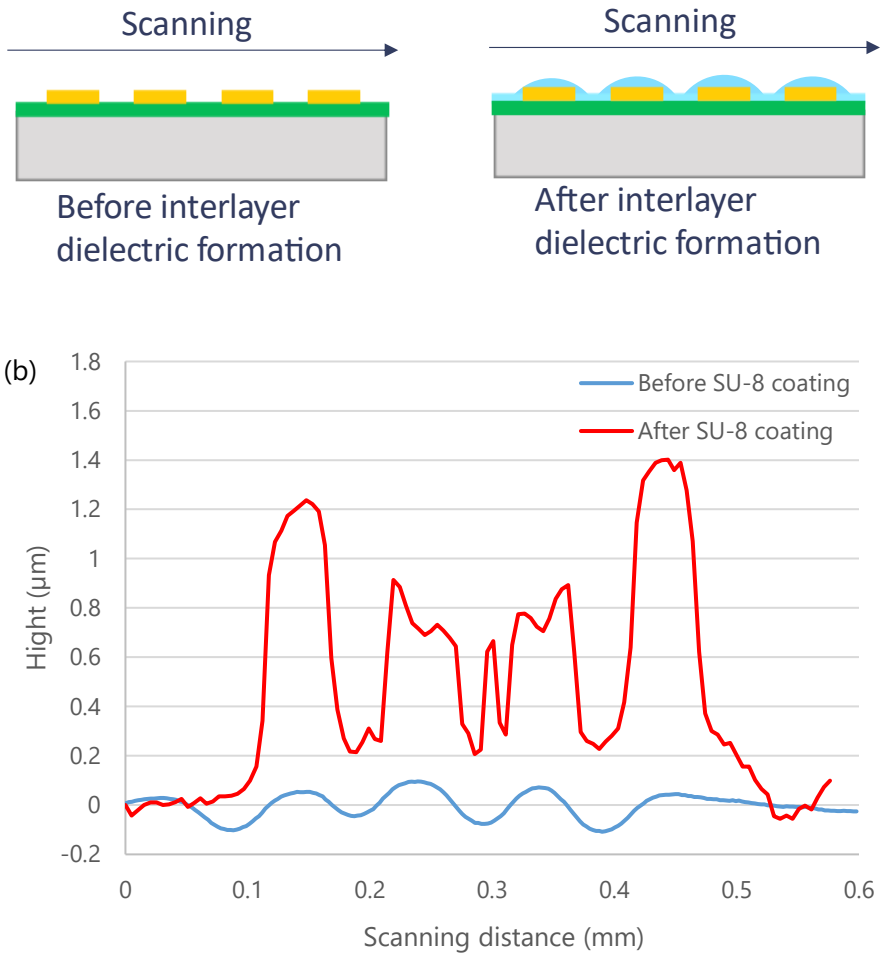

Fig. 2-15 Step height before and after SU-8 coating

Fig. 2-16 shows the outcomes of numerous bending tests of the two-layer wiring. No discernible change in resistance was found in any wiring after 1000 bending cycles. First-layer wiring displayed greater resistance values when compared to second-layer wiring of the same width. The wiring may have grown longer, locally formed thin wiring or microcracks. Depending on how the unevenness of the substrate, different metal thicknesses can be sputtered. Fig. 2-17 shows a cross-sectional schematic of the first layer wiring, and Fig. 2-18 the surface of the first and second layer wiring is shown. The second layer of wiring is formed without wrinkles, while

the first layer of wiring is wrinkled. However, the resistance of both the first and second layer wiring hardly changed Although the number of bending cycles was increased up to 1000 cycles, showing that the two-layer wiring manufactured this time has high flexibility and durability to repeated bending.

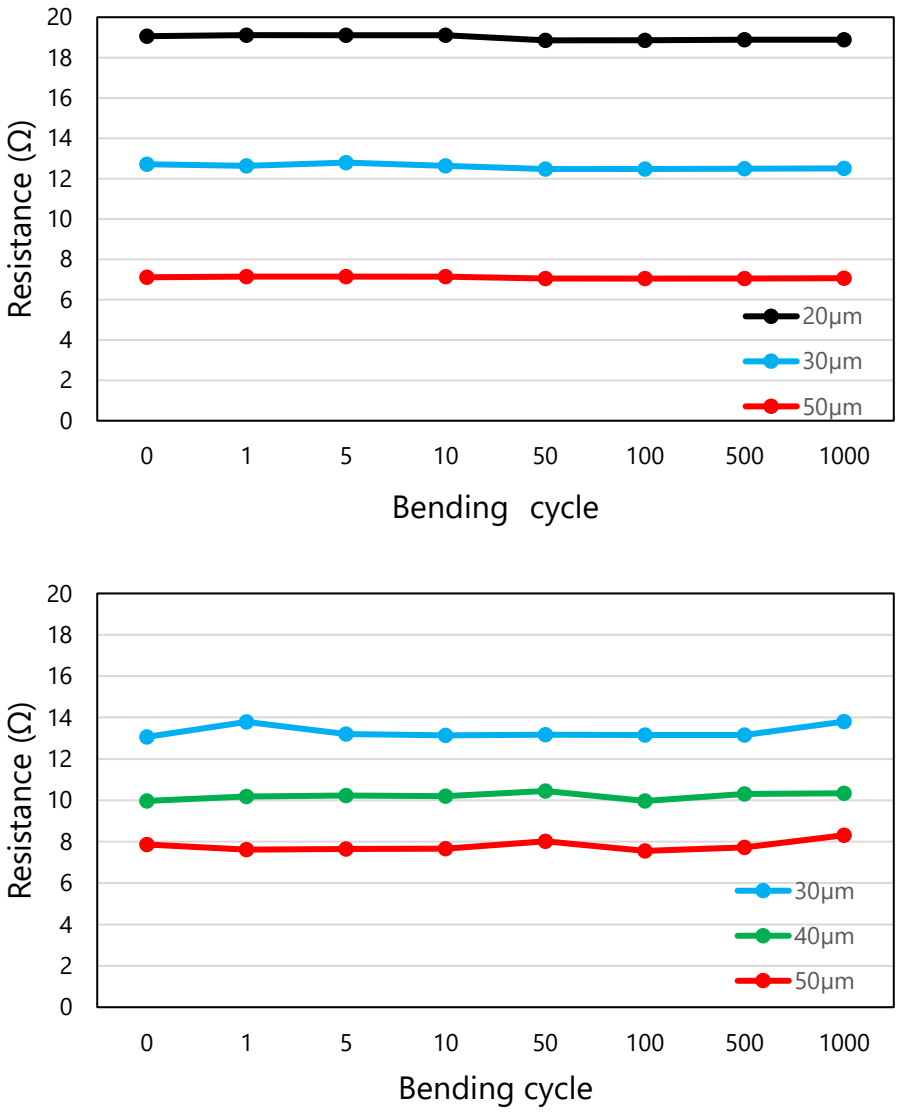

Fig. 2-16 Bending properties of first-layer wiring (upper) and second-layer wiring (lower).

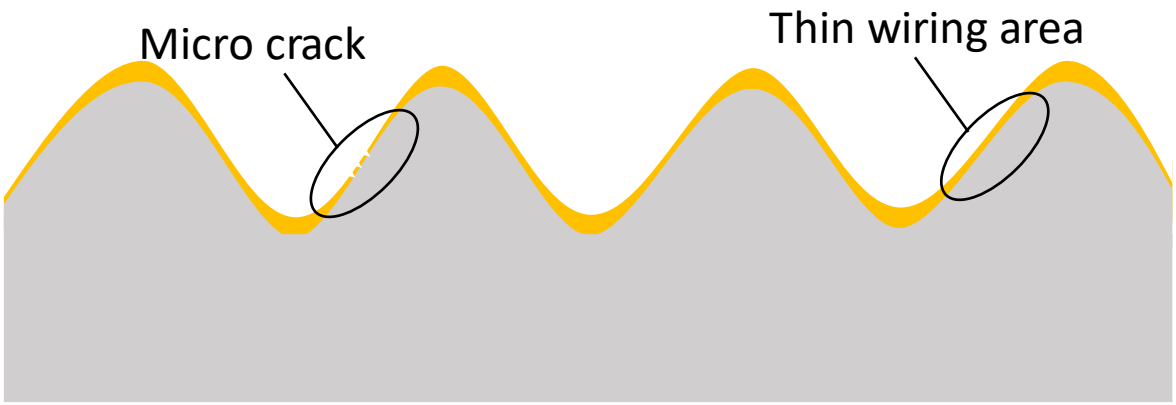

Fig. 2-17 Cross-sectional schematics of the first layer wiring

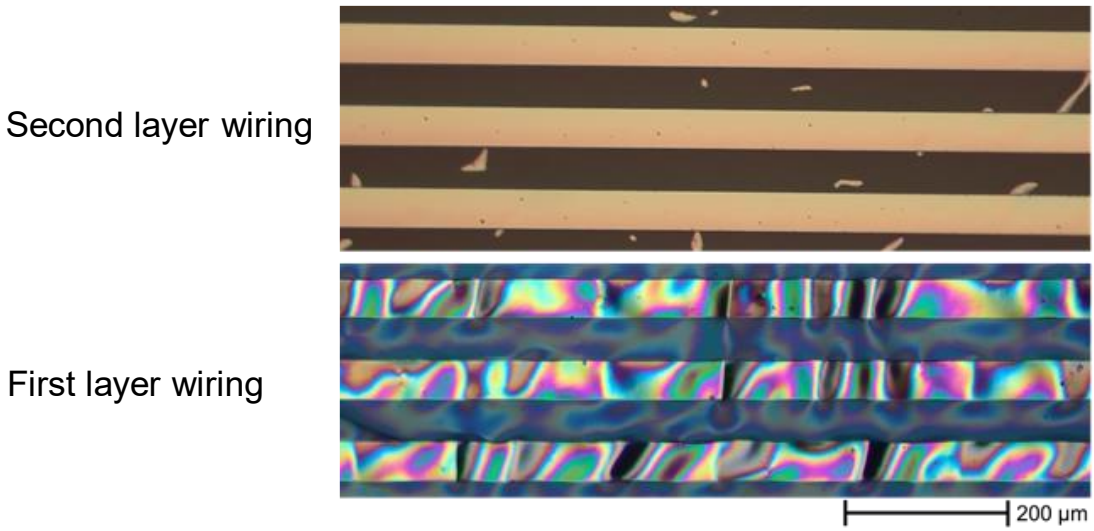

Fig. 2-18 Photo of first and second layer wiring

Contact holes were then created to connect the first and second layer wiring. A picture of the contact holes is displayed in Fig. 2-19. After repeated bending tests, the wiring resistance was determined using the 4-terminal measurement method. The radii of curvature used in the bending test were 10 mm, 5 mm, 2.5 mm, and 1 mm. The measured wiring's width was 40 m. Measurements were taken through two contact holes, as displayed in Fig. 2-20. The change in resistance at each bend radius is shown in Fig. 2-21. For curvature radii of 10 mm, 5 mm, and 2.5

mm, there was little difference in resistance after 1000 cycles of bending. Resistance increased at a radius of curvature of 1 mm, but the rate of increase stayed below 10% after 1000 cycles radius of curvature of 1mm was relatively small, in comparison to small parts of the body, such as fingertips, indicating that the constructed flexible multilayer wiring has extremely high mechanical durability.

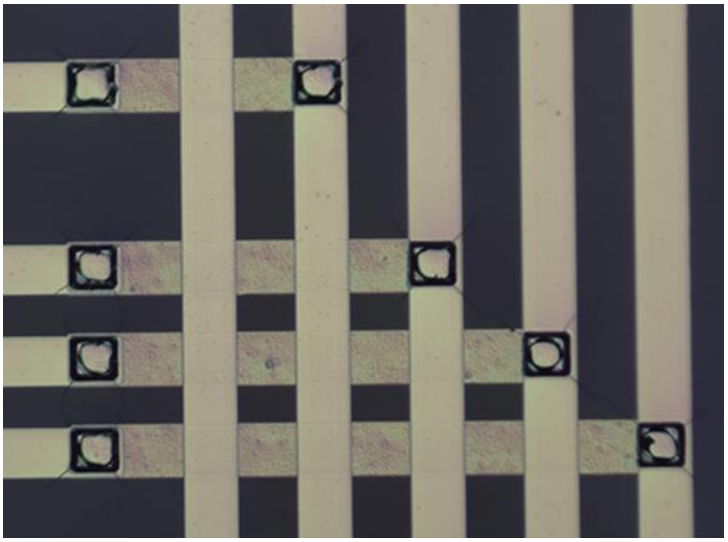

Fig. 2-19 Multilayer wiring with the contact hole

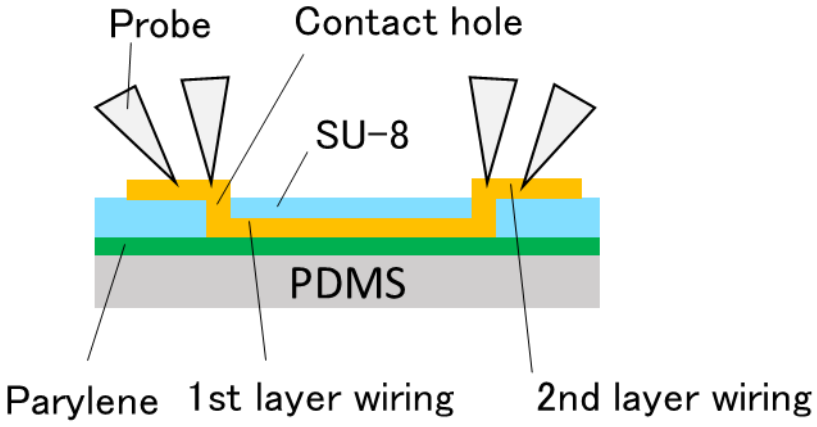

Fig. 2-20 Cross-section of electrical characterization with a flexible multilayer wiring

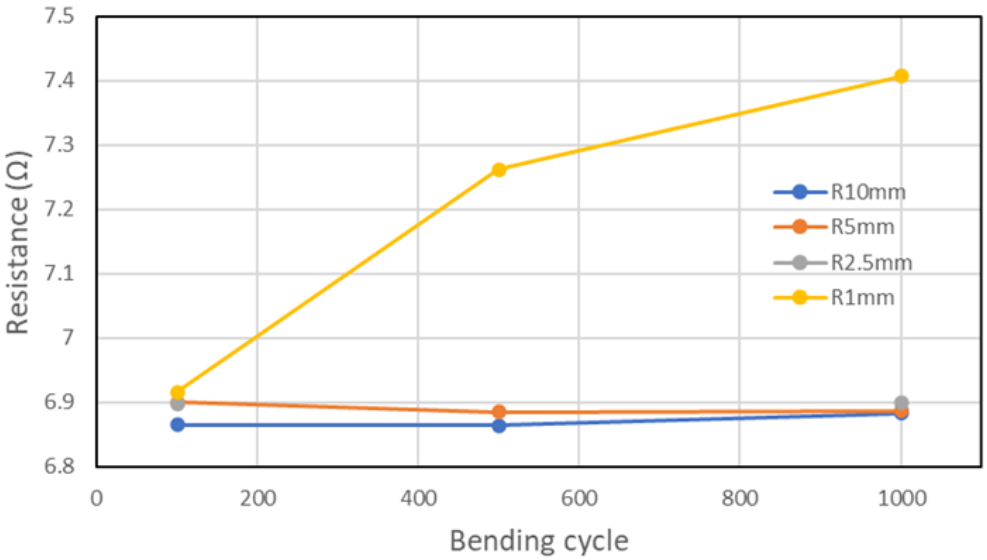

Fig. 2-21 Bending property of flexible multilayer wiring

2.4 Evaluation of Mechanical Durability of Flexible Wiring with a passivation layer

The stress buffer layer thickness was decided by the equation in the prior section. The actual fabricated sample is depicted in Fig. 2 25. The same procedure used to assess flexible multilayer wiring was used for numerous bending tests. A passivation layer was applied on one sample and not on the other. The sample without a passivation layer is structurally undesigned and does not follow the stress-neutral axis. The bending radius was 10 mm. Figure 3-8 shows the outcomes of the repeated bending test. After 1,000 cycles of bending tests with a surface protection film applied to the wiring, the wiring resistance remained unchanged, showing that the surface protection film increased the bending resistance. The passivation layer decreases the stress on the wires when bending by aligning the stress-neutral axis with the wires. Additionally, by protecting the wiring from above, the wiring is prevented from peeling off from the substrate, enabling the

fabrication of highly reliable flexible metal wiring.

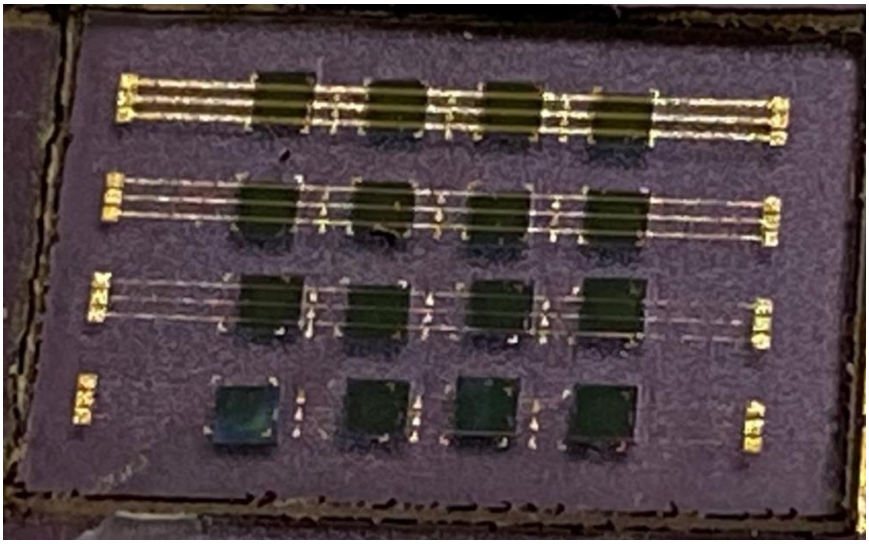

Fig. 2-22 Fabricated sample of flexible wiring with a passivation layer

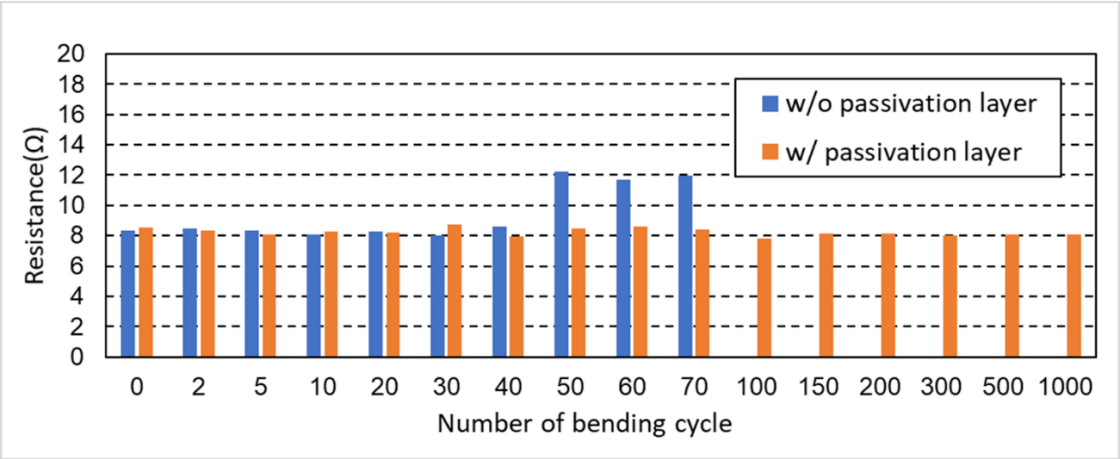

Fig. 2-23 Bending property of flexible wiring with a passivation layer

2.5 Anchoring layer

I use a vapor-deposited Parylene-C thin film as an anchoring layer to lower the die shift in Fig. 2-24. As seen in Fig. 2-25, in the absence of the anchor layer, the shift is more than 800 μm

along the sidewall of the LSI chip. Conversely, as depicted in Fig. 2-26 and Table 2-4, surprisingly, the die shift is significantly reduced even with the near-IR and red mini-LEDs in addition to a tiny capacitor by employing the anchoring layer. It is found that the die shift is decreased to less than 3 μm which is nearly 1/300 to mini-LEDs without the anchoring layer.

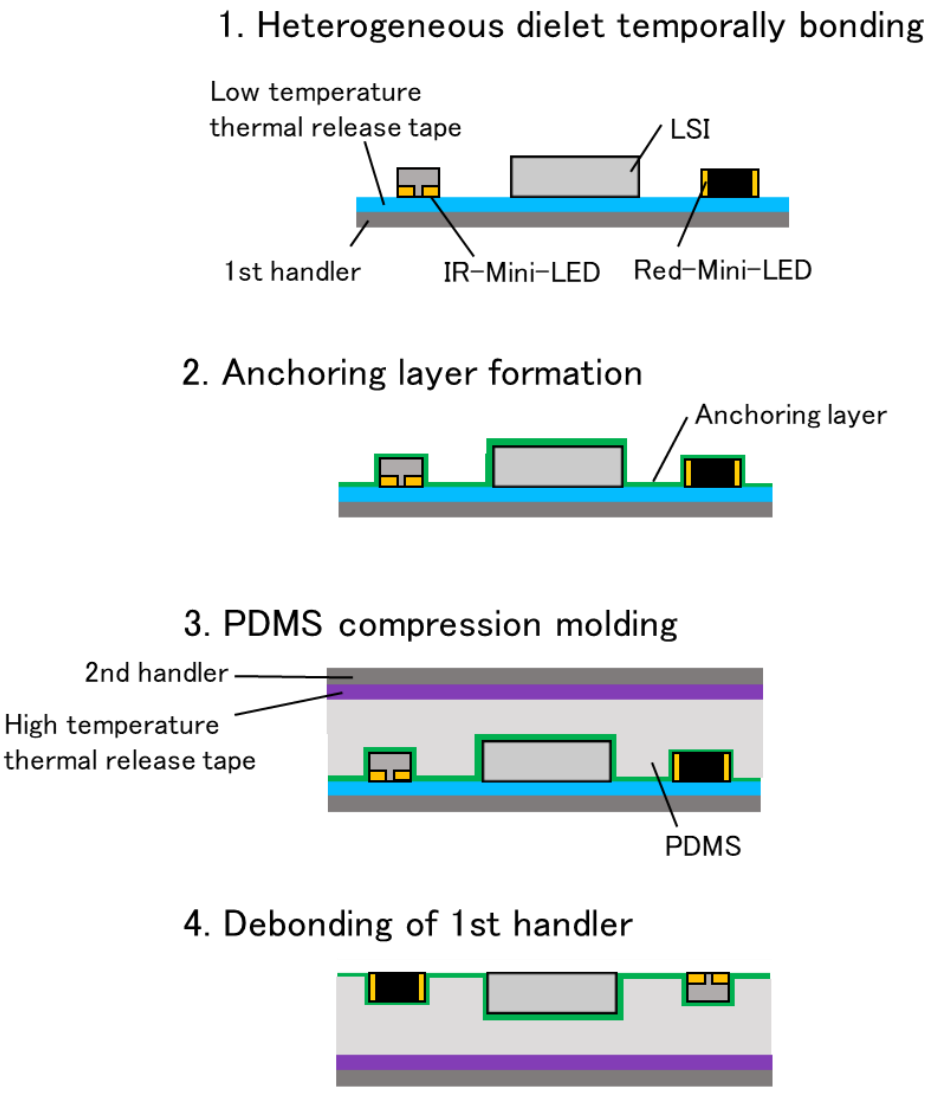

Fig. 2-24 Process flow of PDMS compression molding with anchoring layer

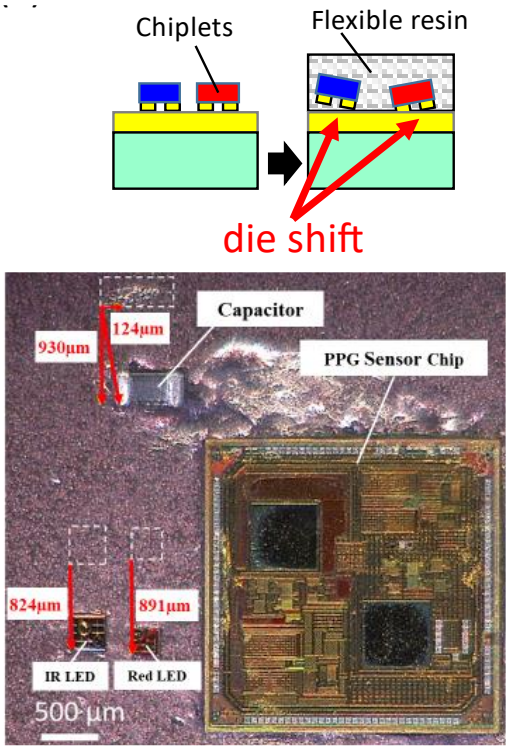

Fig. 2-25 Die shift without anchoring layer

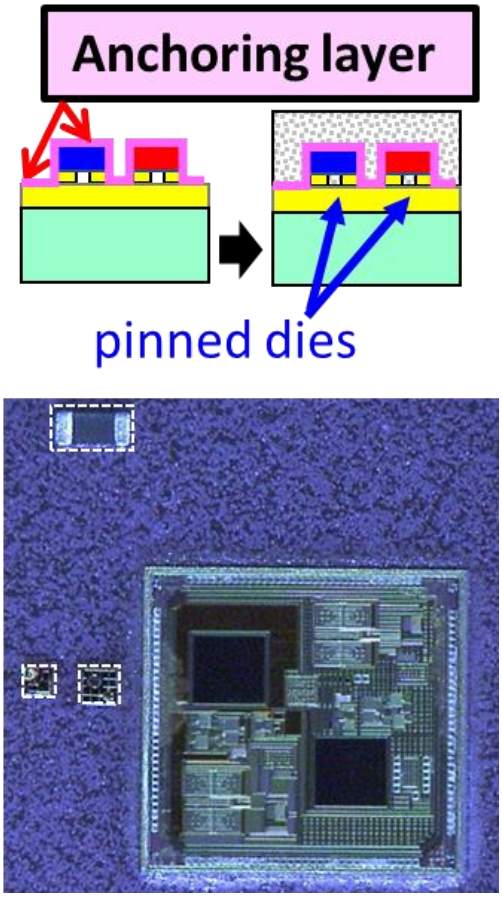

Fig. 2-26 Die shift reduction by anchoring layer

Table 2-4 Comparison of die shift without and with anchoring layer

Without anchoring layer

	Shift in X (μm)	Shift in Y (μm)	Rotation (°)
IR LED	824	34	1.4
Red LED	891	28	1.7

With anchoring layer

	Shift in X (μm)	Shift in Y (μm)	Rotation (°)
IR LED	0.7	0.4	0.1
Red LED	2.7	0.3	0.3

2.6 Conclusions

I worked on a solution for the die shift that causes alignment errors. In this research, I proposed an anchor layer as a technique to suppress die shift regardless of the type of dielet. By introducing

the anchor layer, the die shift of less than 10μm, which is required for the fabrication of Smart Skin Display, was obtained. A potential solution to the traditional die shift issue is the anchor layer, which is a scalable approach that can collectively suppress the die shift of various dielets of different sizes. To further enhance the performance of highly integrated FHE devices, I then focused on the fabrication of flexible multilayer interconnects. Flexible multilayer wiring was structurally designed based on the stress-neutral axis. With this design, the wiring was subjected to less strain, and the flexible multilayer wiring that was manufactured displayed remarkable endurance. The tremendously flexible multilayer interconnections used in this research will allow for the high-density integration of dielets with numerous terminals. This outcome significantly increases the potential of flexible devices.

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Chapter 3

Room-temperature electroplated direct bonding for 3D dielet-on-wafer heterogeneous integration

3.1 Introduction

I suggested Smart Skin Display and a healthcare FHE that included micro-LED and other dielets in Chapter 1. I will go over the stacking of micro-LED and 3D-ICs required to achieve Smart Skin Display in this chapter.

3.1.1 Micro-LED

Micro LED are being considered as a next-generation display since they have a number of advantages over traditional display technologies like liquid crystal displays (LCD) and organic light-emitting diodes (OLED) [1]-[3].

Table 3-1 provides a comparison of each display technology [5]: Voltage is used in LCDs to control the orientation of liquid crystal molecules. LCDs are non-luminescent displays and thus require a backlight. The liquid crystal layer allows the backlight's light to pass through and create an image. Because the orientation of the liquid crystal molecules affects their optical characteristics, the amount of light transmitted is controlled by applying a voltage to the orientation. Power consumption is significant because the backlight is always on when the display is in use. Additionally, even at the lowest levels of light transmission, light from the backlight is still marginally transferred, contributing to a low contrast ratio. Furthermore, the constrained direction of light emission caused by the liquid crystal molecules results in a small viewing angle. OLEDs, which have gained popularity recently, are self-emitting displays that emit light through the recombination of electrons and holes in the light-emitting layer made of organic semiconductors. Because they don't need a backlight, they feature a high contrast ratio and low power consumption. There are downsides, though, including burn-in after extended usage, difficulty in achieving ultrahigh resolution, and a short life span. The required resolution for each application is displayed in Table 3-2. Due to the proximity of a display to the user's eyes, VR/AR applications, which have recently gained popularity in the metaverse, are believed to need a resolution of 2000ppi or higher[6][7]. There have already been reports of micro-LED displays with resolutions higher than this [8]. Attention is being drawn to Micro-LED displays as potential contenders for next-generation displays that address the shortcomings of conventional displays. As illustrated in the figure, micro-LED displays, such as Sony's “Crystal LED”[9] and Samsung's “The Wall”[10] are now distributed mainly for business use. As observed in the figure, it is predicted that the production cost of displays will decline, and shipments of micro-LED displays will rise to nearly 16 million units by 2026[11]. Additionally, micro-LED are a promising technology with potential applications in visible light communication [12]-[14] and

optogenetics[15][16].

Table 3-1 Comparison of LCD, OLED, and micro-LED [5]

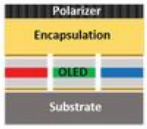
	LCD	OLED	Micro LED
			
Emission Type	Backlight/LED (thick)	Self-emissive (thin)	Self-emissive (thin)
Contrast Ratio	5000 : 1	∞	∞
Luminous Efficacy	Medium (~ 65 lm W^{-1})	Low (~ 20 lm W^{-1})	High (~ 100 lm W^{-1})
Brightness (cd/m^2)	3000	1500	100,000
Life Span	5 ~ 8 years	~ 4 years	> 10 years
Response Time	5 ms	110 μs	~ 0.2 ns
Operating Temperature (°C)	0 ~ 60	-50 ~ 70	-100 ~ 120
Color Rendering	75% NTSC	> 100% NTSC	140% NTSC
Viewing Angle	Poor (~ 100 °)	Best (~ 140 °)	Best (~ 140 °)
Power Consumption (320×320 pixels, 350 cd/m^2)	3.1 W	200 mW	40 mW
Remarks	Afterimage	Burn-in image, Unstable (heat, humidity)	Stable (heat, humidity)

Table 3-2 Comparison of micro-LED application requirements [7].

	High PPI		Low PPI		
Application	AR/MR/VR/Projector	Vehicles	Wearables/Smartphones	Laptop	TV
PPI	>2000	>150	>350	>250	>100
Chip size (um)	<5	<100	<30	<30	20–80
Brightness (nits)	>5000	>5000	>1000	>500	>500
Contrast Ratio	>100 000:1	>100 000:1	>100 000:1	>100 000:1	>10 000:1

Fig. 3-1 Commercially available micro-LED display by Sony (upper)[9] and Samsung (lower) [10]

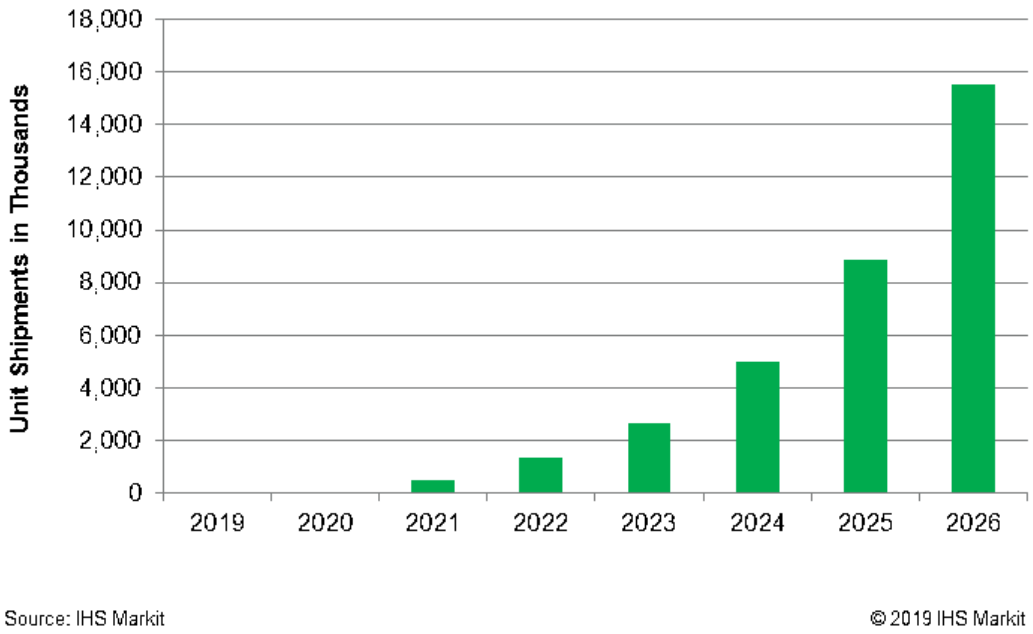


Fig. 3-2 Global micro-LED market shipment forecast [11].

3.1.2 Manufacturing Technology of micro-LED display

The first micro-LED display was realized in 2009. Since then, various technological improvements have been made [17]. The production technology for widely used micro-LED screens is described in this section.

When the size of the display is small, LED can be mounted one at a time by flip-chip bonding. Conventional flip-chip technology has an assembly throughput of 8,000 units per hour[18]. At this rate, it would take several months to produce an 8K display with nearly 40 million pixels. Consequently, micro-LED must be placed in enormous quantities and with great precision to be used as individual pixels on screens bigger than 2 inches [19].

The most common mass transfer is called elastomer stamping or transfer stamping [20]-[22], in which a micro LED is bonded to an adhesive elastomer and transferred to another substrate, as shown in the figure. According to Fig. 3-3 and Fig. 3-4 and , roll transfer is a technique for continually mounting driving circuits and micro-LEDs. Laser release is a method that can selectively mount micro

LED transferred on a laser release sheet as shown in Fig. 3-5. Another method is self-assembly [25][26], which assembles micro-LED in a self-aligning way by using the surface tension of the droplet. So far, no mass transfer technology has emerged that is fast enough for the mass production of micro-LED displays, but this field is being actively researched, and it is expected that an efficient and cost-effective technology will emerge soon.

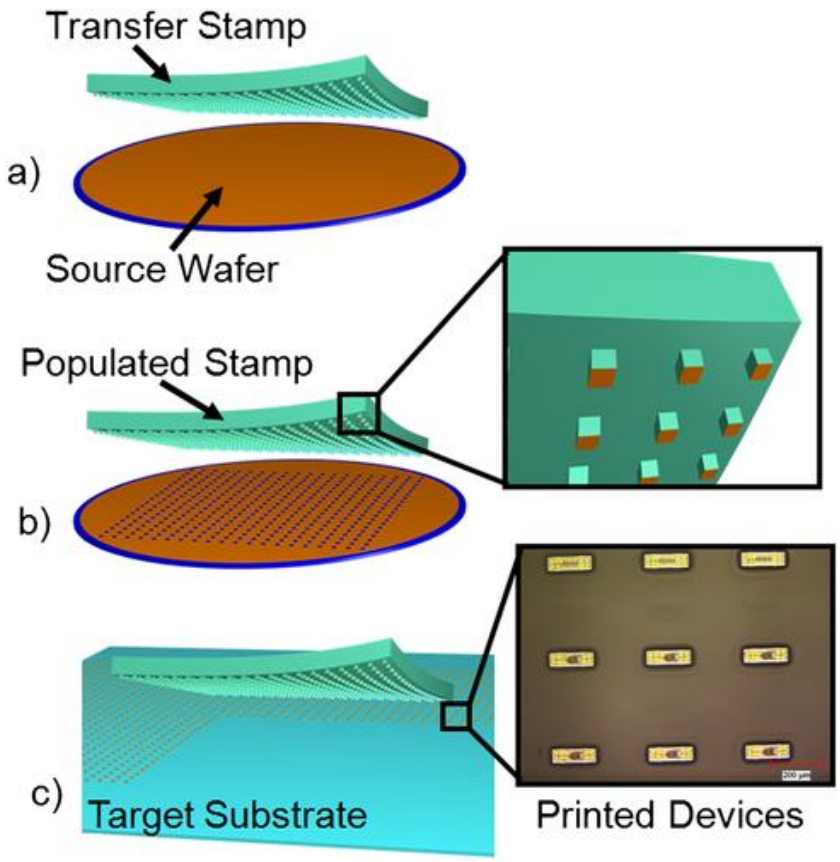


Fig. 3-3 Transfer stamping process [20]

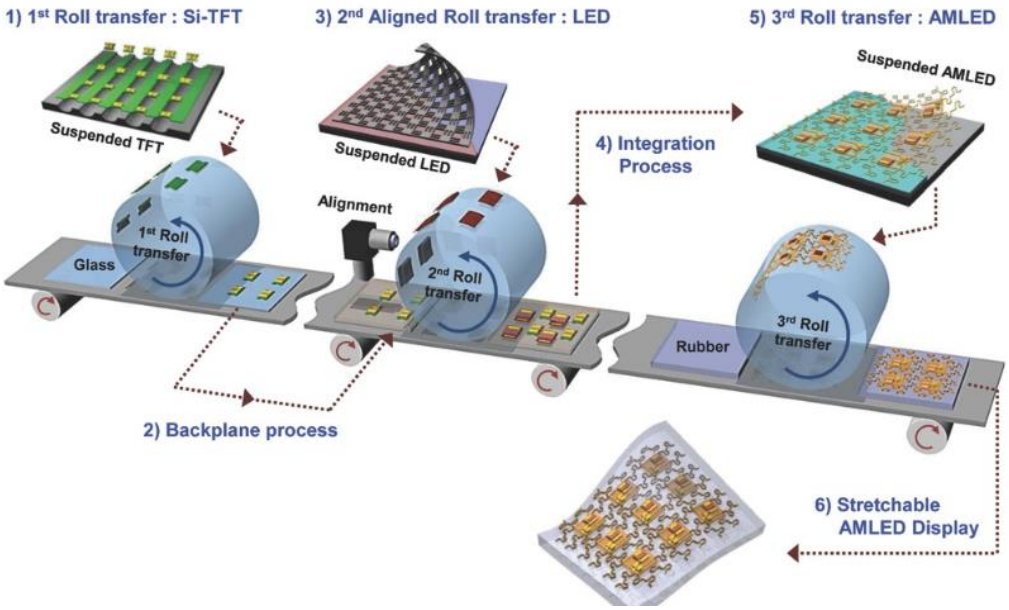


Fig. 3-4 Roll transfer process [23]

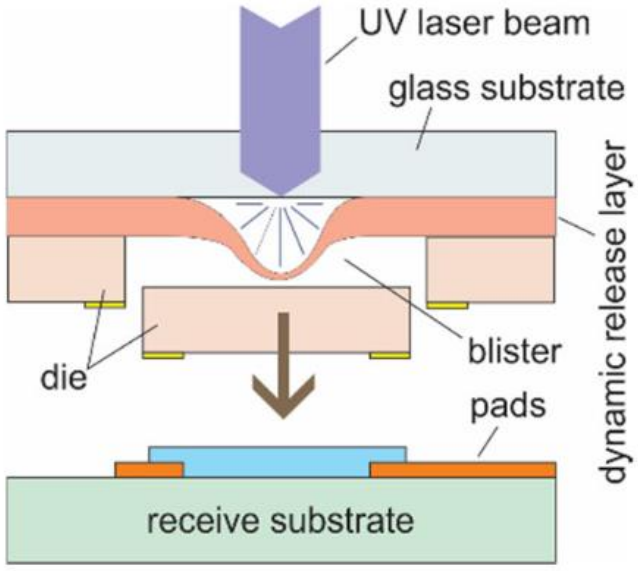


Fig. 3-5 Laser transfer process [24]

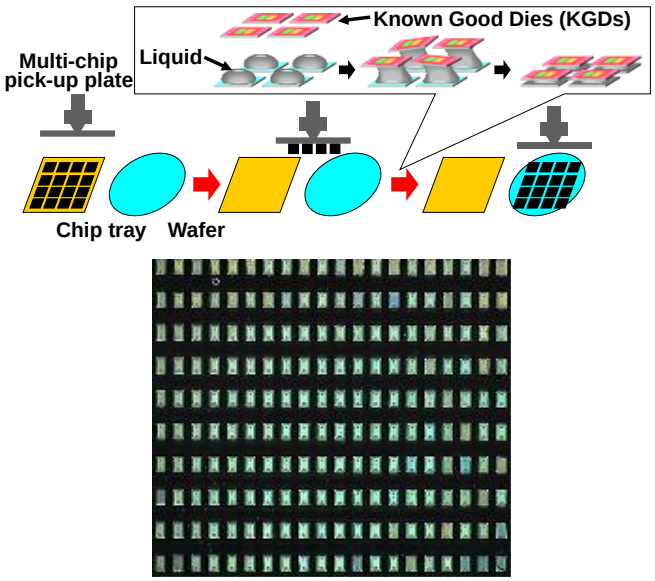


Fig. 3-6 Blue micro-LED chips (75 μm by 125 μm) self-assembled in batches by liquid surface tension.

Then, a description of micro LED connecting technology follows. In general, micro bumps are frequently used for micro LED connectivity [27]-[31]. Microbumps are fine metal bumps with a diameter of 50 μm or less. The figure displays thermocompression flip-chip bonding with tiny bumps. Common micro bumps are thermos compressed at 250 °C or more, above the melting point, and use materials containing Sn. Low-melting solder has also been proposed, and this is thermo-compressed at about 150 °C[33]. Anisotropic conductive film/paste (ACF/ACP)[34][35], which is a film containing conductive particles in resin and may simultaneously fulfill the three tasks of adhesion, conduction, and insulation, is another method of bonding that is available. When a micro LED is thermocompression bonded, conductive particles are sandwiched between the electrodes facing each other, and the electrodes are electrically connected, but electricity does not perform laterally.

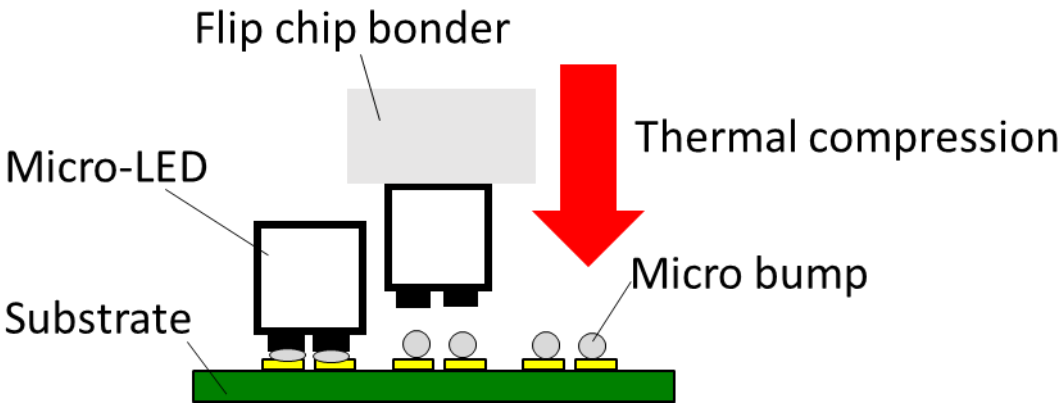


Fig. 3-7 Schematic diagram of micro-LED bonding with a micro bump

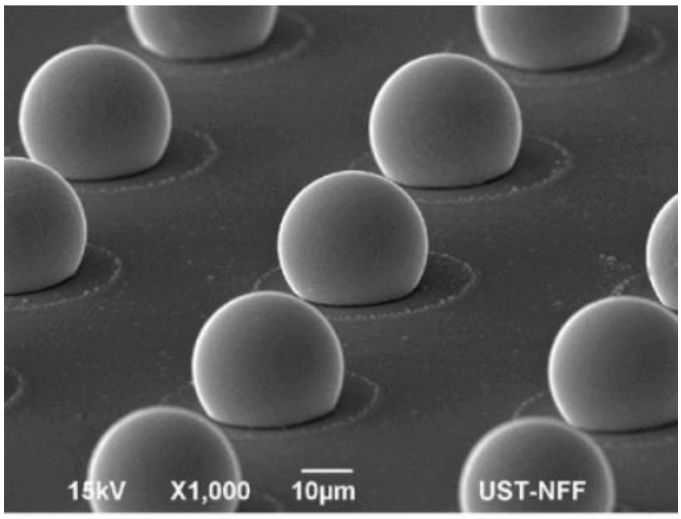


Fig. 3-8 SEM image of micro bumps [32]

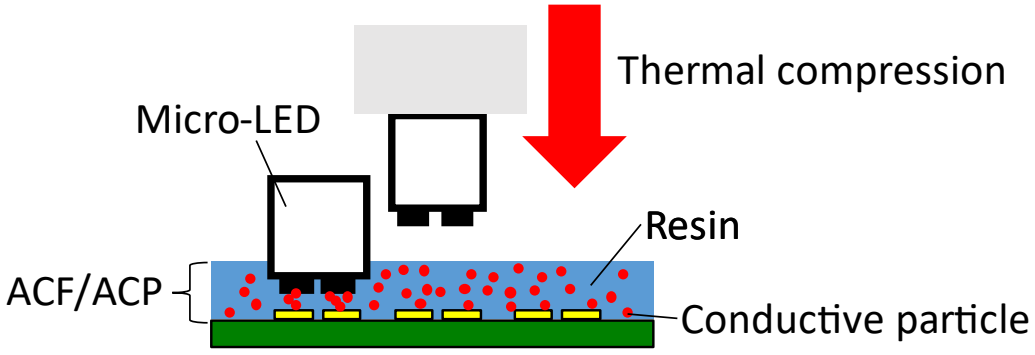


Fig. 3-9 Schematic diagram of micro-LED bonding with ACF/ACP

3.1.3 Direct bonding

Micro bumps have been used for 3D-IC bonding. However, due to solder bridging, sidewall wettability, electromigration (EM), and brittle intermetallic compound (IMC) formation, the micro bump has not been possible to miniaturize the pitch to less than 10μm [36]-0. As a result, direct Cu-to-Cu bonding is currently being extensively researched as a way to achieve further downsizing. Cu-to-Cu bonding can be done in two different ways. One is Cu–Cu thermal compression bonding 0-[43]. The basic mechanism of Cu–Cu thermocompression bonding is the interdiffusion of Cu atoms and grain growth at the bonding interface due to the simultaneous application of temperature and pressure [44]. Fig. 3 10 [45] depicts the Cu–Cu thermal compression bonding process flow. Cu is thermo-compressed by facing each other while being connected by a damascene process. The bonded Cu interface is shown in Fig. 3-11. High temperatures of 300 °C or higher are typically required for thermocompression bonding of successive Cu layers [46][47]. However, warpage occurs at high temperatures as a result of the materials' mismatched thermal expansion coefficients, which reduces coplanarity [48]. As a result, lower temperatures are also desirable to reduce 3D-IC alignment errors [49]. The other approach is hybrid bonding [50][51]. Dielectric-dielectric bonding and metal-metal bonding, such as Cu–Cu, are combined in hybrid bonding. Either annealing to bond Cu after dielectric bonding at ambient temperature or concurrently bonding dielectric and metal can be used for hybrid bonding. The former has higher throughput and is more actively studied. A schematic diagram of hybrid joining is shown in Fig. 3-12. Hybrid joining has the following advantages over thermal compression bonding [53]. (1) Hybrid bonding uses the difference in thermal expansion coefficient between metal and dielectric. It is a scalable bonding technique because this pressure is independent of the huge size. (2) Dielectric bonding is performed at room temperature, minimizing metal oxidation. (3) Tacking, which temporarily fixes the die, can be done in a batch

process. (4) Alignment errors are decreased by the process at room temperature. The thermocompression bonding and hybrid bonding are contrasted in Table 3-3 [53]. Hybrid bonding is already in practical use in the mass production of CMOS image sensors in the W2W process [54]0. Hybrid bonding requires high coplanarity and cleanliness 0. As a result, W2W is easier for hybrid bonding than C2W, which is more likely to generate particles during dicing. However, due to its high density and propensity for hetero-integration, C2W hybrid bonding is particularly appealing. It has been actively studied as a topic that has attracted the most attention in the semiconductor packaging field in recent years [57]-[72]. Hybrid bonding, however, necessitates considerable planarity, rendering it inappropriate for bonding diced micro-LEDs.

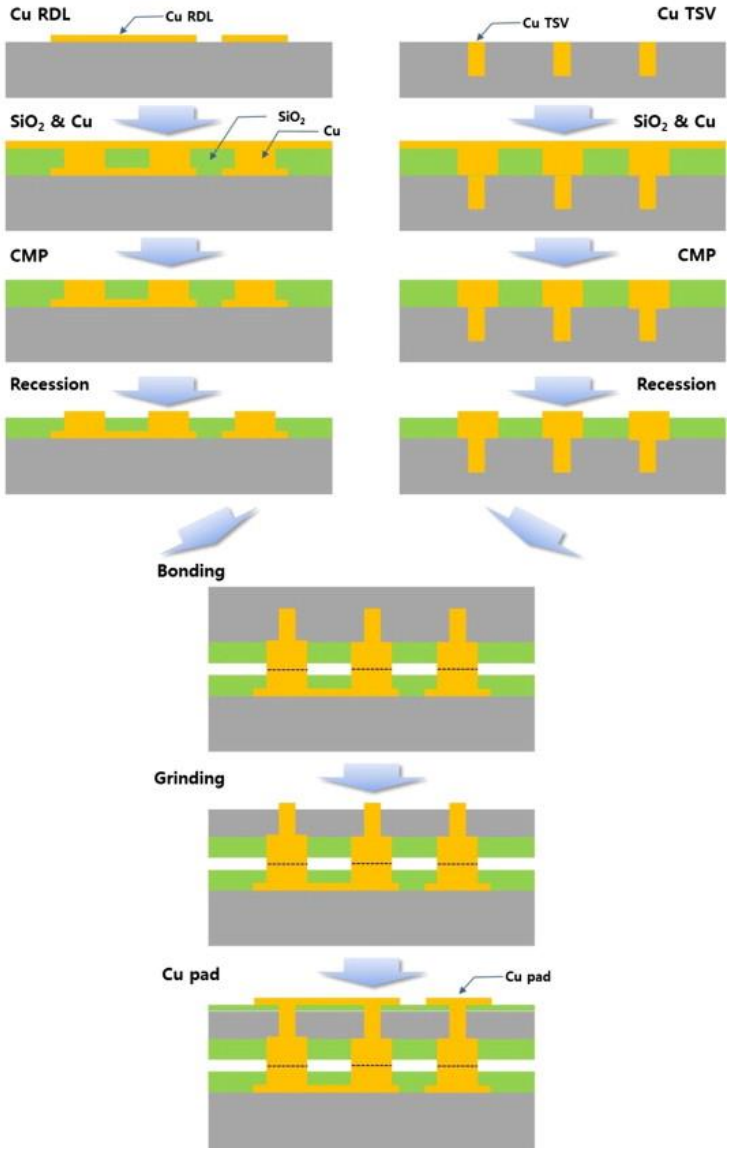


Fig. 3-10 Process flow of Cu–Cu thermal compression bonding [45].

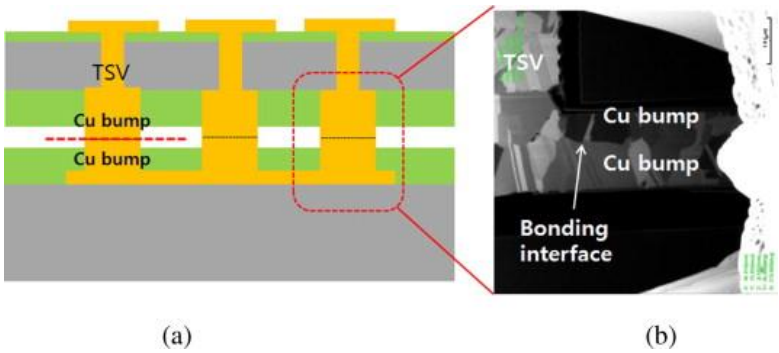


Fig. 3-11 (a) schematic of wafer level stacking (b) FIB image of bonding interface [45].

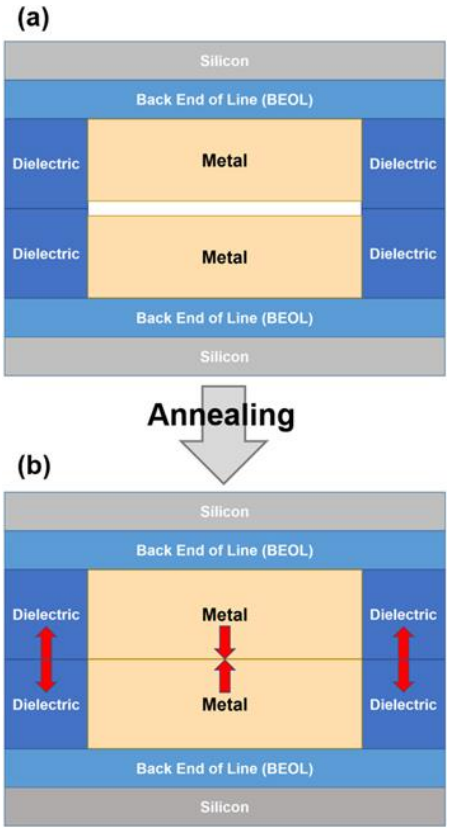


Fig. 3-12 Schematic of hybrid bonding [53]

Table 3-3 Comparison of thermal compression bonding (TCB) and room temperature hybrid bonding (HB) [53]

	TCB	Room temperature HB
Pressure for metal–metal bonding	External pressure from machine motor	Internal pressure from metal thermal expansion; independent of die size
Encapsulation and passivation	Passivation required	Encapsulation is naturally formed
Throughput	Low	High
Alignment	Thermal gradients make accurate alignment difficult	Room temperature tacking makes alignment more accurate

3.1.4 Room-temperature bonding

In this chapter, a micro-LED and an LSI with an LED driver are coaxially stacked in a dielet. Such a structure in a 3D-IC is novel and represents an advanced strategy. Furthermore, by integrating 3D-IC dielets into flexible substrates using FHE technology in this study, which embeds hard chiplets into soft substrates, it is possible to fabricate flexible and multifunctional micro-LED displays. The majority of traditional micro-LED bonding techniques, including micro-bumping and ACF/ACP, are carried out on thick substrates. Vertical cracks, which are generally caused by heat, are one of the main causes of the failure of 3D-ICs [73]. Point loading on thin 3D-ICs raises the risk of cracking as well. The 3D-IC is especially susceptible to chipping or microcracking during the dicing and thinning process [74]- [76], as shown in Fig. 3-13.

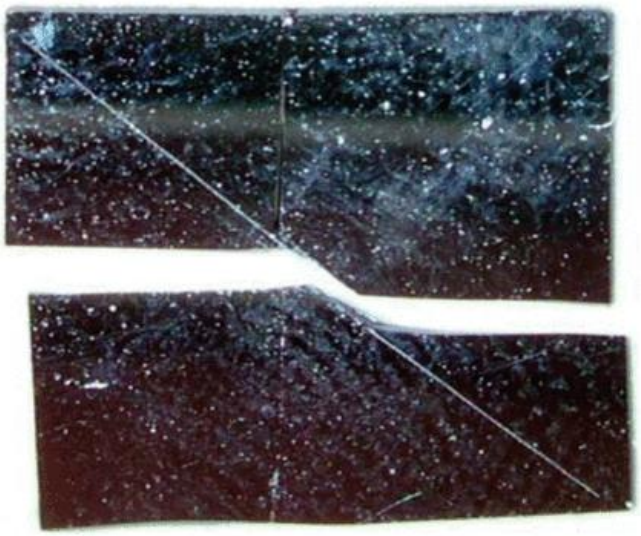


Fig. 3-13 Typical failure modes of thin Si die [76]

Typically, metal bumps are composed of multiple metals. As a result, the thermal gradient of the TCB results in a concentration gradient of the alloy due to the Soret effect [77]. After reaching room temperature, the bumps are still subject to residual pressures caused by this concentration differential. Heat-induced residual stress during bonding encourages electromigration (EM) [78]. EM is a critical reliability issue in solder joints[79]-[82]. Furthermore, cracking is a concern in 3D-ICs with TSVs due to the difference in thermal expansion coefficient (CTE)[83]-[85]. Therefore, the purpose of this effort is to provide a room-temperature bonding technology for micro-LEDs and 3D-ICs.

CEA LETI has proposed a fine-pitch room temperature bonding method [86][87]. In this method, a metal cylinder is bonded to a bump by mating the bumps with the cylinder. However, this approach needs chemical mechanical polishing (CMP). As seen in Fig. 3 15, NanoWired has devised a room-temperature bonding technique that involves crimping together nanowires that have been placed on a chip[88]. However, nanowire deposition requires specialized equipment and is challenging to apply to diced chips.

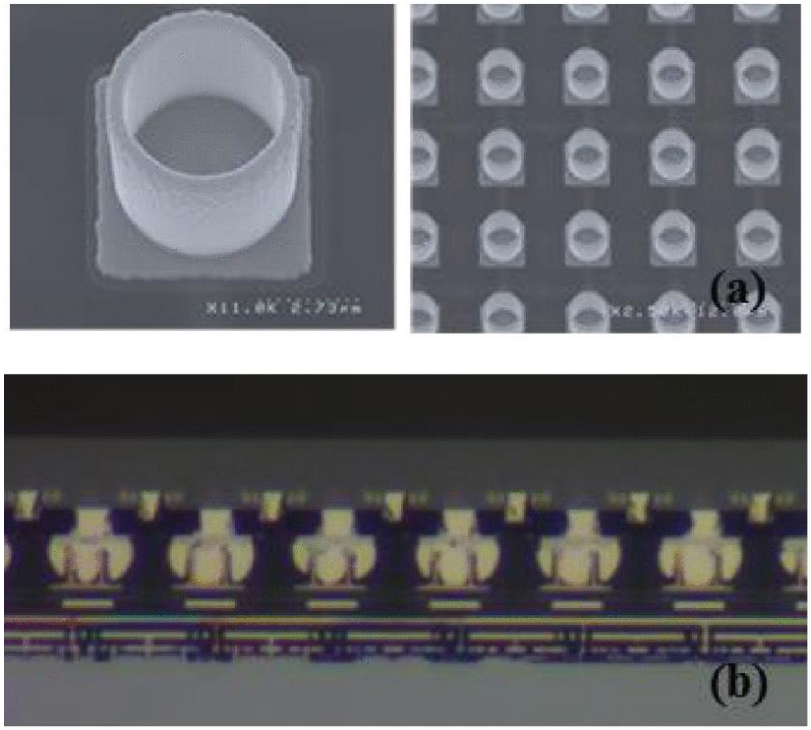


Fig. 3-14 Microtube for fine-pitch bonding at room temperature [87].

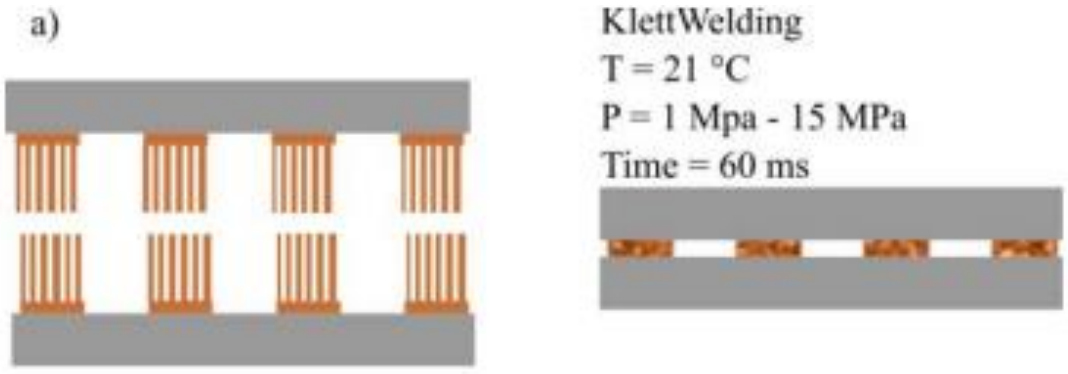


Fig. 3-15 Room-temperature bonding technology using nanowires.

This chapter aims to create new room-temperature junctions applicable to 3D-ICs and micro-LEDs to fabricate Smart Skin Display. For the bonded micro-LEDs, the objective is to reach a

99% electroluminescence yield.

3.2 Experimental

3.2.1 Electroplated Cu direct bonding

This study suggests an electroplated Cu direct bonding method for room-temperature bonding of micro LEDs. Fig. 3-16 depicts a micrograph of a micro-LED. The micro-LED are 100 μm cubes. The process flow for room-temperature Cu direct bonding of micro-LEDs is depicted in Fig 3.17. The micro-LED were attached to metal wiring made on a sapphire substrate in place of 3D-IC. First, Au wiring was formed on the substrate by sputtering and photolithography, Ti/Cu was deposited by sputtering as a barrier/seed layer, and then the photosensitive resin was spin-coated to open the Cu plating growth area by photolithography. Fig. 3-18 depicts the micro-LED arrangement and aperture pattern. The micro-LED is positioned with Smart Skin Display in mind. The micro-LED are arranged in a 6 x 6 arrangement with a pitch of 300um as one unit, and the units are placed in 5 x 5 units with a pitch of 1600 μm. The size of the aperture is 67 μm x 67 μm. The photosensitive resin also serves as a temporary bonding layer to fix the micro-LED. 30 x 30 arrays of micro-LED were temporarily bonded at room temperature. The micro-LED electrodes with the wiring on the substrate were then electroplated with Cu, which grew as a result. The barrier/seed layer was then etched once the photosensitive resin was removed.

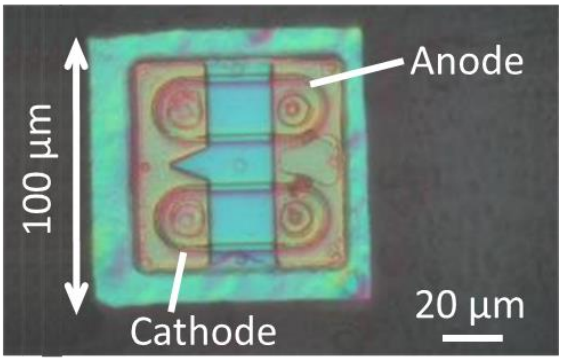


Fig. 3-16 100µm cubic micro-LED

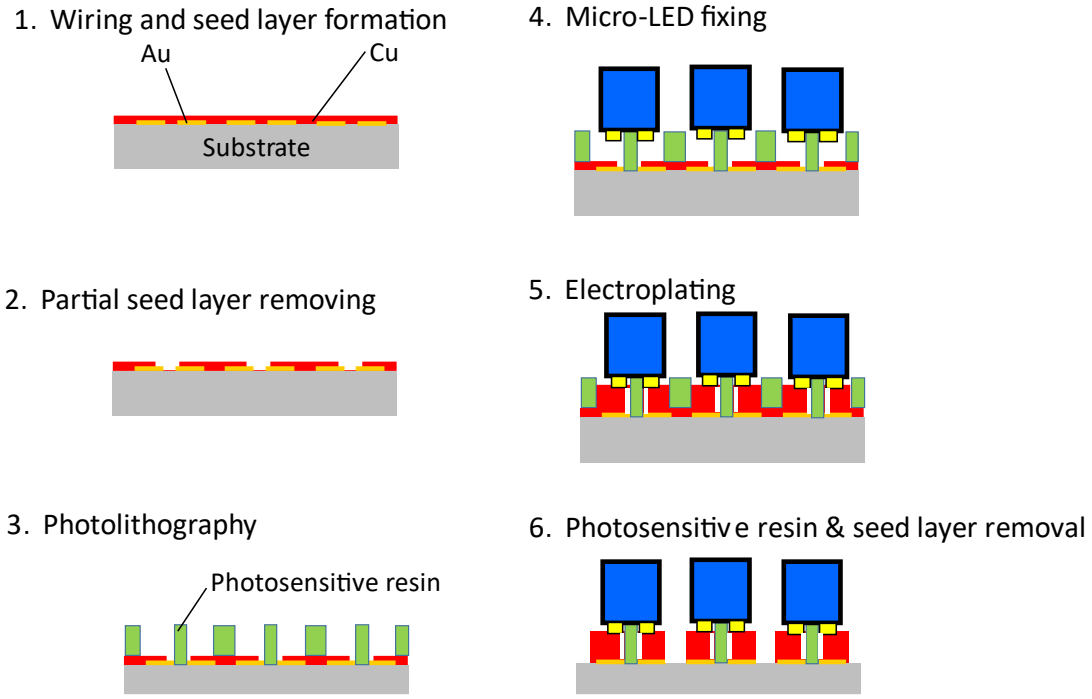


Fig. 3-17 Process flow of electroplated Cu direct bonding

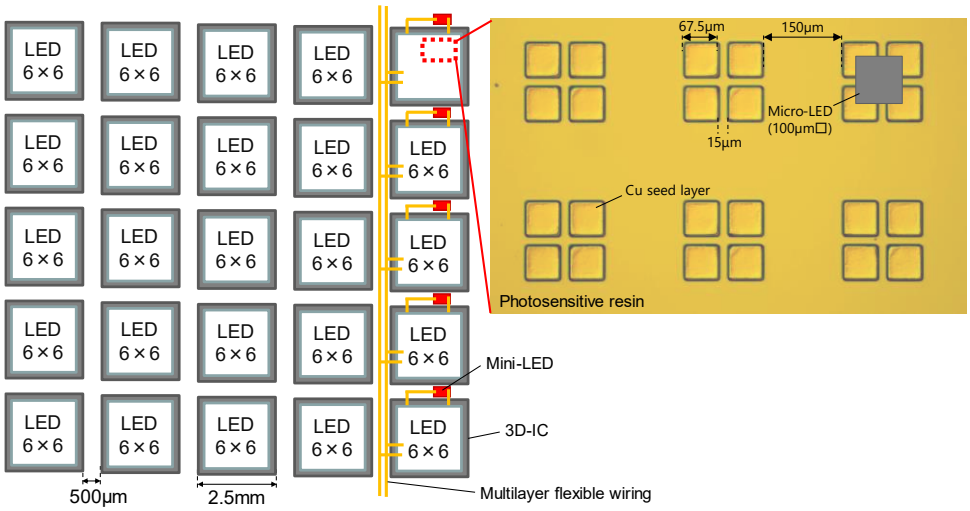


Fig. 3-18 Micro-LED arrangement and aperture pattern.

3.3 Yield evaluation of micro-LED bonded by electroplated Cu direct bonding

The bonded micro-LED arrays' light emission was evaluated. Voltage was applied while a manual probe was in contact with the Au wiring. Photographs of the luminescence are shown in Fig. 3-22. Fig. 3 23 displays the LED's light yield at this time. Three blocks of each 6 x 6 μLED array are extracted, and whether the μLED emits blue light is mapped. The yield was 63%

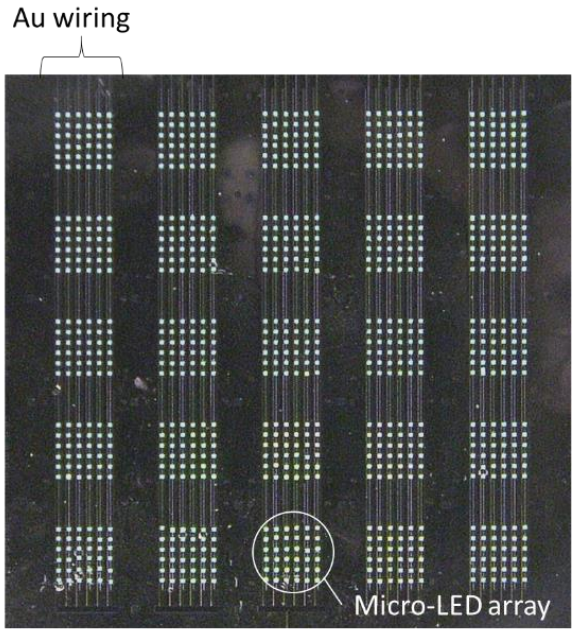


Fig. 3-19 Micro-LEDs temporarily fixed on photosensitive resin

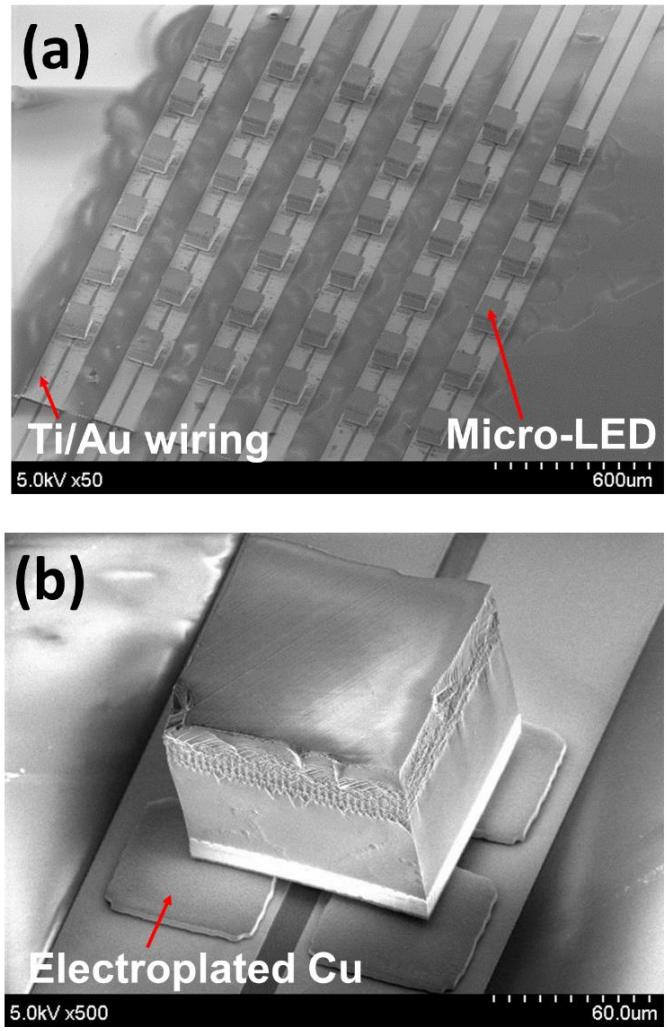


Fig. 3-20 Micro LED array bonded by electroplated Cu direct bonding (a) and magnified micro-LED (b).

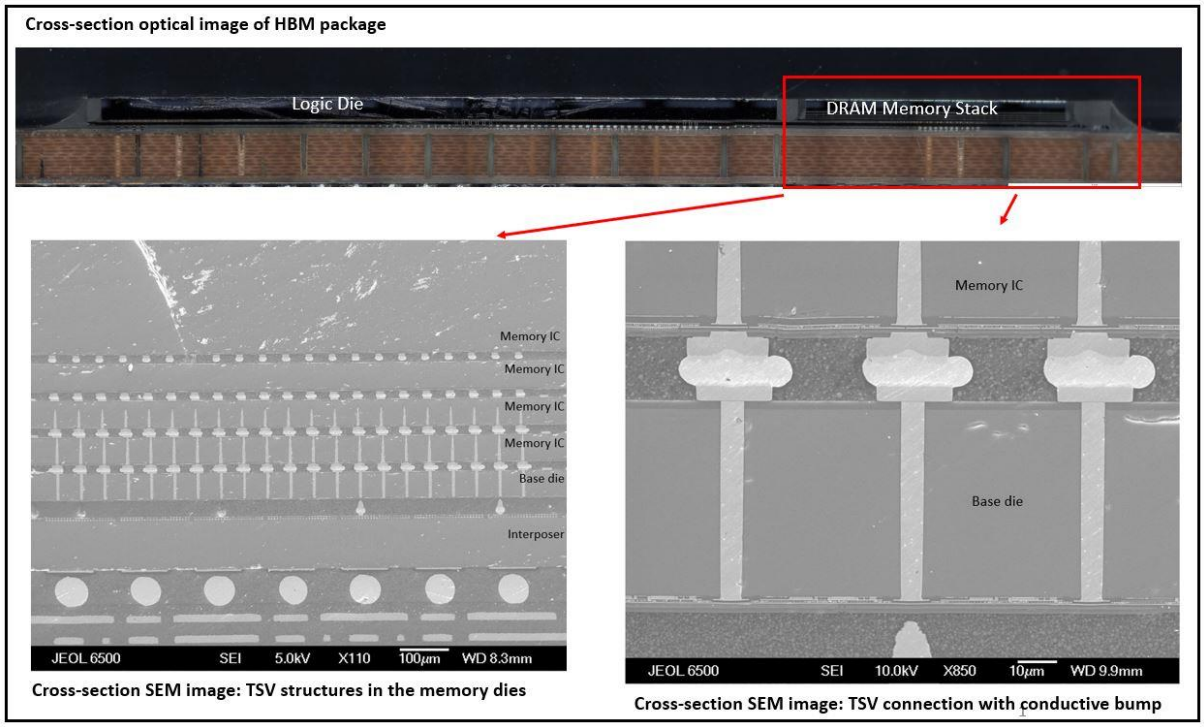


Fig. 3-21 Cross-section of HBM[89]

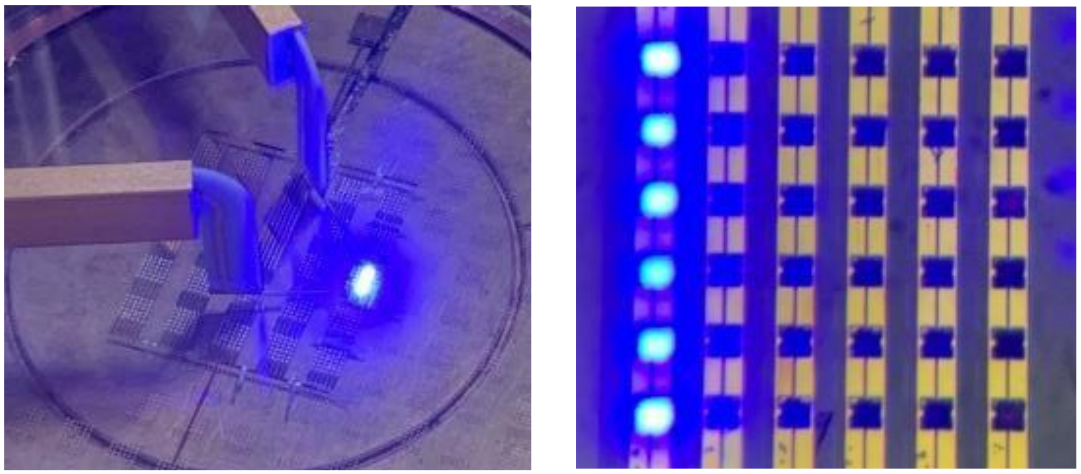


Fig. 3-22 Micro-LED emitting light.

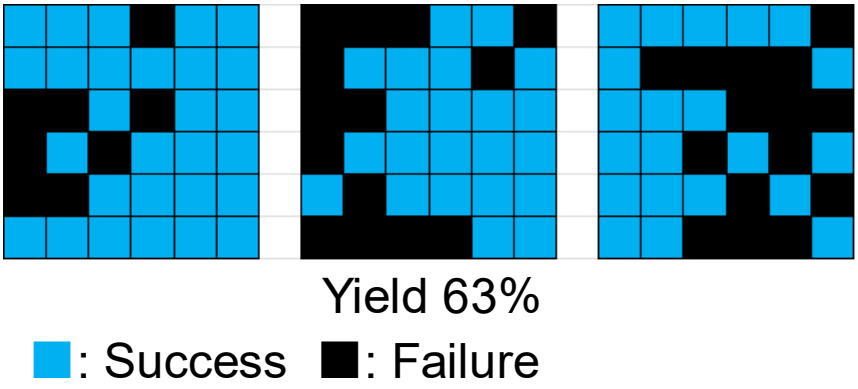


Fig. 3-23 Yield mapping of electroplated Cu direct bonding

3.4 Failure analysis of electroplated Cu direct bonding

In this section, failure analysis of electroplated Cu direct bonding is performed and methods to improve yield are discussed.

3.4.1 Sidewall insulation

The SEM photograph of the plated and bonded micro-LED is shown in Fig. 3-24. Electric current begins to flow in the micro-LED when the developed plating hits its electrodes, which is expected to encourage plating growth on the sidewalls of the LED. Since the GaN layer is exposed on the side of the micro-LED, if the plating touches the side of the LED, a short circuit will occur, which can cause malfunction. As a result, I used the method depicted in Fig. 3 25 to deposit an insulating layer on the sidewall of the micro-LED to insulate it. The micro-LED are supplied fixed on tape. Low-temperature processes are needed for sidewall protection after the singulation process. Typically, the glue layers of dicing tapes are not thermally stable. Since the micro-LED are embedded in the tape's adhesive, the sidewalls of the micro-LED were entirely exposed by oxygen plasma ashing of the adhesive in the area without the micro-LED. Therefore, room-

temperature OER-SiO2-chemical vapor deposition (CVD) is used to improve the interconnect yield with the good quality of SiO2 [90]. Next, SiO2 was deposited on the surface of the micro-LED by OER-CVD. The electrode surface is shielded by the glue, hence this technique has no effect on the Cu direct bonding. The cross-sectional SEM image of the micro-LED with SiO2 is illustrated in Fig. 3-26. On the side surface of the micro-LED, 100 nm of SiO2 was uniformly deposited. The micro-sidewall LEDs has a homogeneous layer of SiO2 film, which lowers the risk of short-circuiting it and boosts yield.

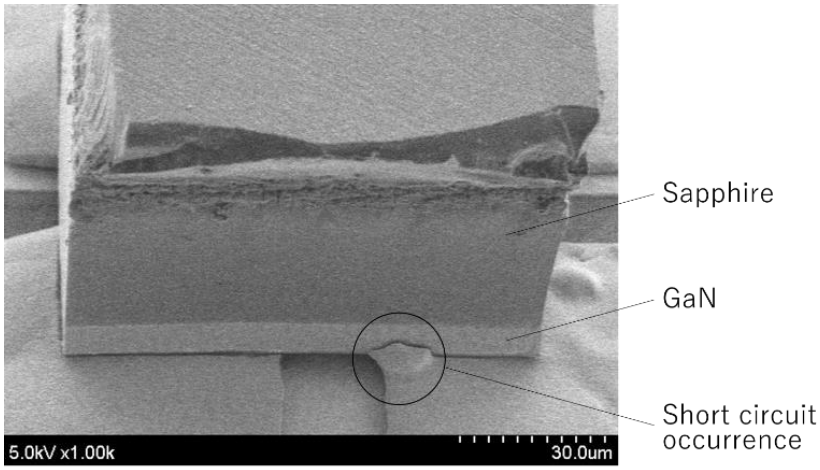


Fig. 3-24 Sidewall plating with bonded LEDs

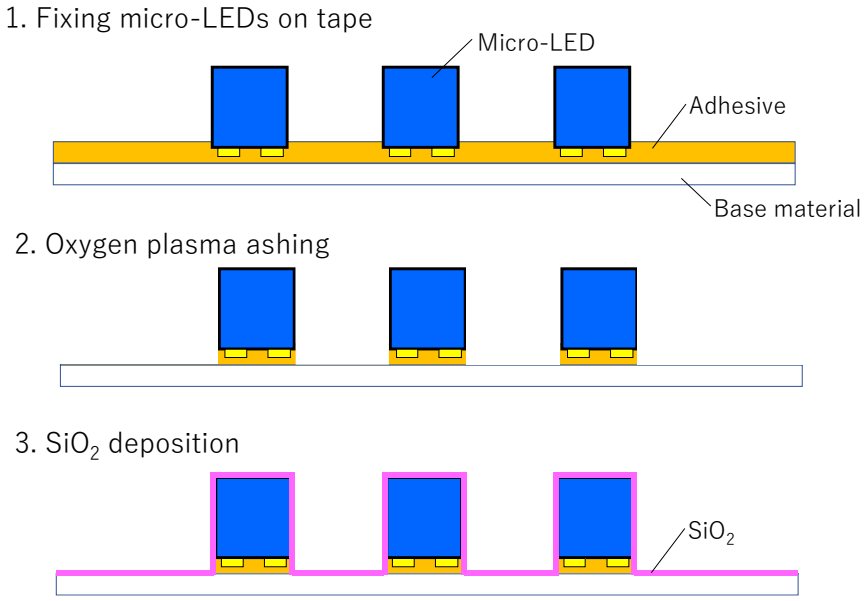


Fig. 3-25 Process flow of OER-SiO2-CVD on the side wall of the micro-LEDs

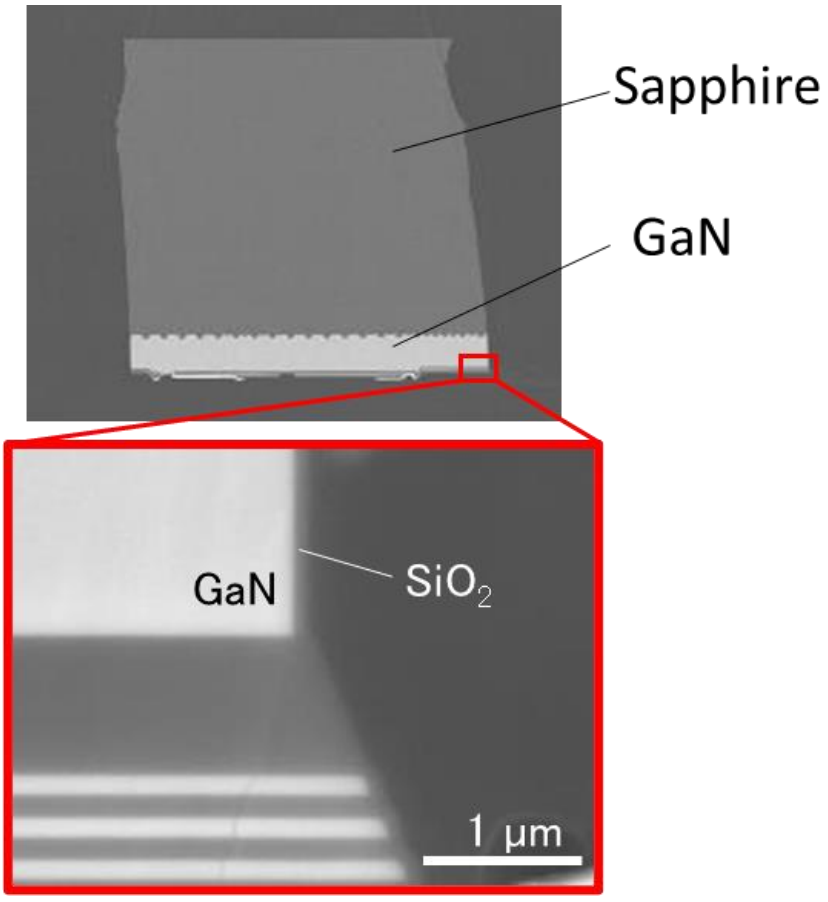


Fig. 3-26 Cross-section of micro-LED sidewall with SiO2

3.4.2 Additional tilt compensation

This section describes another failure, inter-electrode bridge. When a non-operating micro-LED was removed as depicted in Fig, the bridge between the PN electrodes was observed. This is believed to be the case since the micro LEDs were tilted when temporarily fixed, providing a space for the electroplated Cu to bridge. Therefore, I introduced an additional tilt compensation process using a wafer bonder. A 10N force was applied to each LED while the temperatures were set at 50 °C, 70 °C, and 90 °C, which are close to the glass transition temperature of photosensitive resin. After pressure welding at each temperature, the LED was peeled off, and the step of the photosensitive resin at the peeled-off mark was measured using a surface profiler as shown in Fig. 3-27. Fig. 3 28 provides a summary of the images' findings of the photosensitive resin following peeling. The micro LED sinks deeper as the temperature increases, showing that at 90 °C the photosensitive resin expands significantly due to pressure welding. At 70 °C, the photosensitive resin is fully in contact with the entire LED, suppressing the loss of electrode area. Future procedures will incorporate pressure welding at 70 °C.

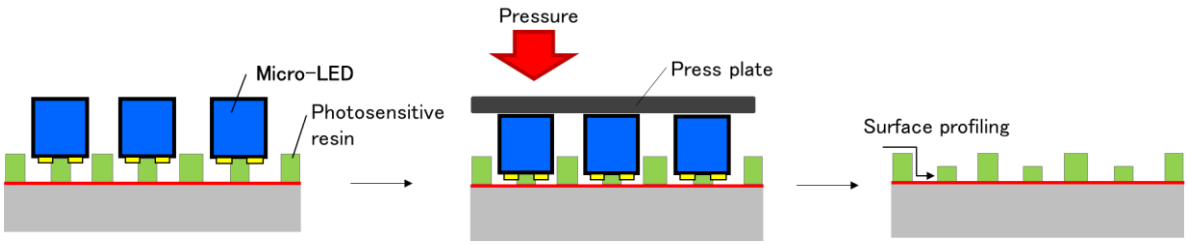


Fig. 3-27 Evaluation method of additional tilt compensation

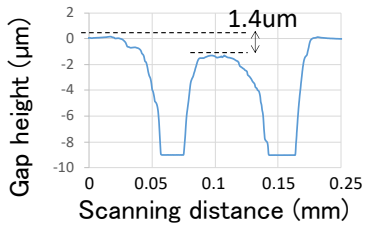
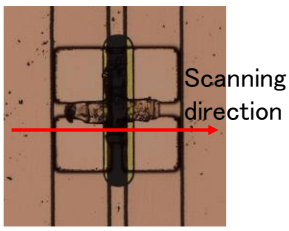
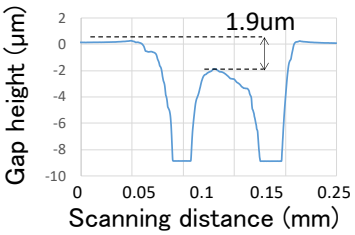
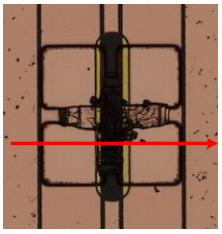
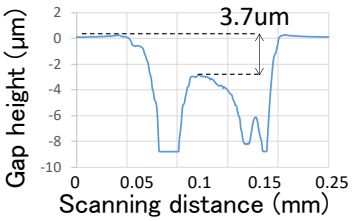
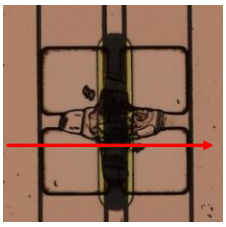
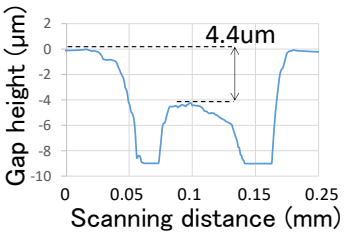
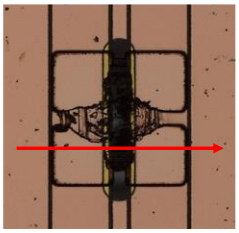
Compensation temperature	Surface profile	Photo of resin after compensation
Without compensation		
50℃		
70℃		
90℃		

Fig. 3-28 Comparison of compensation temperature

3.4.3 Optimized process of electroplated Cu direct bonding

The optimized process flow is shown in Fig. 3-29. I used micro LEDs with insulated side walls. Following pick-and-place temporary bonding of the micro LED, a wafer bonder-added tilt compensation step was applied.

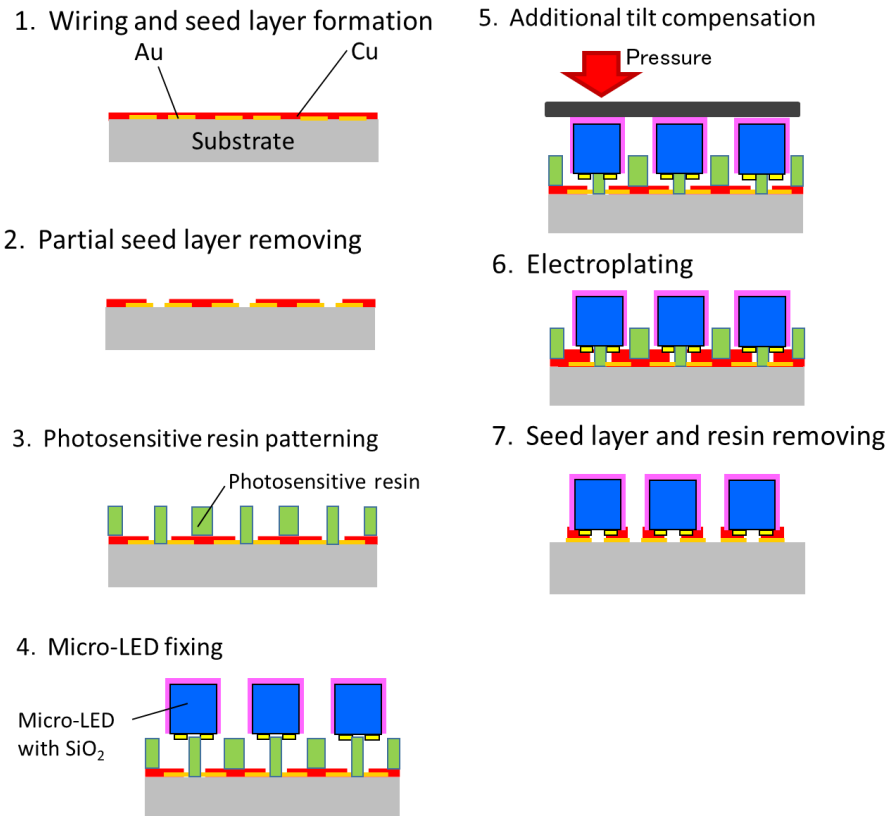


Fig. 3-29 Optimized process flow of electroplated Cu direct bonding

3.5 Yield evaluation of micro-LED bonded by optimized electroplated Cu direct bonding

The results of the luminescence yield evaluation of micro-LED bonded by the optimized process are summarized in Fig. 3-30. The yield with the optimized process was 92% as opposed to the prior procedure's yield of 63%, which is a substantial improvement. The figure displays images of the luminous micro-LED. The 6 x 6 μLED array block is picked up from the bottom right in Fig. 3-31. Although there are differences in electroluminescence intensity, all μLED emit blue light.

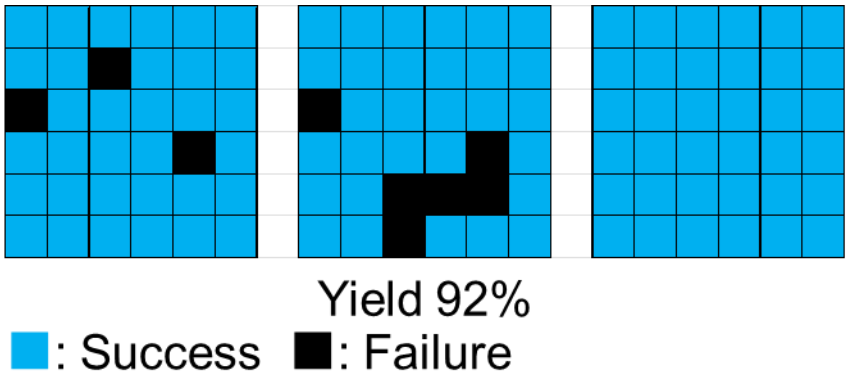


Fig. 3-30 Yield mapping of optimized electroplated Cu direct bonding

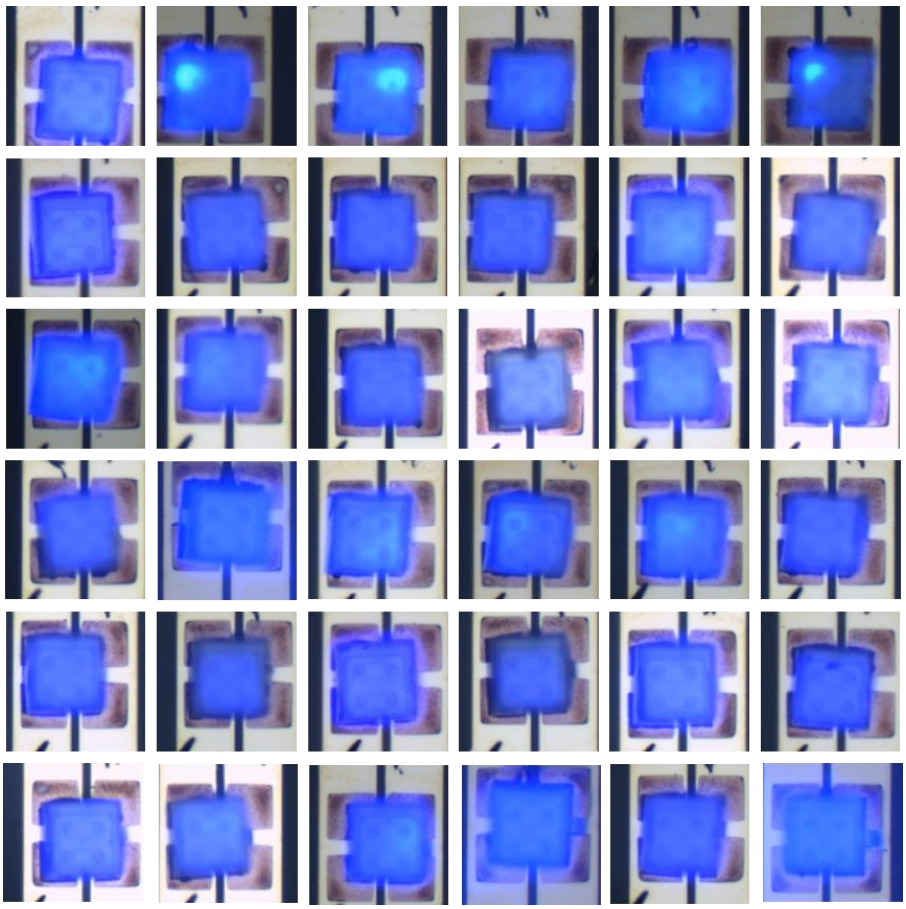


Fig. 3-31 the photo of a μLED array emitting light.

Fig. 3 32 displays the I-V characteristics of the micro-LED following electroplated Cu direct

bonding. The I-V behaviors are primarily divided into three types. The representative I-V curves of the three micro-LED are shown with the microscope images. The I-V characteristics of the first and second micro-LEDs with good and relatively lower electroluminescence intensity are shown in Fig. 3 32(a) and (b). The second micro-LED gives one order of magnitude lower intensity than the first micro-LED when the voltage is increased up to 3 V. However, they are comparable to the perfect micro-LED dies before semi-additive procedure (SAP) bonding. That indicates there is no degradation after SAP bonding. There is no leakage since the level of the current flowing to the negative voltage area is the same as that of the first micro-LED. On the other hand, Fig. 3-32(c) depicts the I-V curve of the third micro-LED having considerably low emission intensity. The current is not flowing enough. The image captured by a fluorescence microscope reveals black emission from the third micro-LED, as can also be seen in Fig. 3 33. The emission intensity of the first and third micro-LED are compared using X-ray transmission images, as shown in Fig. 3-34. Small voids are observed in an intense-emission micro-LED, but there is no resistance increase to positively shift the V_{TH}. However, when the weakest-emitting micro-LED is used, no gaps that could significantly alter the resistance between the electroplated Cu pillars and micro-LED are seen. Small leakage at the pre-etch sections, as detailed below, is likely to be the cause of the third micro-exceptionally LED's low emission.

The main reason for the other non-emission micro-LED is discussed. Another Cu bridge is seen at the failure micro-LED sidewall along partial seed pre-etching patterns, as depicted in Fig. 3 35, extending over the sapphire wafer. The emission failure is attributed to the adhesion between the photosensitive resin and the underneath sapphire wafers: these parts are exposed after partial seed pre-etching. The subsequent design that has been tuned for heterogeneous integration with 3D-ICs should expand this pre-etch pattern to many tens of micrometers in a longitudinal orientation. Additionally, the bridge and short problems would be solved by designing the inter-

aperture spacing formed with the photosensitive resin. This structure is likely to be bridged at the pre-etch sections, which is another reason why the third micro-LED hows emit light insufficiently. The total interconnect yield, excluding the low-emission micro-LED, is 75%.

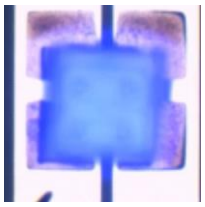
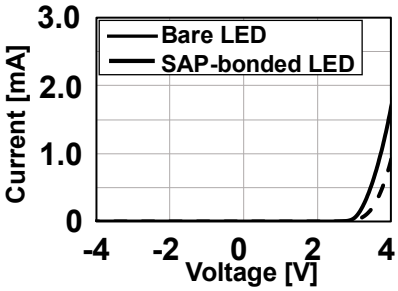
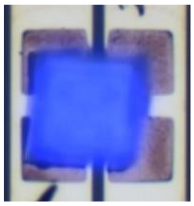
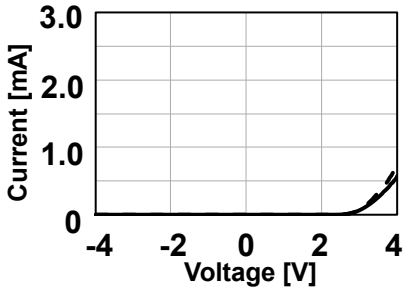
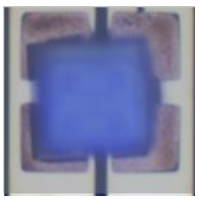
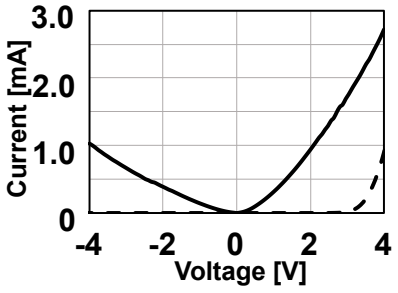
Light intensity	Photo of micro-LED	Electrical characteristics
(a)Intense		
(b)Weaker		
(c)Weakest		

Fig. 3-32 I-V characteristics of intense-emission.

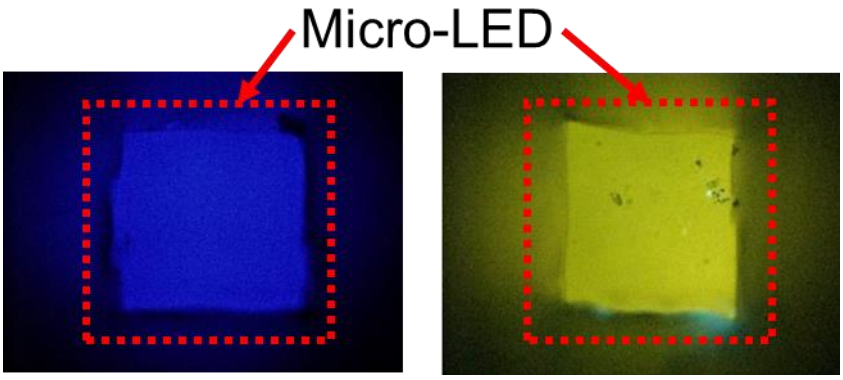


Fig. 3-33 Fluorescence microscope of intense micro-LED(left) and weakest micro-LED (right)

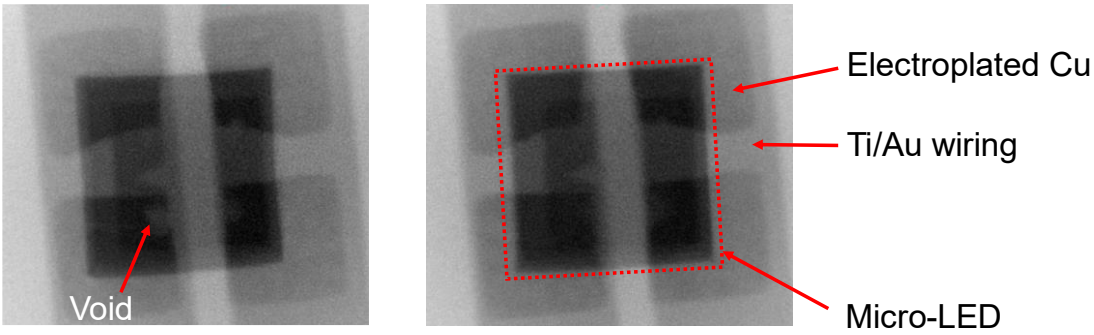


Fig. 3-34. X-ray transmission image of the intense (left) and weakest (right) emission micro-LEDs.

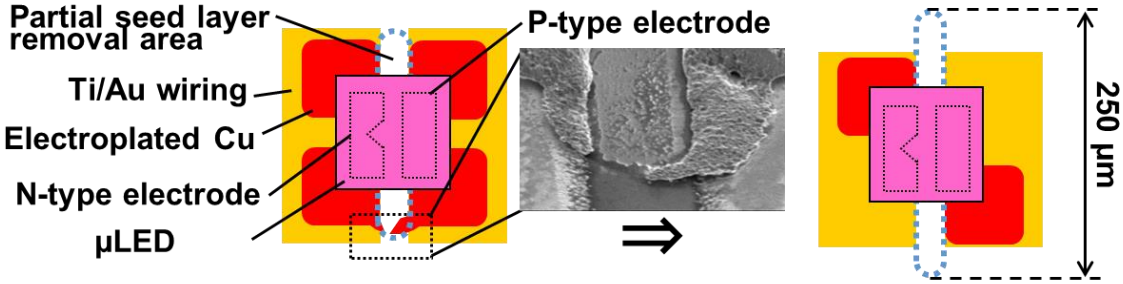


Fig. 3-35 SEM image of an inter-pillar bridge formed at the interface between the photosensitive resin and a wafer, and current and proposed aperture/pre-etch seed designs

3.6 Conclusion

Conventional bonding used for 3D integration requires thermocompression bonding. The 3D-IC is destroyed when a high-temperature point load is applied to it, making it difficult to attach micro dielets to the 3D-IC. Therefore, I have developed room-temperature electroplated direct bonding. Next-generation displays are expected to incorporate micro-LEDs, which were successfully used as micro dielets and bonded with high yields. I have achieved the prospect of achieving its target luminescence yield of more than 99% for Smart Skin Display. Dielets that are not appropriate for thermocompression bonding can be bonded using this procedure in a single batch. Additionally, it is a fantastic bonding technique that may affix multiple heterogeneous chips at once.

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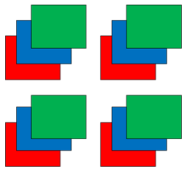
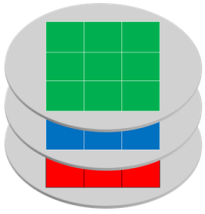
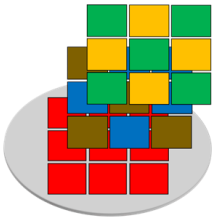
Chapter 4
Micro-LED stacking on 3D-IC using dielet-on-wafer bonding

4.1 Introduction

4.1.1 3D stacking method

Among the fabrication technologies for 3D-ICs, 3D integration methods are typically divided into three categories: chip-to-chip (C2C) [1][3], wafer-to-wafer (W2W) [4]-[7], and chip-to-wafer (C2W)[8]-[14]. Figure 1-9 depictsthe comparison between 3D integration techniques. The C2C process is based on the pick-and-place approach for known good dies (KGD). The C2C stacking method is used in industry for 3D DRAM manufacture. However, the alternative W2W approach is utilized in the large-scale manufacture of 3D image sensors due to the limited production throughput of the C2C process. However, the W2W process cannot remove defective chips in large-scale integration (LSI) wafers before stacking. As a result, the W2W process is applicable only for high-yield LSI wafers. The W2W technique also suffers from a significant drawback when stacking chips of various sizes. The C2W strategy can benefit from both the C2C and W2W strategies. The C2W approach can enhance production yield using KGDs and the throughput using wafer-level processes, and the product throughput becomes higher than that of the C2C method. Additionally, given that the semiconductor industry is currently concentrating on heterogeneous integration, the flexibility in chip size is in line with what the industry needs.

Stacking method	*Chip-to-Chip*	*Wafer-to-Wafer*	*Chip-to-Wafer*
Throughput	Extremely Low (one by one)	High (batch processing)	Low to medium (pick & place)
Yield	High (use of KGD*)	Low	High (use of KGD*)
Flexibility in chip size	High	Low	High
Applications	Packaging	DRAM (high-yield products)	CIS, logic, memory, MEMS, etc.
Schematic			

*KGD: Known Good Dies

Fig. 4-1 Comparison of stacking methods for 3D integration.

4.1.2 Thorough Silicon Via (TSV)

TSV is a critical technology in 3D-IC: 3D integration using TSV offers different advantages, such as reduced delay and power consumption due to shorter electrical path lengths, increased number of input/output pins, enhanced performance per volume, and heterogeneous integration. TSV formation can be classified into three types: via-first, via-middle, and via-last types. The front-side via and the back-side via are two more categories for the via-last type. Fig. 4 2 provides a summary of these procedures [18].

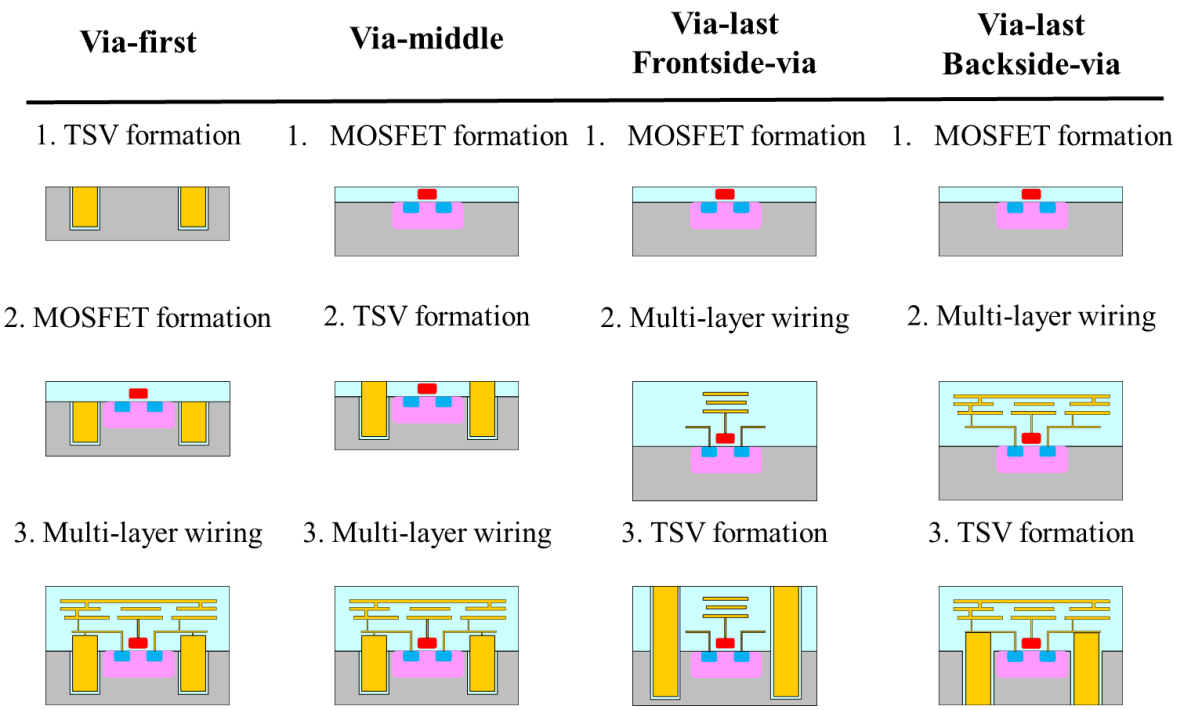


Fig. 4-2 Classification of the TSV formation process [18]

Via-first TSVs are fabricated before the front end of line (FEOL) process [19][20]. Due to the fact that it can develop at high temperatures, a high-quality dielectric layer can be created. Polycrystalline silicon with high thermal stability is used as the TSV filling material because thermal annealing at high temperatures above 900 °C is applied during the gate oxide layer fabrication. Although polycrystalline silicon has good thermal stability, using low-pressure chemical vapor deposition results in high resistance and a low deposition rate (LP-CVD). Recently, the via-middle and via-last processes have been primarily studied.

Via-middle TSVs are fabricated between FEOL and the back end of the line (BEOL) process [21][24]. Figure 1-8 demonstrates how the Bosch technique, also known as deep reactive ion etching (deep-RIE), creates deep silicon vias. The dielectric layer with good quality is deposited at sufficient temperature by CVD including plasma-enhanced CVD and semi-atmospheric ozone-CVD. Then, tungsten [25] or copper is injected into deep silicon vias. The BEOL technique thins

the wafer with TSVs. The TSVs are exposed from the back-side of the wafer. Due to silicon's high diffusion coefficient, any leftover metal on the backside of the wafer generates metal contamination. Therefore, it is important to form a barrier layer around the sidewall of the TSV and the backside surface of the wafer. Cu is typically utilized as TSV filler material due to its low electrical resistance, even though tungsten has high electrical resistance and a poor diffusion coefficient. Owing to the high productivity of the via-middle process, it is primarily used in the mass production of processes with high production yields such as DRAM [26].

Via-last TSVs are fabricated after the BEOL process. Two different approaches can be used for the via-last TSV procedure. [27][29]. One method is via-last/front-side via TSV, which is formed from the surface of the circuit. Although it is quite simple to connect TSV with other wires, etching from the circuit's surface prevents the circuit layer from being overlapped with the front-side TSV area. In addition, it is challenging to etch interlayer dielectric on the circuit surface. However, compared to the via-middle technique, via-last/front-side offers higher metal contamination dependability.

The other method is via-last/backside-via TSV, which is formed from the backside of the wafer. A wafer is thinned from the backside after the BEOL procedures, deep silicon vias are produced by DRIE, a dielectric layer is coated by CVD, and metal-1 (M1) is exposed by DRIE for electrical connections. Then, conductive metal is filled in deep silicon vias. The TSVs are then produced with microbumps using the via-last/backside technique on the backside of the wafer.

The biggest advantage of Via-last TSV is high design flexibility in multi-level metallization. Since Via-last TSVs are not formed in BEOL processes, the TSV fabrication is not limited to the so-called “Mega Fab.” which is an extremely large factory having both FEOL and BEOL for manufacturing semiconductor IC. Even small OSAT and research institutes/labs can fabricate TSVs from the backside of wafers or chips after the BEOL processes to give an electrical

connection to M1 layers. Using multichip-to-wafer stacking and Via-last TSV generation, I have so far shown how to fabricate a number of 3D/TSV devices [30][31]. However, further process optimization is still required to enhance the 3D integration yield. The detailed fabrication process for a typical TSV is shown in

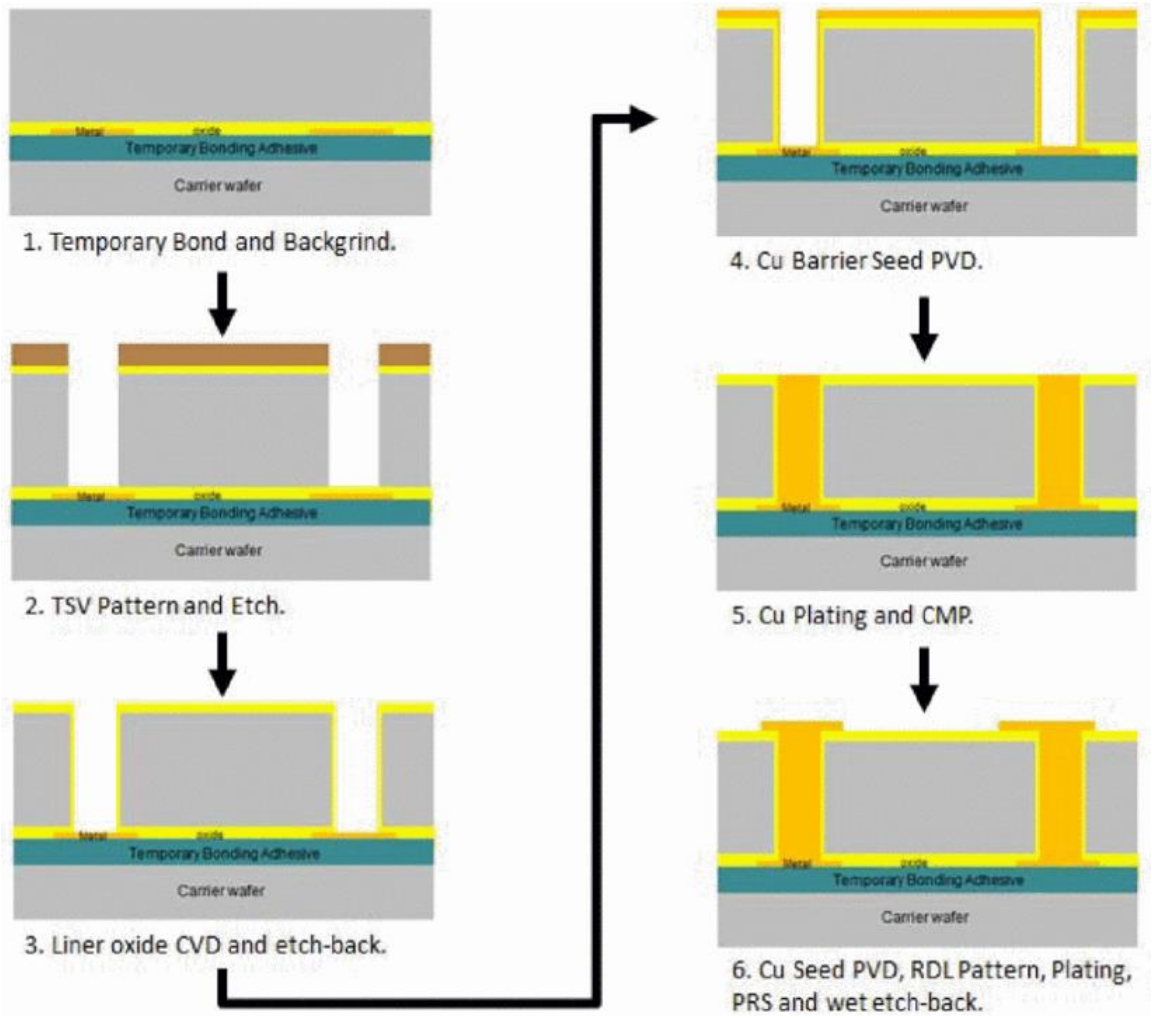


Fig. 4-3 [32]. This is a case of via-last. First, chips are adhered face-down to a carrier wafer that has been treated with a temporary adhesive. Next, mechanical grinding and CMP are used to thin the wafer. Via holes are then formed using the Deep-RIE process. Following the formation of a liner on the sidewalls of the through holes using techniques such as CVD, etc., a barrier/seed layer is next deposited. The via holes are then filled by plating, etc., and CMP removes the

overburdened Cu. Finally, RDL bumps and patterns are created. Barrier/seed layer deposition into deep Si holes, such as those with a TSV diameter of 10 μm and a depth of 100 μm, is the most difficult step in 3D integration (aspect ratio: 10). In addition to perfect coverage of the barrier layer such as Ti, Ta, TiN, and TaN, a thick Cu seed layer is required to fill electroplated Cu in a bottom-up growth fashion. As demonstrated in Fig. 4 4, a significant void can be detected at the bottom of the TSV if the insufficient Cu seed layer is deposited in deep Si holes. In TSV fabrication industry, very limited and expensive long-throw ionized PVD tool is said to be mandatory to deposit the thick Cu more than 100 nm for perfect Cu-TSV filling by electroplating. The conditions required for TSV creation with the maximum aspect ratio utilizing a general-purpose standard PVD apparatus were examined in this study, taking into account the directivity of sputtered metal particles and PVD tool structure.

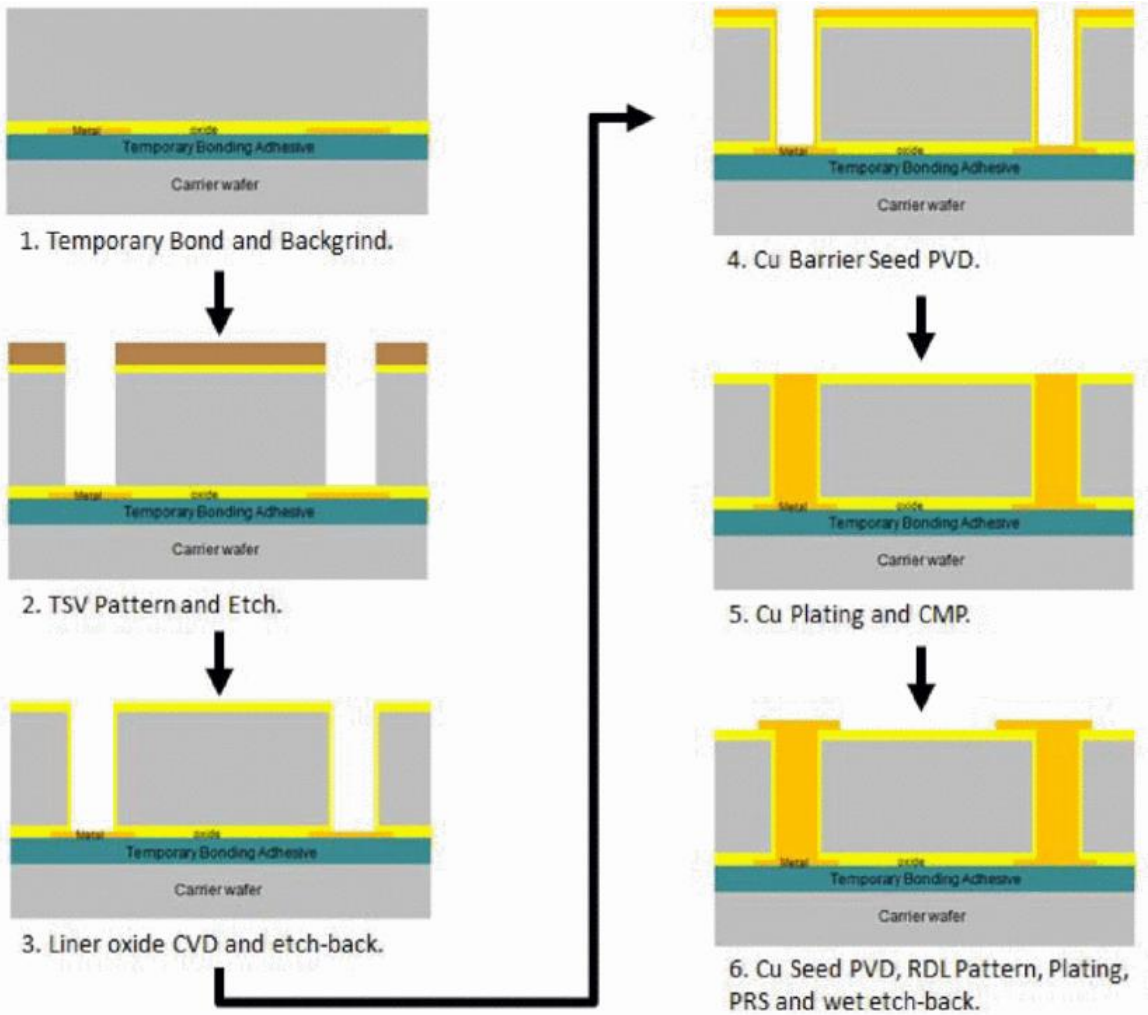
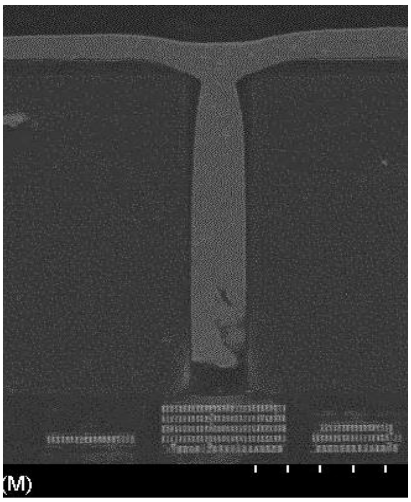


Fig. 4-3 Typical process flow of TSV [32].

(Backside via approach)



(Via middle approach)

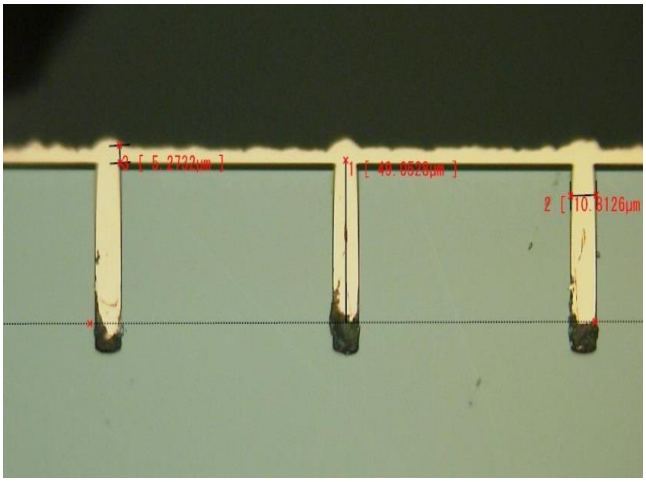


Fig. 4-4 Via fill failures owing to poor coverage of conventional sputtered barrier/seed layers.

4.1.3 Deposition of barrier/seed layer

This study focuses mainly on barrier/seed layer deposition. Higher aspect ratio TSVs are needed as semiconductor processes get finer. Physical vapor deposition (PVD), a widely used industrial technique for depositing metals, experiences shadowing when the aspect ratio rises[33]. The shadowing effect represents a phenomenon in which the coverage of steps at the sidewalls and bottoms of trenches and vias deteriorates, and overhanging structures are formed at the top corners of trenches and vias. Differences in coverage can cause voids in the embedding process. This phenomenon shown in Fig. 4-5 (a) shows the case where the incident light flux has no directionality and angular distribution, Fig. 4-5(b) depicts the case where the incident light flux has directionality and is incident at a right angle to the substrate, and Fig. 4-5(c) demonstrates the case where the incident light flux is incident at a slight angle to the substrate.

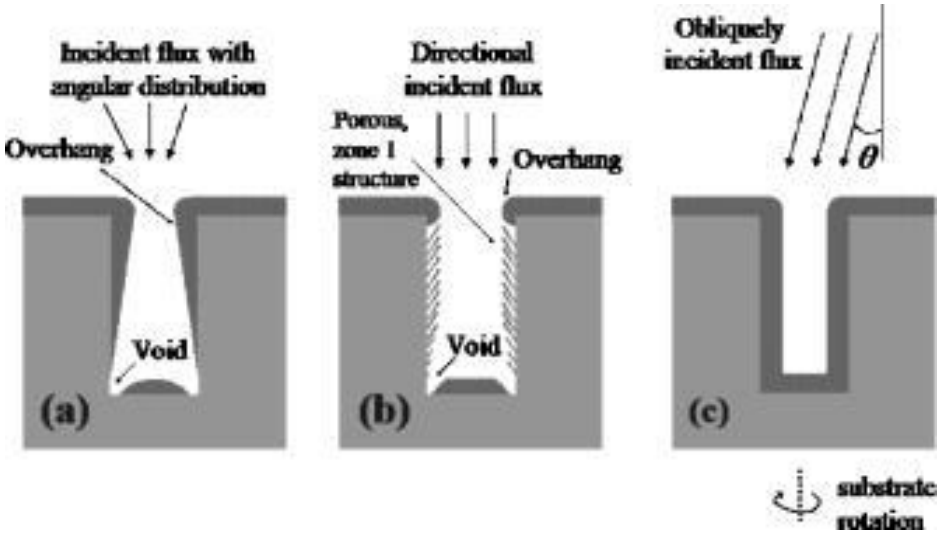


Fig. 4-5 Films deposited in trenches/vias by conventional physical vapor deposition (PVD) [33]

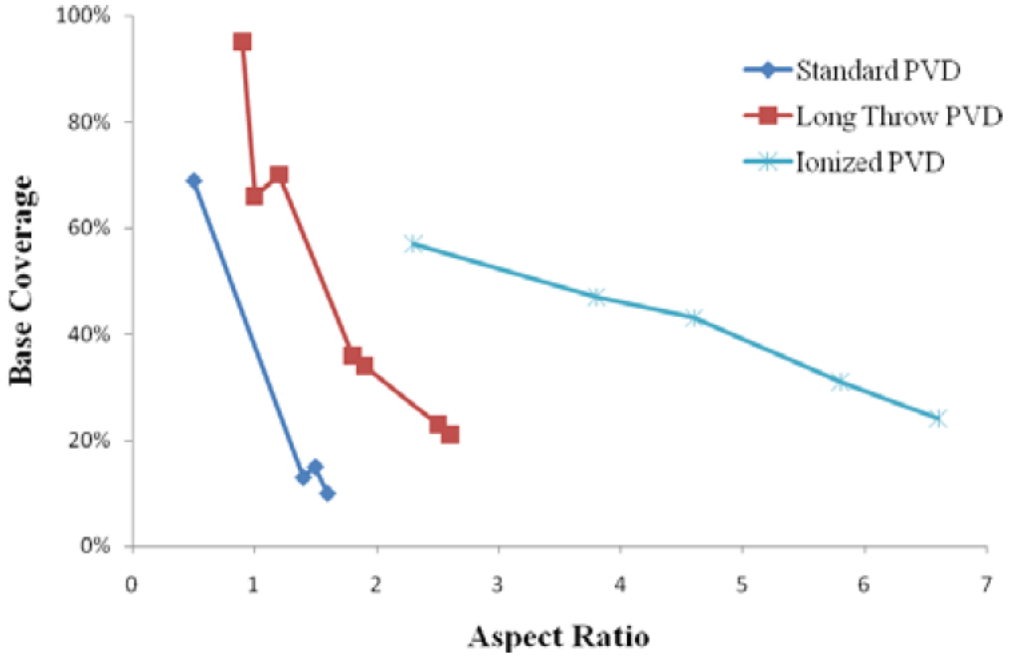
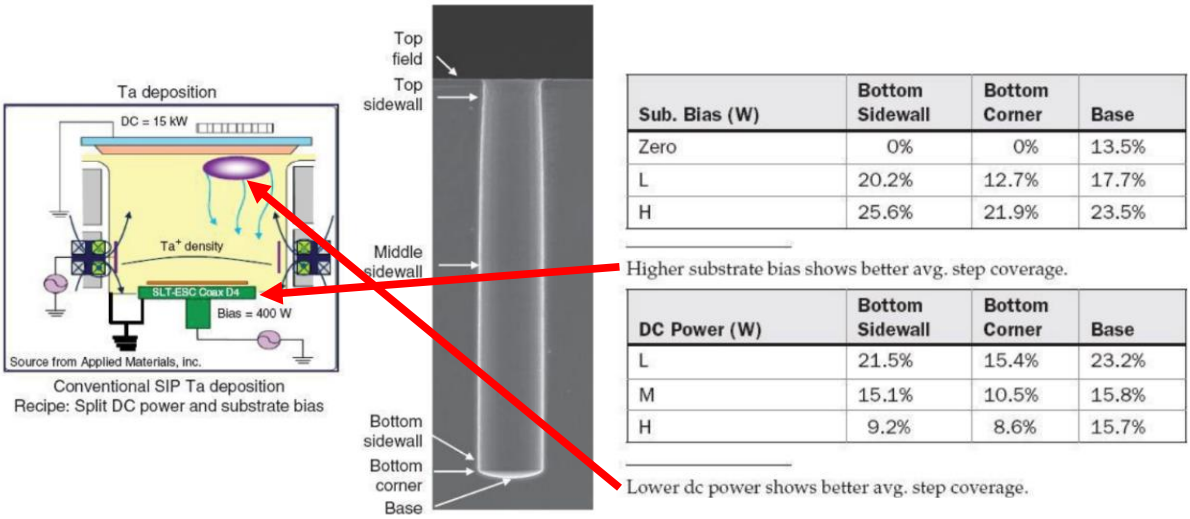


Fig. 4-6 Comparison of the effect of different PVD techniques on base coverage at increasing aspect ratio (TSV diameter: 15 μm) [33]

Long-throw PVD, in other words, directional PVD (DPVD) [34][36] and ionized PVD (iPVD) [34][37] are used to alleviate this step coverage problem; with long-throw PVD, the distance between the target and the substrate is larger, the light flux diverges less and is more perpendicular to the wafer, allowing more incident atoms to reach the bottom of the via. However, high aspect-ratio structures have low sidewall coverage and long-throw PVD is typically less effective, which can result in voids [33]. Fig. 4-6 depicts that coverage is improved by increasing the distance between the target and the substrate. With the help of an applied bias potential to the substrate, ionized sputter particles scattered from the target are made perpendicular to the surface using the iPVD technique. The step coverages at the bottom sidewall, bottom corner, and base of via with a long-throw iPVD of AMAT, the largest company in the special TSV sputtering tool in the industry, are illustrated in Fig. 4-7. Ta as a barrier layer is applied into Si hole with a diameter of 10 μm and depth of 60 μm (aspect ratio: 6), and the substrate vias and DC power for the target metal are controlled. The bottom base coverage is 13.5% when the substrate bias is zero, whereas the bottom sidewall and corner coverages are almost zero. In contrast, high substrate bias application gives drastically increases the coverage up to more than 20% at both the bottom sidewall/corner. The coverages can also vary depending on the DC power, however when the high DC power is used, the minimum bottom corner coverage of 8.6% is reached. On the other hand, the step coverages at the bottom sidewall, bottom corner, and base of via with the long-throw iPVD of AMAT are shown in Fig. 4-8. The substrate vias and DC power for the target metal are regulated, and Cu is placed as a seed layer into a Si hole with dimensions of 10 m in diameter and 30 m in depth (aspect ratio: 3). The resulting Cu step coverages at the middle sidewall are ranging from 5.6% for a low substrate bias and 7.6% for a high bias, respectively. In comparison to the central sidewall, the bottom corner coverages are higher. In comparison to high DC power, the center sidewall coverage is 7.8% for low DC target power. Anyway, it is found that the Cu

coverage is extremely low even when low-aspect-ratio TSV is used. The iPVD does not have high step coverage at high aspect ratios as shown in Fig. 4-9 [39]. Therefore, even when using iPVD with a Cu seed thickness greater than 2 μm, substantial barrier and seed deposition is necessary to completely fill the deep Si hole.



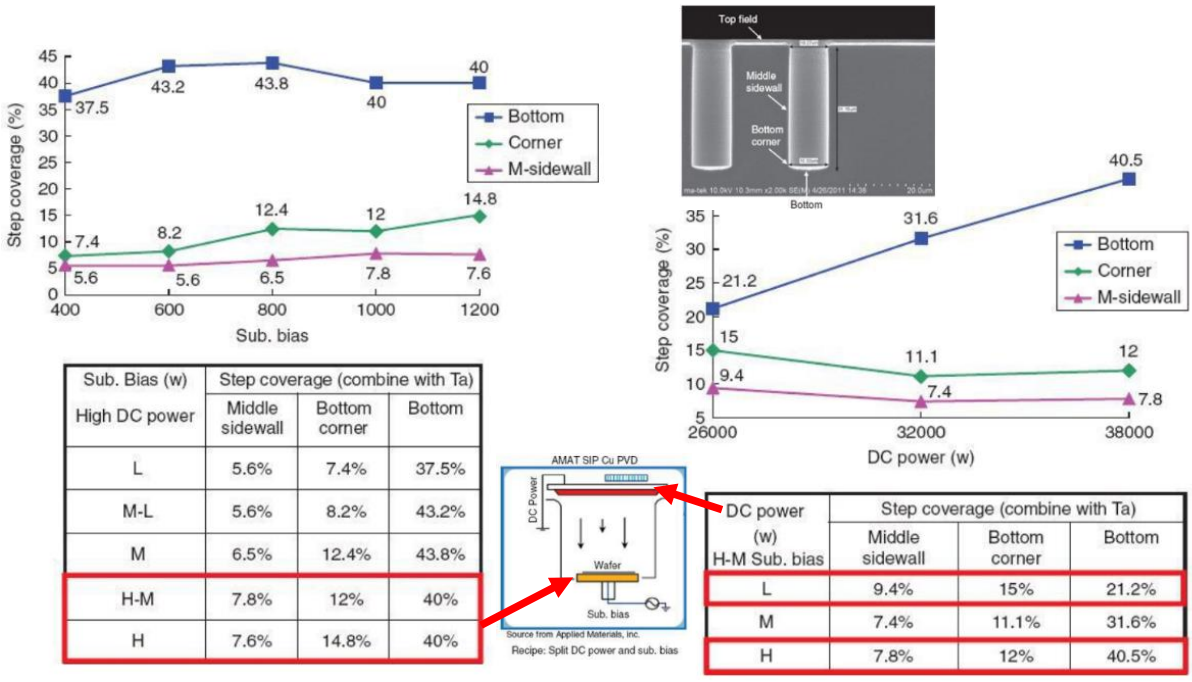
Sub. Bias (W)	Bottom Sidewall	Bottom Corner	Base
Zero	0%	0%	13.5%
L	20.2%	12.7%	17.7%
H	25.6%	21.9%	23.5%

Higher substrate bias shows better avg. step coverage.

DC Power (W)	Bottom Sidewall	Bottom Corner	Base
L	21.5%	15.4%	23.2%
M	15.1%	10.5%	15.8%
H	9.2%	8.6%	15.7%

Lower dc power shows better avg. step coverage.

Fig. 4-7 Step coverage of Ta barrier on TSV with different DC power setting and substrate biases of iPVD [38].



Sub. Bias (w) / High DC power	Step coverage (combine with Ta)		
	Middle sidewall	Bottom corner	Bottom
L	5.6%	7.4%	37.5%
M-L	5.6%	8.2%	43.2%
M	6.5%	12.4%	43.8%
H-M	7.8%	12%	40%
H	7.6%	14.8%	40%

DC power (w) / H-M Sub. bias	Step coverage (combine with Ta)		
	Middle sidewall	Bottom corner	Bottom
L	9.4%	15%	21.2%
M	7.4%	11.1%	31.6%
H	7.8%	12%	40.5%

Fig. 4-8 Step coverage of Cu seed on TSV with different DC power setting and substrate biases of iPVD [38].

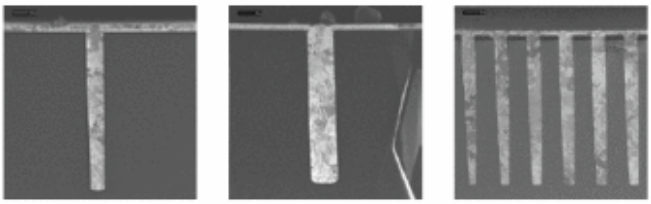
Process	10×100 μm	15×100 μm	5×50 μm
Seed type	iPVD-A	iPVD-B	iPVD-C
Seed thickness (μm in Field)	1.3	2.5	0.3
Step coverage	< 5%	2%	1-3%
Filling rate (μm/min)	1.3-1.6	0.7	1.5-2.0
SEM TSV fill cross-section			

Fig. 4-9 TSV filling performance for iPVD [39].

In this chapter, LSI for Smart Skin Display is processed into 3D-ICs using the Via-last process. The goal is to run the micro-LEDs while stacking them on the 3D-IC without causing

any mechanical damage.

4.2 Experimental

A TSV-specified long-throw iPVD equipment (Sigma fxP 300 PVD, SPTS) with a 2-MHz low-frequency RF substrate bias was used for comparison to standard PVD tools without any substrate bias. The 300-mm wafers may be robotically delivered to each Ti or Cu chamber with the long-throw iPVD system's cluster-style apparatus without releasing the atmosphere. The Ti or Cu target diameter was 14 inches, which was one size larger than the wafers. The distance between the target and the wafer was set at 350 mm or 450 mm. The target-wafer distance for one of the standard PVD tools was 70 mm, while the target and stage diameters were 75 mm and 200 mm, respectively. The typical PVDs utilized in this instance was on 50-mm wafers. The target size is 3 inches, which means the target is one size larger than a 2-inch wafer. The wafer was able to be centered to a chosen target, as illustrated in Fig. 4 10 to carry out dual sputtering of Ti, followed by Cu, without releasing the sputtering pressure to the atmosphere. When the wafer is rotated around the center, the center of the target position was shifted. Although a 2-inch wafer and two 3-inch targets, either Ti or Cu, were centering, another target, either Cu or Ti, was out of alignment. The other standard PVD had a 60-mm target (3 inch)-wafer (2 inch) distance. The center of the larger 3-inch target, Ti or Cu, and the smaller 2-inch wafer were coaxial. In each chamber of Ti and Cu, the target side travels to the wafer side's center without atmospheric release. The wafer was rotated on its axis, tilting it by 5 degrees to lengthen the mean free path. In this investigation, the later standard PVD was used to assess the step coverage of Ti and Cu using electroplated Cu and cross-sectional SEM observation due to the uniformity of the deposition layer.

Samples having deep Si holes with a diameter of 5 μm and a depth of 50 μm (aspect ratio: 10) were used for evaluation of the long-throw iPVD with the low-frequency substrate bias,

alternative to standard 13.56 MHz types. However, samples having deep Si holes with a diameter of 10 μm and a depth of 85 μm (aspect ratio: 8.5) were used for the short-throw standard PVD without substrate bias. These deep Si holes were formed by a typical Bosch etch process with SF_6 and C_4F_8 gases.

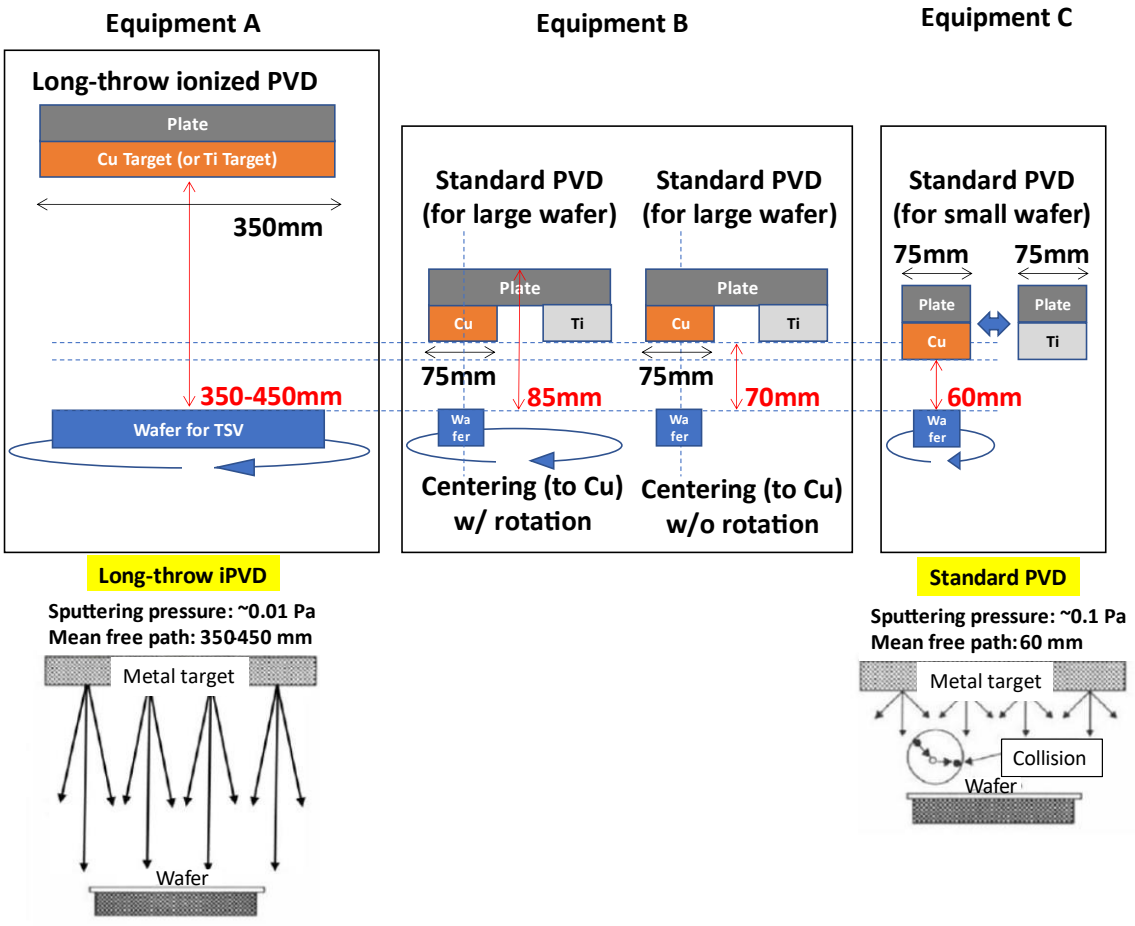


Fig. 4-10 Structure of sputtering tool used in this study and distance between sample and metal targets (Ti and Cu)

4.3 Comparison of barrier/seed layer deposition

between standard and long-through PVD

The deposition of barrier/seed layers for a high aspect ratio via holes remains challenging. To further assess the barrier and seed coverages, a second long-throw iPVD is used with a low-frequency substrate RF bias of 2 MHz. Typically, PVD tools often use 13.56 MHz for RF power, but the lower frequency has effective to enhance the metal particle energy as shown in Fig. 4-11. Here is a list of the correlation between ion energy and ion flux. Compared to high-frequency plasma, the plasma produced by RF power biased with low frequencies has a broadband energy distribution [40]. The high energy metal particles can be re-sputtered at the bottom base where thicker Cu seed is deposited. Re-sputtering of the previously deposited film forces Cu into the shaded area by a big scallop, as illustrated in Figure 4 12. The impact of the long-throw effect (distance between the target and 300-mm wafer) on step coverage is further investigated. The resulting step coverage of Ti/Cu at the via bottom base and sidewall is 6% and 5% for 350-mm distance and 7% and 6% for 450-mm distance, respectively, as shown in Fig. 4 13. The step coverage of the via top sidewall is 13% for 350-mm and 16% for 450-mm distance, but the top thickness on the field layer is 2.4 μm (Cu thickness: approximately 1.6 μm) which is very thick, and the big concern is that large film stress would be caused by the low step coverage. Fig. 4 14 depicts the impact of lower frequency substrate bias on step coverage. Because there are more high-energy metal particles at low-frequency bias, more metal particles enter the through bottom. As a result, re-sputtering occurs at the bottom. As a result, the lower frequency decreases coverage at the bottom and increases coverage at the bottom sidewall. This finding suggests that reducing the substrate bias frequency will result in an improvement in the coverage at the via bottom sidewall.

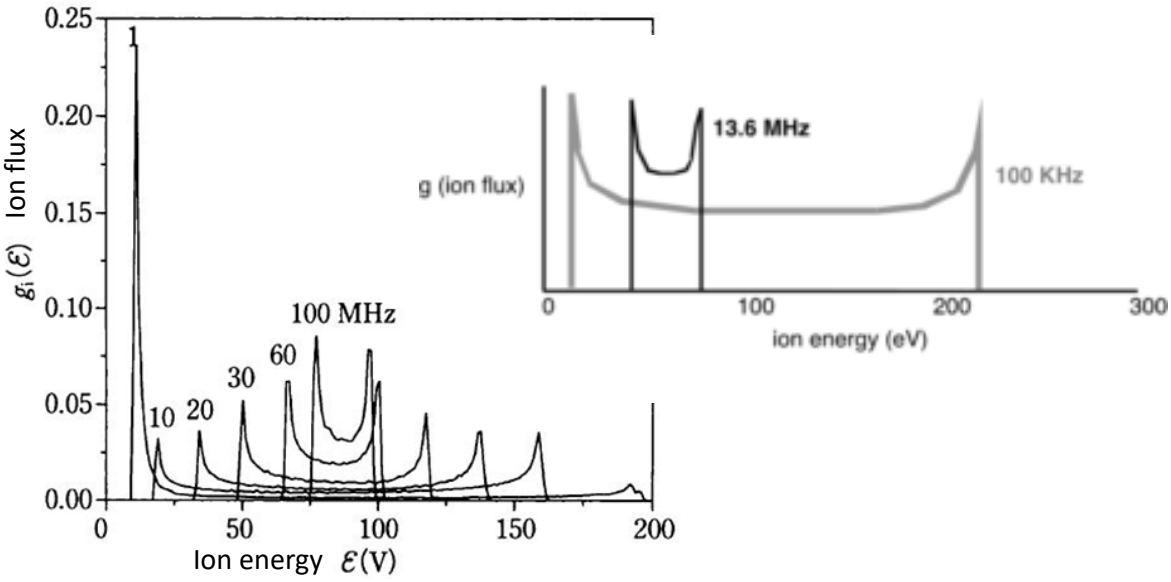


Fig. 4-11 Calculated ion energy distribution function (number of ions vs. ion energy) for argon at "high" and "low" frequencies; data from Dry Etching for VLSI, van Roosmalen et. al.

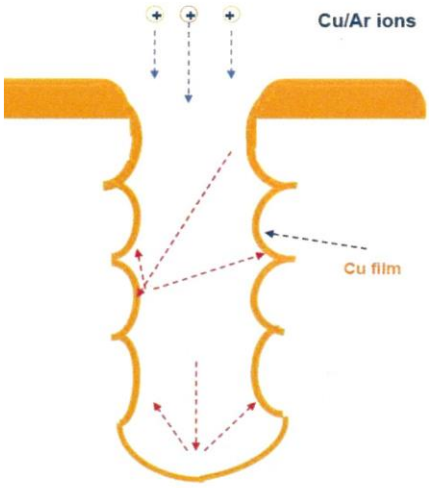


Fig. 4-12 The re-sputtering effect to deposit Cu at the hidden part by large scallop.

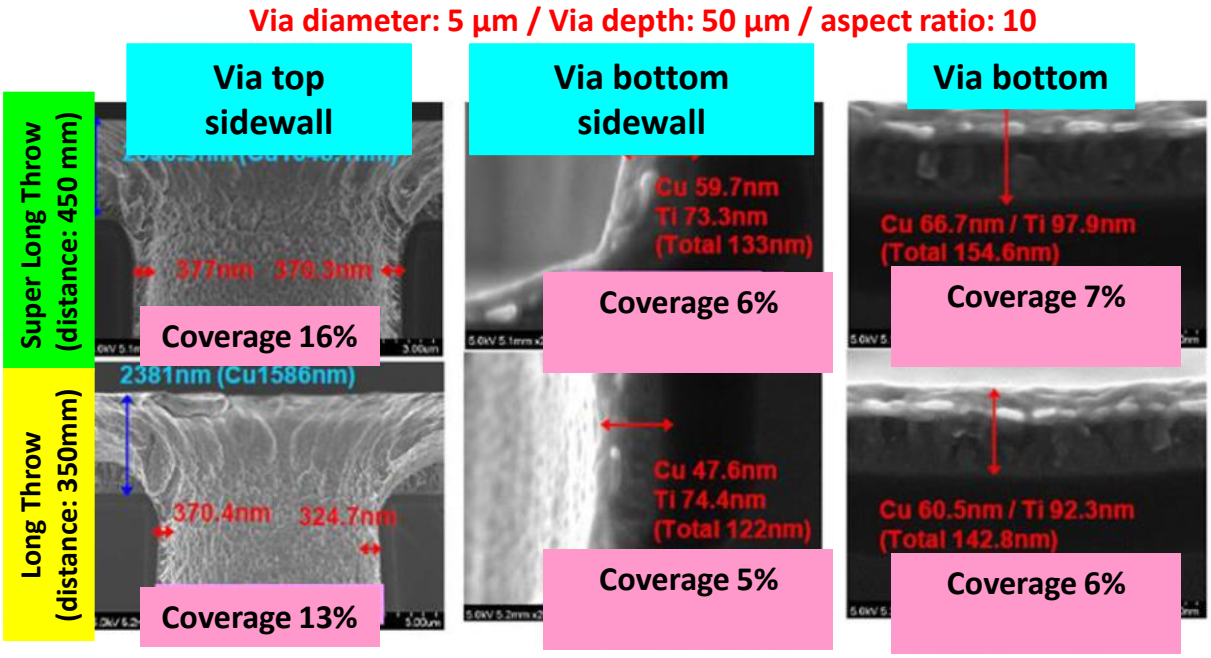


Fig. 4-13 Step coverage of Ti/Cu deposited with long-throw iPVD with low-frequency substrate RF bias (via diameter: 5 µm, via depth: 50 µm, and aspect ratio: 5)

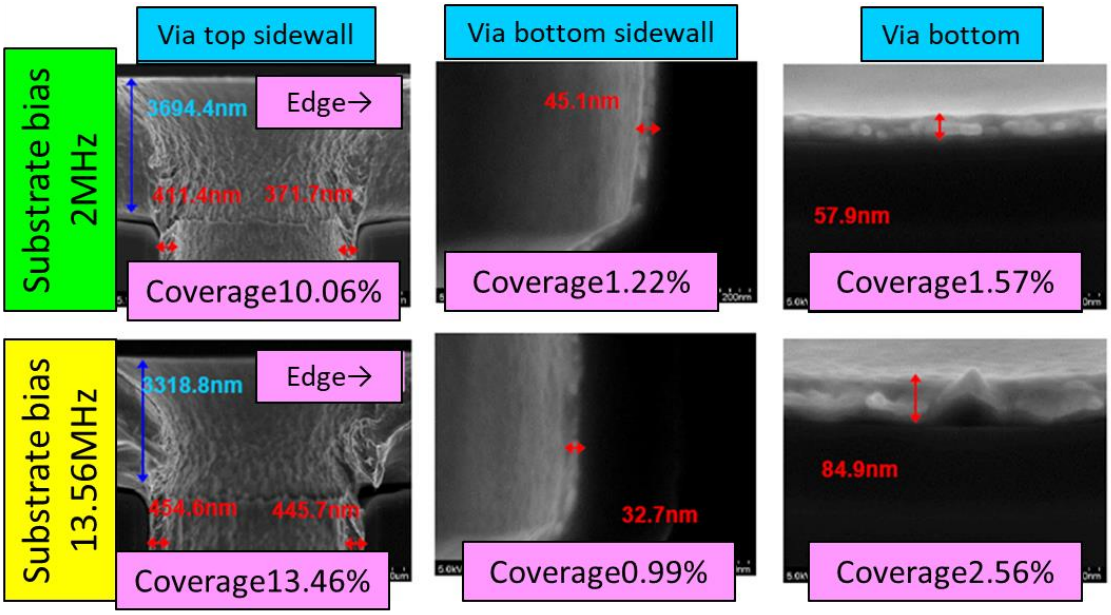


Fig. 4-14 Dependence of step coverage of Cu/Ti on RF bias frequency (via diameter: 5 µm, via depth: 50 µm, and aspect ratio: 5)

In this study, I aimed to fabricate TSV with the highest possible aspect ratio by depositing barrier acid layers using conventional PVD. Smart Skin Display creates multichip 3D-ICs in 5 x 5 arrays. Therefore, the slightest alignment error can be fatal. The largest aspect ratio TSV must be made in order to maximize alignment error tolerance. First, experiments were performed to determine the upper limit of the aspect ratio of TSVs that can be fabricated by conventional PVD. Deep-RIE created through holes on Si wafers that were 10 μm in diameter and 85 μm deep. A 4μm SiO_2 liner layer was then deposited by the TEOS-CVD system. Subsequently, a Ti/Cu barrier/seed layer of 250 nm/1750 nm was deposited by conventional PVD. Finally, Cu electroplating was used to fill the via holes. Figure 4-15 displays cross-sectional SEM images of the manufactured TSVs and shows that embedding failed at TSV depths of 40 μm or higher. This result shows that the maximum aspect ratio of TSV fabricated by conventional PVD is 4. The TSV of the 3D-IC for Smart Skin Display was developed to be 8 μm in diameter and 30 μm in depth based on the findings of this experiment.

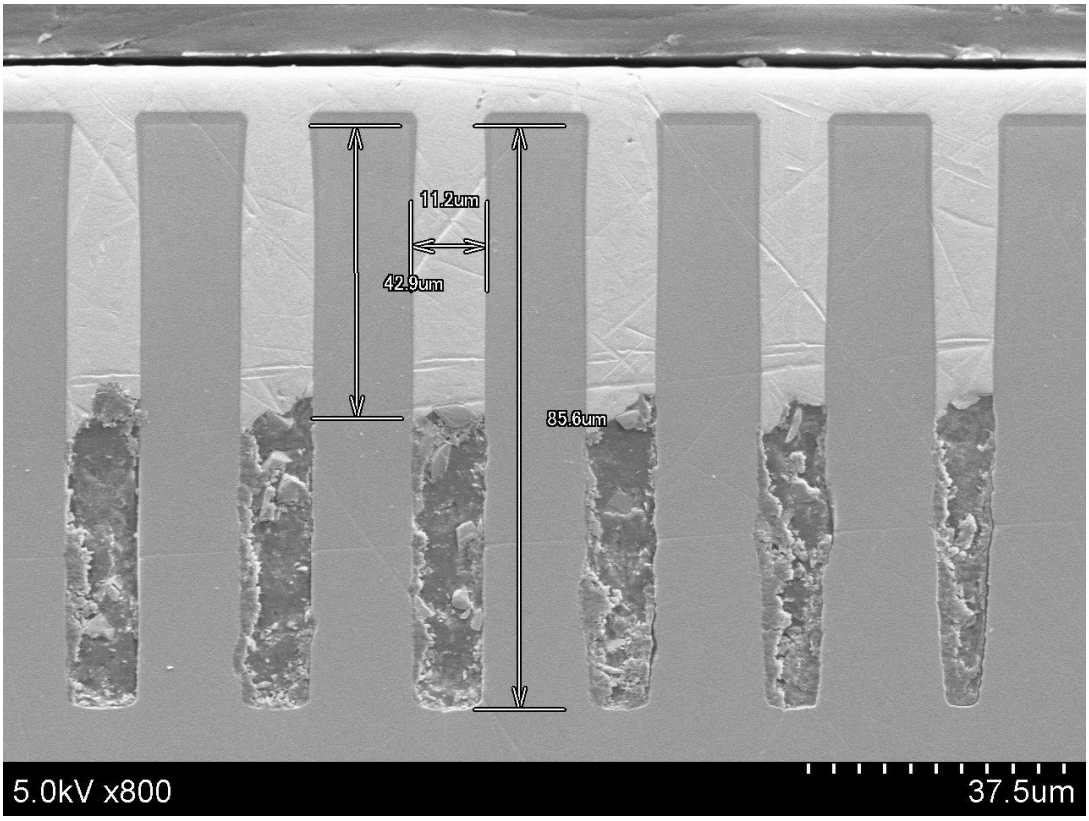


Fig. 4-15 SEM of high aspect ratio TSV.

4.4 3D-IC chip design and specification for Smart Skin Display

This paper describes an LSI dielet that incorporates LED driving circuits, a reflected light sensor, and other components for Smart Skin Display. This dielet was made using TSMC 0.18-micron technology. In Fig. 4 16, the LSI dielet's layout is depicted. Fig. 4 17 also displays the block diagram of the pixel circuit.

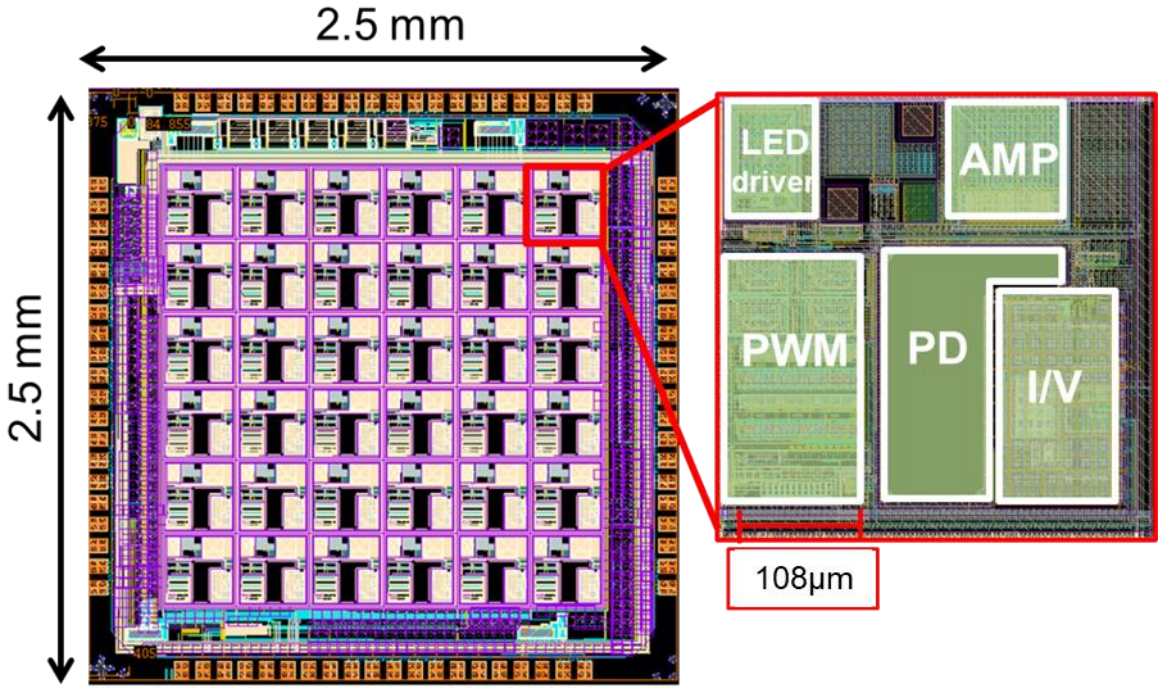


Fig. 4-16 Layout of LSI dielet

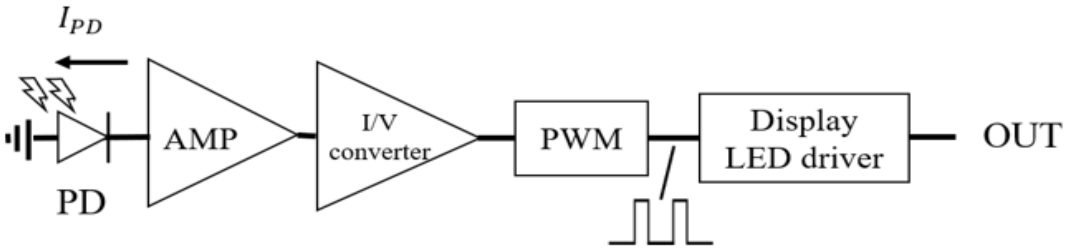


Fig. 4-17 Block diagram of pixel circuit

Infrared and red light is irradiated from the mini-LED to the body, and the photodiodes receive the reflected light. The light-receiving element's modest current is amplified by a current amplifier, and at the last stage an I/V converter with an offset voltage of 0.9 V input converts the amplified current to a voltage. A pulse signal with a duty ratio proportional to the amount of

reflected light received by the photodiodes is generated by feeding the obtained voltage into the pulse width modulation (PWM) circuit in the following stage to control the LED brightnesss. The input voltage is determined as in Equation (4-1).

$$Vin = 0.90(V) + I_{PD} * 256(k\Omega) * 160(k\Omega) \quad (4\text{-}1)$$

The two most commonly used brightness control methods are pulse amplitude modulation, which changes the amplitude of the pulse, and PWM, which changes the duty ratio of the pulse. Although light bulbs still produce light even at input voltages below their authorized levels, it is challenging to regulate the brightness of LEDs by voltage due to the rapid change in relative luminous flux with voltage. Therefore, this LSI adopted the PWM as the driving pulse control method for showing micro-LEDs.

This device has two modes for showing blood vessels. One is the binary mode. In this mode, one reference voltage (Vref_low) is used. When the input voltage is larger than Vref_low, a pulse signal with a duty ratio of 10% is output, and when the input voltage is less than Vref_low, no signal is output. The indication LEDs on the blood vessels do not light up as a result, but those placed where there are no blood vessels do light up brightly

The other is the “depth dimming mode,” in which the display LED can be dimmed in four steps according to the depth of the blood vessel. Three reference voltages (Vref_0, Vref_1, and Vref_2) are used in this mode. When the input voltage is larger than Vref_2, a pulse signal with a duty ratio of 7% is output, and when the input voltage is between Vref_1 and Vref_2, a pulse signal with a duty ratio of 3% is output. When the input voltage is between Vref_0 and Vref_1, a pulse signal with a duty ratio of 1% is output. When the input voltage is less than Vref_0, no signal is output. This state is defined as a duty ratio of 0%. The relative light absorption against the depth of blood vessels is depicted in Fig. 4-18 [42]. Red light is absorbed by blood vessels, hence there is little reflection in the area of shallow vascular depth. In contrast, the amount of

reflected light in the region of deep vascular depth is high. As a result the indicator LED on the blood vessel closest to the skin does not light up, the indicator LED on the next deepest blood vessel lights up with a slight brightness, and the indicator LED on the next deepest blood vessel lights up slightly brighter than that. The non-vessel locations have the brightest indicator LED illumination

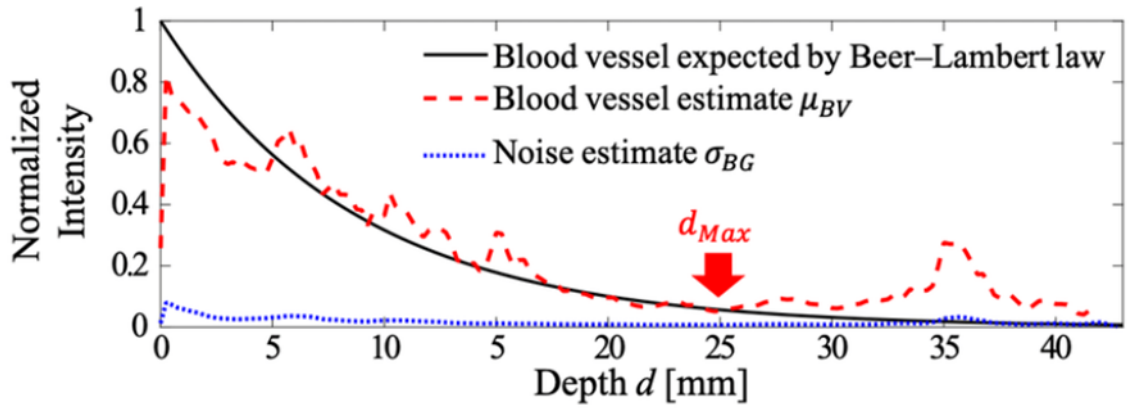


Fig. 4-18 Relative light absorption and blood vessel depth[42].

There were imaging tests done. A red LED was lighted from above to cast a shadow on the pixel array while a thread was stretched over the LSI dielet and an acrylic plate was attached to it to avoid oxidationy. vref_0, vref_1, and vref_2, were input from a reference voltage generation circuit in the same chip, and vref_low was Vref_low was input from an external voltage source. In the same way, the CLK and Reset signals were also input from an external signal generator. A 1 kΩ resistor, simulating a display LED, was connected to the output of the LED drive circuit of each pixel, and the cathode part was measured with an oscilloscope. Fig. 4-19 depicts the measurement system.

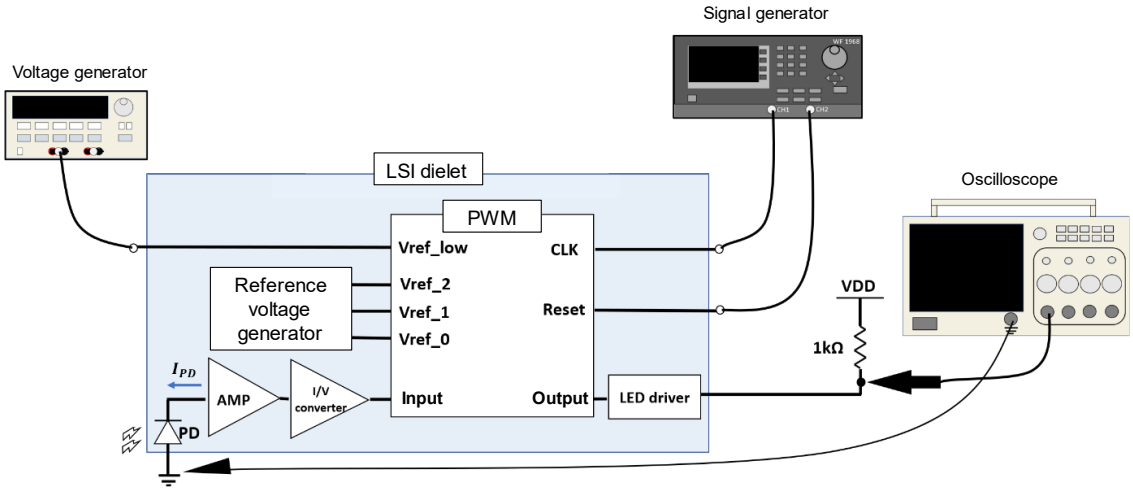
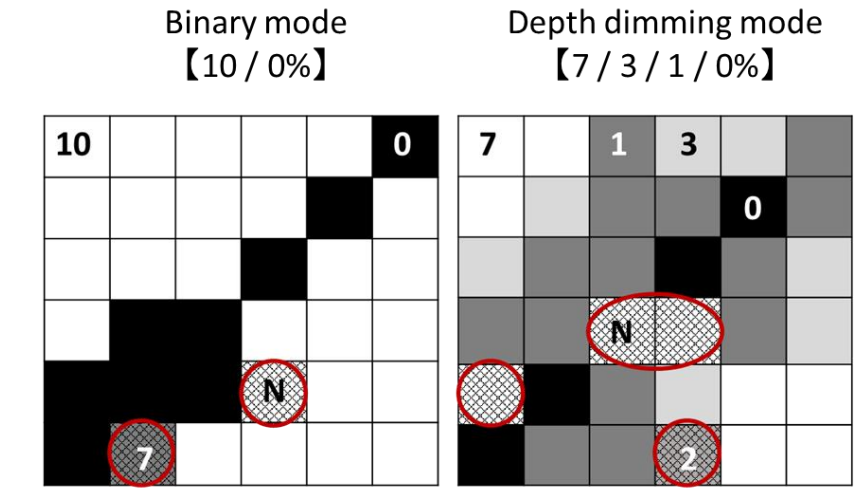


Fig. 4-19 Measurement experiment of LSI dielet

Fig. 4-20 shows the imaging results of the LSI dielet in each mode, and Fig. 4-21 and Fig. 4-22 illustrate the pulse signals measured in each mode. Duty ratios of 10% and 7% were observed in each mode for the pixels that were illuminated the most, and 0% for the pixels that were protected by the thread. In the depth dimming mode, duty ratios of 3 % and 1 % were observed depending on the light exposure. However, a duty ratio that shouldn't be output was seen in both modes (7% in binary mode and 2% in depth dimming mode), together with a big noise waveform, as illustrated in the red frame in Fig. 4 20. These issued have been confirmed and will be improved in the successor chip currently being prototyped.



Numbers in the box: Duty ratio of the measured waveform (%)
N: Noise

Fig. 4-20 Imaging result of LSI dielet

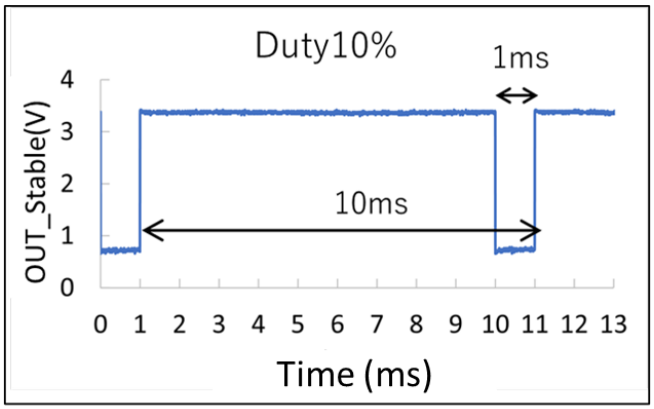


Fig. 4-21 Output signal of binary mode.

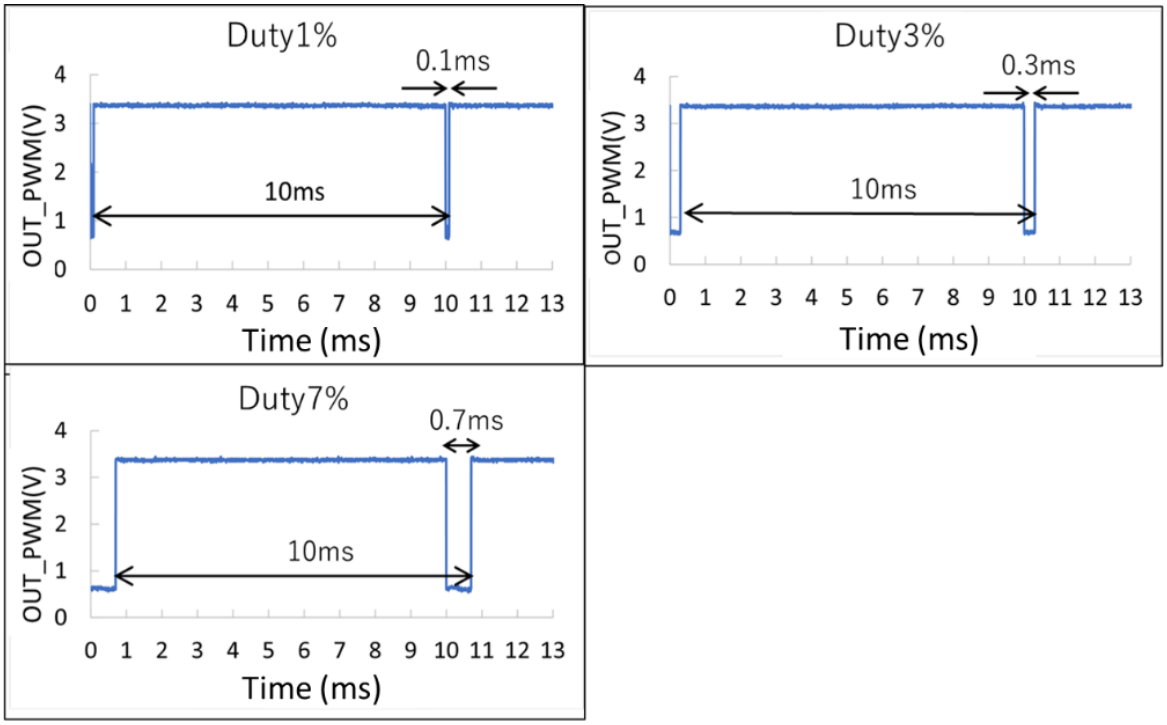


Fig. 4-22 Output signal of depth dimming mode.

4.5 Process integration of via-last TSV formation and micro-LED stacking

This section describes the fabrication of a 3D-IC and the stacking of micro-LEDs and the 3D-IC [43]. The 3D-IC was fabricated with the through-last/back-side Cu-TSV process, as shown in Fig. 4-23. First, an LSI dielet was bonded on a support wafer using a temporary adhesive. After that, mechanical grinding and CMP were used to thin the LSI. Then, via-holes were formed to contact the wiring layer of the LSI dielet. Following this, the SiO_2 liner was deposited by plasma-enhanced chemical vapor deposition (PE-CVD). Here, the deposition gases and temperature were O2, TEOS, and 200 °C, respectively. Via-holes were electroplated with Cu after the Ti barrier and Cu seed layer deposition. The overburdened Cu was removed by wet etching after resist patterning on TSV. Finally, the barrier/seed layer and resist were removed.

Fig. 4-24 shows the process flow of electroplated Cu direct bonding with incoming micro-LEDs.The the100-μm-square micro-LEDs have a 6-μm-thick active GaN layer and approximately 100-μm-thick sapphire substrate. The micro-LEDs were adhered face-down on a dicing tape (non-UV type Elep HolderTM V-series, Nitto). First, the sidewalls of the micro-LEDs singulated by laser cutting were insulated with a 100-nm-thick SiO2 layer deposited by room-temperature OER-SiO2-CVD with TEOS (tetraethoxysilane) (Meiden Nano process Innovation) at the dicing-tape level. Since so-called blue tapes were consisting of a glue layer and base film, a part of the GaN layer was covered with glue: here, the thickness was 10 μm. Before OER-SiO_2-CVD, an ashing process was added to completely expose the GaN sidewall to etch off the glue. The exposed glue layer was removed by O2 plasma (300 W/10 min). In contrast, Ti/Au (15/500 nm) wirings were created on the host thin 3D-IC using sputtering and conventional photolithography with wet etching. Subsequently, Ti/Cu (15 nm/200 nm) as a seed layer was deposited on the wirings with the sputtering system. By using photolithography and wet etch processes, the seed layer was then partially removed in 170-μm-long short line to divide the p- and n-type Au electrodes of the micro-LEDs to be mounted. After that, a photosensitive resin was patterned on the seed layer to open the growth areas (each aperture area: 67.5 x 67.5 μm) for the following Cu plating to interconnect the micro-LEDs with the substrates. During the electroplating process, the photosensitive resin also served as a temporary sticky coating to keep the micro-LEDs in place. The 6 x 6 arrays of the micro-LEDs were arranged in a design with an inter-LED space of 200 μm, and the micro-LED arrays were further arrayed in 5 x 5 3DIC blocks (inter-block space 500 μm). The total number of micro-LED was 900 (30 x 30) pieces. After the micro-LEDs were temporarily fixed at room temperature with a high-speed pick-and-place tool with a tacking force of 10 N for each, an additional compressive force of 10 N was correctively applied using a wafer bonder (EV520, EVG) at 70°C under an atmospheric pressure to compensate the LED tilt. The thicknesses of the

spin-on photosensitive resin were 7 μm and 5 μm before and after the compression processes. Cu pillars were grown by the electroplating process to give an electrical connection with the Au electrodes on the top of the micro-LEDs. Finally, the photosensitive resin was stripped off, and then, the Ti/Cu seed layer was etched off. The resulting micro-LEDs interconnected with the Ti/Au wirings formed on the 3D-IC were characterized using a manual prober.

As shown in Fig. 4-25, the 6 x 6 micro-LED dielets are effectively constructed the thin 3D-IC having TSV without experiencing mechanical damage such as microcracks.As seen from Fig. 4-26, Cu-TSV can be created w ithout any voids and a seam. Bottom-up electroplated Cu is fully filled with a standard PVD without substrate RF bias. The thinned chip thickness is 40 μm as well as the multi-level metallization layer thickness of nearly 10 μm and thinned Si thickness of approximately 30 μm that is given by temporary bonding with a thermally stable adhesive and the subsequent mechanical thinning and Si-CMP. The mechanically harsh process of grinding produces no edge chipping and crack, and final stress relief process of CMP enhances the reliability of the thin and brittle 3D-IC dielet.

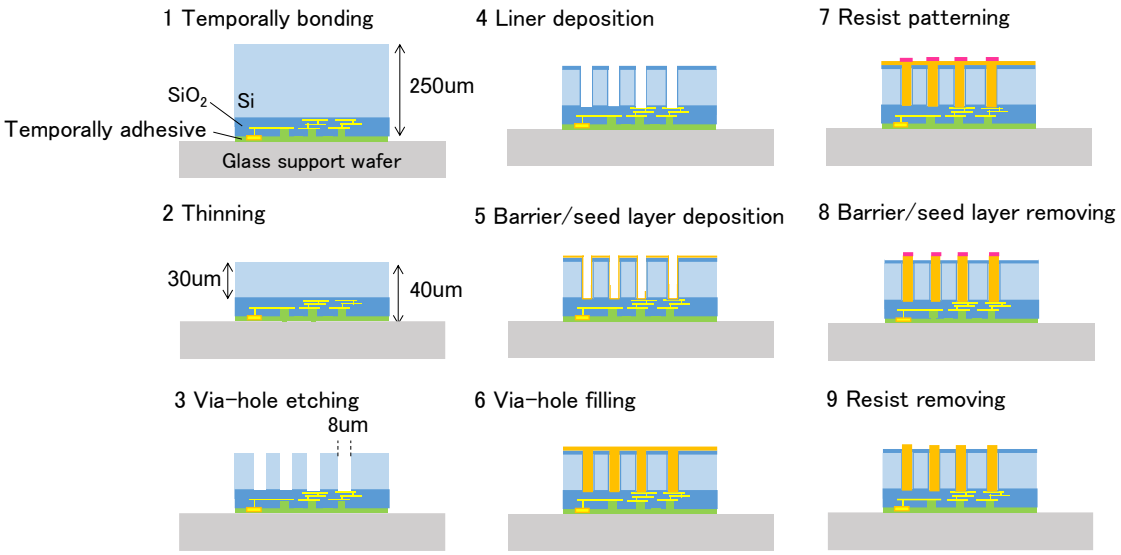


Fig. 4-23 Process flow of 3D-IC dielet

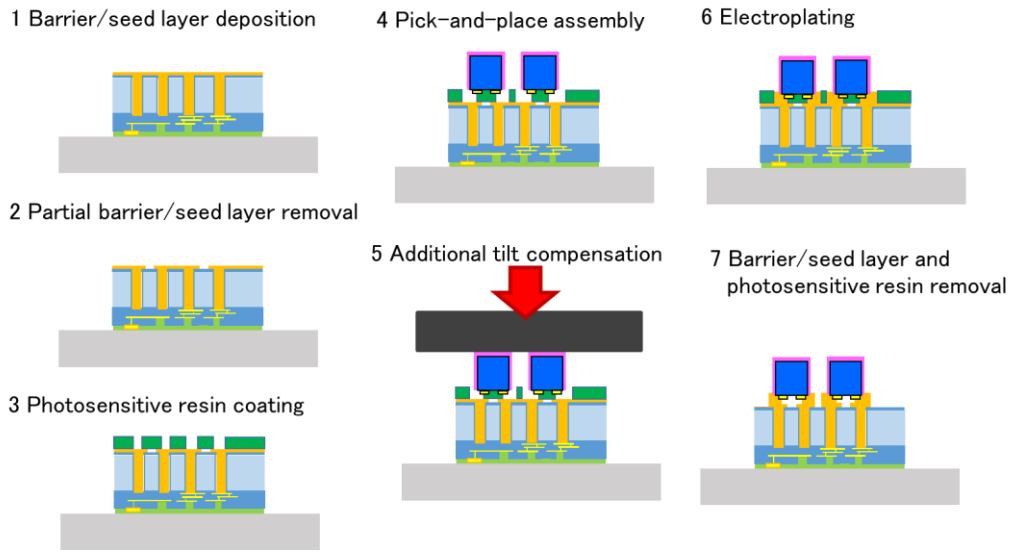


Fig. 4-24 Process of 3D integration with micro-LED

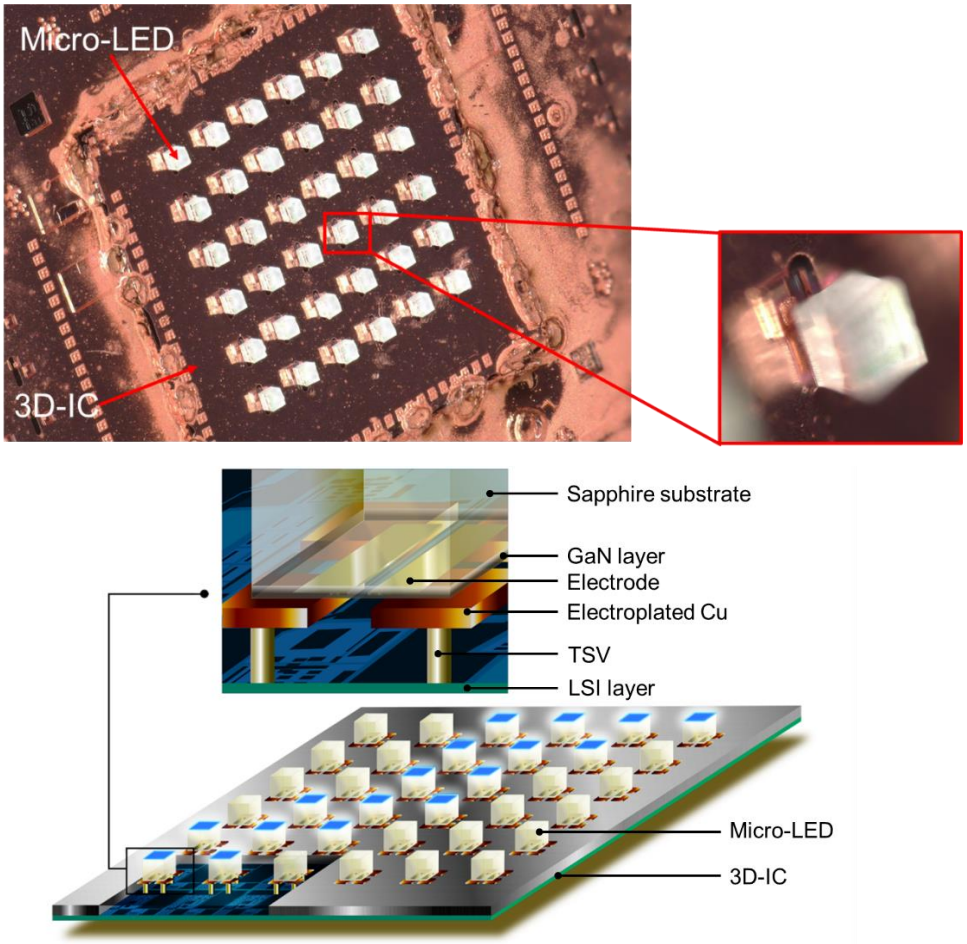


Fig. 4-25 A photomicrograph and schematic of micro-LEDs stacked on a thin 3D-IC dielet

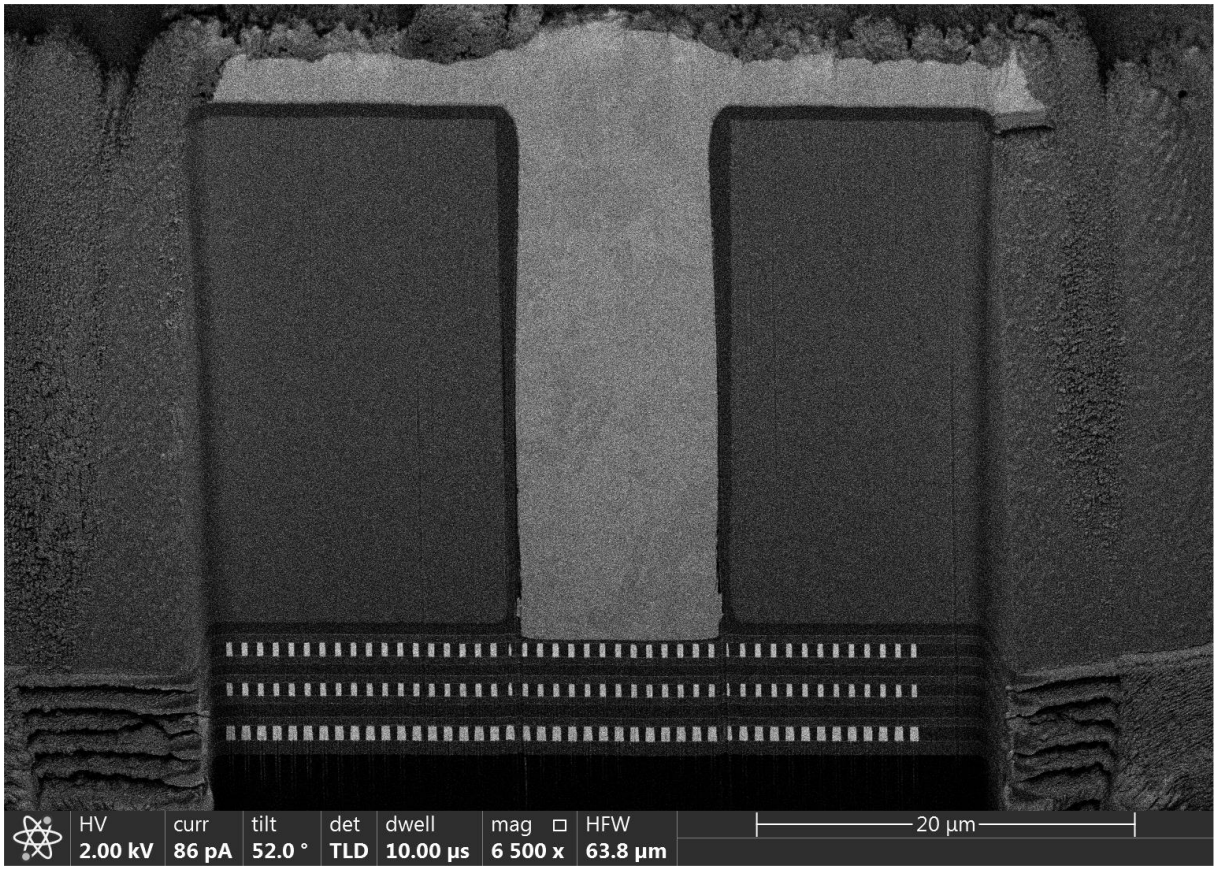


Fig. 4-26 A cross-sectional SEM image of Cu-TSV formed with a standard PVD

4.6 Evaluation of micro-LED stacked on 3D-IC

The micro-LEDs on the 3D-IC are depicted in the figure with the voltage applied and the light emitted. Also shown in the figure, are the electrical characteristics outcomes of the micro-LEDs. These outcomes indicate that the micro-LEDs could be stacked on the 3D-IC without degradation. The figure illustrates the findings of the electrical characteristics evaluation through two TSVs in the fabricated 3D-IC. Since TSV are connected to the wiring layer of the 3D-IC, it can be claimed that the 3D-IC was successfully fabricated without defects.

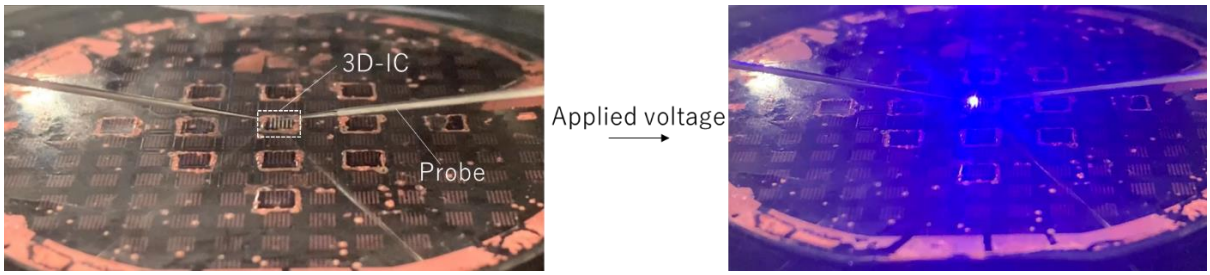


Fig. 4-27 Luminescent micro-LEDs on the 3D-IC

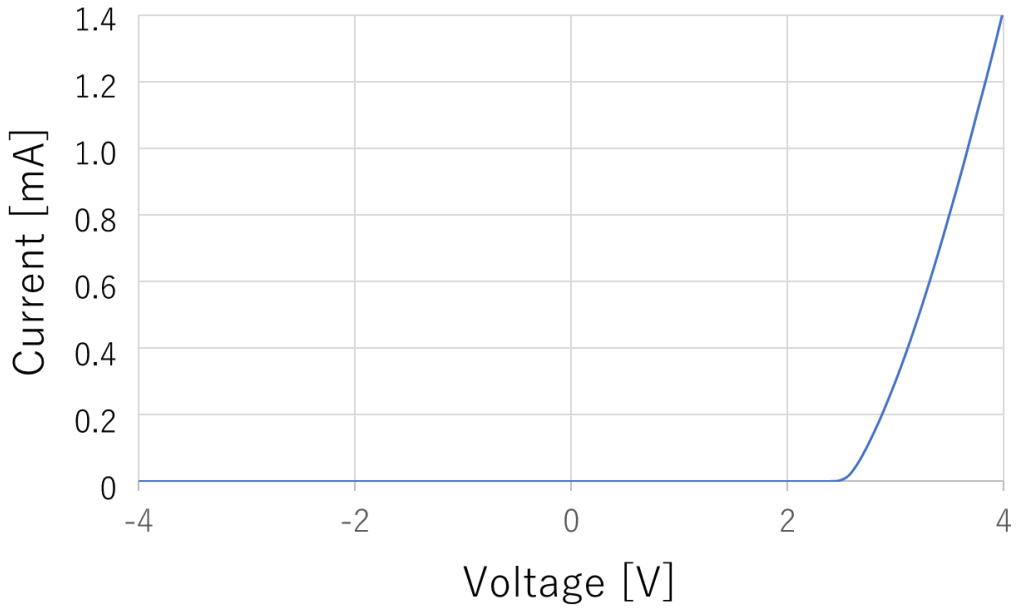


Fig. 4-28 Electrical characteristics of a micro-LED on the 3D-IC

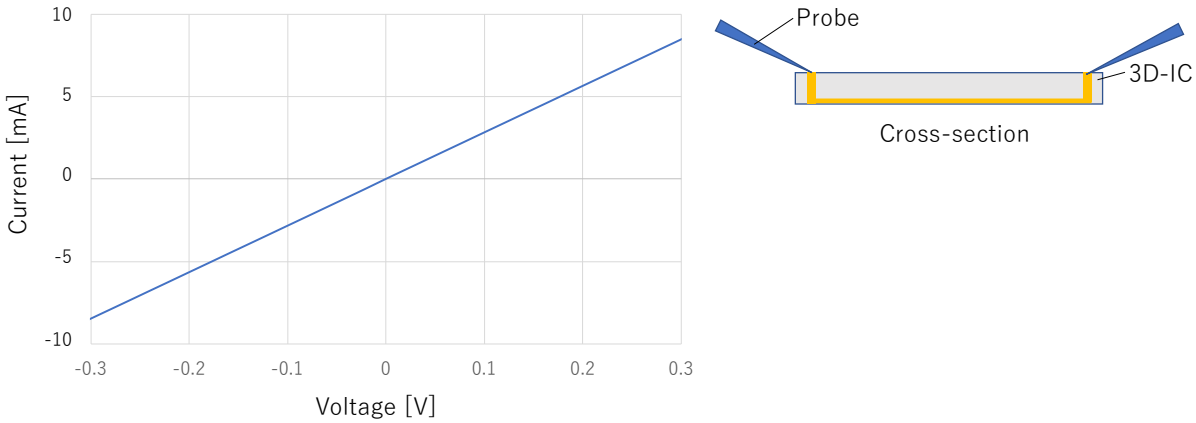


Fig. 4-29 Electrical characteristic of a pair of TSV in 3D-IC

4.7 Conclusion

High capability of standard PVD is confirmed by bottom-up electroplated Cu filling into deep Si holes created by Bosch etch, which provides step coverage evaluation. When sample tilt control and centering of the sample wafers with metal targets are used, the step coverage increases and a fully-filled Cu-TSV with a diameter of 10 μm and a depth of 30 μm (aspect ratio: ~3). Chip-to-wafer 3D integration without complex long-throw iPVD is used to show the low-cost and broadly applicable Via-last TSV manufacturing. The room-temperature Cu direct interconnect technology is developed to heterogeneously integrate micro-LEDs with 3D-IC for Smart Skin Display, which will be used as a wearable micro-LED display and sensors. Electroplated Cu direct bonding without solders and silver composites are applied to die-level 3D integration. Without experiencing any mechanical failure, a 6 x 6 micro-LEDs array is effectively layered on a thinned 3D-IC without mechanical failure. At room temperature, direct bonding and interconnection of the micro-LEDs without the need of solders were accomplished. The via-last TSVs were functioned well and the micro-LED emitted a blue light through the electroplated Cu without electrical damages. A feasibility study of heterogeneous micro-LED stacking on 3D-IC was

shown to give an excellent positive prospect to integrate Smart Skin Display.

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Chapter 5
Conclusion

In this thesis, structural design and creation of fabrication processes were implemented to create highly integrated flexible electronics with heterogeneous “dielets.” Dielets are originally tiny dies such as LED, MEMS, sensors, and passives and carry a broader concept of “chiplet” anticipated to be a technological key driver to accelerate Moore’s law size scaling in the semiconductor industry. Compared to traditional flexible devices in sheet-level processing such as 1) industrially used FPC with few bend parts, 2) ultra flexible devices using low-performance organic semiconductor and low-density printable wiring technologies, and 3) FHE with ultrathin dies susceptible to mechanical stress, my approach was based on wafer-level processing necessary to interconnect all the heterogeneous components called “dielets” integrated into the polymeric flexible substrates. In this research, die-first FOWLP with PDMS was employed to integrate the structurally new FHE. Polyimides (PIs) were greatly used in flexible devices, but the PIs were not cost-effective and had low adaptability. On the other hand, the elastomer PDMS was a highly flexible substance that flawlessly followed complicated 3D structures. Nevertheless, heterogeneous and 3D integration with high-density wirings on or in PDMS was difficult.

In Chapter 2, from the perspectives of integration and reliability, two technological issues in structurally new FHE were listed: The first was “die shift,” wherein tiny dielets had positioning errors due to a serious misalignment event caused by fuluidic force and thermomechanical stress given by PDMS molding. The die shift problem was limited after die placement by using an anchoring layer to cover the heterogeneous dielets. As a result, the die positioning accuracy was by several micrometers.

This result far exceeds the accuracy required for Smart Skin Display. The other issue was the mechanical stress of multi-level wiring of flexible devices when bending. Stress neutral axes were developed at the interlayer dielectric SU-8 between first and second layer wirings. As a result, the bendability was improved with a curvature radius of 2.5 mm or 1 mm. Additionally, during 1,000-cycles repeated bending, the wire resistances were maintained constant, or the resistance change was within 10%. This finding shows that the flexible multilayer wiring used in this research has sufficient durability to survive bending during the handling of Smart Skin Display. These findings indicate that the flexible multilayer wiring of this study has sufficient durability to survive bending when being handled by Smart Skin Display. These technological impacts contributed to further increasing the integration density and increasing the applicability to flexible devices that require smaller bending radii.

In Chapter 3, a room-temperature bonding and interconnect technology was developed for micro-LED stacking on wafers for Smart Skin Display. Electroplated Cu was controlled to interconnect Au electrodes formed on the micro-LEDs without solder and conductive composites (pastes/films) at room temperature. The low-temperature procedure gave no thermomechanical stress and alignment failure due to CTE mismatch. The resistance of the pillar created with the electroplated process was low enough to effectively operate the micro-LEDs well. Further design improvement was required, but a high prospect of achieving close to 100% was described. The other assembly with tiny dielets such as optics, MEMS, sensors, and passives, as well as so-called standard chiplets split from a sizable system on a large chip, could benefit from this approach (SoC).

In Chapter 4, a key issue in traditional die-level multichip-to-wafer 3D integration based on Via-last TSV was covered. Thus, I concentrated on a barrier/seed deposition process by PVD for TSV creation. In industry, TSVs are getting increasingly popular to rapidly increase the performance

of integrated microelectronic systems and are employed in CMOS image sensors, 3D-DRAM called HBM, Si interposers, and so forth, but the cost is still high. TSV was created using a highly costly (around 500 million yen or more) ultralong-through ionized PVD instrument with low-frequency substrate RF bias functionalities. Here, I employed a general-purpose industry-standard PVD (around 5 million yen or less). By centering and tilting wafer samples, the step coverage of the Ti barrier and Cu seed was assessed. Therefore, Cu-TSV, with an aspect ratio of less than 4, was successfully formed without voids and seams. Additionally, I fabricated a Cu-TSV 30 μm long and 10 μm in diameter, successfully stacked and integrated 36 (6 x 6) micro-LEDs on a 40 μm thick brittle 3D-IC without mechanical failure, and successfully operated the micro-LEDs.

Here, I provided a highly integrated FHE called “Smart Skin Display” as an example. It is made up of a number of 3D-IC islands on which a micro-LED array was layered and interconnected through TSV. This study illustrated the integration of the 3D-stacked micro-LED display on the 3D-IC. In order to build structurally innovative FHE based on dielet-on-wafer FOWLP with heterogeneous dielets were created. A room-temperature bonding and connecting method were suggested to enable the high-level heterogeneous 3D integration, and the concept was experimentally demonstrated in this study. This thesis had a technological impact on integration processes to efficiently interconnect all the heterogeneous dielets in lateral and vertical directions and a conceptual impact to improve the performance, functionality, and signal integrity of future flexible devices by utilizing a wafer-level packaging methodology.

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