Faculty of Electronic and Computer Engineering

OPTIMIZATION OF PROCESS PARAMETER VARIATION IN DOUBLE-GATE FINFET MODEL USING VARIOUS STATISTICAL METHODS

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DECLARATION

I declare that this entitled “Optimization of Process Parameter Variation in Double-Gate FinFET Model using Various Statistical Methods” is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature :.....

Name : Ameer Farhan Bin Roslan

Date : 29th March 2022

APPROVAL

I hereby declare that I have read this thesis and my opinion this thesis is sufficient in term of scope and quality for the award of Master of Science in Electronic Engineering.

Signature :.....

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Date : 29th March 2022

DEDICATION

To my beloved family members

To my supportive supervisor and co-supervisor

ABSTRACT

Double-gate FinFET is identified as a prospect in fulfilling the demands required in replacing the current conventional planar MOSFETs due to several advantages. Specifically in its scalability, reduced leakage current, high drive current, with steep subthreshold swing, subsequently improving the I_{ON}/I_{OFF} ratio, thus reducing the power consumption of the device. The susceptibility towards the electrical performance of the device is exposed due to the process parameter variations from the device miniaturization. This research work is aimed towards optimizing the process parameter variation towards the device characteristics with several appropriate statistical methods used. Taguchi statistical method, the Taguchi-based Grey Relational Analysis (GRA), the 2*k*-factorial method, and the Response surface method-central composite design (RSM-CCD) have all been utilized to analyze the performance of the device. ATHENA module of Silvaco TCAD is utilized in this simulation-based fabrication The threshold voltage (V_{TH}), drive current (I_{ON}), leakage current (I_{OFF}) and subthreshold swing (SS) ramifications towards the adjustment of six process parameter that include polysilicon doping dose, polysilicon doping tilt, Source/Drain doping dose, Source/Drain doping tilt, V_{TH} doping dose and V_{TH} doping tilt is studied. The effect of the said process parameter variations were analysed with the utilization of L_{25} orthogonal array (OA), main effects, signal-to noise ratio (SNR) and analysis of variance (ANOVA) for the Taguchi statistical method, the Taguchi-based GRA and the RSM-CCD. Meanwhile the L_{32} OA is utilized in the 2*k*-factorial method where 1/8 fraction design of experiment is used with each requires 64, 32, 16 and eight experiment runs respectively. This has made the L_{32} the nearest available in the 2*k*-factorial method to the L_{25} used in other statistical methods. The performance of the device is analyzed through the I_{ON} values along with I_{ON}/I_{OFF} ratio amongst the statistical methods used. The combination of Taguchi method and GRA is introduced to overcome the limitation of a standalone Taguchi method that can solve only a single response at a time into multi-response optimization for the 16 nm gate length of double-gate FinFET. The Taguchi-based GRA showcases the best improvements with 47.79% for the I_{ON}/I_{OFF} ratio as opposed to 45.39%, 20.54% and 23.01% for the Taguchi method, 2*k*-factorial and RSM-CCD respectively, with I_{ON} at 1656.27 μA/μm for the Taguchi based GRA. Meanwhile, the I_{OFF}, SS and I_{ON}/I_{OFF} ratio optimized at 34.498 pA/μm, 96.743 mV/decade, and 48.0113 M, respectively. The process parameters of 16 nm gate length double gate FinFETs were successfully optimized by using the L_{25} OA of Taguchi based GRA. Following that, a nominal V_{TH}, a high I_{ON} and a low I_{OFF} characteristics were all attained. These proved that the multi-response characteristics of the device can be optimized simultaneously through the implementation of the L_{25} OA of Taguchi based GRA. That said, the V_{TH}, I_{ON} and I_{OFF} value for both devices meet the International Technology Roadmap Semiconductor (ITRS) 2013 prediction for high performance and low power logic multi-gate technology.

PENGOPTIMUMAN VARIASI PARAMETER PROSES DALAM MODEL FINFET DWIGET MENGGUNAKAN KAEDAH STATISTIK PELBAGAI

ABSTRAK

Dwiget FinFET dikenalpasti sebagai prospek dalam memenuhi tuntutan yang diperlukan dalam menggantikan MOSFET planar konvensional semasa kerana beberapa kelebihannya seperti kebolehskalaan, pengurangan arus bocor, arus pemacu tinggi, dengan ayunan subambang yang curam, dan peningkatan nisbah I_{ON} / I_{OFF}, serta pengurangan penggunaan kuasa peranti. kebolehrentanan terhadap prestasi elektrik peranti terdedah kerana variasi parameter proses dari pengecilan peranti. Kajian pengecilan ini bertujuan untuk mengoptimumkan variasi parameter proses terhadap ciri-ciri peranti dengan beberapa kaedah statistik yang sesuai yang digunakan iaitu melalui Kaedah Statistik Taguchi, Analisis Hubungan Grey (GRA) berdasarkan Taguchi, Kaedah Faktorial 2k, dan Kaedah Permukaan Respon-reka Bentuk Komposit Pusat (RSM-CCD) bagi menganalisis prestasi peranti. Modul ATHENA Silvaco TCAD digunakan dalam fabrikasi berasaskan simulasi ini. Voltan ambang (V_{TH}), arus pemacu (I_{ON}), arus bocor (I_{OFF}) dan ramalan ayunan subambang (SS) ke arah penyesuaian enam parameter proses yang merangkumi dos endapan polisilikon, kecondongan endapan polysilicon, dos endapan Sumber / Saliran, kecondongan endapan Sumber / Saliran, dos endapan V_{TH} dan kecondongan endapan V_{TH} dikaji. Kesan dari variasi parameter proses tersebut dianalisis dengan penggunaan tatasusun ortogon L_{25} (OA), efek utama, nisbah isyarat ke kebisingan (SNR) dan analisis varians (ANOVA) untuk kaedah statistik Taguchi, kombinasi Taguchi-GRA dan RSM-CCD. Sementara itu L_{32} OA digunakan dalam kaedah 2k-faktorial di mana 1/8 reka bentuk pecahan eksperimen digunakan dengan masing-masing memerlukan 64, 32, 16 dan lapan eksperimen telah dijalankan. Ia menjadikan kaedah L_{32} paling hamper berbanding kaedah 2k-faktorial yang tersedia kepada L_{25} yang digunakan dalam kaedah statistik lain. Prestasi peranti dianalisis melalui nilai I_{ON} bersama dengan nisbah I_{ON}/I_{OFF} antara kaedah statistik yang digunakan. Kombinasi kaedah Taguchi dan GRA diperkenalkan untuk mengatasi batasan kaedah Taguchi yang berdiri sendiri dalam menyelesaikan hanya satu respon pada satu masa menjadi pengoptimuman multi-respon bagi 16 nm Dwi-get FinFET. GRA berasaskan Taguchi menunjukkan peningkatan terbaik dengan 47.791% untuk nisbah I_{ON}/I_{OFF} berbanding 45.395%, 20.544% dan 23.001% untuk kaedah Taguchi, 2k-faktorial dan RSM-CCD masing-masing, dengan I_{ON} pada 1656.27 μA/μm untuk GRA berasaskan Taguchi. Manakala nilai I_{OFF}, SS dan nisbah I_{ON}/I_{OFF} dioptimumkan masing-masing pada 34.498 pA/μm, 96.743mV/dekad, and 48.0113 M. Parameter proses FinFET panjang get 16 nm berjaya dioptimumkan dengan menggunakan L_{25} OA GRA berasaskan Taguchi, dengan mencapai V_{TH} nominal, I_{ON} tinggi dan ciri I_{OFF} rendah. Ini membuktikan bahawa ciri multi-tindak balas peranti dapat dioptimumkan secara serentak melalui pelaksanaan L_{25} OA dari GRA berasaskan Taguchi di mana nilai V_{TH}, I_{ON} dan I_{OFF} untuk kedua-dua peranti memenuhi ramalan International Technology Roadmap Semiconductor (ITRS) 2013 untuk prestasi tinggi dan kuasa rendah teknologi multi-get logik.

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LIST OF ABBREVIATIONS

Adeq Precision	-	Adequate Precision
Adj R-Squared	-	Cumulative Distribution Function
ANOVA	-	Analysis of variance
CCD	-	Central Composite Design
CMOS	-	Complementary Metal Oxide Semiconductor
CPU	-	Central Processing Unit
C.V.	-	Coefficient of Variation
DIBL	-	Drain Induced Barrier Lowering
DF	-	Degree of Freedom
DoE	-	Design of Experiment
EOT	-	Equivalent Oxide Thickness
FD	-	Fully Depleted
GRC	-	Grey Relational Coefficient
GRG	-	Grey Relational Grade
HP	-	High Performance
IC	-	Integrated Circuit
ITRS	-	International Technology Roadmap Semiconductor
LP	-	Low Power
MOSFET	-	Metal-oxide-semiconductor Field Effect Transistor
MG	-	Multi-gate

MS	-	Mean Square
NMOS	-	n-channel MOSFET
NTRS	-	National Technology Roadmap for Semiconductors
OA	-	Orthogonal Array
ORI	-	Oblique Rotating Implantation
PD	-	Partial Depleted
PMOS	-	p-channel MOSFET
Pred R-Squared	-	Predicted R-Squared
PRESS	-	Predicted Residual Sum of Squares
RAM	-	Random Access Memory
RSM	-	Response Surface Methodology
S/D	-	Source/Drain
SCE	-	Short Channel Effect
SIA	-	Semiconductor Industry Association
SNR	-	Signal-to-noise ratio
SOI	-	Silicon on Insulator
SS	-	Subthreshold Swing
SSQ	-	Sum of squares
TCAD	-	Technology Computer-aided Design
NTRS	-	National Technology Roadmap for Semiconductors

LIST OF PUBLICATIONS

The research papers produced and published during the course of this research are as follows:

Journals (As First Author)

1. Roslan, A.F., Salehuddin, F., Zain, A.S.M., Kaharudin, K.E., et al., 2018. 30nm DG-FinFET 3D construction impact towards short channel effects. In *Indonesian Journal of Electrical Engineering and Computer Science*, 12(3), pp. 1358-1365 (Cited Scopus).

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