IJRCS

International Journal of Robotics and Control Systems
Vol. 3, No. 3, 2023, pp. 510-529
ISSN 2775-2658
http://pubs2.ascee.org/index.php/ijrcs

ASCEE

Power Quality Improvement using a New DPC Switching Table for a Three-Phase SAPF

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ARTICLE INFO

Article History
Received May 12, 2023
Revised June 17, 2023
Accepted July 22, 2023

Keywords
Shunt active power filter;
Power quality improvement;
New DPC switching table;
Harmonics reduction;
IEEE 519-1992

ABSTRACT

This research focuses on the analysis and design of robust direct power control (DPC) for a shunt active power filter (SAPF). The study proposes a novel switching table design based on an analysis of the impact of inverter switching vectors on the derivatives of instantaneous reactive and active powers. The goal is to reduce the number of commutations by eliminating null vectors while maintaining the desired DC-bus voltage using a PI regulator-based anti windup technique. Additionally, a robust PLL structure-based band pass multivariate filter (BPMVF) is utilized to enhance the network voltage. The research demonstrates the effectiveness of the suggested power control through extensive simulation results, showing high performance in both transient and steady-state conditions. The proposed approach offers the advantages of sinusoidal network current, and unitary power factor, and eliminates the need for current regulators and coordinate transformations or PWM generators. Further research directions could explore the practical implementation and real-world performance of this technique in power systems.

1. Introduction

The quantity of non-linear loads causes a significant reduction in the quality of the energy. As a result, the development of harmonic components and reactive power has the potential to contaminate the interconnection network. Authors in [1] used transformer-less SAPF with ANFIS supervised PID controllers. They can lead to imbalances in three-phase systems by generating excessive currents in the neutral. These excessive currents, the injected harmonics, the presence of reactive power, the unbalances and other problems generated by this type of load lead to a weakening of the system's overall efficiency and of the power factor. They are also the cause of consumer disruptions and interference in nearby communication networks [2][3].

Many active filter solutions for the electrical networks depollution have been suggested in the literature. Those that best encounter today's industrial coercions are active parallel [4][5] or series filters [6][7] and active parallel-series combinations, also called Unified Power Quality Conditioners (UPQCs) [8][9]. In the case where the network currents are nonlinear, the Shunt Active Power Filters

(SAPFs) are regarded the optimal solution for the current harmonic reduction in low to medium power applications [10]. In [11], a real-time implementation of SAPF with reduced sensors is presented. Active filtering is more advantageous where a fast response is required in the presence of dynamic loads. In addition, APF represents a powerful tool for general-purpose conditioning as it is able to compensate for reactive power and load imbalance as well. Authors in [12] presents the modelling of a PI-controlled SAPF for power quality improvement-based on P-Q theory.

The basis of direct control has been developed in many appliances. The goal was to get rid of the modulator block and the internal current loop by changing them with a switching table whose inputs are the margins between the reference values and the measurements. The prime developed application was aimed at controlling an electrical motor and the control structure is famous as Direct Torque Control (DTC) [13][14]. In this situation, the motor torque and flux are regulated without any modulation block. Thereafter, a direct power control (DPC) technique was suggested by Noguchi for a grid-connected rectifier control application. In this situation, the regulated variables are the instantaneous reactive and active powers [15].

With the DPC there is no inner current regulation or PWM block, since the inverter switching states, for every sampling time period, are picked from a switching table, based on the instantaneous margin between the reference values and those of the reactive and active powers, and the network voltage vector angular position. With this control law, the DC-bus voltage is controlled for active power control and unity power factor is achieved by clamping the reactive power to zero [16].

Many papers, on PWM rectifiers and a few on active power filters, straight operated the DPC conventional switching table. Whereas, neatly looking at this switching table, it can be noted that for all odd sectors, when the active power error varies, the switching vector stays unchanged which is inconvenient. The same remark can be observed for reactive power and even sectors. Thus, this proves the conventional switching table limitation. Many tests were carried out on the proposed control method. Simulation results show the main advantages for the improvement of power quality and its high performance getting a sinusoidal network current, unity power factor, and robust control of the DC-bus voltage in steady state and transient [17].

The suggested switching table is based on the analysis of the impact of VSI voltage vectors and their position on the variation of instantaneous power. The proposed research has many benefits in power quality improvement, such as achieving a sinusoidal network current, unity power factor, and robust control of the DC-bus voltage in steady-state and transient conditions.

This research aims to enhance the conventional DPC performance by replacing the classic switching table with a robust one. The suggested switching table is obtained by analysing the impact of the VSI voltage vectors and their position on the instantaneous power change: (1) Amelioration of instantaneous power variation from the SAPF electrical model (2) Planning of a different switching table based on the investigation of the reactive and active power variation behaviour for various voltage vectors in the twelve sectors.

This paper is structured as follows: Section 1 introduces the topic and the literature review. Section 2 details the classical and proposed PLL structure. Section 3 analyzes the proposed robust anti-wind-up DC-bus voltage regulator. Section 4 illustrates the basic DPC for SAPF. Section 5 explains the proposed switching table concept. Section 6 presents the simulation environment and the discussion of the results. Finally, Section 7 concludes the paper.

2. Robust PLL Structure

2.1. Classical PLL

The Phase Lock Loop (PLL) is a key element in new control techniques in power electronics. It is used as a way to retrieve phase and frequency information [18][19]. The fundamental PLL form is

shown in Fig. 1, having a Phase Detector (PD), a Loop Filter (LF) which is generally a PI controller, and a Voltage Controlled Oscillator (VCO). Several techniques of PLL have been developed, Fig. 2 represents the full block diagram of the classic PLL.

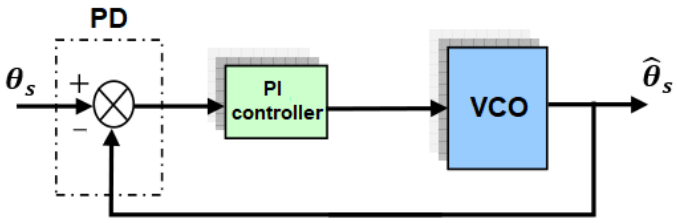


Fig. 1. Synoptic of the Classic PLL

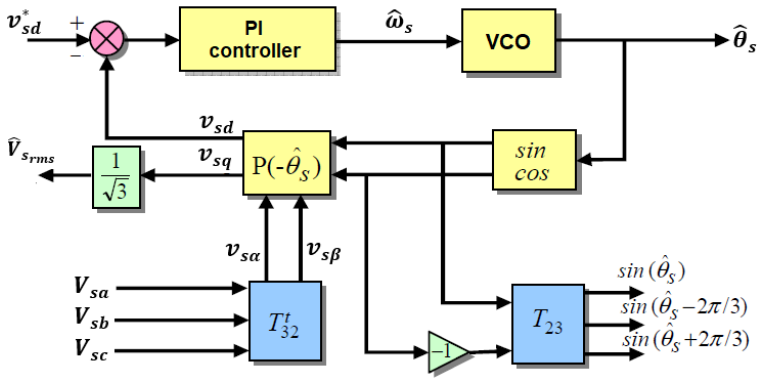


Fig. 2. A Detailed Synopsis of the Classic PLL

The phase-to-neutral grid voltages $V_{s_{abc}}$ are given by:

$$\begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} = \begin{bmatrix} \sqrt{2}V_{s_{rms}} cos(\theta_s) \\ \sqrt{2}V_{s_{rms}} cos(\theta_s - \frac{2\pi}{3}) \\ \sqrt{2}V_{s_{rms}} cos(\theta_s + \frac{2\pi}{3}) \end{bmatrix} \tag{1}$$

where θ_s=$\omega_s t$, ω_s, and $V_{s_{rms}}$ are the phase angle, the fundamental voltage pulsation, and grid-voltage rms value. The Concordia transformation that allows to pass from a 3-phase to the equivalent 2-phase in a coordinate system (α-β) is:

$$\begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} = \begin{bmatrix} \sqrt{3}V_{s_{rms}} sin(\theta_s) \\ -\sqrt{3}V_{s_{rms}} cos(\theta_s) \end{bmatrix} \tag{2}$$

These quantities can be obtained in the synchronously rotating frame by applying the following Park transformation:

$$\begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} = \begin{bmatrix} cos(\hat{\theta}_s) & sin(\hat{\theta}_s) \\ -sin(\hat{\theta}_s) & cos(\hat{\theta}_s) \end{bmatrix} \begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix} \tag{3}$$

When the phase error θ_s-$\hat{\theta}_s$ is small, then (3) will be:

$$v_{sq} = -\sqrt{3}V_{s_{rms}}(\theta_s - \hat{\theta}_s) \tag{4}$$

The PLL will be locked when the estimated angle $\hat{\theta}_s$ is equal to θ_s, then v_{sq}=0. Basing on Fig. 1, the estimated pulsation $\hat{\omega}_s$ is given by:

$$\hat{\omega}_s = FLF(s)(\theta_s - \hat{\theta}_s) \tag{5}$$

where *FLF(s)* is the filter loop (PI controller), which is formulated in this case by the next transfer function:

$$FLF(s) = K_{pp} + \frac{K_{ip}}{s} = K_{pp}(\frac{1+\tau_{ip}s}{\tau_{ip}s}) \tag{6}$$

τ_{ip}=$\frac{K_{pp}}{K_{ip}}$, K_{pp}, and K_{ip} are positive real parameters design. Afterward the angular position $\hat{\theta}_s$ at the VCO output becomes:

$$\hat{\theta}_s = \frac{1}{s}\hat{\omega}_s \tag{7}$$

In goal to determine the parameters of the PI regulator, the synoptic of Fig. 2 can be oversimplified to be identical to that of Fig. 1 as it appears on the diagram of Fig. 3.

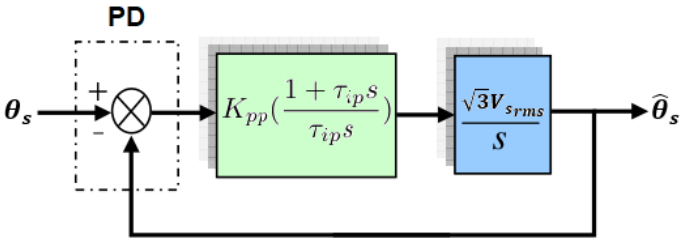


Fig. 3. Simplified Diagram of the PLL

The system closed-loop transfer function is:

$$\frac{\hat{\theta}_s}{\theta_s} = \frac{\sqrt{3}V_{s_{rms}}K_{pp}(\frac{1+\tau_{ip}}{\tau_{ip}s})\frac{1}{s}}{1+\sqrt{3}V_{s_{rms}}K_{pp}(\frac{1+\tau_{ip}}{\tau_{ip}s})\frac{1}{s}} \tag{8}$$

The found transfer function can be identified with the general system of the second order given by:

$$F(s) = \frac{\hat{\theta}_s}{\theta_s} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{9}$$

FLF(s) parameters are expressed as follows:

$$\begin{cases} K_{pp} = \frac{2\zeta\omega_n}{\sqrt{3}V_{s_{rms}}} \\ \tau_{ip} = \frac{2\zeta}{\omega_n} \end{cases} \tag{10}$$

In goal to get a good compromise between stability and dynamic performance, the following values are retained: ζ=0.707, K_{pp}=1.07, K_{ip}=237.7, and τ_{ip}=$4.5.10^{-3}$ seconds.

2.2. The Proposed PLL Structure-Based BPMVF

There are several methods to overcome the identified problems, among them, we cite PLL based on RST regulators [20], fuzzy logic [21][22], neural networks [23], or Adaline networks [24]. All these methods respect a compromise between good dynamics and insensitivity to disturbances of the network voltage. The solution adopted in our work lies in the use of a multi-variable filter ensuring the decoupling between the sensitivity to load variations and the dynamic performances. To prove the effectiveness of the new structure, we will first study the performance of the filter and then the behavior of this new PLL structure by making a comparison with the classical structure evaluated previously. Then, the robustness of the new PLL is validated. Hence, the ultimate expression of the

structural form of the Band Pass Multi-Variable Filter (BPMVF) which is introduced in the PLL is [25][26]:

$$\begin{cases} \hat{v}_{s\alpha} = \frac{k_c}{s}[v_{s\alpha} - \hat{v}_{s\alpha}] - \frac{\omega_c}{s}\hat{v}_{s\beta} \\ \hat{v}_{s\beta} = \frac{k_c}{s}[v_{s\beta} - \hat{v}_{s\beta}] - \frac{\omega_c}{s}\hat{v}_{s\alpha} \end{cases} \tag{11}$$

where ω_c and k_c are tuning gains. The transcription is elaborated in the block diagram in Fig. 4.

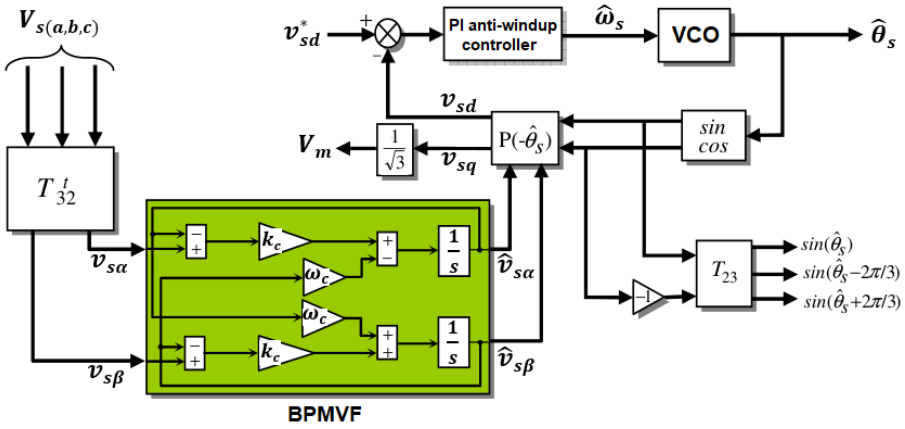


Fig. 4. Diagram of the New Structure of PLL with the BPMVF

3. DC-Bus Controller-Based Anti-Windup

In this section, we will synthesize the DC-bus voltage regulator in such a manner that the DC voltage error as small as possible. The considered controller consists of an anti-windup PI developed on the base of the DC-bus voltage transfer function. In this regard, let's give the DC-bus voltage model. The SAPF DC voltage with its current is given by:

$$i_{dc} = C_{dc}\frac{dV_{dc}}{dt} \tag{12}$$

The coupling filter and the inverter switches power losses are omitted, the power equilibrium between DC and AC side is given by utilizing the instantaneous power theory:

$$V^*_{dc} i_{dc} = \frac{3}{2}(v_{sd} i_{sd} + v_{sq} i_{sq}) \tag{13}$$

where $v_{sd,q}$ and $i_{sd,q}$ are respectively the grid voltage and current in synchronous reference frame. Substituting (12) into (13) yields the following equation:

$$V^*_{dc}(C_{dc}\frac{dV_{dc}}{dt}) = \frac{3}{2}(v_{sd} i_{sd} + v_{sq} i_{sq}) \tag{14}$$

Assuming that the grid voltages are balanced then v_{sd} equals to zero when the synchronization with network voltages is given through a PLL. As a consequence, equation (14) becomes:

$$\frac{dV_{dc}}{dt} = \frac{3}{2}\frac{v_{sd}}{V^*_{sd} C_{dc}} i_{sd} \tag{15}$$

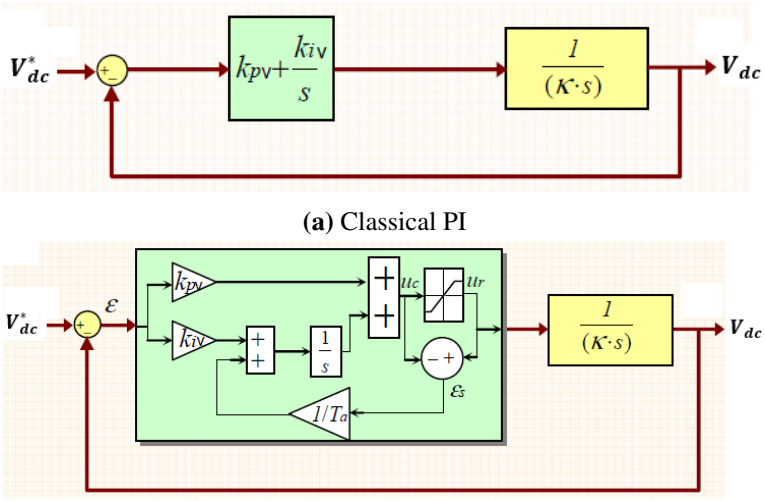
Knowing that v_{sd}=$\sqrt{2}V_{s_{rms}}$:

$$\frac{V_{dc}(s)}{i_{sd}(s)} = \frac{3}{\sqrt{2}}\frac{V_{s_{rms}}}{V^*_{dc} C_{dc} s} \tag{16}$$

Let's define $K=\frac{i_{sd}(s)}{V_{dc}(s)}$, from equation (16):

$$K = \frac{\sqrt{2}}{3}\frac{C_{dc}V_{dc}^{*}}{V_{s_{rms}}} \tag{17}$$

To keep the SAPF DC-bus voltage at the desired value a PI-based anti-windup action is used in accordance with the block diagram of the Fig. 5.



(a) Classical PI

(b) PI Anti-Windup

Fig. 5. Diagram of DC-Bus Voltage Regulation

In goal to decrease the fluctuations of the DC-bus voltage and compensate for system losses, a PI controller whose transfer function is symbolized by $G_{V_{dc}}$ is retained as a corrector for the external loop. Then, by eliminating the disturbance due to the load current [27].

In the DPC schema, to decrease the DC-link capacitor fluctuation voltages and balance for the system loss, a PI-based anti-windup action is inserted in the DC-link voltage regulation loop [28]. From the oversimplified diagram, the closed-loop transfer function is written:

$$G_{V_{dc}} = \frac{K_{pv}s + K_{iv}}{Ks^2 + K_{pv}s + K_{iv}} = \frac{\frac{K_{pv}}{K}(s + \frac{K_{iv}}{K_{pv}})}{s^2 + \frac{K_{pv}}{K}s + \frac{K_{iv}}{K}} \tag{18}$$

where K_{pv} and K_{iv} are the V_{dc} anti-windup controller gains. This transfer function represents a second-order system. So, by equating the two characteristic equations:

$$s^2 + 2\zeta\omega_n + \omega_n^2 = s^2 + (\frac{K_{pv}}{K})s + \frac{K_{iv}}{K} \tag{19}$$

By identifying the terms of (19) we find:

$$\begin{cases} K_{pv} = 2\zeta\omega_n K \\ K_{iv} = K\omega_n^2 \end{cases} \tag{20}$$

It should be noted that the anti-windup of the integral term, coming from saturation, leads to the operation of the servo-control in an open loop during a transient of large amplitude and consequently to excessive integration of the error. To solve this problem, an anti-windup structure is introduced. As long as the regulator output is not saturated, the difference, or offset between the calculated command

and the command actually applied to the system, is zero. When saturation occurs, there is a counter-reaction of this difference, multiplied by a gain $\frac{1}{T_a}$ (T_a=10^{-3}), towards the input of the integrator [29][30].

In goal to get a right compromise between stability and dynamic performance, the following values are retained: ζ=0.707, K_{pv}=0.118, and K_{iv}=6.41.

4. Direct Power Control Strategy

The DPC strategy carried out to the SAPF is elaborated in the synoptic of Fig. 6. It consists of selecting the appropriate state from a switching table based on the margins, which are bordered by an hysteresis band, present in the reactive and active power. Two aspects guarantee a viable operation of the system [31][32]:

- Exact determination of switching states.
- An accurate estimate of the reactive and active power.

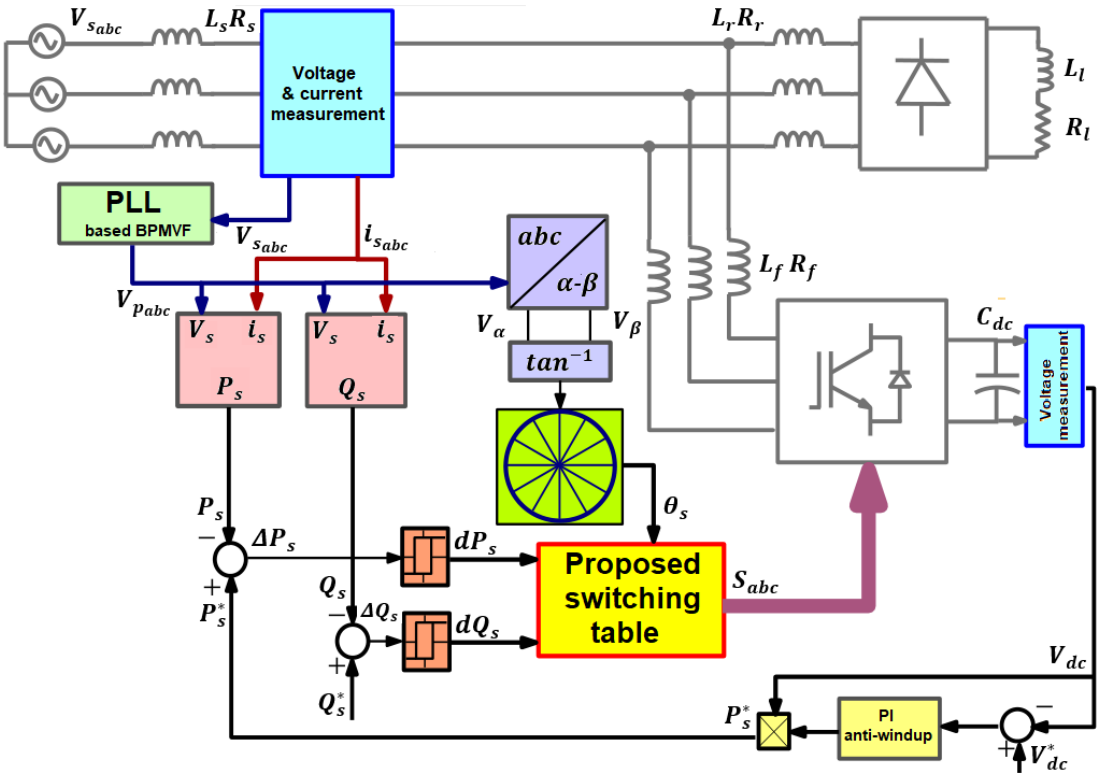


Fig. 6. Synoptic of SAPF Control with the DPC Strategy

4.1. Calculation of Instantaneous Powers

Based on the measurement of the network voltages and currents, the instantaneous reactive and active powers can be computed by the expressions:

$$P_s = V_{sa}i_{sa} + V_{sb}i_{sb} + V_{sc}i_{sc} \tag{21}$$

$$Q_s = \frac{1}{\sqrt{3}}[(V_{sa} - V_{sb})i_{sc} + (V_{sb} - V_{sc})i_{sa} + (V_{sc} - V_{sa})i_{sb}] \tag{22}$$

However, the number of sensors required increases the cost and decreases the system reliability. Thus, in goal to properly estimate the power and at the same time decrease the voltage sensors number, Noguchi proposed the use of a voltage vector estimator [33]:

- Nevertheless, the implementation of such an approach involves the calculation of the time derivatives of the measured currents, which causes the increase in noise in the regulation loop, therefore increasing the distortion level.
- In addition, Nogushi's idea can only be applied to the SAPF with the addition of a third capture of the filter currents (i_f), which will not change anything in terms of the number of sensors.

4.2. Hysteresis Controllers

The principal idea of direct power control is to keep the instantaneous reactive and active powers into a desired band. This control law is based on 2 hysteresis comparators which use as input the margin signals between the reference and estimated values of the reactive and active power.

$$\begin{cases} \Delta P_s = P_s^* - P_s \\ \Delta Q_s = Q_s^* - Q_s \end{cases} \tag{23}$$

These 2 comparators are accountable for deciding at what point a new switching or/and inverter output voltage vector is then applied. If the power margin (P_s or Q_s) is growing and attains the upper level, the hysteresis comparator changes its output to 1 (Fig. 7).

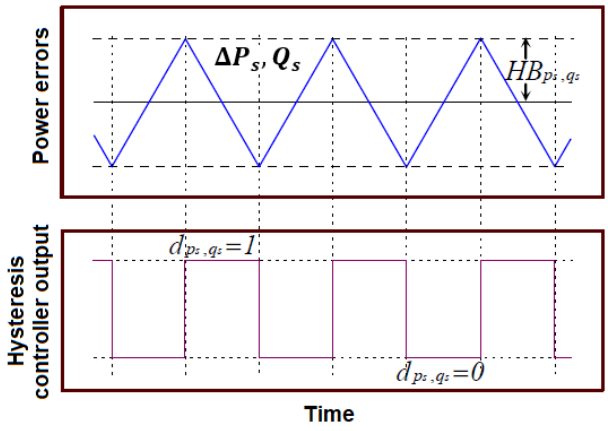


Fig. 7. Two-Level Hysteresis Power Comparator

Thus, the switching table receives the change of the input and switches the output to an suitable vector which will allow the inverter to change the state of the reactive and active power. The hysteresis comparator output level is held until the margin signal attains the lower band, where the output will switch to zero. Despite the fact that the controller output is held until the margin attains the other band, the switching table might switch to another output vector following a switchover of the second hysteresis comparator or a change in the voltage vector position. The behavior of the hysteresis controller with respect to power error limits can be summarized as follows [34]:

$$\begin{cases} \Delta(P_s, Q_s) > HB(P_s, Q_s) \\ -HB(P_s, Q_s) \leqslant \Delta(P_s, Q_s) \leqslant HB(P_s, Q_s) \\ \frac{d(\Delta(P_s, Q_s))}{dt} < 0 \\ d(P_s, Q_s) = 1 \end{cases} \tag{24}$$

$$\begin{cases} \Delta(P_s, Q_s) < -HB(P_s, Q_s) \\ -HB(P_s, Q_s) \leqslant \Delta(P_s, Q_s) \leqslant HB(P_s, Q_s) \\ \frac{d(\Delta(P_s, Q_s))}{dt} > 0 \\ d(P_s, Q_s) = 0 \end{cases} \tag{25}$$

4.3. Sector Choice

The impact of every output vector resulting from the SAPF on the reactive and active powers is much reliant on the actual position of the network voltage vector. Thus, in addition to the signals of the 2 hysteresis comparators, the switching table functions according to the position of the network voltage vector, which turns at pulsation ω_s, in the complex plane. Nevertheless, instead of feeding the switching table the accurate voltage vector position, the sector picking block informs in which area the current network voltage vector is located [35].

In order to increase the precision and also to avert the problems faced at the boundaries of every control vector, the plane of the vector space is partitioned into 12 sectors of 30° each (Fig. 8), where the first sector is allocated between $-\frac{\pi}{3}<\theta_1<0$. Consequential regions counterclockwise follow the same criterion, which can be usually formulated as:

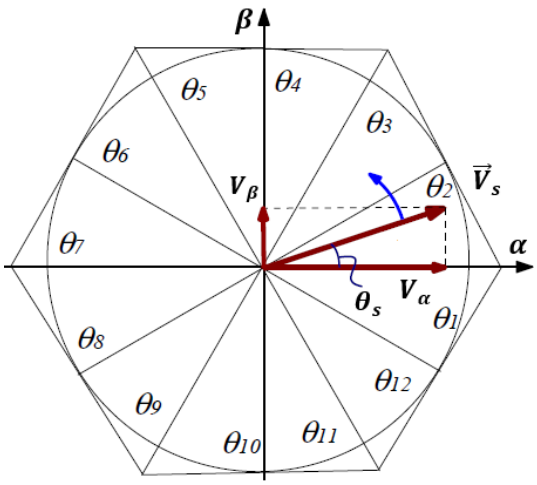


Fig. 8. Voltage Vector Representation in the Space Vector

$$(n-2)\frac{\pi}{6} \leqslant \theta_n \leqslant (n-1)\frac{\pi}{6} \quad n = 1, 2, \ldots, 12 \tag{26}$$

Depending on the network voltage vector angle referenced on the α-axis, the sector where the vector is located will be chosen. The angle is computed using the reverse trigonometric function, based on the voltage vector components in the α-β frame, given by equation (27):

$$\theta = \arctan\left(\frac{v_\beta}{v_\alpha}\right) \tag{27}$$

4.4. Conventional Switching Table

The switching table can be regarded the core of direct power control. It picks a suitable inverter voltage vector to allow the instantaneous reactive and active power to move in the wished direction, also based on the position of the network voltage vector and reactive and active power margins. Depending to the vector space theorem, the instantaneous reactive and active power can be computed from the imaginary and real parts of the multiplication of the voltage vector and the current vector conjugate as it is shown in (28) [36].

$$\begin{cases} P_s = \frac{3}{2}\Re(\overline{V}_s.\overline{i}_s^*) \\ Q_s = \frac{3}{2}\Im(\overline{V}_s.\overline{i}_s^*) \end{cases} \tag{28}$$

The representing of these powers in the rotating frame d-q makes it possible to obtain the following new equations:

$$\begin{cases} P_s = v_{sd} i_{sd} + v_{sq} i_{sq} \\ Q_s = v_{sq} i_{sd} - v_{sd} i_{sq} \end{cases} \tag{29}$$

However, by using a PLL the voltages obtained become purely sinusoidal and balanced which allows the voltage vector to be aligned on the d-axis and the quadratic component will be zero v_{sq}=0. Therefore, equation (29) becomes:

$$\begin{cases} P_s = v_{sd} i_{sd} \\ Q_s = -v_{sd} i_{sq} \end{cases} \tag{30}$$

Based on this approach, Noguchi developed the following switching table (Table 1).

Table 1. Conventional switching table

ΔP_s	ΔQ_s	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	θ_7	θ_8	θ_9	θ_{10}	θ_{11}	θ_{12}
1	0	v_6	v_7	v_1	v_0	v_2	v_7	v_3	v_0	v_4	v_7	v_5	v_0
	1	v_7	v_7	v_0	v_0	v_7	v_7	v_0	v_0	v_7	v_7	v_0	v_0
0	0	v_6	v_1	v_1	v_2	v_2	v_6	v_6	v_4	v_4	v_5	v_5	v_6
	1	v_1	v_2	v_2	v_6	v_6	v_4	v_4	v_5	v_5	v_6	v_6	v_1

5. The Proposed Switching Table for Robust DPC

A 2-level voltage inverter delivers 7 voltage vectors for 8 different combinations. Every voltage vector is calculated based on a combination of the respective switches and the DC-bus voltage [37].

$$v_k = \frac{2}{3} v_{dc} (S_{a_k} + S_{b_k} e^{j\frac{2\pi}{3}} + S_{c_k} e^{j\frac{4\pi}{3}}) \quad k = 0, 1, \ldots, 7 \tag{31}$$

As the time interval between 2 interrupt actions is relatively small, the change in inverter voltage can be approached by:

$$\Delta v_f = v_k \Delta t \tag{32}$$

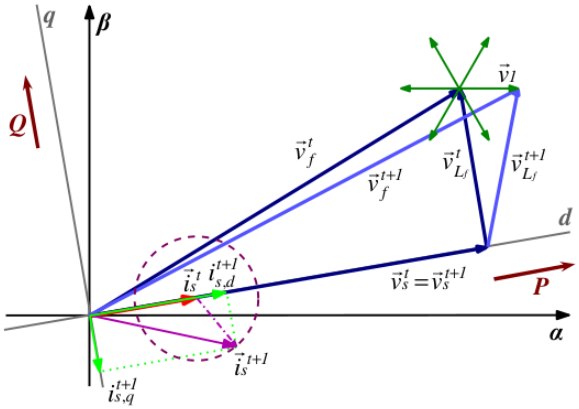
The precedent equations allow to investigate the impact of each inverter output vector on reactive and active power considering particular sectors.

Assume, at time t, a desired reference position in vector space, where the network current $\vec{i}_s^t$ is in phase with its voltage $\vec{v}_s^t$ (d-axis direction) which lies in the second sector, and the voltage of the filter $\vec{v}_f^t$ is such that the state of the inverter undergoes no change, that is to say, that the voltage vector of the latter is either $\vec{v}_0$ or $\vec{v}_7$.

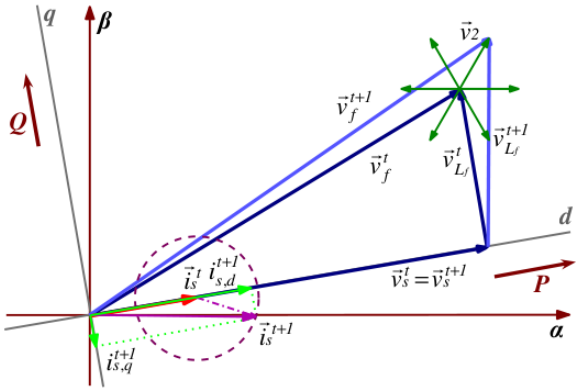
From this position and for the case of Fig. 9(a), if the inverter applies at time t+1 the voltage vector $\vec{v}_1$ for a certain time, this will introduce a displacement of the network current vector $\vec{i}_s^{t+1}$ by a quantity corresponding to a constant hysteresis band (radius of the circle).

By projecting the current vector on the d-q axes, we notice that the component on the d-axis $\vec{i}_{sd}^{t+1}$ has increased and that of the q-axis $\vec{i}_{sq}^{t+1}$ becomes negative non-zero, compared to the previous state at the moment t. So, assuming that the network voltage vector is in the second sector, the application of the voltage vector $\vec{v}_1$ by the inverter will increase the active and reactive power.

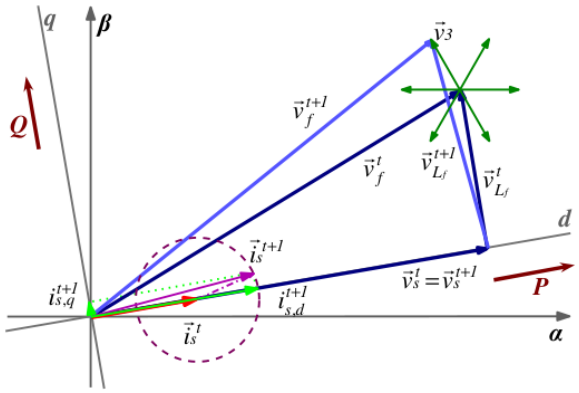
An analogous analysis can be carried out for the other inverter voltage five space vectors as shown in Figs. 9(b) and (f). From the latter, we can see that if the network voltage vector is oriented towards the direct axis d, the active power is straight proportional to the direct constituent of the network current i_{sd}, and the reactive power is established by the quadratic component i_{sq} (Table 2) [38][39][40].



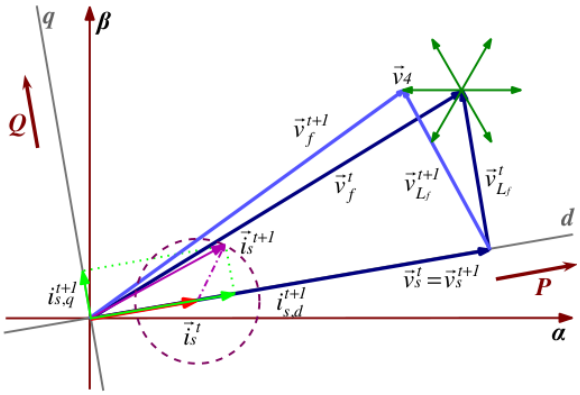
(a) $\vec{v}_1$: P_s increases and Q_s increases



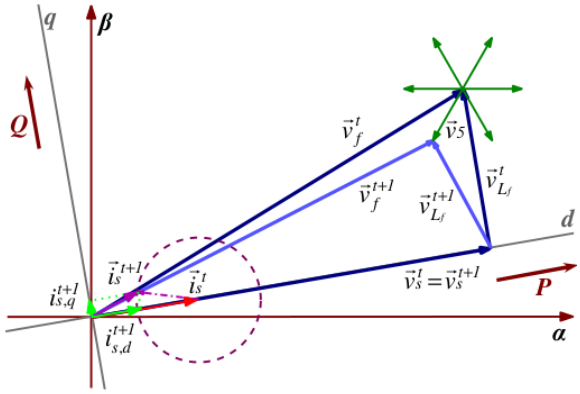
(b) $\vec{v}_2$: P_s increases and Q_s increases



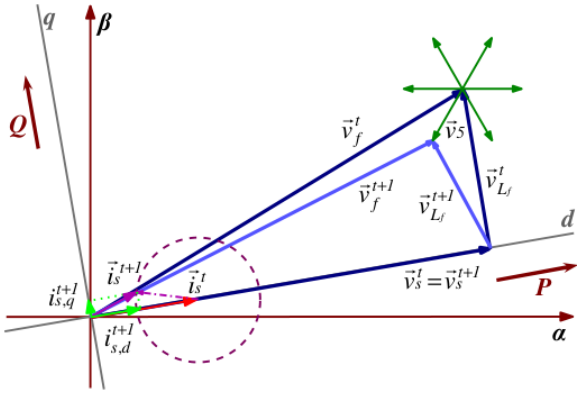
(c) $\vec{v}_3$: P_s increases and Q_s decreases



(d) $\vec{v}_4$: P_s increases and Q_s decreases



(e) $\vec{v}_5$: P_s decreases and Q_s decreases



(f) $\vec{v}_6$: P_s decreases and Q_s increases

Fig. 9. Effect of Inverter Output Vector on Reactive and Active Powers

Table 2. Suggested switching table

ΔP_s	ΔQ_s	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	θ_7	θ_8	θ_9	θ_{10}	θ_{11}	θ_{12}
1	0	v_4	v_5	v_5	v_6	v_6	v_1	v_1	v_2	v_2	v_3	v_3	v_4
	1	v_3	v_4	v_4	v_5	v_5	v_6	v_6	v_1	v_1	v_2	v_2	v_3
0	0	v_6	v_1	v_1	v_2	v_2	v_3	v_3	v_4	v_4	v_5	v_5	v_6
	1	v_1	v_2	v_2	v_3	v_3	v_4	v_4	v_5	v_5	v_6	v_6	v_1

6. Results and Discussion

6.1. Simulation Protocol

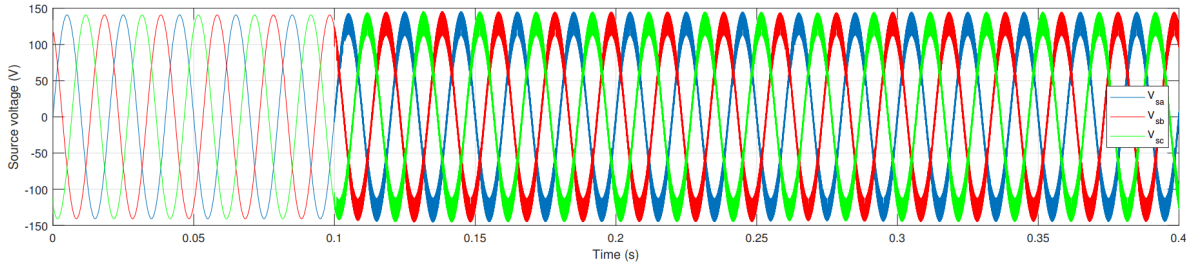
In goal to study the performance of the suggested DPC applied to the SAPF, a complete model is developed under the MATLAB/Simulink utilizing the characteristics in Table 3.

Table 3. Network, Non-Linear Load, and SAPF Parameters

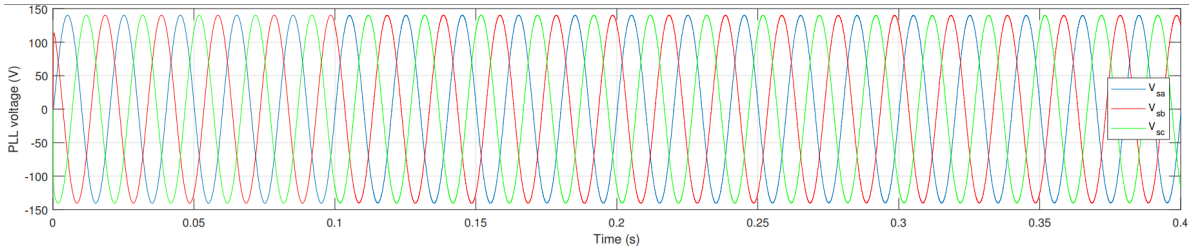
Network parameters	rms voltage	100 V
	Frequency	50 Hz
	Internal resistance	0.1 Ω
	Internal inductance	0.1 mH
Nonlinear load	Load resistance	30 Ω
	Load inductance	1 mH
	Rectifier resistance	0.01 Ω
	Rectifier inductance	0.566 mH
Active filter (SAPF)	Bus capacitor	1100 μF
	Filter inductance	1 mH
	Reference voltage	283 V
Simulation environment	Sampling time	1 μs
	Step type	Fixed step
	Resolution method	Euler (ode1)
	Hysteresis band	HB=0.2

First, a study of the quality of filtering will be carried out by spectral analysis of currents and with a comparison of their distortion rates. Then the stability and the robustness of the control in the cases of closure of the SAPF on the network and the change of the nonlinear load are evaluated. The filter closer is established at t=0.1s and a load variation is applied at t=0.25s by varying the load resistor value from 30Ω to 20Ω. It's important to notice that the DC-bus capacitor is initially charged with a voltage of 241V.

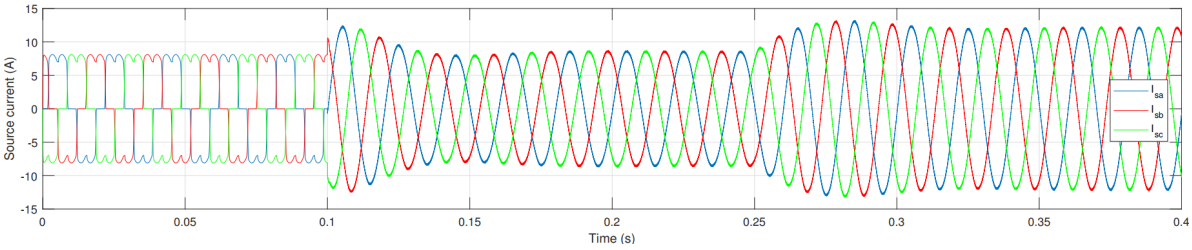
The signals shown in Fig. 10 from top to bottom are the network voltage, the PLL voltage, the network current, the load current, and the filter current. The signals shown in Fig. 11 from top to bottom are the DC-bus voltage, the active power of the conventional DPC, the active power of the proposed DPC, the reactive power of the conventional DPC, and the reactive power of the proposed DPC. Fig. 12 highlights the network's current THD values before and after the filter closer. The curves shown in Fig. 13 are the network current and voltage, the DPC angle, the DPC sector selection, and the evolution of the network voltage in the α-β reference frame.



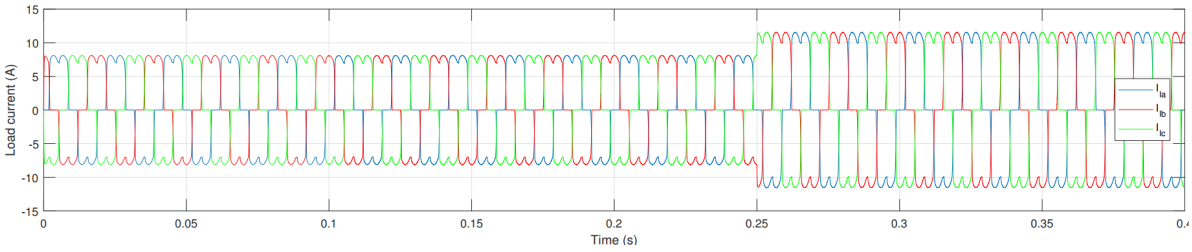
(a) Source voltage: proposed DPC



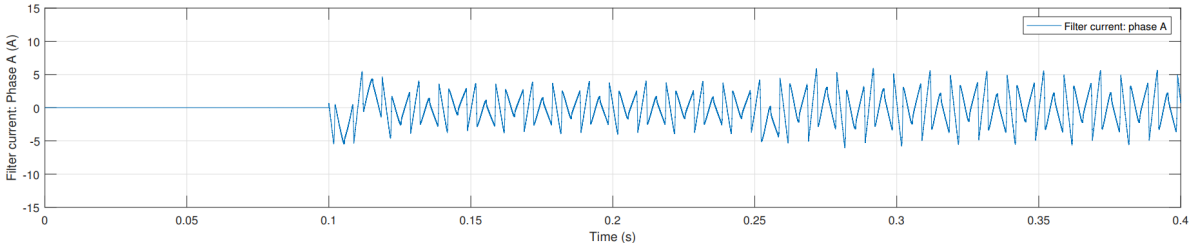
(b) PLL voltage: proposed DPC



(c) Source current: proposed DPC

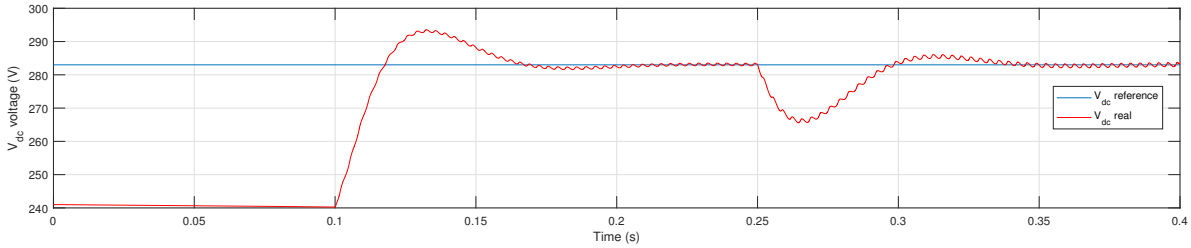


(d) Load current: proposed DPC

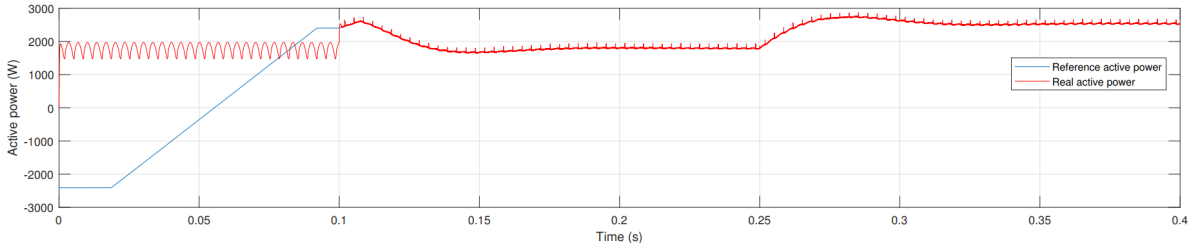


(e) Filter current: proposed DPC

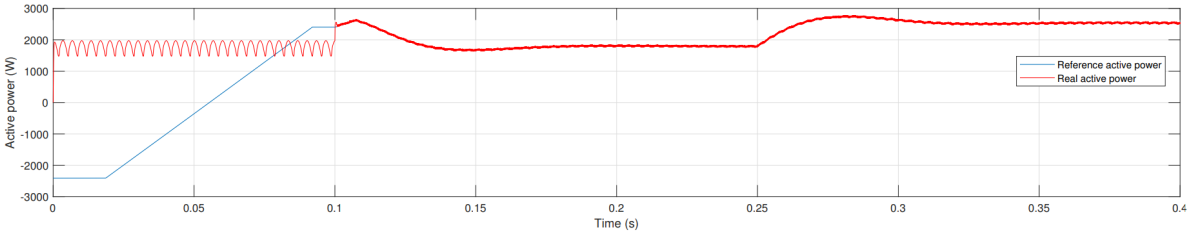
Fig. 10. Simulation Results of the Transient when Closing the SAPF at t=0.1s for a Variable Non-Linear Load



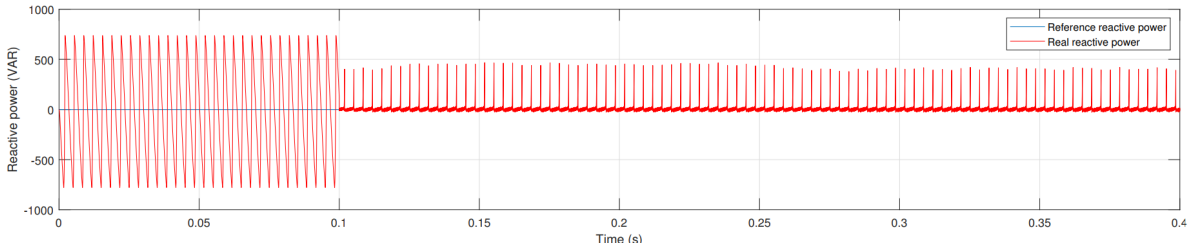
(a) Bus voltage: proposed DPC



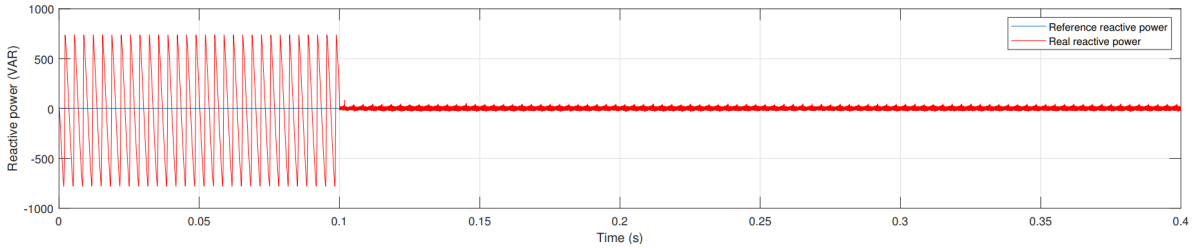
(b) Active power: conventional DPC



(c) Active power: proposed DPC

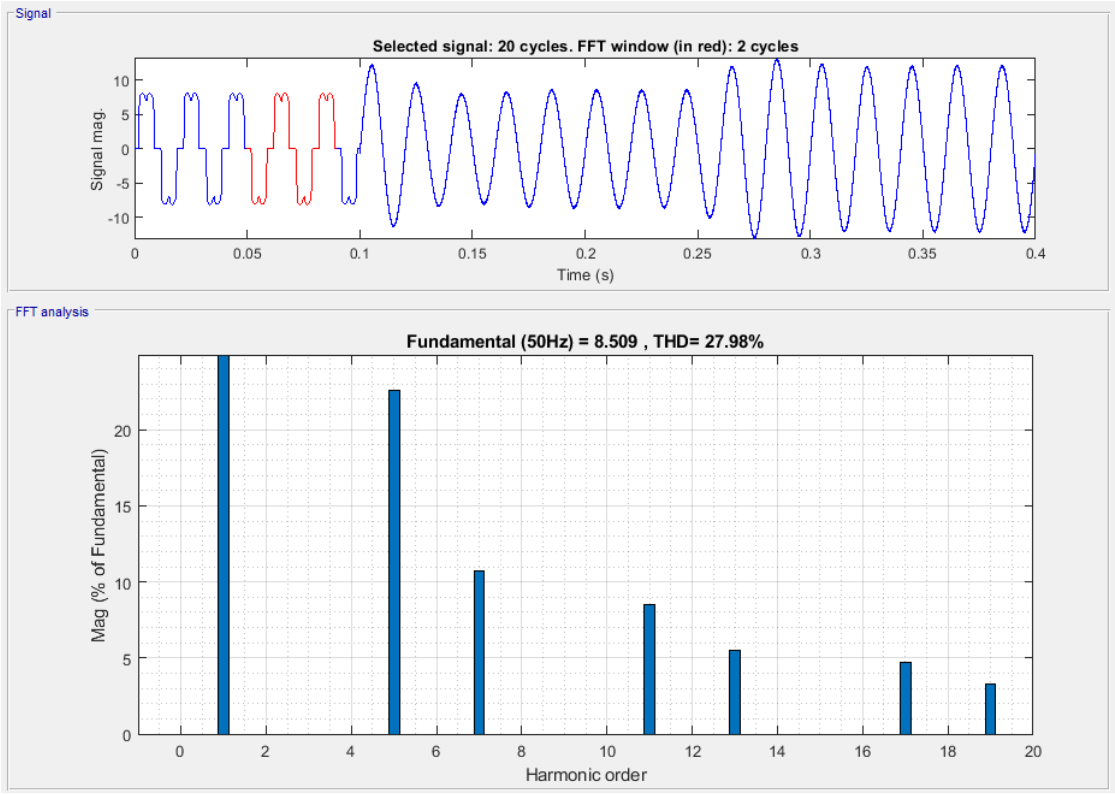


(d) Reactive power: conventional DPC

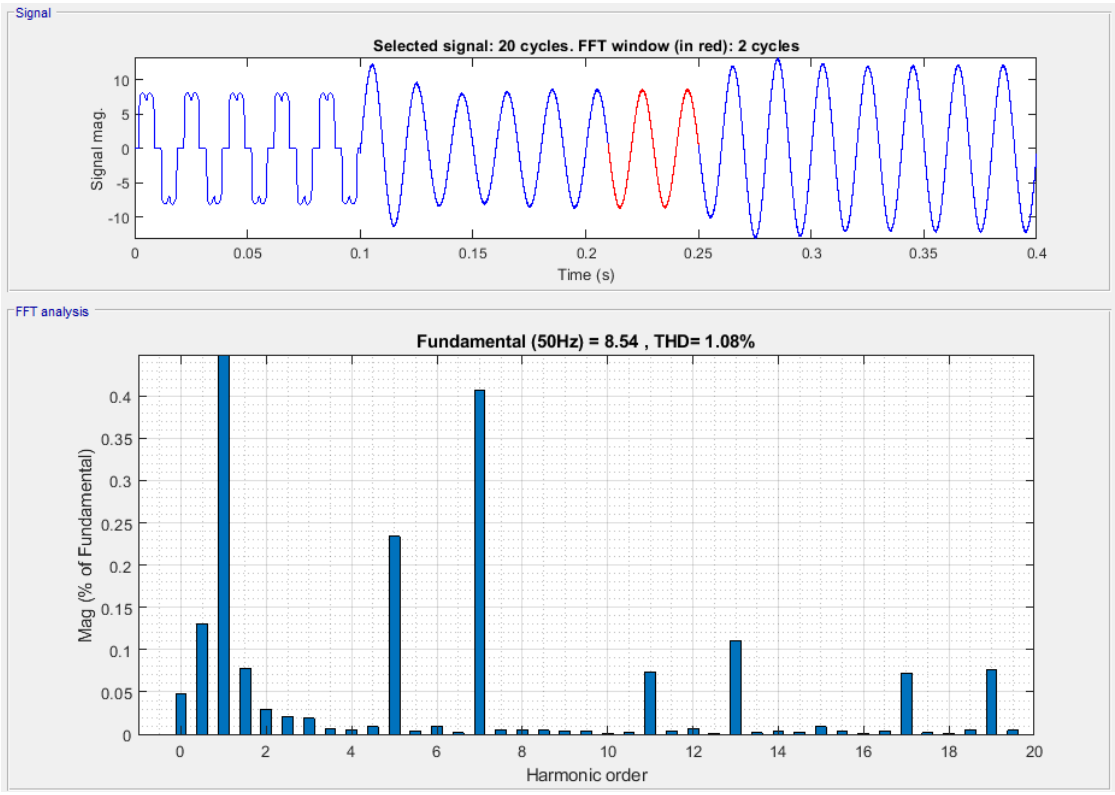


(e) Reactive power: proposed DPC

Fig. 11. DC-Bus Voltage and Instantaneous Power Waveform for the Conventional and the Proposed DPC

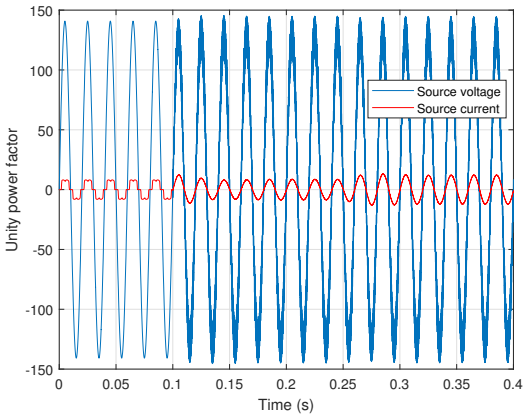


(a) Before filter application

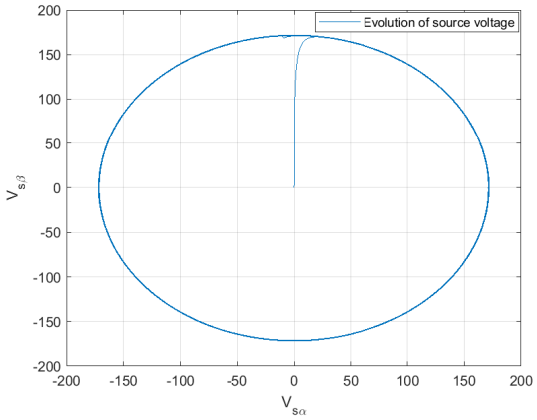


(b) After filter application

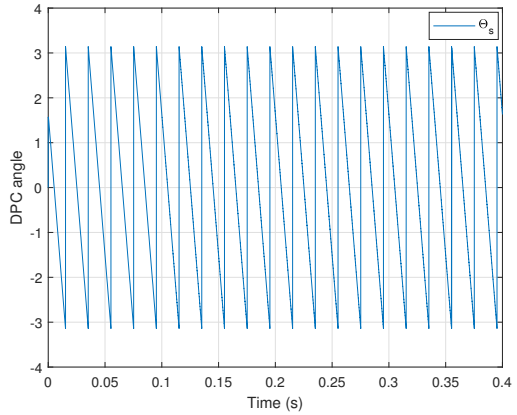
Fig. 12. Spectrum of the Network Current Before and After Filter Application



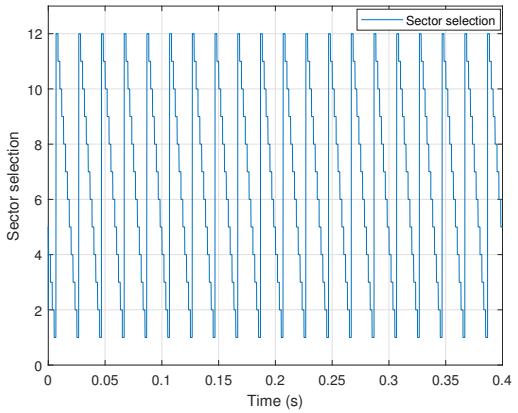
(a) Network voltage and current



(b) Evolution of the source voltage in the α-β reference frame



(c) DPC angle



(d) Sector selection

Fig. 13. The Proposed DPC High Performance

6.2. Results Analysis

Fig. 10(c) shows that before closing the SAPF (before t=0.1s), and due to the nonlinear load, the network current was not sinusoidal. Fig. 11(c) shows the non-zero reactive power produced by the network. After the closer of the SAPF at t=0.1s, the network current becomes quasi-sinusoidal. The active power is constant and narrowly follows its reference (Fig. 11(c)). The reactive power is zero on average (Fig. 11(e)), so ensuring operation with a unity power factor. The DC-bus voltage (Fig. 11(a)) attains its reference (V_{dc}^{*}=283V) in 3-period cycles and keeps its stability during the steady state. Fig. 12 represents the analysis of the network's current spectrum before and after filtering. Before filtering, the value of the harmonic distortion rate was THDi=27.98% (Fig. 12(a)) and after filtering it becomes THDi=1.08% (Fig. 12(b)), which means conformity with the **IEEE 519-1992** standard.

On the other hand, Fig. 13(a) demonstrates the synchronization of the network current and voltage before and after filtering, which means a unity power factor. Fig. 13(b) illustrates the evolution of the network voltage vector on the 2 axes α and β and its representation in the polar coordinates. Fig. 13(c) shows the angle θ_s of the DPC. Fig. 13(d) highlights the sector selection of the DPC. Fig. 13(a) proves again that the suggested PLL delivers a good estimate of the angle θ_s, and generates sinusoidal voltages when the input voltages contain harmonics. The network voltage evolution is very quick. We

can clearly notice that the voltage shape do not exceed the hysteresis boundaries. The sector selection is uniform. Starting from sector 3, the upgrade continues until sector 1 then the choice moves to sector twelve immediately.

Fig. 10(e) clearly shows that the current inrush following the load variation is almost instantaneous, undergoing no distortion with respect to its sinusoidal waveform. But thus causing a decrease in the DC-bus voltage (Fig. 11(a)). The proposed DPC proves then its robustness by the excellent tracking of the reactive and active powers to their references.

This control technique allows to obtain better energy quality compared to other techniques, this can be confirmed by the appearance of the active and reactive powers that follow exactly their references with the desired accuracy, and by presenting no disturbance.

The current call following the variation of the load is almost instantaneous, by not undergoing any distortion towards its sinusoidal form and its quality. But thus causing a decrease in the continuous bus voltage during a transitional of the active power. It' very important to note that the necessary time of the transient of active power is very short.

6.3. Comparative Study

Figs. 11(b) and (c) show the instantaneous active power of the conventional and the suggested DPC respectively. The active power waveform in the suggested DPC shows fewer discontinuities. Figs. 11(d) and (e) show the instantaneous reactive power of the conventional and the proposed DPC respectively. The reactive power waveform in the proposed DPC is better than that of the conventional DPC. There are no discontinuities or fluctuations. The proposed switching table proved good performance characteristics in terms of precision and harmonic reduction.

In case of imbalance of the non-linear load due to the absence of a phase, considered as the most unfavorable case (two currents in phase opposition), the SAPF with the proposed DPC control technique, could not only balance the currents and voltages but also improve the quality of energy.

7. Conclusion

This research presents a detailed design and examination of a new switching table in order to overcome the drawbacks and restrictions of the current DPC switching table. The following objectives are the main focus (1) Improvement in the variation of SAPF instantaneous powers from the electrical model in the stationary reference frame (2) Planning of a different switching table based on the investigation of the reactive and active power variation for different voltage vectors in the twelve sector partition. Under MATLAB/Simulink, the validation of the proposed SAPF-DPC using the modified switching table was carried out. In order to confirm the control strategy's great performance, numerous simulation experiments are conducted, demonstrating how the non-sinusoidal network current (THDi=27.98%) will change to a quasi-sinusoidal current (THDi=1.08%) after the filter application. Since the reactive power is typically zero and the active power closely follows its reference, a unity power factor is assured. The transient regime demonstrates outstanding performance for either overshoot or stability, proving the control's durability.

Author Contribution: All authors contributed equally to the main contributor to this paper. All authors read and approved the final paper.

Funding: This research received no external funding.

Acknowledgment: The authors would like to thank the managers and the members of the "EIE laboratory" for their precious remarks and suggestions.

Conflicts of Interest: The authors declare no conflict of interest.

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