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# Solar-Cell Design Based On A Distributed Diode Analysis

Jack L. Boone
*Missouri University of Science and Technology*

Thomas P. Van Doren
*Missouri University of Science and Technology*

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carrier injection control where the channel is in a gate-induced pinchoff. The $I$-$V$ characteristics in the SIT follow an exponential behavior in the lower current region where the effect of series channel resistance is not significant, while the SIT operates as a voltage-controlled resistor if the channel is not in a gate-induced pinchoff. With increasing current, the $I$-$V$ characteristics change to a nearly linear relation due to a negative-feedback effect associated with series channel resistance.

The temperature coefficient of the current has been shown to be positive in the lower current region where the effect of series channel resistance is negligibly small and positive in the higher current region due to the series channel resistance. Therefore, thermal runaway is completely suppressed in the SIT. By properly designing the structure and the impurity profile, it is possible to eliminate these effects for the fabrication of an SIT having zero temperature coefficient over a wide range of bias conditions.

The series channel resistance in the SIT was measured experimentally, and was found to increase with increasing gate voltage and to decrease with increasing drain current. It has been experimentally demonstrated that the product of series channel resistance and dc intrinsic transconductance in the SIT is less than unity in the bias conditions investigated in this study.

The voltage amplification factor of the SIT has been shown to be almost independent of large variations of drain currents regardless of whether the $I$-$V$ characteristics are in the exponential or linear region. Furthermore, it remains almost constant for the temperature variation from -78°C to 110°C, although the transconductance and the series channel resistance vary with temperature.

Three-terminal devices satisfying the principle described in this paper exhibit the nonsaturation $I$-$V$ characteristic regardless of the material used. A GaAs Schottky-barrier SIT has recently been realized [6], which is very promising for high-frequency and high-speed operation. The success in the realization of a GaAs SIT indicates that the current saturation of a GaAs FET arises from the negative feedback action due to the series channel resistance [5].

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# Solar-Cell Design Based on a Distributed Diode Analysis

JACK L. BOONE AND THOMAS P. VAN DOREN, MEMBER, IEEE

*Abstract*—**The front surface of a p-n junction solar cell has resistive losses associated with the diffused layer, the metal-semiconductor contact, and the grid structure. These losses are analyzed by considering the spatially distributed nature of the p-n junction and the grid conductors. This distributed diode analysis is especially useful for solar cells operated under concentrated sunlight conditions. The results show the dependence of the $V$-$I$ characteristics and the maximum power output per unit cell on the ratio of the diffused layer resistance to the junction dynamic resistance. This ratio can assist the designer in establishing proper grid structure geometries and should typically be less than 0.1 if the power output per unit cell is to be within 3 percent of that for the lossless case. Experimental measurements are reported which confirm the theoretical calculations. An analysis of the grid conductor losses associated with multiple-connected unit cells shows the disastrous effect that the grid header resistance can have on the performance of a solar cell. The results indicate that the use of a tapered header conductor to decrease the metal coverage may actually worsen cell performance.**

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The authors are with the University of Missouri-Rolla, Rolla, MO 65401.

## List of Symbols

$g_p$ p-n junction shunting conductance, $\mho \cdot m^{-2}$.
$I$ Unit cell sheet current as a function of distance, A.
$I_L$ Total output current from many unit cells, A.
$I_0$ Unit cell terminal current, A.

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$I_r$ Unit cell reverse saturation current, A.
$J_d$ p-n junction diode current density, $A \cdot m^{-2}$.
$J_0$ p-n junction reverse saturation current density, $A \cdot m^{-2}$.
$J_s$ p-n junction short-circuit current density, $A \cdot m^{-2}$.
$L$ One-half the grid spacing, m.
$P_n$ Normalized maximum power output.
$R_d$ Equivalent lumped series resistance of diffused layer, Ω.
$R_g$ Resistance per unit cell of main grid conductor, Ω.
$R_j$ Dynamic resistance per unit cell of p-n junction, Ω.
$R_L$ Unit cell load resistance for maximum power, Ω.
$r_m$ Resistance per square of grid metallization, Ω.
$R_m$ Resistance of grid metallization, Ω.
$r_s$ Resistance per square of semiconductor front surface, Ω.
$R_s$ Total series resistance per pair of unit cells, Ω.
$T$ Width of a grid conductor branch line, m.
$V$ p-n junction voltage as a function of distance, V.
$V_L$ Output voltage from paralleled unit cells, V.
$V_{ex}$ p-n junction voltage at $x = L$, V.
$V_0$ Unit cell terminal voltage, V.
$V_{oc}$ Unit cell open-circuit voltage, V.
$V_T$ Thermal voltage, V.
$W$ Unit cell width, m.

## I. Introduction

THE SEVERAL AUTHORS who have investigated the aspects of ohmic losses in p-n junction solar cells [1]-[5] attribute the losses for planar junction cells with a front surface grid structure to the resistance of the base bulk, base contact, the front surface semiconductor sheet, the grid contact, and the grid structure. Wolf's analysis [1] makes it possible to express the "unit cell" resistance as a lumped element in series with an ideal diode. This treatment is based on the assumption that the unit cell is essentially one-dimensional and that the current is uniformly distributed over the active surface. Handy [2] developed a more extensive lumped element model, which takes into consideration all the resistance losses and attempts to develop two-dimensional solutions for the sheet resistance losses. These and other similar treatments provide sufficiently accurate results to allow one to model the solar cell losses as lumped resistances, which are functions of the material resistivity and geometry.

In this paper, the resistive losses in a solar cell are described in terms of the measurable parameters associated with the p-n junction so that investigators can relate the $V$-$I$ terminal characteristics to the junction parameters more accurately and designers can avoid unnecessary degradation in cell performance as a result of resistive losses emanating from poorly designed grid structures. Base and back surface losses for the planar geometry are assumed to be insignificant and are not considered.

The conventional grid structure shown in Fig. 1 is used in the analysis, because other grid patterns lead to essentially the same conclusions. To simplify this analysis further, it is assumed that $W >> L$ so that a one-dimensional analysis of the sheet resistance losses can be utilized. No real loss in generality is involved, because the two-dimensional model can be handled by superposing the one-dimensional predictions.

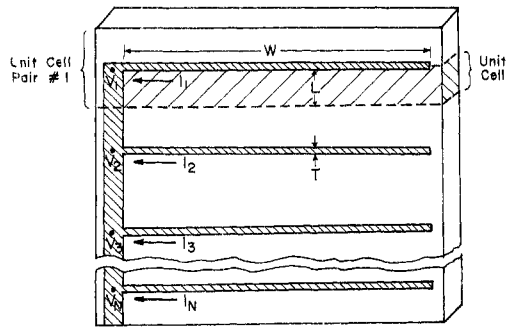


Fig. 1. A conventional solar-cell grid structure showing a typical unit cell.

## II. Losses in the Diffused Layer

*Distributed Diode Analysis*

Resistive losses in the diffused layer are caused by the lateral flow of current across the front surface of the solar cell. An accurate analysis of these losses must take into consideration the spatial variation of the p-n junction voltage. This can be accomplished by using a distributed one-dimensional model [3], [4], as shown in Fig. 2.

The differential equations for the junction voltage $V$ and sheet current $I$ along an incremental section of the model are

$$dV/dx = (r_s/W)\, I \tag{1}$$

and

$$dI/dx = W\{-J_s + J_0 [\exp (V/V_T) - 1] + g_p V\}. \tag{2}$$

For nonideal p-n junction devices both $J_0$ and $V_T$ are functions of $V$. However, most of the results to be discussed will concern junction voltages corresponding to the range between open circuit and maximum power output. Over this voltage range both $J_0$ and $V_T$ may frequently be assumed independent of $V$. The remainder of the $V$-$I$ characteristic between maximum power output and short circuit will be slightly incorrect due to the assumption of constant values for $J_0$ and $V_T$.

The use of

$$(dV/dx)^2 = \int d\,(dV/dx)^2 = \int 2\,(d^2V/dx^2)\, dV = [(r_s/W)\, I]^2 \tag{3}$$

and the imposition of the boundary conditions

$$I(L) = 0 \quad \text{and} \quad V(L) = V_{ex} \tag{4}$$

lead to the solution

$$I = \{(2W^2/r_s)\, [(J_s + J_0)\,(V_{ex} - V) + J_0 V_T\, (\exp V/V_T - \exp V_{ex}/V_T) + (g_p/2)\,(V^2 - V_{ex}^2)]\}^{1/2}. \tag{5}$$

If it is assumed that the shunt conductance $g_p$ is negligible and (5) is used in (1), then

$$dV/dx = \{2r_s(J_s + J_0)\, [(V_{ex} - V) + V_T \exp ((V_{ex} - V_{oc})/V_T)\, [\exp ((V - V_{ex})/V_T) - 1]]\}^{1/2}. \tag{6}$$

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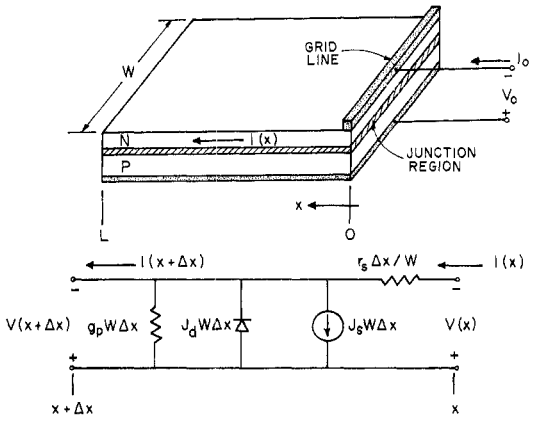


Fig. 2. Solar-cell structure and the distributed equivalent circuit for the one-dimensional n-on-p solar cell.

For properly designed solar cells, it has been shown [5] that $(V_{ex} - V) < V_T$. This allows for the expansion of the exponential term on the right-hand side of (6). The solution of (6) and the simplification of (5) using this condition yield

$$V \simeq V_{ex} - (r_s/2)(J_s + J_0)\,[1 - \exp((V_{ex} - V_{oc})/V_T)]\,(L - x)^2 \tag{7}$$

and

$$I \simeq W(J_s + J_0)\,[1 - \exp((V_{ex} - V_{oc})/V_T)]\,(L - x). \tag{8}$$

Equation (7) indicates that the junction voltage $V$ varies quadratically with position and reaches an extremum $V_{ex}$ at $x = L$. The extremum is a maximum in the case of active solar-cell operation and a minimum for a passive cell driven by an external source.

By setting $x = 0$, one obtains the unit cell terminal characteristics in the dimensionless forms

$$V_0/V_T \simeq (V_{ex}/V_T) - (R_d/R_{jo})\,[1 - \exp((V_{ex} - V_{oc})/V_T)] \tag{9}$$

and

$$I_0/J_sWL \simeq [(J_s + J_0)/J_s]\,[1 - \exp((V_{ex} - V_{oc})/V_T)] \tag{10}$$

in which

$$R_d/R_{jo} = r_s(J_s + J_0)\,L^2/2V_T = (r_sL/2W)/[(V_T/J_0WL)\exp(-V_{oc}/V_T)]. \tag{11}$$

The term $R_d$ is the equivalent series resistance of the diffused layer, and $R_{jo}$ is the junction dynamic resistance at the open-circuit voltage. The equations are valid for $(V_{ex} - V_0) < V_T$, which is equivalent to $R_d/R_{jo} < 1$.

Fig. 3 shows the $V$-$I$ characteristics for cells with various $V_{oc}/V_T$ and $R_d/R_{jo}$ ratios. Numerical techniques can be used to obtain solutions for the $V$-$I$ characteristics for cells in which $(V_{ex} - V_0) > V_T$; however, solar cells for this case have fill factors (FF) which are less than 0.6, which means that the performance of these devices is so inadequate that they are of marginal interest.

A lumped element model of the distributed unit cell can be obtained by rearranging (9) and (10) to yield

$$V_0 \simeq V_{ex} - R_dI_0 \tag{12}$$

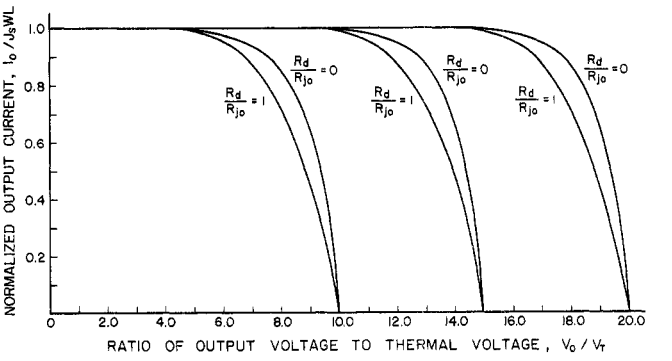


Fig. 3. Unit cell $V$-$I$ characteristics for various $V_{oc}/V_T$ and $R_d/R_{jo}$ ratios.

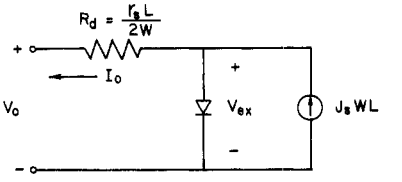


Fig. 4. A lumped element model of a unit cell valid for $(V_{ex} - V_0) < V_T$.

and

$$I_0 \simeq WL\{J_s - J_0[\exp(V_{ex}/V_T) - 1]\}. \tag{13}$$

These equations dictate the model shown in Fig. 4.

*Maximum Power Output Conditions*

At the maximum power point, the relation

$$I_0/V_0 = -dI_0/dV_0 \tag{14}$$

can be used in conjunction with (7) and (8) to show that

$$V_{ex}/V_T \simeq 2(R_d/R_{jo})\,[1 - \exp((V_{ex} - V_{oc})/V_T)] + [\exp((V_{oc} - V_{ex})/V_T) - 1]. \tag{15}$$

The ratio $V_{ex}/V_T$ can be determined from (15) for a given set of device parameters and used in (9) and (10) to determine the maximum power output.

Fig. 5 shows the effect that the ratio $R_d/R_{jo}$ has on the output of the cell at maximum power. Although the loss in power output appears to be a slowly varying function of $R_d/R_{jo}$, it is apparent that an unsuitable choice of grid spacing for a given cell can result in significant losses that could be avoided.

In an effort to ascertain that the linear theory provides useful results for values of $R_d/R_{jo} < 1$, a simple cell such as the one shown in Fig. 1 was tested in the circuit shown in Fig. 6.

Assuming that the diode can be modeled as shown in Fig. 4, a set of curves with nearly constant $I_{sc}$ and $V_{oc}$ can be generated for each value of incident sunlight by varying $R_s$. A sample of such curves is shown in Fig. 7. Since $I_{sc}$ and $V_{oc}$ are almost constant, the data can be presented in the format shown in Fig. 5. The correlation between experiment and theory is excellent. An examination of the data in Fig. 5 reveals that in order to maintain a large fill factor, $R_d$ must be decreased as $I_s$ increases, which implies a reduction in grid spacing. Further, it is desirable to strive for large values of

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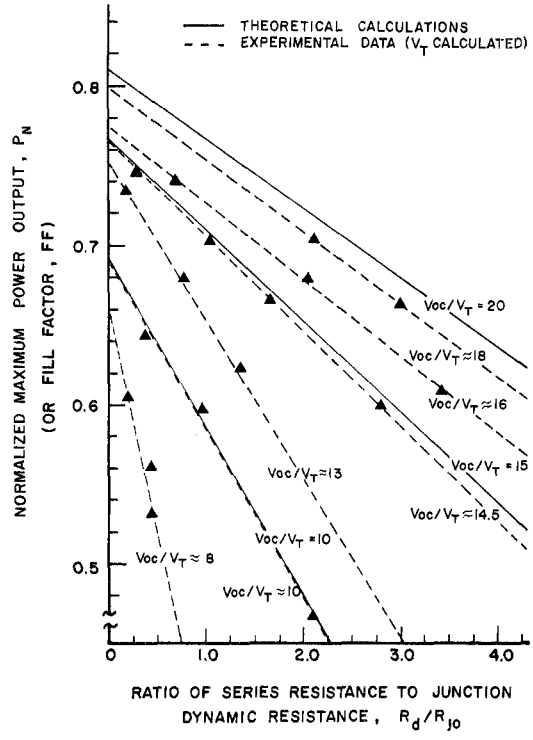


Fig. 5. Normalized maximum output power versus the resistance ratio $R_d/R_{jo}$. The output power is normalized relative to the product of the open-circuit voltage ($V_{oc}$) and the ideal short-circuit current ($WLJ_s$).

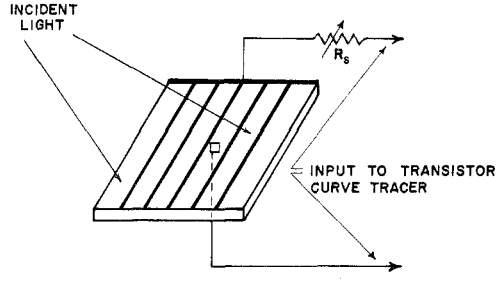


Fig. 6. Test arrangement for varying $R_s$ with a fixed $I_{sc}$ and $V_{oc}$.

$V_{oc}/V_T$ by a reduction in reverse currents or a reduction in $V_T$ even at the expense of an increased $R_d/R_{jo}$ term.

For example, a silicon cell under one-sun conditions with 0.3-cm grid spacing, 0.52 V at open circuit, 25 mA/cm$^2$ short-circuit current density, 10-Ω/sq sheet resistance, and $V_T$ = 0.026 V would have $R_d/R_{jo} = 0.11$ with a corresponding fill factor of 0.805 (see Fig. 5). If the same cell is subjected to ten suns, the $R_d/R_{jo}$ ratio would increase by a factor of ten and result in a fill factor of 0.765 if $V_{oc}/V_T$ remains the same. Actually, $V_{oc}/V_T$ tends to decrease as $I_s$ is increased resulting in an even more pronounced decrease in relative output. Aside from the effects associated with increased carrier concentration, it is possible to compensate for the increase in $I_s$ by decreasing $R_d$; that is accomplished by decreasing the grid spacing for a given diode.

Using (12), (13), and (15), the load resistance required for maximum power transfer is

$$R_L = (r_s L/2W) + (V_T/J_0 WL) \exp(-V_{ex}/V_T). \quad (16)$$

The effect of the grid conductor and contact resistances can

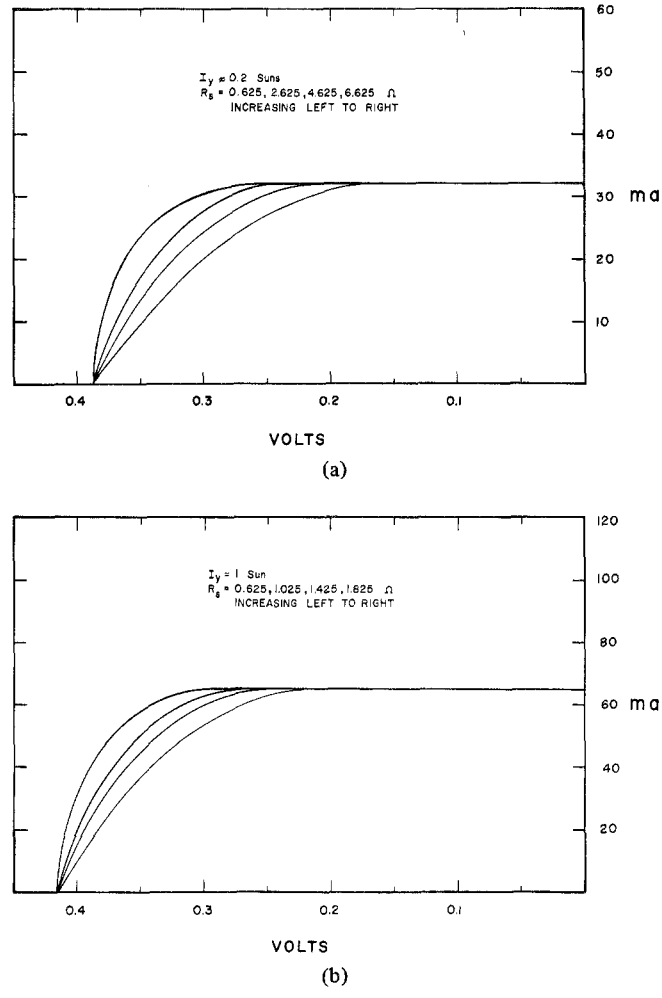


Fig. 7. $V$-$I$ characteristics for a solar cell with $R_s$ as a parameter. (a) Light intensity approximately 0.2 suns. (b) Light intensity approximately 1 sun.

be easily included by adding an additional resistance to $R_d$, as shown in the next section.

## III. Grid Conductor Losses

When each unit cell pair, consisting of an active collection area and a branch grid line, is connected to the main grid conductor, it can be shown how the resistance of the main grid conductor, as compared to the total series resistance of the unit cell pair, affects the total load current available from a group of unit cells.

The losses occasioned by the grid structure are associated with the resistance of the grid material and the contact resistance that occurs at the metal-semiconductor interface. These two effects have the same geometrical distribution and can be lumped together as an effective sheet resistance $r_m$. For the model considered in this paper, the resistance associated with the contacts for one unit cell is given by

$$R_m = r_m W/T. \quad (17)$$

A finite number of unit cell pairs may be represented for the structure shown in Fig. 1 by the lumped element model shown in Fig. 8. The total series resistance per pair of unit cells is

$$R_s = (R_m + R_d)/2 = (r_m W/2T) + (r_s L/4W). \quad (18)$$

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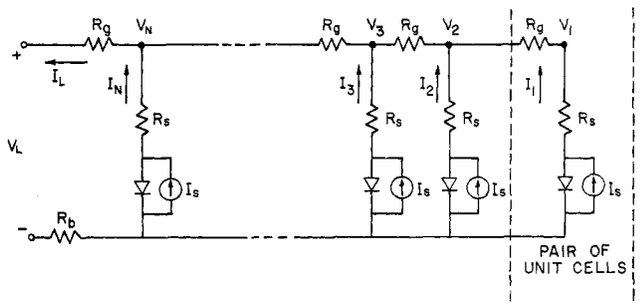


Fig. 8. A lumped element model of a solar cell.

If one starts with unit cell pair 1, then

$$V_1 + I_1 R_s = V_T \ln [(I_s + I_r - I_1)/I_r] \tag{19}$$

$$V_2 + I_2 R_s = V_T \ln [(I_s + I_r - I_2)/I_r] \tag{20}$$

and

$$V_1 - V_2 = I_1 R_g . \tag{21}$$

A combination of the above equations yields

$$I_2 R_s - I_1 (R_g + R_s) = V_T \ln [(I_s + I_r - I_2)/(I_s + I_r - I_1)] . \tag{22}$$

For the normal case of $R_g \ll R_s$, it can be shown that

$$V_T \ln [I_s + I_r - I_2)/(I_s + I_r - I_1)] \simeq 0 \tag{23}$$

and

$$I_2 \simeq (1 + R_g/R_s) I_1 . \tag{24}$$

In general,

$$I_j \simeq I_{j-1} + (R_g/R_s) \sum_{k=1}^{j-1} I_k . \tag{25}$$

By neglecting the higher order terms involving $(R_g/R_s)^n$ for $n \geqslant 2$, one obtains

$$I_j \simeq I_1 \left[ I + (R_g/R_s) \sum_{k=1}^{j-1} k \right] = I_1 [1 + j(j-1)(R_g/R_s)/2] . \tag{26}$$

For a total of $N$ unit cell pairs, the output current is given by

$$I_L = \sum_{j=1}^{N} I_j = I_1 [N + N(N^2 - 1)(R_g/R_s)/6] . \tag{27}$$

Using

$$I_N = I_1 [1 + N(N-1)(R_g/R_s)/2]$$

$$I_L = N I_N \{ [1 + (N^2 - 1)(R_g/R_s)/2] / [1 + N(N-1) \cdot (R_g/R_s)/2] \} . \tag{28}$$

Equation (28) clearly shows the disastrous effect that the grid header resistance can have on the performance of a solar cell. As an example, consider a cell consisting of 20 unit cell pairs with $R_s = (R_m + R_d)/2 = 0.1 + 2.0 = 2.1\ \Omega$ and $R_g = 0.04\ \Omega$. For this case, the total output current is

$$I_L = 45.27\, I_1 = 9.82\, I_{20} \tag{29}$$

which is less than one-half the output current available for zero grid header resistance.

## IV. Conclusions

Solar-cell analysis, particularly for concentrated sunlight conditions, must include the spatial variation in the p-n junction voltage. Such a distributed diode analysis has been used to determine the dependence of the $V$-$I$ characteristics and maximum power output on the ratio of diffused layer resistance to junction dynamic resistance. The results indicate that solar cells should be designed such that

$$(r_s(J_s + J_0) L^2/2V_T) < 0.1$$

in order to maintain the power output per unit cell within 3 percent of that for the lossless case. For concentrated sunlight, it is necessary to use very small grid spacings, possibly as small as 500 $\mu$m, and narrow grid branch lines ($\simeq$5 $\mu$m).

There is still some inconsistency relative to the predicted value for $V_T$. An examination of (12), (13), and (15) would indicate that it is possible to determine $V_T$ from the vertical axis intercept ($R_d = 0$) of the data presented in Fig. 5. Examination of these data reveals an apparent value for $V_T$ varying from 0.02 V to a value in excess of 0.052 V as the cell size and/or light intensity is increased. Data for light intensities greater than 1.5 kW/m$^2$ could not be accurately handled under the present theory because deviations from the linear theory became apparent. All the cells used in obtaining these data were designed for operation in unconcentrated sunlight. For a given cell, as the light intensity is increased, the open-circuit voltage also increases as expected; however, the ratio $V_{oc}/V_T$ decreased, suggesting that $V_T$ is increasing at a rate which seems large relative to the range of light intensity used. An increase in $I_0$ rather than $V_T$ may be an alternative explanation. Access to this information through experimentation has not been accomplished at this time.

As shown in Section III, grid conductor losses can be significant for cell structures which have a number of unit cells connected by a resistive header. Since the primary loss is associated with those unit cells which are farthest removed from the cell terminals, the use of a tapered header to decrease the metal coverage on a cell may be self-defeating. It should always be ascertained that $R_g \ll R_s$ and $R_g$ should be as close to zero as practical. Further, to insure that the p-n structure determines the $V$-$I$ characteristics, the grid finger resistance (including contact resistance) should be much smaller than the diode sheet resistance.

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