Admittance spectroscopy of CdTe/CdS solar cells subjected to varied nitric-phosphoric etching conditions

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In this work we investigate the electric and structural properties of CdTe/CdS solar cells subjected to a nitric-phosphoric (NP) acid etching procedure, employed for the formation of a Te-rich layer before back contacting. The etching time is used as the only variable parameter in the study, while admittance spectroscopy is employed for the characterization of the cells' electric properties as well as for the analysis of the defect energy levels. Particular attention was also given to the characteristics of unetched devices and it is shown that despite the larger height of back-contact barrier such samples show well defined admittance spectra, as well as allow for extraction of as much as five defect levels in the range of 0.08–0.9 eV above the valence band. In contrast, admittance characteristics of the etched samples show a decrease of the number of the detectable trap levels with increasing etching time. (Hence it is usual for only one or two trap levels to be reported in the literature for finished devices.) The latter leads to the anomalous Arrhenius energy plots as well as the breakdown of low-frequency capacitance characteristics for samples etched with times larger than 30 s. The observed effects are attributed to physical thinning of the cells, the etching out of grain boundaries, and the tellurium enrichment of the CdTe surface by NP etching. We also perform analysis of the back-contact barrier height as extracted from dark *I-V* measurements at different temperatures. The dependence of this barrier height on NP etching time is compared with that of conversion efficiency, from which conclusions are drawn about both positive and negative effects of the nitric-phosphoric etch. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2402961]

I. INTRODUCTION

The nitric-phosphoric acid (NP) etch is conventionally applied for the surface treatment of the CdTe absorber layer of CdTe/CdS solar cells, before deposition of back-contact metallic layer.[1–3] This procedure leads to the formation of a Te-rich layer which is believed to lower the barrier for carrier transfer from CdTe into the metal and results in the formation of a low-resistance contact, and hence also in the decrease of the cell series resistance as well as improved efficiency.[4,5] Similar results are obtained using bromine-methanol etching solutions; however, the method, although effective in the laboratory conditions, is difficult to apply on the industrial scale due to variations in the reproducibility from this process and the corrosive nature of the solution.[6] Thus NP etch is used in the industrial processes of, for example, the ANTEC Solar Energy production line for manufacturing CdTe/CdS cells, samples of which are used in the present work.

It is important to note that not only positive but also negative effects of nitric-phosphoric etching were reported in the literature. The latter are as follows. (i) NP etching strongly affects the regions near grain boundaries (GBs) where the etching rate is significantly larger than that on top surfaces of the intragrain regions.[7] (ii) This creates crevices along the GBs, spreading from the top of the CdTe absorber layer into its depth as the etching time increases.[4,5] (iii) At sufficiently long etching times such process leads to the appearance of electrical shunts in a treated cell. (iv) The detrimental effect on conversion efficiency of long etching times has been related to these shunts.[7]

So far the studies of NP etching effects were mostly focused on the analysis of microscopic images and photoluminescence,[5] remote beam induced current,[8] conductivity and *I-V* measurements,[9,10] as well as light and dark *C-V* measurements.[11] There has not been, however, a comparative study of ac electrical properties of the both etched and unetched devices, and neither is there an understanding of the possible effects of the NP etch on the defect distribution and energy levels. In this work we attempt such a study applying an admittance spectroscopy technique to a number of devices etched by the NP acidic mix of a standard ratio, and using etching time as the only variable parameter. Particular attention is also given to the measurements on unetched samples as this is the part which has not been covered in previous studies of admittance on CdTe/CdS solar cells,[12–14] and as we show, it is especially important for the general material characterization. We also perform a comparative study of the effect of etching on the device efficiency versus the effect on the height of back-contact barrier.

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The magnitude of the latter was determined from the analysis of device *I-V* characteristics measured at different temperatures in the dark.

II. SAMPLES AND EXPERIMENTAL TECHNIQUE

Our studies were performed on samples manufactured on the ANTEC Solar Energy AG production line, and hence have a particular relevance to mainstream commercial applications. The samples comprise of indium tin oxide (ITO) layer on soda-lime glass, followed by 100 nm of CdS, and 6–8 μm of CdTe, where both CdS and CdTe layers were deposited by close space sublimation. The structures were then subjected to a standard $CdCl_2$ activation treatment in vapor environment. These manufacturing stages were completed on the ANTEC Solar production line. The following NP etch treatment was done in our laboratory, where varied and well controlled etching times were applied for a series of samples. The devices were completed with a 100 nm thick gold back contact, deposited either on a NP etched CdTe surface or directly without etching. In this study the complete and optimized devices have efficiencies of about 7%–8% (It is known[15] that an additional activation stage, using wet $CdCl_2$ treatment of these industrial cells in laboratory conditions, can increase the device efficiency up to 11%. This treatment, however, was not applied in this work to allow for a direct comparison with industrial processes.)

The composition of the used etching solution was 70% phosphoric acid, 1% nitric acid, and 29% de-ionized water. The following samples were studied in this work: sample I, unetched; sample II, etched for $t=10$ s; sample III, $t=20$ s; sample IV, $t=30$ s; sample V, $t=40$ s; sample VI, $t=60$ s; and sample VII, $t=90$ s.

The admittance measurements were carried out on a Solartron 1260 impedance analyzer equipped with a 1296 dielectric interface. The frequency range used in experiments was from 50 mHz to 1 MHz, and the temperature range was from 150 to 380 K.

III. EXPERIMENTAL RESULTS AND ANALYSIS

A. Admittance of unetched devices

In Fig. 1 the admittance spectroscopy (AS) data[16] are shown for the unetched sample I taken at different temperatures. The imaginary part of admittance is represented by the capacitance-frequency dependence, while the real part is plotted as the conductance divided by the cyclic frequency with a bulk (diode) contribution subtracted from it. The latter contribution is determined as either dc or low-frequency value of the total conductance.[17] As it is seen in Fig. 1(a), there is a clear structure of three peaks in the conductance frequency dependence at room temperature, indicating the presence of at least three defect energy levels in the spectrum. It is also seen that the positions of these peaks correspond to the steplike curvatures of $C(f)$, as expected from admittance spectroscopy theory.[16,18]

Recently a revised approach has been suggested to admittance characteristics of a *p-n* junction containing deep levels in the depletion region, which employed a concept of single defect capacitance and also included a rigorous evaluation of displacement currents in the system.[19] In particular, the proposed formulation of that work suggests a simple relation between normalized conductance and capacitance for the case of weak screening:

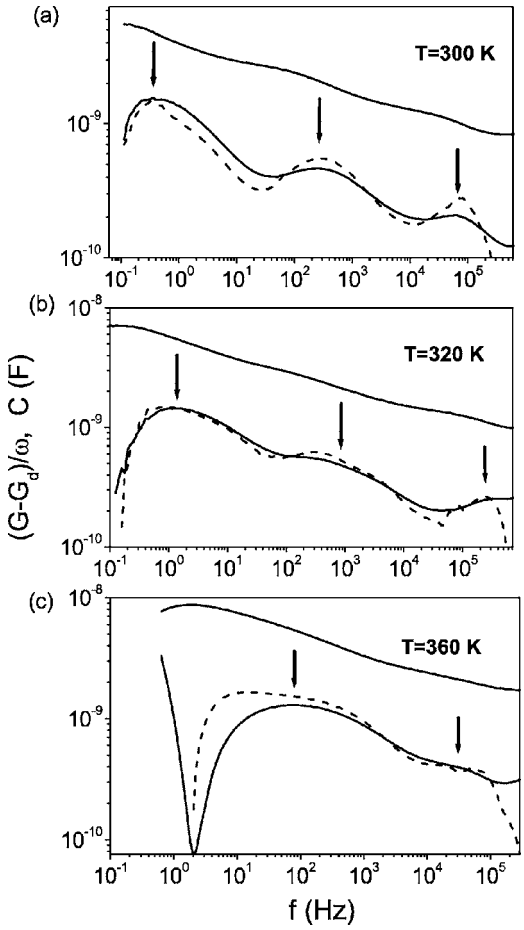

FIG. 1. AS data measured at different temperatures for an unetched sample (sample I). Lower solid lines, frequency dependence of normalized conductance $(G-G_d)/\omega$; upper solid lines, frequency dependence of capacitance C. The dashed lines correspond to the logarithmic derivative: $(-\pi/2)dC/d\ln f$. The arrows indicate the positions of the conductance peaks—they shift with increasing T.

$$\frac{G-G_d}{\omega} = -\pi\frac{dC}{d\ln\omega} = -\pi f\frac{dC}{df}, \tag{1}$$

where G is the total ac conductance of the cell, G_d is the dc conductance, C is the total capacitance, and $\omega=2\pi f$ is the cyclic frequency.

In Ref. 19 the equation was tested on a CdTe/CdS cell, showing good agreement with experiment. Importantly, for the cell studied in Ref. 19 no distinct defect levels were detected in the conductance spectrum. We have applied Eq. (1) to the $C(\omega)$ shown in Fig. 1 and have found a good agreement with $[G(\omega)-G_d]/\omega$ dependence, though the best fit is obtained with a factor of $\pi/2$ [dashed lines in Figs. 1(a)–1(c)] instead of π. The latter can be due to the fact that the condition of weak screening as defined by theory is not strictly fulfilled in our unetched samples (further discussion of this point is provided below).

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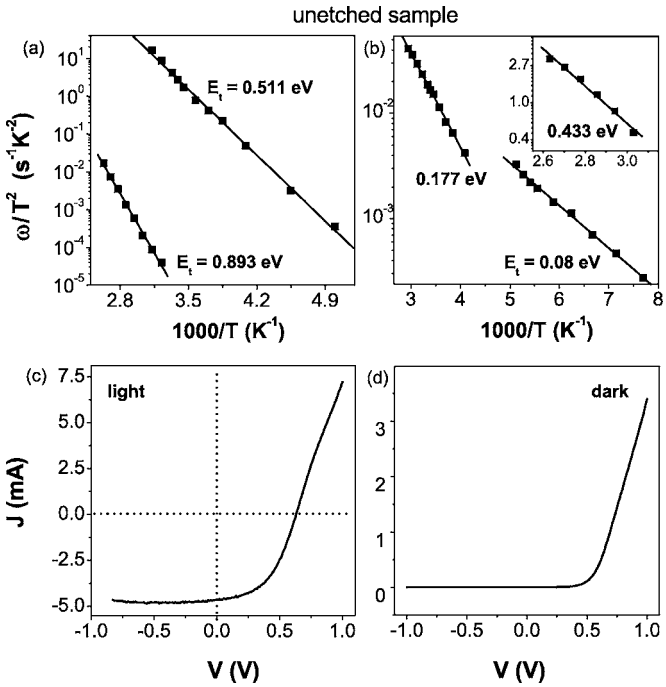

FIG. 2. [(a) and (b)] Arrhenius plot of the normalized conductance peak positions for sample I (unetched). Symbols, experimental data; solid lines, linear fits. [(c) and (d)] light and dark *I-V* characteristics of the same sample.

As the temperature is increased, the frequency at which the individual impurity level responds to the applied ac modulation changes as[17]

$$\omega_I = 2\xi_0 T^2 \exp\left(-\frac{E_t - E_V}{kT}\right), \tag{2}$$

where E_t is the trap energy, E_V is the top of the valence band, and ξ_0 is the temperature-independent emission parameter. This dependence leads to shifting of the conductance peaks to higher frequencies with increasing temperature, as can be seen in Figs. 1(b) and 1(c). Thus, from the analysis of the peak positions at different T one can extract the trap energy E_t corresponding to each of the observed peaks. It has to be mentioned here that the formalism discussed above is valid only when the carrier mobility of the sample is high enough and the T dependence of the thermal velocity can be given by the free band approximation ($V_{\text{th}} = \sqrt{kT/2\pi m^*}$, where m^* is the hole effective mass).[18] In practice it is impossible to determine the mobility of the carriers in a fully completed solar cell, and a separate study of the films of absorber layer material subjected to the same treatment is necessary.[20] Previous work on CdTe/CdS solar cells, however, indicates that the above formalism is well applied to this system,[12–14,21] and as is shown below, it also describes self-consistently the experimental data obtained in this work, suggesting that the mobility of the studied samples is reasonably high.

Experimentally, we have observed five peaks in the conductance frequency dependence of unetched samples, which was measured in the temperature range of 150–380 K. The resulting Arrhenius plots for these data are shown in Figs. 2(a) and 2(b). The slope of $\ln(\omega/T^2)$ vs $1/T$ linear dependence provides the value of the trap energy E_t as follows from Eq. (2). The energy levels extracted this way are summarized in Table I.

As it is seen from the table, the comparison of these energy values with those reported for CdTe previously [as obtained by both deep-level transient spectroscopy (DLTS) and AS] shows a good agreement. We would like to emphasize that the above results indicate that unetched samples are well characterized by conventional admittance spectroscopy, derived theoretically for structures with only one *p-n* junction or Schottky barrier, and despite of the well known fact that unetched devices have a large back-contact barrier, giving rise to appearance of a Schottky diode near the contact. The latter leads to the presence of two back-to-back diodes in the equivalent circuit of the solar cell, and hence the evaluation of the admittance should be adjusted for such a case. Empirically, however, the methodology derived for admittance in the one diode case is still valid for the case of unetched devices, as evidenced by both (a) clear Arrhenius plots [strictly linear $\ln(\omega/T^2)$ vs $1/T$ dependence, Fig. 2] and (b) a good agreement between extracted trap energy values with that known in the literature values. Moreover, the obtained relation between the derivative of $C(\omega)$ and the normalized $G(\omega)$, Fig. 1, further supports this conclusion.

One of the possible explanations as to why there is in the admittance spectra a response from only one barrier related to *p-n* junction, but not from the barrier due to back contact, can be obtained from the observation done in Ref. 30. It was noticed for fully processed CdTe/CdS devices that the impedance spectra presented on the Nyquist plot show only one semicircle in normal conditions, and can be well described by equivalent circuit model suggesting only one diode/barrier structure. However, at a certain dc bias applied, a second semicircle on the Nyquist plot started to become visible in the high-frequency range of the spectra, suggesting the presence of a second barrier due to back contact.[30] From this we suppose that the ac response from the back contact occurs predominantly in the range of high frequencies, and is enhanced by dc bias, while at zero bias and in the lower frequency regime, where the response from defect levels is studied, the ac spectra are relatively undisturbed. A more detailed experimental investigation of this problem is under way.

TABLE I. Defect energy levels in the unetched sample as extracted from AS data and compared to literature values E_t^*, measured with respect to the top of the valence band E_V.

E_t (eV)	0.893	0.511	0.433	0.177	0.08
E_t^* (eV)	0.86–0.93	0.49–0.54	0.43	0.17–0.185	0.07–0.09
Defect	V_{Cd}^{2-}	Cd_i^{2+}	V_{Cd}^{-}	$V_{Cd}^{2-}-Cl_{Te}^{+}$	As, P
Refs.	[21 and 22]	[23–25]	[23 and 26]	[23 and 25]	[27–29]

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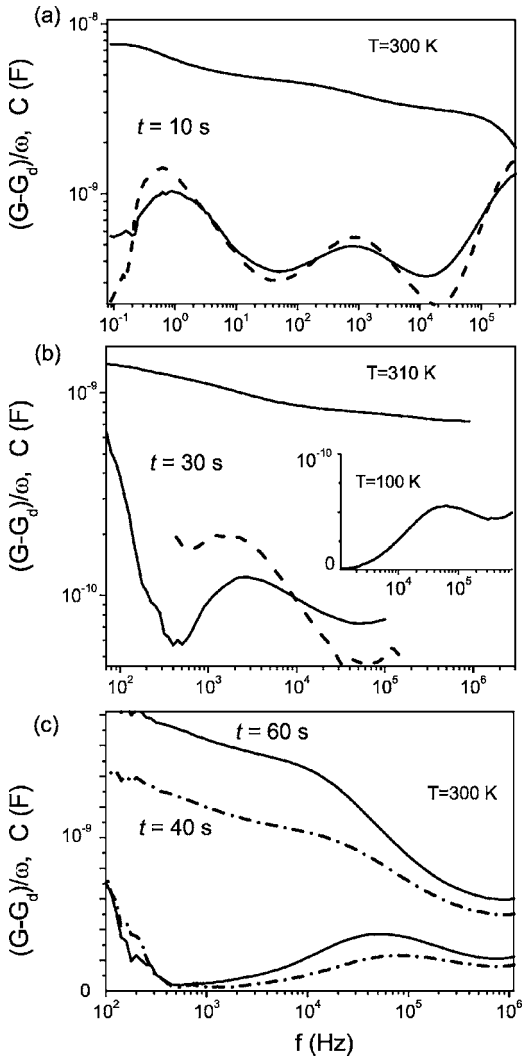

FIG. 3. AS data of four NP etched samples at near to room temperature. (a) Sample II etched for 10 s and (b) sample IV etched for 30 s (the upper solid lines correspond to capacitance, while lower solid lines to normalized conductance). The dashed lines in (a) and (b) correspond to the logarithmic derivative of the capacitance $(-\pi/2)dC/d\ln f$. The inset to (b) shows normalized conductance of sample IV at $T=100$ K. (c) AS data for samples V and VI etched for 40 (dash-dotted lines) and 60 s (solid lines), respectively; the two upper lines correspond to capacitance.

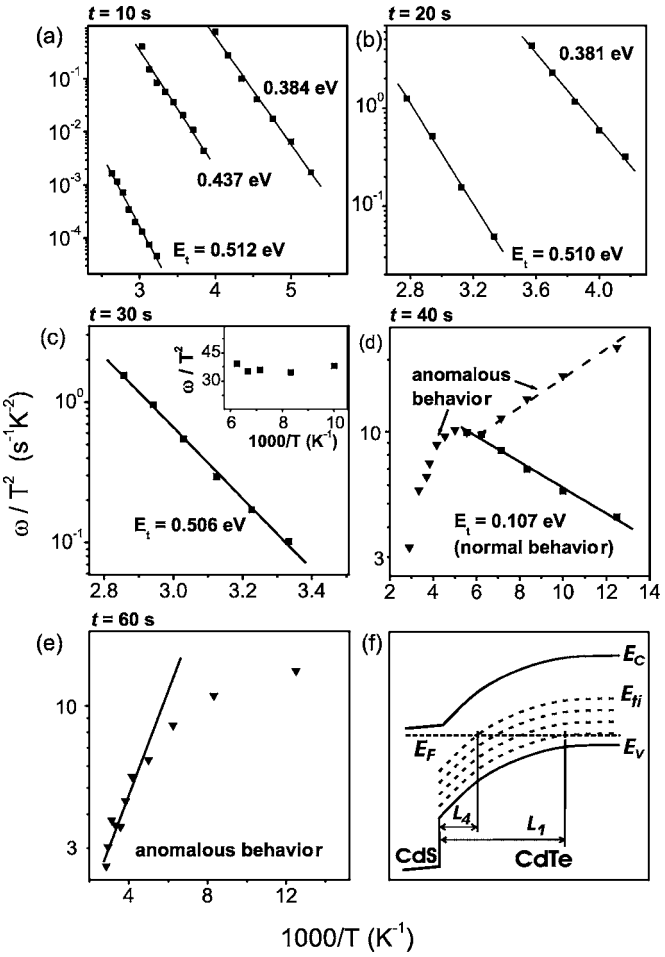

FIG. 4. [(a)–(e)] Arrhenius plots of the peak positions of admittance maxima for five samples (II–VI), etched for different time t as indicated on the plots. Symbols, experimental data; solid lines, linear fits. (f) Band diagram of p-n junction in CdS/CdTe solar cell. The dashed lines indicate positions of deep and shallow levels.

B. Effects of varied NP etching

Applying NP etching for different periods of time before deposition of gold back contacts allows the study of the effect of the formation of Te-rich layer at the surface of CdTe on electric properties as well as cell performance.[4,5,7] Our AS data for samples II and III etched for 10 and 20 s, and as taken over the entire temperature range, show structures of several peaks in normalized conductance, which are similar to those in Fig. 1 for the unetched device [typical traces for sample II are shown in Fig. 3(a)].

The situation becomes significantly different as etching times of 30 s or more are introduced. For each of these samples only one peak was observed in the studied frequency range at $T>250$ K, Figs. 3(b) and 3(c), although an additional peak was observed for sample IV ($t=30$ s) at low temperatures, as shown in the inset of Fig. 3(b). Also, for sample V an unexpected splitting of the high temperature peak [Fig. 3(c)] was observed at $T<200$ K (not shown), and at the same time the single conductance peak of sample VI [also shown in Fig. 3(c)] has a position almost independent of T in the entire range. For sample VII (not shown), which was etched for 90 s, no peak structure was observed at all in the entire temperature range. Also, a good fit of the conductance data is obtained by Eq. (1) for the 10 s etched sample, with the same coefficient of $\pi/2$, Fig. 3(a), as in case of the unetched devices. At larger etching times the observed correspondence is no longer fulfilled as seen in Fig. 3(b) for $t=30$ s.

More information about the effect of etching can be extracted from the Arrhenius plots. In Figs. 4(a) and 4(b) such plots are given for samples II ($t=10$ s) and III ($t=20$ s). It is seen that the behavior of the peak positions is well described by the theoretical expression, Eq. (2), which is also in agreement with previous studies on fully processed CdTe/CdS devices.[13,21] For these samples we have observed three and two defect levels, respectively, as seen on the plots [Figs. 4(a) and 4(b)]. The levels at energies near 0.51 and 0.43 eV compare well with the ones identified for unetched devices (Table I), while the level at 0.38 eV appears only in these two etched samples. The latter level was observed previously

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in CdTe/CdS solar cells grown by electrodeposition,[31] and was attributed to the formation of Cd vacancy related defects resulting from residual acceptor impurities in the electrolyte solution. In our work, where the 0.38 eV level was observed only in the etched devices, it is clear that some action of the etching introduces this level. This may be by, for example, unintentional impurity doping or by creation of V_{Cd} related defects[31] during tellurium enrichment of the near-surface region.

Figure 4(c) shows the Arrhenius plot for sample IV ($t=30$ s) and for which the behavior of the high T peak position is also well described by Eq. (2). Only one deep level at 0.507 eV is detected, which is in agreement with previous results on samples I-III, which all show the presence of a level near 0.51 eV.

The inset to Fig. 4(c) shows a similar plot for the low T conductance peak of sample IV, and the observation that the parameter ω/T^2 is almost independent of temperature signifies either a very shallow trap energy of this state or a breakdown of the transport characteristics at low T caused by NP etching process. Further support for the latter can be seen from Figs. 4(d) and 4(e), where, firstly, only a part of the ω/T^2 vs T^{-1} can be described by the expected dependence with ($E_t=0.107$ eV) for sample V, while no part of the data agrees with normal behavior at all for sample VI (clearly the same can be said about sample VII as no conductance were observed in AS spectra). Thus, a clear progressive deterioration of the experimental ability to probe defect states by AS is seen with an increase of the etching time above 30 s.

The deterioration also correlates with the reduction in the number of levels resolved, which starts with five defect levels detected on unetched devices, changing to three levels on 10 s etched, and to two and one levels on 20 and 30 s etched samples, respectively. Also, and very importantly, one can notice that mostly shallower trap levels disappear first from the energy plots, and secondly, at $t=30$ s only the deep level at $E_t=0.51$ eV is observed. [We find that the 0.86 eV level, observed in unetched devices but not seen in AS spectra of the etched samples, is masked in the latter case by a large low-frequency tail in $G(\omega)$, which develops with increasing t; see Fig. 5(a).]

Qualitatively such behavior can be understood from the analysis of the band diagram of the CdTe/CdS solar cell and its relation to the ac response as measured by admittance spectroscopy. In Fig. 4(f) the position of defect levels in the band gap of CdTe absorber layer is shown by dashed lines. As it is seen they cross the Fermi level at various spatial distances from the CdTe/CdS junction depending on the magnitude of any particular level: deep ones cross closer to the junction, while shallow levels cross further away from the junction and closer to the back contact (right-hand side of the diagram). The ac response comes only from the states close to the Fermi level, hence the defect levels detected by admittance spectroscopy are well defined in both their energetic and spatial positions.

As the NP etching is commenced from the surface that has become the back contact, CdTe is dissolved and the layer is thinned. Hence the material which contributes to ac response is removed. The deeper the etching, the more of the regions where shallower levels are crossing Fermi level will be gone, therefore suppressing their respective contributions in the admittance spectra.

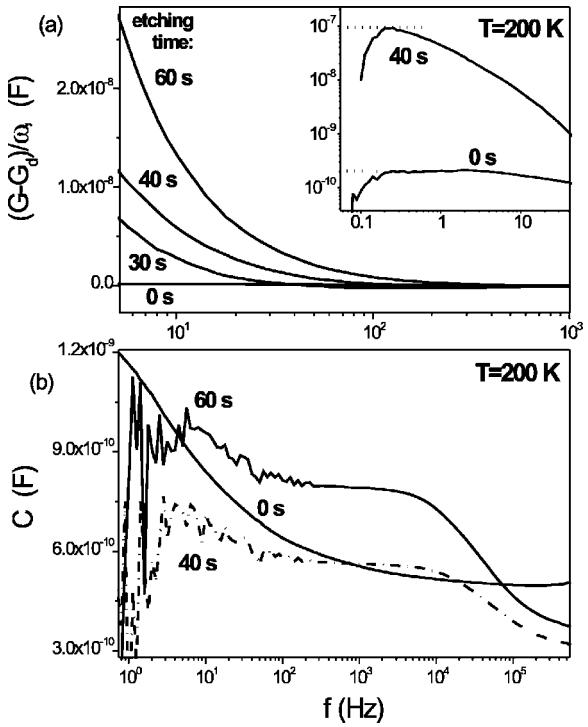

FIG. 5. (a) Normalized conductance in the low-frequency range for samples I, IV, V, and VI (etched for $t=0$, 30, 40, and 60 s, respectively). Inset: Zoom-in of the data at $f<10$ Hz for samples I and V. (b) Low-frequency capacitance for samples I, V, and VI, demonstrating the drastic change in $C(f)$ caused by the NP etching at $f<100$ Hz. The data in (a) and (b) were obtained at $T=200$ K.

However, it has been reported previously that NP etching not only induces formation of the Te-rich layer on the surface of CdTe absorber layer and thus thins off this layer but also causes etching and enrichment by Te along the grain boundaries, deep into CdTe layer when the etching times are sufficiently long.[5,7] It is also important that such "selective" etching of GBs occurs at much faster rates than that of intragrain regions. From this one can suggest that the etching effect of suppressing the ac response from shallower defects points out that such response comes mostly from grain boundaries, and not from the intragrain regions which remain relatively intact after 20–30 s long etch. (The latter is easily verified by the measurements of the overall thickness of the film after etching.) Therefore, this implies, firstly, that the charged defects contributing to the carrier transport are mostly located in the GBs and not the interior of the grains, and, secondly, that the etching suppresses responses from such defects.

One important point should be made regarding the observed effect of disappearance of shallower levels with increasing etching time. In principle, one could suggest a link between this effect and the change in the electric field near the CdTe surface induced by a change in the back-contact barrier height. The back contact is always associated with downward band bending,[4] but the magnitude of this is reduced by increased etching time [see later and Fig. 6(b)]. The

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band bending shifts both the top of the valence band and trap energy levels in that region, with respect to the Fermi level. In this case, to explain the observed phenomenon, the shallow trap levels E_t should be shifted below the Fermi level E_F, so that there would be no crossing of E_t and E_F [Fig. 4(f)], and hence no contribution to the ac signal from such states. In reality, however, the effect of etching on the back-contact electric field is opposite: as the *etching* is increased the barrier for holes is lowered, i.e., its electric field is decreased, thus leading to shifting upwards of both E_V and trap levels E_t with respect to the Fermi level in the region close to the back contact.

Therefore we believe that back-contact effect does not influence the observed phenomenon and suggest that the transformation of the admittance spectra observed under increasing NP etching time is a result of grain boundary modifications (as grain boundaries are etched out). One of the most obvious mechanisms of such modification, and as mentioned above, can be a result of Te enrichment at grain boundaries, which would effectively cause a drop in GB resistance (R_{GB}). Moreover, the capacitive properties of grain boundaries are also changed in this case—firstly by additional doping (segregation) inside of them and secondly by the effective "screening" of electrical field of the depletion region inside of grain boundaries—if the amount of enriched Te is large.

This interpretation is supported by the low temperature data shown in Fig. 5, where the low frequency $(G-G_d)/\omega$ and C measured at $T=200$ K are plotted for samples I, IV, V, and VI. Low temperature is beneficial for the study of both screening and impurity effects, as the contribution from phonon activation is reduced in the transport phenomena. One can see that there is a dramatic increase in conductance (or $1/R_{GB}$) at $f<100$ Hz as the etching time is increased from 0 to 60 s. [Fig. 5(b)]. Such enhancement of the low-frequency tail of the conductance indicates a significant increase in the concentration of deep-level states (which have low response frequencies), and this is most likely to be caused by the increased enrichment of Te from the free surface into the bulk of the CdTe layer as described above. [As is seen in the inset to Fig. 5(a), the maximal difference in normalized conductance between unetched and 40 s etched samples reaches almost three orders of magnitude.]

On the other hand, Fig. 5(b) shows that capacitance of the etched samples is also dramatically affected in the low-frequency range as compared to unetched sample. At $f<100$ Hz the $C(f)$ dependence first becomes very noisy, and at $f<10$ Hz it starts rapidly decreasing, indicating a complete breakdown in the transport.

Clearly, the low-frequency capacitance behavior correlates with the observed increase in the conductance at low f, indicating that the suggested mechanism of enhanced GB conduction can indeed take place and lead to "squashing" of the depletion region inside of GBs, as well as to shunting of the depletion region capacitance of the CdTe/CdS junction of the cell. The last two effects (from GB capacitance and capacitance of the junction) should, in principle, contribute to the total capacitance simultaneously, which makes discrimination between their respective roles difficult in this experiment. This, however, can be a subject of future investigation. Two important conclusions can be drawn from the above observations: (i) that the carrier transport of both etched and unetched devices is dominated by properties of their GB regions and (ii) that excessive NP etching ($t>30$ s) significantly alters the electric properties of the cells and can even shunt the cells completely via highly conductive GBs at larger etching time.

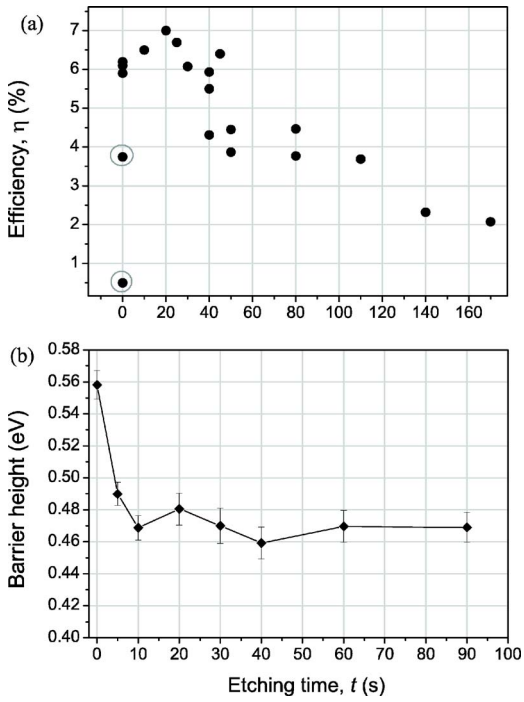

FIG. 6. Dependence on the NP etching time of (a) light conversion efficiency and (b) back-contact barrier height. NP etching reduces the large scatter of efficiencies seen for unetched cells and eliminates low performing contacts (circled points).

C. Cell efficiency versus back-contact barrier height

In the context of the above observations for large NP etching times it is important to assess carefully both positive and negative effects of etching at the intermediate periods ($t<30$ s). For this purpose we carried out a comparative study of conversion efficiency and back-contact barrier height at different etching times t (Fig. 6).

The cell efficiencies were obtained from I-V curves measured under 1.5AM illumination from a solar simulator, while the barrier height at the back contact was determined from temperature dependence of the series resistance of the cell extracted from I-V measurements in the dark at varied temperatures (from 100 to 300 K). The latter method is described in detail in Ref. 32.

As it is seen in Fig. 6(a), the efficiency η of unetched samples is relatively high in most cases with respect to the maximal value of about 7%. At the same time these values are quite narrowly distributed (around 6% in this case). However, at *some* instances (approximately three times out of ten) the efficiency can be quite low as indicated by two encircled points on this plot. We believe that such low values are associated with the cleanness (or lack of such) of the

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CdTe surface before back contacting. This is confirmed by the fact that as soon as NP etching is introduced the large range of such scatter (from 0.5% to 6%) disappears altogether. (We note, however, that high efficiency values of about 10%–11% have been obtained previously without wet etching prior to back-contact deposition.[12]) The efficiency rises with increasing etching time, reaching maximum at $t \simeq 20$ s, after which it gradually decreases ($t > 90$ s). The optimal value of the NP etching time is known to vary from one laboratory to another, typically between 20 and 60 s. In our experience such variation is strongly dependent on how long the samples were kept in open air after their manufacture and before back contacting, i.e., on the thickness of the oxide layer formed on the surface. For this work the samples were kept in vacuum immediately after receiving them from the manufacturer, hence lower optimal etching time t. It is also important to mention that out of all the parameters defining the quality of I-V curves of the etched samples, i.e., the conversion efficiency of the cells, it is the short circuit current (J_{sc}) which is affected the most by variation of t. For example, J_{sc} decreases by a factor of 2 or more from its maximal value within the period of $t \sim 100$ s, while the filling factor (FF) decreases only by about 20% and the open circuit voltage (V_{oc}) remains practically unchanged. For the case of the etching time $t=0$, the main difference between well performing cells (with $\eta \approx 6\%$) and those with poor quality [as the ones encircled in Fig. 6(a)] is mostly the difference in V_{oc} and FF which determines the drop in efficiency. According to our observations the latter takes place because of the well known "roll-over" effect in I-V characteristics, which is attributed to poor quality of back contact.

The dependence of the back-contact barrier height on t is shown in Fig. 6(b). The magnitude of the barrier drops from 0.56 eV for unetched sample to approximately 0.47 eV in the first 10 s of etching, after which it remains constant within the experimental error. It is important to point out that for the plot in Fig. 6(b) we have chosen the unetched device of the poorest quality from the set described above (with the light conversion efficiency of only 0.5%) which, as one would expect, should have the largest value of the back-contact barrier, which is indeed the case as direct measurements show. Nonetheless, one can see from the plot that even in this worst case scenario the overall change in the barrier height is only of about 20% (from 0.56 to 0.47 eV). This points out that although NP etching improves the cell performance of the cells, it does not eliminate completely the back-contact barrier.

Another important conclusion which can be drawn from Fig. 6 is that there is a significant difference between optimal etching time for maximal efficiency $t=20$ s and the time when the back-contact barrier reaches its saturated value $t=10$ s. This implies that continual improvement in efficiency after the first 10 s of etching is not related to the magnitude of the barrier, and hence formation of the Te-rich layer on CdTe surface, but rather has a different origin. We believe that it is most likely caused by the relatively fast etching along the grain boundaries and by the enrichment of this GB regions with Te, for these are the strongest modifications in electrical and structural properties of the etched cells, as it was discussed in the previous section [see Figs. 4(a) and 4(b)]. This implies, however, that Te enrichment of GBs is not entirely a negative effect (as in creating electrical shunts), but, in fact, it has a positive characteristic if the etching times are not larger than a certain value. The nature of such positive characteristic could be the substantial increase in the "effective" back-contact area, with highly conductive (Te-filled) regions of GBs acting as extra collectors of the photogenerated and diffused carriers.

IV. DISCUSSION AND CONCLUSIONS

From our results on unetched devices we can conclude, firstly, that unetched devices can be well characterized by conventional AS, and the interference from the back-contact Schottky barrier can be neglected at least on an empirical level. (It is important to stress, though, that this result was obtained on samples which were stored in vacuum prior to back-contact deposition, thus avoiding the formation of a thick oxide layer on the surface of CdTe.) Secondly, the admittance spectra of unetched devices reveal much richer structure than that of etched samples, with as many as five defect levels detected. It should be pointed out that previously the maximal number of energy trap levels extracted from AS data for a single CdTe/CdS device, as reported in literature, was not more than 2. (This being for fully processed devices, implying NP or Br–MeOH etching before back contacting.) This suggests that it can be advantageous to characterize unetched devices as opposed to the etched ones, if the purpose of the study is the characteristics of the constituent materials (CdTe absorber layer, etc.) Also, in this case one would eliminate the additional source of traps from wet etching [as it was shown in Figs. 4(a) and 4(b) the additional level at 0.38 eV was detected in etched samples].

We have also shown that the capacitance data and frequency dependence of conductance of the unetched sample (Fig. 1) obey the theoretically predicted proportionality [Eq. (1)] and directly correlates with the results on the etched samples [Fig. 3(a)], which additionally verifies the conclusion about applicability of the known formulation for AS to unetched devices. It is interesting that in both etched and unetched devices the coefficient of proportionality in Eq. (1) turns out to be $\pi/2$ instead of the theoretical value of π. In the revisited admittance spectroscopy theory[19] which includes the evaluation of displacement current, Eq. (1) was obtained for the case of weak screening. The verification criterion for such a regime is by the small variation of capacitance over the entire frequency range, which, however, is not fulfilled for the samples studied here where C varies by a factor of 3 or more. On the other hand, it was pointed out[19] that the validity of Eq. (1) should also hold beyond the weak screening case, hence the observed correspondence with a smaller prefactor in this work might be expected.

The progressive effect of NP etching with time as measured by AS can be summarized as follows: (1) shallower trap levels disappear first from the AS energy plots, (2) at $t=30$ s only the deep level at $E_t=0.51$ eV remains resolved, (3) this can reflect the disruption of ac response due to spatially deeper etching, with the predominant effect being on

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grain boundaries, (4) in the context of (3), the disruption of ac response indicates that trap/defect levels detected by AS are mostly concentrated near GBs, and (5) that etching off of this region leads to Te enrichment as well as quenching of the electric field inside of GBs. The latter effect is also found to be beneficial in terms of enhanced current collection and thus improved conversion efficiency for etching times up to 20 s.

From these observations it is also possible to suggest that the positive effect observed by Te enrichment of GBs can be utilized and improved using the introduction of other materials for intentional doping. Perhaps considerable improvement obtained in conversion efficiency of samples with back-contact containing copper bears direct relevance to this,[33] as Cu atoms are known to diffuse easily through CdTe layer, and hence in principle they can accumulate at GBs. (The evidence for that mechanism has been reported recently.[34]) The improved control of such diffusion of Cu or other metal can potentially be utilized in rigorous grain boundary engineering, and perhaps even assist in overcoming the time instability known for CdTe/CdS solar cells containing Cu.

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