Pentacene-based metal-insulator-semiconductor memory structures utilizing single walled carbon nanotubes as a nanofloating gate

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A pentacene-based organic metal-insulator-semiconductor memory device, utilizing single walled carbon nanotubes (SWCNTs) for charge storage is reported. SWCNTs were embedded, between SU8 and polymethylmethacrylate to achieve an efficient encapsulation. The devices exhibit capacitance-voltage clockwise hysteresis with a 6 V memory window at ± 30 V sweep voltage, attributed to charging and discharging of SWCNTs. As the applied gate voltage exceeds the SU8 breakdown voltage, charge leakage is induced in SU8 to allow more charges to be stored in the SWCNT nodes. The devices exhibited high storage density ($\sim 9.15 \times 10^{11}\,cm^{-2}$) and demonstrated 94% charge retention due to the superior encapsulation. © *2012 American Institute of Physics*. [doi:10.1063/1.3675856]

Floating gate memory devices with discrete charge storage nodes display longer charge retention characteristics than the traditional continuous floating gate equivalents.[1,2] Typically, Au, Ag, or Ge nanocrystals (NCs) or C_{60} nanocomposites are utilized as discrete charge storage nodes in metal-insulator-semiconductor (MIS) or transistor memory devices.[3–5] Issues related to lack of chemical inertness, mechanical and thermal stability of such NCs and nanocomposites hinder their applications as storage nodes in organic nonvolatile memory devices (ONVM).[6] Carbon nanotubes (CNTs) were found to be more favorable for such applications because of their higher thermal stability, chemical inertness, reduced surface states and favorable work function (4.8 eV for pristine CNTs).[6] CNTs embedded in a high-k dielectric were reported as a nanofloating gate in MIS (Ref. 7) and transistor memory devices.[6] The nearly ideal surface states enhances CNTs' charge retention characteristics compared to that of metallic NCs.[8,9] Their high thermal and mechanical stability and relative chemical inertness also make CNTs attractive choices for organic and flexible electronics applications. Earlier reports of hybrid CNT memory devices[6,7] describe structures fabricated using SiO_2 dielectric because SiO_2 is well characterized, therefore simplifies the analysis of the effects of CNTs. However, Si/SiO_2 is not suitable for use in flexible electronics which requires the memory devices to be built up using organic semiconductors and insulators ("all organic").

We report on the fabrication and characterization of a SWCNTs and pentacene-based ONVM device consisting of a MIS structure, which exhibited a relatively large memory window at low sweeping voltages and high charge retention. SWCNTs were sandwiched between SU8 photoresist and polymethylmethacrylate (PMMA) insulators to serve as charge storage nodes. The device structure, shown in Fig. 1(a), consists of Al/SU8/SWCNTs/PMMA/pentacene/Au layers. Such devices are critical for the development of a range of new applications in flexible and plastic electronics.[3]

Poly(ethyleneimine) (PEI) ($M_w = 25\,000$), poly(acrylic acid) (PAA) ($M_w = 4\,000\,000$), sodium dodecyl sulphate (SDS), PMMA, and pentacene were purchased from Sigma-Aldrich and SU8 obtained from MicroChem Corp (MCC). Commercial SWCNTs (purchased from Carbon Nanotechnologies Inc.) were purified until the impurity content was

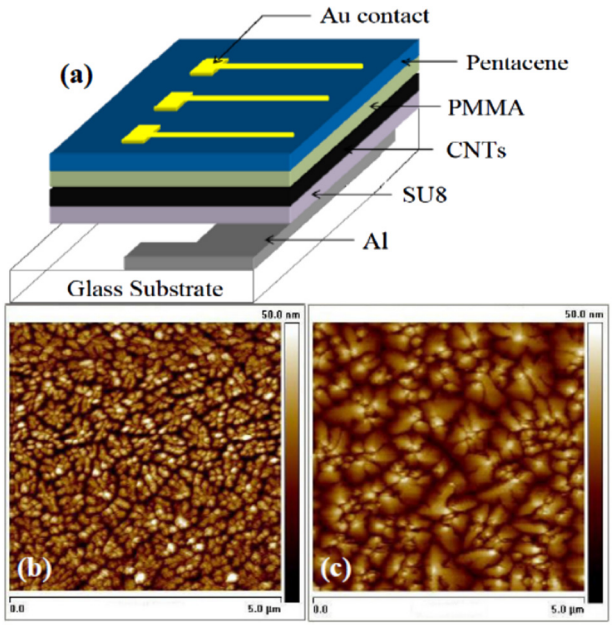

FIG. 1. (Color online) (a) Schematic diagram of the Al/SU8/CNTs/PMMA/pentacene/Au device. $5 \times 5\,\mu m$ AFM images of pentacene grown on (b) SU8 and (c) PMMA.

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below 5 wt. %. The purchased SWCNTs have 2/3 semiconducting and 1/3 metallic CNTs according to the manufacturer data. These were combined for the fabrication of the device shown in Fig. 1 as follows:

A glass substrate was cleaned using a piranha solution and a 100 nm thick Al gate was thermally evaporated through a shadow mask. A 90 nm thick layer of SU8 was spin coated (30 s at 3000 rpm, then baked for 5 min at 95 °C) and UV cross-linked to serve as a gate dielectric. SWCNTs were deposited by the layer-by-layer (LbL) deposition, a technique based on a charge reversal to build up bi-layer assemblies of oppositely charged (functionalized) molecules. The details of this technique and various SWCNT film architectures are reported elsewhere.[10,11] Briefly, the deposition began by the alternate immersion of the substrate in aqueous PEI (cationic, pH = 8.5) and PAA (anionic, pH = 6.5) solutions, for 15 min each to form seed layers to facilitate the adhesion of SWCNTs onto the SU8 layer. The substrate was then repeatedly immersed in PEI solution for 15 min then $SWCNT_a$ solution (anionic SWCNTs, dispersed in SDS) for 30 min. The final SWCNTs matrix consisted of three $SWCNT_a$-PEI bilayers. The diameter of the SWCNTs utilized as charge storage elements in this investigation is estimated to be in the order of 1.5-2 nm.[12]

PMMA (20 wt. % in chlorobenzene) was subsequently spin coated to a 40 nm thickness and baked for 25 min at 120 °C. Pentacene was thermally evaporated at a rate of 0.01-0.07 nm/s to a thickness of ~30 nm. Finally, 30 nm of gold was deposited, through a shadow mask, to form Ohmic contacts. A PC driven LCR Bridge (HP-4192) was used to record the capacitance-voltage (C-V) behavior of the devices at 400 kHz with a 0.5 V/s scan rate. Each test consisted of a double sweep (positive–negative) at room temperature in air. The morphology of the pentacene layers deposited on SU8 and PMMA was investigated by atomic force microscopy (AFM) and shown in Fig.1. Films grown on SU8 (Fig. 1(b)) exhibited fine polycrystalline structures with insulating characteristics. In contrast, relatively large grain sizes (~1.2 μm) were found when pentacene was deposited on PMMA, Fig. 1(c). This indicates that the substrate chosen for deposition significantly affects the electronic properties of the pentacene film. Since larger pentacene crystals are generally associated with superior semiconducting performance,[13] we utilized PMMA for the top dielectric on which pentacene was grown. Conversely, SU8 was utilized as the gate dielectric due to its chemical stability during the SWCNTs deposition process.

A control device Al/SU8/PMMA/pentacene/Au was fabricated without SWCNTs and its C-V characteristic is shown in Fig. 2(a). The control device exhibited the usual characteristics of MIS structures based on p-type semiconductors, with flatband voltage of −2.5 V and full semiconductor depletion at 0 V. The double voltage sweep exhibited no hysteresis which is indicative of the absence of charge trapping in the bulk dielectrics and at the surfaces of the SU8 and PMMA layers. Assuming that the MIS structure consist of an insulator capacitance (C_{Ins}) connected in series with a semiconductor capacitance (C_S), the C-V characteristics of the control devices may be used to extract fabrication parameters. The majority carriers accumulate at the interface

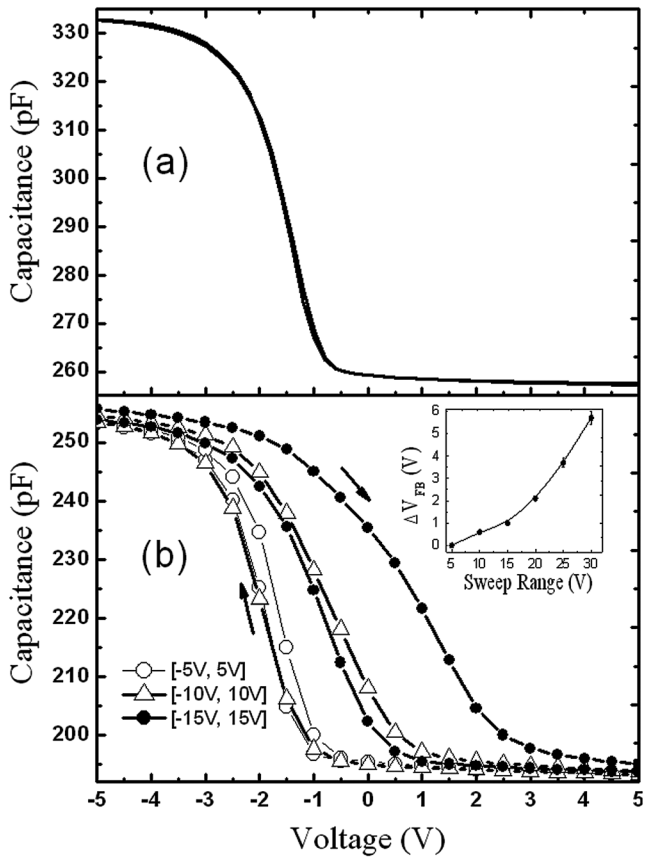

FIG. 2. C-V double sweep of (a) control device Al/SU8/PMMA/pentacene/Au and (b) SWCNT embedded memory device: Al/SU8/CNTs/PMMA/pentacene/Au.

between the insulator and the semiconductor when the device operates in the accumulation region. Thus, the maximum accumulation capacitance ($C_{max} = 332$ pF) can be used to estimate the dielectric constant of the insulator stack, $C_{max} \cong C_{Ins} = A\ \epsilon_{Ins}/d_{Ins}$,[14] where ϵ_{Ins} is the dielectric constant of the SU8/PMMA insulator stack, d_{Ins} the cumulative SU8 and PMMA thickness, and A the device area (1 mm^2). Using the insulator stack thickness measured using AFM (130 nm), we obtained $\epsilon_{Ins} = 43.18 \times 10^{-12}$ F/m, corresponding to an effective relative permittivity of 4.88. The intrinsic doping concentration (N_a) of the pentacene thin film semiconductor is calculated using,[14]

$$C_{FB} = A\frac{\epsilon_{Ins}}{d_{Ins} + \frac{\epsilon_{Ins}}{\epsilon_S}\sqrt{\frac{K_bT}{e}\frac{\epsilon_S}{eN_a}}}, \quad (1)$$

where C_{FB} is the flatband capacitance, ϵ_S is the dielectric constant of pentacene ($3 \times 8.85 \times 10^{-12}$ $F.m^{-1}$),[15,16] K_b the Boltzmann constant, T the temperature (300 K), and e the electric charge. The measured capacitance at the flatband voltage (−2.5 V) is estimated to be 320 pF (Fig. 2(a)). Accordingly, the calculated intrinsic doping concentration was ~4.61×10^{17} cm^{-3}, in a close agreement with recently reported values.[15,16] Applying a positive DC bias to the gate of a p-type organic MIS capacitor causes majority carriers in the semiconductor to be repelled from the insulator interface. This is associated with a decrease in the capacitance as the depletion region expands (Fig. 2(a)). For a thin film, the

capacitance is at its minimum when the organic semiconductor is fully depleted (the equivalent of the inversion regime for a conventional Si/SiO_2 metal-oxide-semiconductor (MOS) device). Thus, the minimum capacitance is determined by the insulator and semiconductor capacitances in series. The minimum capacitance (C_{min}) corresponding to full depletion is then given by,[17]

$$C_{min} = A\frac{\epsilon_{Ins}}{d_{Ins} + \frac{\epsilon_{Ins}W_{Max}}{\epsilon_S}}. \quad (2)$$

The maximum depletion width, $W_{Max} = 26$ nm calculated from equation (2) is close to the estimated pentacene thickness.

The addition of SWCNTs as a floating gate to the control sample to form Al/SU8/CNTs/PMMA/pentacene/Au, resulted in clear hysteresis in the *C-V* curves (Fig. 2(b)). As it is difficult to obtain accurately the flatband voltage, we estimated the window as the shift between the forward and reverse scans at the point when capacitance is about 85% of the difference between accumulation and inversion capacitances. Forward sweeps below ±10 V exhibited curves similar to those of the control devices, with 255 pF accumulation capacitance and a very small negative shift in the flatband voltage to (−2.8 V). In contrast, a clear positive shift in flatband voltage to (−1.8 V) is evident for ±15 V voltage sweep as shown in Fig. 2(b). The difference in the accumulation capacitance to the control device was expected due to a change in the effective insulator stack thickness when SWCNTs are embedded.

The small negative shift in the flatband voltage (compared to the control device) after the forward sweep and for sweeping voltage below ±10 V indicates that a very few incorporated holes originating from the pentacene become trapped on the SWCNTs layer. The positive shift in flatband voltage for the voltage sweep from 15 V to −15 V is attributed to the breakdown in the SU8 dielectric strength, resulting in a leakage current and electrons transfer through the SU8 film to the floating gate. Typical values for SU8 dielectric strengths are 100-150 V/μm and thickness dependent. Hence, for a 90 nm thick SU8 layer, the breakdown voltage is very close to 13 V.[18] The reverse sweep showed a distinct change in the flatband voltage shifting to about 1.3 V for ±15 V sweeping voltage range. The hysteresis is attributed to the presence of SWCNTs as a floating gate and results from the charging and discharging of the SWCNTs when negative and positive voltages are consecutively applied. The shape of the hysteresis curves for low sweeping voltages, below the SU8 breakdown voltage (Fig. 2(b), specifically the short depletion regions) reflects high charge transport mobility for the semiconductor layer. This will lead to fast charging and discharging of the CNTs in the memory stack. As shown in the inset, Fig. 2(b), the hysteresis in the *C-V* curves increased with sweeping voltages in the measured range (from ±5 V to ±30 V). For sweeping voltages below the SU8 breakdown voltage, the memory window increases almost linearly with increasing sweep voltages and becomes negligible for voltages below ±5 V. However, at higher sweeping voltages (above ±15 V), the memory window rises slightly sharper and reaches 6 V at ±30 V due to the charge leakage induced by the soft breakdown in the SU8 dielectric strength. The fact that the centre of the hysteresis is very close to the 0 V, makes the memory structures produced favorable for lower operating voltages. Subsequent measurements indicated that the typical results (Fig. 2) are repeatable after several rounds re-testing. The devices also display a clockwise hysteresis, a positive flatband voltage shift in the *C-V* characteristics during the reverse voltage sweeps (Fig. 2(b)). These results are consistent with the behavior of a p-type semiconductor (pentacene in this device) MIS structure where electrons are injected into the SWCNT floating gates from the Al electrode through the SU8 organic insulator. This could be due to the high resistivity of PMMA (10^{13} Ω.cm at 10^6 V.cm^{-1} applied field) which prevents charges from tunneling from the pentacene through PMMA to the SWCNT floating gate.[17] We therefore believe that when a negative voltage (higher than the flatband voltage) is applied to the gate electrode, electrons are injected from the gate through the SU8 thin film into the floating gate resulting in charging the SWCNTs layer. Equally, a higher positive gate voltage must be applied to reach depletion in the pentacene. Accordingly, the *C-V* curve in Fig. 2(b) is shifted towards more positive voltage. The charges stored in the SWCNTs floating gate (Q) can be estimated from $Q = C_{FB} \times \Delta V_{FB}$, where ΔV_{FB} is the flatband voltage shift. This gives approximately 9.15×10^{11} cm^{-2} charges stored in the SWCNTs floating gate for ±30 V sweep voltage. Some preliminary tests on the reproducibility, stability, and repeatability of the memory structures have been undertaken. Devices fabricated on the same substrate showed a maximum variation in the accumulation capacitance of 10% and 5% variation in the flatband voltage. However, all devices stored under vacuum were tested regularly over a period of six months and produced repeatable memory behaviour with a variation in hysteresis of not more than 5%.

The retention behavior of the MIS-based memory structures were observed by monitoring the capacitance with time after charging the device for a few seconds and then applying a stress voltage (0 V in this study). Here, a two second −13 V pulse was applied to charge the memory device. Over 94% of the charges trapped in the SWCNTs remained confined in the floating gate over the measurement time of more

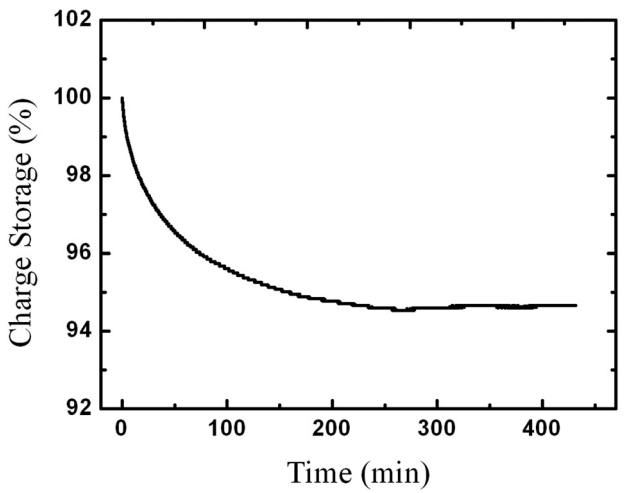

FIG. 3. Charge retention characteristics of Al/SU8/CNTs/PMMA/pentacene/Au memory devices.

than 6 h of continuous testing as shown in Fig. 3. The relatively small change in the capacitance after six hours of continuous testing indicates that the MIS memory structure has a very good retention capacity and there is a very little leakage current in the MIS structure.

In summary, we have demonstrated a pentacene and CNT-based floating gate memory device in the form of Al/SU8/CNTs/PMMA/pentacene/Au structure. Enhanced memory effects were achieved by carefully selecting and processing appropriate organic insulators to encapsulate the SWCNT charge storage elements. This resulted in memory effects at relatively low voltages and high charge retention of 94% after 6 h. The charge trapping effect is attributed to the charges injected from the gate through the SU8 to the SWCNTs, becoming significant as the breakdown voltage of SU8 is approached. The characteristics described in this investigation clearly demonstrate the potential for SWCNTs to be used as storage elements in advanced non-volatile organic memory devices in flexible electronics.

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