Subthreshold characteristics of pentacene field-effect transistors influenced by grain boundaries

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Grain boundaries in polycrystalline pentacene films significantly affect the electrical characteristics of pentacene field-effect transistors (FETs). Upon reversal of the gate voltage sweep direction, pentacene FETs exhibited hysteretic behaviours in the subthreshold region, which was more pronounced for the FET having smaller pentacene grains. No shift in the flat-band voltage of the metal-insulator-semiconductor capacitor elucidates that the observed hysteresis was mainly caused by the influence of localized trap states existing at pentacene grain boundaries. From the results of continuous on/off switching operation of the pentacene FETs, hole depletion during the off period is found to be limited by pentacene grain boundaries. It is suggested that the polycrystalline nature of a pentacene film plays an important role on the dynamic characteristics of pentacene FETs. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4721676]

I. INTRODUCTION

Organic semiconductors have emerged as viable materials for flexible electronic devices due to several clear advantages over conventional silicon-based materials such as large-area coverage, mechanical flexibility, and low-temperature processing capability.[1–3] Pentacene is one of the promising *p*-type organic semiconductors for field-effect transistors (FETs). Pentacene films prepared by thermal evaporation have a polycrystalline nature, and the grain size and grain boundary density strongly influence the charge transport in the films.[4,5] It is generally recognized that structural defects in pentacene films, such as grain boundaries, decrease the field-effect mobility of pentacene FETs by trapping charges.[6] This has thus expedited researches on increasing the pentacene grain size to enhance the field-effect mobility of the pentacene FET. On the other hand, in contradiction to those works, Knipp *et al.* reported that changing surface wetting of a gate dielectric more towards a hydrophobic surface by using octadecyltrichlorosilane leads to the growth of smaller grains but the mobility is improved by a factor of 2–3 for untreated dielectrics.[7] Yang *et al.* also presented a characteristic improvement for the pentacene FETs having smaller grains grown on a polymeric gate dielectric with lower surface energy.[8] Likewise, similar results have been reported for the case of the pentacene FETs with gate dielectrics treated with self-assembled monolayers (SAMs) using octyltrichlorosilane, octadecylphosphonate, π-σ-phosphonic acid, etc.[9–13] These works emphasized that the carrier mobility of pentacene FETs with hydrophobic SAM-treated gate dielectrics was always better than untreated FETs which exhibited larger dendritic pentacene grains. The controversy essentially lies on the growth kinetics of pentacene molecules into a film, such as molecular orientation/ordering as well as interconnection and packing density between grains.[14–19] Recent studies on this subject thus underline the significance of initial growth of pentacene molecules for the performance of pentacene FETs.[20,21] Nevertheless, a more comprehensive study of the effect of pentacene grain boundaries on the charge-depletion characteristics of the pentacene FET in the subthreshold region is still lacking. This is of prime importance to optimize a driving voltage and a switching frequency of integrated circuits based on these FETs.

In this study, we present a systematic study on the subthreshold characteristics of polycrystalline pentacene FETs. Two different deposition rates of pentacene molecules were used to vary grain size and grain boundary density in the pentacene film. Our experimental results for the current-voltage characteristics and the capacitance-voltage characteristics reveal that a hysteretic behaviour in the subthreshold region is more pronounced for the FET with smaller pentacene grains, demonstrating that the depletion of holes in the conducting channel can be limited by grain boundaries in the pentacene film. In Sec. II, we describe device fabrication, characterization of the film morphology, and measurements of the electrical properties of the pentacene devices. Experimental results are presented in Sec. III. In the remaining section, some concluding remarks are then made.

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II. EXPERIMENTAL DETAILS

Bottom-gate, top-contact FETs were fabricated using pentacene as the active material. For the bottom gate electrode, a 150-nm-thick Al layer was thermally deposited on a glass substrate through a first shadow mask. Then, a polystyrene (Sigma Aldrich, approximately 1 wt. % in chloroform) gate dielectric layer was spin-coated and baked at 100 °C for 1 h in a dry oven, followed by pre-curing at 80 °C for 10 min. The thickness of the polystyrene dielectric layer was about 220 nm, as measured by a surface profiler (Alpha Step IQ). After completing the curing processes, a 60-nm-thick pentacene layer (Tokyo Kasei Kogyo Co. Ltd., used without further purification) was thermally evaporated through a second shadow mask. Herein, two different deposition rates of 0.05 and 0.3 nm s^{-1} were used to produce the morphological changes in the pentacene films. Note that the grain growth of pentacene molecules is highly sensitive to deposition conditions such as deposition rate and substrate temperature.[22] Finally, 50-nm-thick Au source and drain electrodes were thermally deposited using a third mask. The channel length (L) and width (W) of our FETs were 90 and 400 μm, respectively. In order to examine the interfacial characteristics between the polystyrene dielectric layer and the pentacene film, a metal-insulator-semiconductor (MIS) capacitor was also fabricated using identical processes; the pentacene film was deposited at a rate of 0.05 nm s^{-1}. All evaporation processes were carried out under a base pressure of $\sim 1.6 \times 10^{-6}$ Torr.

The crystallinity of the pentacene film was studied by x-ray diffraction (XRD) (DMAX 2500, Rigaku) with monochromatic Cu Kα ($\lambda = 1.54$ Å). The surface morphologies of the fabricated films were observed with an atomic force microscope (AFM) (XE150, PSIA Inc.) in contact mode. The capacitance-voltage and current-voltage characteristics of the fabricated devices were measured with an impedance analyzer (HP 4192 A, Agilent Technologies) and semiconductor analyzer (EL 421 C, Elecs Co.), respectively.

III. RESULTS AND DISCUSSION

A. Structural and morphological characteristics of pentacene films

Figure 1(a) shows the XRD peaks for pentacene films deposited at the two different rates of 0.05 and 0.3 nm s^{-1}. All the diffraction peaks correspond to the (00*l*) Bragg peaks of pentacene, confirming the formation of well-ordered pentacene films. From the strongest diffraction peaks around 5.76° and 5.75°, both films exhibit a thin-film phase with an interplanar spacing of about 1.53 nm. However, AFM images in Figs. 1(b) and 1(c) show that the pentacene film deposited at a rate of 0.05 nm s^{-1} is composed of larger grains as compared to that deposited at a rate of 0.3 nm s^{-1}. This is because the nucleation density of pentacene molecules strongly depends on the deposition rate.[22] Faster deposition of pentacene molecules generally yields a larger number of nucleation sites, resulting in smaller pentacene grains in the film. Bae *et al.* reported that the structural packing density of pentacene grains within the framework of the initial layer-by-layer coverage is of prime importance for the charge transport in

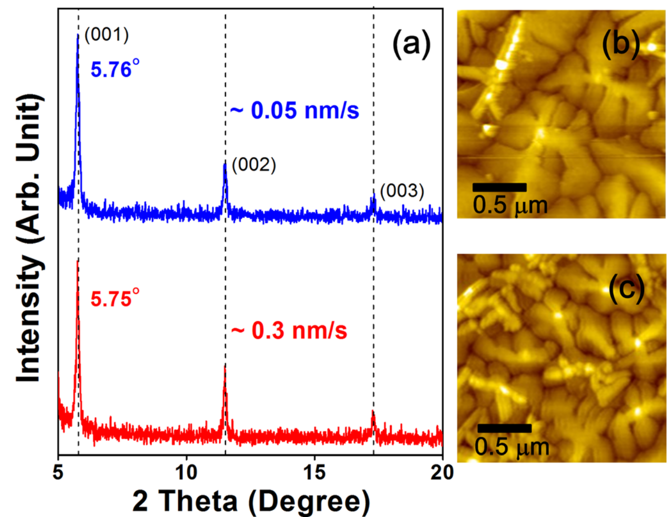

FIG. 1. (a) XRD spectra of pentacene films grown at different deposition rates. AFM images of pentacene films deposited at (b) 0.05 and (c) 0.3 nm s^{-1}.

the pentacene film; a better connectivity among adjacent pentacene grains, which is intimately produced by a higher packing density of the pentacene grains on a gate dielectric layer, contributes to enhancing the field-effect mobility in the pentacene FETs.[20] This explains that the presence of grain boundaries in the pentacene film inevitably limits the carrier mobility in the pentacene FETs. Different polymorphs of the pentacene films shown in Figs. 1(b) and 1(c) are thus expected to influence on the charge transport in the fabricated FETs. Based on the results, we could confirm that the two different deposition rates of pentacene molecules produced morphological changes, such as grain size and grain boundary density, in the fabricated pentacene films.

B. Capacitance-voltage characteristics of MIS capacitor

In order to understand the interfacial characteristics between the polystyrene dielectric layer and the pentacene film, the capacitance-voltage (*C-V*) characteristics of the pentacene-based MIS capacitor were analyzed by applying a small ac signal with an amplitude of 10 mV; the measurements were made at 1, 10, and 100 kHz, using the arrangement depicted in Fig. 2(a). Theoretically, the capacitance value in the depletion region corresponds to the series capacitance value of the polystyrene dielectric layer and the pentacene film, while the value for the accumulation region equals that of the polystyrene dielectric layer itself. In this case, holes vertically transport through the pentacene film under the influence of the applied voltage, as shown in Fig. 2(a), and thus the effect of pentacene grain boundaries can be neglected. From the *C-V* plots in Fig. 2(b), it is observed that the accumulation capacitance rather increases on increasing the applied frequency from 1 kHz to 100 kHz, whereas the depletion capacitance remains nearly constant. The frequency dependence of the accumulation capacitance observed by us is likely due to low carrier mobility in the pentacene film. However, there is no abrupt decrease (or increase) in the

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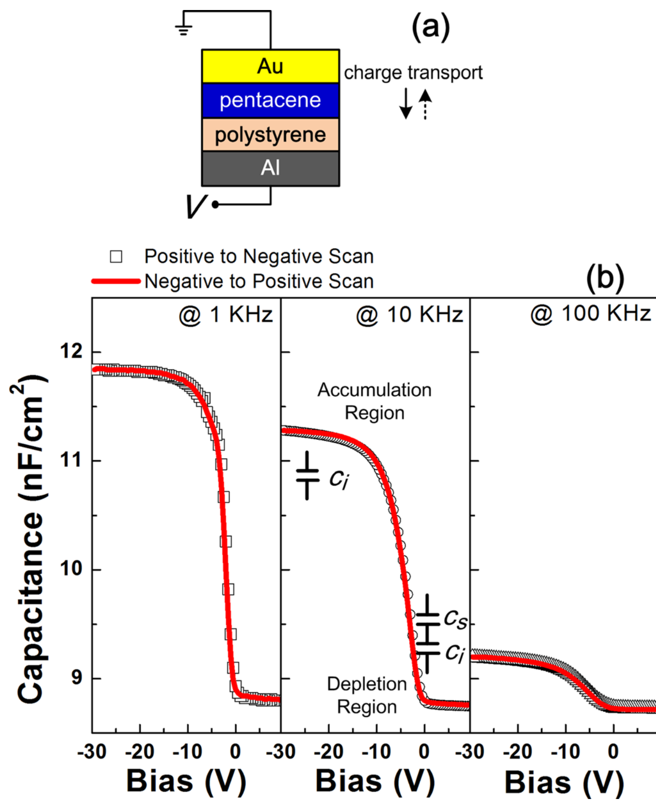

FIG. 2. (a) Schematic illustration of the capacitance measurement setup. (b) *C-V* curves for the fabricated MIS capacitor according to the voltage sweep direction at different frequencies. The insets represent equivalent circuits for accumulation and depletion regions in the *C-V* curve.

accumulation capacitance with increasing bias and frequency. Considering that the leakage conduction through a dielectric leads to an apparent change in the accumulation capacitance, the results suggest that the obtained capacitance was not influenced by leakage currents through the polystyrene dielectric layer. The apparent frequency dispersion and bias dependence of accumulation capacitance are also found in the literature.[23] Besides, recent works have systematically investigated the capacitive behaviours in pentacene films and organic devices as well.[24–26] Particularly, in our results, we would like to note that the fabricated MIS capacitor shows negligible hysteresis with no shift in the flat band voltage upon reversal of the voltage sweep direction; there was no critical hysteretic behaviour in the *C-V* characteristics even with varying the measurement frequency. This indicates that there were no fixed charges formed at the interface between the polystyrene dielectric and pentacene layers.[27] Hence, the electrical characteristics of the pentacene FETs will be examined in terms of the morphological changes in the pentacene films only.

C. Current-voltage characteristics of pentacene FETs

Figure 3(a) shows the drain current-drain voltage curves (I_D-V_D) of the fabricated FETs operating at a gate voltage (V_G) of −20 V. It is well known that larger pentacene grains are conducive to an increase in the electrical conduction properties in pentacene films because grain boundaries limit the charge transport in the films.[28] Larger pentacene grains deposited at a rate of 0.05 nm s^{-1} are thus responsible for higher I_D of the FET in our results. Meanwhile, the device fabricated with a pentacene deposition rate of 0.3 nm s^{-1} exhibited a gradual increase in the saturation current, which would correlate with smaller pentacene grains. Figures 3(b) and 3(c) show the transfer characteristics of the pentacene FETs operating at a V_D of −30 V. In both cases, hysteresis upon reversal of the V_G sweep direction is observed in the subthreshold region, which is more pronounced for the FET with smaller pentacene grains deposited at a rate of 0.3 nm s^{-1}. However, both FETs exhibit no significant difference in I_D for V_G exceeding the threshold voltage (V_T) as well as no discernible V_T shift upon the reversal sweep of V_G, as shown in the insets of Figs. 3(b) and 3(c). These results would suggest that the grain boundaries in the pentacene film play a dominant role on the subthreshold characteristics of pentacene FETs. Important device parameters are summarized in Table I; the insulator capacitance value obtained at 10 kHz was used for calculating the field-effect mobility. It is thought that lower field-effect mobility for the FET fabricated with the pentacene deposition rate of 0.3 nm s^{-1} originated from less connectivity between pentacene grains in the film.

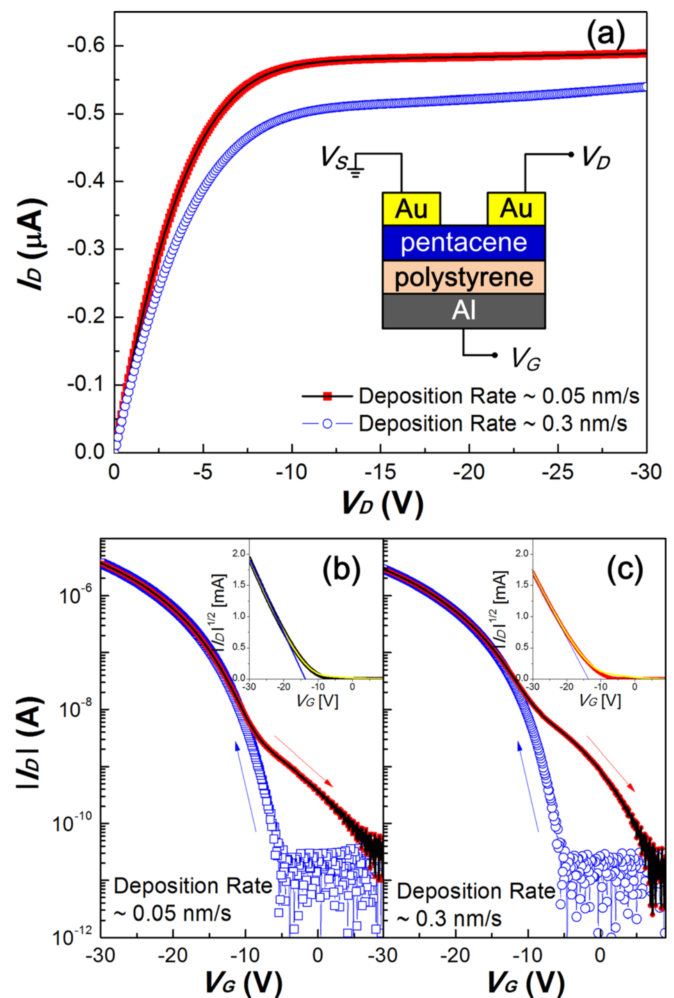

FIG. 3. (a) Output characteristics of FETs fabricated with two different deposition rates of pentacene molecules. The inset shows the schematic representation of the fabricated FET. Transfer characteristics of devices with pentacene deposition rate of (b) 0.05 and (c) 0.3 nm s^{-1}.

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TABLE I. Device parameters related the deposition rate of pentacene molecules.

Deposition rate (nm s^{-1})	Mobility (cm^2 V^{-1}s^{-1})	V_T (V)	Subthreshold swing (V decade^{-1})	I_{On}/I_{Off}
0.05	0.63	−13.8	1.6	$\sim 1.6 \times 10^5$
0.3	0.45	−13.6	1.8	$\sim 1.2 \times 10^5$

Herein, the Levinson technique is used to investigate the effect of pentacene grain boundaries on the electrical characteristics of the pentacene FET. Based on the approximated I_D equation in the linear regime,[29]

$$\ln\left(\frac{I_D}{V_G}\right) = \ln\left(\frac{W\mu_G V_D C_i}{L}\right) - \frac{q^3 N_t^2 t}{8\varepsilon_r\varepsilon_0 kTC_i}\left(\frac{1}{V_G}\right), \quad (1)$$

where μ_G, C_i, N_t, ε_r, and t are the charge mobility in the grain, the capacitance of the polystyrene dielectric layer, the density of trap per unit area, the relative permittivity of pentacene, and the thickness of the polycrystalline pentacene film, N_t can be estimated from the slope, s, of the Levinson plot [ln(I_D/V_G) vs. ($1/V_G$)] using the following formula,[30]

$$s = \frac{q^3 N_t^2 t}{8\varepsilon_r\varepsilon_0 kTC_i}. \quad (2)$$

Figure 4(a) displays that the slope for the FET where the pentacene film was deposited at a rate of 0.3 nm s^{-1} is steeper than that for the device fabricated with the pentacene deposition rate of 0.05 nm s^{-1}. Taking the operating temperature T as 300 K and the ε_r of pentacene as 4,[31] $N_t \sim 8.1$ $(\pm 0.2) \times 10^{17}$ and 3.7 $(\pm 0.4) \times 10^{17}$ cm^{-2} are estimated for the pentacene FETs fabricated with the deposition rate of 0.3 and 0.05 nm s^{-1}, respectively; the slopes were taken from the best linear fits. Meanwhile, in contrast to the prediction that the Levinson plot should result in a straight line, the plots of our FETs were not straight. This may indicate that the grain boundaries are traps rather than barriers. Furthermore, it is often observed that such nonlinearity in the Levinson plot for pentacene FETs gets more pronounced with increasing V_D in the linear regime.[32] Hence, the prominent nonlinear decay for the FET having larger pentacene grains is likely due to a larger number of charge carriers conducting in the FET as exemplified by higher I_D in Fig. 3(a); as more charges conduct in the pentacene FET, more charges are prone to be trapped at grain boundaries. The results clearly substantiate the fact that the grain boundary trap density decreases as the grain size of pentacene increases. Such traps at grain boundaries are thought to be related with the connectivity between pentacene grains as discussed in the Subsection III A. Therefore, the hysteretic features in the subthreshold region shown in Figs. 3(a) and 3(b) can be explained on aspects of the hole depletion behaviour in the presence of localized states in the polycrystalline pentacene film. Such localized states are expected to be filled by increasing V_G since field-induced charges are more accumulated in the conducting channel with increasing V_G. Figure 4(b) shows the time-dependent degradation of I_D in the saturation region, obtained by applying V_G of −20 V and V_D of −30 V. As can be predicted from higher grain boundary traps, the initial decay for the FET with smaller pentacene grains (i.e., deposition rate of 0.3 nm s^{-1}) is much faster in comparison with the case of larger pentacene grains (i.e., deposition rate of 0.05 nm s^{-1}). One more important point is that there are sporadic increases in I_D for the FET with smaller pentacene grains, which are marked with filled circles in Fig. 4(b). This result can be interpreted with the multiple trapping and release model for charge transport in the polycrystalline pentacene film.[33] We consider that energetic traps, i.e., localized states, at the grain boundaries in the pentacene film limit the charge transport rather than producing immobile charges. Accordingly, it is required to investigate the dynamic characteristics of pentacene FETs under continuous on/off switching conditions.

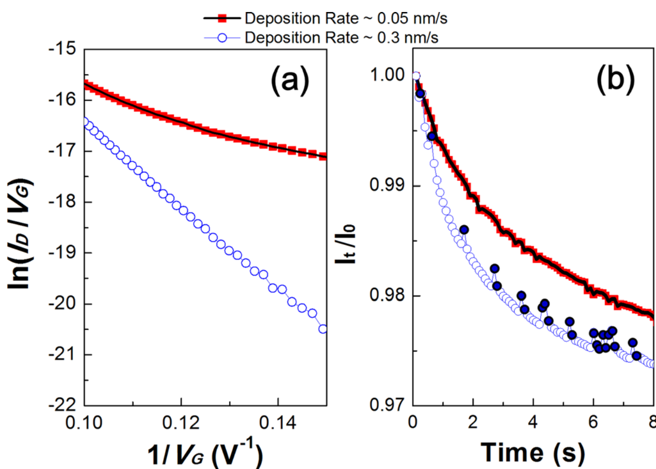

FIG. 4. (a) Levinson plots and (b) time-dependent I_D decay curves of the two different pentacene FETs.

D. Dynamic characteristics of pentacene FETs

We now examine the dynamic characteristics of the two pentacene FETs in relation to the influence of pentacene grain boundaries. As shown in Fig. 5(a), the pulse of V_G with the amplitudes of −20 V and 0 V was applied to switch the FET on and off, respectively, while a constant V_D of −30 V was continuously applied. The pulse period time (T_{total}) was defined as the sum of the pulse-on and pulse-off times (t_{on}, t_{off}), and the pulse duty ratio was defined as t_{off} per T_{total}.[34] Figure 5(b) shows the dynamic response of each FET at the pulse duty ratio of 1/2 ($t_{off} = 10$ s, $T_{total} = 20$ s). During the off period, both devices were not fully switched off and the off-state I_D increased under continuous on/off switching conditions. These results elucidate the slow depletion of holes in the subthreshold region, which is intimately associated with grain boundary traps in the pentacene film. Our explanation is also supported by the higher off-state I_D for the device with smaller pentacene grains. Figure 5(c) shows the dynamic characteristics of the two pentacene FETs when the pulse duty ratio is 2/3 ($t_{off} = 20$ s, $T_{total} = 30$ s). Although the depletion behaviors of holes during the off period are still slow, there are no significant increases of the off-state I_D for

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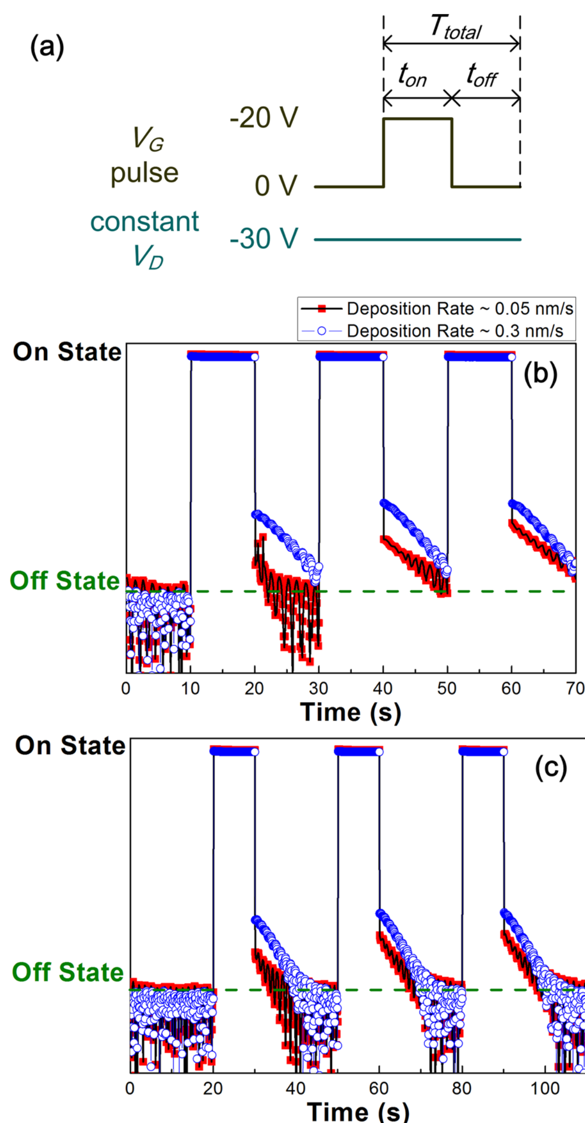

FIG. 5. (a) Driving schemes of V_G and V_D. Variations of I_D under dynamic on/off switching of FETs with pulse duty ratio of (b) 1/2 and (c) 2/3.

both devices. In fact, the off-state I_D values are almost comparable to its initial value even under consecutive pulse operations. It should be recognized that it took about 10 s for the full depletion of holes in the two FETs irrespective of the pentacene grain size and grain boundaries in this study. Two possible mechanisms may be responsible for the results; the non-uniform distribution of active traps in the conducting channel and the remnant polarization of the polystyrene dielectric layer itself. However, the former seems to be plausible for our results because the dielectric constant of polystyrene is as low as 2.65. Note that the effects of remnant polarization are generally observed for polymeric insulators with high dielectric constants.[35] On the other hand, as the internal electric field in the conducting channel decreases from the source electrode toward the drain electrode, most trap states localized around the source electrode can be preferentially filled with holes. It is considered that effective traps affecting the subthreshold characteristics as well as the dynamic properties of polycrystalline pentacene FETs would be more dominantly distributed near the drain electrode. This may be indicative of similar hole-depletion times observed in Fig. 5(c), which were less influenced by grain size and boundary in the pentacene film. Further quantitative analysis on the distribution of effective traps in the conducting channel will provide a more comprehensive understanding of the device physics.

IV. CONCLUSION

We described the influence of pentacene grain boundaries on the subthreshold characteristics of polycrystalline pentacene FETs. Two different deposition rates of pentacene molecules produced the change of pentacene grain size and grain boundary density. The fabricated FETs exhibited hysteretic behaviour in the subthreshold region, which was more pronounced for the device having smaller pentacene grains. Herein, the observed hysteresis is explained on aspects of the depletion behaviour of conducting holes in the presence of grain boundaries in the pentacene film. The fact that an extended off-state period contributed to more stable operation of the pentacene FET during consecutive pulse operations suggests that the polycrystalline nature of a pentacene film plays an important role on the dynamic characteristics of pentacene FETs. These results can be extended to determine the optimum driving scheme for organic FET-based circuits and analyze the device physics in relation to the morphological characteristics of an organic semiconductor layer.

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[1]B. Crone, A. Dodabalapur, Y. Y. Lin, R. W. Filas, Z. Bao, A. LaDuca, R. Sarpeshkar, H. E. Katz, and W. Li, Nature (London) **403**, 521 (2000).
[2]T. Yamao, H. Akagami, Y. Nishimoto, S. Hotta, and Y. Yoshida, J. Nanosci. Nanotechnol. **9**, 6271 (2009).
[3]J.-H. Kwon, S.-I. Shin, J. Choi, M.-H. Chung, T.-Y. Oh, K.-H. Kim, D. H. Choi, and B.-K. Ju, J. Nanosci. Nanotechnol. **10**, 3198 (2010).
[4]Y. Y. Lin, D. J. Gundlach, S. F. Nelson, and T. N. Jackson, IEEE Electron Device Lett. **18**, 606 (1997).
[5]J. H. Park, C. H. Kang, Y. J. Kim, Y. S. Lee, and J. S. Choi, Mater. Sci. Eng., C **24**, 27 (2004).
[6]A. Bolognesi, M. Berliocchi, M. Manenti, A. D. Carlo, P. Lugli, K. Lmimouni, and C. Dufour, IEEE Trans. Electron Devices **51**, 1997 (2004).
[7]D. Knipp, R. A. Street, A. Völkel, and J. Ho, J. Appl. Phys. **93**, 347 (2003).
[8]S. Y. Yang, K. Shin, and C. E. Park, Adv. Funct. Mater. **15**, 1806 (2005).
[9]O. Marinov, M. J. Deen, and B. Iñiguez, J. Vac. Sci. Technol. B **24**, 1728 (2006).
[10]J. E. McDermott, M. McDowell, I. G. Hill, J. Hwang, A. Kahn, S. L. Bernasek, and J. Schwartz, J. Phys. Chem. A **111**, 12333 (2007).
[11]H. Ma, O. Acton, G. Ting, J. W. Ka, H.-L. Yip, N. Tucker, R. Schofield, and A. K.-Y. Jen, Appl. Phys. Lett. **92**, 113303 (2008).
[12]M. F. Calhoun, J. Sanchez, D. Olaya, M. E. Gershenson, and V. Podzorov, Nature Mater. **7**, 84 (2008).
[13]T. Umeda, D. Kumaki, and S. Tokito, J. Appl. Phys. **105**, 024516 (2009).

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[14]I. Kymissis, C. D. Dimitrakopoulos, and S. Purushothaman, IEEE Trans. Electron Devices **48**, 1060 (2001).
[15]C. D. Dimitrakopoulos and P. R. L. Malenfant, Adv. Mater. **14**, 99 (2002).
[16]Y. Y. Lin, D. J. Gundlach, S. F. Nelson, and T. N. Jackson, IEEE Trans. Electron Devices **44**, 1325 (1997).
[17]M. Shtein, J. Mapel, J. B. Benziger, and S. R. Forrest, Appl. Phys. Lett. **81**, 268 (2002).
[18]D. H. Kim, D. Y. Lee, H. S. Lee, W. H. Lee, Y. H. Kim, J. I. Han, and K. Cho, Adv. Mater. **19**, 678 (2007).
[19]A. Virkar, S. Mannsfeld, J. H. oh, M. F. Toney, Y. H. Tan, G.-Y. Liu, C. Scott, R. Miller, and Z. Bao, Adv. Funct. Mater. **19**, 1962 (2009).
[20]J.-H. Bae, W.-H. Kim, H. Kim, C. Lee, and S.-D. Lee, J. Appl. Phys. **102**, 063508 (2007).
[21]J. Park, J. H. Bae, W. H. Kim, S. D. Lee, J. S. Gwag, and D. W. Kim, Solid-State Electron. **54**, 1650 (2009).
[22]F. J. Meyer zu Heringdorf, M. C. Reuter, and R. M. Tromp, Nature (London) **412**, 517 (2001).
[23]D. P. Norton, Solid-State Electron. **47**, 801 (2003).
[24]J. W. P. Wu, Mater. Today **8**, 32 (2005).
[25]C. H. Kim, O. Yaghmazadeh, D. Tondelier, Y. B. Jeong, Y. Bonnassieux, and G. Horowitz, J. Appl. Phys. **109**, 083710 (2011).
[26]A. Sleiman, M. C. Rosamond, M. A. Martin, A. Ayesh, A. A. Ghaferi, A. J. Gallant, M. F. Marbrook, and D. A. Zeze, Appl. Phys. Lett. **100**, 023302 (2012).
[27]J. Park, B. J. Park, H. J. Choi, Y. Kim, and J. S. Choi, IEEE Electron Device Lett. **30**, 1146 (2009).
[28]A. D. Carlo, F. Piacenza, A. Bolognesi, B. Stadlober, and H. Maresch, Appl. Phys. Lett. **86**, 263501 (2005).
[29]S. H. Jin, K. D. Jung, H. Shin, B.-G. Park, and J. D. Lee, Synth. Met. **156**, 196 (2006).
[30]Y.-W. Wang, H.-L. Cheng, Y.-K. Wang, T.-H. Hu, J.-C. Ho, C.-C. Lee, T.-F. Lei, and C.-F. Yeh, Thin Solid Films **467**, 215 (2004).
[31]T. Li, J. W. Balk, P. P. Ruden, I. H. Campbell, and D. J. Smith, J. Appl. Phys. **91**, 4312 (2002).
[32]D. Guo, T. Miyadera, S. Ikeda, T. Shimada, and K. Saiki, J. Appl. Phys. **102**, 023706 (2007).
[33]C. D. Dimitrakopoulos, I. Kymissis, S. Purushothaman, D. A. Neumayer, P. R. Duncombe, and R. B. Laibowitz, Adv. Mater. **11**, 1372 (1999).
[34]T. Miyadera, T. Minari, S. D. Wang, and K. Tsukagoshi, Appl. Phys. Lett. **93**, 213302 (2008).
[35]W.-H. Kim, J.-H. Bae, M.-H. Kim, C.-M. Keum, J. Park, and S.-D. Lee, J. Appl. Phys. **109**, 024508 (2011).

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