Nanofabrication using nanotranslated stencil masks and lift off

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Nanofabrication using nanotranslated stencil masks and lift off

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We propose and demonstrate a technique for forming nanometer-scale metal features based on evaporation onto a substrate through a stencil mask. In this work, the stencil mask is laterally translated by a piezoflexure stage, between evaporations of different metals. The metals are chosen based on their etch chemistry to allow one material to be lifted off with respect to another. In this way, sidewall features are formed with dimensions and spacings controlled by moving the translational stage, which has 1 nm resolution. © *2004 American Vacuum Society.*
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I. INTRODUCTION

Simple fabrication approaches are desired for sub-50 nm feature formation. In particular, it would be useful to construct wires with nanometer dimensions spaced relative to one another with nanometer precision. In this article, we describe a sidewall process in which the feature sizes are set by the piezoelectric translation of a stencil mask and the features are revealed by a bimetal lift-off process. Since commercial piezoelectric positioning stages now achieve nanometer resolution, the minimum feature size of this technique approaches a few nanometers. Nanofabrication using stencil masks has been previously reported,[1,2] but not in combination with sidewall processing.

The nanomechanical device which has motivated this work is shown schematically in Fig. 1. This switch[3] consists of two nanometer-scale metal lines of different thicknesses and an overlying metal cantilever. The gap between the cantilever source electrode and the supply-connected drain electrode, d_C, is made shorter than the gap between the source and gate-connected electrode, d_G. When a bias is applied between gate and source, the source cantilever is attracted to the gate. Because of the thicker metallization of the drain electrode, the source forms a tunneling contact with the drain while maintaining a significant distance from the gate, as shown by Fig. 1(b), thereby creating a nanometer-scale switch. Like a field-effect transistor, this device should exhibit both current and voltage gain. Such a switch, at the dimensions shown in Fig. 1, could switch at several gigahertz with a 1.5 V signal swing.[3]

II. METHODOLOGY

The approach for achieving nanometer scale lines and spaces is outlined in Fig. 2 as would be used to create the gate and drain electrodes of the nanomechanical switch of Fig. 1. A sequence of evaporations is shown, Figs. 2(a)–2(d), performed in a single pump-down cycle of a conventional electron-beam evaporator. Shown in Fig. 2(a) is the side view of a fixed shadow mask mounted over a substrate on which the nanostructure is to be formed. In this example, SiO_2 represents a grown oxide on a silicon wafer. Following each evaporation [Figs. 2(b)–2(d)], the substrate is translated laterally with respect to the shadow mask leaving a set of nanometer, interembedded, in this case metal, features. Note that the shadow mask opening does not determine the size of the feature; the feature size is controlled by the translation of the shadow mask. Materials for evaporation are chosen based on their etch chemistry. The principle is that one metal can be lifted off with respect to the other by selective etching. In this example, aluminum is the lift-off structure for platinum; the Al is removed by etching in $HCl:H_2O$ without attacking the underlying oxide or etching the platinum, leaving a pair of nanometer-scale lines with a controlled difference in height and precise separation, as shown in Fig. 2(d). In this article, we demonstrate the steps shown in Figs. 2(a) and 2(b), and the metal lift-off technique.

Sidewall processing using this technique requires steep side walls. The edge sharpness of the side walls, i.e., the edges of the deposited patterns, is mainly governed by the evaporation geometry as illustrated in Fig. 3. An analysis shows the width of the edge taper, *w*, of a deposited feature through a stencil mask is approximated by

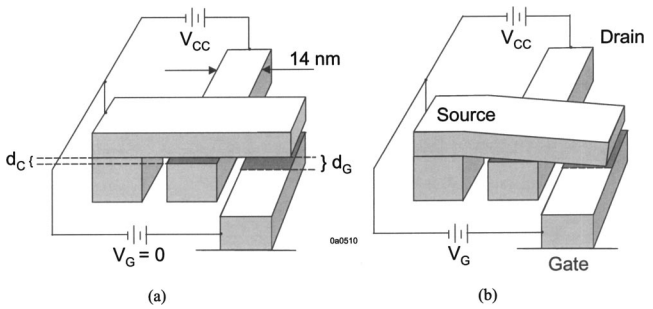

FIG. 1. Vertical nanoelectromechanical switch: (a) Natural open position, and (b) closed position under positive gate bias. As a representative scale, the contact length is chosen to be 14 nm with d_C and d_G of 2 and 4 nm, respectively.

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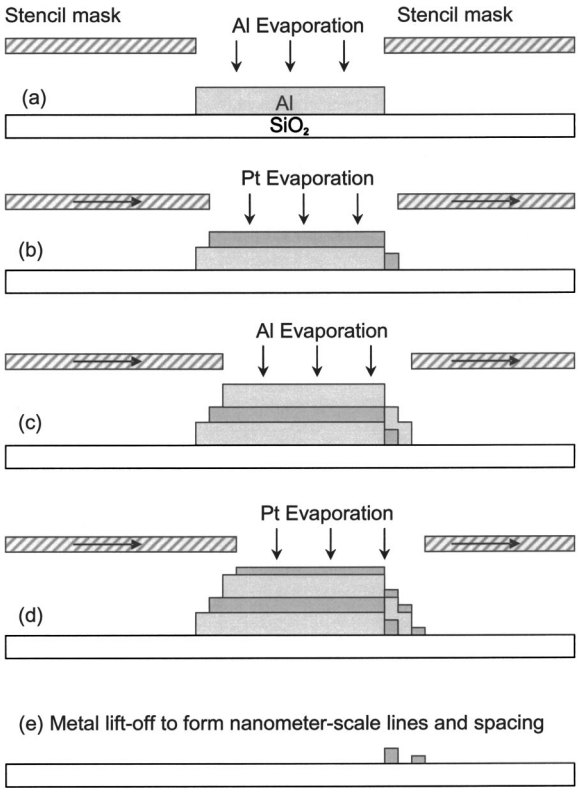

FIG. 2. Formation of nanometer metal wires with nanometer spacings by translating a stencil mask and lift off: (a) Aluminum is evaporated through a stencil mask, (b) the mask is translated by nanometers and platinum is evaporated, in (c) and (d) the process is repeated, followed by (e) where lift off is used to reveal nanometer-scale lines with nanometer spacings. Thickness differences between the two lines are feasible since they are set by the deposition conditions.

$$w \cong \frac{h+t}{H} d, \tag{1}$$

where h is the substrate-to-mask spacing, t is the thickness of the mask, H is the mask-to-evaporation-source distance, and d is the diameter of the molten evaporation source. In order to get sharp side walls, we desire thin masks, large source-to-substrate throw, and a small or collimated evaporation source.

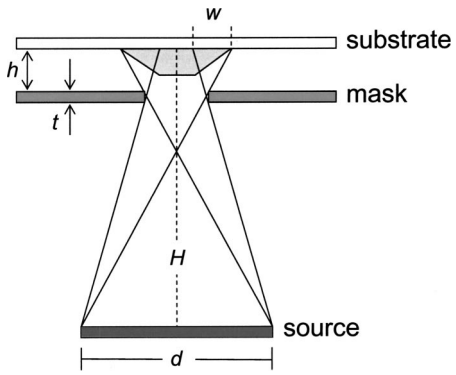

FIG. 3. Factors influencing the sharpness of sidewall features.

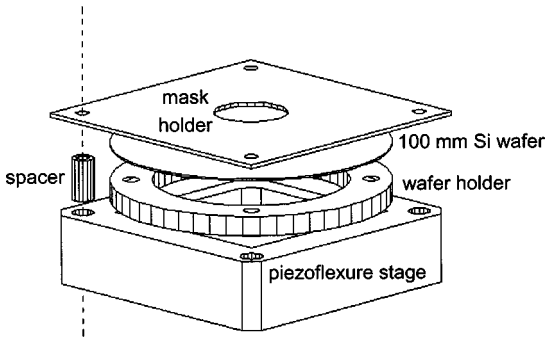

FIG. 4. Fixture assembly for nanotranslated stencil mask and substrate. Parts from top to bottom include: Stencil mask holder, 100 mm Si wafer, wafer holder, spacer, and $x-y$ flexure nanotranslation stage.

III. EXPERIMENT

In this work, the deposition of metals was performed in a commercial Airco/Temescal (Berkeley, CA) FC-1800 electron-beam evaporation system which has a source-to-substrate throw of 50 cm. We used ultrathin masks ($t \leqslant 1\ \mu$m) in contact mode to decrease the term $h+t$ in Eq. (1). In addition, we designed an aperture of 3 mm diameter to reduce the size of the evaporation source. With such a configuration, the expected edge taper, w, is 6 nm, which is tolerable when the resulting lift-off features are tens of nanometers. We note that with a better system configuration, for example, a larger evaporator with longer source-to-substrate distance and better collimation, the feature edge taper width can be reduced to $\sim$1 nm which means that wires on the order of a few nanometers in width are feasible.

The translation of the shadow mask is achieved using a commercial Polytec-PI (Auburn, MA) P-731 flexure $x-y$ nanopositioner with built-in capacitive sensors which operate under closed-loop feedback control. A mask–substrate fixture has been designed constructed, as shown in Fig. 4. A 100 mm wafer was fixed to the wafer holder that is mounted on the flexure portion of the Polytec-PI $x-y$ stage, the mask holder is attached to the fixed portion of the $x-y$ stage via three spacers (one is shown). Through the circular aperture in

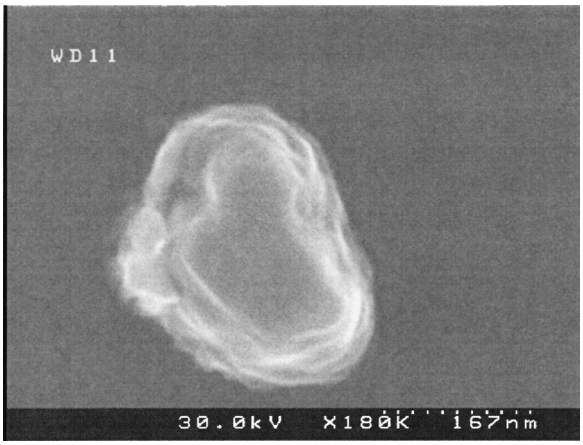

FIG. 5. SEM of an Al nanodot produced by depositing through a polyimide membrane mask.

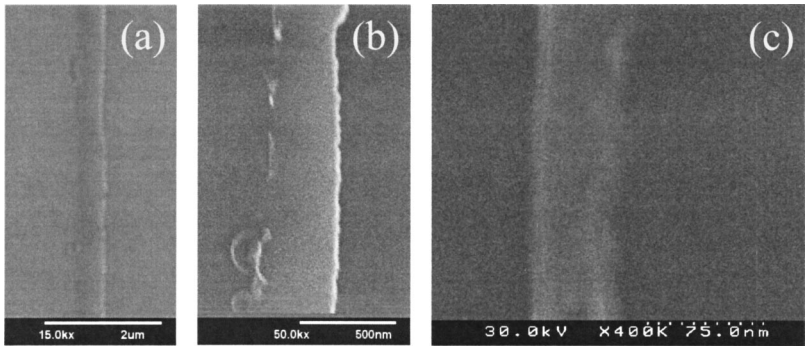

FIG. 6. Wires fabricated by a combination of nanotranslated stencil masks and metal lift-off processing: (a) 330 nm Ti/Pt wire, (b) enlarged portion of (a), and (c) 45 nm Ti/Pt wire.

the center of the mask holder, a stencil mask mounted on an aluminum ring is placed to establish close contact and flatness between the substrate and the mask. Finally, the mask is fixed to the mask holder by silver paste.

Experiments have been carried out using two types of ultrathin masks, a KOH-etched Si rigid mask and a polyimide membrane mask. Rigid masks were fabricated using 10 mil thick double-side-polished silicon wafers with patterned Si_3N_4 and KOH etching. Due to the directional selectivity of Si etching by KOH, a slope of 54.74° is formed, (111) plane, along the openings of the mask. Polyimide membrane masks, with a thickness of approximately 1 μm, were formed by reactive ion etching. These masks are stiff enough to be used in contact mode and the sub-0.5 μm apertures allowed us to observe the effect of hole clogging in stencil masks. With these membrane masks, it is also possible to directly ''write'' nanofeatures onto the substrate by translating the substrate during evaporation of metals.

IV. RESULTS AND DISCUSSION

The clogging of mask openings by evaporated materials is a common concern when the featuring size is on the nanometer scale.[2] This phenomenon introduces a sidewall slope in the deposited metal which can be compensated for with the translation of the mask relative to the substrate during deposition. We studied this effect by evaporation of metals through nanosized, patterned polyimide membrane masks. Figure 5 shows a scanning electron micrograph (SEM) of a nanodot produced by depositing 300 nm of aluminum onto SiO_2 through a polyimide membrane mask. It can be seen from Fig. 5 that an edge taper results. Based on our experimental geometry for this evaporation, the expected edge taper is about 20 nm. An edge taper of ~55 nm is observed from Fig. 5. The extra 35 nm of taper is introduced by the clogging of the mask opening. The thickness of the evaporated aluminum is 300 nm, the clogging growth rate is about 1/9th of the deposition rate.

Figure 6 shows metal wires formed by the sidewall metal lift-off process of Fig. 2. After the deposition of a 300 nm Al layer, the substrate was translated and a bilayer of 5 nm of Ti and 45 nm of Pt were deposited. The Ti layer served as an adhesion promoter to the SiO_2. Shown in Fig. 6 are two sizes of lines produced after lift off, 320 and 45 nm. It can be seen in Fig. 6(a) that over the extension of several microns, the wire exhibits a good uniformity with an average width of 330 nm and no observable discontinuities. In fact, we found this kind of uniformity over millimeter lengths. Figure 6(b) shows an enlarged portion of the same wire showing some edge roughness. The 45 nm wire shown in Fig. 6(c) shows greater irregularities along the lift-off edge structure with approximately 20 nm of roughness. Since the left-hand side, which is not influenced by the lift-off process, is still straight and smooth, this irregularity can only be attributed to the lift-off process. This may be caused by a tearing off of the top layer Pt during the lift-off process. It may also be introduced by some incomplete material removal as we have observed in regions where the etching is not allowed to complete.

V. CONCLUSIONS

We have outlined a technique to create nanometer scale structures with nanometer spacings with resolution of both wires and spaces set by piezoelectric translation. A sidewall bimetal lift-off process achieved feature sizes as small as 45 nm. Geometrical considerations, namely, source-to-substrate distance, mask-to-substrate distance, mask thickness, and source size, are found to be decisive parameters determining the ultimate smallness. Compensation schemes, such as translational correction, will need to be introduced to address mask clogging and achieve the minimum feature sizes of this technique.

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