The Geometry of Catastrophic Fracture during High Temperature Processing of Silicon

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Abstract

The geometry of fracture associated with the propagation of cracks originating at the edges of (001) oriented, 200mm diameter silicon wafers has been investigated under two regimes of high temperature processing. Under spike annealing, fracture did not occur on low index planes and all except one wafer exhibited crack patterns that started initially to run radially, but after a distance of typically 20 to 30 mm, turned and ran almost tangentially. Wafers subjected to plateau annealing, with a 60 second dwell time at high temperature, predominantly fractured through radial cracks running along <110> directions. X-ray diffraction imaging reveals substantial slip in all wafers subjected to plateau annealing. We demonstrate using finite element (FE) modelling that the change in fracture geometry is associated with this plastic deformation, which changes the stress distribution during the cooling phase of the rapid thermal annealing cycle. FE simulations without plastic relaxation show that the radial component of the thermal stress distribution is compressive in the centre of the wafer, causing the crack to run tangentially. Simulations incorporating temperature dependent plasticity showed that the equivalent stress becomes tensile when the plateau anneal allows time for significant plastic relaxation, permitting the crack to continue propagating linearly.

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One Sentence Summary:

We explain the two different modes of silicon wafer fracture during high temperature processing in terms of plastic relaxation of thermal stresses during plateau annealing.

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1. Introduction

Wafer breakage during high temperature processing is a multi-million dollar problem in semiconductor manufacturing lines, the prime cost being in loss of product during the time taken to stop the line, recover the broken wafer, clean and restart the affected tool. Although Chen *et al.* (2009, 2010) found a statistical correlation between wafer failure during processing and the geometry of the edge bevel shape, the prime origin of these failures appears to be cracks at the wafer edge associated with misaligned handling tools. Rather than rely on statistical approaches (Cook, 2006; Brun and Melkote 2009), we have developed an X-ray diffraction imaging (XRDI) technique for assessing the probability that individual cracks will propagate (Tanner *et al.,* 2012). This methodology underpins commercial XRDI products now on the market.

The fracture mode has been a matter of question as it has been noted that (001) oriented wafers sometimes fracture quasi-circumferentially and sometimes parallel to low index <110> directions. When failure occurs by the former mode during high temperature processing, the disruption can be substantial due to small fragments falling and subsequently shattering, resulting in difficulty in cleaning the affected tool. In this paper, we show that the two different fracture modes are related to plastic relaxation occurring, or not occurring, during the dwell time at high temperature.

2. Experimental Method

We have studied the different modes of wafer breakage from edge cracks artificially introduced into 200 mm diameter, (001) oriented, silicon wafers by 50N Vickers indentations

located at 90, 180 and 270° with respect to the orientation notch and placed between 20 and 120μm from the bevel edge. Indentations were performed with a Mitutoyo AVK-C2 Hardness Tester (Garagorri *et al*. 2010). For loads below 50 N and indents located typically 1mm from the bevel edge, four-fold crack patterns resembling those described by Cook (2006) were observed. However, when the symmetry was broken by the proximity of the wafer edge break-out occurred predominantly on the wafer edge side of the indent, relaxing the strain and leaving one or more long cracks lying in the direction of the wafer centre. Provided that the crack length exceeded about 2mm length and the indent was positioned within 70 μm of the bevel edge catastrophic fracture could occur in our rapid thermal annealing (RTA) system. The cracks were found to be good models of cracks introduced by damage associated with misaligned robotic handling tools.

The Si wafers used were dislocation-free silicon wafers purchased from Y Mart Inc, Palm Beach Gardens, Florida, USA. All wafers were within 0.2° of (100) orientation. The nominally defect-free, double side polished, p-type wafers had resistivity below 10 ohm mm, and were of thickness 725 (±25) μm. No edge defects were visible either under optical inspection or in XRDI images of the as-received wafers, which had been packed and shipped in standard cassettes.

All RTA experiments were conducted in a JetFirst 200C system, purchased from Qualiflow Therm-Jipelec. Details of the temperature-time profile during the annealing sequence, which was almost independent of the maximum temperature, can be found in Wittge *et al.* (2010). Two annealing schemes were used. In both cases, the heating time to 1000 °C was 10 seconds and cooling achieved under forced gas convection. In the spike annealing procedure, cooling

began immediately on reaching 1000 °C, while the plateau annealing involved holding the temperature at 1000 °C for 60 seconds prior to cooling.

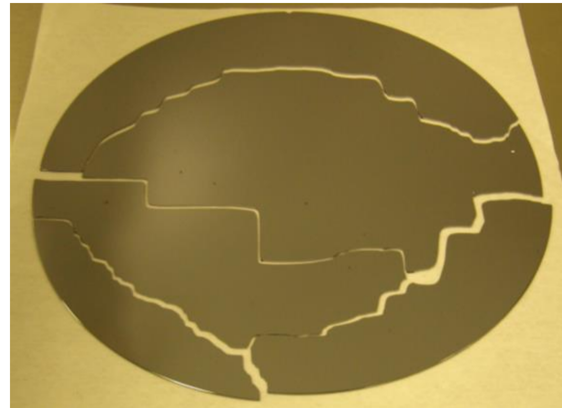
X-ray Diffraction Imaging was performed with the BedeScan™ tool (Bowen *et al.* 2003) at Jordan Valley Semiconductors (UK). MoKα (wavelength 0.0708nm) radiation was used in the (Laue case) transmission geometry. The tool was operated in survey mode with a CCD detector of pixel size 23.5 µm and the adjacent three pixels were binned, giving an effective resolution of 70.5 µm. The step size between each successive section topograph in the scan was six times the pixel size (141 µm), giving a reasonable compromise between resolution and scan time. Under these conditions a complete scan of a 200 mm wafer took about 90 minutes.

3. Results

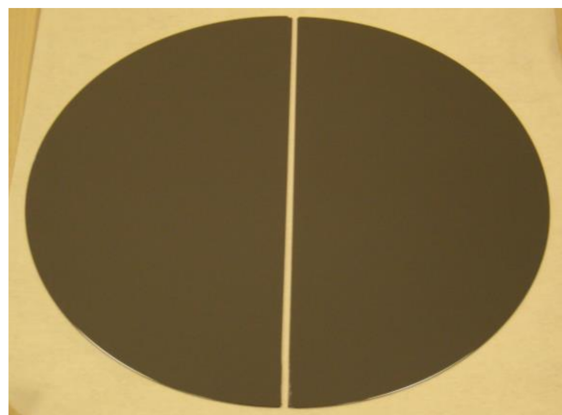
We have found that the fracture geometry during rapid thermal annealing (RTA) varied dramatically between wafers that had been subjected to spike annealing (Fig 1(a)), where cooling began immediately on reaching the peak temperature, compared with those that had experienced plateau annealing (Fig 1(b)), where wafers were held at the maximum temperature for 60 seconds. Spike annealed wafers exhibited crack patterns that started initially to run radially, but after a distance of typically 20 to 30 mm, turned and ran almost tangentially. Fracture did not occur on low index planes and was very irregular in direction (Fig 1(a)).

On the other hand, those wafers subjected to plateau annealing fractured along <110> directions (Fig 1(b)), corresponding to average cleavage on {111} planes, which have the

lowest surface energy of the low index planes [3]. There was a high degree of consistency in this attribution over all the wafers examined (Table 1).



(a)



(b)

Fig 1. 200 mm diameter silicon wafers that fractured during RTA. (a) Spike annealed at 800°C, (b) plateau annealed at 1000°C

Table 1

Temperature (°C)	Plateau Anneal	Spike Anneal
600	T[a],R	T,T,R[b]
800	R,R,R,R,R,R,R	T,T,T,T,T,T,T,T,T
1000	T[c],R[b],R,R,R,R	T,T,T

R = crack runs radially in a <110> direction
T = crack runs almost tangentially

a. Fractured during plateau
b. Fractured during heating
c. No obvious anomaly

Table 1 Crack type for wafers subjected to RTA

In all our RTA experiments, three thermocouples were placed on the rear surface of the wafer and when wafer fracture occurred, there was an abrupt and characteristic change in the temperature recorded, due to the disconnect between the wafer and the thermocouple (Fig 2). A perturbation in at least two of the thermocouple readings at the same time (the perturbation of one could mean just failure of the thermocouple), typically a sudden temperature drop, was enough to detect the instant of breakage. We observed that, in the great majority of cases and where the wafer was properly located in the RTA tool, fracture did not occur during the heating of the wafer, but during the forced cooling process.

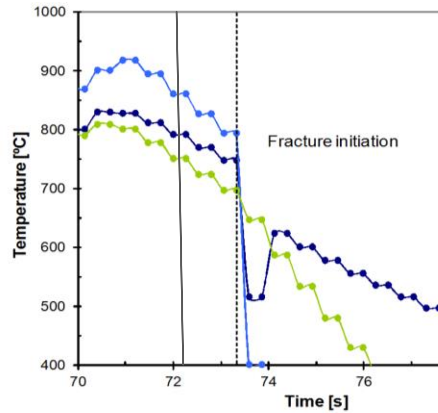


Fig 2. Characteristic changes in the three thermocouple readings at the point of wafer fracture.

Yoo *et al.* (2002) observed an elastic deformation of wafers during temperature ramp up. The wafer shape began to deform as the temperature increased to a maximal deformation at a temperature of 800°C. By the time a temperature of approx. 950°C had been reached, the wafer then became flat again, indicating that different stresses are introduced in the wafer during the RTA processing. Recently, Calvez *et al.* (2014) have used finite element (FE) modelling to predict critical propagation paths of cracks, initiated at the wafer edge, through silicon power devices subjected to accelerated thermal cycling tests. We have used finite element modelling of the elastic stresses within the wafer under realistic thermal conditions in the RTA furnace (Tanner *et al*. 2012, Garagorri *et al.* 2012) to identify the elastic stresses to which the initial cracks are subjected. Finite element modelling of the time-resolved thermal distribution in the RTA furnace was performed using the commercial software ABAQUS® version 6.10-EF1. The finite element model included a stainless steel processing chamber where the wafer is heated, and a very thin quartz window which separates the process chamber and the reactor from the heating source. A total of 118859 elements have been necessary, where 5332 are associated with the axisymmetric mesh describing the

substrate wafer. During heating, we observed that the tangential stresses at the wafer edge were always compressive, keeping the crack closed. On cooling, the tangential stress switched sign, opening the crack, enabling it to propagate radially. However, the stress in the centre of the wafer remained compressive and beyond about 20 mm, the crack would not propagate further in this direction. At this point it is energetically favourable for the crack to turn into a tangential direction as the radial stress remains tensile. This tensile stress opens the tangential crack, which propagates in an almost circumferential direction (Tanner *et al.* 2012). Figure 3 shows the boundary between the tensile and the compressive regimes in the FE simulations superimposed on the image of a broken wafer. The paths of the major circumferential cracks follow this boundary.

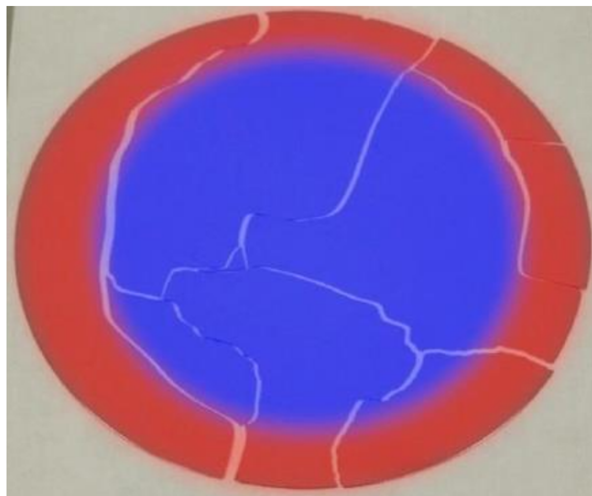


Fig 3. Overlay of the simulated boundary between tensile (red) and compressive (blue) radial stress and an image of a fractured wafer.

As evident in Table 1, all spike annealed wafers, except one low temperature anneal where the wafer unusually broke during the heating sequence, exhibited this circumferential cracking. However, despite excellent agreement between the predicted and observed fracture patterns in spike annealed wafers, no way could be found in which this purely elastic FE model of the wafer stresses could be adjusted to predict the existence of long straight cracks

running along the <110> directions in plateau annealed wafers. We argue that the explanation of the two crack families lies in the presence of the substantial slip that occurs during plateau annealing providing relaxation of the compressive strains in the wafer centre.

X-ray diffraction imaging of spike annealed wafers has shown that slip is initiated at the wafer bevel but that it does not propagate more than about 1 mm into the wafer (Tanner *et al.* 2011) and is not usually evident in large area, low resolution X-ray diffraction images. However, XRDI of wafers subjected to plateau annealing, where the wafer is held for a 60 seconds at a temperature above the brittle to plastic transition, always revealed lengthy slip bands Wittge *et al.* 2010, Garagorri *et al.* 2012) and usually showed slip steps visible optically on the surface. The slip band length followed an Arhenius exponential variation with maximum annealing temperature T [10] and varied linearly with dwell time (Fig 4), consistent with a constant dislocation velocity $\upsilon(\tau,T)$ under the imposed stress field τ of the form

$$\upsilon(\tau,T) = A\left(\frac{\tau}{\tau_0}\right)^{m(T)} \exp\left(-\frac{E}{k_B T}\right) \qquad \text{Eq. 1}$$

and where E is the activation energy (measured to be 2.1±0.2 eV), A and τ_0 are constants and m is close to unity and a function of T.

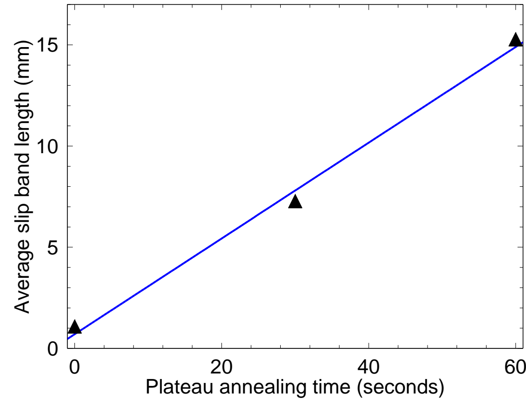


Fig 4. Average slip band length, taken from pairs of points at equal angles around the wafer perimeter, as a function of plateau annealing time at 1000°C.

An example of the slip bands in such a wafer that fractured radially is given in Fig 5. The image was taken in transmission mode with a BedeScan™ tool (Bowen *et al*. 2003). Fracture was initiated at a 50N Vickers indent at the top left of the wafer and propagated entirely in the $[1\bar{1}0]$ direction.

Inclusion of the effect of plastic relaxation was achieved by incorporating temperature dependent plasticity. The stress-strain curves were calculated from dislocation dynamics simulations using the open source *Micromegas* code. This software is a development of the work of Devincre *et al.* (2001). Dislocations are allowed to glide on all the 12 slip systems of {111} planes along <110> directions. Cross slip is not included in the simulations but as there is good correlation between slip band width and length in the diffraction images, the overall effect on the macroscopic strains will not be affected by this omission.

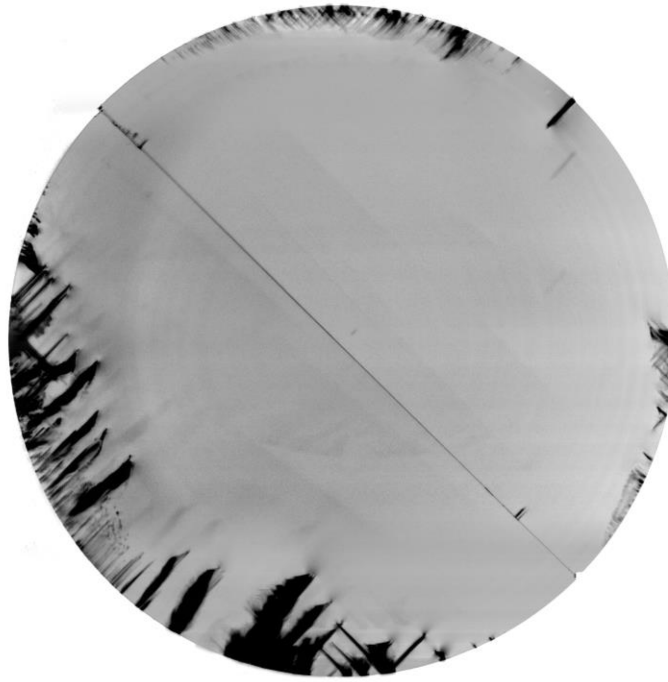


Fig 5. Linear fracture in the radial direction of a 200 mm diameter wafer subjected to a 1000°C plateau anneal. 400 reflection, MoKα radiation. The BedeScan™ image is formed from a single scan of the two broken halves of the wafer.

Finite element modelling of the stresses with inclusion of plastic deformation revealed a very different stress distribution as a function of annealing time. During the heating sequence the stresses were in the same sense as that predicted by the purely elastic model in that the tangential stress at the wafer edge was compressive, keeping the crack closed. As creep is not included in the FE model, the plastic relaxation will here be fully developed prior to cooling. On cooling, as for the purely elastic simulation, the tangential stress at the edge switched sign (Fig.6(c)), opening the crack. However, in contrast to the purely elastic simulation, with inclusion of plastic relaxation, the radial stress near the edge of the wafer did not switch from compressive to tensile (Fig.6(a)). As the tensile radial stress responsible for the change in crack orientation is no longer present, the crack continues to propagate. Because the {111} planes have the lowest surface energy (Tanaka *et al.* 2006), cleavage on these planes occurs

preferentially and the brittle crack opens on this plane, resulting in a single, linear, fracture of the wafer which projects into the <110> direction in the plane of the wafer (Figs 1(b) and 5). As cooling continues, the radial strain begins to change to tensile (Gorostegui-Colinas 2012) but not uniformly (Fig.6(b)). The asymmetry of the resulting stress distribution is due to the crystallographic symmetry of the available slip systems being superimposed on the asymmetry associated with the heating elements in the furnace, resulting in a quite complex variation in the resolved shear stress as a function of angle around the wafer (Garagorri *et al.* 2012). At this stage, the tangential stress at the wafer edge is also predicted to switch back to being compressive (Fig 6(d)) but by this time, the wafer will have fractured.

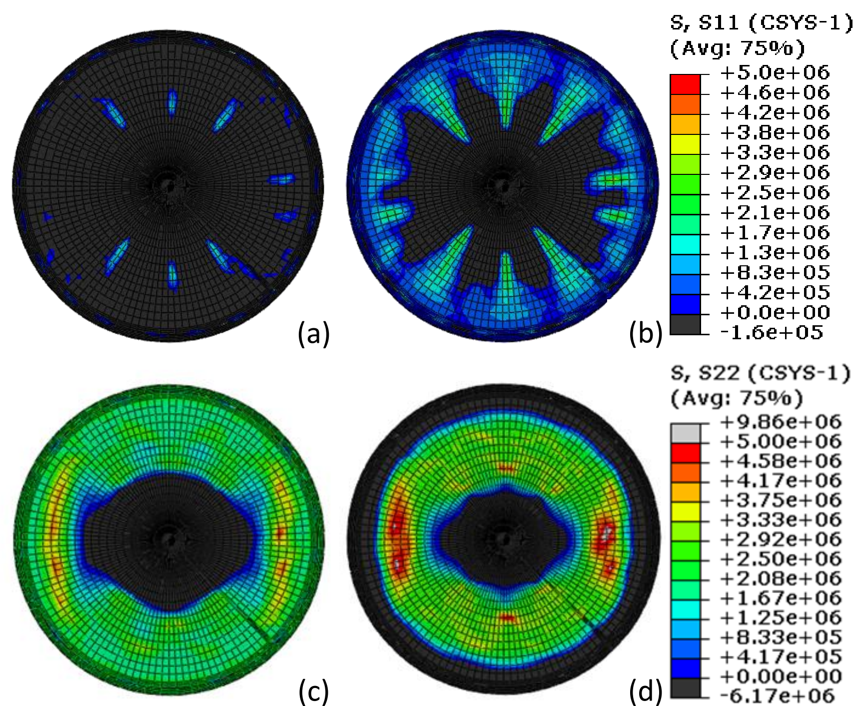


Fig. 6. Evolution of radial [s_{11}] (a and b) and tangential hoop [s_{22}] (c and d) stresses during an anneal at 800ºC. (a) and (c) correspond to 2s into cooling while (b) and (d) correspond to a time of 30s after the start of cooling. Temperature dependent plasticity is used in the simulations. Units: Pa

The maximum stresses shown in Fig. 6 are of the order of 5 to 10 MPa and are determined by the thermal gradients in the RTA furnace used for the experiments. While these stresses are seemingly low, there is a large stress concentrator effect associated with the cracks we have introduced (and also for the cracks observed arising from handling tool damage, Tanner *et al.* (2012)). Brede (1993) reported the fracture toughness K_{Ic} of silicon to be 0.92 $MPa.m^{-0.5}$ at room temperature and in the ductile regime above 800°C as between 2.76 and 7.36 $MPa.m^{-0.5}$. For the case of a plate with an edge crack of length a under tensile loading, the critical stress σ_f is given by

$$\sigma_f = \frac{K_{Ic}}{1.12\sqrt{\pi a}} . \qquad \text{Eq. 2}$$

As exemplified in Tanner *et al.* (2012), the length of the critical cracks in our experiments was typically 10 mm and thus we find σ_f = 4.6MPa at room temperature and between 13.9 and 37MPa in the ductile regime above 800°C. These values are of the order of magnitude found in the finite element simulations and we note that our experimental stress configuration is different to the case of a simple plate under tensile loading.

Samuels and Roberts (1989) studied the fracture of silicon initiated from indents under four point bending. They observed that below a critical temperature T_c, failure was by brittle fracture while above T_c the failure was by ductile plastic yielding. They demonstrated that T_c is a function of lattice hardness (doping level) and strain rate, their measured activation energy of 2.1±0.1eV being in excellent agreement with our value, quoted above. While we do have evidence of plastic deformation during the plateau annealing, we have no evidence of ductile plastic yielding and none of the fractures show associated slip bands. The only examples of slip band nucleation at crack tips during plateau annealing are in wafers that did

not fracture and the cracks did not propagate. Brittle fracture normally occurs during wafer cooling and we note that the FE simulations show that the temperature at the wafer edge is always lower than that at the centre. The thermocouples, which are located away from the wafer edge, will always give a reading higher than that at the edge. The evidence suggests that fracture from the edge crack predominantly occurs in the brittle regime but that during the plateau, the macroscopic plastic deformation relaxes the stress. We note that, when plastic relaxation does not occur, and the crack propagation is almost tangential, the crack path is not smooth and at a microscopic level the brittle crack path probably changes rapidly between low energy planes.

4. Conclusions

The very different fracture geometries in damaged silicon wafers following high temperature annealing under spike and plateau conditions are attributed to the presence of plastic relaxation during the plateau dwell time. This attribution of plastic deformation relaxing the stresses and resulting in linear cracking along the low index direction during plateau annealing, during which the wafer is held at a high temperature for 60 seconds, is consistent with the averaged dislocation velocity of 0.24 (±0.02) mm s^{-1} presented in Fig. 4. In practice, a significant time is needed for the slip to occur and relax the thermal stresses. The lack of plastic relaxation in the spike anneal process arises from the fact that the wafer is not held for sufficiently long in the plastic regime above the brittle-ductile transition for the dislocations to travel far during that time.

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