Density and Energy Distribution of Interface-states in the Grain-boundaries of Poly-Silicon Nanowire

Iddo Amit[†], *Danny Englander*[†], *Dror Horvitz*, *Yaniv Sasson and Yossi Rosenwaks*[*]

Department of Physical Electronics, School of Electrical Engineering, Tel-Aviv University,

Ramat-Aviv 69978, Israel.

KEYWORDS: Nanowire, Top-down, Grain boundary, Polycrystalline silicon, Kelvin probe microscopy, Charge trapping.

ABSTRACT: Wafer-scale fabrication of semiconductor nanowire devices is readily facilitated by lithography based top-down fabrication of poly-silicon nanowire (P-SiNW) arrays. However, free carrier trapping at the grain boundaries of polycrystalline materials drastically changes their properties. We present here transport measurements of P-SiNW array devices coupled with Kelvin probe force microscopy at different applied biases. By fitting the measured P-SiNW surface potential using electrostatic simulations, we extract the longitudinal dopant distribution along the nanowires, as well as the density of grain boundaries interface states and their energy distribution within the band-gap.

Wafer-scale fabrication of semiconductor nanowire arrays is important in the efficient realization of transistors and biological and chemical sensors[1-8]. Nanowire arrays can increase the device performance, mainly with regards to signal to noise ratio[9-11], while exploiting the benefits of the robust CMOS fabrication technology. The natural choice for a reliable, low-cost mass production of functioning wires is lithography based top-down fabrication of poly-silicon nanowire (P-SiNW) arrays. Recently, P-SiNW transistors with different gate architectures, such as omega gate[12] and gate-all-around[13] were demonstrated. The top-down fabrication approach[14], supported by advanced lithography techniques[15] was used to fabricate novel memory transistors[16], and logic devices[17]. However, a key issue in polycrystalline devices that distinguishes them from single crystalline semiconductors is the properties and characteristics of the crystallites grain boundaries (GBs). Therefore, a design of a polycrystalline device requires information of both the density and the energy-distribution of interface states at the GBs[18,19].

In his seminal work from 1975, Seto noted that trapping of free carriers at the GB interface states (GBIS) affects the material conductivity by changing two basic properties of the semiconductor. First, the trapping of free carriers induce depletion regions at the vicinity of the GB. Since the width of the depletion region is a function of both the interface states density and the doping level, heavily doped P-Si will be nearly unaffected by free carriers trapping, as the trapped charge will be screened. On the other hand in lightly doped P-Si, the depletion region can extend throughout the whole grain, resulting in a fully depleted semiconductor. Second, the charge accumulation at the GB produces a potential barrier for free carriers transport across the boundary, decreasing the charge carrier mobility[18]. The increasing interest in P-Si in the early 1980s resulted in some new data regarding both the GBIS density and energy distribution[20-21]. For bulk P-Si, the GBIS distribution was experimentally determined to have a 'U-shape' across the

energy gap, with different peak values ranging from 4×10^{13} to 10^{14} $cm^{-2}eV^{-1}$. However, to the best of our knowledge, such measurements were not reported for nanoscale devices in general and for nanowires in particular.

We present here measurements of dopant distribution and density of GBIS in P-SiNW arrays. A wafer-scale fabrication process using the top-down approach enabled us to produce various P-SiNW arrays of 2, 20 and 50 wires of different lengths ranging from 0.5 to 41 μm. The wires are characterized by transport measurements, coupled with Kelvin probe force microscopy and electrostatic simulations. This enabled us to extract the longitudinal doping profile of the nanowire[22], as well as the density of GBIS and their energy distribution within the band-gap.

P-SiNW arrays were fabricated utilizing the sidewall P-Si spacer formation technique[23-25]. The NWs, as well as the source and drain pads were fabricated by the following three lithography steps: (1) formation of the insulating SiO_2 spacers and the source and drain pad regions. This step was followed by P-Si deposition over the entire wafer. (2) Formation of P-SiNWs on each side of the spacer by dry etching the excess P-Si, and (3) symmetrical doping of the source and drain pads as well as some of the P-SiNW itself using ion implantation. Steps (1) and (2) of the lithography procedure are shown schematically in Fig. 1 a (*i-iv*). Following the lithography, the wafers were annealed at 1050°C for 4 s to promote dopant activation and recover the P-Si grain size of 20 nm. The fabrication process produced a matrix of NW arrays, varying both in number of NWs per array and in NW's length. More details of the fabrication process are described in the supporting information.

The KPFM measurements were carried out using a Dimension Edge AFM system (*Bruker AXS*) and a conductive Pt/Ir-coated tip in a controlled nitrogen environment glove-box (less than 5 ppm H_2O). Measurements were performed in the "dual frequency mode", where the topography

is measured at the first mechanical resonance of the tip in the "tapping mode", and the contact potential difference (CPD) is measured by electrically exciting the tip at its second resonance frequency. To facilitate the KPFM measurements, the P-SiNW arrays were electrically contacted by a fourth lithographic step, and a deposition of 220 nm aluminum contacts, which form Ohmic contact to the source and drain pads.

A schematic representation and an SEM micrograph of the final P-SiNWs structures are shown in Fig. 1 b. and c., respectively. The top-down formed NWs are resting against both sides of the SiO_2 spacers, and have a quarter-of-a-circle cross section. Morphological characterization of the P-SiNWs was performed using TEM cross sections which showed a nearly uniform radius of curvature in all measured devices (Fig. 1 d.). We estimate the mean size of P-Si grains from the TEM micrographs to be around 20 nm with approximately spherical shape.

Fig. 2 a. shows a KPFM image of a single P-SiNW, grounded at both sides. The device shown is a 9 µm long wire, with a 5 µm long intrinsic region, and two 2 µm long n^+ regions, one at each end. For convenience, we have termed the regions (from left to right) 'source', 'channel' and 'drain', as shown in Fig. 2 a. The KPFM measures the contact potential difference (CPD) which is basically the difference in work functions between an AFM tip (Φ_t) and the sample (Φ_s), so that $CPD = -(\Phi_t - \Phi_s)/q$, where q is the elementary charge[26]. Accordingly, the figure shows five distinct regions in the wire, longitudinally symmetric about its center: at the sides of the P-SiNW, the wire and the highly doped pads overlap as seen from the wide doped regions surrounding the NW; the slightly less doped source and drain are observed connecting the pads to the intrinsic channel which is at the middle of the wire. The work function contrast, between these connecting segments and the channel clearly show the difference in charge carrier concentration between the different parts. Several CPD line scans, measured along the middle

part of the wire and at different drain biases, are presented in Fig. 2 b (solid lines). The applied bias on the drain electrode was varied from $+2V$ to $-2V$ in $0.5V$ steps, while the source was grounded. The channel of the P-SiNW is easily identified as the region where most of the potential drop occurs. The junctions built-in voltage, V_{bi}, measured when both electrodes were grounded, is around $0.23V$ indicating a difference of roughly four orders of magnitude in charge carrier concentration between the n^+ and i segments. At a negative bias (the upper part in Fig. 2 b.), the source-channel junction is under reverse bias, and the potential drop is larger on this junction. The 'current limiting' potential barrier is observed on the opposite (drain-channel) junction. When applying a positive bias (lower part in Fig. 2 b.) the left drain-channel junction becomes reversely biased, and the potential barrier is seen at the other side.

The CPD measured for both n^+-i interfaces deviates from the expected profiles for an abrupt junction. First, in these junctions, the V_{bi} should be around half of the band gap energy, whereas the measured value corresponds to a significantly lower doping difference across the junction. Second, the CPD profile at the doped regions exhibit a small slope, which can be attributed to a non-uniform axial doping in those regions, most probably due to diffusion taking place during the high temperature fabrication. The formation of an n^+-i-n^+ structure by ion implantation involves a photolithography step where the NW's channel was protected from the ion flux by a photoresist. Secondary ion mass spectroscopy (SIMS) measurements performed on blank wafers that underwent the same implantation and anneal process resulted in an exponentially decaying doping profile with N_D=$5\times10^{19}cm^{-3}$ at the surface; this corresponds to a decrease of one order of magnitude within the first $10nm$. Following the implantation process, a thermal annealing (RTA) step was required to promote grain size recovery and activation of dopants. During this process, P atoms diffused through the n^+-i junction thus partially depleting the source and drain segments

from their impurity atoms, and unintentionally doping the channel. This process changed the interface profile to that of an n^+-n junction.

In order to extract the doping profile and GB interface states characteristics from the CPD measurements of the n^+-i-n^+ structures, the surface potential was calculated using the Sentaurus TCAD Device Simulator (*Synopsys Inc*.). The NW was modeled by a quarter-of-a-cylinder shaped SiNW, resting against two SiO_2 spacers as shown schematically in the inset of Fig. 2 b. The cylinder radius is 50 nm and is 9.4 μm in length, which are divided to five segments as follows: two 200 nm long highly doped "contact" regions on both ends of the wire, representing the symmetric source and drain pads with constant n^+ doping concentration of 5×10^{19} cm^{-3} (not seen in Fig. 2). The contact pads doping concentration is based on SIMS measurements performed on ion implanted blank wafers (see supporting information for the SIMS measurements details). Next to the contacts pads, there are two 2 μm long n^+ segments, corresponding to the source and the drain, with a surface doping value of $N_D(n^+)$ just at the interface with the channel (intrinsic). Even though the n^+ regions were doped with the same dose as the one used for the contact pads, the doping density is reduced due to diffusion of dopants to the intrinsic segment during the RTA drive-in process as was previously discussed. As a result, the n^+ segments have both axial and radial non-uniform doping profiles, which were incorporated into the model by the following relation: $N_D(x,r) = 1.3\times N_D(n^+) \cdot \exp(-x/0.78\mu\text{m}) \cdot \exp(r/21.7\text{nm})$, where x is the NW's axial coordinate, and r is its radial coordinate, with $r = 0$ at the center of the NW. The exponential decay constants were extracted from the SIMS and KPFM measurements, for radial and axial values, respectively. We note here that diffusion profiles should be described by an error-function; however, the error-function model could not be used in the Sentaurus simulator, and the exponential decay was found to be a good approximation. The channel

segment in the NW is a 5 μm long region with an axially uniform doping profile. The base doping value in this segment is $N_D(n^-)$ on the surface, and the radial doping gradient of the intrinsic segment is similar to that in the n^+ segment.

In order to account for charge carrier trapping at the GBs, we have used a mean-distribution approach where we assumed that the GB interface traps are spread evenly across the volume of the nanowire. For this purpose, we considered the grains in the NW to be a lattice of 20 nm spheres in a cubic close-packed (CCP) formation. Based on this geometry we derived an interface-to-bulk ratio which allows us to convert the surface density of interface states in the GB, into volume density of traps within the NW bulk, according to:

$$\rho_{BT} = \frac{\sigma_{GBIS} \cdot S}{V} = \frac{\sigma_{GBIS} \cdot 4^2 \pi r^2}{\left(\frac{4r}{\sqrt{2}}\right)^3} = \sigma_{GBIS} \frac{\pi}{r\sqrt{2}} \qquad (1)$$

Where ρ_{BT} is the mean-distributed volume density of bulk trap states, σ_{GBIS} is the surface density of GBIS, r is the sphere radius, S is the cumulative surface area of the spheres in an FCC "unit cell" and V is the unit cell volume. Using the interface-states surface density values reported in [18,20,21], one can estimate ρ_{BT} to be in the order of 10^{18} cm^{-3}. To confirm the validity of the mean-distribution approach, we have reproduced the well-known doping – free carriers density relation which is shown in Fig. 1 of Ref. 18 (see Fig 3 (a)). For this purpose, the average charge carrier density was calculated as a function of nominal doping using our mean-distribution approach, taking into account a single trapping energy at 0.37eV below the conduction-band minimum. The results of this calculation are presented in Fig. 3 (a), where the black solid line is the original data from Ref. 18, and the blue dots are the results of the electrostatic model. We note that Seto's results were published for boron doping, and his model includes a single trapping energy at 0.37eV above the valance band maximum. However, since the Fermi-Dirac distribution function is symmetrical for holes and electrons around the Fermi energy, we can use an equivalent trap energy for electrons and achieve the same result.

Our proposed model includes a U-shape distribution of charge traps across the band-gap (Fig. 3 (b)). This approach shows an identical trend to both measured and theoretical reports in the literature in the high doping regime; however, our model shows a significantly higher free-carriers depletion in the lower doping regime. We explain this difference as follows: First, our model is three dimensional assuming spherical grains whereas the Seto model is one-dimensional. Second, while Seto assumed a single trapping energy within the band gap, our model assumes a U-shaped distribution of traps, in accordance with Refs. 20,21, which becomes prominent in the lower doping regime.

The dashed lines in Fig. 2 b. were calculated using the above model to match the measured CPD (solid lines). The figure shows a good agreement between the simulated and measured surface potential up to the source-channel interface (around 5 μm in Fig. 2 b). The results around the source and its corresponding pad could not be fitted and we attribute these discrepancies to the diffusion controlled doping profile of the NW. The axial doping inhomogeneities in the wire intrinsic part were neglected in these simulations. These inhomogeneities, which stem from rapid diffusion of doping atoms along the NW axis, are probably the source of the band bending seen at the source region, in Fig. 2 b. The results of the optimized model yielded $N_D(n^+)=10^{18}$ cm^{-3} and $N_D(n^-)=3\times10^{17}$ cm^{-3}, accounting for both the measured built-in potential, and the shape of the voltage drop across the wire. The acceptor and donor type interface states density and distribution that were best fitted to the measured CPD (Fig. 2b) are:

$$DOS_A = \rho_{BT} e^{-\left|\frac{E-E_C}{\sigma_0}\right|} \qquad (2a)$$

$$DOS_D = \rho_{BT} e^{-\left|\frac{E-E_V}{\sigma_0}\right|} \qquad (2b)$$

Where the interface density was found to be $\rho_{BT} = 6.7\times10^{18}$ cm^{-3}eV^{-1}, and σ_0 = 0.15 eV is the decay coefficient that defines the width of states distribution within the band gap as described in Fig. 4 a. These GB interface states density are in good agreement with previously published values for Si-Si interface states, as our optimized ρ_{BT} corresponds, using our model, to a σ_{GBIS} = 3×10^{12} cm^{-2}eV^{-1}.

The dopants and charge carrier concentration distribution calculated using the model are presented in Fig. 4 b. The slightly-graded step between the n^+ segment and intrinsic part is a result of the model approximations; as mentioned above, the axial dopant distribution of the intrinsic segment was assumed constant, while in practice there is an axial gradient due to the diffusion during the RTA process. As our model shows, there is only a minor difference between the doping densities on the n^+ and i sides of the junction. The contrast between the source / drain segments and the channel stem from the non-uniform bulk traps density: on the highly doped source / drain, most of the traps are populated, and therefore, the region present a high density of charge carriers, whereas in the channel, the bulk traps density is larger than the doping level, and thus, the region is fully depleted.

In summary, we have measured and analyzed the doping distribution and interface states energy distribution in top-down fabricated P-SiNW. The nanowire arrays were produced using a low-cost fabrication process and were found to be uniform in shape and grain size distribution. By fitting the CPD measurements, we extracted both the surface density of GBIS and their energy distribution within the band gap. The results show that while the doping levels on the nanowire show a gradual decrease along the NW axis, the trapping of free carriers at the GBIS produces a "threshold" level of doping, below which the silicon becomes fully depleted. It is therefore crucial to take this effect into consideration when designing a P-Si based device. Our

mean-distribution approach for grain boundary simulations introduced a simplified method to incorporate the complex geometry of poly-crystalline material in a TCAD simulation. While this approach is in a remarkable agreement with respect to the electrostatic effects reported in the literature, it cannot be used to simulate transport, as the dynamics of the charge carriers is largely dependent on the periodicity and geometry of the potential barriers formed by the charged grain boundaries.

The presented analysis yielded crucial information required for the design of sensing and electronic devices based on poly-crystalline nanowires. This is due to the fact that in poly-crystalline materials, the device electronic performance is governed not only by the dopant concentration, but also by the distribution and density of grain-boundary interface states.

FIGURES

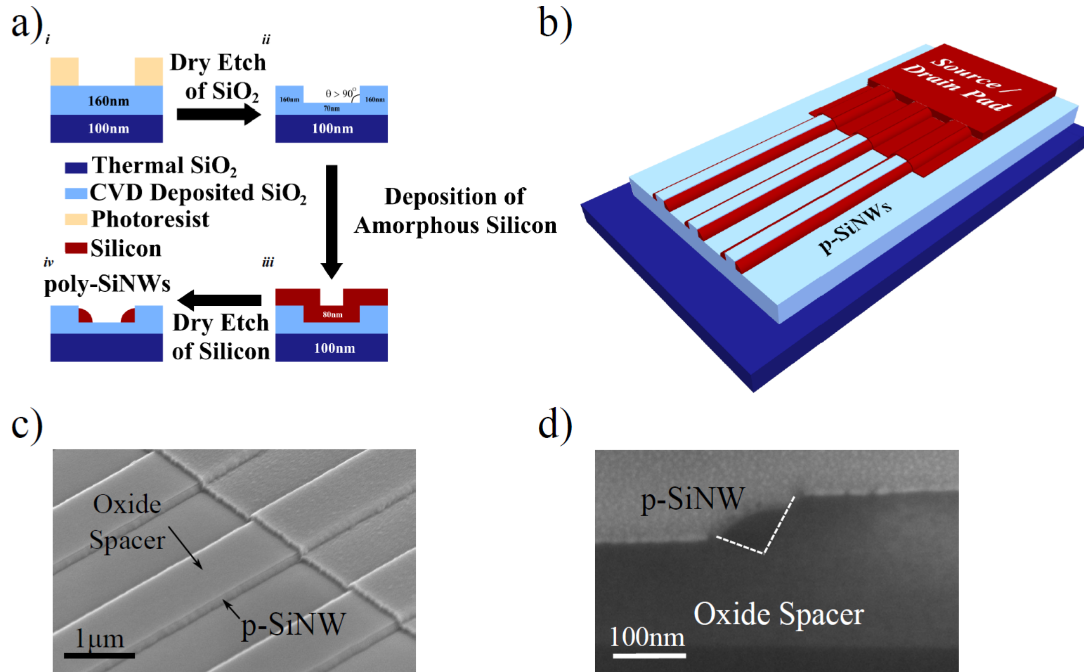

Figure 1: (a) Schematic representation of the fabrication process: *i*. photolithographic formation of the windows for etching; *ii*. dry etching of the CVD grown SiO_2 to form spacers with a side-angle which is slightly larger than 90°; *iii*. deposition of amorphous silicon; and *iv*. dry etching of the silicon to form nanowires. (b) A scehmatic representation of the final architecture. For graphical clarity, only one half of a device is shown. (c) An SEM micrograph of the source / drain pad region with part of the nanowire array device which lies in proximity to the pad. The micrograph shows the oxide spacers stretching from one pad to another (not shown here) and the P-SiNWs are just visible at the sides of the spacers. (d) A TEM micrograph of a single NW cross section.

a)

b)

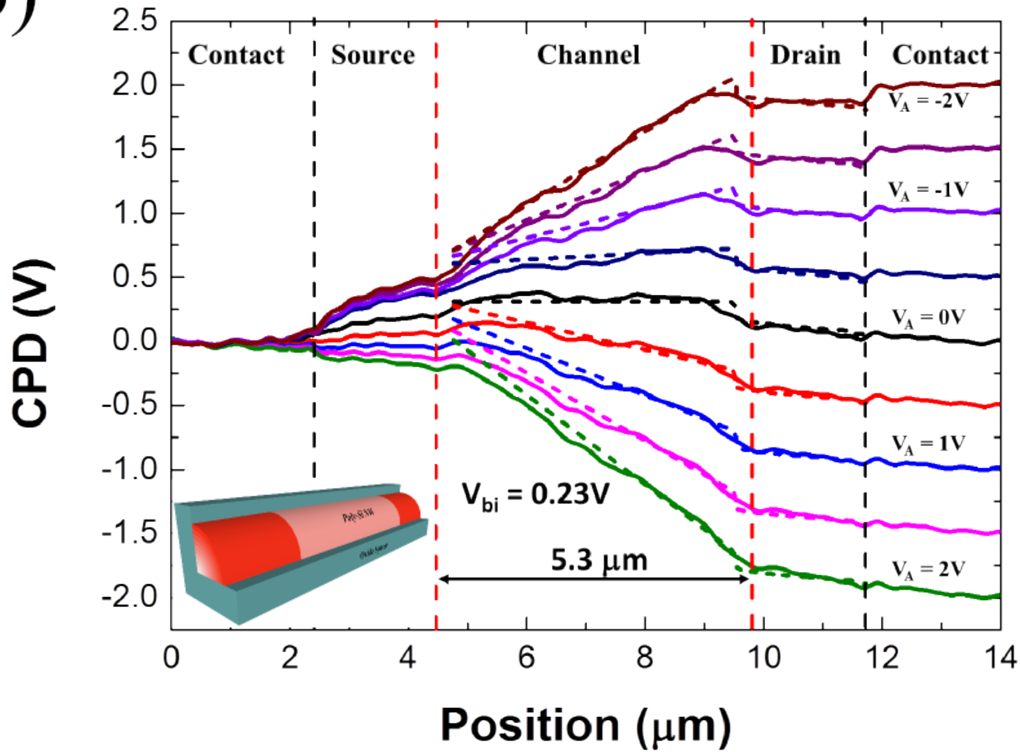

Figure 2: (a) A KPFM image of a single nanowire, showing the CPD map along the device. The figure shows a higher work function at the chennel (intrinsic) part of the nanowire than the work function at the source and drain regions, suggesting that the electron density within the central region is lower than on the sides. (b) CPD line profiles (solid) superimposed with numerical reconstruction results (dashed) for the P-SiNWs. The line profiles were taken across the axial direction of the P-SiNW at several drain biases spanning from $-2V$ to $2V$ with $0.5V$ steps. The source and drain pads, n^+ doped and intrinsic segments are clearly marked on the graph. The inset of (b) shows the model geometry (not to scale) used to simulate the devices.

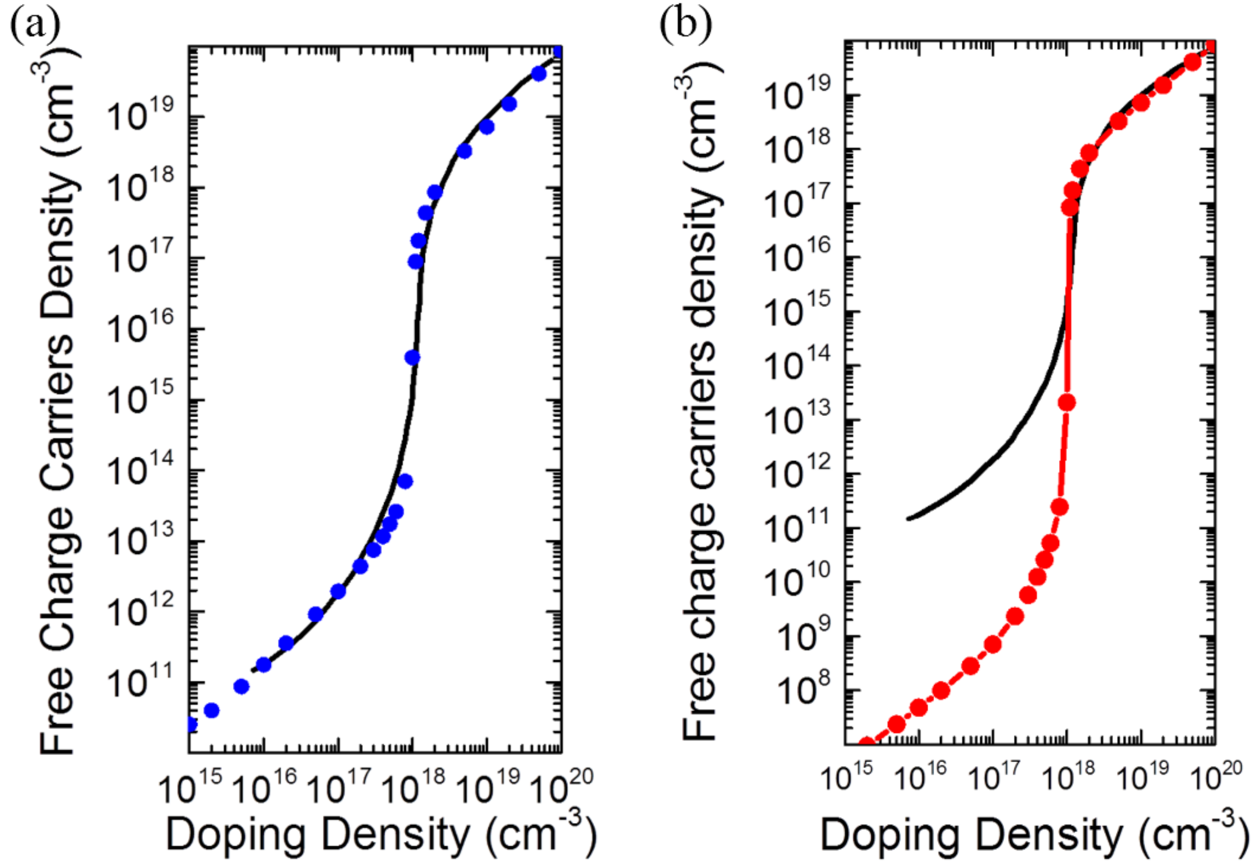

Figure 3: A comparison between the model for free charge carriers density as a function of doping presented by Seto in Ref. 18 (solid black line), and our proposed mean distribution model. (a) Reproduction of Seto's model where only a single trapping energy, at 0.37eV below the conduction band minimum, is taken into account (blue circles). The comparison shows that our calculation method is in good quantitative agreement with the published data. (b) Our model, fitted with a U-shape distribution of interface state traps. (red circles). The red solid line is a guide for the eyes. There is a remarkable qualitative similarity. However, a considerable difference is visible in the lower doping regime. The origins for which are given in the main text.

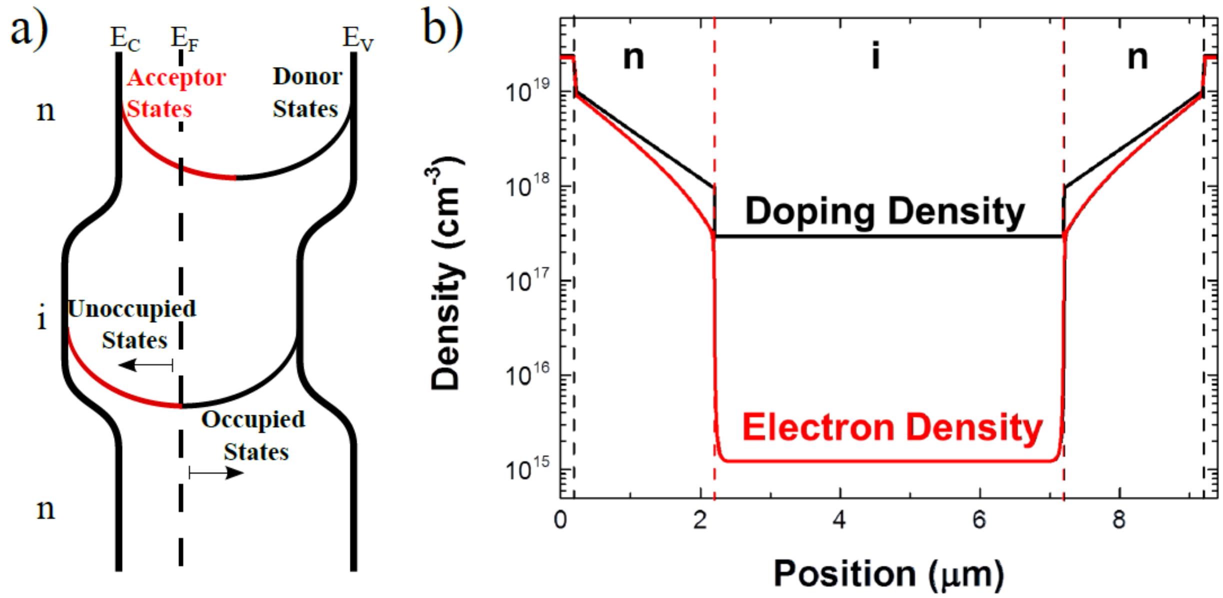

Figure 4: (a) An idealized band structure of the n^+-i-n^+ device, showing the GBIS dispersion across the band gap. Here, the black line represent states which are occupied with an electron, and the red line represent states which are not occupied. (b) A comparison between the chemical doping and the electron density at different regions across the wire, as extracted from the optimized simulation results. It is clearly seen in even though the central (intrinsic) region is only slightly less doped than the side regions, it is fully depleted due to charge carriers trapping in the GIBS.

ASSOCIATED CONTENT

Fabrication details, SIMS analysis of doped P-Si wafers, and examples of the electrostatic model optimization process are included in the supporting information. This material is available free of charge via the Internet at http://pubs.acs.org.

AUTHOR INFORMATION

Corresponding Author

*E-mail: yossir@eng.tau.ac.il

Notes

The authors declare no competing financial interest.

Author Contributions

† These authors contributed equally.

REFERENCES

(1) Hsiao, C.-Y.; Lin, C.-H.; Hung, C.-H.; Su, C.-J.; Lo, Y.-R.; Lee, C.-C.; Lin, H.-C.; Ko, F.-H.; Huang, T.-Y.; Yang, Y.-S. *Biosen. Bioelectron.* **2009**, *24*, 1223 – 1229.

(2) Lin, C.-H.; Hung, C.-H.; Hsiao, C.-Y.; Lin, H.-C.; Ko, F.-H.; Yang, Y.-S. *Biosen. Bioelectron.* **2009**, *24*, 3019 – 3024.

(3) Lin, C.-H.; Hsiao, C.-Y.; Hung, C.-H.; Lo, Y.-R.; Lee, C.-C.; Su, C.-J.; Lin, H.-C.; Ko, F.-H.; Huang, T.-Y.; Yang, Y.-S. *Chem. Commun.* **2008**, 5749–5751.

(4) Stern, E.; Klemic, J.F.; Routenberg, D.A.; Wyrembak, P.N.; Turner-Evans, D.B.; Hamilton, A.D.; LaVan, D.A.; Fahmy, T.M.; Reed, M.A. *Nature* **2007**, *445*, 519–522.

(5) Li, Z.; Chen, Y.; Li, X.; Kamins, T.I.; Nauka, K.; Williams, R.S. *Nano Lett.* **2004**, *4*, 245–247.

(6) Patolsky, F.; Zheng, G.; Lieber, C. M. *Future Medicine* **2006**, *1*, 51–65.

(7) Cui, Y.; Wei, Q.; Park, H.; Lieber, C. M. *Science* **2001**, *293*, 1289–1292.

(8) Zhang, G.-J.; Chua. J.-H.; Chee, R.-E.; Agarwal, A.; Wong, S.M.; Buddharaju, K.D.; Balasubramanina, N. *Biosen. Bioelectron.* **2008**, *23*, 1701 – 1707.

(9) Zheng, G.; Patolsky, F.; Cui, Y.; Wang, W.U.; Lieber, C.M. *Nat. biotechnol.* **2005**, *23*, 1294–1301.

(10) Gao, Z.; Agarwal, A.; Trigg, A.D.; Singh, N.; Fang, C.; Tung, C.-H.; Fan, Y.; Buddharaju, K.D.; Kong, J. *Anal. Chem.* **2007**, *79*, 3291–3297.

(11) Vu, X.; GhoshMoulick, R.; Eschermann, J.F.; Stockmann, R.; Offenhäusser, A.; Ingebrandt, S. *Sensor. Actuat. B-Chem.* **2010**, *144*, 354–360.

(12) Im, M.; Han, J.-W.; Lee, H.; Yu, L.-E.; Kim, S.; Kim, C.-H.; Jeon, S.C.; Kim, K.H.; Lee, G.S.; Oh, J.S.; Park, Y.C.; Lee, H.M.; Choi, Y.-K. *IEEE Electr. Device L.,* **2008**, *29*, 102–105.

(13) Su, C.-J.; Tsai, T.-I.; Liou, Y.-L.; Lin, Z.-M.; Lin, H.-C.; Chao, T.-S. *IEEE Electr. Device L.* **2011**, *32*, 521–523.

(14) Agarwal, A.; Buddharaju, K.; Lao, I.K.; Singh, N.; Balasubramanian, N.; Kwong, D.L. *Sensor. Actuat. A-Phys.* **2008**, *145-146*, 207–213.

(15) Choi, Y.-K.; Zhu, J.; Grunes, J.; Bokor, J.; Somorjai, G.A. *J. Phys. Chem. B.* **2003**, *107*, 3340–3343.

(16) Huang, P.-C.; Chen, L.-A.; Sheu, J.-T. *IEEE Electr. Device L.* **2010**, *31*, 216–218.

(17) Ecoffey, S.; Mazza, M.; Pout, V.; Bouvet, D.; Schmid, A.; Leblebici, Y.; Declercq, M.J.; Ionescu, A.M. *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International* **2005**, 269–272.

(18) Seto, J. Y. *J. Appl. Phys.* **1975**, *46*, 5247–5254.

(19) Demami, F.; Rogel, R.; Salaün, A.-C.; Pichon, L. *Phys. Status Solidi C.* **2011**, *8*, 827–830.

(20) De Graaff, H.C.; Huybers, M.; De Groot, J.G. *Solid State Electron.* **1982**, *25*, 67.

(21) Fortunato, G.; Migliorato, P. *Appl. Phys. Lett* **1986**, *46*, 1025.

(22) Amit, I.; Givan, U.; Connell, J.G.; Paul, D.F.; Hammond, J.S.; Lauhon, L.J.; Rosenwaks, Y. *Nano Lett*. **2013**, *13*, 2598–2604.

(23) Demami, F.; Pichon, L.; Rogel, R.; Salaün, A.-C. *IOP Conference Series: Materials Science and Engineering* **2009**, *6*, 012014.

(24) Chang, C.-W.; Deng, C.-K.; Chang, H.-R.; Chang, C.-L.; Lei, T.-F. *IEEE Electr. Device L.* **2007**, *28*, 993–995.

(25) Wu, C.-Y.; Liao, T.-C.; Yu, M.-H.; Chen, S.-K.; Tsai, C.-M.; Cheng, H.-C. *VLSI Technology Systems and Applications (VLSI-TSA), 2010 International Symposium on* **2010**, 61–62.

(26) Rosenwaks, Y.; Shikler, R.; Glatzel, T.; Sadewasser, S. *Phys. Rev. B* **2004**, *70*, 085320.

TABLE OF CONTENTS FIGURE