Letter

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Just Accepted

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ABSTRACT:

We report the development of highly efficient and stable solution-processed organic light emitting transistors (OLETs) that combine a polymer heterostructure with the transparent high-k dielectric poly(vinylidenefluoride$_{0.62}$-trifluoroethylene$_{0.31}$-chlorotrifluoroethylene$_{0.7}$) (P(VDF-TrFE-CTFE)). The polymer heterostructure comprises of the poly[4-(4,4-dihexadecyl-4H-cyclopenta[1,2-b:5,4-b']dithiophen-2-yl)-alt-[1,2,5]thiadiazolo[3,4-c]pyridine] (PCDTPT) and Super Yellow as charge transporting and light emitting layers, respectively. Device characterization shows that the use of P(VDF-TrFE-CTFE) leads to larger channel currents ($\approx$2 mA) and lower operating voltages (-35 V) than for previously reported polymer based OLETs. Furthermore, the combined transparency of the dielectric and gate electrode, results in efficient bottom emission with external quantum efficiency of $\approx$0.88 % at a luminance L $\geq$ 2000 cd m^{-2}. Importantly, the resulting OLETs exhibit excellent shelf life and operational stability. The present work represents a significant step forward in the pursuit of all-solution-processed OLET technology for lighting and display applications.

KEYWORDS: organic light-emitting transistors, high-k dielectric, polyvinylidene

fluoride copolymer

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1. INTRODUCTION

Organic light-emitting diodes (OLEDs) are now recognized as an important technology for application in ultrathin flexible displays on plastic or metal foil-base substrates. OLED based smart phones and large-size TVs have already entered the market, with the majority of these products utilizing rigid glass substrates. Despite the tremendous progress however, improvements in power efficiency, lifetime and cost are still needed in order to realize the full potential of the technology.[1-3] Such requirements are even more pertinent for lighting and have driven development of solution-based fabrication processes that will also impact on the display sector.[4-5] Additionally, the control circuitry that drives the OLED pixels needs to transition from the rigid and brittle inorganic semiconductor technologies to soluble semiconductors deposited at low temperature which will enable integration with flexible plastic substrates. However, the low carrier mobility of organic semiconductors is not yet sufficient for such current-driven display backplanes [6-8] and oxide semiconductors look more

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promising in the first instance, albeit with the added challenge to deposit these materials at appropriate temperatures.[9]

An alternative to an OLED with associated drive circuitry is to combine the functionality of switching and light-emission in a single device, an organic light-emitting transistor (OLET).[10-12] The latter combines both light-emitting and switching functions in a single device. Because of this multi-functionality, OLETs provide great promise for simple processing of advanced pixel architectures.[13-16]

Despite the significant progress that has already been made in the performance of OLETs, there are still numerous technical obstacles that need to be overcome, including the simultaneous achievement of high luminance, high external quantum efficiency (EQE) and low voltage operation.[17-21] A key strategy to increase the driving current capabilities while reducing the operating voltage is to introduce high-k gate dielectrics. Previously, OLETs with low operation voltages (~10 V) have been reported employing Al_2O_3/PMMA and Al_2O_3/ZrOx bilayer gate dielectrics, however, the Al_2O_3 thin films were deposited by atomic layer deposition (ALD), which has a slow deposition rate and the Al_2O_3/ZrO$_x$ bilayer required ozone exposure and a photochemical curing step.[22-23] In addition, OLETs with a thermally deposited trilayer organic stack and a poly(vinylidenefluoride-trifluoroethylene-chlorotrifluoroethylene) P(VDF-TrFE-CFE) dielectric have been reported to exhibit higher EQE with reduced operating voltage, when compared to those with a low-k poly(methyl methacrylate) (PMMA) dielectric layer.[24-26] However, the P(VDF-TrFE-CTFE) polymer has not been used in OLETs before despite its intriguing properties, including high-k, outstanding electromechanical response, and low dielectric leakage.[27-31]

Here, we demonstrate efficient and stable, multi-layer solution-processed OLETs in a non-coplanar electrode structure comprising the high-k dielectric P(VDF-TrFE-CTFE), a charge-transporting layer of poly[4-(4,4-dihexadecyl-4H-cyclopenta[1,2-b:5,4-b']dithiophen-2-yl)-

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alt-[1,2,5]thiadiazolo[3,4-c]pyridine] (PCDTPT), and a light-emissive layer of the Super Yellow polymer. The P(VDF-TrFE-CTFE) dielectric exhibited excellent endurance and the devices consequently showed high operational stability and device lifetime. Carefully engineered bottom emission OLETs exhibited Luminance of >2000 cd/m^2 and an EQE value of ~0.88 %.

2. EXPERIMENTAL SECTION

2.1. Transistor Fabrication and Characterization.

Super Yellow (PDY-132), poly[4-(4,4-dihexadecyl-4H-cyclopenta[1,2-b:5,4-b']dithiophen-2-yl)-alt-[1,2,5] thiadiazolo[3,4-c]pyridine] (PCDTPT), and poly(vinylidenefluoride$_{0.62}$-trifluoroethylene$_{0.31}$-chlorotrifluoroethylene$_{0.7}$) (P(VDF-TrFE-CTFE)) polymers (see Figure 1 (a) for chemical structures) were purchased from Merck, 1-Material and Piezotech Arkema. Super Yellow and PCDTPT were dissolved in toluene and chlorobenzene at 7 mg/mL and 5 mg/mL concentration, respectively. A 2-butanone solution of P(VDF-TrFE-CTFE) was prepared at a concentration of 30 mg/mL and vigorously stirred overnight. The P(VDF-TrFE-CTFE) solution was spin-coated (1500 rpm, 60 s, 300 nm-thickness layer) on ITO-glass substrates pre-patterned to form the gate electrode and annealed at 100 °C for 20 min. PCDTPT was spin-coated (2000 rpm, 40 s, 50-nm thickness layer) on top of the P(VDF-TrFE-CTFE) layer, followed by annealing at 150 °C for 30 min. MoO$_3$ (~ 5 nm) and Au (~ 20 nm) were then thermally deposited on top of the PCDTPT layer using a shadow mask to define the source electrode. Super Yellow was next spin-coated (2500 rpm, 30s followed by 3000 rpm, 10 s, 100-nm thickness layer) and again annealed at 150 °C for 30 min. The device structure was completed by shadow-masked vacuum deposition of the drain

electrode, comprising Cs_2CO_3 (~ 5 nm) capped with Al (~ 20 nm). The transistor channel length and width were 75 μm and 14 mm, respectively.

2.2. Measurements.

The electrical characterisation of the devices was performed within a nitrogen-filled glove box using an Agilent B2902A semiconductor parameter analyser. The capacitance-frequency (C-f) response of the P(VDF-TrFE-CTFE) layer was measured using a Fluxim Paios measurement system. Electroluminescence (EL) and photoluminescence (PL) spectra were measured using a UV-vis spectrometer (Ocean-Optics USB4000-XR). Charge carrier mobility was calculated from the transistors' transfer characteristics in the saturation regime. The luminance of the devices was determined from the photocurrent generated by a calibrated photodiode, referenced to a standard luminance meter (Minolta LS-100), taking into account the relative emission area. EQE was obtained from the luminance, source-drain current (I_D), and emission spectra of the devices, assuming Lambertian emission. Tapping mode atomic force microscope (AFM) images were recorded using a Digital Instruments Dimension 3100 scanning probe microscope (SPM) with NanoScope IVa SPM control station. Optical transmission spectra, over the wavelength range 400-850 nm, were measured using a Shimadzu UV-1800 spectrophotometer.

3. RESULTS AND DISCUSSION

Figure 1 shows a schematic of the device structure, the energy level alignments and a simplified operation model. Super Yellow was chosen as the emissive layer with PCDTPT as hole-transporting layer and P(VDF-TrFE-CTFE) as the high-k gate dielectric. Improved charge injection into the organic layers was facilitated by the non-coplanar device structure

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with asymmetric source and drain (S-D) contacts (Figure 1 (b)). The device operation can be

considered in terms of a combination OLED-transistor structure (Figure 1(c)). The highest

occupied (HOMO) and lowest unoccupied (LUMO) molecular orbital levels of each material

(Figure 1 (b)) are taken from the literature.[32-34] As described in Figure 1(c), holes are injected

from the MoO_3/Au source contact into the HOMO energy level of the PCDTPT layer and

subsequently transported across the channel by the PCDTPT layer. Electrons on the other

hand are injected from the Cs_2CO_3/Al drain contact into the LUMO of the Super Yellow

layer where they combine with holes to form excitons that decay radiatively generating

optical photons. Here we note that the presence of MoO_3 layer at the interface between Au

and PCDTPT promotes contact doping that increases the electrical conductivity of the bulk

film near the contact, thereby reducing contact resistance.[35-36] In addition, the Cs_2CO_3

electron injection interlayer can play an important role in lowering the work function of Al

(*ca.* −2.1 eV for Cs_2CO_3/Al *vs* -4.2 eV for Al) by forming an Al-O-Cs complex.[37]

Figure 1

We first investigated the gate dielectric using a metal (ITO) - insulator (P(VDF-TrFE-

CTFE)) - metal (Al) (MIM) structure, whose capacitance *vs* frequency (C-f) response over

the range 10 to 10 MHz is shown in Figure 2(a). The capacitance decreased with increasing

frequency as the polarization response time is limited by dipole alignment in the high-*k*

dielectric.[38] The P(VDF-TrFE-CTFE) film capacitance (C) measured at 10 kHz is 86.3

nF/cm^2, from which a *k* value of 29.3 was calculated using the parallel plate capacitor

equation [C = (kε_0A) / d], with ε_0, A, and d, being the vacuum permittivity, area of overlap of

the electrodes, and film thickness, respectively. These C and *k* values are comparable to those

obtained from a Si/SiO$_2$/P(VDF-TrFE-CTFE)/Al capacitor (Figure S1). The relatively high

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breakdown voltage, demonstrating dielectric endurance up to 2.5 MV/cm ($\approx$ 75 V), is shown

in the current density-electric field (J-E) graph (Figure 2(b)) and a leakage current density of

less than 10^{-5} A/cm^2 was observed. We note that the P(VDF-TrFE-CTFE) dielectric layer did

not reach its breakdown voltage in the studied bias range.

For full transistor structures, as shown in Figure 2(c), typical output characteristics (drain

voltage *vs* drain current, V_D–I_D) with distinct linear and saturation regimes were observed.

Large I_D values (> 1mA) were observed when V_G was biased at above -20 V (see Figure

2(d)). Based on height-mode AFM images of P(VDF-TrFE-CTFE) and PCDTPT layers on

glass and ITO-glass substrates (see Figure S2) both polymers form smooth layers; a root

mean square roughness 0.92 nm, 1.74 nm 1.24 nm and 1.24 nm was found for P(VDF-

TrFE-CTFE) on glass, PCDTPT on glass, PCDTPT on P(VDF-TrFE-CTFE) coated glass and

PCDTPT on P(VDF-TrFE-CTFE) coated ITO-glass, respectively. The surface morphology is

uniform, facilitating lateral charge transport in the channel region and reducing charge

trapping at the surface of the P(VDF-TrFE-CTFE) and PCDTPT layers. In addition, as shown

in Figure 2(d), we observe the expected hysteresis between the forward and reverse scan

transfer curves, associated with ferroelectric polarization switching in the high-*k* dielectric.

The hole mobilities (μ_h) extracted from the transfer curves were 0.55 and 0.39 cm^2 V^{-1} s^{-1}

and threshold voltages (V_{TH}) were -0.83 and 4.36 V for the forward and reverse scans,

respectively. Both μ_h and V_{TH} were calculated in the saturation region using the gradual

channel approximation model. The high capacitance of the P(VDF-TrFE-CTFE) layer allows

low voltage operation due to the significant accumulation of holes at the PCDTPT/P(VDF-

TrFE-CTFE) interface.

Figure 2

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The variation in luminance and EQE at V_D = -35 V measured from the bottom and top of the device (c.f. Figure S3) are shown as a function of V_G in Figures 3(a) and (b), respectively. The bottom emission luminance (L = 2368.9 cd m^{-2}) at V_G = -35 V was ~13.6 times higher than the top emission (L = 174.5 cd m^{-2}). The higher luminance for the bottom emission was observed across a wide range of V_D and V_G values (see optical output characteristics in Figure S4). In addition, the EQE value for the bottom emission (0.88 %) was approximately one order of magnitude higher than for the top emission (0.066 %). Both EQE values saturate for $|V_G| \geq 20$ V (Figure 3(b)), consistent with balanced hole and electron injection and minimal exciton quenching at high electric fields. The EQE is presented as a function of luminance in Figure 3(c), with good bottom emission performance achieved all the way up to 2500 cd/m^2. Also shown as an inset to Figure 3(c) is an image of Super Yellow emission emanating from such a device biased at $V_D = V_G = -35$ V. The observed hysteresis in the luminance / EQE *vs* V_G curves between forward and reverse scans can be attributed to the ferroelectric properties of the P(VDF-TrFE-CTFE) layer leading to differing amounts of charge recombination. The electroluminescence (EL) spectrum for such an OLET is shown in Figure 3(d), closely overlapping but narrowed relative to the corresponding PL spectrum (Figure S5). The EL peaks at λ = 550 nm, with the PL extending further into the red. Figure 3(d) also shows transmission spectra measured through an ITO-glass substrate coated with P(VDF-TrFE-CTFE) and PCDTPT (T_{Bottom}) and through a spectrosil substrate coated with Cs_2CO_3 and Al (T_{Top}), with layer thicknesses as used in the device. These samples therefore represent the light path from the Super Yellow emission layer in both directions through a half-stack but without accounting for microcavity resonance effects in the full stack structure. We observe that T_{Bottom} (565 nm) $\approx$ 91.03 % is significantly higher than T_{Top} (565 nm) $\approx$ 19.3 %. The even higher EQE ratio between bottom emission and top emission is a consequence of the latter effects.

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Figure 3

Device operational stability was monitored over a 250 s time window for ITO-glass/ P(VDF-TrFE-CTFE)/PCDTPT/Super Yellow/Cs_2CO_3/Al OLETs, with I_D and bottom emission luminance values continuously recorded under constant bias ($V_D = V_G = -35$ V) and in ambient conditions. As shown in Figure 4(a), I_D decreased by a relatively modest amount ($\sim 11\%$) over this period, indicating relatively good electrical stability for an un-encapsulated structure. More importantly, Figure 4(b) demonstrates that only a marginal reduction by ~ 2.1 % in the device luminance occurred over the same period. Typically, both extrinsic (e.g. oxygen, water, and temperature) and intrinsic (e.g. excited state and charge carrier interactions) factors are complicit in degradation, with reductions in charge carrier mobility and charge injection efficiency previously reported to result.[39] Our devices showed more stable charge carrier mobility and charge injection, leading to only a marginal reduction in device luminance over the period observed. A further study will be needed to explore the longer-term device lifetime and associated degradation mechanisms.

Figure 4

4. CONCLUSIONS

In conclusion, we have demonstrated efficient and stable solution-processed bottom-emitting organic light emitting transistors using a high-k dielectric in combination with an asymmetric electrode device architecture. The P(VDF-TrFE-CTFE) dielectric layer was shown to play a critical role in reducing the operating voltage while the asymmetric electrode

architecture improved the hole and electron injection into the light emissive Super Yellow layer, leading to efficient radiative recombination. Importantly, the OLETs showed high maximum channel currents ($\approx$ 2 mA), with a hole mobility μ_h value in the range 0.39 - 0.55 $cm^2\ V^{-1}\ s^{-1}$. The high μ_h together with the obtained EQE of $\approx$ 0.88 % allows the luminance for bottom emission devices to reach values in excess of 2000 cd/m^2. Noticeably, the OLETs exhibited promising operating stability with peak EQE and luminance measured at maximum I_D. It is evident that introduction of a high-k dielectric can positively influence both the operational stability and lifetime of the OLETs. Our results thus present a significant opportunity to advance OLET performance towards efficient, bright and stable operation in numerous applications, including solid-state lighting, optical communications, smart pixels and integrated optoelectronic systems.

■ ASSOCIATED CONTENT

Supporting Information

This material is available free of charge via the Internet at http://pubs.acs.org.

■ AUTHOR INFORMATION

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Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENT

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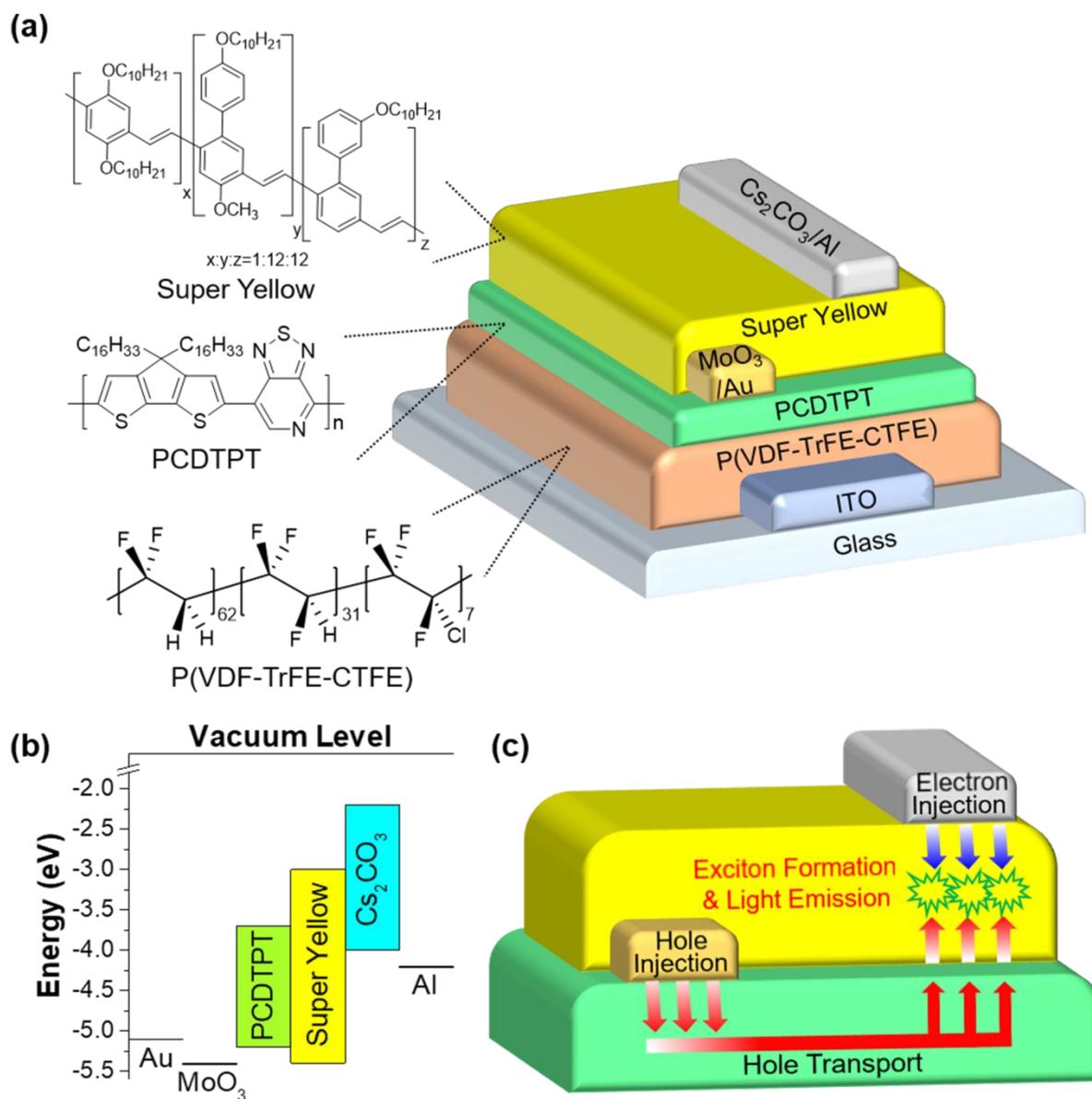
Figure 1. (a) Chemical structures of Super Yellow, PCDTPT, and P(VDF$_{0.62}$-TrFE$_{0.31}$-CTFE$_{0.7}$) polymer light-emitting, hole-transporting, and gate dielectric layer materials, respectively; also shown is a schematic device structure. (b) Energy level diagram for the studied organic light-emitting transistor structures with asymmetric source-drain electrodes. (c) Schematic depiction of the operating mechanism of the OLETs, showing hole injection from the source electrode into PCDTPT, lateral hole transport, electron injection from the drain electrode into Super Yellow, exciton formation within that layer and light emission therefrom.
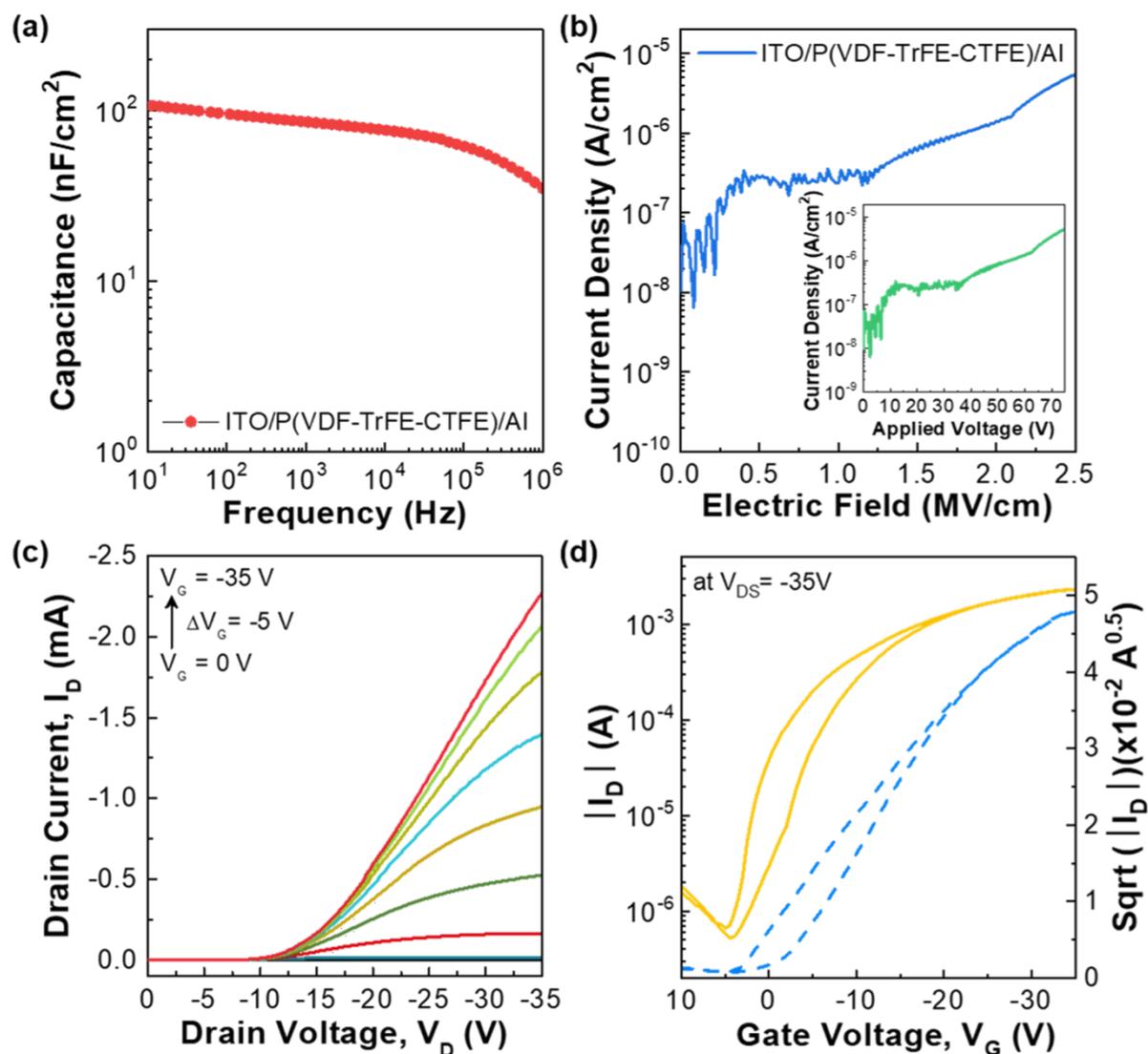
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Figure 2. (a) Capacitance-frequency, and (b) current density-electric field characteristics for MIM capacitor structures comprising ITO/P(VDF-TrFE-CTFE)/Al. (c) Output and (d) transfer curves for the studied OLETs.
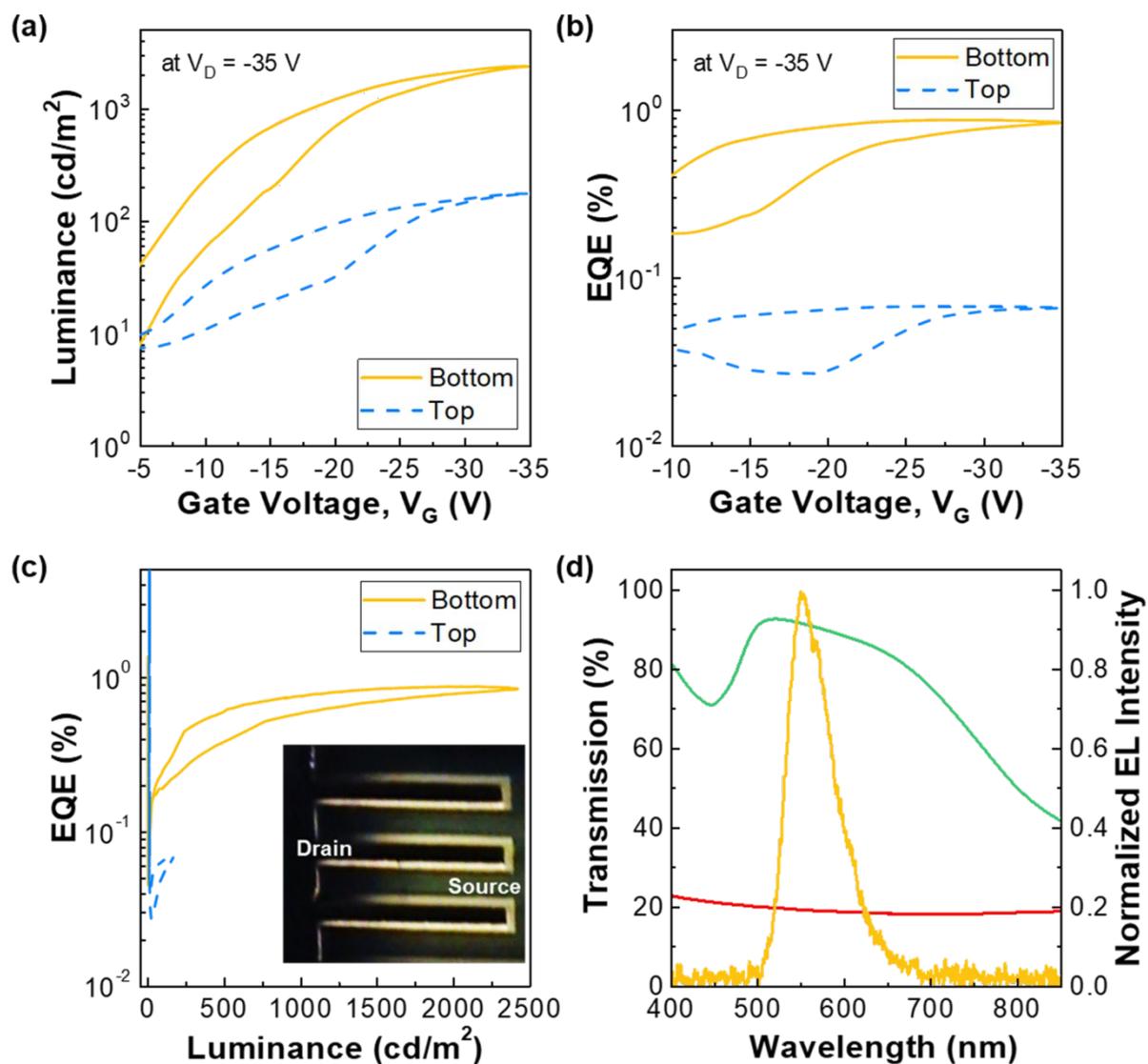
Figure 3. (a) Optical transfer characteristics, (b) external quantum efficiency (EQE), and (c) EQE as a function of device luminance for both top and bottom emission directions. Inset in (c) shows an OLET during operation. (d) Normalized electroluminescence (EL) spectrum and transmittance spectra for the top (Cs_2CO_3/Al; red line) and bottom (glass/ITO/P(VDF-TrFE-CTFE)/PCDTPT; green line) electrode stacks.
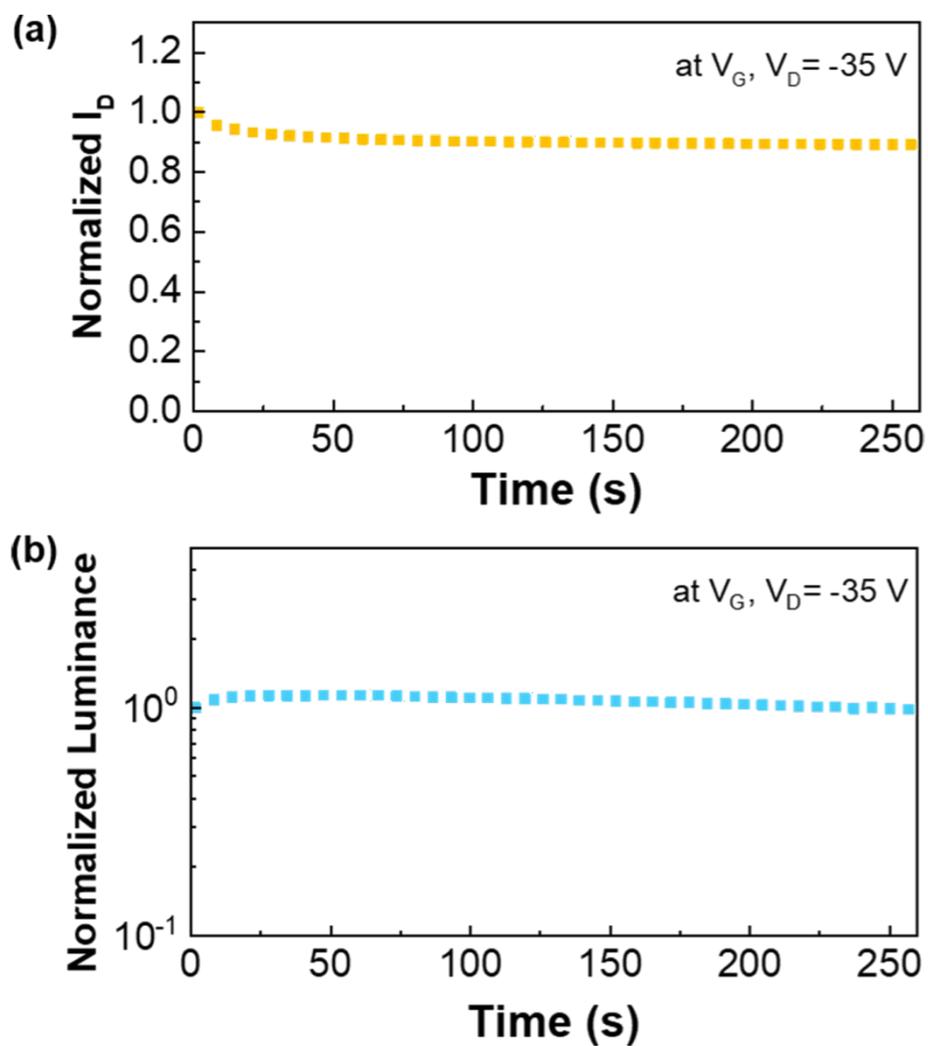
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Figure 4. Operational stability for a PCDTPT/Super Yellow OLET. (a) Normalized I_D, and (b) normalized luminance under constant driving conditions of $V_G = V_D = -35$ V.

Table 1. Performance parameters of high-k dielectric-based OLETs (Note that all transistor parameters were extracted from more than 5 devices and the averaged values are displayed).

Mobility ($cm^2V^{-1}s^{-1}$)	On/off ratio	Vth (V)	EQE (%)	Luminance ($cd\ m^{-2}$)
0.55 / 0.39 (Forward / Backward)	4340 / 3460 (Forward / Backward)	-0.83 / 4.36 (Forward / Backward)	0.11 / 0.88 (Top / Bottom Emission)	180 / 2422 (Top / Bottom Emission)

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