Effect of Gate Conductance on Hygroscopic Insulator Organic Field Effect Transistors

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Abstract: Hygroscopic insulator field effect transistors (HIFETs) are a class of low voltage operating organic transistors that have been successfully demonstrated for biosensing applications through modification of the gate electrode. However, the modification of the gate electrode often leads to non-ideal transistor characteristics due to changes in its intrinsic electrical properties. This work investigates the effect of gate conductance in HIFETs using PEDOT:PSS as a model gate electrode. This in-depth study reveals that a reduction in gate conductance results in a reduction in the effective gate voltage and plays an important role in defining HIFET characteristics. Key figures of merit, including ON/OFF ratio, threshold voltage, transconductance and saturation mobility increase with increasing gate conductance and reach a plateau once optimum gate conductance is attained. This effect is attributed to a decrease in the effective gate voltage along the gate electrode arising from its resistivity when a gate leakage current is present. These results are widely applicable and serve as design rules for HIFET device optimization.

1. Introduction

Organic thin film transistors (OTFTs) are a unique platform for the development of tailored sensors for diverse applications. Owing to the intrinsic properties of organic materials, OTFTs can be thin, lightweight,[1] flexible,[2] printable[3] and biodegradable,[4] and as transistors, OTFTs exhibit signal amplification and transduction capabilities. OTFT sensors have been proposed for a range of applications including medicine,[5, 6] food quality control,[7] and environmental monitoring.[8] In such sensors, an OTFT interacts with a targeted analyte to produce an electrical response. Typically, this will either involve direct interaction of the analyte with the semiconductor channel,[9] or a modification of the electric field between the channel and the gate[10] to modulate the channel current.

Among the different classes of OTFTs available for sensing, hygroscopic insulator field effect transistors (HIFETs) are particularly attractive, combining advantages of different device architectures. Like standard organic field effect transistors (OFETs), HIFETs are fully solid state and operate in accumulation mode (normally 'off'),[11] thus offering an advantage over standard organic electrochemical transistors (OECTs) that require the additional complexity of electrolyte containment and are typically depletion mode (normally 'on') and thus possibly less power efficient.[12] Yet, in common with OECTs, HIFETs operate under low voltages (<1 V), below the breakdown threshold of water,[13] ideal for sensing in aqueous conditions. Additionally, HIFETs have a fully solution processable device structure, compatible with inexpensive large scale manufacturing techniques.[3] HIFETs have been reported not only for application as sensors of various analytes including solvents,[14] glucose,[5] and protons,[16] but also as components in inverter circuits[14] and ring oscillators.[15] Reports indicate slow switching speed as a limitation of HIFETs, but is not considered to be a significant concern for most sensing applications.[14, 17]

The operating mechanism of HIFETs has been attributed to mobile ions in the moisturized hygroscopic dielectric. Using poly(4-vinylphenol) (PVP) as the dielectric, the phenol groups ionise in the presence of moisture absorbed from the ambient atmosphere, mobilising cations (H^+). The cations drift away from the transistor channel under the applied gate potential, leaving the fixed ionised phenol groups at the interface with the organic semiconductor, where electrochemical doping is thought to take place, modulating channel conductivity.[18] Sensing using HIFETs has been accomplished through modification of the gate electrode to include membranes and/or recognition elements suitable to the analyte.[5, 16] However, the modified gate electrodes exhibit poorer electrical characteristics, resulting in non-ideal current saturation (channel current, I_{ds}, is not constant with drain-source voltage, V_{ds}, in the saturation regime), larger OFF currents, and poorer current modulations with gate voltage.[5, 16]

Literature commenting directly on the effects of gate conductance in OTFTs is limited. Low resistivity is sometimes discussed as a key requirement for gate electrodes,[19] and resistance in a gate electrode is known to increase signal delay, an important consideration for active matrix panels.[20] Recently, we demonstrated that, for our proton sensitive HIFET gated with a film of proton conducting sulfonated mesoporous silica nanoparticles (SO_3H-Si-MCM-41), the transistor characteristics are significantly improved by adding conductive polymer poly(3,4-ethylenedioxythiophene) doped with poly(styrene sulfonate) (PEDOT:PSS), while maintaining proton sensitivity.[21] This suggests a strong relationship between transistor performance and gate conductance for HIFETs. In this report, we have systematically studied and established the effect of the conductance of the gate electrode on key figures of merit for HIFETs, using PEDOT:PSS as the model gate electrode.

2. Results and Discussion

2.1. Device Structure and Gate Conductance Variation

Our HIFET device employs a top gate/bottom contact architecture (**Figure 1**a, b), with poly(3-hexylthiophene-2,5-diyl) (P3HT) as the semiconductor and poly(4-vinylphenol) (PVP) as the hygroscopic dielectric, closely following previous reports.[5, 11, 16, 21] The HIFETs have a channel length of 50 μm and width of 3 mm and were fabricated using solution processing methods (details in *experimental section*) on pre-patterned indium tin oxide (ITO) source and drain electrodes, with a separate gate contact pad.

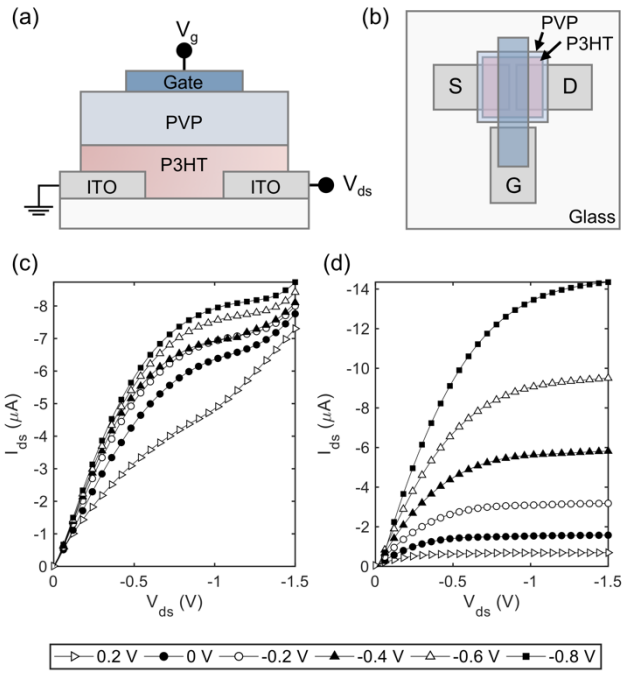

Figure 1. HIFET device structure, (a) cross section, and (b) top view. Output characteristics of a HIFET gated with (c) SO_3H-Si-MCM-41 and (d) PEDOT:PSS.

Typical output characteristics of a modified HIFET using SO_3H-Si-MCM-41 as the gate for proton sensitivity are shown in Figure 1c. Though the output characteristics have defined linear and saturations regimes, the device exhibits poorer saturation current, lower ON current and higher OFF current than a HIFET with a PEDOT:PSS gate (Figure 1d), which has a much higher conductance.[21] This suggests a strong influence of gate electrode conductance on transistor characteristics.

To fully understand the effect of gate conductance on HIFET characteristics, HIFETs were fabricated with PEDOT:PSS gates of varied conductance. This was obtained by diluting the commercial as-received dispersion of PEDOT:PSS with water. The conductance ($G = I/V$) of 3×3 mm PEDOT:PSS films cast from a range of concentrations was determined using I-V sweeps (Figure S1a), and was observed to increase approximately linearly with the concentration of the PEDOT:PSS dispersion (**Figure 2**). Diluted PEDOT:PSS dispersions yield thinner films (Figure S1b), resulting in the reduced conductance. We note that gate conductance values in devices may differ slightly from those presented in Figure 2 due to a difference in film dimensions, while nevertheless exhibiting the same relative conductance.

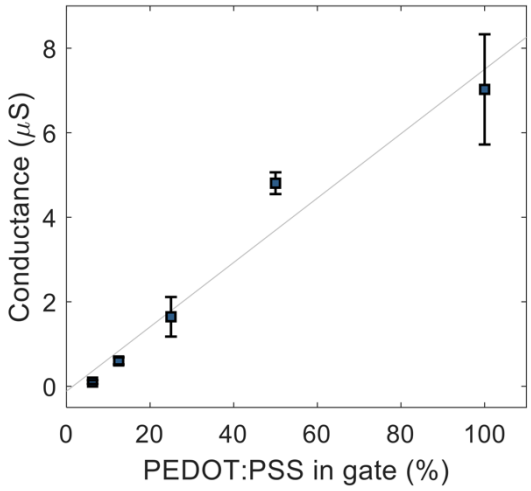

Figure 2. Conductance of PEDOT:PSS gates with dilution.

2.2. Output and Transfer Characteristics

Output and transfer characteristics of HIFETs with PEDOT:PSS gates of 100%, 25% and 6.25% are shown in **Figure 3**a-f. From Figure 3a and 3b, the HIFET with a gate electrode of 100% PEDOT:PSS dispersion exhibited excellent output and transfer characteristics, comparable to similar PEDOT:PSS gated devices previously reported.[11, 21] The 100% PEDOT:PSS gated HIFET exhibited a well-defined saturation regime, distinct current modulations, and relatively low OFF currents. In common with previous reports, our HIFETs operate under low voltages. As mentioned earlier, this is an advantage of the HIFET device architecture over standard

OFETs as low voltages allow operation under aqueous conditions, where voltages beyond 1.23 V can induce electrolysis of water.[13]

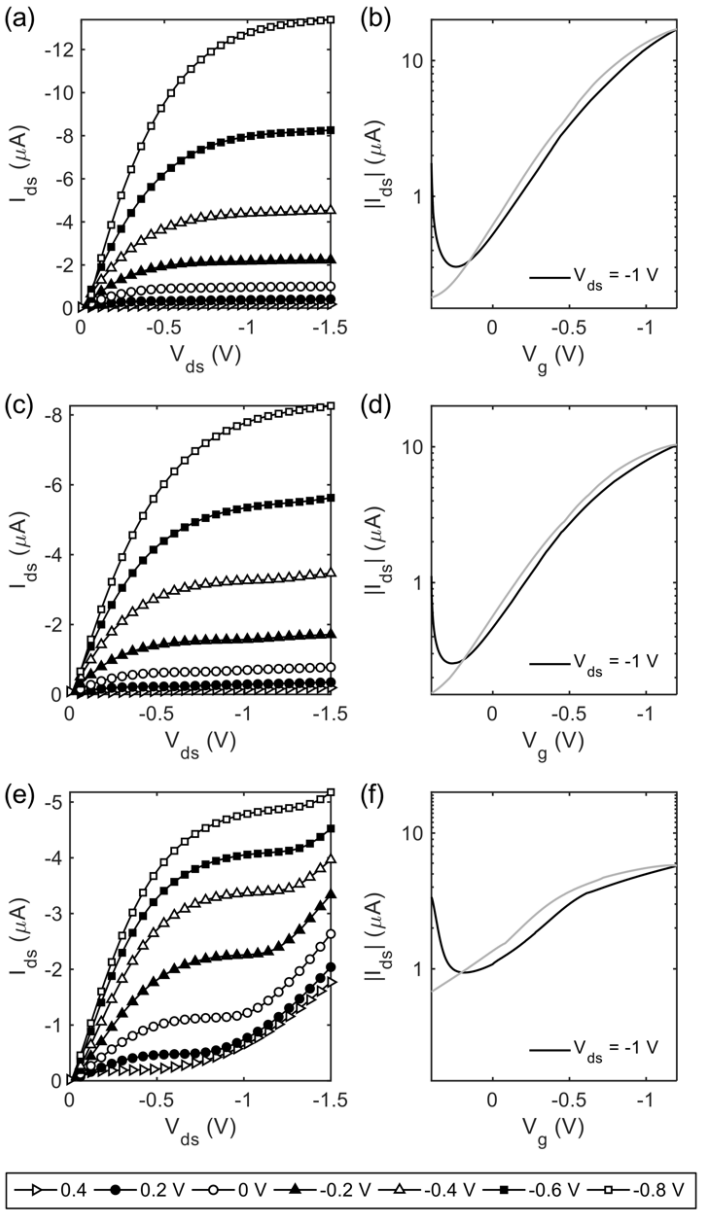

Figure 3. Output and transfer characteristics for HIFETs gated by PEDOT:PSS films deposited from (a,b) 100%, (c,d) 25% and (e,f) 6% of the stock PEDOT:PSS dispersion. The legend below indicates gate voltages for the output curves. Black and grey lines in transfer curves indicate forward and reverse sweeps, respectively.

As the gate conductance reduces, a significant effect is poorer current saturation. Rather than maintaining a constant I_{ds} in the saturation regime, I_{ds} increases with V_{ds}, particularly beyond -1 V. This effect is subtly present with a 25% PEDOT:PSS gate (Figure 3c), but intensifies with decreasing gate conductance, becoming prominent at 6.25% PEDOT:PSS (Figure 3e). This

reflects similar trends to the output characteristics of HIFETs gated with SO_3H-Si-MCM-41 (Figure 1c). Previous studies on HIFETs with Nafion gate electrodes report similar behavior in the saturation regime,[5] an effect that we believe is due to the poor conductance of Nafion. Output characteristics for intermediate 50% and 12.5% gates are included in Figure S2.

The non-ideal character of the saturation regime has been reported earlier in HIFETs with the same layout as shown in Figure 1b, where a third ITO contact pad has been used to interface with the gate. [5] In these earlier reports, there was some concern that when the gate conductance was very low the ITO contact functions as an offset gate and distorts the saturation current. We have shown that this is not the case (see Figure S3). Rather, this is consistent with known effects from large gate-drain leakage currents, manifesting as large OFF currents.[22] This is consistent with our observation of increased OFF current for 12.5% and 6.25% PEDOT:PSS gates (**Figure 4**b), where deviation from saturation is most apparent. In general, we observe that non-idealities in both output and transfer curves correspond to situations with large gate current. For example, the initial large I_{ds} in the forward transfer sweeps correspond to large positive gate currents (adding to I_{ds}), the most ideal regions to where gate currents approach zero, and reduced current in the tail regions correspond to where an increasing negative gate current (subtracting from I_{ds}) is observed (Figure S6). The gate current during output sweeps (Figure S7) likewise show that a positive gate current corresponds to the distortions in the saturation regime. The effect is more significant for devices with poorly conducting gates.

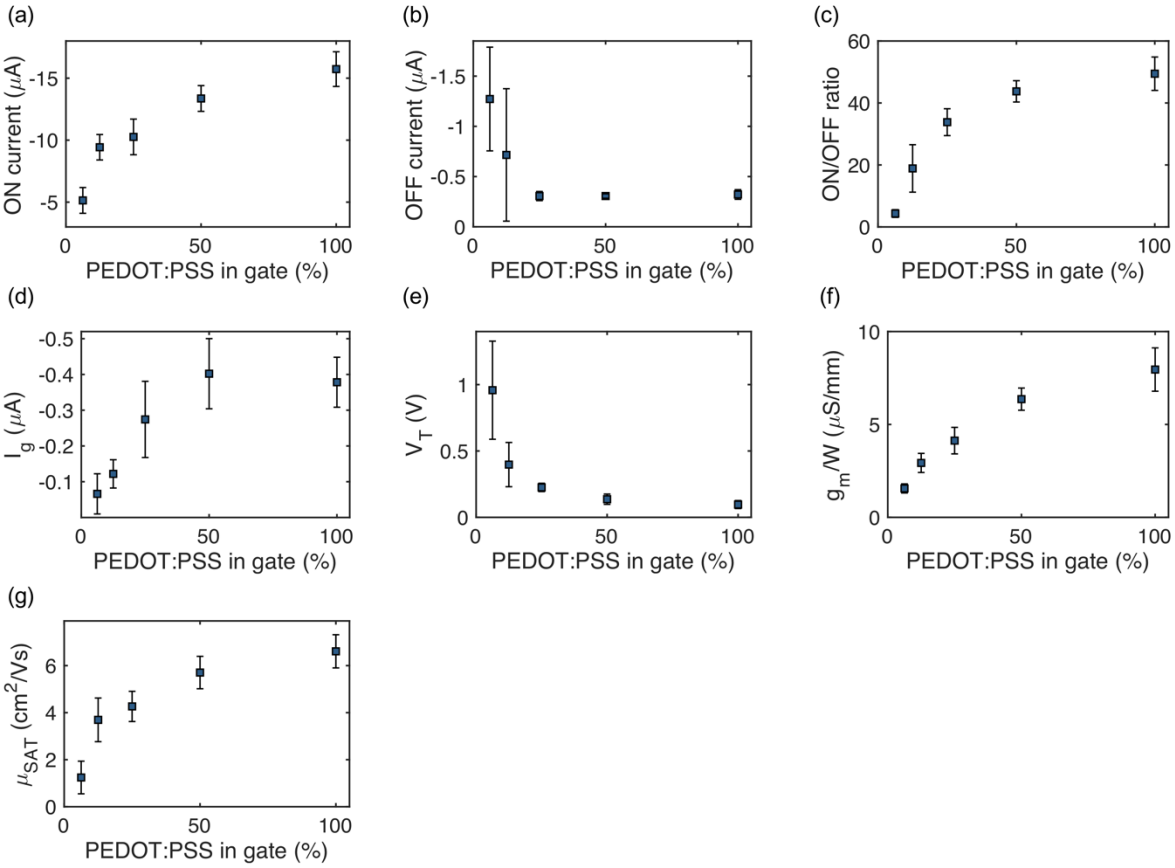

Figure 4. Plots showing the variation of key figures of merit with the amount of PEDOT:PSS in the gate. Figures of merit shown are the (a) ON current, (b) OFF current, (c) ON/OFF ratio, (d) gate current at V_g = -1 V and V_{ds} = -1 V, (e) threshold voltage, (f) transconductance, and (g) apparent saturation mobility.

2.3. Figures of Merit

2.3.1. Device currents

Reduced gate conductance has the effect of reducing the ON current (defined as the maximum I_{ds} in the transfer sweep), in addition to increasing the OFF current (minimum current) when very poorly conducting. These trends are evident in the output and transfer curves (Figure 3), and clearly illustrated in Figure 4a and b, where average ON and OFF currents are plotted with respect to the relative amount of PEDOT:PSS in the gate. As a result, the ON/OFF ratio increases significantly with gate conductance (Figure 4c). Overall, this reflects an increasing

ability of the applied gate voltage to induce ion movement in the dielectric, causing charge accumulation in the channel and hence controlling the drain-source current.

In ideal OFET operation, current does not flow across the dielectric, so the gate conductance is not expected to be relevant to overall device performance.[23] HIFETs, by contrast, exhibit relatively large gate-source currents (see Figure 4d, Figure S6 and S7). The gate current reflects a combination of electronic leakage through the dielectric and the flow of charge into and out from of the gate in response to the movement of ions within the dielectric layer, corresponding to doping ($-I_g$) or de-doping ($+I_g$) of the semiconductor.[17] Whether the behavior of ions at the gate/dielectric boundary is purely capacitive, with the formation of a double layer, or involves some faradaic behavior with oxidation/reduction of the PEDOT:PSS, is unclear to us and awaits further study. We note that HIFETs have been demonstrated using a gold gate electrode, suggesting that redox behavior at the gate is not essential to the fundamental HIFET working mechanism. Moreover, we suppose the thick, dry PEDOT:PSS film to be largely inaccessible to ions, except for the immediate boundary, unlike solvent swelled PEDOT:PSS in the presence of a liquid electrolyte.

A consequence of the presence of a significant gate current is that the voltage in the gate is subject to Ohm's Law and there will be a progressive reduction of the voltage along the length of the gate, dependent on its resistance. Voltage to the gate is generally applied to the ITO pad at one end of the gate (see Figure 1b), and the gate extends for several millimeters perpendicularly to the transistor channel and thus in parallel with its width. Transistor operation is driven by the voltage difference between the channel and the gate at any given point. If the effective gate voltage above the channel is lower than the applied gate voltage, this will result in weaker-than-expected electric fields and hence poorer current modulation overall. To examine this effect theoretically, we modified the gradual channel approximation that has been widely used to model field effect transistors by incorporating a linearly reducing gate voltage

over the width of the channel, in accordance with Ohm's Law. Equation 1 is the standard gradual channel equation for the saturation current and Equation 2 is the modified equation.

$$I_{ds}^{sat} = \frac{W}{2L}\mu C_i\left(V_g - V_T\right)^2 \quad (1)$$

$$I_{ds}^{sat} = \frac{W}{2L}\mu C_i\left[\left(V_g - V_T\right)^2 - \left(V_g - V_T\right)\beta W + \frac{1}{3}\beta^2 W^2\right] \quad (2)$$

In these equations, W and L are the width and length of the transistor channel, respectively, μ is mobility, C_i is the geometrical capacitance of the dielectric, V_g is the applied gate voltage, V_T is the threshold voltage and β is a parameter encapsulating factors affecting the gate resistance (see supporting information for details). **Figure 5**a-d shows simulated output characteristics for both the standard and modified gradual channel approximation. It was assumed that the gate current is constant and flows across the full length of the gate. Adding the reducing gate potential has the primary effect of reducing the magnitude of I_{ds}. **Figure 6** shows how the simulated saturation current, the ON current for these devices, varies with gate conductance. As the conductance increases, the current approaches the 'ideal' saturation current obtained with the standard gradual channel approximation. This trend is very similar to the experimental data for ON current in Figure 4a.

The hypothesis that effective gate voltage is changing with gate conductance also accounts for the observations of gate current (Figure 4d). Experimentally, the negative gate current at $V_g = V_{ds} = -1$ V increases in magnitude with gate conductance (Figure 4d). If the effective gate voltage increases, more cations will be drawn toward the gate, producing a capacitive current as negative charge flows into the gate to compensate accumulating cations. Additionally, the leakage current from gate to drain will be decreasing. This current is positive while the electric field between gate and drain points toward the drain.

Based on the success of our model in explaining the observed trends, we propose that a voltage drop across the gate is the primary factor in the variation of device performance with gate conductance. An alternative explanation that may be considered is that the device performance is related to the changing capacitance of the gate with thickness. In OECTs, PEDOT:PSS capacitance is understood to exhibit linear dependence on volume, due to ion penetration throughout the volume of the film.[24] However, the PEDOT:PSS film in a HIFET differs from those in OECTs in that it is dry (except for ambient humidity) and much thicker (typically several micrometers). We, therefore, expect limited electrochemical activity within the volume of the film, and hence that capacitance would not scale significantly with thickness. HIFETs employed for sensing with aqueous analytes, however, will likely exhibit significant activity in the gate.

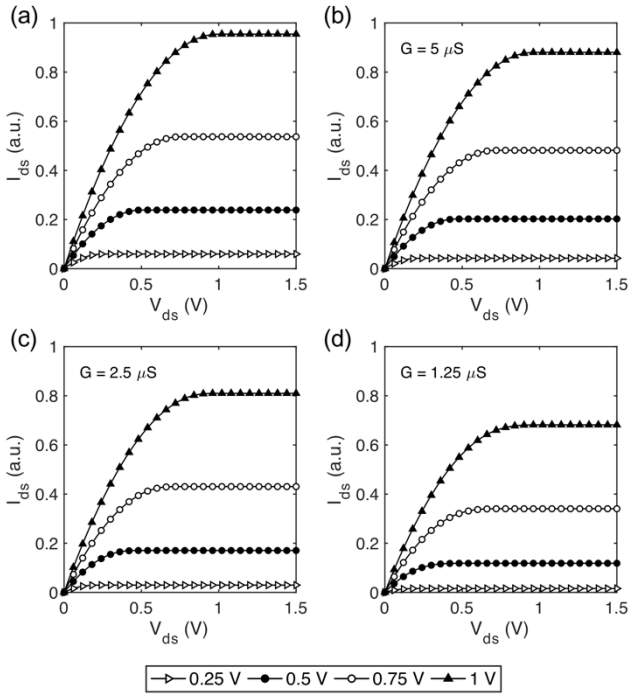

Figure 5. Simulated output curves, using (a) the standard gradual channel approximation, (b,c,d) modified gradual channel approximation with decreasing gate conductance (*G*), corresponding to increased *β*.

2.3.2. Threshold Voltage

In addition to device currents, threshold voltage, V_T, is another key transistor figure of merit, intended to characterize the minimum gate voltage at which mobile charge carriers begin to accumulate in the semiconductor. We estimated V_T by the conventional method,[25] though it is recognized that nonideal behavior in OTFTs can lead to ambiguities and errors in the extraction of V_T.[26] For our purposes, we are only concerned with general trends, rather than accurate measurements of a physically-significant threshold voltage (see supporting information for details, Figure S4).

Though HIFETs require a negative gate voltage to accumulate mobile charge carriers in the channel, the threshold voltage is a small positive value. In their proposed mechanism, Bäcklund et al.[18] posit that the polarity of the PVP phenyl groups induces a small accumulation of charge in the P3HT, meaning the device is slightly 'on' in the absence of a gate potential. Applying a positive gate potential relative to the channel causes mobile positive ions to drift toward the P3HT and can compensate the negative poles of the phenyl groups to turn the device 'off', giving us a positive threshold voltage. In Figure 4e, we clearly observe that threshold voltage decreases (approaches zero) with increasing gate conductance. Like ON current, this result appears to reflect an increase in the effective gate voltage, where a smaller applied voltage is required to achieve the same effect.

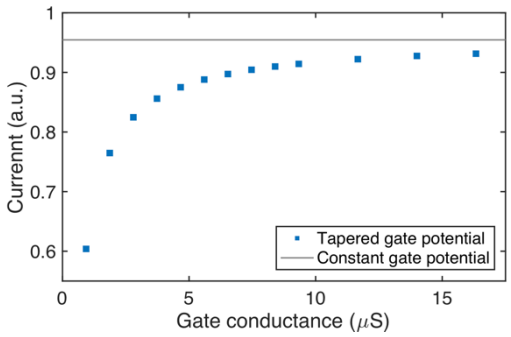

Figure 6. Simulated saturation current I_{sat} at V_g = −1V for the modified gradual channel approximation with gate conductance. Grey line shows the result for the standard gradual channel approximation.

2.3.3. Transconductance

Changing gate conductance likewise has a significant impact on the transconductance of the HIFET. Transconductance, defined as the derivative of the transfer curve ($g_m = \delta I_{ds}/\delta V_g$), characterizes a fundamental property of transistor: its ability to modulate and amplify an input signal. Figure 4f plots the average maximum transconductance, scaled with respect to the width of the transistor channel. With greater gate conductance, a given change in applied gate voltage is able to produce a greater change in I_{ds}. In output plots, this is manifest in the separations between output curves measured at different gate voltages (see Figure 3).

2.3.4. Apparent Field Effect Mobility

To observe the change in field effect charge carrier mobility with change in gate conductance, we estimated saturation mobility using conventional equations developed for field effect transistors.[27] In HIFETs, current modulation occurs via ionic doping rather than a conventional field effect, so estimated mobility should be taken as an 'apparent mobility', rather than a direct indicator of true charge carrier mobility in the P3HT film. Nevertheless, we regard this parameter as a valuable means to compare overall device performances. Figure 4g illustrates the increase in the apparent saturation mobility with gate conductance. This effect, again, can be explained in terms of a voltage drop across the gate that depends on its conductance. As the effective gate voltage approaches the applied gate voltage, this results in greater ionic doping of the semiconductor, increasing channel conductivity for a given applied gate voltage. As this reflects the same phenomenon that we suggest is responsible for the change in ON currents and transconductance, the apparent mobility follows a similar trend. Indeed, using the modified gradual channel model (Equation 2) to calculate the saturation current, then calculating the mobility using the unmodified equation (Equation 1), reproduces the same variation in extracted mobility with gate conductance as is observed experimentally. Similar to organic electrochemical transistors (OECTs) and electrolyte-gated OFETs (EGOFETs),[12] the ionic

doping of the channel in HIFETs can result in greater charge accumulation than a standard field effect, hence the low operating voltages and high currents compared to many conventional OFETs. Previous reports indicate that the apparent mobility is larger in HIFETs for a given channel conductivity than in comparable OFETs.[11] We have demonstrated here that ensuring good gate conductance is important to maximizing this inherent advantage.

It is worth noting that the value of each figure of merit begins to plateau as the amount of PEDOT:PSS in the gate approaches 100%. The 3×3 mm 100% PEDOT:PSS films exhibited a conductance of ≈ 7 μS (Figure 2), corresponding to a material conductivity of ≈ 0.7 Sm^{-1}. A HIFET using a high conductivity grade PEDOT:PSS gate (conductance ≈ 400 μS, conductivity ≈ 40 Sm^{-1}) yielded no improvement over the 100% gate of the lower conductivity PEDOT:PSS (see Figure S8 and Table S2). Indeed, the standard PEDOT:PSS generally performed slightly better. Thus, there appears to be no advantage in seeking further improvements to gate conductance in this case, where any voltage reduction across the gate would have a negligible effect. This is supported by our modified gradual channel model, which predicts a rapid initial increase in transistor performance, after which it begins to level out and closely approaches the 'ideal' case where there is no voltage loss across the gate (see Figure 6).

3. Conclusion

To summarize, we have characterized the performance of hygroscopic insulator OTFTs with varied gate conductance. Increasing conductance improves key performance parameters, including drain-source current, ON/OFF ratio, transconductance, and apparent carrier mobility. We have shown that this can be explained by an increase in effective gate voltage, approaching the applied gate voltage with greater gate conductance. The effective voltage is significantly lower than the applied voltage in low-conductance gates when a leakage current is present. We additionally observe that further performance gains become negligible once a certain moderate conductance is achieved. This latter observation has positive implications for the optimization

of HIFET-based and other OTFT-based sensors where the gate composition is modified to incorporate sensing functionality. Only a moderately conducting electrode is necessary, thus allowing for the incorporation of additional, poorly conducting materials to facilitate interaction with the analyte. In HIFET based sensors, the difference in capacitance in different gate electrodes when an analyte gets in contact with the gate will play a role in the performance, and therefore will be investigated in future research in our group.

4. Experimental Section

The glass substrates were purchased pre-patterned with indium tin oxide (ITO) source and drain electrodes, and a separate gate contact pad (Xin Yan Technology LTD.). Substrates were cleaned with acetone and Alconox, then ultrasonicated in a sequence of water, acetone and isopropanol, for 10 minutes each, drying with compressed air between each treatment. A 60 nm film of regioregular P3HT (Rieke Metals, LLC, RMI-001EE) was spin coated from a 13 mg/mL solution in chloroform and chlorobenzene (1:1) at 3000 rpm for 30 seconds. The film was annealed at 60°C for 10 minutes. The PVP dielectric (Sigma-Aldrich, 436224) was spin coated from an 80 mg/mL solution in ethanol at 2000 rpm for 60 seconds and annealed at 85°C for 10 minutes, producing an 800 nm film. Gate electrodes (2×8 mm) were drop cast in place over the channel and connected to the ITO gate contact pad adjacent to the device (see Figure 1b).

Gate conductance was varied by progressively diluting a stock dispersion of PEDOT:PSS (Heraeus, CLEVIOS P VP AI 4083) with deionized water. 10 µL of PEDOT:PSS dispersion was used for each gate, and left to dry under ambient conditions. For the high conductivity gate, high conductivity grade PEDOT:PSS (Sigma-Aldrich, 739332) was used. To measure IV characteristics, the same gate solutions were deposited across two ITO contacts (3×3 mm area between contacts).

HIFETs were characterized immediately following fabrication. Output and transfer characteristics were recorded using a Keysight B1500A semiconductor analyzer. IV curves for the different gates were measured with the same setup.

Supporting Information
Supporting Information is available from the Wiley Online Library or from the author.

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Supporting Information

Effect of Gate Conductance on Hygroscopic Insulator Organic Field Effect Transistors

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Gate conductance

PEDOT:PSS films of area 3×3 mm^2 were prepared using different concentrations of PEDOT:PSS. Conductance (G = I/V) was calculated using the slope of trend lines fitted to the IV curves.

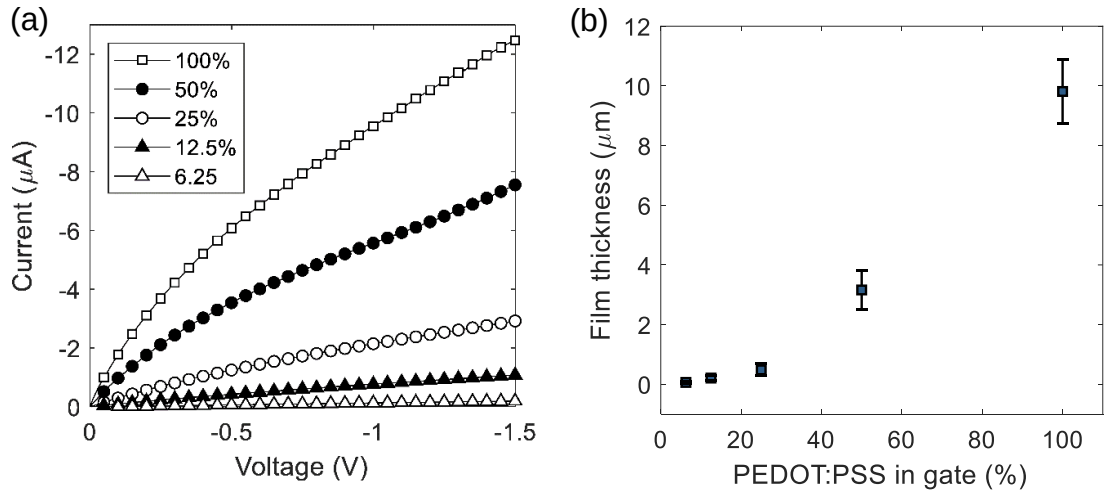
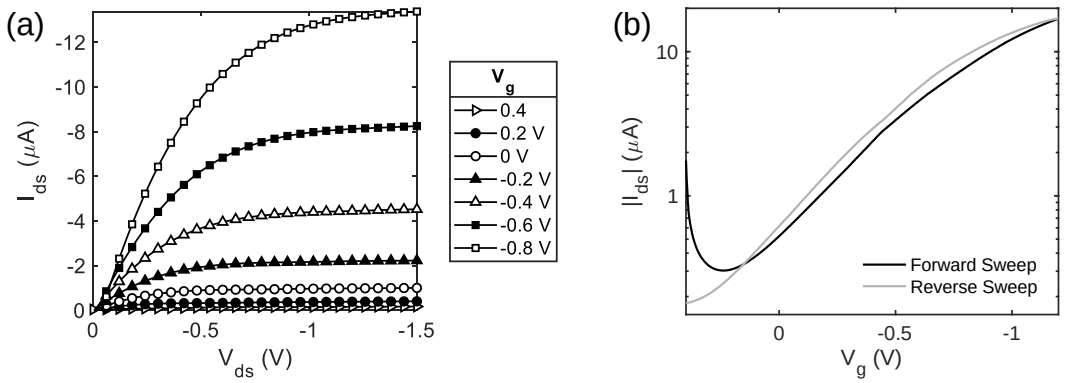


Figure S1: (a) Current-voltage relationship for PEDOT:PSS films deposited from dispersions of varied concentration. **(b)** Plot showing the relationship between thickness of PEDOT:PSS films and the concentration of PEDOT:PSS, expressed as a percentage of the stock solution. Film thickness is measured by stylus profilometry.

Output and transfer characteristics



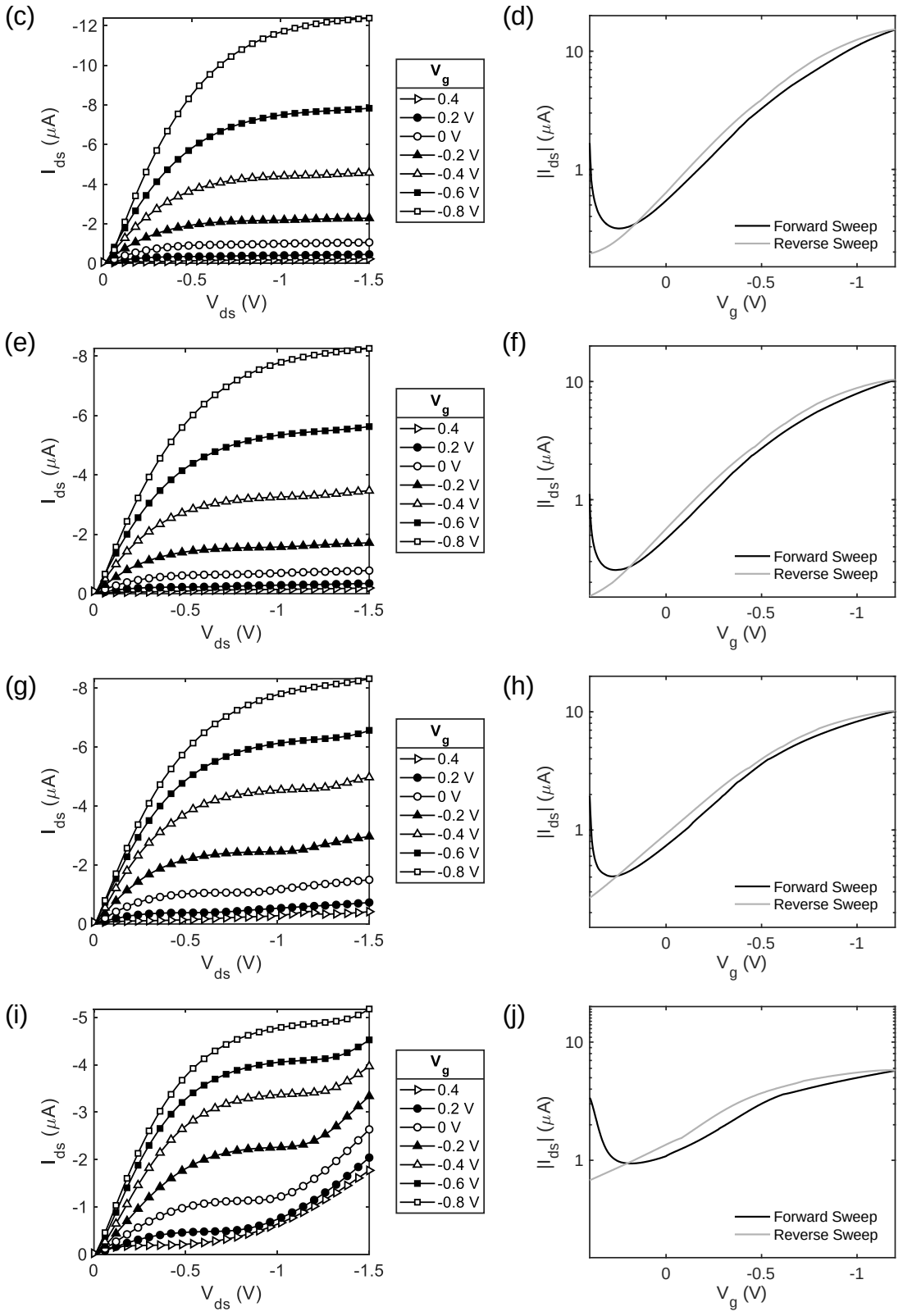


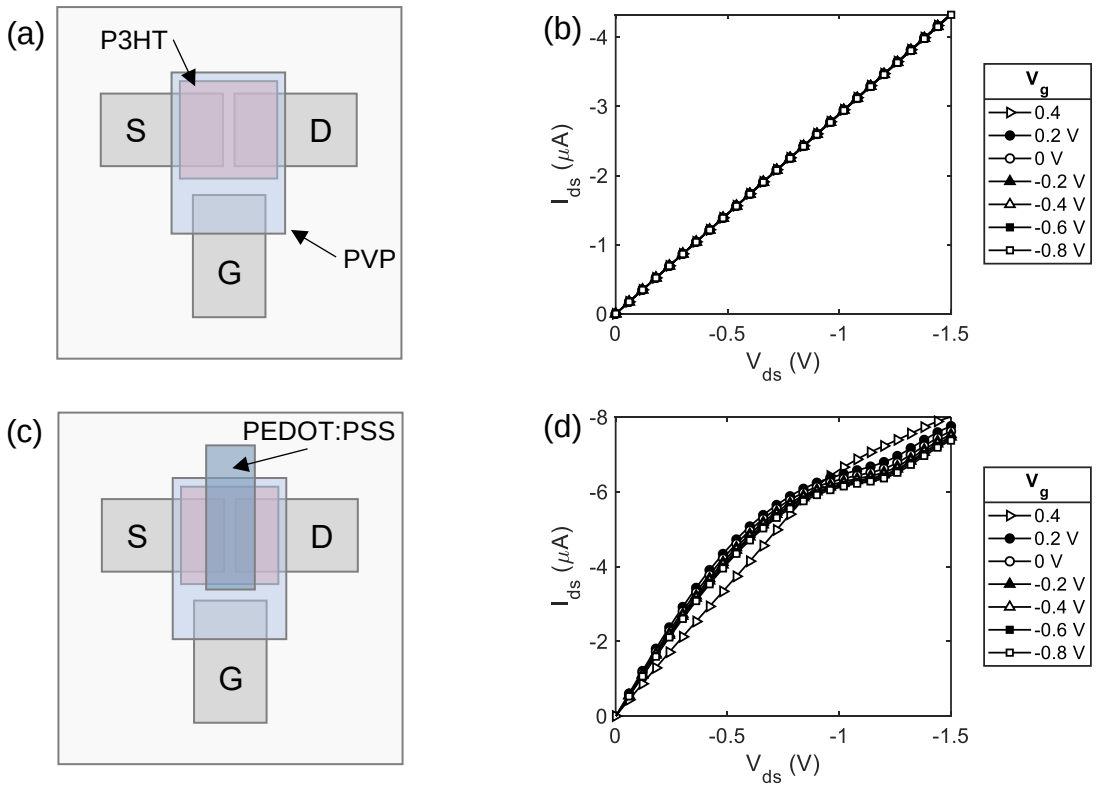
Figure S2: Output and transfer plots for HIFETs gated by PEDOT:PSS films deposited from (a,b) 100%, (c,d) 50%, (e,f) 25%, (g,h) 12.5% and (i, j) 6.25% dispersions. Examples shown here are the devices with each gate type that exhibited the best ON/OFF ratio.

Offset gate test

Devices were fabricated to test whether the offset ITO gate contact pad could be acting as an 'offset gate' when gate conductance is low that could be distorting the saturation regime. One set of devices was fabricated without the usual PEDOT:PSS gate electrode, and instead the PVP dielectric layer was extended to make contact with the ITO gate contact (**Figure S3a**). In this configuration, this would give the ITO pad the best chance to act as a gate for the transistor. **Figure S5b** shows the output curve. No modulations were observed.

When a PEDOT:PSS film is added to the device, but not connected to the ITO pad (**Figure S3c**), the output characteristics change (**Figure S3d**). The gate voltage still fails to modulate the current, indicating no significant gating effect from the ITO gate, but there is now a small saturation effect. This is possibly due to increased moisturisation of the PVP layer due to the deposition of the PEDOT:PSS. Mobilised positive ions in the PVP would be drawn by the negative drain voltage and begin to de-dope the channel, causing pinch off to occur.

When the voltage is applied to the PEDOT:PSS film rather than the ITO pad (**Figure S3e**), current modulations are seen as normal (**Figure S3f**). Device performance is worse than when the ITO pad is used as an intermediary between the voltage probe and the PEDOT:PSS (the standard case), justifying our use of the ITO to improve electrical contact between the two.



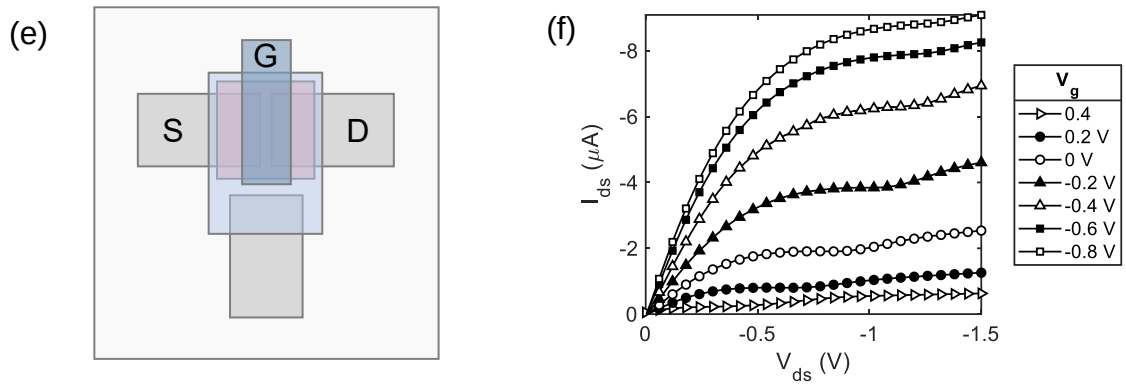


Figure S3: Top views of device structures and output plots for modified HIFET devices. (a,b) ITO connected to PVP and used as gate, no PEDOT:PSS. (c,d) ITO connected to PVP and used as gate, while PEDOT:PSS is present as a non-active layer. (e,f) Same device as (c) but PEDOT:PSS is used as gate and ITO is non-active.

Extraction of figures of merit

Figures of merit were extracted from transfer curves (measured in the saturation regime, V_{ds} = -1 V) using standard methods (see Table S1 below).

Table S1: Tabulation of methods of extracting transistor figures of merit.

Figure of merit	**Method of extraction**
ON current	Maximum current in transfer sweep: (I_{ds} when V_{ds} = -1 V and V_g = -1.2 V)
OFF current	Minimum current in transfer sweep
ON/OFF ratio	Ratio of ON to OFF current
Gate current (I_g)	Gate current recorded during transfer sweep when V_{ds} = -1 V and V_g = -1 V
Threshold voltage (V_T)	The point of intersection with the gate voltage axis of a straight line extrapolated from the plot of $\sqrt{I_{ds}}$ with V_g This method is derived from the gradual channel approximation for field effect transistors that describes the saturation current as follows:[1] $$I_{ds} = \frac{W}{2L}\mu_{sat}C_i(V_g - V_T)^2$$ We extracted V_T by choosing a region of the $\sqrt{I_{ds}}$ vs. V_g curve, fitting a trend line to that region, and extracting the x-axis intercept from the fitted equation. For consistency, lines were chosen to best fit the most linear region of our $\sqrt{I_{ds}}$ vs. V_g plot, occurring around V_g = -0.5 V in most cases (see Figure S4 below).

Transconductance (g_m)	Transconductance is the derivative of the transfer curve ($\partial I_{ds}/\partial V_g$). We achieve this by fitting a polynomial to the transfer curve, taking the derivative and extracting the maximum. See Figure S5.
Apparent saturation mobility	Field effect saturation mobility is calculated using the standard equation:[2] $$\mu_{sat} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{ds}}}{\partial V_g}\right)^2$$ Where, L and W are the channel length and width and C_i is the capacitance per unit area of the dielectric. The value for $\frac{\partial\sqrt{I_{ds}}}{\partial V_g}$ is estimated by finding the gradient of the straight line fitted to the plot of $\sqrt{I_{ds}}$ with V_g, used to determine the threshold voltage. For C_i, we used 4.3 nF/cm^2, a measurement of a dry PVP film from [3], though this value will vary depending on the ambient humidity (change of 20-40%) and the PVP thickness. Since we experimented under normal laboratory conditions (low humidity) and used a similar PVP thickness, we use the cited value as a reasonable approximation.

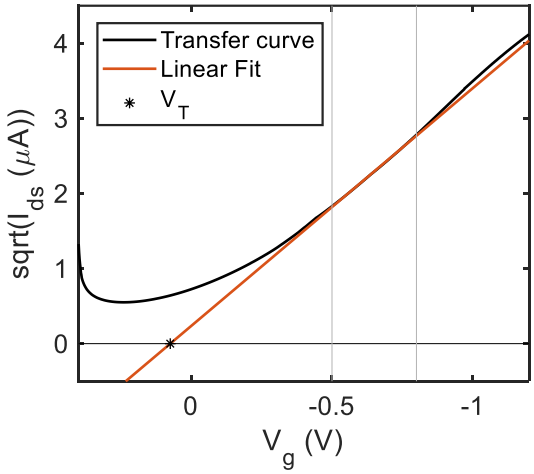


Figure S4: Figure showing the extraction of the threshold voltage for a standard HIFET (100% PEDOT:PSS gate). The square root of I_{ds} is plotted with V_g and a straight line is fitted to the region enclosed by the vertical grey lines, which is approximately linear. The threshold voltage is the point at which the fitted line crosses the x-axis.

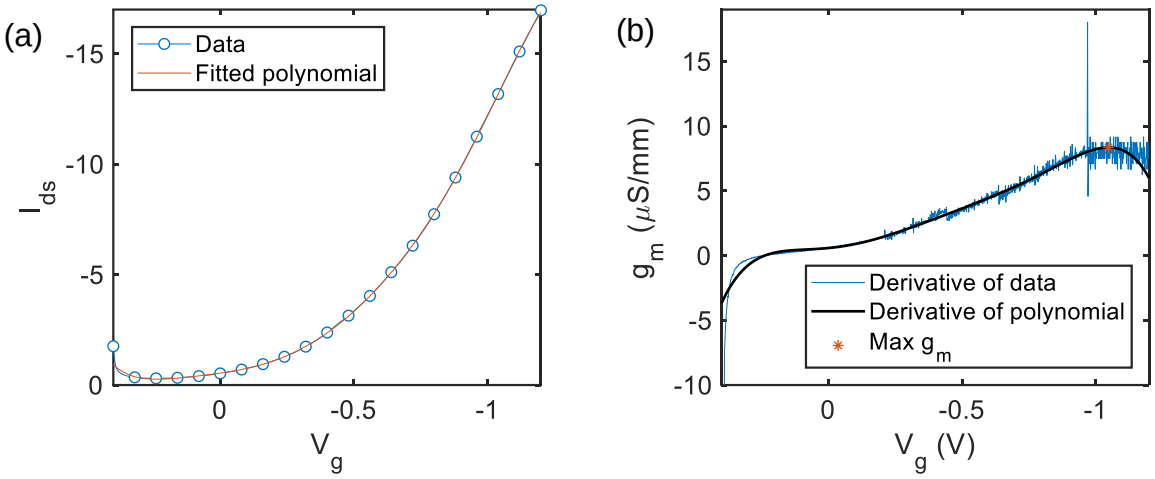


Figure S5: Figures showing the extraction of the transconductance for a standard HIFET (100% PEDOT:PSS gate). (a) The transfer curve is plotted and a polynomial is fitted. (b) The first derivative of the fitted polynomial is plotted alongside an approximate derivative of the measured data set. The polynomial follows the data reasonably well, but without the noise. The maximum transconductance is extracted from the derived polynomial.

Gate current

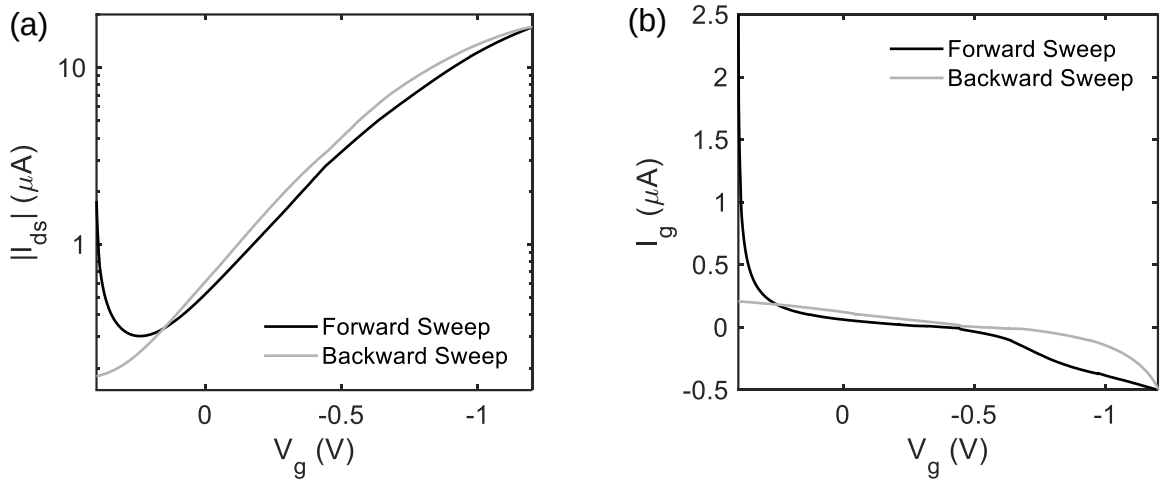


Figure S6: Figures plotting (a) transfer characteristics, and (b) gate current, measured simultaneously (at V_{ds} = -1V) for a standard HIFET (100% PEDOT:PSS gate). Gate current changes dynamically with gate voltage.

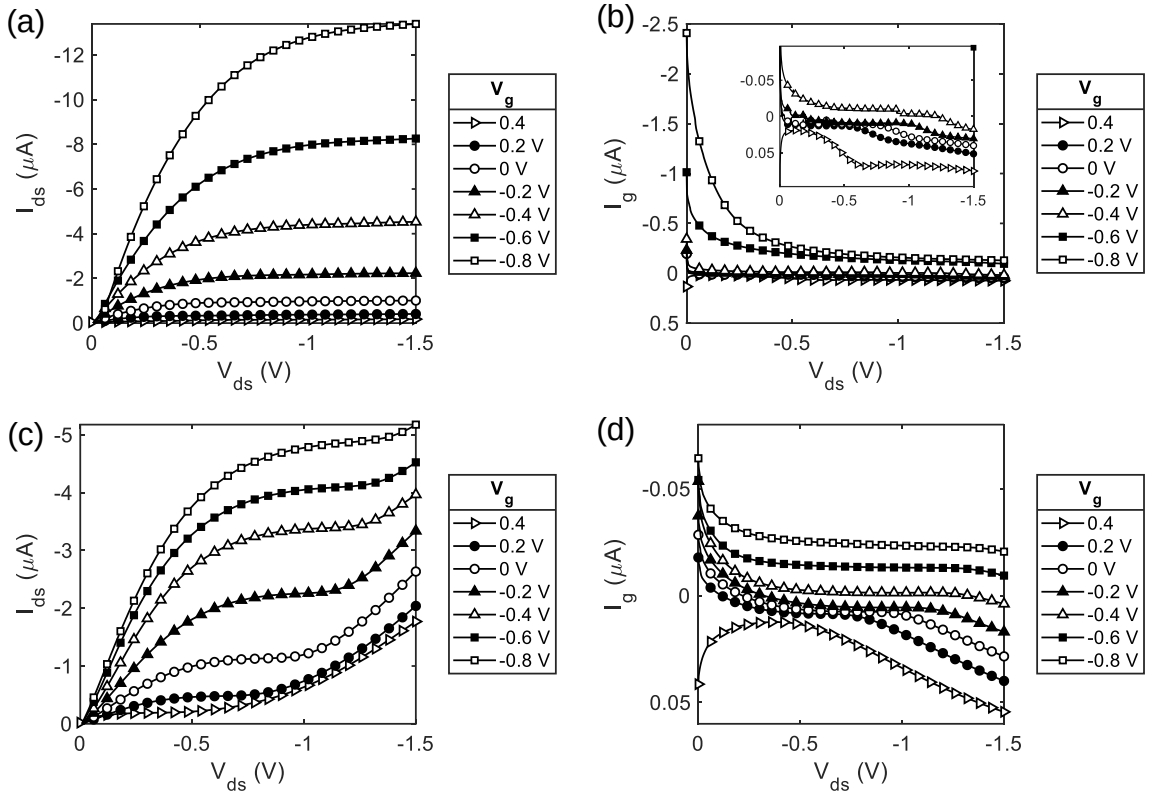


Figure S7: Figures plotting output characteristics, and gate current, measured simultaneously for, (a,b) a standard HIFET (100% PEDOT:PSS gate) and (c,d) a HIFET with a poorly conducting gate (6.25% PEDOT:PSS). Gate current changes dynamically with drain-source voltage.

High conductivity PEDOT:PSS gate

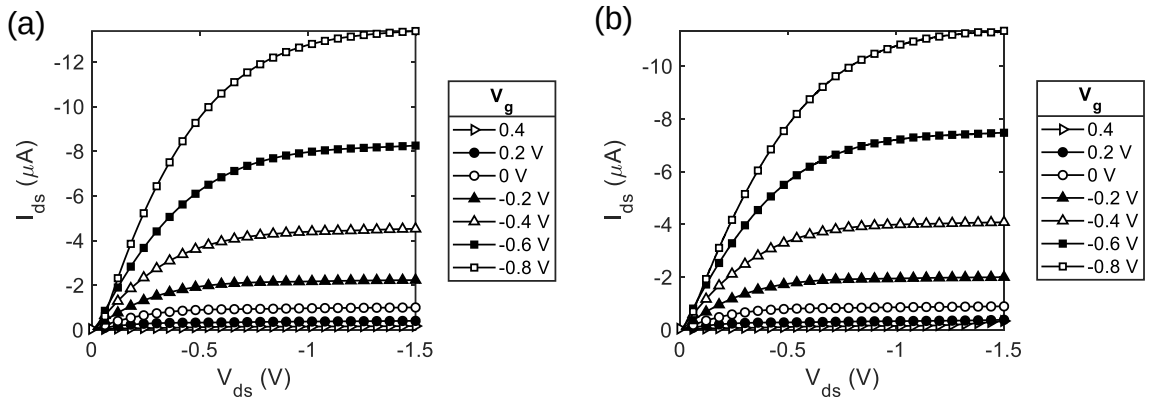


Figure S8: Output curves for HIFETs with (a) standard 100% PEDOT:PSS gate, and (b) high conductivity grade 100% PEDOT:PSS gate.

Table S2: Comparison of figures of merit for best-performing HIFET with standard PEDOT:PSS gate and the best-performing HIFET with a high conductivity grade PEDOT:PSS gate.

Figure of Merit	Standard PEDOT:PSS	High conductivity PEDOT:PSS
ON current	16.96 μA	14.05 μA
OFF current	0.30 μA	0.28 μA
ON/OFF ratio	55.98	50.35
V_T	0.09 V	0.18 V
g_m/W	8.35 μS/mm	5.46 μS/mm
μ_{sat}	7.47 cm^2/Vs	5.86 cm^2/Vs

Gradual channel approximation with tapered gate potential

To model the effect of a tapered gate potential, we have modified the standard gradual channel approximation that describes the operation of an idealised field effect transistor. We replaced the term V_g with an effective gate voltage, V_g^{eff}. We model the gate resistance using Ohm's law; the voltage drop at a location along the gate, y, is the product of the gate current, I_g, and the resistance, R, of that section of the gate. The resistance will vary linearly with the length of that gate section:

$$R_g = \frac{\rho}{t_g w_g} y$$

Where ρ is the gate resistivity, y is the length of the gate section, t_g is the gate thickness and w_g is the gate width. Thus, the effective gate voltage is the following:

$$V_g^{eff} = V_g - I_g R_g = V_g - \frac{I_g \rho}{t_g w_g} y = V_g - \beta y$$

We simplify the gate parameters using the term, β.
In the gradual channel approximation, the mobile charge density per unit area of the channel is:

$$Q_{mob} = C_i \left(V_g^{eff} - V_T - V(x) \right)$$

Where, C_i is the gate insulator capacitance, V_T is the threshold voltage and $V(x)$ is the channel voltage at position x, which varies between 0 at the source electrode ($x = 0$) and V_{ds} at the drain ($x = L$). In this model, we assign x to the direction along the length of the channel between the electrodes, and y is the direction of the channel width (Figure S9). The gate electrode extends along the channel width. For the sake of simplicity, we assume the gate begins at $y = 0$, and that the full V_g is applied here.

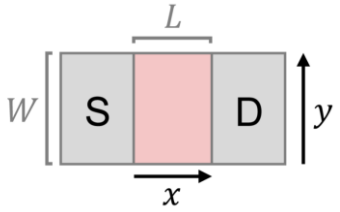


Figure S9: Top view of modelled transistor channel of length L and width W.
We begin with the equation for the current along the full length of the channel, for a given position, y. This is identical to the standard gradual channel equation, with channel width dy:

$$dI_{ds} = \frac{dy}{L}\mu C_i\left[(V_g^{eff} - V_T)V_{ds} - \frac{1}{2}V_{ds}^2\right]$$

To calculate the full I_{ds} for the channel, we must integrate over y. How we do this will depend on the operating regime.

Non-saturation regime

Saturation will occurs in the channel wherever $V_{ds} \geq V_g - \beta y - V_T$. The channel will be fully unsaturated when the minimum value of $V_g - \beta y\ - V_T$ (substitute $y = W$) is less greater than V_{ds}.

So, for:

$$V_{ds} < V_g - \beta W\ - V_T$$

The following equation describes the drain-source current:

$$I_{ds} = \int_{y=0}^{y=W} \frac{\mu C_i}{L}\left[(V_g - \beta y - V_T)V_{ds} - \frac{1}{2}V_{ds}^2\right] dy$$
$$= \frac{W}{L}\mu C_i\left[\left(V_g - V_T - \frac{1}{2}\beta W\right)V_{ds} - \frac{1}{2}V_{ds}^2\right]$$

Mixed regime

Because of the tapered gate potential, there will be a regime where pinch-off occurs in only part of the channel. This will occur when:

$$V_g - \beta W - V_T \leq V_{ds} < V_g - V_T$$

The boundary between these regions of the channel will be when:

$$y_{sat} = \frac{V_g - V_T - V_{ds}}{\beta}$$

Thus, we must integrate over two regions: up to y_{sat} and then from y_{sat} to W. In the latter region, we substitute $V_{ds} = V_g - \beta y - V_T$.

$$I_{ds} = \int_{y=0}^{y=y_{sat}} \frac{\mu C_i}{L}\left[(V_g - \beta y - V_T)V_{ds} - \frac{1}{2}V_{ds}^2\right] dy + \int_{y=y_{sat}}^{y=W} \frac{\mu C_i}{2L}(V_g - \beta y - V_T)^2 dy$$
$$= \frac{\mu C_i}{L}\left[y_{sat}\left((V_g - V_T)V_{ds} - \frac{1}{2}V_{ds}^2\right) - \frac{\beta y_{sat}^2}{2}V_{ds} + \frac{W}{2}(V_g - V_T)^2\right.$$
$$\left. - \frac{\beta W^2}{2}(V_g - V_T) + \frac{\beta^2 W^3}{6} - \frac{y_{sat}}{2}(V_g - V_T)^2 + \frac{\beta t^2}{2}(V_g - V_T)\right.$$
$$\left. - \frac{\beta^2 t^3}{6}\right]$$
$$= \frac{\mu C_i}{L}\left[y_{sat}\left((V_g - V_T)V_{ds} - \frac{1}{2}V_{ds}^2\right) - \frac{\beta y_{sat}^2}{2}V_{ds} + (V_g - V_T)^2\left(\frac{W}{2} - \frac{y_{sat}}{2}\right)\right.$$
$$\left. + (V_g - V_T)\left(\frac{\beta y_{sat}^2}{2} - \frac{\beta W^2}{2}\right) + \frac{\beta^2 W^3}{6} - \frac{\beta^2 y_{sat}^3}{6}\right]$$

Saturation regime

Finally, the channel is fully saturated when:

$$V_{ds} \geq V_g - V_T$$

In this regime, we substitute $V_{ds} = V_g - \beta y - V_T$, and integrate over the full channel width:

$$I_{ds} = \int_{y=0}^{y=W} \frac{\mu C_i}{2L}(V_g - \beta y - V_T)^2 dy$$
$$I_{ds} = \frac{W}{2L}\mu C_i\left[(V_g - V_T)^2 - (V_g - V_T)\beta W + \frac{1}{3}\beta^2 W^2\right]$$

References

[1] J. Zaumseil, H. Sirringhaus, Chem. Rev. 2007, 107, 1296.
[2] P. Kevin, M. A. Malik, P. O'Brien, J. Cameron, R. G. D. Taylor, N. J. Findlay, A. R. Inigo, P. J. Skabara, J. Mater. Chem. C 2016, 4, 5109.
[3] H. G. O. Sandberg, T. G. Bäcklund, R. Österbacka, H. Stubb, Adv. Mater. 2004, 16, 1112.