Holographic Lithography

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Abstract: This review summarises the work of the Durham-Sheffield, UK team working on Holographic Lithography over the last decade. It collates progress in 3D resolution and overall scale of the substrate wiring patterns designed and considers a range of approaches and applications.

1. Summary

Creating ever finer micro-connections on silicon substrates has been a major thrust in lithographic research over the past 50 years with sub 20nm feature sizes giving rise to hugely complex circuits. There is an increasing need to write comparably fine structures on 3D substrates but this presents significant challenges and, unsurprisingly, feature sizes are lagging behind somewhat. Serial writing using laser beams is a potential way forward. As an alternative, the collaboration between Durham University and Sheffield University, UK over the last decade has made progress with holographic writing where the complete circuit might be made with one exposure, keeping to the 2D mask illumination paradigm. Simply put, we replace the conventional 2D mask with a hologram plate. The hologram is computer generated due to its complexity and the lack of a real object. Attention also needs to be given to the photoresist to prevent the loss of detail when the material might lose resolution by guttering on the 3D internal corners. This review starts with our first masks to project 3D structures and the early point source computations leading on to sub-micron multiple tracks created by iterated holograms. Using the latest liquid crystal modulators the technique is offering a new manufacturing method for 3D chip interconnection. The authors are encouraged by these laboratory results and are looking for the best applications to develop the process further.

Our initial method for accomplishing photolithography on grossly non-planar substrates was to compute an approximation of the diffraction pattern that would produce the desired light-intensity distribution on the substrate to be patterned. As a simple example, the cylindrical Fresnel Zone Plate pattern of the desired track can be created and matched to the distance from the plate. The nearer the track then the finer the zone plate mask pattern. This pattern is then digitised and converted into a format suitable for manufacture by a direct-write method. The resultant computer-generated hologram mask is then used in a custom alignment tool to expose the photoresist-coated substrate. The technique is expected to have many potential applications in the packaging of microelectronics and micro-electromechanical systems [1].

To the electronics industry, photolithography is the primary technique by which patterns are transferred from mask to substrate. The substrates are either semiconductor wafers or printed circuit boards, both of which are nominally flat. The growth of micro-electro-mechanical and micro-electro-opto-mechanical systems (MEMS and MOEMS) and the search for higher-density electronics packaging solutions is leading to the requirement to pattern fine features onto non-planar substrates. Standard photolithographic techniques cannot be used with these surfaces because the unavoidably large gap between mask and substrate incurs diffractive line broadening, with a consequent loss of resolution. We demonstrated a method for realising photolithography on non-planar substrates using computer-generated holographic (CGH) masks. The technique described enables photolithography to be realised in three dimensions [2].

To address the issue of fine-line interconnections over non-planar surfaces, we introduced the idea of using CGH masks for more challenging geometries. The patterning of electrical interconnections onto the piezo-electric actuators of an ink-jet print head was the starting point. Uniform coverage of the substrate was achieved using an electro-depositable photoresist with the required pattern transferred using a custom-designed chrome-on-glass mask using a standard mask aligner. We found that large arrays of 140 µm-pitch electrical interconnections could be successfully deposited onto 500µm-high piezo-electric actuators. It was necessary to modify the shapes of the line segments on the mask in order to compensate for diffractive line broadening. For more extreme 3D geometries it is necessary to consider the use of holographic masks [3].

The CGH are derived from analytical expressions and encode both amplitude and phase information. We illustrate the performance with a 100μm line exposed onto a substrate in the form of a plane/slope/plane, in which the change in depth is 40mm. Enhancements to the line shape are discussed that make the technique more robust to manufacturing process variations. The fact that features in the range 10-100μm can be imaged at large distance whilst coping with significant changes of depth shows that the technique has great potential in the microelectronics packaging industry [4]. This photolithographic process using digital holograms enables the fine-pitch patterning of grossly non-planar substrates. Considerations of hologram design, fabrication and verification particular to the lithographic process are discussed in [5].

In [6] we reported on a real 3D antenna device that had been fabricated by our methods and tested for the first time. We demonstrated the direct photolithographic patterning of a non-planar substrate by creating 62 micron helical tracks on a 22 mm high cone. The projection of focused light on to the three dimensional surface was achieved using a CGH suitably illuminated so as to create the required pattern on the photoresist coated surface. We addressed the key challenges encountered for the implementation of holographic photolithography in three dimensions, including mask design, manufacture and alignment, exposure compensation and chemical processing. Control of line width and resolution over the non-planar surface is critical and non-trivial but is possible. We described the methods adopted and critically assess the structures created by this process. The bi-helical cone is representative of a broadband, high frequency coil like structure, known in wireless communications as a log-periodic antenna. Our findings were disclosed in a series of patent applications from August 2004 onwards. They cover in turn "Holographic Lithography using geometrical shapes", "Sub-micron 3D Holographic Lithography" and "Improvements in or relating to Holography" using iteratively designed CGH. [7, 8 & 13].

We then turned our attention to patterning controlled-width tracks onto anisotropically micromachined silicon. Experimental and simulation results were presented using 3D holographic photolithography which significantly reduces the problem normally present in patterning non-planar surfaces. A negative-acting electrodepositable photoresist (InterVia 3D-N) was used in the study. Its deposition onto the 3D substrate is optimised by modification of the coating temperature, thickness and of pre-exposure bake conditions. We showed the successful patterning of a constant-width 8 μm line down the sloping sidewall of a 500 μm thick silicon wafer. This is beyond the conventional resolution limit and indicates the potential of the technique for realising high-density 3rd dimension routing in electronic packages [9].

An important step was taken when we applied an iterative algorithm for hologram design with multiple output image planes arranged in close proximity to create continuous patterns within an imaging volume. These holograms have been designed for photolithography on 3D surfaces and computed to be projected from addressable spatial light modulators. The influence of simulated image plane separation on the final image and its suitability for lithography, was assessed. Results were presented and the most suitable case was demonstrated experimentally. Essentially the process allows the computation of the CGH for an arbitrary 3D pattern [10].

Using this versatility, we described patterning multiple 10 μm wide conductive tracks down the vertical sidewall of a 500 μm thick silicon die. An optical technique was modified, to use a CGH mask in conjunction with a diffraction grating. 3D holographic photolithography has been demonstrated as a powerful method for eliminating the troublesome diffractive line broadening that is usually encountered when patterning non-planar substrates. When used in conjunction with a grating, it creates the possibility to pattern fine features onto vertical surfaces, perpendicular to the mask, an achievement outside the normal realm of photolithography [11] & Fig 1.

Nearly all antenna structures fabricated for high volume markets are confined, where possible, to essentially planar geometries. This is driven by the need to minimise fabrication and packaging costs. For certain applications considerable performance gains can however be achieved by utilising the third dimension. A well-known example is the helical spiral structure, which has been manufactured for high-performance GPS receivers Helical antennas can be constructed by scanning a laser beam across a rotating substrate or alternatively with our 3D method using a single exposure, regaining the potential for mass-production [12].

More recently we have described the fabrication of an electrically-small antenna and its subsequent characterisation. The patterning of meander lines conformed onto a hemispherical substrate was achieved by iterative holographic lithography, which used time-division multiplexing of a series of iteratively optimised computer-generated holograms. The meander lines had a line width of 100 μm and line separation of 400 μm, with a line pitch of 500 μm and a total meander length of 145 mm. The working frequency was found to be 2.06 GHz, with an efficiency of 46%. This work demonstrates a new method for the fabrication of 3D conformal antennas and the state of the art at present [14] and Fig 2.

In conclusion; the techniques described above offer an attractive new toolset for the continued use of photolithography in crafting silicon structures to manufacture complex circuits using light. The advantage of speed offered by single exposure illumination for 2D manufacture now extends to 3D chip production which should be

appealing if the volume of items to be manufactured is large. New spatial light modulators are enabling smaller pitched diffraction over larger areas and the computing power needed to calculate the CGH is tractable even for relatively complex circuits given the optical algorithms developed. Fixed physical masks provide even better resolution with photo-reduction methods allowing sub-micron vertical tracks to be created. The key question seems to be "where can the process be exploited best"? Here we speculate on potential road blocks to steer a path forward. Is it because through hole silicon via technology is always competitive, though its reliability, cost and loss of silicon area are negatives? Is a new silicon process requiring advanced optics and very fine alignment still too risky to deploy in anything other than a research tool? Or, is the stated need for mass manufacture of "systems on a chip" not great enough to trigger the new manufacturing paradigm yet?

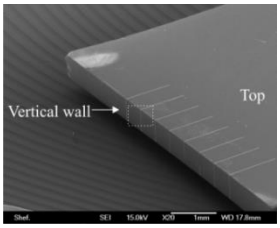

Fig. 1. Our process allows patterning of fine features onto vertical surfaces beyond the normal realm of photolithography [11].

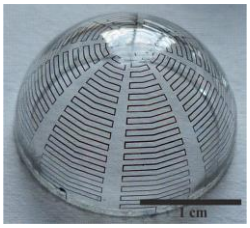

Fig.2 Electrically-small antenna on hemispherical substrate manufactured using holographic photolithography [14].

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