Identification of Slow States at the SiO_2/SiC Interface Through Sub-Bandgap Illumination

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Abstract. We show that it is possible to obtain information relating to deep level interface traps, or so called 'slow states', by using the photo-CV characterisation method. Sub-bandgap illumination has been chosen in order to avoid band-to-band excitation for the creation of minority carriers. This enables information to be extracted from trapping states at the SiO_2/SiC interface that are energetically deep within the band gap. Empirical observations of deep level trapping states with life times in the order of tens of hours are reported and the interface trap density as a function of energy has been extracted using the Terman method. Characterisation of these interface states will aid the development of new fabrication processes, with the aim of reducing the interface trap density to the same level as that of the SiO_2/Si interface and facilitating the production of higher quality SiC based devices.

Introduction

Recently, the demand for SiC as a semiconductor for resilient sensors and ultra-efficient power electronics has increased rapidly. Applications such as solid state sensors exposed to one or a combination of 'hostile' environmental ambient conditions and high temperature / ultra-efficient drives in electric vehicles, to name but a few, are not possible with conventional Si based devices due to the unfavourable material properties. SiC is a material that is well suited to these novel and demanding applications, due to the wide bandgap and silicon to carbon bonding. The development of dielectric based devices on SiC, such as MOSFETs, requires high quality interfaces. However, previous research has shown that in comparison with the SiO_2/Si interface, the density of traps (D_{it}) in the SiO_2/SiC interface is substantially larger [1]. In order to better understand this issue and the effect on transistor structures, the SiO_2/SiC interface must be fully characterised so that fabrication processes can later be optimized in order to reduce D_{it} and improve the quality of oxide stacks.

The conventional interface characterization methods such as the Terman method [2] which use the high-frequency C-V and G-V characteristics of SiC MOS structures, are only able to evaluate information relating to interface traps with a short response time, which lie within 0.5eV of the band edges. The long response time of the deep level interface traps (those energetically deep in the band gap) mean they do not have time to respond to the probe signal and are not thermally isonised due to their energy being substantially greater than the thermal energy. We have shown previously that photo-illumination of the MOS structure can generate a higher number of minority carriers [3], which enable them to interact with these deep level states, allowing their characterization. In this work, we have extended the analysis to include sub-bandgap illumination to investigate the decay time of deep level traps [4] without the influence of minority carriers.

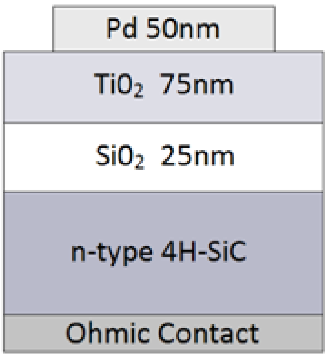


Figure 1 – MOS structure investigated

Experimental

Metal-Oxide-Semiconductor (MOS) capacitor structures with a high-κ dielectric layer were fabricated on research grade 4H-SiC epilayers with thickness of 2μm and doping concentration of $3.25 \times 10^{15} cm^{-3}$. The structure is layered as Pd/TiO_2/SiO_2/4H-SiC, where the TiO_2/SiO_2 dielectric stack is used to increase the critical electric field in the device. Photonic excitation was provided by a 175W xenon fibre optic light source, which is passed through a dual grating monochrometer (300 to 800nm spectral range) with a fibre optic output, directed above the gate of the device. The wavelength and photonic intensity were measured using a hyper-spectral CCD based spectrometer. Figure 1 shows a schematic cross section of the capacitor structure used in this study. 1MHz C-V and G-V characteristics were measured using an Agilent 4284A precision LCR measurement bridge.

The illumination of the device was performed at two wavelengths, $\lambda = 350nm$ (above bandgap) and $\lambda = 550nm$ (sub-bandgap). The voltage was first swept from accumulation to deep depletion to sweep the mobile charges from the oxide – SiC interface in order that the traps are empty. The device was then illuminated via fibre optic for 60 seconds, whilst a DC bias of -6 volts was used to hold the device in deep depletion. The bias was then swept back from deep depletion to accumulation. The illumination intensity was varied between dark and 60k relative intensity in increments of 10k for each consecutive pair of C-V and G-V sweeps. During time constant investigations, the illumination was turned off after an initial 'trap filling period' and then the device was repeatedly swept from deep depletion to accumulation in 30 minute increments.

Results

Figures 2 and 3 show the C-V and G-V curves under 350nm illumination. The data shows that with increasing illumination intensity, the C-V curve shifts toward a more negative bias. This shift can be explained by a change in semiconductor work function, which is due to the photo-generation of carriers moving the position of the Fermi level. The amplitude of the main G-V peak decreases and a secondary peak becomes apparent at a more negative bias. This secondary peak is representative of a second trapping level at the interface with different activation energy. This trapping level is often linked to interface traps formed through the inclusion of nitrogen clusters at the SiO_2/SiC interface [5].

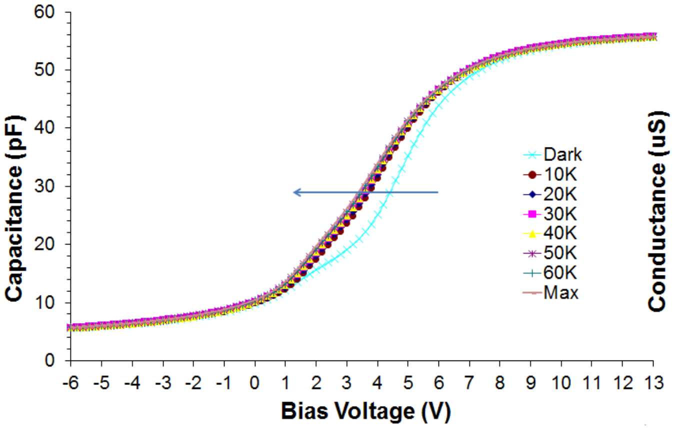


Figure 2 – 350nm C-V curves showing the shift in flatband voltage (V_{FB}) due to a change in the semiconductor workfunction.

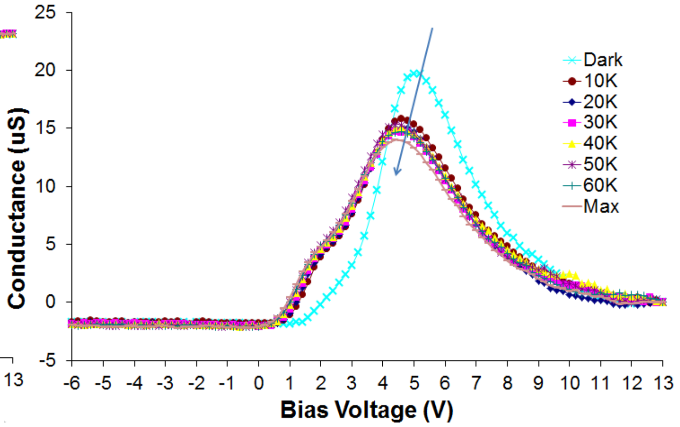
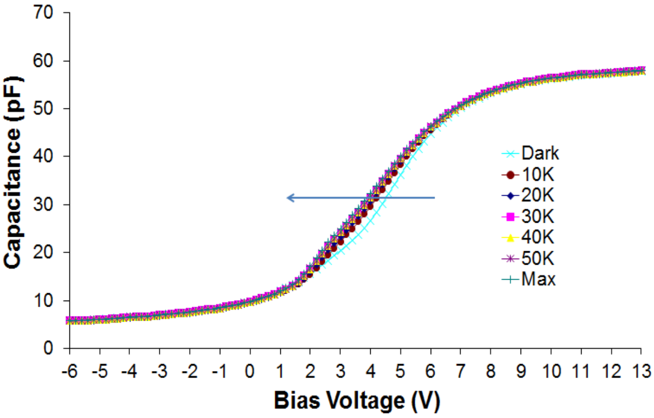


Figure 3 - 350nm G-V curves showing the reduction in the amplitude of the dominant trapping state with increasing illumination intensity.

Figures 4 and 5 show the C-V and G-V characteristics under 550nm illumination. The shift in flatband voltage in the C-V data is less pronounced than that observed in figure 3, due to the absence of intrinsic carrier photo-generation and the reliance on extrinsic photo-generation. The G-V data shows a reduction in amplitude of the main peak with increasing illumination intensity. This is similar to that observed in the $l = 350nm$ data, and is thought to be related to the changes in time constant of the dominant trapping state [6]. The data also shows that the second peak increases in amplitude with increasing photon intensity. The $l = 550nm$ illumination is activating this trapping state and with increased intensity results in an increasing number of carriers interacting with this trap. The shift in horizontal position of the conductance peak in both Figure 3 and Figure 5 is linked with the change in flatband voltage caused by the illumination of the device.



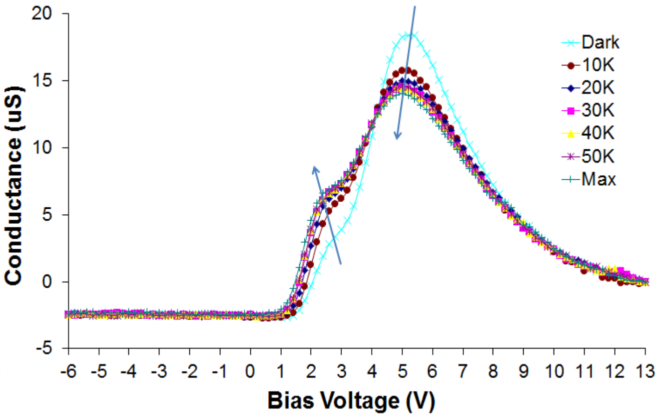
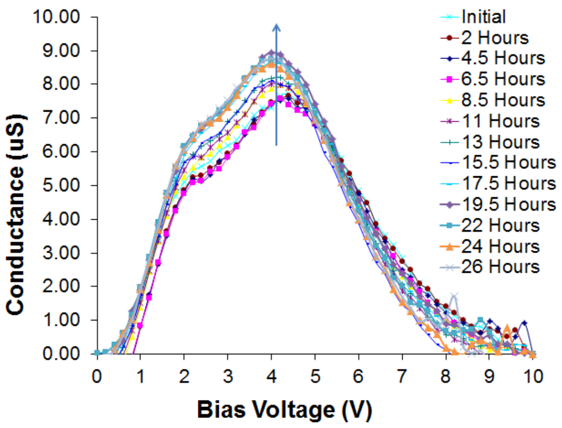


Figure 4 – 550nm C-V curve with a less pronounced shift in V_{FB} due to the reliance on extrinsic photo generation of carriers.

Figure 5 - 550nm G-V curve, the growth of the second trapping level is clearly visible as the intensity is increased.

When the illumination is removed, the interface traps relax. The time in which the trap takes to release this captured charge carrier depends on the time constant of that trapping level and this is determined by the energy difference between the trap and the Fermi level. Figure 6 shows the G-V characteristics of the device as a function of time since the illumination has been removed. The data reveals that after a period of 26 hours, the interface has not fully relaxed and the G-V characteristic has reduced to a value below the initial sweep taken under illumination. These observations show the existence of interface traps with different activation energies and traps that are energetically deep in the bandgap which have extremely long lifetimes.



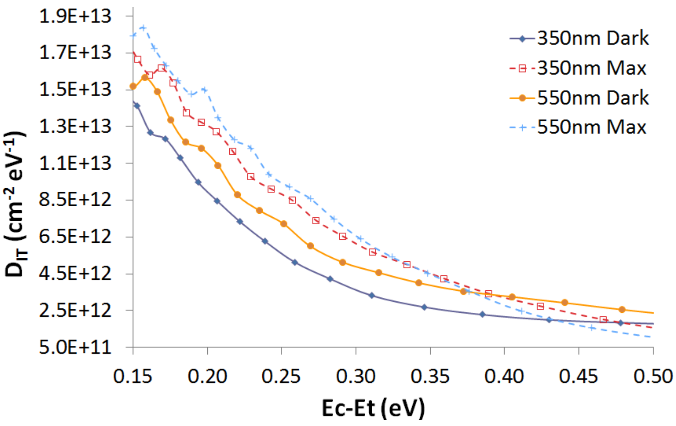


Figure 6 – 26 hour delay G-V curves showing relaxation of the interface traps.

Figure 7 - Extracted interface trap density as function of energy using the Terman method.

The Terman method was used to extract the interface trap density as a function of energy between 0.2eV and 0.5eV below the conduction band edge. The extracted values are shown in Figure 7 and show that D_{it} is 1.8×10^{13} $cm^{-2}eV^{-1}$ at the conduction band edge and 2×10^{12} $cm^{-2}eV^{-1}$ at 0.5eV below the conduction band. These extracted values are much larger than that of the SiO_2/Si interface which is usually in the order of 10^{10} $cm^{-2}eV^{-1}$. The data indicates that following illumination at both wavelengths the distribution of interface states change across the energy range considered. The results of the Terman analysis reveal that the low energy traps (energies of less than 0.48eV for 350nm and less than 0.38eV for 550nm) increase in density and the high energy traps (energies above 0.48eV for 350nm and above 0.38eV for 550nm) decrease in density. This suggests a redistribution of interface states caused by photo-illumination and can be linked to the change in amplitude in the main and secondary peaks observed in the G-V characteristics in Figures 3 and 5.

Considering the evidence we have reported on in Figures 3, 5, 6 and 7, we have shown that information regarding deep level traps has been extracted from the photo-CV characterisation of the SiO_2/Si interface.

Summary

In this paper we have shown experimental evidence for the existence of deep states by the use of sub-bandgap illumination for the first time in SiC. It has been reported that interface trapping levels can be activated by using a specific wavelength of light to target trapping levels deep within the bandgap and information extracted by using Terman analysis. The interface trap density at the SiO_2/SiC interface has been found to be between 1.8×10^{13} $cm^{-2}eV^{-1}$ and 2×10^{12} $cm^{-2}eV^{-1}$ depending upon the energy level. We can excite trapping levels by generating minority carriers by illumination and we have observed interface time constant dispersal, by observing the reduction in amplitude of the dominant trapping level and the increase in a second trapping level with increasing intensity of illumination. Observations have also led to information regarding the time constants of interface traps and have been found to have extremely long lifetimes, in the order of tens of hours and evidence suggests even longer than that. It has been also found that under illumination, there is an interface state redistribution, allowing characterisation of deep interface states, which relates to the decrease and increase in amplitude the dominant and second trapping states respectively. It should be possible to excite other trapping levels with other wavelengths of light to obtain more information on the SiO2/SiC interface to enable process monitoring and overcome the problem of high D_{IT} and in the near future be able to produce high quality, high performance SiC based power and sensing devices for the emerging but demanding applications that the electronics industry has yet to realize commercially.

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