Ph.D.Dissertation

Design of Fast Transient Response Digital Low-Dropout Regulator for Advanced Memory Application

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by

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Department of Electrical and Computer Engineering
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Abstract

In this dissertation, the design of a fast transient response digital low-dropout regulator (DLDO) applicable to next-generation memory systems is discussed. Recent technologies in memory systems mainly aim at high power density and fast data rate. Accordingly, the need for a power converter withstanding a large amount of load current change in a short period is increased. Accordingly, a solution for compensating for a voltage drop that causes significant damage to a memory data input/output is searched according to a periodic clock signal. With this situation, two structures that achieve fast transient response performance under the constraints of memory systems are proposed.

To mitigate the transient response degradation under slow external clock conditions, an adaptive two-step search algorithm with event-driven approaches DLDO is proposed. The technique solves the limitations of loop operation time dependent on slow external clocks through a ring-amplifier-based continuous-time comparator. Also, shift register is designed as a circular structure with centralized control of each register to reduce the cost. Finally, the remaining regulation error is controlled by an adaptive successive approximation algorithm to minimize the settling time. Fast recovery and settling time are shown through the measurement of the prototype chip implemented by the 40-nm CMOS process.

Next, a digital low dropout regulator for ultra-fast transient response is designed. A slope-detector-based coarse controller to detect, compensate, and correct load current changes occurring at every rising or falling edge of tens to hundreds of megahertz

clocks is proposed. Compensation efficiency is increased by the method according to the degree of change in load voltage over time. Furthermore, the LUT-based shift register enables the fast loop response speed of the DLDO. Finally, a bidirectional latch-based driver with fast settling speed and high resolution are proposed. The prototype chip is implemented with a 40-nm CMOS process and achieves effective load voltage recovery through fast transient response performance even with low load capacitance.

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Keywords: Fast transient response, low-dropout regulator (LDO), digital low-dropout regulator (DLDO), linear search, binary search, ring-amplifier based comparator (RA-CMP), circular shifting register (CSR), event-driven, slope detector, LUT-based shift register, bi-directional latch-based driver, comparator (CMP)-triggered oscillator.

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Chapter 1

Introduction

1.1 Motivation

Power converters, including DC-DC converters, are widely used in an integrated system-on-chips (SoCs) as a power supply source that can provide stable current and voltage to building blocks. Power converter supplies appropriate power from large systems to small sub-modules as shown in Fig. 1.1. Recently, however, many functions have been integrated into a single die. Therefore, it is hard to integrate all of the power converters that supply power to the intellectual properties (IPs) due to various constraints. For example, there are sub-blocks with multiple functions within building blocks, such as phase-locked-loop and analog-to-digital converter, and the power conditions for each block to operate in an optimal state are different. If all of the sub-blocks in the system receive power from one source, their transient current will affect

the surrounding blocks as noise through the power source. As such, the supply noise generated in the power converter's output also acts as a factor that degrades the performance of the target IP [1].

Low-dropout regulator (LDO) has been proposed to overcome these problems and is commonly used in SoC design. LDO regulates supply voltage, allows IP to achieve higher power efficiency, and reduces power noise caused by external power sources. In addition, even if a single supply battery is used, various supply voltages can be

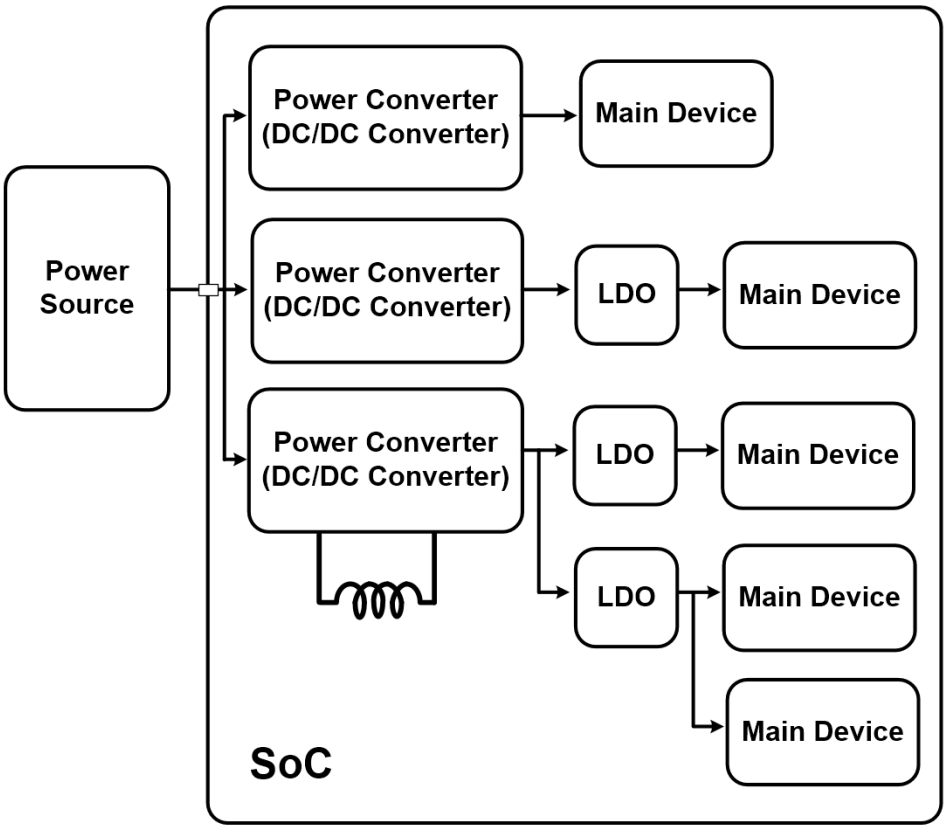

Fig. 1.1 Power delivery system in SoC.

created and distributed with fewer resources. Therefore, LDO is currently adopted as an appropriate power block since the chip area has become increasingly important.

Also, high-performance LDO regulators designed to support advanced memory have been released. LDO used in memory requires various characteristics compared to the existing conventional structure. A key feature is the ultra-fast transient response, minimizing output-voltage fluctuations. Frequent changes in voltage commonly occur in UFS-based MCPs due to varying levels of read and write performance. However, ultra-fast transient response regulates these fluctuations to a steady state within 100 ns [2].

1.2 Various types of LDO

1.2.1 Analog LDO vs. Digital LDO

LDO is defined as two types according to the pass gate configuration: analog low-dropout regulator (ALDO) [6] – [29] and digital low-dropout regulator (DLDO) [31] – [53] are shown in Fig. 1.2 and Fig. 1.3, respectively. ALDO is used in applications that require high power supply rejection (PSR) performance and low output ripple. However, structures using error amplifier(EA) is often designed with cascodes to obtain sufficient gain, which causes voltage headroom problems. In addition, the analog EA requires re-design whenever the process changes. After all, these characteristics are not suitable for LDO designs as the process becomes finer.

Meanwhile, DLDO is widely used in the recent trend of lowering the supply power according to process scaling since it generally operates well even at low voltages. By using a digital circuit, a higher loop gain than ALDO can be obtained, and because an error detector is used instead of EA, robustness to supply voltage is obtained. In addition, DLDO is attracting more attention in high technology process design than ALDO because DLDO shows better scalability, portability, and integration performance. DLDO adopts a method of controlling power MOSFET with the digital manager. Since the voltage applied to the gate of the MOSFET is a logic of 0 or 1, the MOSFET always operates in the linear or cut-off range. DLDO shows better current density than ALDO because MOSFET current is adjusted in full range. Also, on-resistance is smaller than ALDO’s, so the small voltage drop is presented.

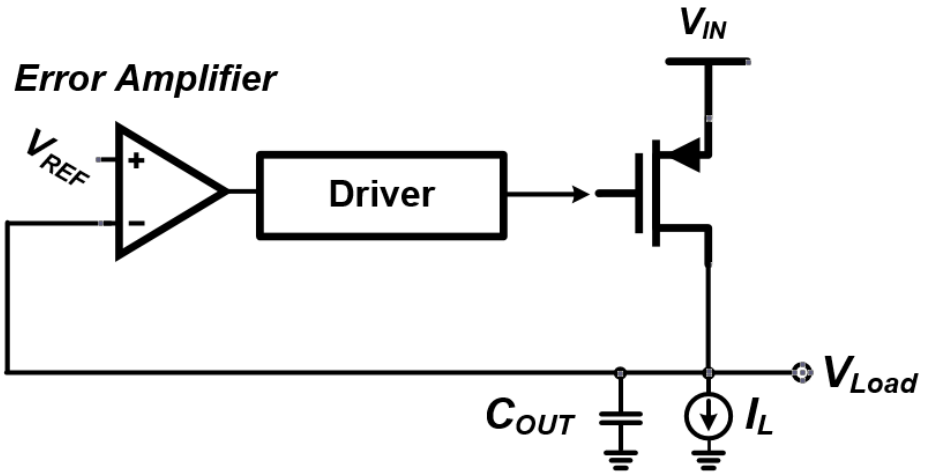

Fig. 1.2 Block diagram of conventional analog LDO.

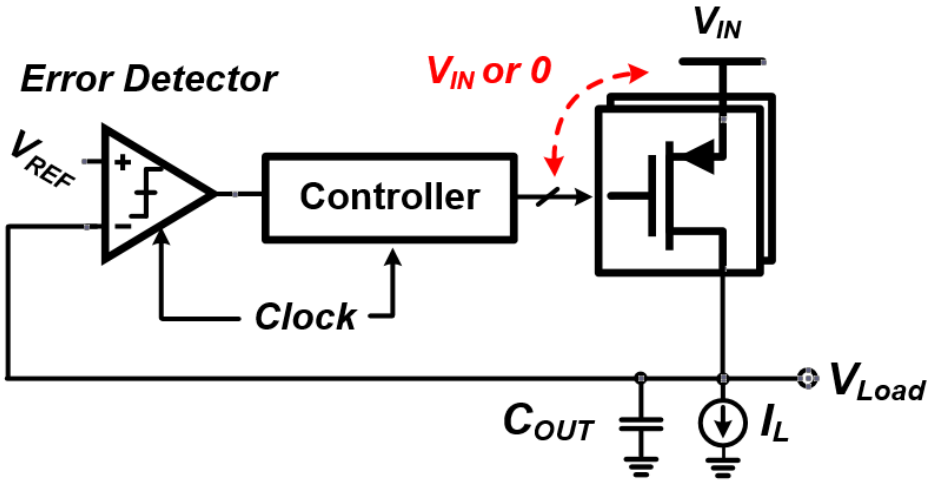

Fig. 1.3 Block diagram of conventional digital LDO.

1.2.2 Cap LDO vs. Cap-less LDO

Fig. 1.4 and Fig. 1.5 show LDO types with and without load capacitors, respectively. Depending on the capacitance value attached to the output node of the LDO, various performances change represents the LDO. The total capacitance of the output node is the sum of the capacitance intentionally added by the designer and the capacitance by parasitic. In general, if there is no intentionally added capacitor or it is not large, it can be seen as a cap-less structure [7], [11], [20], [29], [39], [50]. In terms of a transient response, the load capacitor has the advantage of slowing down the rate at which a drop occurs. In addition, the capacitors at the load stage show good PSR performance at high frequencies for LDOs. However, the area occupied by the capacitor is large enough and leads to a big problem that reduces the overall area efficiency. The use of external capacitors occupying a large area is becoming difficult in a recent integrated circuit environment where the number of physical fins is limited as the die size is reduced. Also, the large capacitance makes a dominant pole at the load in the LDO system. Therefore, a stability issue due to load current variation should be reviewed and designed through a sufficient number of simulations. Design that exploit the cap-less structure is weak against the voltage drop caused by the load current variation, so various methods have been proposed to supplement load transient response of cap-less LDO. For example, NMOS structure [20], feedforward structure [25] and self-clocked structure [50] for faster response of LDO to variation are proposed.

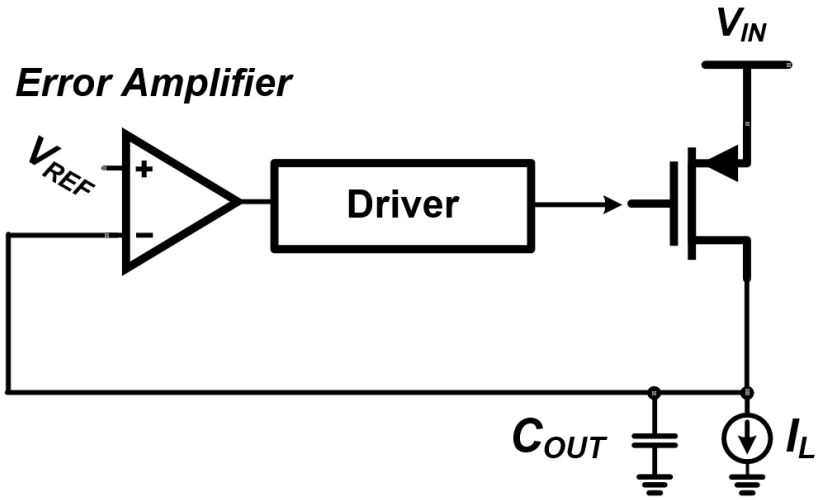

Fig. 1.4 Block diagram of Cap LDO.

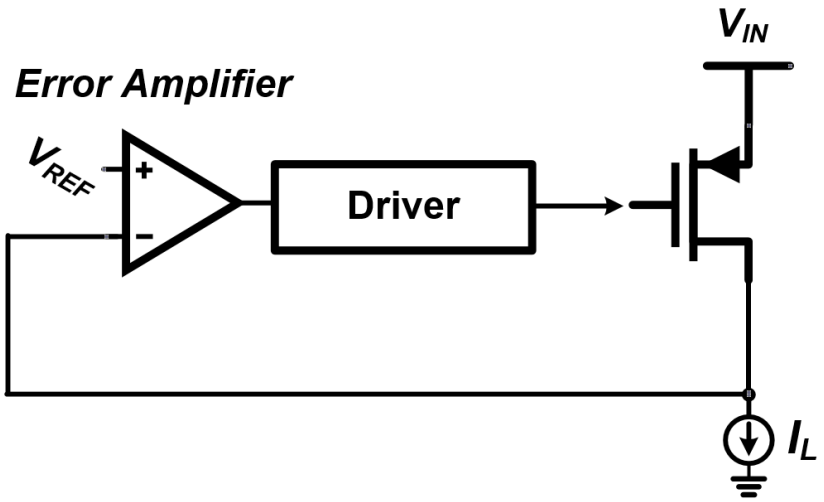

Fig. 1.5 Block diagram of Cap-less LDO.

1.3 Thesis Organization

This thesis is organized as follows. In Chapter 2, the backgrounds of the DLDO are explained. First, basic DLDO behavior is provided, and then analyze the elements necessary for LDO to have a fast transient response. After that, several LDO design methods for improving transient performance are introduced.

In Chapter 3, a fast droop-recovery event-driven digital LDO with Adaptive linear/binary two-step search is presented. The event-driven DLDO offers fast recovery performance and reduced undesirable output shooting with coarse and fine two-step regulation. In addition, the two-step regulation controller is connected by asynchronous signal transition logic helps to respond immediately to load variations.

In Chapter 4, a fast transient response digital LDO with current LUT-based control for digital load application is presented. The slope detector using the CMP-triggered oscillator tracks the load variation immediately and measures the voltage change speed at the load. Furthermore, using LUT reduces the delay caused by complex computational processes with slew-rate information of load voltage. Besides, the settling speed of DLDO is improved using the bi-directional latch-based drivers.

Chapter 5 summarizes the proposed works and concludes this thesis.

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Chapter 2

Backgrounds on Digital Low-Dropout Regulator

2.1 Basic Digital Low-Dropout Regulator

The general DLDO structure is shown in Fig. 2.1. DLDO consists of a comparator that senses a load voltage and outputs a digital value of 1 or 0 compared to a reference voltage and a controller part that adjusts the gate voltage of the power MOSFET by receiving the comparator output value. In addition, output load capacitors are generally required to reduce voltage drop by load variation. Various implementation methods have been proposed depending on the elements constituting LDO are implemented.

For example, the error detector is also implemented in various ways. Depending

on the method of sensing the load voltage, the LDO type is divided into time-driven design and event-driven design [31], [33] – [35]. As shown in Fig. 2.2, time-driven design operates the voltage regulation loop using digital values based on errors every certain period, while the comparator operates based on the clock. If the load variation occurs in the middle of two adjacent clock edges, the delay occurs until the loop starts because the trigger signal generation depends on the clock edge. Moreover, it is the worst time for voltage droop or overshoot because it allows load variation to proceed freely without any control during this time. Time loss can be minimized by increasing the speed of the operation clock, but many resources are required for this. An event-driven structure has been proposed to alleviate this performance–resource trade-off.

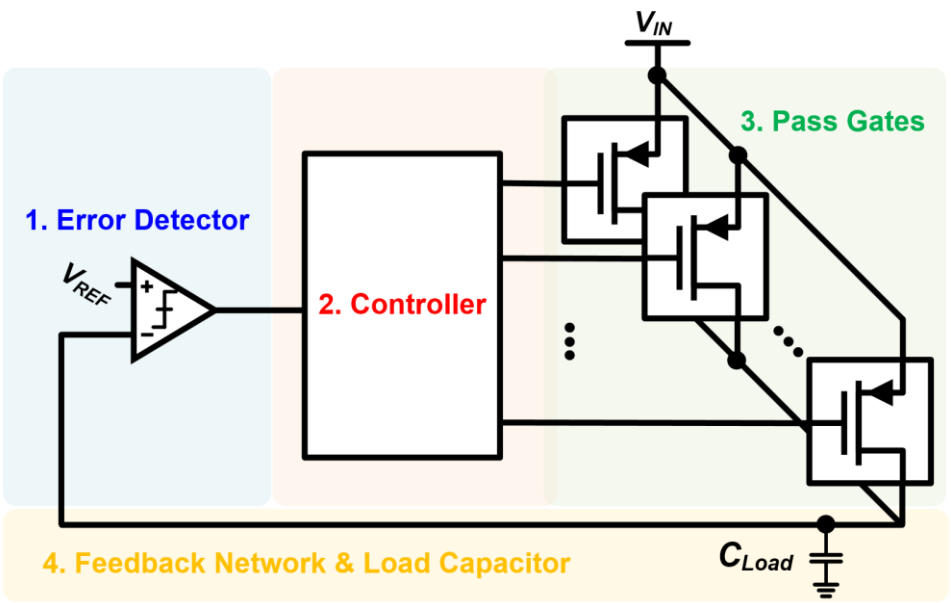

Fig. 2.1 Structure of basic digital low-dropout regulator.

This structure continuously senses the load voltage and outputs a logic value if it exceeds a certain threshold. In other words, since it immediately reacts to load variations outside the allowable range, a fast reaction rate can be obtained regardless of the operation clock.

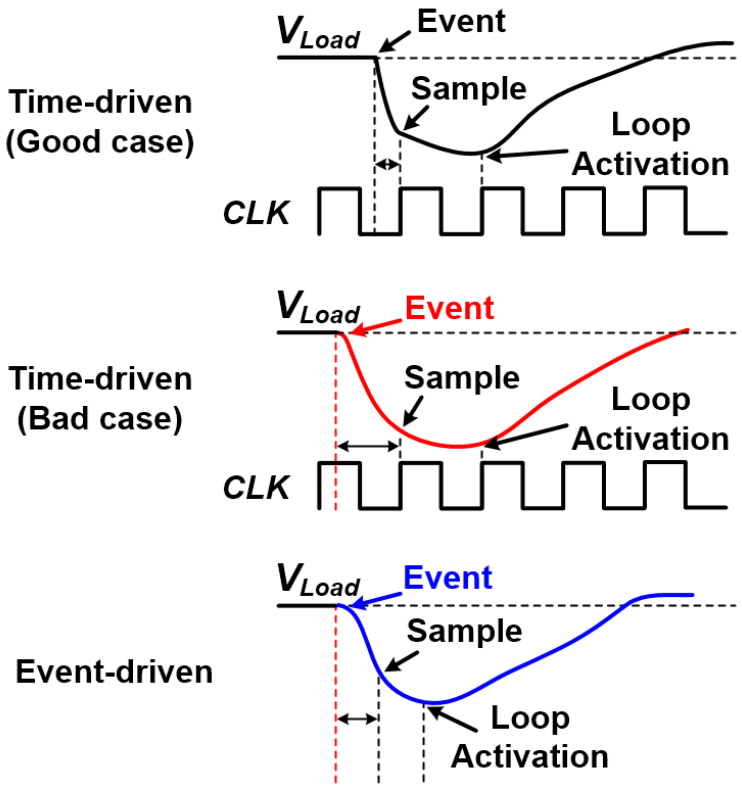

Fig. 2.2 Conceptual procedure of time-driven and event-driven regulation methods.

2.2 Fast Transient Response Low-Dropout Regulator

In light of the role of LDO in finally supplying stable voltage and current to IP, even a small perturbation of load voltage may cause the internal system to malfunction or fail. Moreover, as low-voltage operation has become important recently, the allowable voltage error range has decreased further [1]. Therefore, it is crucial to minimize the load voltage variation under LDO operating conditions for stable operation of IP. In addition, in the case of digital load applications, where current consumption occurs periodically, it is an essential factor in the speed of application operation to quickly recover and set the voltage droop to the target voltage to prepare for the next drop.

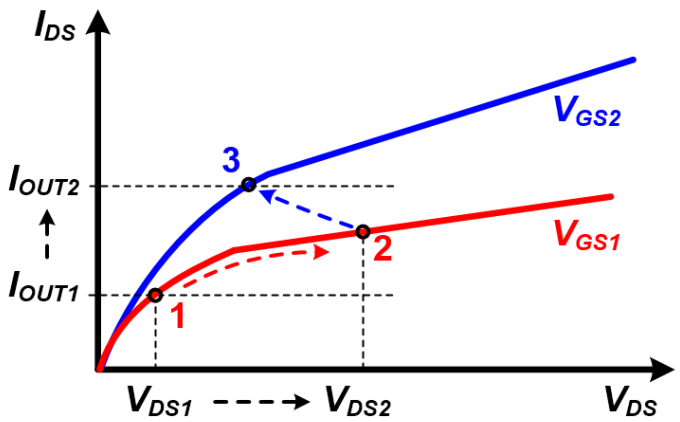

Fig. 2.3 Pass gate V_{DS}-I_{DS} curve with increasing I_{OUT}.

2.2.1 Response Time

In this section, the load voltage variation caused by the load current variation is examined through formulas and figures. Also, explore response times, which are important for reducing load voltage variations.

Fig. 2.3 shows a graph of a case where the load current increases rapidly. To take a general situation as an example, a pass gate serving as a power source is assumed as a PMOS. When the load current steps up rapidly from I_{out1} to I_{out2}, which is a steady state, the load voltage of LDO drops significantly. Droop occurs since LDO's feedback loop does not immediately respond to load variation, and the pass gate tries to flow only as much current as previously supplied. Because the feedback control is not activated immediately after the load variation occurs, the gate-source voltage (number of PMOSs in the ON state in DLDO) of the PMOS remains the same just before the variation occurs. Therefore, the drain-source voltage of PMOS increases from V_{DS1} to V_{DS2} according to the load current variation, as shown in Fig. 2.3. In the meantime, the feedback loop starts to operate, and as the gate voltage of the pass gate PMOS begins to change, the current supplied begins to increase. The load voltage no longer drops when the pass gate current reaches the load current. DLDO increases the pass gate current supplied as the number of PMOS segments in the on state increases, not the gate voltage of the PMOS. To estimate the falling load voltage, the total impedance shown at the load stage is as follows.

$$\boldsymbol{Z_{Load} = \ r_{ds} \ || \ R_F \ || \ R_{Load}} \tag{2.1}$$

r_{ds} represents the output resistance of PMOS pass gates, R_F represents the resistance of the feedback network, and R_{Load} represents the impedance depending on the output. Using this, the maximum load voltage variation when a load current change of ΔI_{Load} occurs before the feedback loop is activated as follows.

$$\Delta \boldsymbol{V_{max}} = \boldsymbol{Z_{Load}} * \Delta \boldsymbol{I_{Load}} \tag{2.2}$$

$$\Delta V_{max} = (r_{ds} \;||\; R_F \;||\; R_{Load}) * \Delta I_{Load} \tag{2.3}$$

Until now, load voltage variation is obtained by assuming a situation in which only resistance is present at the load stage. In general, LDO exhibits poor transient response performance when the capacitance is small at the load stage. Therefore, the previous analysis is performed again, considering the capacitance at the load stage.

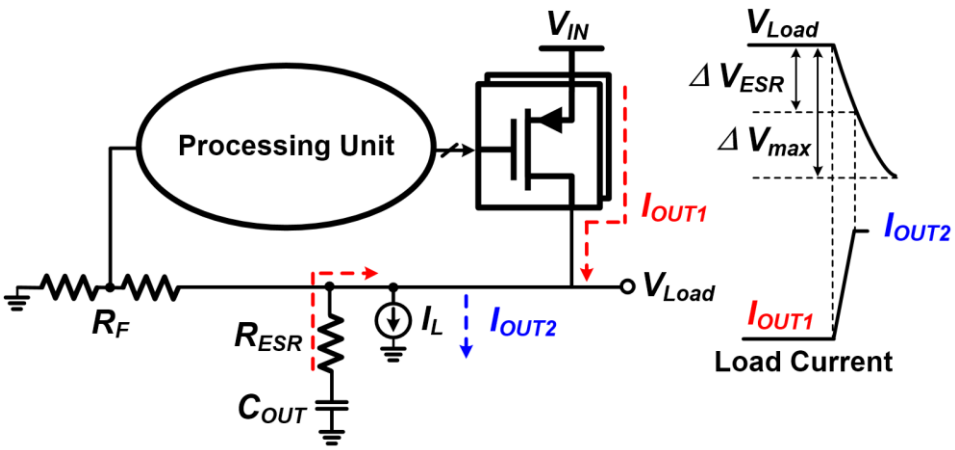

Fig. 2.4 Diagram of current flow and load voltage variation with load-transient response.

Fig. 2.4 shows the case where the load current increases in step function where a load capacitor is added to the LDO. Unlike the PMOS pass gate supplied all of the increased load currents in the previous analysis, it can be temporarily supplied from the load capacitor. As a result, the burden on the increase in load current covered by the PMOS pass gate is reduced until the feedback loop of LDO is activated. The total load impedance, including the load capacitor, is expressed by the equation as follows.

$$\boldsymbol{Z_{Load}} = \boldsymbol{r_{ds}} \;||\; \boldsymbol{R_F} \;||\; \boldsymbol{R_{Load}} \;||\; \boldsymbol{Z_C} \tag{2.4}$$

Here, Z_C is an impedance of a load capacitor, including an equivalent series resistance (ESR). The maximum load voltage variation equals the changed amount of load current multiplied by the load impedance. This is expressed in an equation as follows.

$$\Delta \boldsymbol{V_{max}} = (\boldsymbol{r_{ds}} \;||\; \boldsymbol{R_F} \;||\; \boldsymbol{R_{Load}} \;||\; \boldsymbol{Z_C}) * \Delta \boldsymbol{I_{Load}} \tag{2.5}$$

Due to capacitance, the load voltage slowly drops with a delay up to the max value. On the other hand, ESR is a resistor connected in series to the capacitance and can instantaneously cause a significant voltage drop regardless of the capacitor. This is expressed by a formula as follows.

$$\Delta \boldsymbol{V_{ESR}} = \boldsymbol{R_{ESR}} * \Delta \boldsymbol{I_{Load}} \tag{2.6}$$

The smaller ESR makes the effect less critical. Suppose that the ESR of the capacitor to be used for analysis is smaller than that of Z_C. In addition, the effect of increasing pass gate current caused by an increase in drain-source voltage by voltage drop is excluded from the analysis. According to the law of charge conservation, it is used as follows.

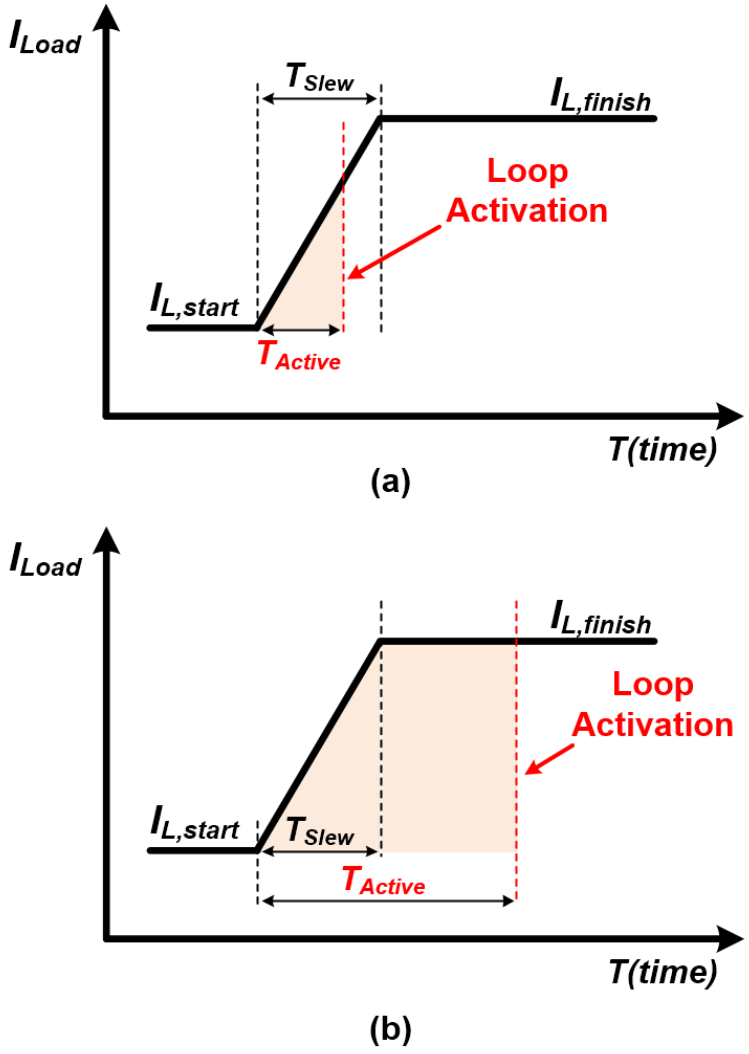

Fig. 2.5 Graph of loop activation time depending on load current slew-rate.

$$\Delta \boldsymbol{V_{Load}} = \Delta \boldsymbol{I_{Load}} * \frac{\boldsymbol{T_{Active}}}{\boldsymbol{C_{Load}}} \tag{2.7}$$

ΔV_{Load} is the change in load voltage, ΔI_{Load} is the change in load current, and C_{Load} is the capacitance of the load capacitor. In addition, T_{Active} is the duration between the load current variation occurring and the pass gate current changes. T_{Active} is sometimes called response time.

Fig. 2.5 illustrates the amount of charge the capacitor discharges when the load current's transition rate (slew rate) is slower or faster than the T_{Active}. For the load voltage to no longer fall, the pass gate current must reach the final load current value. Considering this, the time it takes for the load voltage to not drop, T_{Total}, can be expressed as the sum of the time until the loop is activated and the time until the final current is reached.

$$\boldsymbol{T_{Total}} = \boldsymbol{T_{Active}} + \boldsymbol{T_{Follow}} \tag{2.8}$$

As the time required for the pass gate current to reach the target is shortened, a slight voltage variation occurs under the same external conditions. However, to obtain the exact value at which the load voltage drops, it must be calculated considering the situation where the pass gate current increases after T_{Active}.

As shown in Fig. 2.6(a), if T_{Slew} has an order value similar to T_{Active}, the amount of charge supplied by the capacitor depends on the slew rate. Therefore, the amount of charge discharged from the capacitor is as follows.

$$\begin{aligned} \mathbf{Q} = (\boldsymbol{T_{Active}} + \ \boldsymbol{T_{Follow}}) * \Delta \boldsymbol{I_{Load}} - \frac{\mathbf{1}}{\mathbf{2}} \boldsymbol{T_{Follow}} \Delta \boldsymbol{I_{Load}} \\ - \frac{\mathbf{1}}{\mathbf{2}} \boldsymbol{T_{Slew}} \Delta \boldsymbol{I_{Load}} \end{aligned} \tag{2.9}$$

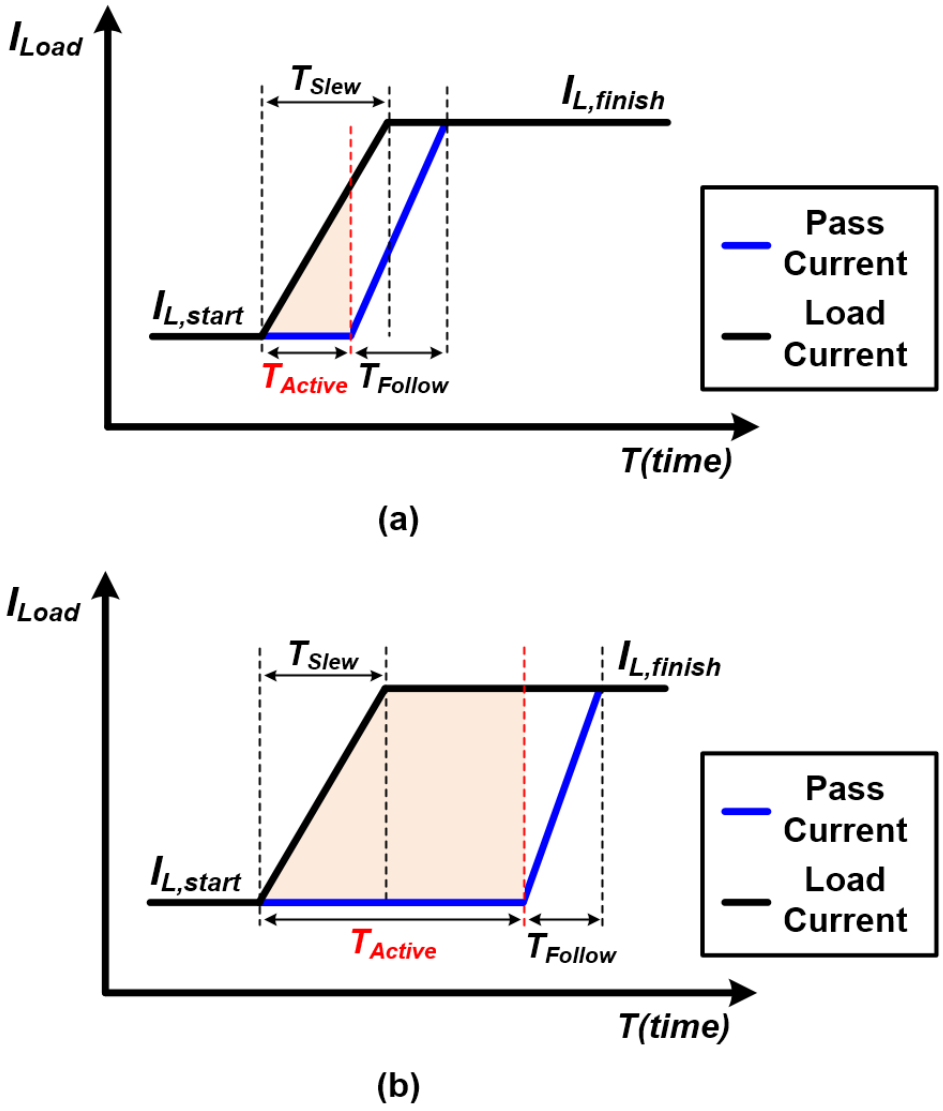

Fig. 2.6 Graph of pass gate and load current.

$$\mathbf{Q} = \left(\boldsymbol{T_{Active}} + \frac{\mathbf{1}}{\mathbf{2}} \boldsymbol{T_{Follow}} - \frac{\mathbf{1}}{\mathbf{2}} \boldsymbol{T_{Slew}} \right) * \Delta \boldsymbol{I_{Load}} \tag{2.10}$$

Therefore, the load voltage droop generated through as follows.

$$\Delta \boldsymbol{V_{Load}} = \Delta \boldsymbol{I_{Load}} * \frac{\boldsymbol{T_{Active}} + \frac{\mathbf{1}}{\mathbf{2}} \boldsymbol{T_{Follow}} - \frac{\mathbf{1}}{\mathbf{2}} \boldsymbol{T_{Slew}}}{\boldsymbol{C_{Load}}} \tag{2.11}$$

As shown in Fig. 2.6(b), if T_{Slew} is much smaller than T_{Active}, the load current transition time has little effect on the load voltage variation.

$$\Delta \boldsymbol{V_{Load}} = \Delta \boldsymbol{I_{Load}} * \frac{\boldsymbol{T_{Active}} + \frac{\mathbf{1}}{\mathbf{2}} \boldsymbol{T_{Follow}}}{\boldsymbol{C_{Load}}} \tag{2.12}$$

2.2.1 Settling Time

Settling time is the time elapsed from the initial onset of the load transient to when the output voltage returns within a few percent of a steady-state value [3]. It is an essential feature in the voltage regulation of the digital load, which requires periodic motion between two events where the load current changes. The load voltage must be quickly brought to the target voltage for the digital core and peripheral circuits to operate without problems. In addition, the shorter the setting time, the easier it is to reduce the duration between events without any problem in power stability.

Setting time is also associated with the DC regulation accuracy of LDO. It is a factor associated with the bandwidth of the LDO feedback loop, while DC regulation accuracy is associated with the DC loop gain. The higher the DC loop gain, the lower the final regulation error. Therefore, high DC loop gain and bandwidth of the LDO feedback loop are required to improve DC regulation accuracy and settling time performance, respectively.

The following section explains various regulation techniques that help improve digital LDO transient response performance, including the event-driven method.

2.3 Various Methods for Implement Fast Transient Digital LDO

2.3.1 Event-Driven Digital LDO

Most event detection systems perform based on a clock. Input is sampled every clock cycle, and the system considers the sampled input as a new event and decides whether to transmit it to the controller. As shown in Fig. 2.7, the system with the

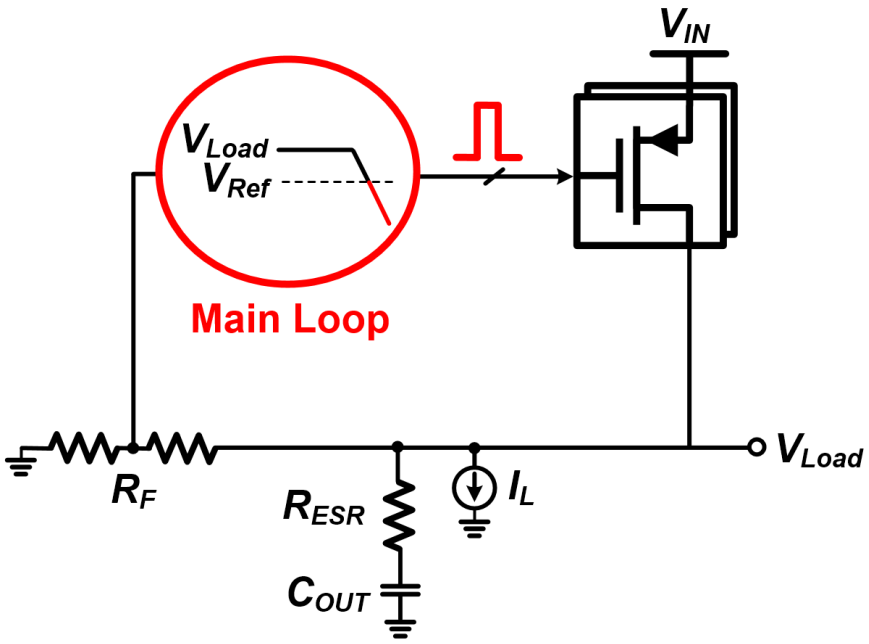

Fig. 2.7 Conceptual block diagram of event-driven digital LDO.

event-driven approach accepts new inputs only when the input changes by a certain amount or more from the previous state (i.e. new event) [31], [33] – [35]. As briefly mentioned in the previous section, the advantage of the event-driven regulation method is that the size of the output capacitor can be taken small without a high clock speed supplied. This advantage is even more apparent when a system requires many regulators to provide various power. Also, even if the output capacitor is set to be small and vulnerable to load voltage variation, the overall voltage drop is reduced due to the fast response time.

In addition, the event-driven regulation method has another advantage over the time-driven regulation method. The time-driven system tries to continuously update the controller's output, even in a steady state. Therefore, not only does it consume unnecessary power, but it also generates a ripple in output. On the other hand, the event-driven system stops updating after the output is set, and only quiescent currents, such as the leakage current of the digital circuit or the bias current of the comparator, are consumed. Therefore, it is possible to mitigate the trade-off relationship between power and transient response.

2.3.2 Feedforward Control

Unlike a loop that continuously senses a load variation and regulates voltage through feedback, the feedforward scheme is a regulation method that reduces the voltage drop with one current compensation immediately after the load variation occurs. It is also called initialization because it compensates at the beginning of the regulation process. As shown in Fig. 2.8, the feedforward compensation mechanism is not achieved through the main feedback loop. Usually, a fast second loop is implemented in addition to the main loop to immediately reflect the change in load voltage

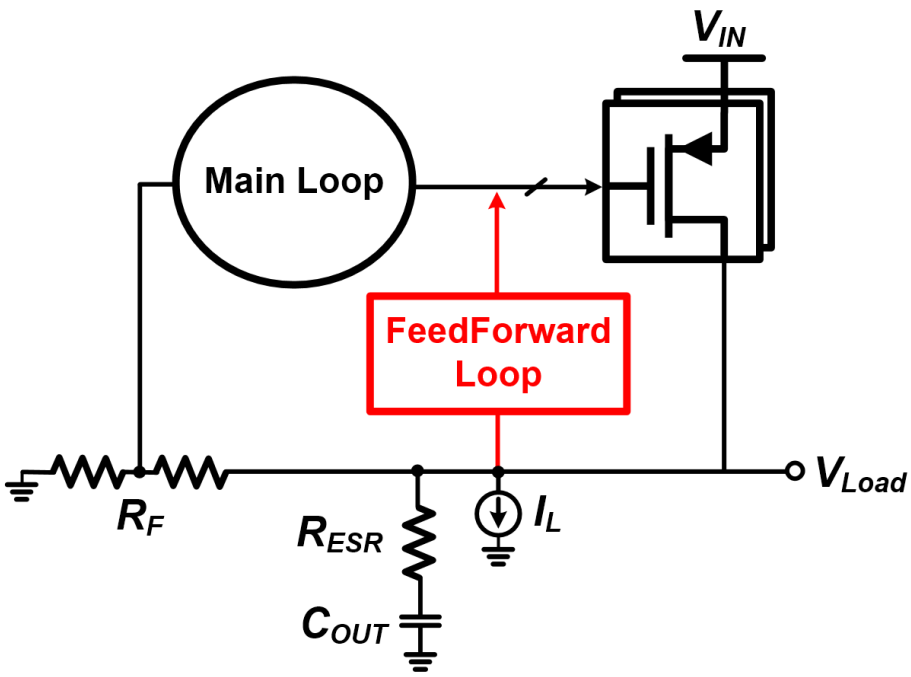

Fig. 2.8 Conceptual block diagram of feedforward-control digital LDO.

for pass gate control [3]. Since the main loop operation requires detecting and processing errors, it takes time to reflect the pass gate current even if the load variation is detected. This problem can be solved by configuring a fast loop that removes unnecessary elements. The voltage drop is also reduced by responding much faster to the load variation. It is crucial to compensate for an appropriate current because the feedforward scheme only compensates once per drop event. Also, it is not a feedback mechanism, so it has the advantage that stability-related issues do not occur.

Feedforward control can be implemented in various ways. For example, in [5], which uses a multi-bit clocked ADC, quantizes the current to be compensated and calculates it appropriately. In [54], the droop detector block is implemented as an LPF that can detect an instantaneous change when the voltage drops, thereby triggering a signal that quickly controls the pass gate without going through the main loop.

2.3.3 Computational Digital LDO

A computational scheme is a regulation method that finds and applies the control code that power MOSFET should target at once through computational logic. Unlike the regulation method through multiple cycles of feedback loops, computational regulation is completed with a single cycle control. Therefore, the accuracy and speed of obtaining the final current value are important factors in this scheme. [36] measured the ratio of time taken until the same voltage drop occurs using the maximum available current range to obtain the final current as shown in Fig. 2.9. Presented scheme is expressed by a formula as follows.

$$I_{Load,Final} = I_{MAX} * \frac{T_1}{T_1 + T_2} \tag{2.13}$$

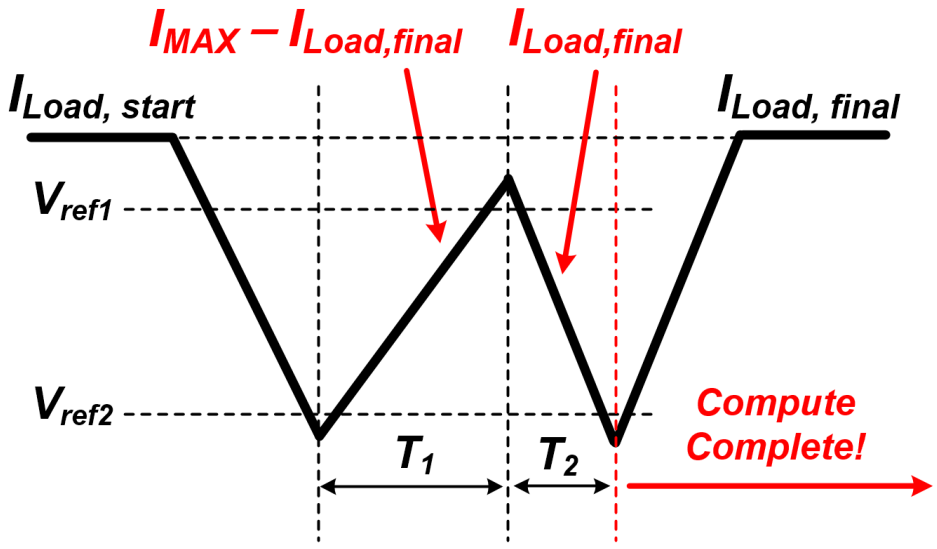

Fig. 2.9 Conceptual procedure computational digital LDO.

I_{MAX} is the maximum available current of LDO, T_1 is the time required to raise the maximum current to load by a specific voltage, and T_2 is the time required to drop the maximum current to load by the specific voltage at the pass gate.

Finding the control code at once, regardless of the output capacitor value, not only reduces the long setting time in the unnecessary searching process but also alleviates the ripple. To calculate the final current value accurately, the compute logic shall operate after the load current transition is completed. For this reason, if the output capacitor fails to delay the load current variation until the loop becomes active, a significant voltage drop may occur.

2.4 Design Points of Fast Transient Response Digital LDO

Based on the background of Chapter 2, this section summarizes the areas that need attention in designing LDO with a fast transient response. DLDO takes time for a load current variation to be compensated. It takes the sum of the time to detect the load voltage drop and output results in the error detector and the time to receive the output of the error detector, interpret it, and output to pass gate directly. DLDO does not respond to load variation during this time, and free-drop occurs unless an output capacitor is attached to the load node.

First, an error detector is the first block that generally senses the load variation and determines the direction to compensate for errors, except for methods such as feed-forward regulation. Since it is the first step in operating the loop, it is most important to determine the transient response performance of the entire DLDO. So the error detector should be operated quickly and accurately. In addition, not only does it react quickly, but it has to minimize voltage drop by optimized current compensation immediately after the loop activation.

Next, the controller directly adjusts the pass gate ON/OFF based on the result obtained through the comparator in the front. Therefore, it is a block that plays the most adjacent role in the load current track. The control code by the previous control should be stored, and new information according to the error detector output in the current state should be reflected in the control code. The shift register is the most commonly

used structure as a controller while satisfying these conditions. The shift register raises or decreases the control code value once each time an action signal is generated.

Shift registers change all output values in synchronization with the operating signal, so flip-flops are often used to store each value. In order to raise the control code value to multi-step during a single operation signal, a barrel shifter structure is adopted. As the number of steps that can be selected increases, the structure becomes exponentially complicated. Therefore, it is necessary to optimize the structure according to the function of the controller.

Chapter 3

A Fast Droop-Recovery Event-Driven Digital LDO With Adaptive Linear/Binary Two-Step Search for Voltage Regulation in Advanced Memory

3.1 Overview

Recent technologies in memory systems, such as embedded DRAM (eDRAM), resistive RAM (Re-RAM), and phase-change RAM (PC-RAM), require a dedicated

power management scheme because of their increased power density and data rate [55]. Sensing all bit-line data per word-line activation draws a large current, causing a significant voltage droop that should be recovered within tens of ns, which is the access period of each bank. However, sub-1V supply voltage makes it difficult to attain the fast recovery using analog low-dropout regulators (ALDOs). A digital LDO (DLDO) can be applied to memory systems to realize low-voltage regulation with fast response [56]. Nevertheless, such memory systems impose several critical constraints on the DLDO. An operating clock frequency f_{CLK} is limited to tens of MHz, worsening the transient response. In addition, an on-chip output capacitor C_{OUT}, which only have hundreds of pF, causes a large voltage droop by the steep load current variation.

In addressing performance degradation by the f_{CLK} and C_{OUT} constraints, several schemes have been reported to improve the transient response. While a linear search

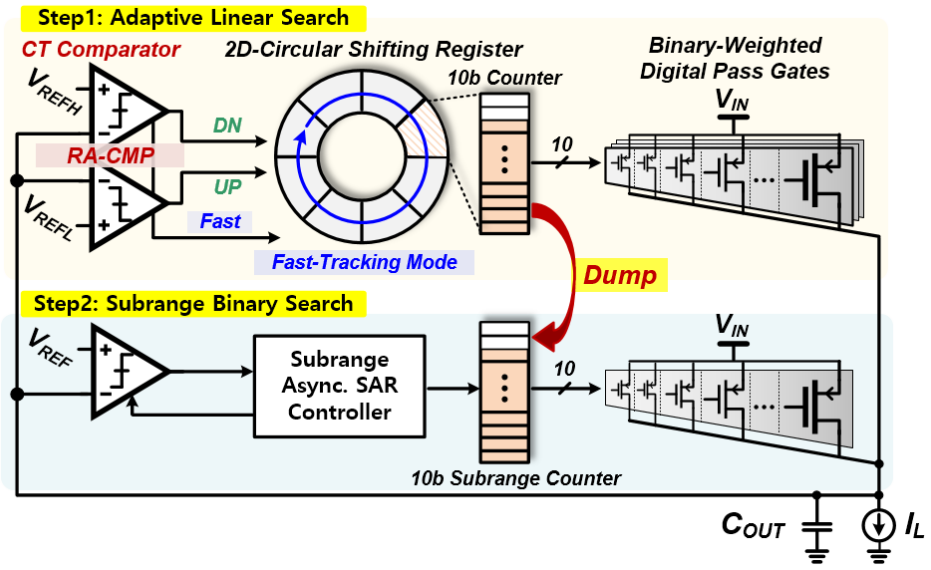

Fig. 3.1 Overall architecture of proposed DLDO.

based on a barrel shift register [49], [57] - [58] can improve the regulation speed, multi-step control increases the structural complexity and requires a multi-bit analog-to-digital converter (ADC) [49]. Another approach is a binary search based on a successive-approximation register (SAR) [59]. The binary-search regulation can provide a fast transient response, but trial-and-comparison procedure of the SAR operation can cause significant overshoot or undershoot.

In this Chapter 3 proposes an event-driven DLDO with an adaptive two-step search procedure that aims to achieve fast droop recovery with mitigation of the f_{CLK} and C_{OUT} constraints. Fig. 3.1 shows the proposed architecture, which combines an adaptive linear search and a subrange binary search. A continuous-time (CT) ring-amplifier-based comparator (RA-CMP) realizes the event-driven operation overcoming the f_{CLK} constraint. A two-dimensional circular shifting register (2D-CSR) conducts the adaptive linear-search regulation by boosting recovery from the voltage droop. Then, a subrange SAR performs the binary-search regulation with an adaptive current range, thus reducing overshoot or undershoot.

Chapter 3 is organized as follows: Section 3.2 explains the operating principle and overall architecture of the proposed DLDO. Section 3.3 describes the circuit implementation in detail. The measurement results are presented in Section 3.4.

3.2 Proposed Digital LDO

3.2.1 Motivation

Fig. 3.2 shows the conceptual searching procedures for conventional DLDOs. The linear-search DLDO has limitation of the slow transient response, while the binary-search DLDO shows large overshoot or undershoot during regulation. Conversely, the proposed searching procedure shown in Fig. 3.3 performs an adaptive linear search for coarse-step regulation and a subrange binary search for fine-step regulation, providing fast transient response without significant shootings. Fig. 3.4 and Fig. 3.5

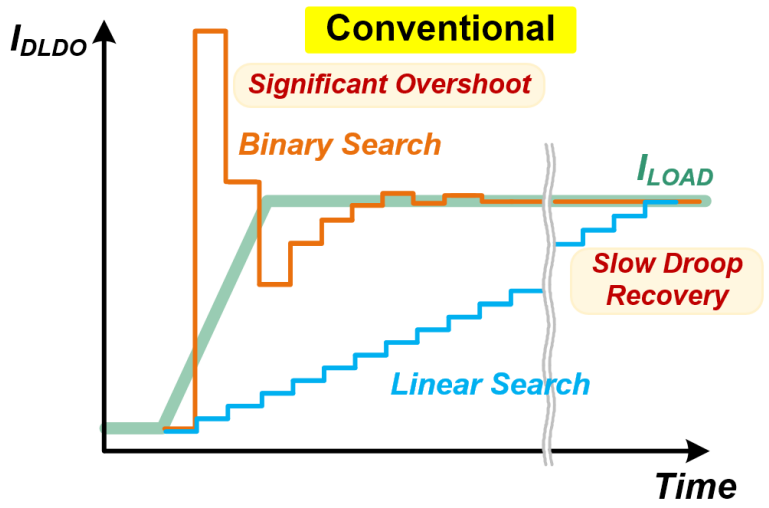

Fig. 3.2 Conceptual procedures of conventional linear/binary searches

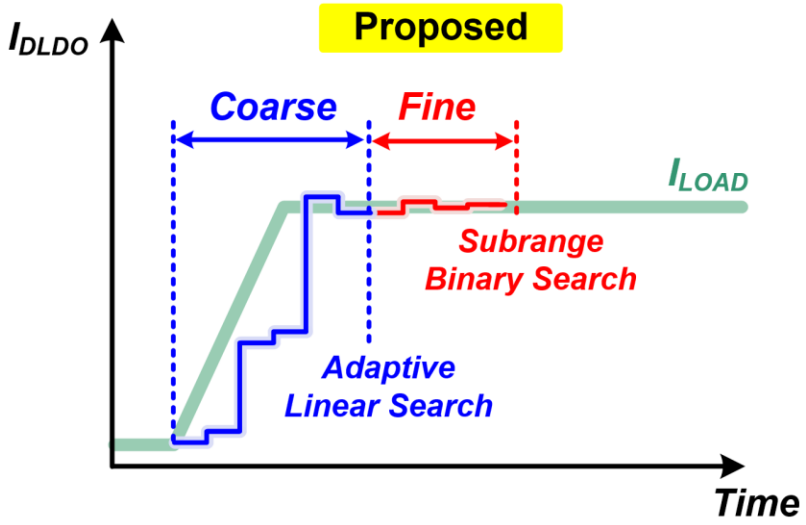

Fig. 3.3 Conceptual procedures of proposed two-step adaptive search.

show the state diagram and the timing diagram of the proposed searching procedure, respectively. When V_{OUT} becomes lower than V_{REFL} or higher than V_{REFH}, the RA-CMP triggers an adaptive linear-search controller (ALSC) by activating *UP* or *DN* signal. The ALSC adjusts the searching steps adaptively based on an amplified output error V_{ERR}. When a large V_{ERR} is detected, a fast-tracking mode is enabled to increase the number of searching steps for fast V_{ERR} recovery. Otherwise, the ALSC updates the CSR sequentially.

After the linear-search regulation, a subrange binary-search controller (SBSC) triggers *SAR_DUMP* to set an adaptive binary-search range by referring to the turn-on bits of the CSR. After that, *SAR_EN* is enabled to start the subrange SAR (Sub-SAR) for the fine-step regulation. The subrange operation can reduce not only the number

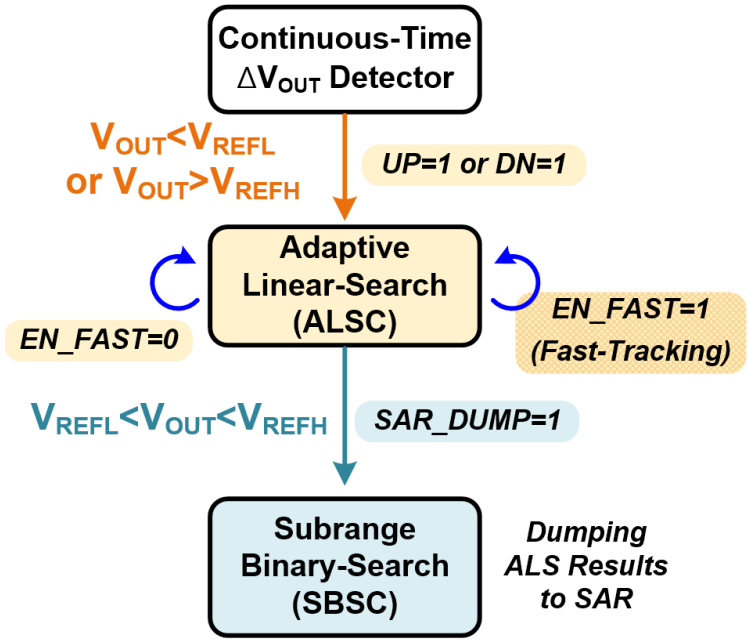

Fig. 3.4 State diagram of proposed searching procedure.

of searching steps but also the undershoot or overshoot in V_{OUT} by eliminating overflow bits. In addition, the asynchronous operations of the ALSC and SBSC allow the DLDO to achieve fast transient response, despite the f_{CLK} limitation.

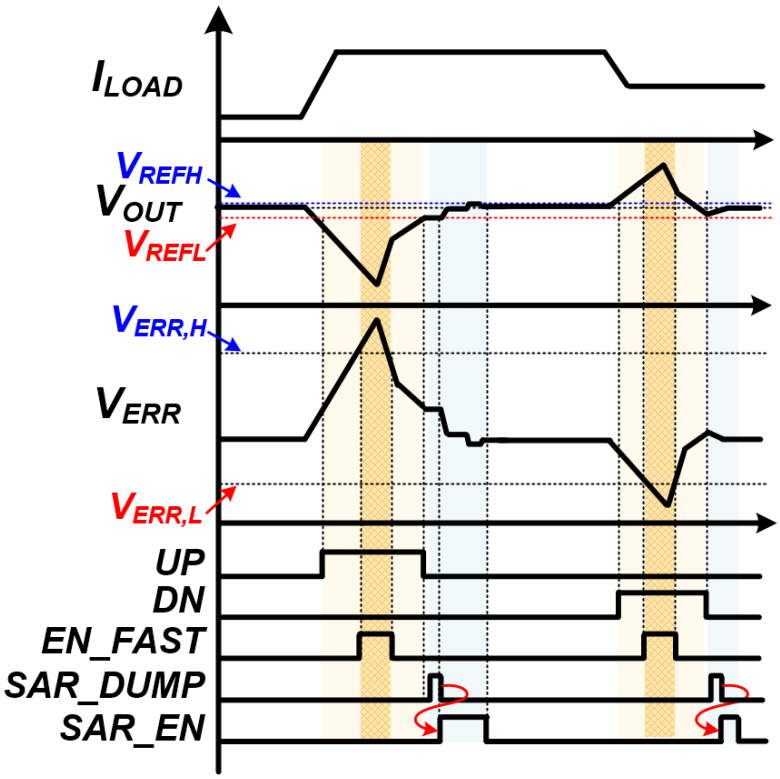

Fig. 3.5 Timing diagram of proposed DLDO operation.

3.2.2 ALSC with Two-Dimensional Circular Shifting Register

The ALSC is implemented with the 2D-CSR and the corresponding binary-weighted pass gate arrays. Fig. 3.6 shows the block diagram of the 2D-CSR element. Each CSR element consists of an asynchronous timing controller (ATC), an 1b register as a pointer, and a 10b thermometer-coded counter (TC-CNT). The 2D configuration of the 10b TC-CNT in each element allows the ALSC to realize the fast-tracking mode easily by updating either a single element or eight elements entirely. The ATC manages the asynchronous operations of the pointer and the TC-CNT in the same element. During the ALSC operation, the activated pointer moves clockwise or counter-clockwise, which corresponds to shifting up or down, respectively. At the CSR element where the pointer is activated, the TC-CNT increases or decreases its value according to *UP* or *DN* signal. If the RA-CMP triggers *EN_FAST* due to a large

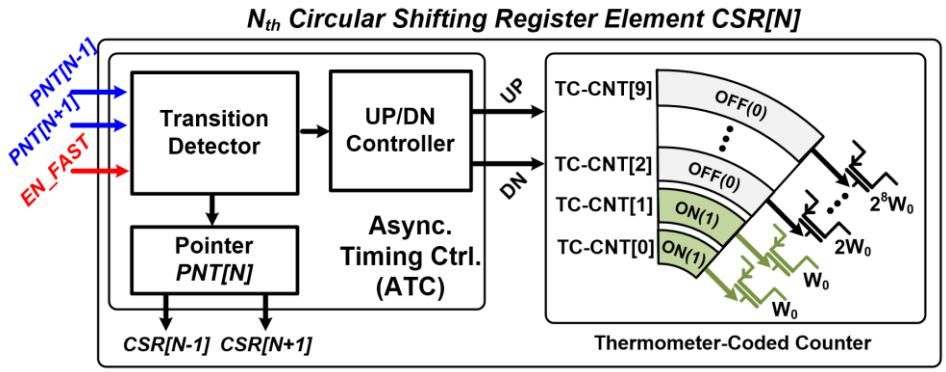

Fig. 3.6 Block diagram of the CSR element.

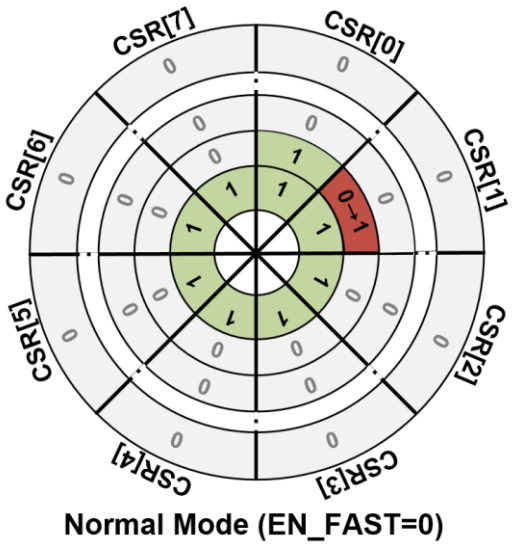

Fig. 3.7 Block diagram of 2D-CSR operation in normal mode.

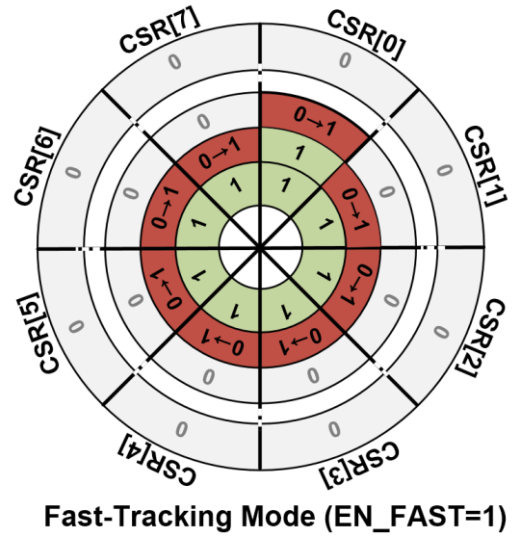

Fig. 3.8 Block diagram of 2D-CSR operation in fast-tracking mode.

output variation, all elements in the 2D-CSR are updated at once in increment or decrement, as shown in Fig. 3.7 and Fig. 3.8. The fast-tracking mode can increase or decrease the current by double considering the previous regulation. Thus, the ALSC realizes a boosted recovery from the voltage droop without critical undershoot or overshoot. At this time, the regulation speed of the ALSC is mainly determined by the number of updated elements and logic delay per searching step. Considering stability of the DLDO, the maximum number of updated elements is designed as eight during the fast-tracking mode. The post-layout simulated logic delay per update is about 1ns at V_{IN} of 1V, realizing fast regulation speed without use of several GHz clock.

3.2.3 SBSC with Subrange Successive-Approximation Register

The SBSC is implemented by a 10b Sub-SAR, as shown in Fig. 3.9. At the start of the SBSC, *TC-CNT[9:0]* in *CSR[0]* is transferred to the Sub-SAR. As illustrated in Fig. 3.10, when *TC-CNT[*CNT_{MSB}*:0]* has turn-on bits ("1"), the Sub-SAR conducts the binary search from CNT_{MSB} to 0 instead of a fixed number of steps. In this way, the Sub-SAR adaptively adjusts a full-range of the successive approximation according to the ALSC status. The subrange operation provides a faster binary search by eliminating the overflow bit, thus reducing undershoot or overshoot during the trial-and-comparison procedure, as shown in Fig. 3.11.

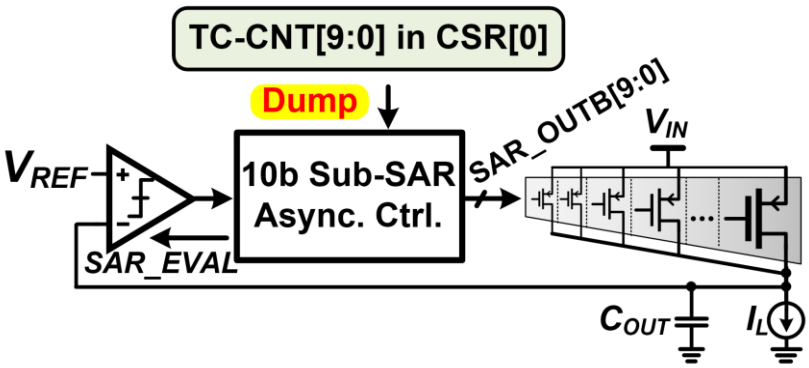

Fig. 3.9 Block diagram of the SBSC.

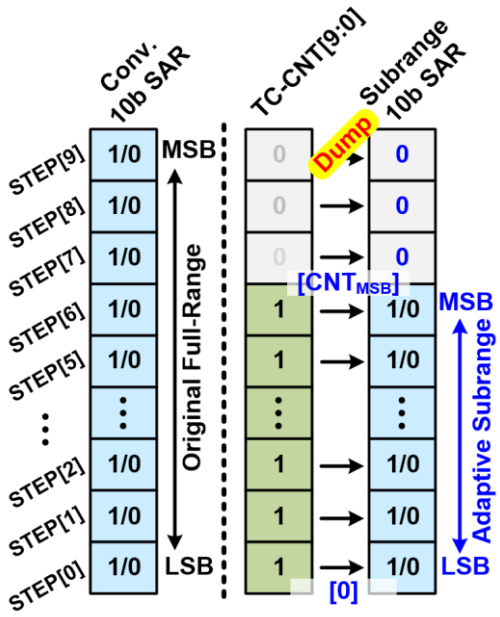

Fig. 3.10 Operational principles of subrange-decision procedure.

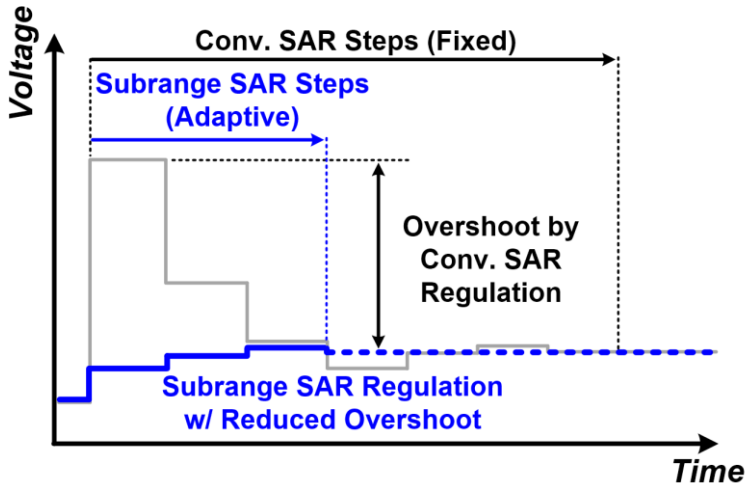

Fig. 3.11 Operational principles of adaptive subrange SAR regulation.

3.2.4 Stability Analysis

Fig. 3.12 shows the discrete-time DLDO model and open-loop transfer function. The DLDO control model is constructed with RA-CMP, ALSC, SBSC, zero-order hold (ZOH), and continuous-time output stage. F_{CLK} and F_{OUT} are the equivalent operating frequency of the control model and output stage pole, respectively. The DC gain K_{DC} comes from current conversion ratio of the output stage. The RA-CMP is modeled with a comparator considering the detection delay which is the same range with logic delay in the following digital controller. The ALSC and SBSC are modeled with K_{SR} and K_{SAR} which represent gains of each control stages, respectively. Using the discrete-time model, stability of the DLDO is analyzed as shown in Fig. 3.13 ~ Fig. 3.16. With the load current I_{LOAD} of 10mA and 100mA conditions, pole analyses versus K_{SR} and K_{SAR} are conducted. According to the design of the ALSC and SBSC, K_{SR} and K_{SAR} are not larger than eight and two, respectively. In those K_{SR} and K_{SAR} ranges, the DLDO shows stable operation as shown in Fig. 3.13 ~ Fig. 3.16.

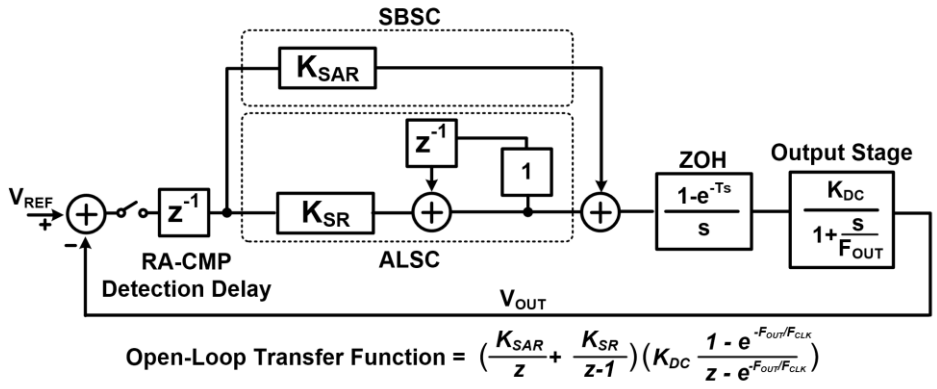

Fig. 3.12 Discrete-time DLDO control model.

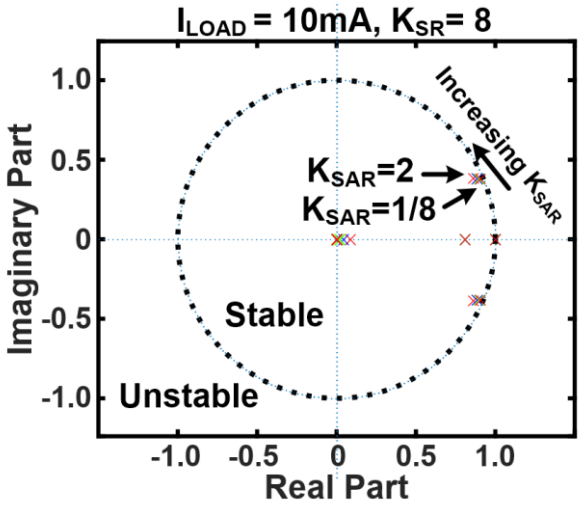

Fig. 3.13 Pole plots of the DLDO model at I_{LOAD} of 10mA and 100mA across K_{SR} and K_{SAR}(1).

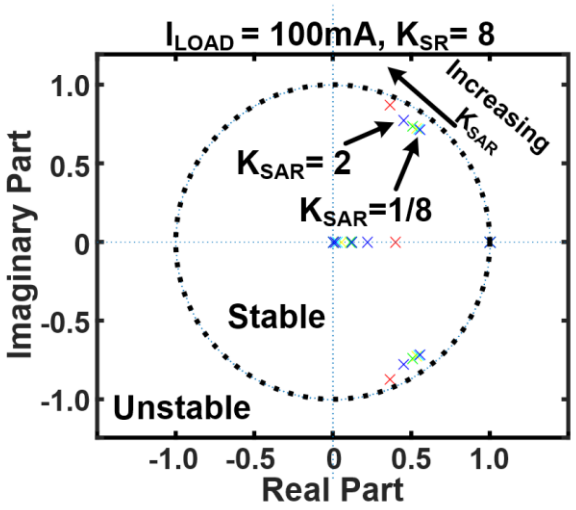

Fig. 3.14 Pole plots of the DLDO model at I_{LOAD} of 10mA and 100mA across K_{SR} and K_{SAR}(2).

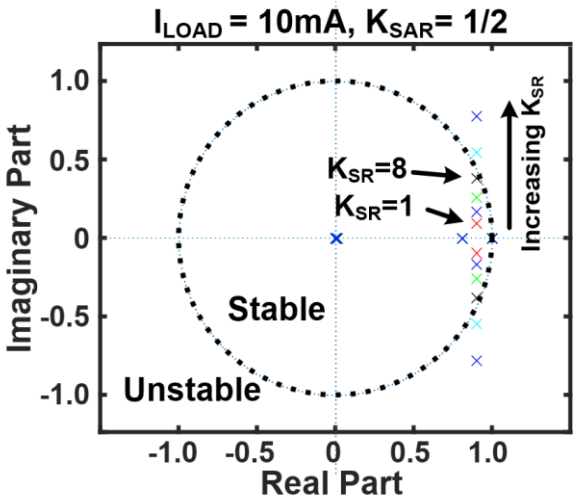

Fig. 3.15 Pole plots of the DLDO model at I_{LOAD} of 10mA and 100mA across K_{SR} and K_{SAR}(3).

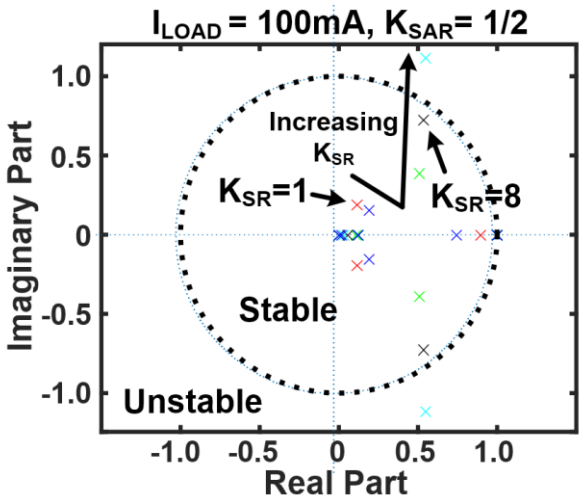

Fig. 3.16 Pole plots of the DLDO model at I_{LOAD} of 10mA and 100mA across K_{SR} and K_{SAR}(4).

3.3 Circuit Implementation

3.3.1 Time-Interleaved Ring-Amplifier-Based Comparator

Fig. 3.17 shows the schematic of 1.5b RA-CMP that compares V_{OUT} with V_{REFH} and V_{REFL}. Each comparator is implemented with time-interleaved ring amplifiers to offer a seamless conversion [25]. When V_{ERR} exceeds a boundary range from $V_{ERR,L}$ to $V_{ERR,H}$, *EN_FAST* is activated, and the ALSC conducts fast-tracking regulation. Out-of-range detection of V_{ERR} is realized by trip-point programmable inverters (TPP-INV) [60] that provide continuous-time detection.

The RA-CMP can operate with auto-zeroing frequency F_{AZ} ranging from 10 kHz to 100 MHz. The F_{AZ} can be determined depending on available clock frequency, power-supply rejection bandwidth, or V_{REF} tracking speed. Fig. 3.18 and Fig. 3.19 show Shmoo plots indicating operation of the RA-CMP when supply ripple is injected with frequency range from 1 kHz to 100 MHz and amplitude range from 20 to 200 mV_{PP}. If the RA-CMP generates *UP* or *DN* signals due to the power-supply ripple at the given amplitude and frequency, the corresponding ripple injection condition is marked as "*Fail*". Because of the auto-zeroing process in the RA-CMP, higher F_{AZ} offers more robustness to the power-supply ripple [25]. Therefore, the F_{AZ} can be chosen depending on the required power-supply-rejection (PSR) performance of the DLDO. Fig. 3.20 shows the Monte Carlo simulations of the RA-CMP detection delay with 500 trials. Under the global process variation and local mismatch effect, the RA-CMP

maintains fast detection delay below 1ns, which ensures robustness to the process variation. To examine a sensitivity to temperature variation, the detection delays of the RA-CMP are simulated by varying operating temperature from -30 ℃ to 100 ℃ as shown in Fig. 3.21. The simulated detection delay ranges from 0.6 ns to 0.76 ns, which guarantees the RA-CMP operation within the wide temperature range.

Fig. 3.17 Circuit implementation of the RA-CMP.

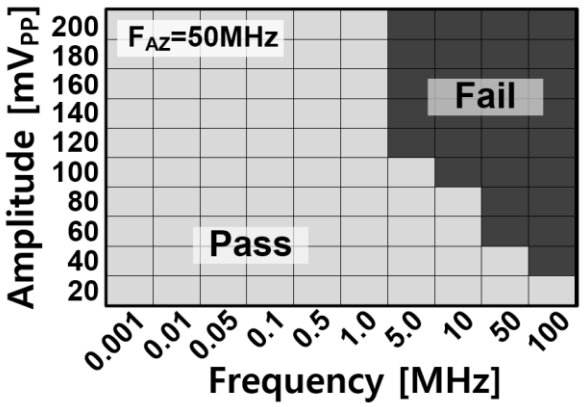

Fig. 3.18 Simulated Shmoo plots for supply-ripple sensitivity of the RA-CMP at F_{AZ} = 50 MHz.

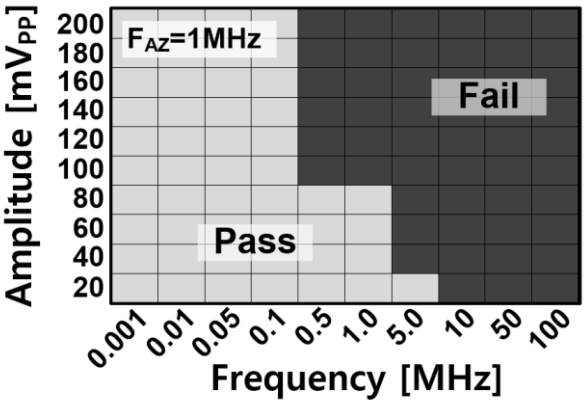

Fig. 3.19 Simulated Shmoo plots for supply-ripple sensitivity of the RA-CMP at F_{AZ} = 1 MHz.

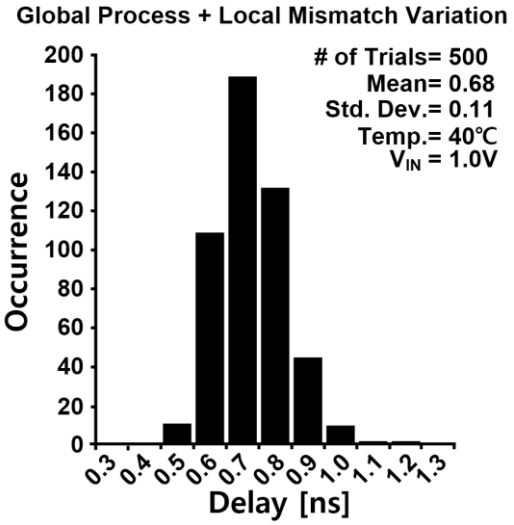

Fig. 3.20 Monte Carlo simulation of the RA-CMP detection delay under global-local process variation with 500 trials.

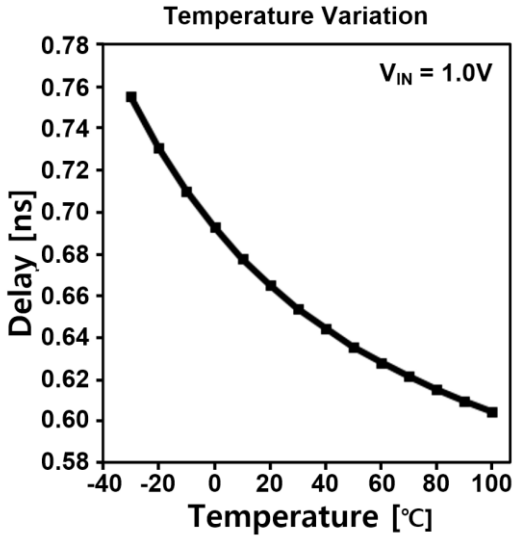

Fig. 3.21 Simulated detection delay of the RA-CMP versus temperature.

3.3.2 Asynchronous 2D Circular Shifting Register

Fig. 3.22 shows the circuit implementation of the 2D-CSR element. The 1b pointer and 10b TC-CNT are implemented using a C-element that offers asynchronous operation. The ATC in *CSR[N]* updates their pointer and TC-CNT by detecting transitions in adjacent *CSRs* while *UP* or *DN* signal is activated. However, the fast-tracking mode can cause a limit-cycle oscillation (LCO) due to propagation delay in the ALSC. To

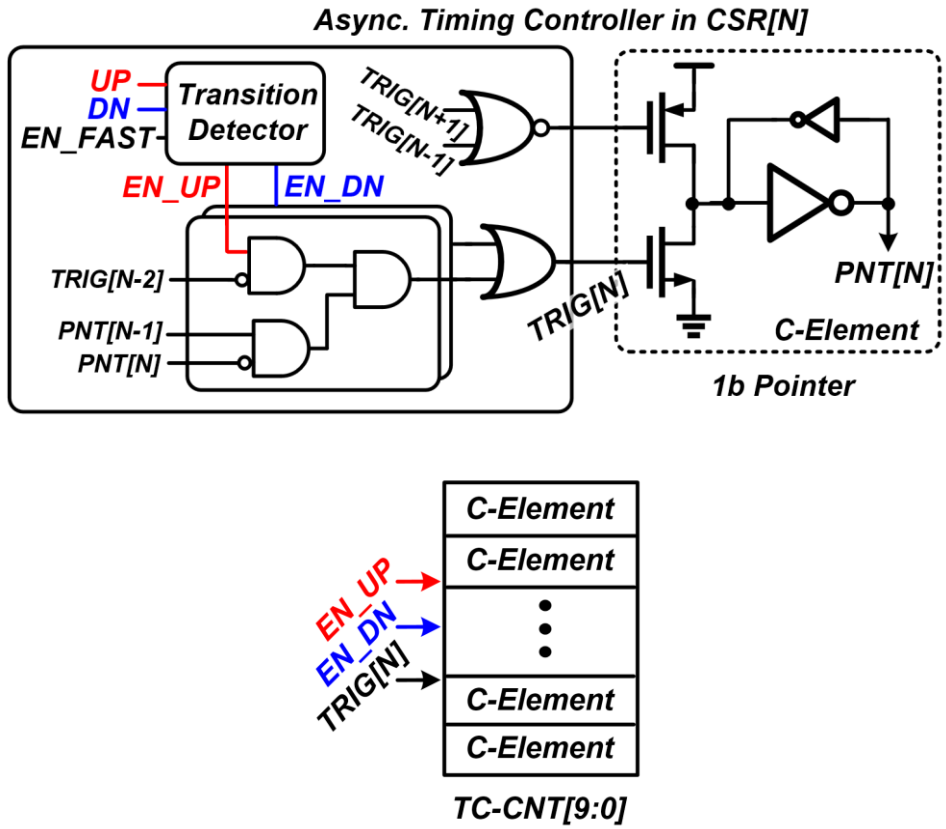

Fig. 3.22 Circuit implementations of the 2D-CSR.

prevent the LCO that alternates *UP* and *DN* signals, an LCO detector is realized with cascaded flip-flops triggered by *UP* or *DN* in sequence, as shown in Fig. 3.23. The number of allowed *UP*/*DN* oscillations can be programmable via *OSC[3:0]*. When the LCO detector activates *EN_LOCK*, the fast-tracking mode is forced to be turned off, and the ALSC can exit from the LCO.

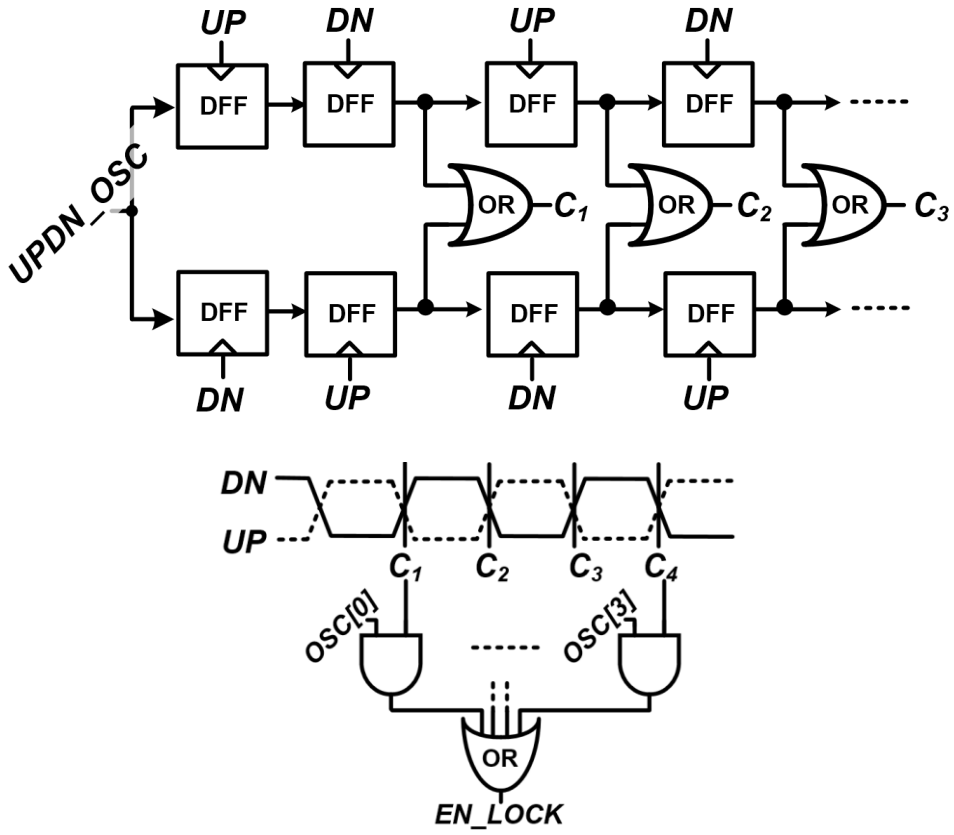

Fig. 3.23 Circuit implementations of the limit-cycle-oscillation detector.

3.3.3 Subrange Successive Approximation Register

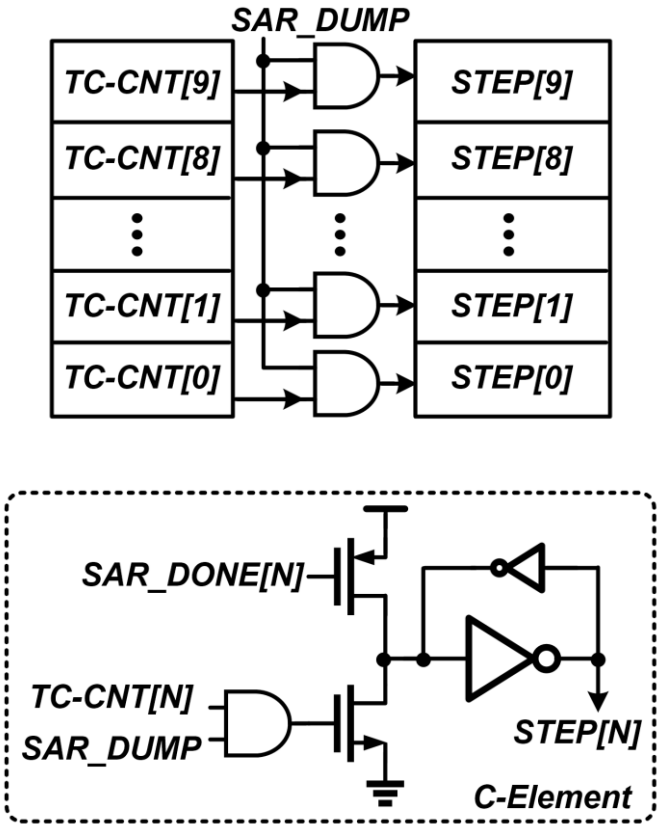

Fig. 3.24 Circuit implementations of the adaptive subrange register.

Fig. 3.24 shows the implementation of the asynchronous 10b Sub-SAR. The subrange operation is realized by dumping 10b *TC-CNT[9:0]* of *CSR[0]* into *STEP[9:0]*, which is a 10b C-element register for indicating the binary-search step. The overflow bits are initiated to turn-off bit (“0”) and the subrange bits are initiated to turn-on bit (“1”) for the following trial-and-comparison procedures. Fig. 3.25 and

Fig. 3.26 show the SAR control logic and its timing diagram. If the boundary of turn-on and turn-off bit in *STEP[9:0]* is *STEP[N]*, the SAR controller performs the binary search by activating *SAR_EVAL[N]*, which triggers a Strong-Arm latch comparator.

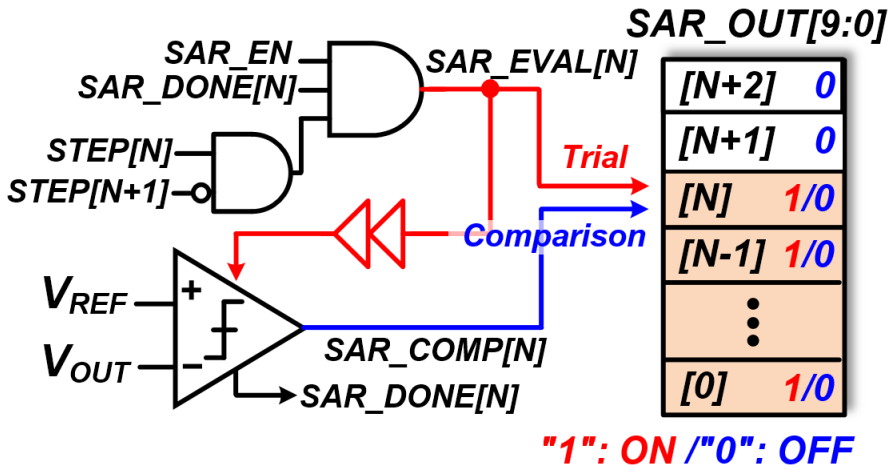

Fig. 3.25 Circuit implementations of the SAR control logic.

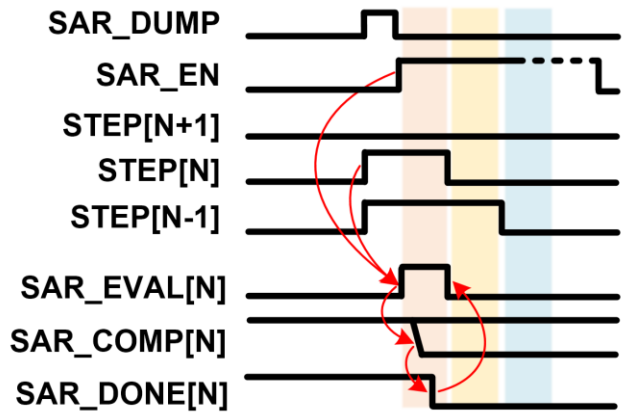

Fig. 3.26 Timing diagram of the asynchronous Sub-SAR operation.

After the trial-and-comparison procedures, the SAR output register *SAR_OUT[N]* is updated according to the comparator output *SAR_COMP[N]*. Then, *SAR_DONE[N]* and *STEP[N]* are disabled and the next searching step is conducted at *STEP[N-1]* stage. In this way, the Sub-SAR realizes the asynchronous operation and the adaptive number of search steps.

3.4 Mesurement Results

The prototype of the proposed DLDO is fabricated in a 40nm CMOS process. Fig. 3.27 shows the die photomicrograph of the prototype. The fabricated DLDO occupies an active area of 0.062 mm^2 that includes an on-chip output capacitor of 150 pF. The DLDO supports input voltage V_{IN} ranging from 0.6 to 1.2 V at a dropout V_{DO} of 5 0 mV. The measured quiescent current and current efficiency versus V_{IN} are shown in Fig. 3.28. The DLDO achieves peak current efficiencies better than 99.7 % across the entire V_{IN} range. In the measurements, an 1 MHz clock is applied to the RA-CMP for the time-interleaved operation, and other blocks did not use any clock source. Fig. 3.29 shows the power breakdown of the overall DLDO at V_{IN} of 1.0 V and F_{AZ} of 1 MHz. Owing to the asynchronous operation, the ALSC and SBSC consume only 11.1 %

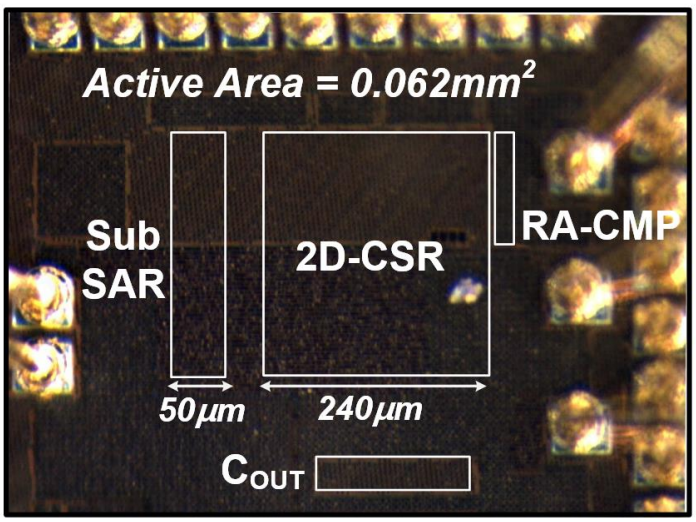

Fig. 3.27 Die photomicrograph of the fabricated DLDO.

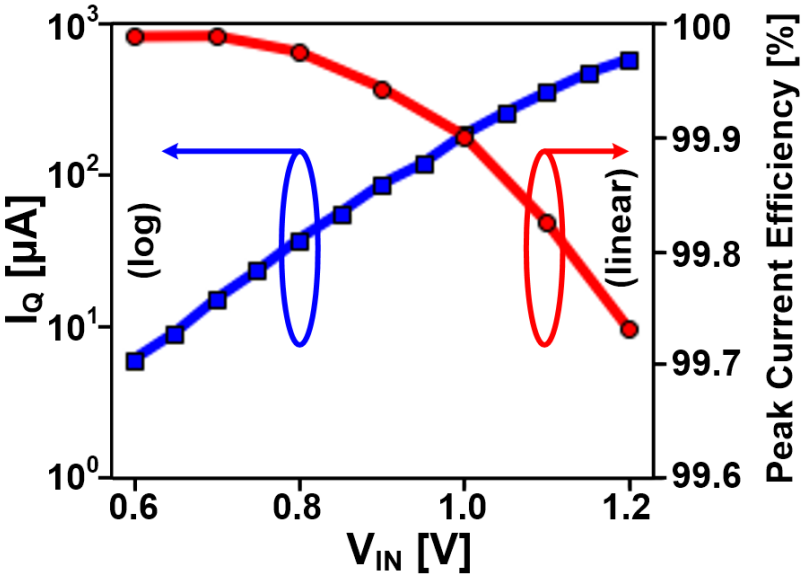

Fig. 3.28 Measured quiescent current and peak current efficiency versus input voltage V_{IN}.

and 5.9 % of quiescent current. The RA-CMP occupies 83% of the entire quiescent current. Depending on the input voltage V_{IN}, the current consumption of the RA-CMP can be scaled efficiently as shown in Fig. 3.30.

Fig. 3.31 and Fig. 3.32 show the measured load transient responses. At a V_{IN} of 1 V, a load current step of 104.2 mA is applied within an edge time T_{Edge} less than 1 ns. The DLDO achieves a droop recovery time $T_{Recovery}$ of 6ns and a settling time $T_{Settling}$ of 15ns. The voltage droop V_{Droop} is measured as 140 mV. At a V_{IN} of 0.6 V with a load step of 28.2 mA, the DLDO achieves a $T_{Recovery}$ of 28 ns and a $T_{Settling}$ of 45 ns. Fig. 3.33 and Fig. 3.34 show the comparison of load transient responses depending on

the fast-tracking mode in the ALSC. At V_{IN} of 1.0 V, $T_{Recovery}$ are significantly improved by the fast-tracking mode. Fig. 3.35(a) and Fig. 3.35(b) show the measured load regulation and line regulation across the V_{IN} range, respectively. The two-step searching procedure achieves not only the fast droop recovery but also accurate regulation. Fig. 3.36 shows the post-layout simulation results of the PSR at F_{AZ} of 1, 10, and 50 MHz. The PSR can be improved by increasing F_{AZ}. The PSR is less sensitive to the load current I_{LOAD}, and the DLDO can maintain the PSR even if the load current is increased to full load condition. Table 3.1 shows the performance summary and comparison with other works [49][59][61][62]. The proposed DLDO achieves highly improved transient responses of $T_{Recovery}$ and $T_{Settling}$, providing a fast droop recovery for advanced memory systems.

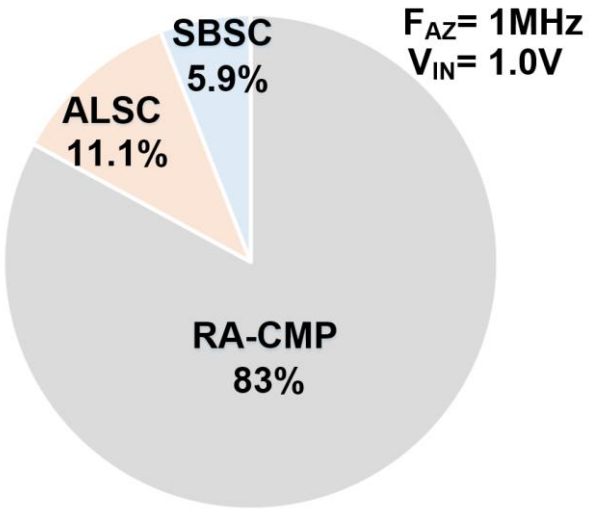

Fig. 3.29 Simulated power breakdown of the DLDO.

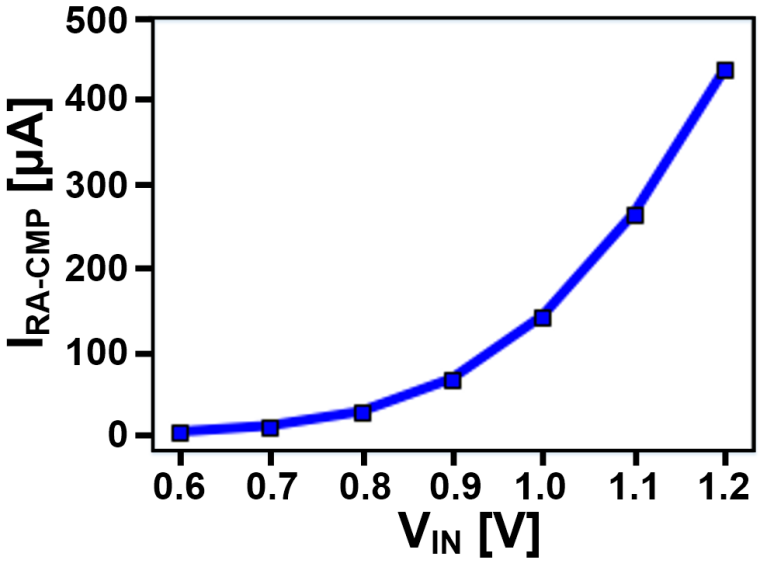

Fig. 3.30 Simulated current consumption of the RA-CMP versus input voltage V_{IN}.

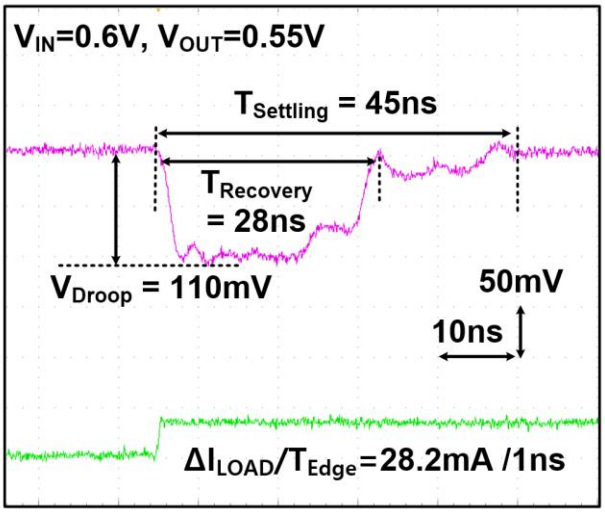

Fig. 3.31 Measured load transient responses at V_{IN} of 0.6 V.

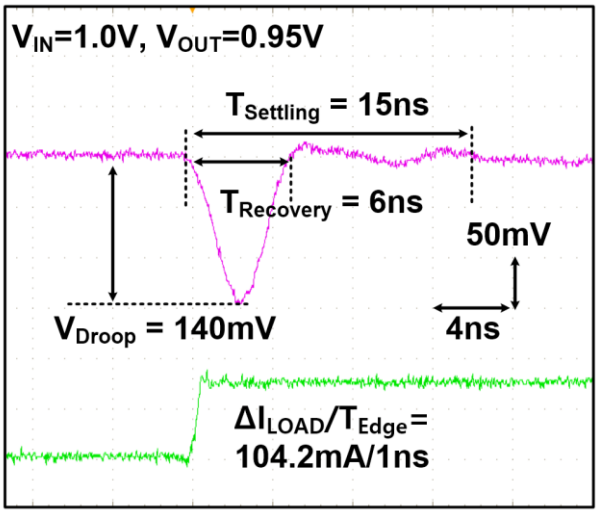

Fig. 3.32 Measured load transient responses at V_{IN} of 1.0 V.

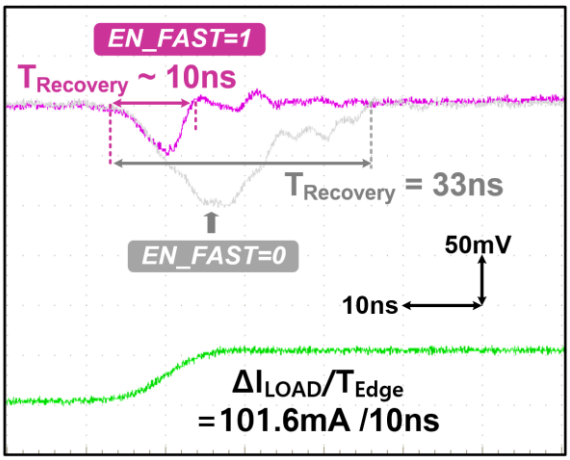

Fig. 3.33 Measured load transient improvements by fast-tracking mode with load steps of 101.6mA/10ns at V_{IN} of 1.0V.

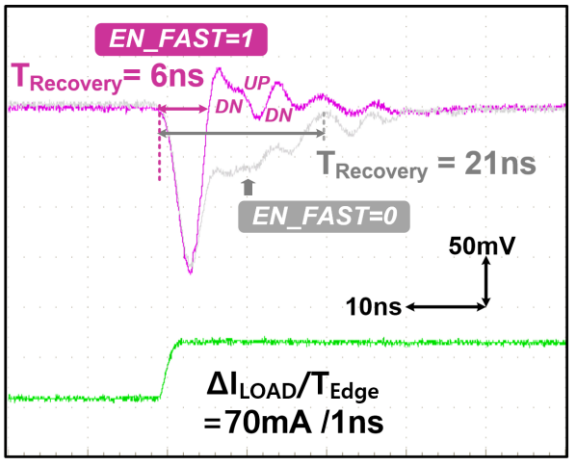

Fig. 3.34 Measured load transient improvements by fast-tracking mode with load steps of 70mA/1ns at V_{IN} of 1.0V.

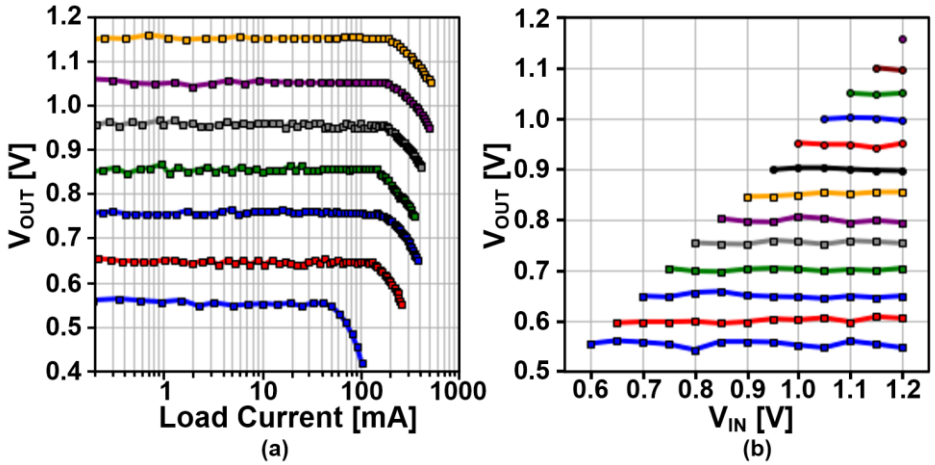

Fig. 3.35 Measured (a) load regulation and (b) line regulation.

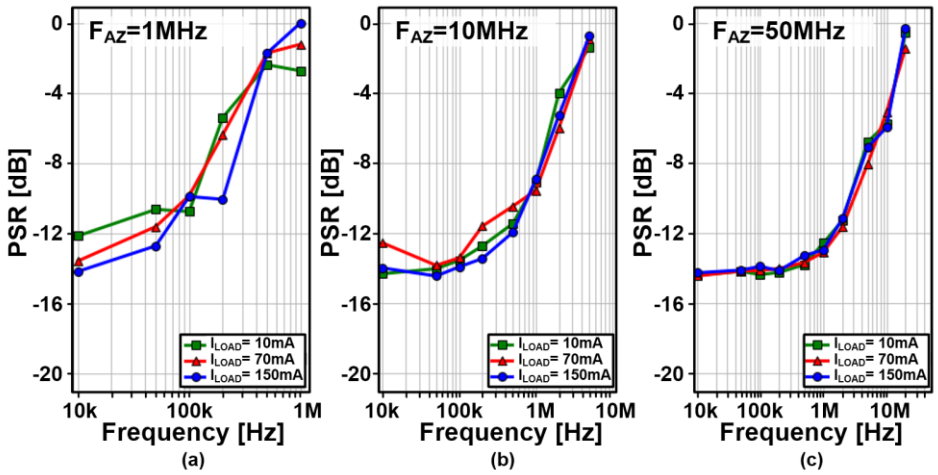

Fig. 3.36 Post-layout simulated PSRs at F_{AZ} of (a) 1MHz, (b) 10MHz, and (c) 50MHz.

Table 3.1 PERFORMANCE SUMMARY AND COMPARISON

	[49] ISSCC 2019	[59] JSSC 2018	[61] TPE 2020	[62] TPE 2021	This work
Technology [nm]	65	65	130	110	**40**
Operating Type	Digital Time-Driven	Digital Time-Driven	Digital Time-Driven	Digital Time-Driven	**Digital Event-Driven**
f_{CLK} [MHz]	16-100	1-240	250	100	**1**
Search Type	Computational	Binary/ PD/PWM	Adaptive	Variable Step-Size	**Adaptive Linear-Binary**
V_{IN} [V]	0.65-1.15	0.5-1	0.5-1.22	0.8-1.2	**0.6-1.2**
V_{OUT} [V]	0.6-1.1	0.3-0.45	0.35-1.17	0.7-1.1	**0.55-1.15**
$I_{LOAD,MAX}$ [mA]	16.3	2	145	50	**200**
C_{LOAD} [nF]	0.25	0.4	1.5	0.04	**0.15**
I_Q [µA]	80-1200	14	3200	188.8-197.9	**6-550**
$T_{Recovery}$ [ns] @ V_{IN}, f_{CLK}	N/A	N/A	N/A	67 @ 1V, 100MHz	**6 @ 1V, 1MHz**
$T_{Settling}$ [ns] @ V_{IN}, f_{CLK}	27.9 @ 1.1V, 100MHz	100 @ 0.5V, 100MHz	55 @ 0.98V, 250MHz	N/A	**16 @ 1V, 1MHz**
ΔV_{Droop} [mV] @ $\Delta I_{LOAD}/T_{Edge}$	46 @ 5.6mA/0.1ns	40 @ 1.06mA/1ns	280 @ 40mA/0.1ns	360 @ 47.5mA/1ns	**140 @ 104.2mA/1ns**
Peak Current Efficiency [%]	99.7	99.8	97.8	92.98-99.61	**> 99.7**
FoM$_1$ [ps] *	29.3^+	199^+	63.9^+	1.26^+	**5.36**
FoM$_2$ [ps] **	N/A	N/A	N/A	107.2	**1.527**

* **FOM$_1$ =** $T_R (I_Q/\Delta I_{LOAD})$, $T_R^+ = C_{LOAD} (\Delta V_{Droop}/\Delta I_{LOAD})$ *at* $T_R >> T_{EDGE}$, T_R *=Response time*

** **FOM$_2$ =** $T_{Recovery} (\Delta V_{Droop}/V_{OUT})(I_Q/\Delta I_{LOAD})$. *[M.A. Akram, IEEE JSSC 2019]*

Chapter 4

A Fast Transient Response Digital Low-Dropout Regulator with Slope-Detector-based Multi-Step Control for Digital Load Application

4.1 Overview

LDO is an efficient power regulator in SoC design and a key block that affects overall system performance. In particular, the integrated digital low-dropout regulator (DLDO) is easily used because it does not require passive devices. Recently, DLDO has been improving several performance indicators with various architectures. For

example, event-driven DLDO has an advantage in fast activation speed, and computational DLDO obtains a short setting time by reducing the number of times the feedback loop operates. However, real-time reflection of sudden current consumption by digital clocks over several tens of MHz requires achieving both time-wise performance and voltage-wise performance.

In this Chapter 4, the fast transient response DLDO employing a slope detector and a bi-directional latch-based driver is presented. Short response time and settling time are achieved with the optimization of the loop activation process by CMP-based oscillators and LUT-based shift register. Furthermore, not only reduce activation time, but also reduce voltage droop and recovery time by performing slew-rate-based compensation. Thanks to these features, the presented DLDO settled to a target voltage less than 5 ns.

4.2 Proposed Digital LDO

4.2.1 Motivation

LDO is a power converter that supplies stable voltage and current in many sub-block units. In particular, DLDO is often used in SoC or core processors that require dynamic voltage frequency scaling (DVFS) to reduce power consumption because of its advantage in low-voltage operation [36], [63]. In other words, DLDO is chosen when reliable supply power is required during periodic transition situations. There are two critical factors in tracking load current changes that are repeated at the same time interval. First, the ability to respond quickly to instantaneous voltage drops, and second, the load voltage must be stabilized before the next event occurs. Recently, many methods have been proposed for DLDO to respond quickly to voltage drops and take control actions. Among them, feedforward compensation shows good performance in terms of fast transient response, with other loops that can detect drops in addition to the main loop. In general, DLDO's main loop has a delay in accepting significant changes in the input and controlling the pass gate for feedback. This delay is a relatively long time compared to the fast loop added intentionally for the fast voltage drop. Therefore, feedforward methods operate strongly in high di/dt environments as fast as they can react. In addition, there is an advantage in stability issues since feedback does not occur and compensates for the drop event only once. However, there is also a disadvantage of the droop detector operating only once to compensate for the current. When the load current changes over a long time, it is hard to respond to the load

current variation that changes later because the control is handed over to the main loop after the feedforward compensation is initially made. For example, if the current drops slowly in the initial transition and then shows a sudden change, the drop detector will only catch the initial gentle interval and compensate for the corresponding amount. Therefore, the portion that makes up the voltage drop is more significant at the rear, but the corresponding drop is not compensated with the appropriate current at once. Instead, it is compensated by the main loop according to the clock cycle.

In order to achieve a fast response and recovery time of load voltage variation according to the load current transition speed, the delay until the main loop becomes active is minimized in the proposed DLDO. Also, in the process of minimizing it, a system that can detect load current transition speed and compensate for an appropriate value, like a droop detector, is established. In addition, the DLDO presents a fine-control loop that can achieve a fast setting time for the next load current event.

4.2.2 Architecture of Digital LDO

Fig. 4.1 shows the simplified structure of the proposed DLDO. DLDO consists of two loops: the main loop (including slew-rate-dependent controller and coarse loop controller) that operates first when a load variation occurs and the fine-control loop that operates later. Pass gate groups controlled by each loop are distinguished to effectively compensate for the load current when an event occurs. For example, the pass gate of the main loop is sized to compensate for a large amount of current, even with a slight change in the control code. In addition, the incremental regulation scheme [64] has been applied so that the following control codes significantly impact the voltage drop compared to the previous control code.

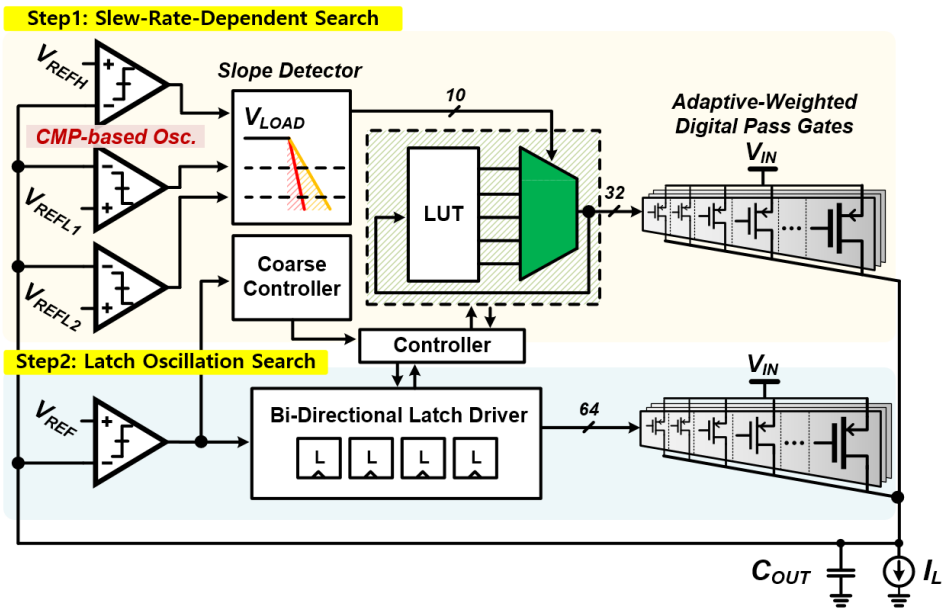

Fig. 4.1 Overall structure of proposed DLDO.

On the other hand, the fine-control loop is configured in the unary size to compensate for the remaining regulation errors and settle into a steady state. Also, the number of pass gates and control bits is 32 in the coarse loop and 64 in the fine loop, respectively. Finally, the comparator (CMP)-based oscillator, the starting point of each loop, used the same structure in both loops.

The proposed main regulation scheme of DLDO is a compensation method that quickly compensates for a moderate amount of current immediately after the event occurs, such as feedforward regulation [43]. However, it does not include a short-cut loop that can directly control the pass gate. Instead, the loop configuration is implemented to accommodate multiple feedback controls during the load current transition time by reducing the activation time of the coarse-control loop and adding a detector that can measure the current change amount. After the sudden change in load voltage by current transition, the coarse loop, which adjusts the control code one at a time, operates instead of the slew-rate-dependent compensation. The coarse loop helps the load voltage recover quickly near the target voltage after the drop stabilizes. In addition, the slew-rate-dependent compensation controller and the coarse loop controller are designed as one digital block to achieve area compactness. Both controllers use the LUT-based shift register by default to adjust the control code. Therefore, the activation time of the main loop can be reduced since the pass gate current can be changed immediately depending on the load change.

After the load voltage reaches the target voltage, the coarse-loop cycle is completed, and the regulation control is handed over to start the fine control loop. The DLDO has a comparator that receives the target and load voltage as inputs to detect reaching. The fine-control loop uses the bi-directional latch-based driver to achieve low regulation

error and obtain fast setting time. The bi-directional latch-based driver consists of 64 drivers [54] connected in series. Unlike [54], the activation direction of the latch is implemented in both directions. The proposed DLDO secured response time and setting time for fast transient response through these two loops.

4.2.3 Slew-Rate Dependent Coarse-Control Loop

Fig. 4.2 illustrates the detailed structure of the slew-rate dependent coarse-control (SDC) loop. This loop consists of the CMP-based oscillators, the slope detector, the coarse controller, and the LUT-based shift register. Among them, the coarse controller and the LUT-based shift register are written in digital code and synthesized using the auto P&R tool. The main operation of the SDC loop is divided into two.

First, the load current variation event type is detected using the slope detector. Load current variation is classified into the current flowing in the steady state, the current flowing after the event, and the edge time taken to generate the event. Since the steady-state current is a known value, the load current variation can be tracked by the logic circuit if the final current value and edge time are determined. Therefore, the

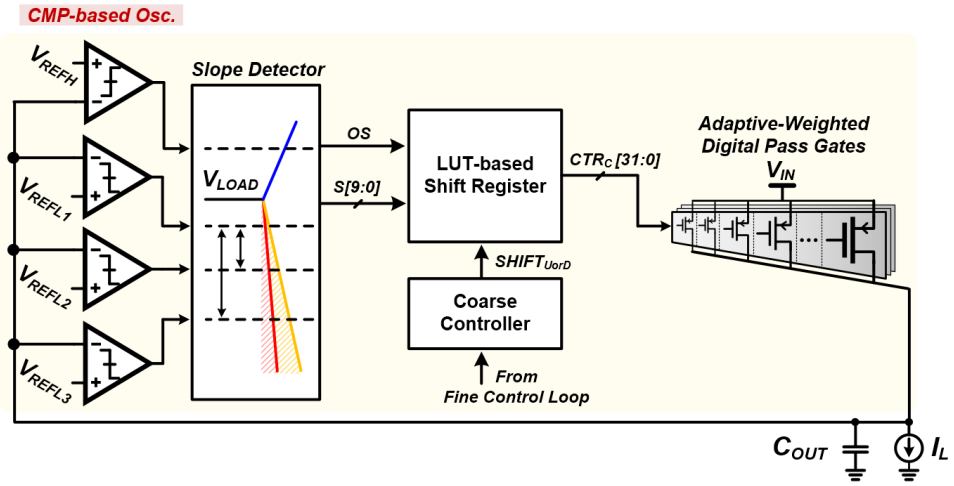

Fig. 4.2 Structure of SDC loop.

slew rate of the current changes is required to obtain these two values simultaneously. On the other hand, as previously represented in equation 2.10, the load voltage variation is proportional to the load current variation, so it is okay to track the voltage instead of the current that is difficult to sense. Therefore, the slope detector is designed to obtain information about the voltage variation per time in the load (output). The slope detector takes two reference voltages as inputs and outputs a signal when the load voltage exceeds both voltage levels. In addition, it subdivided the slope by measuring the time taken to go through two voltage levels. As a result, the slope detector divides the type of slope into 10 bits and selects the value to be shifted from the preconfigured LUT based on this information. In addition, since LUT is used, calculating the desired control code by processing the slew rate information is omitted. So the proposed DLDO activates the main loop more quickly than previous computing DLDO.

Next is the behavior of the coarse-control loop after the slope detector compensation. The coarse loop operates after completing one current adjustment according to the slew rate. The coarse loop determines whether the pass gate current should be up or down through the output of the CMP-based oscillator, comparing the target voltage with the current load voltage. Also, the loop transfers the control code to the pass gate using the same shift register as the slope detector. Meanwhile, even after the coarse loop starts to operate, the slope detector continues to detect the load voltage. The coarse loop changes one control code per one clock cycle. If the load current variation occurs faster than this, the slope detector can operate again to compensate for the pass gate current significantly. At this time, the value passed by the slope detector is the result of detecting the voltage slope again after the current compensation of the first

slope detector operation. On the other hand, these two different compensation methods, the slope detector, and the coarse-control loop use the same shift register to pass gates, so each command signal must not overlap. Therefore, supplement circuit is added to gate the signal so that the coarse-control loop does not trigger when the slope detector is operated.

4.2.4 Fine-Control Loop

Fig. 4.3 illustrates the detailed structure of the fine-control loop. The fine-control loop comprises the CMP-based oscillator with the bi-directional latch-based drivers, and the several logic gates for the controller. Except for the CMP-based oscillator, all blocks are written and synthesized in digital code. The primary purpose of this loop is to stabilize the load voltage perturbation by the load current variation to the target voltage. To achieve the main goal quickly, the proposed DLDO exploits a latch-based driver rather than a shift register conventionally used in DLDO. The existing shift register has been shifted to one control code per clock. However, due to the fine-control characteristics closely related to regulation accuracy performance, it is hard to use a fast clock or operate multiple control codes at one active signal. The latch-based driver has a fast activation transfer speed, even if it operates many control codes, allowing it to quickly reach the desired target code. Therefore, the proposed driver is designed to have a high bit resolution and reach the desired point quickly.

On the other hand, the driver turn-on signal does not turn off immediately even if the desired code is reached because it is configured as a latch. In this case, the driver

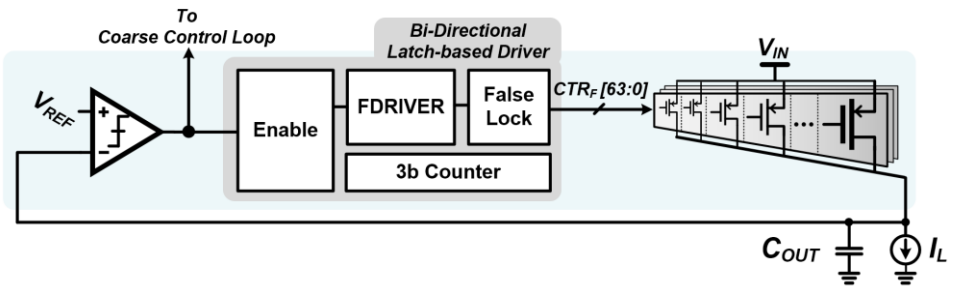

Fig. 4.3 Structure of fine-control loop.

activation stops at a code greater than or less than the desired code, leaving a regulation error. The bi-directional latch-based driver is proposed to solve this problem with a three-step speed control mechanism. It approaches the final control code at its slowest speed just before the load voltage is set. Finally, the controller receives a signal that the current load voltage is high or low based on the target voltage. If up or down signal is repeated, it is determined that the load voltage is set to the target voltage, and the regulation is complete. The detailed structure of fine-control driver is shown in Fig. 4.4.

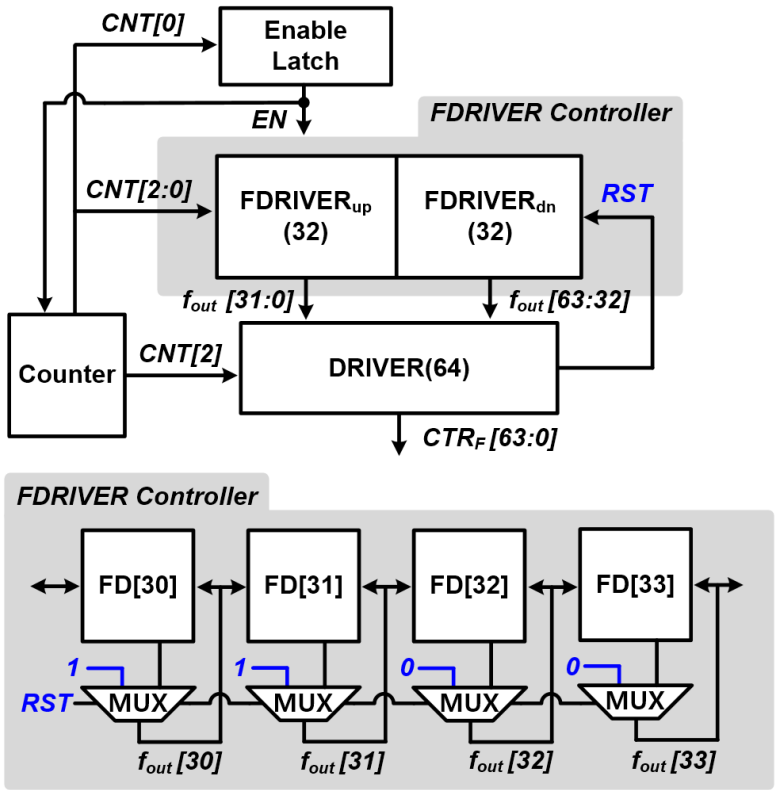

Fig. 4.4 Structure of fine-control driver.

4.2.5 Control for Load-Transient Response

In this section, the SDC and the fine-control loop algorithms are described above in the time domain. The load transient response to the load current step is shown in Fig. 4.5. This illustration represents a sudden drop that occurred in the load voltage, which exceeded the detection areas of the slope detector, V_{RefL1} and V_{RefL2}. CMP-based oscillators sample load voltage at GHz speed and compare it with reference voltages. Therefore, it is possible to send a signal to the LUT-based shift register within hundreds of ps after the load voltage crosses the lower reference line. As such, the first current compensation has a fast response time and supplies an appropriate amount of current to the pass gate. After the load voltage starts to recover, the situation is divided into two cases according to the load current variation. First, due to the compensation of the slope detector, the pass gate current is close to the final load current, and the voltage recovery has been made to some extent. Second, additional drops continue to occur even after the recovery, resulting in a drop in load voltage. In the first case, the control action of the slope detector provides sufficient current compensation, which leads to a canonical situation in which the coarse-control loop and fine-control loop operate sequentially. In the second case, load current variation is still more significant than the pass gate current despite the coarse-control loop being operated after the slope detector compensation to change the control code one by one per clock. In this case, the load voltage passes V_{RefL1} and V_{RefL2} again, creating an environment where the slope detector must operate again, and current compensation is made as much as the slew rate.

After the slope detector compensation, the fine-control loop also starts to operate. The pass gate turn-on signal is triggered since the load current is still larger than the pass gate current. On the other hand, the fine-control loop settles at an intermediate value of 64'hFFFFFFFF_00000000 when the reset signal is received. Therefore, the control code on the fine loop must be switched towards 64'h00000000_00000000. If the load voltage is recovered to the target voltage before all control codes are zero, it is the best case, but if not, DLDO needs to find a place to receive more current. At this point, the coarse loop operation starts. The proposed DLDO applied a false lock scheme. If the fine loop control code is stuck at both ends, i.e.,

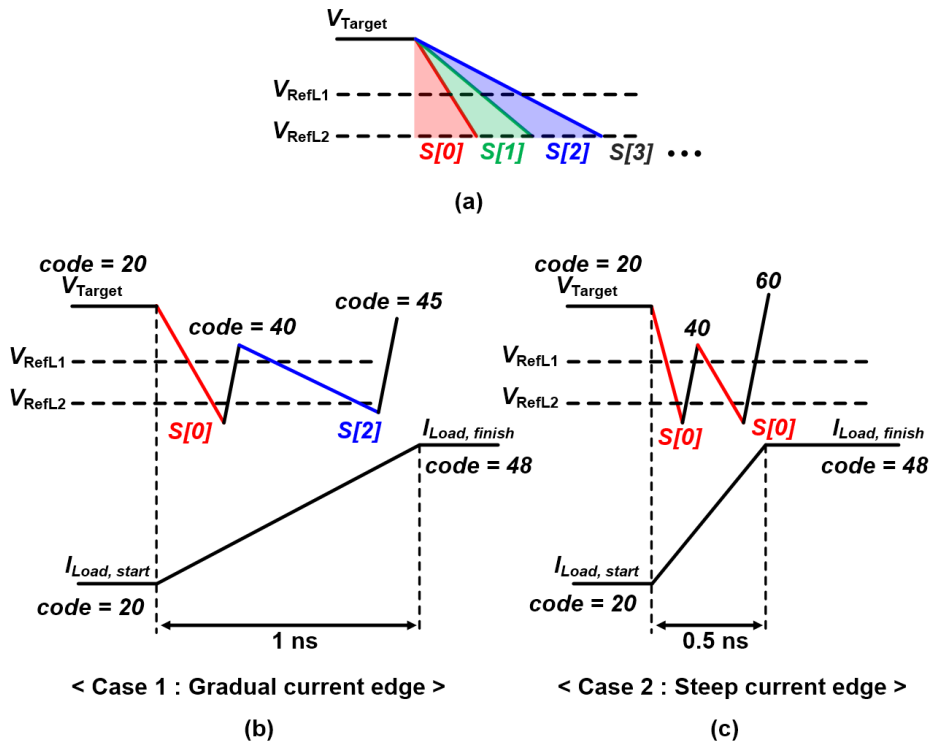

Fig. 4.5 Conceptual timing diagram of load current variation.

64'h00000000_00000000 or 64'hFFFFFFFF_FFFFFFFF, disconnect the latch driver of the fine loop from the pass gate. Instead, give the pass gate a replica code that copies the currently stuck code. After that, the control code of the fine loop is reset, and the coarse loop control code shifts depending on the stuck code. The fine loop also resumes operation according to the up and down signal from the comparator after the reset. However, the code is not transferred to the pass gate. When the coarse loop control code changes and the load voltage finally reaches the target voltage, the false stuck code is released from the pass gate. From then on, the control code transferred by the fine loop is applied, and the pass gate current is changed. After the fine loop is fully active again at the pass gate, the setting process is performed as described in section 4.2.4.

4.3 Circuit Implementation

4.3.1 Comparator-Triggered Oscillator Design

Basic clocked comparator structure receives a clock from a conventional oscillator. The basic comparator requires time from the input change to the output determination. So the output of the comparator is in the metastability state before the required time passes. If the clock that drives the comparator is too fast, sampling will occur at the next edge when the output is metastable. As a result, load and reference voltage cannot be appropriately compared with these sampled output values. In addition, it is difficult to adequately sample the comparator output with the clock of the conventional oscillator with a fixed period because the time when the output is trapped in the metasta-

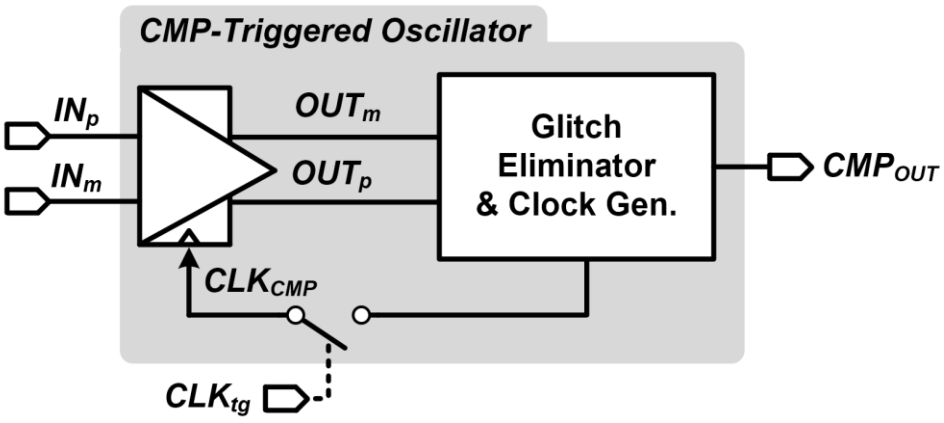

Fig. 4.6 Structure of CMP-based oscillator.

bility depends on the input or supply power voltage value. Therefore, to fundamentally avoid metastability, the oscillator must generate the clock frequency with enough margin. The inevitably required slow motion frequency is an important cause of the overall slowness of the loops in DLDO. Thus, a CMP-triggered oscillator has been proposed to mitigate the trade-off between metastability and DLDO operation speed [17]. The CMP-triggered oscillator design of the proposed DLDO is shown in Fig. 4.6. The oscillation path includes paths that cause the metastability of the comparator. Therefore, the closer the two input voltages the comparator compares, the longer it is stuck in metastability and the longer the oscillation cycle. This structure allows the comparator to operate at the maximum clock frequency for correct comparisons under the current conditions. The output of the comparator is received by the logic circuit directly following. This logic block operation includes removing glitches from the

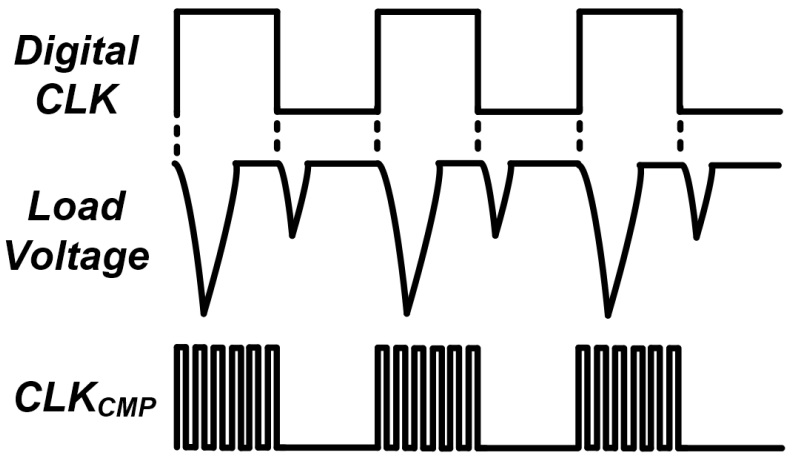

Fig. 4.7 Timing diagram of CMP-based oscillator and load voltage.

comparator output and oscillating the CLK_{CMP} using changes in the output values. The glitch eliminator and clock generation block are a simple combination of NOR and XOR gates, respectively.

Meanwhile, the proposed DLDO targets a load application operated by a digital clock. As shown in Fig. 4.7, a large load current variation occurs during the edge event of the digital clock, resulting in a significant load voltage drop or overshoot that can affect the overall system operation. It is possible to increase the energy efficiency of the power converter by identifying the phases that require regulation using this edge signal. Therefore, the CMP-triggered oscillator is designed to switch the clock path with an external trigger signal. Suppose the clock path is cut off, and the CMP-triggered oscillator stops operating. In that case, the entire loop of the DLDO stops together, which can increase power efficiency by consuming only quiescent current. In this DLDO, regulation can be performed by selecting positive or negative edges using an externally supplied digital clock as an input signal to CLK_{tg}.

Furthermore, the structure of the comparator used in the proposed DLDO does not need to be synthesized differently from [17], so a low-noise self-calibrating dynamic comparator [18] is used, which can operate quickly and obtain sampling acuity at the same time. The detailed structure of the dynamic comparator is shown in Fig. 4.8.

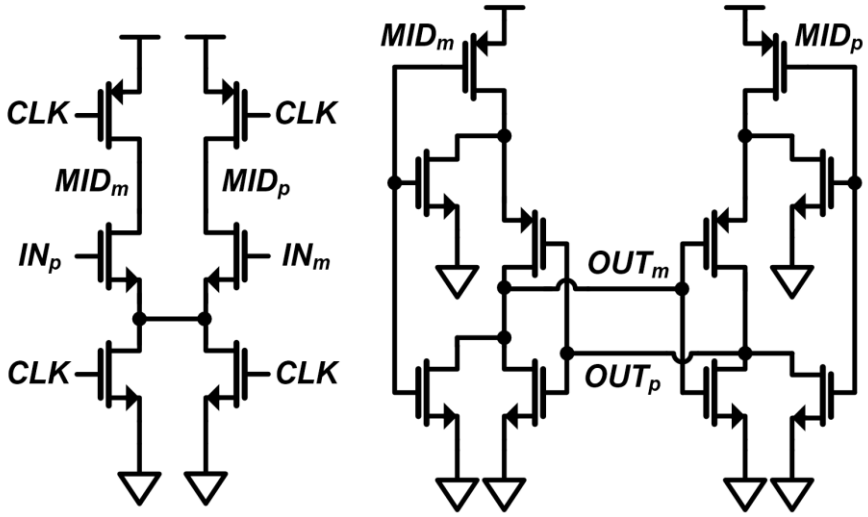

Fig. 4.8 Structure of low-noise dynamic comparator.

4.3.2 Slope Detector Design

Generally, in the time-driven DLDO architecture, the response to the load variation's performance is more challenging than in the event-driven design since the time-based design can only respond to the droop after a synchronous error detector operates with the clock signal. The disadvantage is that the time-driven scheme must have a high clock speed to obtain a fast response time. Therefore, [54] proposed a structure including a droop detector to respond faster to load variation using a time-driven design. However, this structure requires additional compensation paths in addition to the main regulation loop. Furthermore, it is not able to supply the amount of current that needs to be compensated.

In contrast, using a fast self-generated clock, the proposed DLDO with a time-driven scheme can quickly sample and obtain a large amount of changing load voltage information. The information obtained is the basis for accurately tracking changes in load current and compensating for the appropriate pass current. So the basis is included in the proposed DLDO implemented by the slope detector logic to realize this scheme.

As shown in Fig. 4.9, the slope detector consists of several D Flip Flops. By default, it performs a time-to-digital converter (TDC) operation. Fig. 4.10 shows the timing diagram of the internal signals of the slope detector as an example in one case where a load voltage droop occurs. First, the signal *C[0]* received from the CMP-triggered oscillator comparing REF_{L1} and load voltage operates the flip-flop by the clock of the slope detector. If the load voltage continues to drop and becomes lower than REF_{L2} after a certain period, *C[1]* is triggered. If *C[0]* is repeated for N cycles before *C[1]*

triggered, flip-flops triggered by *C[1]* each receive *T[N-1]* as an input to count it. Therefore, if *C[0]* passes two cycles at the time when *C[1]* is triggered, *T[0]* and *T[1]* change to 1 at each edge and remain at 0 from *T[2]*. Flip-flops with *T[0]* and *T[1]* as inputs perform sampling at the time when *C[1]* rises to 1, and at the same time, *S[0]* and *S[1]* change their values to 1. Likewise, *C[2]* is the output of a CMP-triggered oscillator comparing REF_{L3} and load voltage. *C[2]* is used as the clock of flip-flops that receive *T[3:0]* as input, such as *C[1]*. These flip-flops find that if more voltage drops occur during the same time interval compared to the flip-flop of *C[1]*, the slope is steeper than the *C[1]* group.

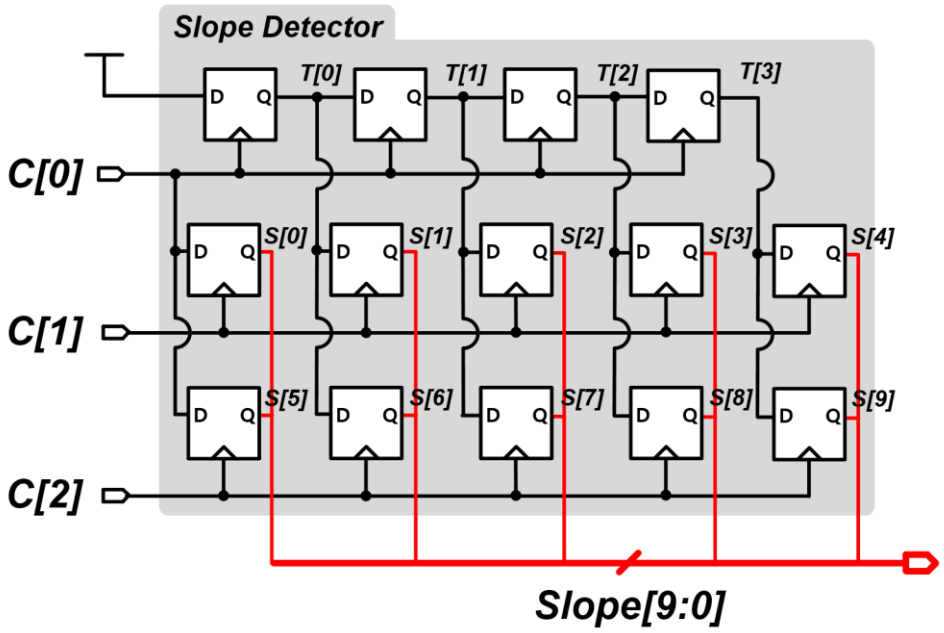

Fig. 4.9 Structure of slope detector.

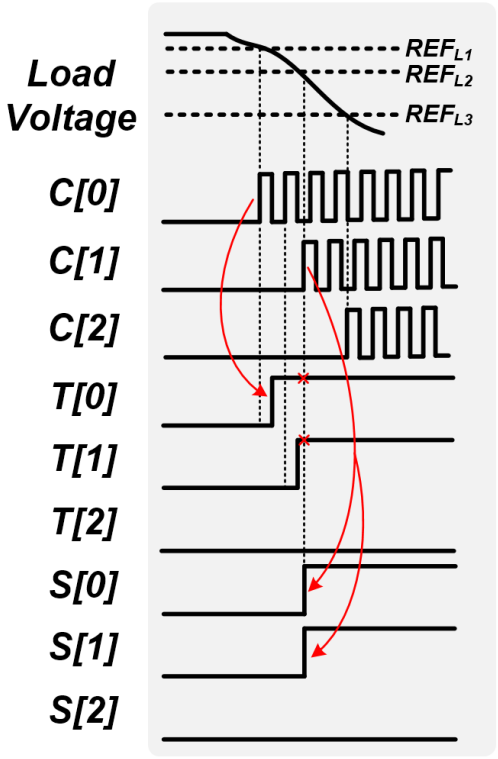

Fig. 4.10 Timing diagram of slope detector.

4.3.3 LUT-based Shift Register Design

Fig. 4.11 shows the structure of the LUT-based shift register (SR). The LUT-based SR consists of a preconfigured LUT, a register to store the control code, an os filter, and a clock generator. In addition, all of the internal functions are written in digital code and synthesized using the auto P&R tool. By default, the LUT-based SR functions as a block that finally outputs the control code CTR_C that activates the coarse pass gate. To perform this role, LUT-based SR accepts the *Slope[9:0]* from the slope detector and the shift signal of the coarse controller as input. The two signals make a trigger signal that causes the LUT-based shifter to prepare the shift required for the next operation while the clock generator starts the cycle of the SR.

Meanwhile, before the signal information is entered into the LUT-based shifter, it goes through OS filter logic. In this filter logic, a signal that determines overshoot is received as input and prioritized in addition to the slope and coarse control information. If the slope detector detects a significant load voltage change rate, it is applied to the LUT-based shifter in preference to the shift signal of the coarse controller. In addition, the information output from CMP-triggered oscillators compared to load voltage is clock gated according to the priority of the information because each of them functions as a trigger for the clock generator. If overshoot occurs, all output of the slope detector is blocked, and only the shift signal of the coarse controller and the fine loop control is set to the target voltage. Fig. 4.12 shows the detailed clock generator structure, which triggers the SDC and fine-control loop.

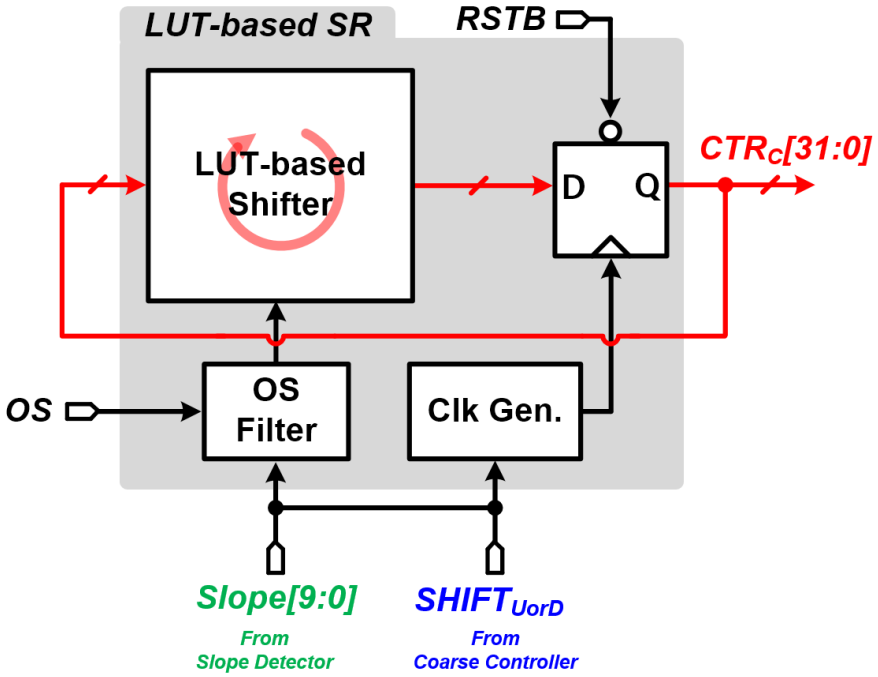

Fig. 4.11 Block diagram of LUT-based shift register.

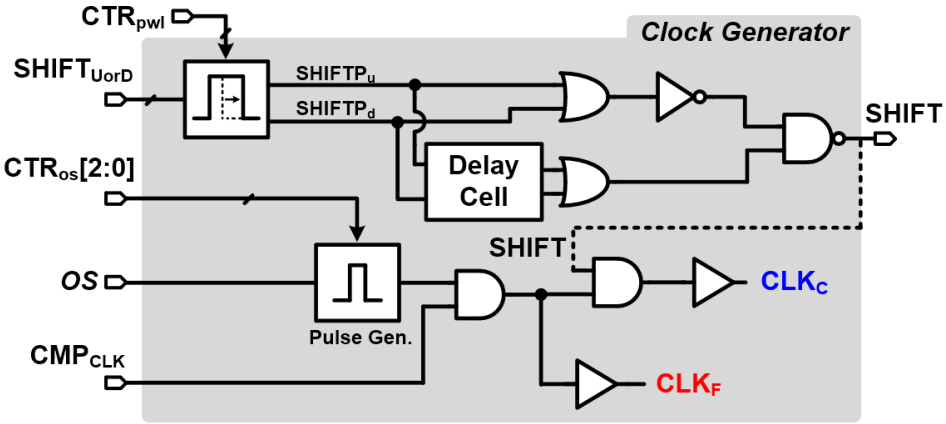

Fig. 4.12 Structure of clock generator.

4.3.4 Bi-Directional Latch-based Driver Design

The bi-directional latch-based driver included in the proposed DLDO is designed to replace the clock-based conventional shift register. The conventional shift register, which shifts one code per clock, consumes many clock cycles according to the initial code setting. Furthermore, unlike the previously introduced latch-based driver [54], the proposed driver is used for fine control, so the accuracy of settling in the desired code is additionally required. However, due to the nature of latch-based, it is hard to obtain a correct code unless sufficient loop bandwidth is supported with a high-speed

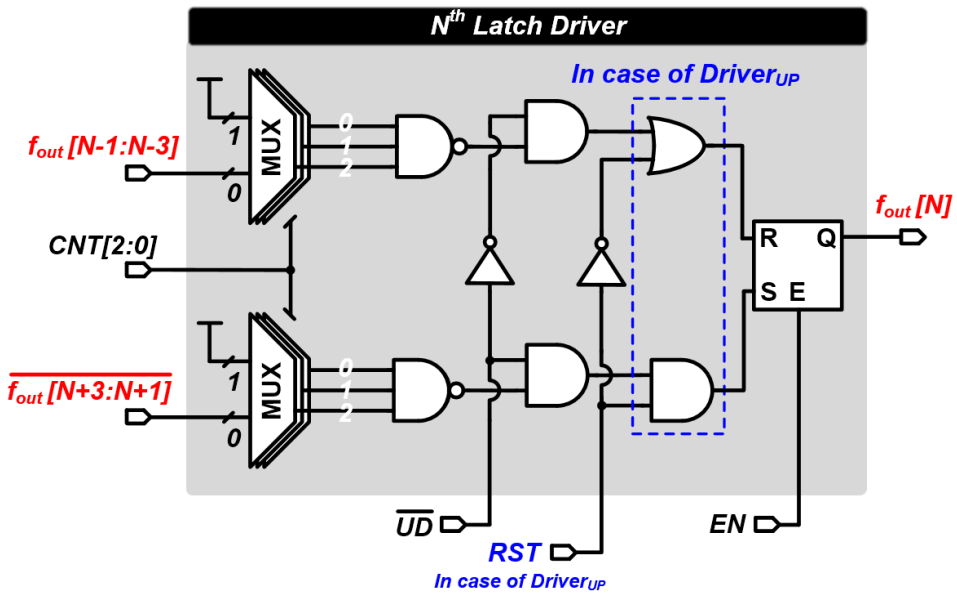

Fig. 4.13 Structure of Nth latch-based driver.

activation signal transition. Therefore, to solve this problem, the latch-based driver that can be transitioned on both sides and control the transition speed in the fine control loop is proposed.

The structure of the proposed bi-directional latch-based driver is shown in Fig. 4.13. The Nth latch driver (3 < N < 60, N is an integer) is compose of a sequential block of 64 latch drivers. In latch driver, SR latch is used to assign 0 or 1 to pass gate according to the signal at the front of DLDO. The signal *EN* that enables the SR latch starts to

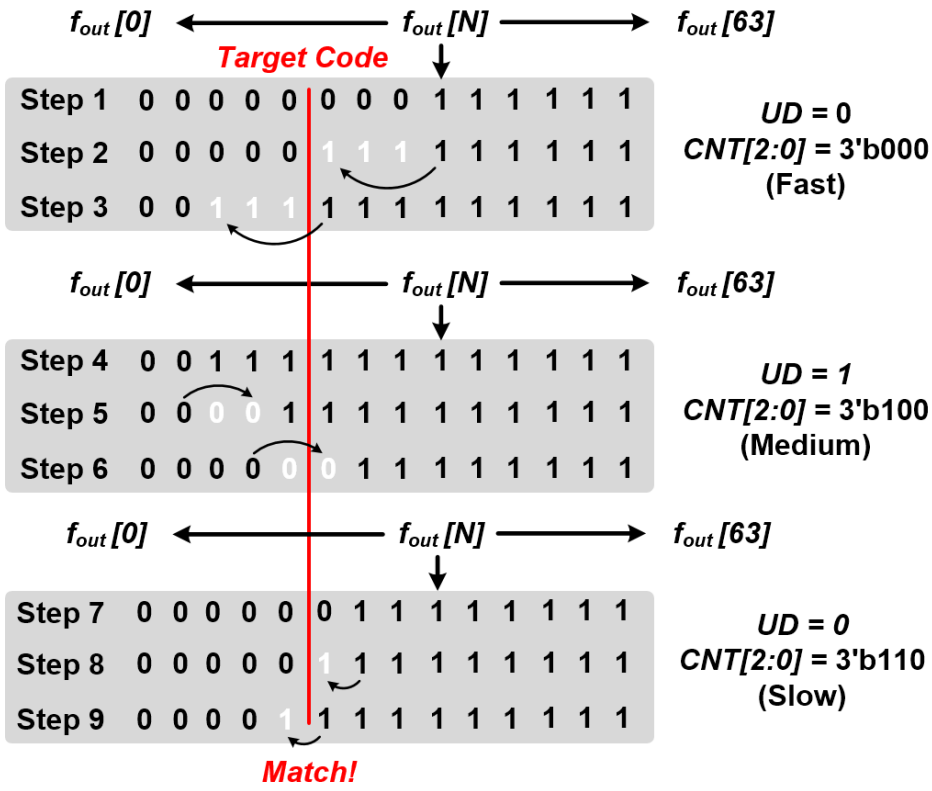

Fig. 4.14 Operation process of bi-direction latch-based drivers depending on UD and CNT.

becomes active after the compensation of the slope detector is made. The signals that determine set and reset of SR latch are computed by the output f_{out} *[N-1:N-3]* of the previous three latch drivers and the output f_{out} *[N+3:N+1]* of the subsequent three latch drivers, respectively. If the result of the CMP-triggered oscillator compares the target voltage and load voltage, *UD*, is 1, the reset path is enabled, and the set path is disabled. First, the reset path checks the value from f_{out} *[N-1]* to f_{out} *[N-3]*, but if all values are 1, the reset path is inactive. It means f_{out} *[N]* will not be reset (0, pass gate ON). If f_{out} *[N-3]* is 0, the reset path is activated, and f_{out} [N] is reset and returns to zero.

Meanwhile, *CNT[2:0]* is the output of the 3b counter, which controls the transition speed of the latch driver. *CNT* 3 bits are used as control signals for each of the three MUXs, and when *CNT* each bit is 0, the MUX passes the output f_{out} *[N]* of the latch driver, but when the *CNT* value is 1, it always outputs a value of 1. In other words, a MUX with a *CNT* value of 1 does not reflect information from the previous or subsequent latch driver in the current latch driver. The initial counter value starts with 3'b000 and changes each code to 1, beginning with MSB every time it exceeds the target voltage. Therefore, the fine-control regulation process ends if it becomes 3'b111 after three counter-bit changes. Fig. 4.14 shows the details of this process.

On the other hand, as discussed in section 4.2.4, there are two types of latch drivers, Driver_{UP} and Driver_{DN}, for initial code setting during global reset. For Driver_{UP}, the RST signal and OR and AND gate configurations are shown in Fig. 4.13 in blue. However, for Driver_{DN}, the inverted *RST* is applied instead of *RST*, and OR and AND gate positions are changed. The two different structure allows the output to be quickly

reset to intermediate code during global reset. The 64 outputs of the latch driver generated by this mechanism do not directly connect to the pass gate but go through the filter logic for the false lock scheme once. Fig. 4.15 shows the structure of the false-lock filter logic.

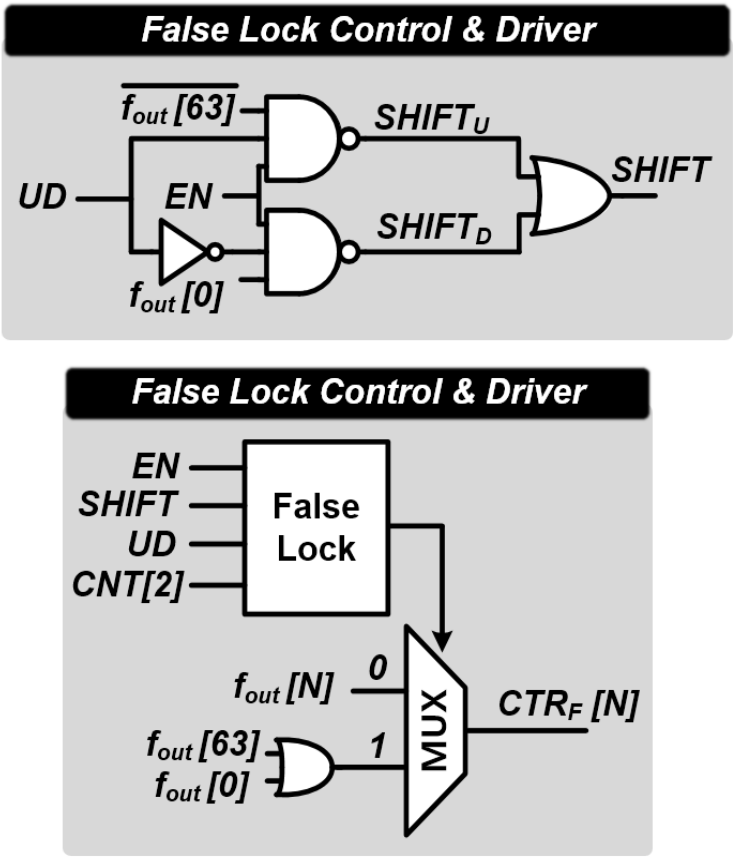

Fig. 4.15 Structure of false lock control block and driver.

4.4 Measurement Results

The prototype of the proposed DLDO is fabricated in a 40nm CMOS process. Fig. 4.16 shows the die photomicrograph of the prototype. The fabricated DLDO occupies an active area of 0.017 mm^2 that includes an on-chip output capacitor of 18 pF. The DLDO supports input voltage V_{IN} ranging from 0.6 to 1.0 V at a dropout V_{DO} of 50 mV. Fig. 4.17 shows the power breakdown of the overall DLDO at V_{IN} of 1.0 V. The synthesized LUT-based shift register and fine-control driver consume 45.2 %, 15.4 % quiescent current in the entire DLDO, respectively. Owing to CMP disable switch from CLK_{tg}, CMP-based oscillators consume only 18.3 % quiescent current.

Fig. 4.18 shows the simulated clock frequency generated from the CMP-based oscillator. At a V_{IN} of 1 V, CLK_{CMP} achieves 4.988 GHz in FF and 3.337 GHz in SS. Fast oscillation CMP makes DLDO possible fast droop recovery and current compensation. Fig. 4.19 shows the simulated transition speed of the bi-directional latch-based driver. Depending on the counter value, transition speed varies through 0.6 to 1.0 V V_{IN} range.

Fig. 4.20 and Fig. 4.21 show the post-simulated load transient responses. At a V_{IN} of 1 V, a load current step of 150 mA is applied within an edge time T_{Edge} 2 ns. The DLDO achieves a droop response time $T_{Response}$ of 1.9 ns and a settling time $T_{Settling}$ of 11.82 ns. The voltage droop V_{Droop} is measured as 175 mV. Table 4.1 shows the performance summary and comparison with other works [49][54][62][65]. The proposed DLDO achieves highly improved transient responses of $T_{Response}$ and $T_{Settling}$, providing the good FOM_2, compared to prior-art LDOs in the table.

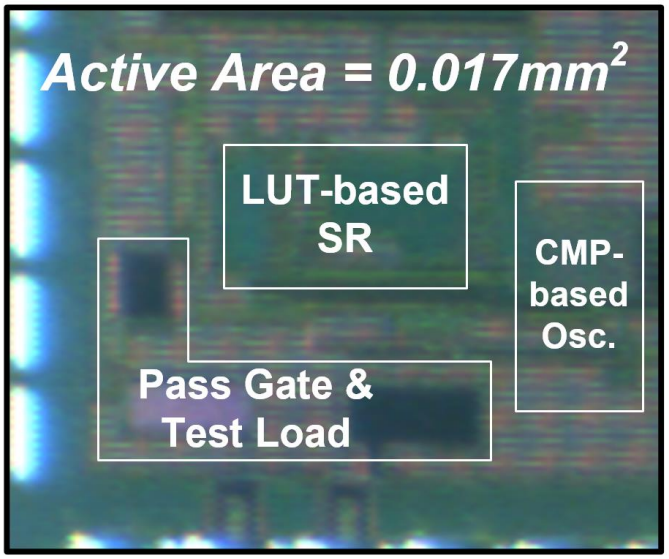

Fig. 4.16 Die photomicrograph of the fabricated DLDO.

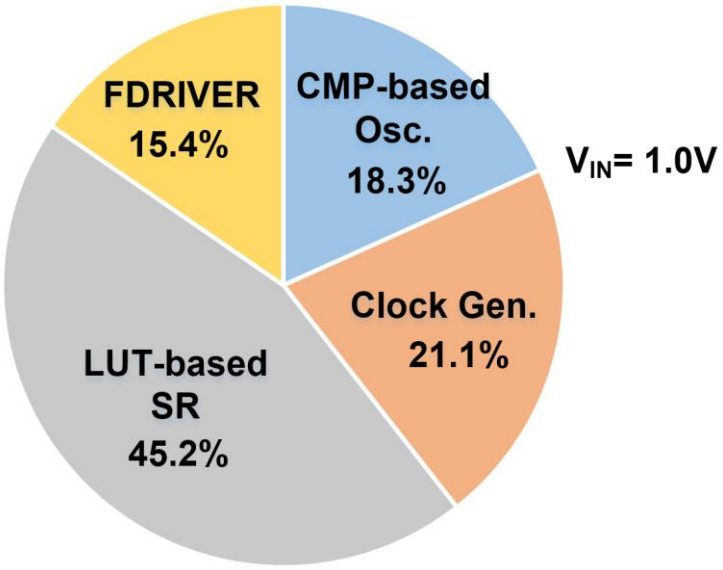

Fig. 4.17 Simulated power breakdown of the DLDO.

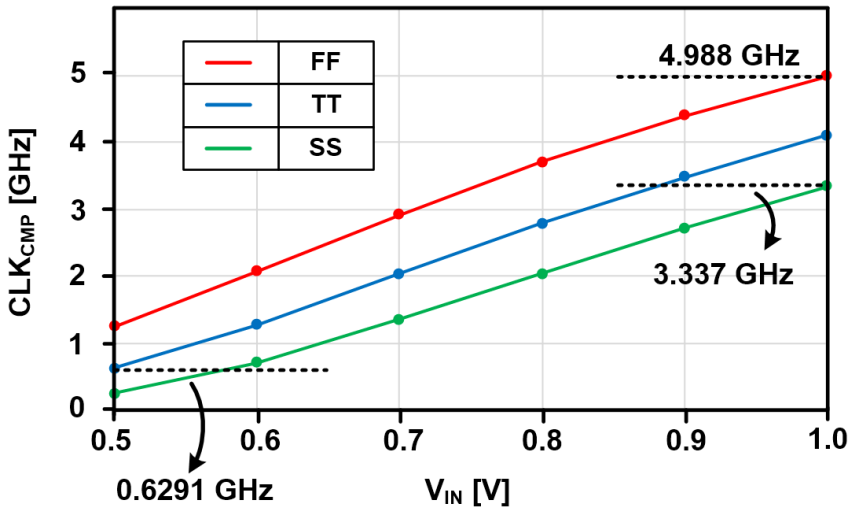

Fig. 4.18 Simulated CLK_{CMP} frequency depending on supply voltage.

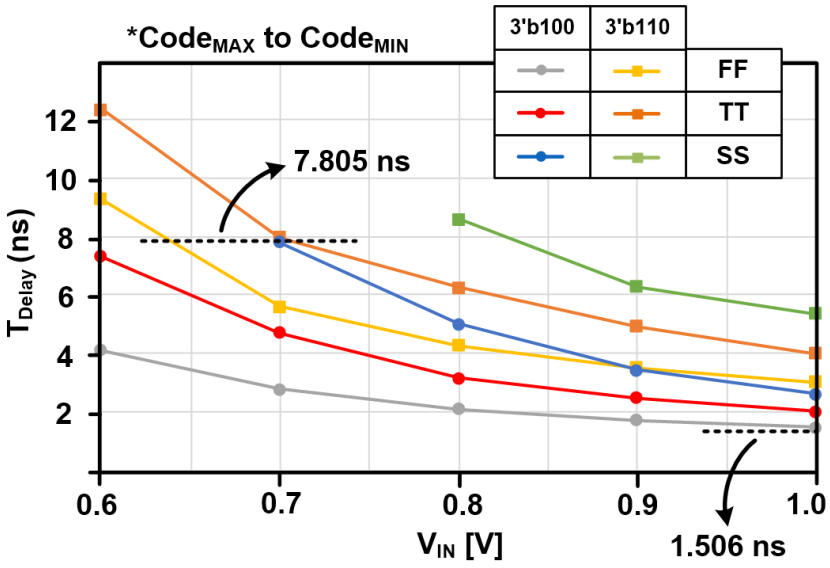

Fig. 4.19 Simulated bi-directional latch-based driver transition speed.

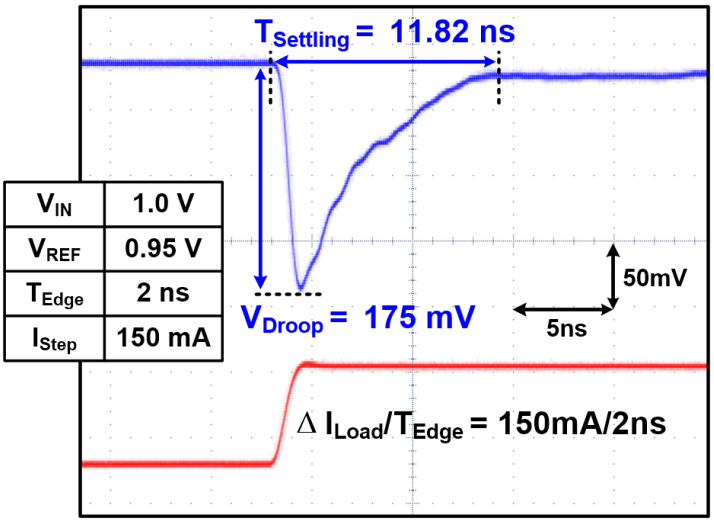

Fig. 4.20 Load transient response with 1.0-V supply and 150-mA step-up current.

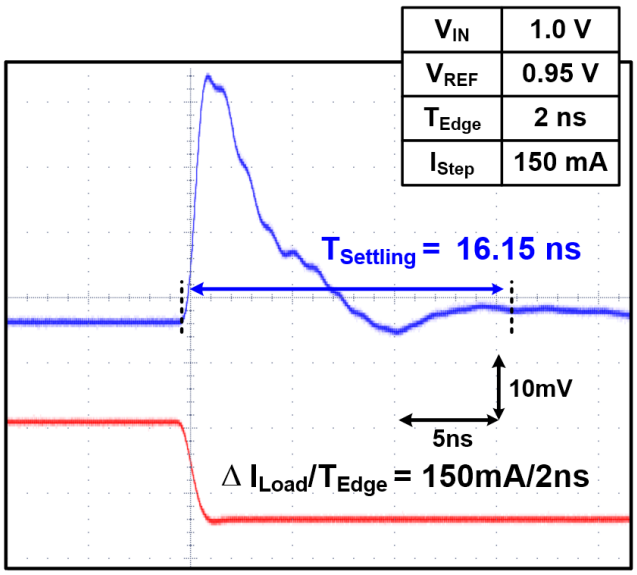

Fig. 4.21 Load transient response with 1.0-V supply and 150-mA step-down current.

Table 4.1 PERFORMANCE SUMMARY AND COMPARISON

	[49] ISSCC 2019	[54] ISSCC 2020	[65] TPE 2022	[62] TPE 2021	This work
Technology [nm]	65	28	40	110	**40**
Operating Type	Digital Time-Driven	Digital FeedForward	Digital Event-Driven	Digital Time-Driven	**Digital Time-Driven**
Search Type	Computational	Latch-based	Adaptive Linear-Binary	Variable Step-Size	**Slope Detect**
V_{IN} [V]	0.65-1.15	0.5-1	0.6-1.2	0.8-1.2	**0.6-1.0**
V_{OUT} [V]	0.6-1.1	0.45-0.95	0.55-1.15	0.7-1.1	**0.55-0.95**
$I_{LOAD,MAX}$ [mA]	16.3	160-480	200	50	**200**
C_{LOAD} [nF]	0.25	0.004	0.15	0.04	**0.018**
I_Q [µA]	80-1200	7.7-241	6-550	188.8-197.9	**195**
$T_{Response}$ [ns] @ V_{IN}	N/A	1.4 @ 0.9V	6 @ 1V	67 @ 1V	**1.9 @ 1V**
$T_{Settling}$ [ns] @ V_{IN}, f_{CLK}	27.9 @ 1.1V	310 @ 0.9V	16 @ 1V	N/A	**11.82 @ 1V**
ΔV_{Droop} [mV] @ $\Delta I_{LOAD}/T_{Edge}$	46 @ 5.6mA/0.1ns	112 @ 430mA/2ns	140 @ 104.2mA/1ns	360 @ 47.5mA/1ns	**175 @ 150mA/2ns**
Peak Current Efficiency [%]	99.7	99.99	> 99.7	92.98-99.61	**99.9**
FoM$_1$ [ps] *	29.3$^+$	0.618 *	5.36	1.26$^+$	**2.47**
FoM$_2$ [ps] **	2.93	1.236	5.36	1.26	**4.94**

* **FOM$_1$** = $T_R (I_Q/\Delta I_{LOAD})$, $T_R^+ = C_{LOAD} (\Delta V_{Droop}/\Delta I_{LOAD})$ at $T_R >> T_{EDGE}$, T_R =Response time

** **FOM$_2$** = **FOM$_1$** $*(T_{Edge}/1\ ns)$

Chapter 5

Conclusion

In this thesis, several architectures of fast transient response DLDO are presented. At first, an event-driven DLDO with an adaptive two-step search for realizing a fast droop recovery in advanced memory system is presented. The ALSC with 2D-CSR and the SBSC with 10b Sub-SAR provide fast regulation with mitigation of undesirable output shootings. The DLDO is fabricated in the 40-nm CMOS technology with an active area of 0.0062 mm^2. The ranges of input and output voltages are from 0.6 V to 1.2 V and from 0.55 V to 1.15 V, respectively. During recovery from a 104.2-mA load-current step with a 1-ns slew, the DLDO achieves 140-mV voltage droop and 6-ns recovery time.

Besides, a fast transient response DLDO employing a slope detector and a bi-directional latch-based driver is presented. Fast response time and settling time are achieved with optimization of loop activation process by LUT-based shift register.

The DLDO is fabricated in a 40-nm CMOS process. When the load current is increased by 150 mA with a 2-ns edge rise time, the DLDO exhibits 1.9-ns response time, 11.82-ns settling time, and voltage droops of 175 mV with V_{IN} of 1.0 V. This work offers the total chip area of 0.017 mm^2.

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초 록

본 논문은 차세대 메모리 시스템에 적용 가능한 빠른 과도 응답 성능을 가지는 디지탈 낮은 드롭아웃 레귤레이터의 설계에 대해 기술한다. 메모리 시스템의 최근 기술들은 높은 전력 밀도와 빠른 데이터 속도를 주된 목표로 하며 이에 맞추어 단기간, 많은 양의 부하 전류 변화를 견디는 파워 컨버터의 필요성이 높아지고 있다. 이에 주기적인 클락 신호에 따라 메모리 데이터 입출력에 유의미한 손상을 발생시키는 전압 강하를 보상하는 해결 방안을 탐색한다. 이를 통해 메모리 시스템이 가지는 제약조건 하에서 빠른 과도 응답 성능을 달성하는 두 가지 구조를 제안한다.

첫 번째 시연으로서, 느린 외부 클락 조건에서 유발되는 디지탈 낮은 드롭아웃 레귤레이터의 과도 응답 성능 저하를 완화시키기 위한 이벤트 주도 방식의 적응형 두 단계 서치 기술을 제안한다. 본 기술은 느린 외부 클락에 의존한 루프 동작 시간의 한계를 고리 증폭기 기반 연속 시간 비교기를 통해 해결한다. 또한 자리 이동 레지스터의 구현에 소모되는 비용을 줄이고자 각 레지스터의 제어 장치를 중앙으로 집적시킨 순환형 구조로 설계되었다. 마지막으로 남아있는 조정 에러는 적응방식의 축차 비교형 알고리즘으로 제어하여 교정에 필요한 시간을 최소화하였다. 40-nm CMOS 공정으로 구현된 프로토타입 칩의 측정을 통해 부하 전압의 빠른 회복 속도와 정정시간을 보임을 확인하였다.

두 번째 시연으로서, 초고속 과도 응답 환경에 적합한 디지털 낮은 드롭아웃 레귤레이터가 설계되었다. 수십~수백 메가헤르쯔 클락의 상승 또는 하강 엣지마다 발생하는 부하 전류 변화를 탐지하고 보상하고 정정하

기 위해 기울기 탐지기 기반 coarse 제어기 기술을 제안한다. 시간에 따른 부하 전압 변화의 정도에 따라 차등 보상하는 알고리즘을 적용함으로써 보상 효율을 높였다. 나아가 순람표 기반 자리이동 레지스터는 부하 전류 과도 상태 이후 디지탈 레귤레이터의 빠른 루프 응답 속도를 가능케 하였다. 마지막으로 남은 조정 에러를 제어하는데 있어서 기존 자리이동 레지스터 방식에서 벗어나 빠른 수렴 속도와 높은 해상도를 가지는 양방향 래치 기반 드라이버가 제안되었다. 해당 프로토타입 칩은 40-nm CMOS 공정으로 구현되었으며, 낮은 부하 축전용량에도 빠른 과도 응답 성능을 통해 효과적인 부하 전압 회복을 이루어 내었다.

주요어: 빠른 과도 응답, 낮은 드롭아웃 레귤레이터, 디지털 낮은 드롭아웃 레귤레이터, 선형 탐색, 2 진법 탐색, 고리 증폭기 기반 비교기, 둥근 시프팅 레지스터, 이벤트 주도, 기울기 탐지기, 순람표 기반 시프트 레지스터, 양방향 래치 기반 드라이버, 비교기 촉발 공진기

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