The Role of Defects and Interface Degradation on Ferroelectric HZO Capacitors Aging

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***Abstract*— The discovery of ferroelectricity in HfO_2-based materials, especially $Hf_{0.5}Zr_{0.5}O_2$ (HZO), opened to a wide range of applications. In fact, innovative HZO memories, such as ferroelectric tunnel junctions (FTJs), are suitable candidates as ultra-low power storage/synaptic elements, holding the data as a polarization state. Yet, a clear link between the device degradation and material/interface properties is still lacking. In this work, we elucidate the degradation dynamics in metal-HZO-metal (MFM) capacitors by combining ab-initio calculations, physics-based simulations, dedicated experiments, and custom data analysis based on a recently introduced small-signal device model. Stress/measure experiments are conducted to: *i*) extract the $2P_r$ (remnant polarization) evolution throughout device lifetime (from pristine to wake-up and fatigue); *ii*) determine parasitic series impedance and key material properties through a small-signal model; *iii*) evaluate the leakage current. Including the contribution of the parasitic series impedance in physics-based simulations allows reproducing leakage profiles and their cycling evolution. The combination of the proposed approaches allows to better interpret the behavior of these devices and retrieve the key role of process conditions (specifically post-deposition steps) in determining the device lifetime and overall reliability.**

Keywords – Ferroelectric Capacitors, Ferroelectric Modeling, Small signal model, Neuromorphic.

I. INTRODUCTION

Ferroelectric devices, especially those relying on HfO_2-based materials, (e.g., $Hf_{0.5}Zr_{0.5}O_2$ (HZO)) are currently actively investigated as they are expected to be key enablers for the change of paradigm required by the computing architectures to efficiently sustain the ever more stringent performance and energy efficiency requirements.

In fact, the increasing demand of autonomous and intelligent systems [1], [2], together with massive data management [3], is revealing the limitations of typical CMOS architectures, such as scaling [4], and energy consumption [5]. In particular, the latter is mainly given by the intrinsic separation of processing and memory units [6] and their constant need to communicate.

To overcome these constraints, different approaches have been explored, leading to the development of innovative devices [7]–[9] and circuit designs [10]–[12], building the foundations of the emerging Logic in Memory (LiM) [13]–[15] and brain-inspired computation [16]–[18], both merging in the same circuital elements memory and computation.

Among them, innovative HZO memories [19]–[21], such as ferroelectric tunnel junctions (FTJs), are found to be suitable candidates to act as ultra-low power storage/synaptic elements, holding the data as a polarization state. FTJs consist in a metal-dielectric-ferroelectric-metal (MDFM) stack, and combine remarkable advantages, such as low power consumption, CMOS compatibility, fast access speeds, high-scalability, low footprint, and non-volatility [22]–[24]. Also, differently from FeRAM [25] or metal-ferroelectric-metal (MFM) capacitors [26], [27], their asymmetry in the stack, given by the presence of the dielectric (DE), allows a non-destructive read-out thanks to dependence on the ferroelectric (FE) polarization of the device band diagram and electrical resistance [28], resulting then in an intentional asymmetric leakage current used to retrieve the stored data.

The ferroelectricity in HZO is generally related to the non-centrosymmetric orthorhombic ferroelectric phase (o-phase) [29] which is reported to be heavily influenced by dopant material and concentration. However, besides the o-phase, the interface quality between the HZO layer and the upper and lower metal electrodes also has an important impact on the performance of the device. In fact, even in MFM capacitors, ideally symmetrical structures, the presence of interfacial layers with different thicknesses, due to deposition process, often leads to a stack and leakage asymmetry [30], as confirmed by hard x-ray photoelectron spectroscopy (HAXPES) measurements [31], [32].

Also, the lifetime of these devices is typically characterized by three working regions. Starting from a pristine state, the ferroelectricity in HZO is expected to increase (i.e., $2P_r$) with increasing the number of stress (or operation) cycles due to the presence of wake-up effect [33]. These mechanisms drive the device in the typically desired working condition (woken-up state), characterized by the stability of ferroelectric properties [34], [35]. However, a prolonged cycling degrades the device, bringing it in the fatigue region, and eventually to breakdown [34], [35]. So far, a clear link between the device degradation and material/interface properties is still lacking.

In this work, we elucidate the degradation dynamics in M-HZO-M capacitors (Fig. 1a) by combining ab-initio calculations, physics-based simulations, dedicated experiments and custom data analysis based on a recently introduced small-signal device model [36], [37].

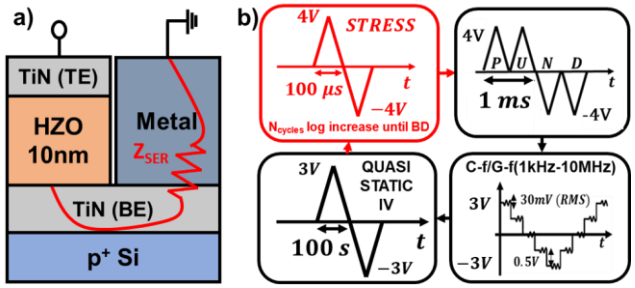

Fig. 1 – (a) Schematic of 10nm HZO capacitor. (b) Stress/measurement sequence. The stress consists in positive and negative triangular pulses with peak voltages of ±4V and a period of 200μs. After each sequence cycle, the number of stress pulses is logarithmically increased until the device BD.

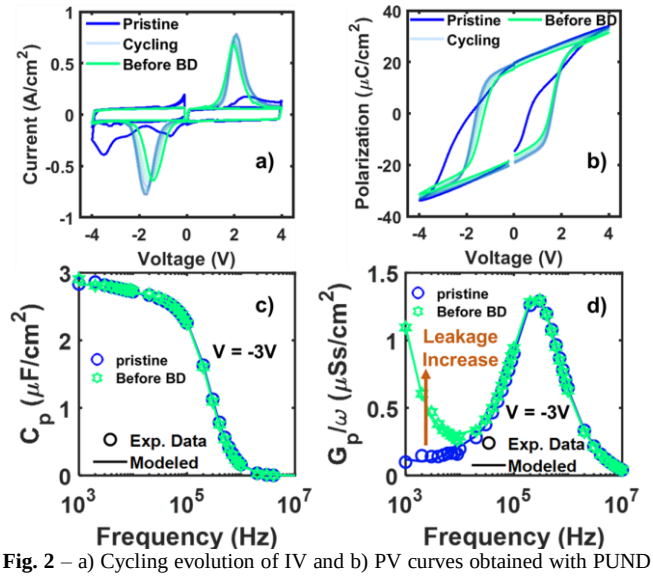

Fig. 2 – a) Cycling evolution of IV and b) PV curves obtained with PUND measurements, highlighting the pristine and before BD cases. c-d) Experimental (symbols) and modelled (lines) C_p and G_p/ω profiles taken from C-f/G-f at -3V, comparing the pristine and before BD cases, using model and parameters of Fig. 3.

Stress/measure experiments (illustrated in Fig. 1b) are conducted to: *i*) extract the $2P_r$ (remnant polarization) evolution throughout device lifetime (from pristine through wake-up and fatigue); *ii*) determine parasitic series impedance between grounded tips and the capacitor (Fig. 1a in red) and key material properties through impedance spectroscopy [38], analyzed with our small-signal model [36], [37]; *iii*) evaluate the leakage current. Asymmetries in leakage response and its evolution are reproduced and interpreted by means of physics-based simulations, including the presence of interfacial parasitic layers at both interfaces (e.g., TiO_x and $TiON_x$ suggested earlier in similar structures [39]) with different properties.

The paper is organized as follows: Section II describes the analyzed devices, together with the details of the implemented stress/measure sequence and the small-signal model. To strengthen our measurements interpretation (in particular leakage asymmetry and its evolution) and model the effect of defects and the presence of interfacial layers with bottom and top electrodes, we exploited the Ginestra® [40] platform, the details of which are reported in Section III. Also, a sensitivity analysis on different device properties (i.e., layer's thickness (t), permittivity (ϵ), and defect's density (δ)) is performed, and its results are employed in Section IV to reproduce the leakage profiles at pristine, wake up, and fatigue (right before device breakdown (BD)). The results retrieved from simulations and

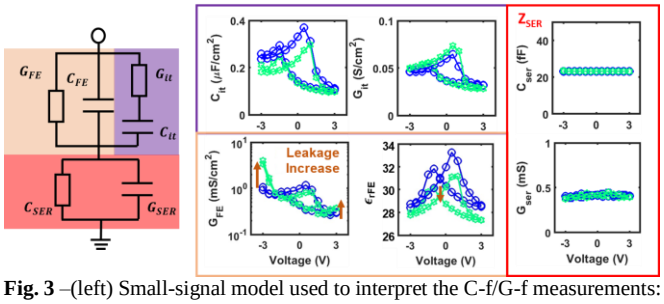

Fig. 3 –(left) Small-signal model used to interpret the C-f/G-f measurements: pure ferroelectric capacitance and conductance (orange), contribution of traps and possible parasitic layers (purple), and series impedance (red). (right) Parameters extracted from Fig.2c-d experimental data, divided using the same colour code on the left.

small-signal modeling are then compared to comprehensively interpret the mechanisms underlining the MFM degradations. Conclusions follow.

II. Devices and Experiments

The MFM devices studied in this work, fabricated by NaMLab, are TiN/ 10nm-HZO (FE)/ TiN stacks (Fig. 1a), with a 100μm diameter. The bottom electrode (BE), shared by all capacitors, is accessible via a common metal pad, and introduces an inevitable parasitic series impedance (Fig. 1a in red) [41] between the grounded tip and the actual capacitor, with consequences on the interpretation of the results [36], [41]. Fabrication details for these devices are reported in [42]. To study the degradation mechanisms in these stacks we perform a dedicated stress/measure sequence (illustrated in Fig. 1b) consisting of: *i*) positive-up-negative-down (PUND) (execution time 2ms), fundamental to extract polarization-voltage (PV) curves and $2P_r$ evolution (which reveals the pristine, wake up and fatigue regions); *ii*) impedance spectroscopy by means of capacitance-frequency/ conductance-frequency measurements (C-f/G-f). A DC voltage ([+3V; -3V], step 0.5V) is applied at the top electrode (TE) of the capacitor, with a superimposed small AC signal with frequency sweeping from 1kHz to 10MHz and 30 mV amplitude, allowing to retrieve the total admittance (expressed as parallel capacitance C_p and a conductance G_p (usually reported as G_p/ω [43])), which is then analyzed by means of the small-signal model; *iii*) quasi-static IV measurements (execution time 200s), revealing the leakage current with a negligible capacitive contribution (dV/dt).

Fig. 2 shows the results of PUND and C-f/G-f measurements, highlighting the difference between the pristine and the last cycle (before breakdown (BD)). As expected, leakage increases with stress, as highlighted by the low-frequency G_p/ω [36], [37] (Fig. 2d). This is further confirmed by the analysis of the C-f/G-f curves by the small-signal model (Fig. 3) including HZO physical properties [36], [37] (i.e., voltage dependence of HZO permittivity (ϵ_{rFE}) and of HZO conductance (G_{FE})), a first-order equivalent trap response and equivalent interfacial layers effect [39], [44], [45] (C_{it} and G_{it}), together with the parasitic series impedance ($Z_{SER} = C_{SER}//G_{SER}$). It is worth noting that ϵ_{rFE} represent an equivalent contribution of the different ferroelectric and non-ferroelectric phases inside the layer, together with the effect of the interfacial layers permittivity. Reproducing C_p and

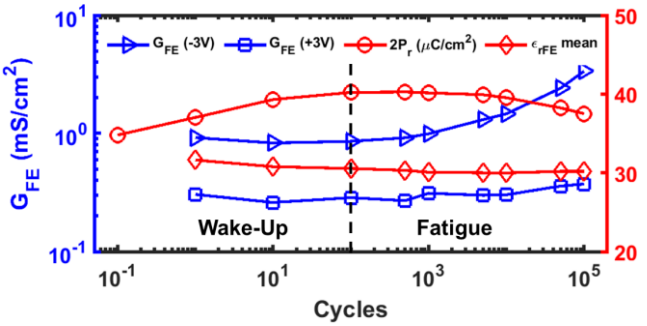

Fig. 4 – Comparison of the evolution of $2P_r$ (red circles) with small-signal parameters of interest. G_{FE}s are taken at ±3V, the voltages where the leakage evolution is more significant.

G_p/ω curves at different voltages with the small-signal model allows to extract the model parameters, as reported in Fig. 3. The evolution of G_{FE} at ±3V with cycling confirms the leakage increase (Fig. 3-4), especially for the highest fields. Fig. 4 reports the cycling evolution of $2P_r$, G_{FE} (±3V) and the voltage-averaged ϵ_{rFE}, showing trends in-line with those reported in the literature for pristine, wake-up and fatigue regions [34]. Notably, fatigue onset coincides with the increase of G_{FE} (-3V), possibly referable to defects generation [33], [37] The decreasing trend of ϵ_{rFE} suggests that degradation may also involve reactions, likely at the interfaces as reported in [31], [32], [35], [44]. Also, Fig. 5a reports the quasi-static IV profiles during the device lifetime. Notably, the asymmetry visible in Fig. 5a is comparable to the one of FTJ with a t_{DE} = 2nm (DE = Al_2O_3, ϵ=6-8 [37], [46]) between the HZO and the TE (Fig. 5b), further strengthening the hypothesis of the presence in MFM of interfacial layers with different properties (e.g., thickness and ϵ [34], [45]) that likely play a similar role as DE in the FTJ.

III. Modeling and Simulations

To reproduce the asymmetry observed in measurements, we model a 3-layer stack (including also a Z_{SER} equivalent to the one extracted by C-f/G-f, as shown in Fig. 6) which allows us to separate zones within the material with different key parameters, such as layer thickness (t), ϵ, and defects density (δ). The reference simulated device is a 100·100nm² stack with a bottom interfacial layer (IB) with ϵ_{IB}=60, an HfO_2 bulk (BK) with an equivalent ϵ_{BK}=32, and a top interfacial layer (IT) with ϵ_{IT}=15. To understand the impact of each parameter on the quasi-static IV profile we carried out a sensitivity analysis (reported in Fig. 7), which consists in varying for each layer a single parameter per time, i.e., the thickness of the top (t_{IT}, Fig. 7b), bulk (t_{BK}, Fig. 7c), and bottom layer (t_{IB}, Fig. 7d), starting from an IV profile generated by a specific reference stack (Fig. 7a). The same analysis is performed varying ϵ (Fig. 7e-h) and δ (Fig. 7i-l) to get a better understanding of their impact.

All the simulations are carried out using Ginestra® [40], which includes Schottky and thermionic emission, direct (WKB approximation), trap-assisted (TAT – including trap-to-trap contribution), and Fowler-Nordheim tunneling, as well as the trapped charge term in the Poisson's equation. We include defects in the ferroelectric HfO_2 bulk having thermal (E_{TH} = 2.1±0.7 eV) and relaxation (E_{REL} = 1 eV) energies which are very close to those predicted by hybrid-DFT calculations for oxygen vacancies in the orthorhombic

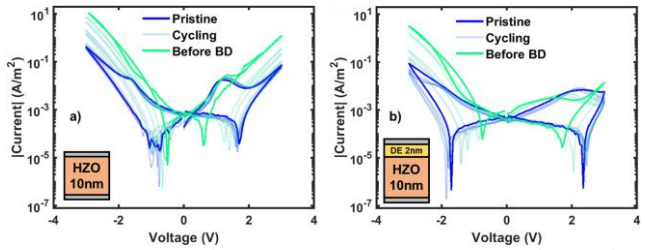

Fig. 5 – a) Evolution of quasi-static IV curves during the lifetime of the device, highlighting the pristine and before BD cases. b) Quasi-static IV curves during the lifetime of an FTJ with t_{HZO} = 10nm and t_{DE} = 2nm, showing similar asymmetry as in a).

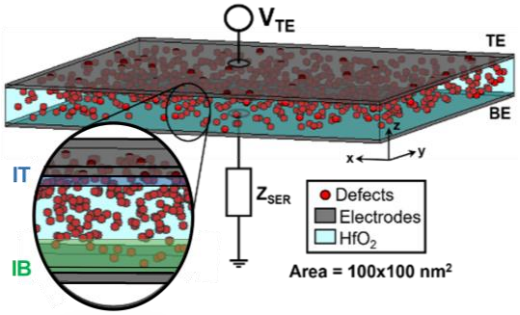

Fig. 6 – Model of the MFM cell simulated in Ginestra®, including the presence of a Z_{SER} with the value derived from the small-signal model.

ferroelectric phase of HfO_2 ($E_{TH} \approx 1.8$ eV, $E_{REL} \approx 0.7$ eV) [47]. For simplicity, the same defects are used within all layers. Ferroelectric switching is modeled using a Preisach model for the HfO_2 layer with $P_r^{\pm}$=7μC/cm², saturation polarization $P_s^{\pm}$=6.999μC/cm², and coercive field $E_c^{\pm}$=1.5 MV/cm. It is worth noting that, due to the nature of the Preisach model, these parameters are dedicatedly calibrated to reproduce switching at the very low dV/dt employed in quasi-static IVs (i.e., different values should be used to reproduce data at different dV/dt, as those in Fig. 2b).

The sensitivity analysis suggest that leakage current is strongly influenced by the thickness of each layer, as well as by the ϵ_{IT}, while the δ of the interfacial layers has almost no impact.

IV. Results and Interpretation

Considering the results retrieved by the sensitivity analysis, we reproduced the experimental quasi-static IV profiles of pristine (Fig. 8a), wake-up (Fig. 8d) and before BD (Fig. 8c) conditions. As reported in the band diagrams (all taken at -3V, Fig. 8d-f), the pristine state is characterized by a δ in HfO_2 of $7\cdot10^{18}$cm^{-3} with a normal distribution in space (μ=6.8nm, σ=3.1nm), and an equivalent stack ϵ of 31.5. The wake-up conditions are well reproduced by just considering defects redistribution in space, with the normal distribution shifted closer to the TE (μ=7.2nm, σ=3.2nm), in agreement with previous earlier simulation results and independent reports [37], [48]. Replicating the before BD case (Fig. 8c), requires instead increasing δ in HfO_2 ($1.5\cdot10^{19}$cm^{-3}). Moreover, the t_{IT} must increase at the expenses of t_{BK}, resulting in an equivalent stack permittivity drop to 29.8. Interestingly, this interface layer thickening with cycling has been seen in a device with equivalent structure under similar stress conditions using scanning TEM [45], confirming that degradation in these devices is strongly related to interface phenomena. Notably,

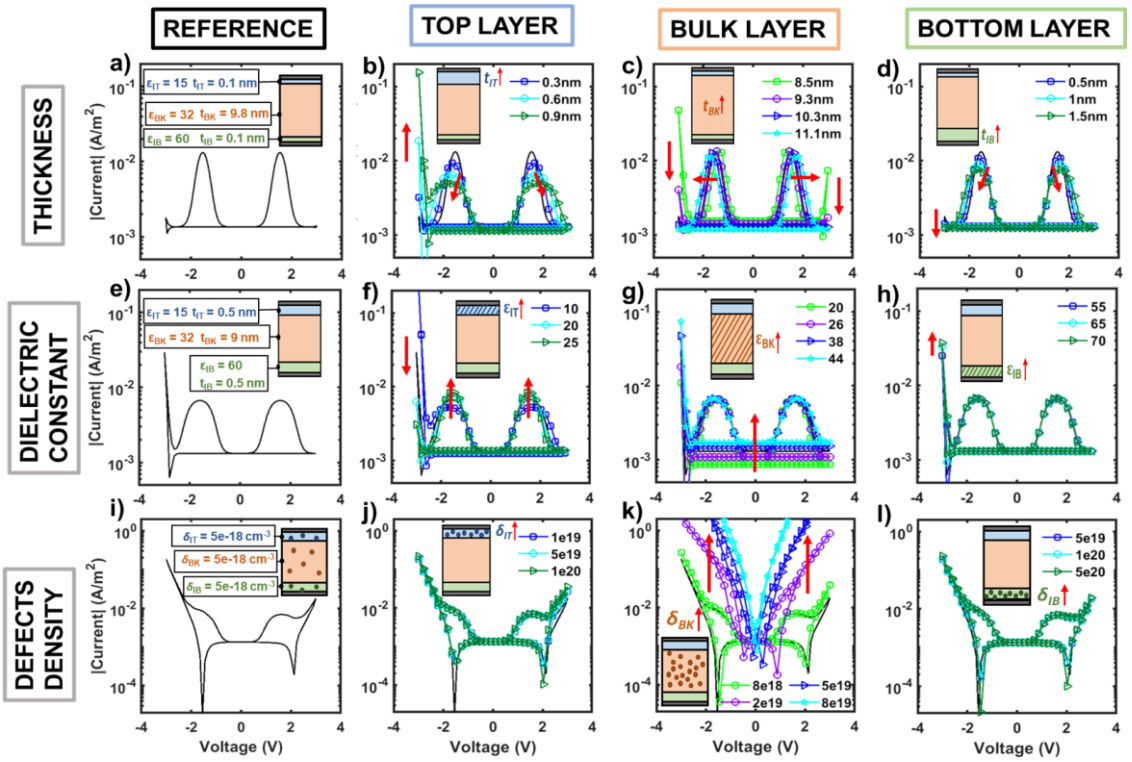

Fig. 7 – Sensitivity analysis on main stack parameters (layers thickness (b-c-d), dielectric constant (f-g-h) and defects density (j-k-l)), considering the presence of interfacial top (IT) and bottom (IB) layers. a-e-i) Reference layers parameters and profiles, used as starting points for the different analysis. For each case, we considered a symmetric Preisach model with $P_r^{\pm}$=7μC/cm², $P_s^{\pm}$=6.999μC/cm², and $E_c^{\pm}$=1.5 MV/cm.

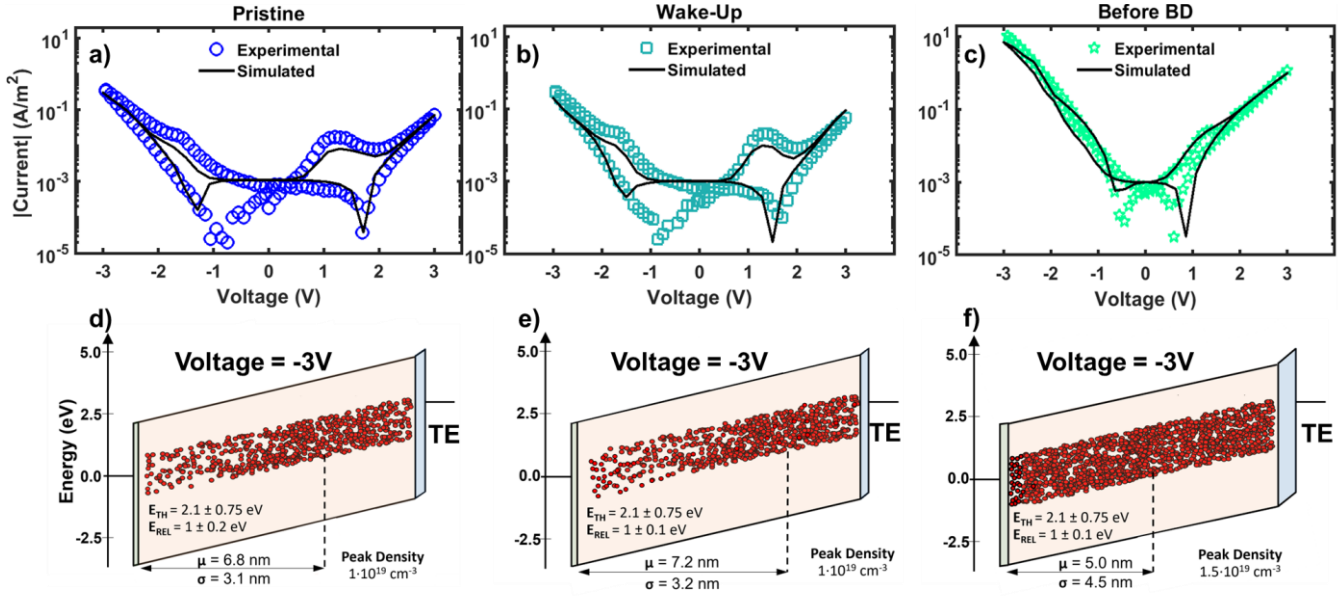

Fig. 8 – Fig. 5a experimental (symbols) and simulated (lines) profiles of quasi-static IV for pristine (a), wake-up (100 cycles) (b) and before BD (1e5 cycles) (c) cases, with respective band diagrams and parameters (d-e-f) at V = -3V.

due to defects generation, here data are best reproduced by a uniform defect's distribution in space (μ=5nm, σ=4.5nm). Remarkably, as shown in Fig. 9, the obtained equivalent ϵ trend follows the one of the voltage-averaged ϵ_{rFE} extracted by the small-signal model (Fig. 3), confirming the dependability of the latter.

Besides, the evolution of the (normalized) defect's number ($n_d/n_{d\ pristine}$ (#)) follows the one of the (normalized) G_{FE}(-3V) ($G_{FE}/G_{FE\ pristine}$ (-3V)) extracted by the small-signal model, further confirming the supposed wake-up and degradation mechanisms [34], [37], [45], [48].

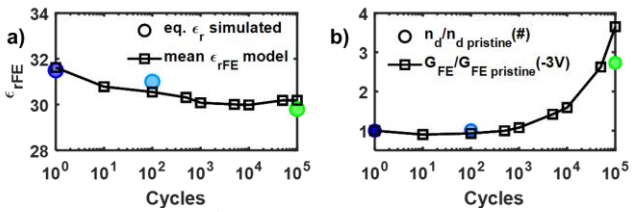

Fig. 9 – a) Comparison of cycling evolution between the voltage-averaged ϵ_{rFE} extracted by the small-signal model and the equivalent ϵ of the stack obtained in simulation. b) Comparison of cycling evolution between FE leakage (G_{FE} (-3V)) extracted by the model and simulated defects numbers, both normalized by their pristine values.

V. Conclusions

In this work, we interpreted stress/measure results on a MFM stack combining a small-signal compact model together with physics-based simulations, performed on a 3-layer stack to include the effect of the presence of interfacial layers with metal electrodes due to deposition process. A sensitivity analysis on the main parameters of each layer is performed, retrieving their principal role in the stack response and providing an interesting investigating tool for analyzing fabrication processes. The results of this analysis are then used to reproduce experimental quasi-static IV profiles, highlighting that: *i*) wake-up mechanisms are associated with a defects redistribution, as previously suggested by [33], [37]; *ii*) fatigue is driven by a mild defect generation and by a definite degradation of the TE interface, as previously observed using scanning TEM [45]. It is then arguable that similar phenomena may rule over the degradation of FTJ devices.

Acknowledgments

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