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Fast cryogenic probing of silicon FinFET devices for quantum computing

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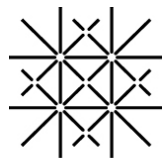

Department of Physics
Quantum Coherence Lab

Fast cryogenic probing of silicon FinFET devices for quantum computing

Master Thesis

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Abstract

Silicon spin qubits are a promising candidate for quantum computing. In this work we focus on two important aspects in the realization of quantum computers. First of all, we try to gain more insight in the driving mechanisms of the qubit, secondly we will address the scalability of silicon spin qubits and demonstrate a rapid testing technology for quantum devices.

The spin-obit interaction for holes in silicon, all-electrical control of the spin qubit is achieved by coupling to the spin via spin-orbit interaction. If holes are confined in one-dimensional nano-structures, this interaction is predicted to be highly tunable [1]. In this these the direction and strength of the spin-orbit filed are investigated. We observe a out-of-plane g-factor anisotropy with a modulation of 30 % and find a maxima in the g-factor 13 degrees out of the sample plane.

To enhance the scalability of silicon spin qubits, statistics on device characteristics are required. The bottleneck in obtaining these statistics is the requirement to wire-bond and cool-down each device while the amount of devices which can be simultaneously cooled down is limited. Here we present a probe station which can operate at cryogenic temperatures and is able to characterize up to 192 different devices. We show that this probe station can perform an automated characterization sequence on a set of 21 independent working devices in the same cool down. This will allow for fast and large-scale pre-characterisation of spin qubit devices in the near future.

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Chapter 1

Introduction

Quantum computing is expected to solve a lot of currently unsolvable problems with its use of quantum bits (qubits). Due to its exponential scalability problems can be solved faster. In recent years substantial progress has been made in the development of a quantum computer [2–4], Google even claimed to have achieved quantum supremacy [5], using their superconducting qubit based quantum processor, with 53 qubits. However to achieve a usable fault tolerant quantum computer approximately 10^6 qubits are necessary [6, 7]. To achieve this, a scalable and cheaper approach to quantum computing has to be found.

In principle any quantum two level system can be used as a qubit (the building block of a quantum processor). besides superconducting qubits, spin qubits have been proposed by Loss and Divencenzo in 1998 [8]. Other options, like topological qubits and trapped ions are also explored [9]. Experiments on spin qubits started with gate-defined quantum dots in GaAs, first with the discovery of several novel read out techniques of the spin and charge state in the quantum dot [10–12]. Not long thereafter coherent control of the electron spin was implemented [13]. Another control mechanism of the electron spin was established using a slanting magnetic field, induced by a micromagnet, and rapid electric field pulses [14]. To assess the quality of a qubit the quality factor is defined as the ration of the coherence time to the manipulation time. In GaAs all atoms have a nuclear spin which limits the coherence time [15] and the spin-orbit interaction is leading to a long operation time [13]. To decrease the operation time experiments moved to InAs nanowires with a strong spin-orbit interaction, a first working demonstration of these qubits was given by Nadj-Perge et al. in 2010 [16].

More recently studies have focussed on finding solutions with less nuclear spins and thus a longer coherence time. A solution was found in silicon, with only 4.7 % atoms with a nuclear spins, and a strong spin-orbit interaction for holes. Another argument to move to silicon was the extensive knowledge already available on silicon fabrication processes in the the classical computing industry and its large scale silicon platform. By using CMOS (Complementary Metal Oxide Semiconductor) compatible techniques, qubits were developed [17]. Not long thereafter a design for a quantum processor in silicon was proposed [18], even though the proposed computing unit is an idea for the future, it provided a goal to built towards for scalable quantum computers. Several works have shown operation of single hole spin qubits [19, 20], either using CMOS technology or using CMOS compatible materials. Very recently two independent groups have achieved single qubit operation above 1 K [21, 22]. Multi qubit operation has also been achieved recently in different experiments [23, 24]. All these advances are important to eventually built a spin qubit computing unit.

Spin qubits come in two flavours, the first one based on electrons, the other is based on holes (vacancies in the valency band). The advantage for hole spin qubits is that the can solely be driven by electrical field pulses [17, 25], while for electrons either a oscillating magnetic field [13] or a

slanting magnetic field in combination with electric field pulses [14] is necessary. The spin-orbit interaction is predicted to be electrically controllable [26, 27].

In this work we will use silicon quantum dots integrated in fin field-effect transistors (FinFETs). These devices have been used to accumulated stable quantum dots, both ambipolar and unipolar [28, 29]. Here we obtain the out-of-plane g-factor anisotropy to infer information about the spin-orbit vector. With this information a future qubit in these devices can be optimized for fastest operation and longest coherence.

To address the scalability of this platform we develop a fast device characterization instrument for quantum (dot) devices. A probe station like approach is implemented on a variable temperature insert (VTI) for use at cryogenic temperatures. With this cryo-prober up to 192 devices can be quickly tested for stability and other device properties. This approach can be very useful for optimizing the gate layout of a novel type of device.

The idea of rapid wafer scale testing of devices at cryogenic temperatures has been around since the 1980s [30–32]. However, at the time the devices had to be pre-soldered to the needles making the machines bulky and non flexible. More recently, improvements have been made such that the probes can move and the devices behave like classical probe stations [33, 34], the ability to use RF-lines was also added in these improved designs. These ideas have also recently been commercialized by Lakeshore [35] and Microxact [36]. The number of probes and the temperature range is still limited for these devices. More recently Intel, in collaboration with Bluefors and Afore [37], announced the first large scale wafer testing machine for spin qubits down to 4 K. With our device we hope to built an affordable and flexible solution for automated testing of a large quantity of devices. Our cryo-prober can be mounted on a VTI and thus be used for temperatures in the range of 1.5 K to 400 K.

In this work we will use the cryo-prober to test the properties of single quantum dot devices. Moreover, the transistor properties of these devices will be tested at cryogenic temperatures. The properties of transistors at cryogenic temperatures is important information when trying to built the quantum classical interface [38]. This is the circuitry required to control any qubit, currently most experiments have these control units externally, implementing these control units on chip increases the scalability of the qubit devices. Several studies have been done to do study the effects of temperature on classical MOSFET transistors [39, 40]. Simple multiplexers [41] and a complete control chip [42] using transistors at cryogenic temperatures have also already been experimentally realized. On of the challenges here is to use industrial processes to start scaling up the amount of qubits and reduce the amount of control lines going to room temperature.

1.1 Thesis structure

This thesis will continue in Chapter 2, with a theoretical introduction to electronic transport in FinFET quantum dot devices and spin states therein. In Chapter 3 we will introduce the spin-orbit interaction, first from a theoretical perspective and then built a numerical simulation to explore the the spin-orbit interaction in the context of double quantum dots. The experimental techniques, set-ups and devices will be explained in Chapter 4. The main results of the thesis will be discussed in Chapter 5. In the final Chapter (Chapter 6) of this work we will summarize the results and draw conclusions as well as provide an outlook to future research, and other angles to explore.

Chapter 2

Electronic transport and quantum dot theory

In this chapter we discuss the electronic properties of quantum dots (QDs). We start by looking at a single QD and will then expand to two QDs in series. Furthermore an overview of spin states in QDs will be given, leading in to a section on Pauli spin blockade, finally we will discuss some Pauli spin blockade lifting mechanisms.

2.1 Electronic transport in transistors

A transistor is a defined channel with a source and drain and a gate on top of the channel which regulates the transport from source to drain. A transistor is considered "on" when the gate is tuned such that a current can flow from source to drain, the "off" state is in the case there is no current flow from source to drain.

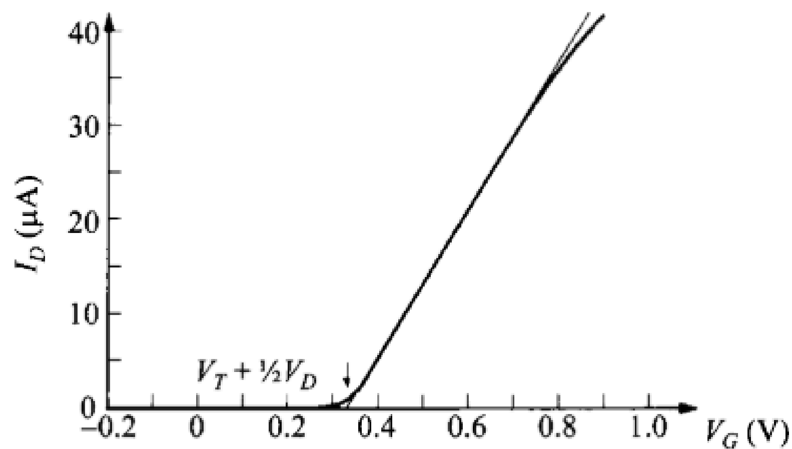

Figure 2.1: A typical IV curve for a transistor with indicated the threshold voltage. Figure taken from [43]

The typical transfer characteristics of a MOSFET transistor are shown in figure 2.1. this curve is called an I-V curve. From this curve the threshold voltage, or the voltage at which the tran-

sistor turns on can be extracted [43]. This is usually done by finding the linear regime of this curve. This regime can be found by looking at the derivative (also called the transconductance). From the point of maximum transconductance the threshold voltage is extrapolated by finding the zero-crossing of a line with the slope of the maximum transconductance.

To compare the operation characteristics between the low and high bias regime is the drain induced barrier lowering (DIBL) as a characteristic is introduced. This effect is mainly present in short channel transistor where in the case of a large source drain potential difference a current will still flow despite the transistor being in the off state. This also lowers the threshold voltage, the DIBL can be calculated by

$$DIBL = -\frac{V_{th}^{high} - V_{th}^{low}}{V_{sd}^{high} - V_{sd}^{low}}, \tag{2.1}$$

where $V_{th}^{high/low}$ is the threshold voltage under high or low bias and $V_{sd}^{high/low}$ the source drain bias in high and low bias mode. Typical values for the high and low bias regime are 1 and 0.1 V.

Another important parameter is the subthreshold swing, which is a measure for how fast the transistor turns on. The subthreshold region is defined as the regime in which the gate bias is below the threshold and the semiconductor is depleted. In this regime the source-drain current is dominated by the diffusion current. The subthreshold swing can be calculated from the I-V curve using the following definition

$$SS = \log(10)\frac{dV_g}{d(\log(I_d))}. \tag{2.2}$$

In which V_g is the gate voltage and I_d the current through the transistor. The subthreshold swing is temperature dependent, and can be calculated using

$$SS = \log(10)\left(\frac{k_B T}{e}\right)\left(\frac{C_{ox} + C_D}{C_{ox}}\right), \tag{2.3}$$

here k_B is the Boltzmann constant, e the elementary charge, T the temperature, C_{ox} the geometric gate capacitance and C_D the capacitance of the interference traps in the channel.

2.2 Single quantum dots

Quantum dots are zero-dimensional objects with trapped charge carriers. Due to the similarity to the confinement potential of atoms, they are often referred to as artificial atoms. Semiconductor quantum dots are often formed by locally depleting the semiconductor of charge carriers to form a confinement potential which holds a discrete amount of charge carriers. In this case however the quantum dots are formed by accumulating charges under the gates. Other examples of quantum dots include strain induced layer growth or nanoscale colloidal particles. The name artificial atom arises from the fact that the wavefunctions of the electrons in such a small region behave like the wavefunction of an single atom.

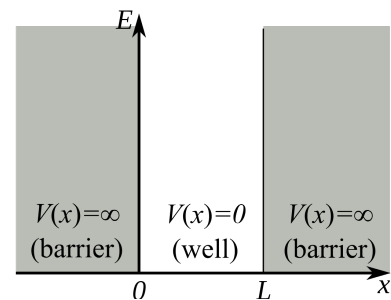

Figure 2.2: An illustration of the infinitely deep square well potential, figure taken from [44]

In the simplest approximation the potential of a QD is described as an infinitely deep square well (see figure 2.2). This model is sometimes called the particle in a box model [45]. In this model the wavefunctions are described by the standing wave

approximation. This means that the wavefunction can be described by the following equation:

$$\Psi(x) = \sqrt{\frac{2}{L}} \sin\left(\frac{n\pi}{L} x\right). \tag{2.4}$$

Where L is the width of the well and n is a positive integer. The energy of this system is

$$E_n = \frac{n^2 \pi^2 \hbar^2}{2m^* L^2}, \tag{2.5}$$

here m^* is the effective mass of the electron or hole in the potential well and $\hbar$ is the reduced Planck constant.

Another commonly used model to describe the energy of the states in a quantum dot is the constant interaction model [46]. Two crucial assumptions are made, the first one is that Coulomb interaction between the electrons in the dot or the environment is modelled with a constant capacitance C. This capacitance is the sum of capacitance of the source, drain and gate. Other capacitances in the system can also be added to this capacitance. The second assumption is that the single particle energy is unaffected by interactions. The ground state energy of the Nth electron on the dot is modelled by

$$U(N) = \frac{(-e(N - N_0) + C_s V_s + C_d V_d + C_g V_g)^2}{2C} + \sum_N E_n(B), \tag{2.6}$$

in which N_0 is the amount of electrons on the dot when $V_g = 0$, V_g is the gate voltage V_s and V_d are the source and drain voltages respectively, C_g, C_s and C_d are the capacitances of the gate source and drain and E_n are the single-particle energy levels, which depends on the potential taken to model the quantum dot. using equation 2.6 we can determine the electrochemical potential of the dot

$$\mu(N) = U(N) - U(N-1) = \left(N - N_0 - \frac{1}{2}\right) E_c - \frac{E_c}{e} \left(C_s V_S + C_d V_d + C_g V_g\right) + E_n. \tag{2.7}$$

With $E_c = \frac{e^2}{C}$ the charging energy of the dot. This equation describes the transition between the N-electron ground state and the (N-1)-electron ground state. The spacing between two adjacent ground state electrochemical potentials is the so called addition energy defined by

$$E_{add}(N) = \mu(N+1) - \mu(N) = E_c + \Delta E. \tag{2.8}$$

ΔE is energy spacing between the two quantum levels, in case of degenerate levels this can be zero.

Transport through a quantum dot is only possible when an electrochemical potential of the quantum dot lies between the source and drain electrochemical potential. Otherwise the transport is blocked – this blocked regime is called Coulomb blockade. By changing the gate voltage of the gate defining the quantum dot, thus changing the electrochemical potential of the quantum dot, Coulomb peaks can be observed. These are current spikes of an sequential electrons tunnelling through the quantum dot. By counting the coulomb peaks, the number of electrons on the dot can be counted. By looking at the spacing of the peaks, the addition energy of the dot can be extracted.

2.3 Double quantum dots

When two quantum dots are placed in an array the electronic and transport properties change, as both dots can influence each other and, transport is only possible after tunnelling through both dots. The models described in the previous section are still valid, although extra terms for interaction are added to describe the double dot system [47]. The dot energy is modelled by

$$U(N_1, N_2) = \frac{1}{2} \left(N_1^2 E_{c1} + N_2^2 E_{c2}\right) + N_1 N_2 E_{Cm} + f\left(V_{g1}, V_{g2}\right), \tag{2.9}$$

with

$$\begin{aligned} f\left(V_{g1}, V_{g2}\right) =& \frac{1}{e}\left[C_{g1}V_{g1}\left(N_1 E_{c1} + N_2 E_{Cm}\right) + C_{g2}V_{g2}\left(N_1 E_{Cm} + N_2 E_{c2}\right)\right] \\ &+ \frac{1}{e^2}\left[\frac{1}{2}\left(C_{g1}^2 V_{g1}^2 E_{c1} + C_{g2}^2 V_{g2}^2 E_{c2}\right) + C_{g1}V_{g1}C_{g2}V_{g2}E_{Cm}\right] \end{aligned} . \tag{2.10}$$

In equations 2.9 and 2.10 $V_{g1,2}$ is the gate voltage of dot 1 or 2, $C_{g1,2}$ is the capacitances of gate 1 or 2, $E_{c1,2}$ is the charging energy of each dot, E_{Cm} is the electrostatic coupling energy, which can be related to the tunnel coupling (t_c) between the dots. The electrochemical potential is still defined by equation 2.7. N_1, or N_2 can be used to differentiate between the two dots. When the coupling capacitance (C_m) is zero, we obtain the limiting case that the energy can be modelled by the sum of two independent dot energies. In the other limit (when $\frac{C_m}{C_{1/2}} \to 1$) the electrostatic energy is given by

$$U(N_1, N_2) = \frac{\left(e(N_1 + N_2) + C_{g1}V_{g1} + C_{g2}V_{g2}\right)^2}{2\left(\widetilde{C_1} + \widetilde{C_2}\right)}, \tag{2.11}$$

where $\widetilde{C}_{1/2} = C_{1/2} - C_m$ is the capacitance of the dot.

Equipped with these equations we can start drawing stability diagrams of the double quantum dot (DQD) system. The typical stability diagrams for the three regimes can be found in figure 2.3, in (a) a stability diagram for two completely decoupled QDs is found, in (b) the typical honeycomb structure of a DQD stystem is shown, the regime in which $\frac{C_m}{C_{1/2}} \to 1$ is shown in (c). In the remainder of this chapter we will focus on the diagram shown in figure 2.3(b).

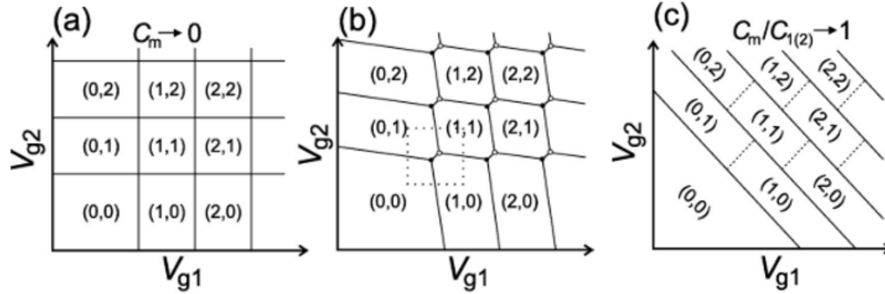

Figure 2.3: The stability diagram for the three main regimes of a double quantum dot system, with in (a) in case of no mutual capacitance (C_m), (b) intermediate mutual capacitance regime and in (c) the regime in which $\frac{C_m}{C_{1/2}} \to 1$. Figure taken from: [47]

Indicated by the dotted square area there are two triple points of different kind: one for the electron and one for the hole transport process. A zoom in of this area can be found in figure 2.4a. Along the solid lines one of the electrochemical potentials is equal to the source/drain, while at the dashed lines he electrochemical potentials of the dot align, but no transport is possible.

In figure 2.4b the triple points are shown for a finite bias. The triple points are now expanded in two triangular regions in which a current flows through the double dots. Only along the baseline of triangles resonant tunnelling is possible, while in the rest of the triangular areas inelastic and co-tunnelling events are responsible for the current. When the bias is increased the triangles can start to overlap forming a single structure. Also, with increasing bias additional transitions indicating resonant transport via the excited orbital states become visible.

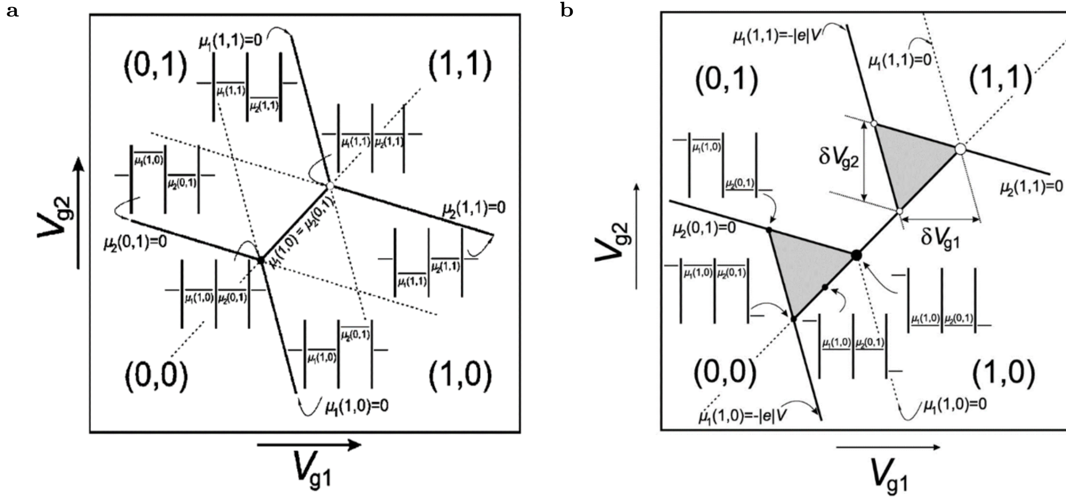

Figure 2.4: Close ups of the area around the triple points in figure 2.3. In (a) the four different charge states are separated by the solid lines. The dashed lines indicate the points at which the chemical potentials align but there is no current through the double dot system. In (b) the same region is shown with a finite bias applied, the solid lines again separate the charge domains. Transport is possible within the gray region, along the base line of the triangle resonant tunnelling is possible. In the rest of the triangle transport is due to inelastic tunnelling and co-tunnelling. Figures adapted from [47]

Spin states

When considering transport through quantum dots the spin property of the electrons also has a big influence on the transport. We consider, the regime in which there are two electrons in the quantum dots. In this case, the electrons can form singlet and triplet states [45]. As usual, the spin part of the wavefunction for the singlet state is antisymmetric and for the triplet state symmetric. In energy space there are two important quantities when looking at the singlet and triplet states: If the electrons are on a different dot the lowest energy singlet and triplet state are separated by the exchange interaction energy (J). When the electrons are on the same dot the separation between the singlet and triplet state is the singlet-triplet splitting (ΔST). An in detail explanation of transport through charge transitions and their behaviour in an external magnetic field can be found in chapter 3.

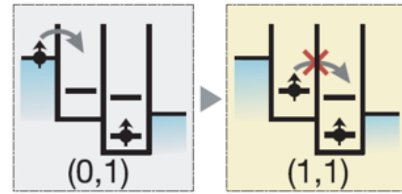

Figure 2.5: An illustration of PSB in a double dot system, figure take from [13]

Now that the spin states of the electrons are introduced we should also consider the Pauli-exclusion principle which states that no particles with the same quantum number (often only spin state is used) can be in the same energy level. This leads to a new type of blockade in the double dot system, which is called Pauli spin blockade (PSB). An illustration of this effect is found in figure 2.5. In this illustration we see that an electron with spin up can tunnel onto the left dot but cannot tunnel further to the right dot, due to the Pauli exclusion principle. An electron with spin down, on the other hand, would just tunnel through the whole system resulting in a measurable current. PSB can bee seen in the bias triangles by changing the sign of the bias voltage. If there is a blockade for one of the bias directions, the baseline of the blockaded bias triangle is strongly suppressed in current [48]. The spin blockade can be lifted by applying an external magnetic field. In chapter 3 we will explain the details behind spin blockade lifting through the spin-orbit interac-

tion. Hyperfine interaction is another common spin blockade lifting mechanism and is explained in Section 2.3.

Valley states

Besides spin states there is a third degree of freedom for electrons in silicon quantum dot systems, this degree of freedom is called valley states. Valley states are not available for holes in silicon. These valleys are local minima in the conduction band of the material and are degenerate in energy in bulk silicon. Silicon has a six-fold symmetric Brillouin zone, which leads to six local minima/valleys. In silicon quantum dots the degeneracy of two of these valley states is lifted due to the confinement in the quantum dot [49]. The splitting of these valley states depends on the electric fields confining the electrons in the dots, and is thus gate tunable [50]. These valley states can also block transport through a double quantum dot system, which is what we would call a valley-blockade [51]. When combined with Pauli spin blockade a so called spin-valley blockade can be visible. The blockade can then be lifted through two separate mechanisms: A spin flip event, caused by either the hyperfine (predominantly present in electron systems see section 2.3) or spin-orbit interaction. Secondly, by mixing valley states which happens as an electron with the same spin is filled into another quantum state of the same dot, which lifts the blockade [52].

Hyperfine interaction

The hyperfine interaction is the interaction between the spin state of the nucleus and the spin state of the electrons (or holes) in the semiconductor (or any other material for that matter). The spin state of the nuclei generate a magnetic field which couples to the electrons. In the volume of a quantum dot typically $10^3 - 10^5$ nuclei are present all with a fluctuating spin. The average field of these nuclei adds up to the Overhauser field (B_N) [53]. In the picture of an artificial atom the electron in the quantum dot starts precessing around the Overhauser field. However, the hyperfine field fluctuates strongly in amplitude and direction from dot to dot and over time. This causes the electron spin to dephase from its original well defined spin-state to an incoherent state. This is detrimental for qubits as this limits the amount of time the spin is coherent and thus useful for qubit operations.

If a double system is in the spin blockade configuration the hyperfine interaction can lift the PSB. The Overhauser field can mix orbital and spin degrees of freedom which can lead to a spin flip. A second type of spin flip happens when a spin flips and also flips the spin of a nuclei [54], this is also called a spin-flip-flop event. The fluctuations in the Hyperfine field are usually of the order of a few mT [55], which can be explained by the fact that there is a mismatch between the Bohr magneton for electrons/holes and nuclei. This leads to a difference in Zeeman energy at higher fields and thus preventing a spin-flip-flop event to happen. Spin blockade, as mentioned earlier, results in vanishing of the baseline of the blockaded bias triangle, however the hyperfine interaction causes the baseline of the triangle to be visible around zero field.

In this chapter we have explained the basic physics of quantum dots and introduced Pauli spin blockade. Two Pauli spin blockade lifting mechanisms have been introduced. In the next chapter we will introduce the spin-orbit interaction which is another spin blockade lifting mechanism and one of the main topic of this thesis.

Chapter 3

Spin orbit interaction

In this chapter the influence of the spin-orbit interaction (SOI) on the spin states and transport through a double quantum dot system will be discussed. First, the theoretical framework describing the SOI will be explored then the origin of SOI in silicon quantum dots will be worked out. Finally, we will model the spin-orbit interaction in a double quantum dot system.

3.1 Origin of the spin-orbit interaction

As the name suggests SOI is the interaction between the orbital and spin wavefunctions. This is a relativistic effect, but can be modelled using symmetry arguments of the system. There are two types of asymmetries, which cause SOI: bulk inversion asymmetry (BIA) and structural inversion asymmetry (SIA) [56]. The lattice structure of the crystal plays a big role in determining which of these is dominant.

BIA is predominantly present in systems without inversion symmetry, a common example of this are crystals with a zincblende lattice structure. To approximate this effect a third order approximation can be made, this term is named Dresselhaus term [57]. This term can be described by

$$H_D \propto k_x \left(k_y^2 - k_z^2\right) \sigma_x + k_y \left(k_z^2 - k_x^2\right) \sigma_y + k_z \left(k_x^2 - k_y^2\right) \sigma_z, \tag{3.1}$$

in which $k_{x,y,z}$ are the respective momentum vector components and $\sigma_{x,y,z}$ are the Pauli matrices describing the different spin states.

SIA was originally predicted to be a bulk effect but more recently it has also been proven and shown to exists in lower dimensional structures [58]. This effect is a combination of the orbital effects and an asymmetry in the crystal potential. This effect is named after Emmanual Rashba who discovered the effect in 1959 [59], the well known Rashba hamiltonian is

$$H_R = -\alpha_R(\sigma \times \mathbf{k}), \tag{3.2}$$

where $\mathbf{k}$ is the momentum vector and σ is the vector of Pauli matrices.

Spin-orbit interaction in the context of silicon double quantum dots

In silicon systems there is no Dresselhaus SOI due to the fact that silicon is bulk inversion symmetric. It has been predicted that in silicon nanowires (FinFET device can be modelled as nanowires) a newly found type of Rashba SOI is present called direct Rashba spin-orbit interaction (DRSOI) [26]. This interaction is found to be controllable by electric fields. The growth direction of the nanowires also has a large influence of the strength of the Rashba SOI [1].

The presence of SOI is both a burden and benefit for spin qubits, as on one hand it limits the coherence time of the qubit, as charge noise is coupled to the spin via the SOI. On the other hand

SOI enables the use of electric dipole induced spin resonance (EDSR) to operate a qubit. In the simple picture of a the Pauli spin blockade, as described in chapter 2, the SOI can flip a spin and thus lift the blockade. It has been predicted [60] and shown [61] that in silicon hole devices which have a strong SOI, this leads to a disappearance of the ground-state transition of a blockaded bias triangle. To observe this effect an external magnetic field can be used. At a finite field the blockade becomes lifted and a transport signal is observed. The width of this spin-blockade gap is given by the interdot tunnel coupling and strength of the SOI [62]. The external magnetic field gives a perpendicular component to the spin-orbit vector, this component enables spin relaxation. This means there is an expected leakage current with a magnetic field applied and no (or less) current without a magnetic field applied.

Another important feature of SOI is the singlet-triplet anticrossing, or avoided crossing, at high magnetic fields. This avoided crossing was first seen by J.R Petta and D.C Ralph in metallic nanoparticles [63], later a simple model was developed to extract the spin-orbit strength in a double dot system [64]. The SOI strength can be converted to a SOI length, which is an important parameter when comparing the spin-orbit strength between different material platforms. Later in this work we will try to use this anticrossing to extract the SOI strength in our system. The spin-orbit length can be calculated from the spin-orbit energy by

$$\Delta_{so} = \frac{E_z}{sqrt2} \frac{r_{12}}{\lambda_{so}}, \tag{3.3}$$

here E_z is the Zeeman energy, r_{12} the effective distance between the two electrons and λ_{so} the spin-orbit length. In recent works this anticrossing has been seen in InSb and InAs nanowires [65, 66] and several silicon systems [61, 67].

3.2 A simple model for the spin-orbit interaction in double quantum dots

In this section we build a simple model for the spin-orbit interaction and other interactions within a double quantum dot system. We start with the time-independent Schrödinger equation and expand the Hamiltonian for the different bases states within a DQD system. We can then solve for the Eigenstates of this Hamiltonian and obtain information about the bases states of a DQD system.

As a basis model, Hamiltonians are taken from Nadj-Perge et. al (2012) [66] and Stepanenko et al. (2012) [68]. We then define the following basis states for our model Hamiltonian: $S(0,2)$, $T_-(0,2)$, $T_0(0,2)$, $T_+(0,2)$, $S(1,1)$, $T_-(1,1)$, $T_0(1,1)$, $T_+(1,1)$. We then obtain the following Hamiltonian

$$H = \begin{pmatrix} -\epsilon & \Delta_{so} & 0 & 0 & -t & -i\cdot t_+ & i\cdot t_0 & i\cdot t_+ \\ \Delta_{so} & \Delta ST-\epsilon-B_E & 0 & 0 & -i\cdot t_+ & t_2 & 0 & 0 \\ 0 & 0 & \Delta ST-\epsilon & 0 & i\cdot t_0 & 0 & t_2 & 0 \\ 0 & 0 & 0 & \Delta ST-\epsilon+B_E & i\cdot t_+ & 0 & 0 & t_2 \\ -t & i\cdot t_+ & -i\cdot t_0 & -i\cdot t_+ & -V & 0 & \delta B & 0 \\ i\cdot t_+ & t_2 & 0 & 0 & 0 & -V-B_E & 0 & 0 \\ -i\cdot t_0 & 0 & t_2 & 0 & \delta B & 0 & -V & 0 \\ -i\cdot t_+ & 0 & 0 & t_2 & 0 & 0 & 0 & -V+B_E \end{pmatrix}. \tag{3.4}$$

In the table 3.1 the symbols and different interactions present in this Hamiltonian are explained. To further simplify our model we assume that the g-factor in both dots in the DQD system is the same and turn off the spin-orbit interaction between the $T_{-/+}(1,1)$ and $S(0,2)$ states. Which

leads to the following Hamiltonian

$$H = \begin{pmatrix} -\epsilon & \Delta_{so} & 0 & 0 & -t & 0 & 0 & 0 \\ \Delta_{so} & \Delta ST - \epsilon - B_E & 0 & 0 & 0 & t_2 & 0 & 0 \\ 0 & 0 & \Delta ST - \epsilon & 0 & 0 & 0 & t_2 & 0 \\ 0 & 0 & 0 & \Delta ST - \epsilon + B_E & 0 & 0 & 0 & t_2 \\ -t & 0 & 0 & 0 & -V & 0 & 0 & 0 \\ 0 & t_2 & 0 & 0 & 0 & -V - B_E & 0 & 0 \\ 0 & 0 & t_2 & 0 & 0 & 0 & -V & 0 \\ 0 & 0 & 0 & t_2 & 0 & 0 & 0 & -V + B_E \end{pmatrix}. \tag{3.5}$$

Table 3.1: Explanation of the parameters in model Hamiltonian in equation 3.4

Symbol	**Parameter**
i	Imaginary unit
ϵ	Detuning energy between $S(1,1)$ and $S(0,2)$
t	Tunnelling coupling between $S(1,1)$ and $S(0,2)$
t_2	Tunnelling coupling between $T(1,1)$ and $T(0,2)$
t_+	Spin-orbit interaction between $T_{-/+}(1,1)$ and $S(0,2)$
t_0	Spin-orbit interaction between $T(1,1)$ and $S(0,2)$
ΔST	Singlet triplet splitting
Δ_{so}	Spin-orbit energy, or width of the anticrossing
V	Coulomb advantage for $(1,1)$ states
$B_E = (g_1 + g_2)\mu_B B/2$	External magnetic field in energy
$\delta B = (g_1 - g_2) mu_B B$	Magnetic field energy due to variations in g-factor between the quantum dots
$g_{1/2}$	effective g-factor of dot 1 or 2

To solve the Hamiltonian the linear algebra package in the Numpy Python library is used. Afterwards the eigenstates need to be sorted. This is done by maximizing the L_∞-norm of the Eigenvectors. Which takes the maximum of the absolute value of the eigenvectors, by sorting these for every transition we can obtain a smooth result.

3.3 Simulation results

In this section we will first test the model by performing some rudimentary test simulations of well known results. After that we will simulate a full system and try to explain transitions in old measurements.

The first test will be to simulate the Zeeman splitting of the different states in the a double quantum dot system. For this simulation all spin-orbit factors are set to 0, to simplify the results. The results of the simulation are shown in figure 3.1. We can clearly see that the triplet states with a net spin up or down diverge from the triplet state without a net spin, which is the expected behaviour for the triplet states. The singlet-triplet splitting and the Coulomb advantage are also visible in this plot.

As a second test we vary the detuning and plot the Eigenenergies of the states. The results of this test are displayed in figure 3.2, with in 3.2b a zoom in of the crossings visible in 3.2a. This simulation is done at a finite magnetic field such that the triplet states are split up, and we can identify the different interactions in the model. When looking at the crossings we see that due to the tunnel coupling between $(1,1)$ and $(0,2)$ states a gap forms. This gap changes depending

on the size of the tunnel coupling. In this case the tunnel coupling between $S(1,1)$ and $S(0,2)$ is twice as strong as the tunnel coupling between the triplet states. If the tunnel coupling was turned off the states would cross without any interaction. There is only a tunnel coupling present for states with the same spin quantum number.

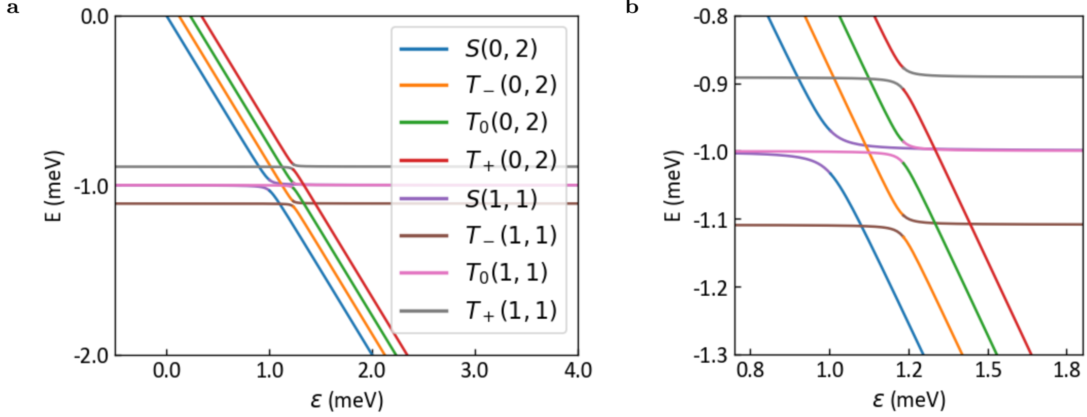

Figure 3.2: Detuning versus energy simulation of the simplified model at a finite magnetic field without spin-orbit interaction

Both tests are actually not directly measurable in a double quantum dot system. We can, however, measure transitions in which transport happens. These are transitions from a $(1,1)$ state to a $(0,2)$ state. To simulate such measurements we loop over different magnetic field configurations and track the position of these $(1,1)$ to $(0,2)$ intersections in figure 3.2b. The result of such a simulation, now with the spin-orbit interaction turned on, is shown in figure 3.3. To dissect this graph, the first important point to understand is that everything below zero detuning ($\epsilon = 0$) is in the Coulomb blockade, meaning that these transitions are unmeasurable. The sharp transitions/steps visible in the plot are artefacts due to limitations in step size, in a measurement these lines would be continuous.

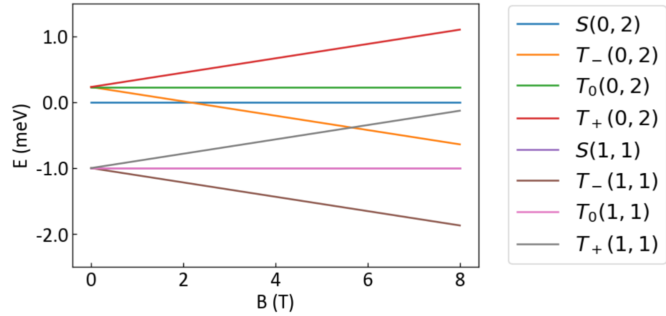

Figure 3.1: Simulation of the Zeeman splitting of the states in a double dot system.

We will first look at the most important and best understood transitions in figure 3.3, which are the $T_{-}(1,1) \rightarrow T_{-}(0,2)$ (blue) and $T_{-}(1,1) \rightarrow S(0,2)$ (red) transitions. For increasing magnetic field the $S(0,2)$ and $T_{-}(0,2)$ states get closer together until they are degenerate and start to separate again. Instead of crossing the red and blue lines show an anticrossing due state mixing by the spin-orbit interaction. The width of this anticrossing can be related to the SOI strength [64].

Other transitions which have been measured before are the $S(1,1) \rightarrow T_{-}(0,2)$ (purple) and $T_{+}(1,1) \rightarrow T_{-}(0,2)$ (gray) transitions. These transitions have been seen by Pfund et al. in InAs nanowires [65]. Since these transitions require higher order spin flips the intensity of these is expected to be lower then the earlier mentioned transitions. The singlet-singlet transition (pink),

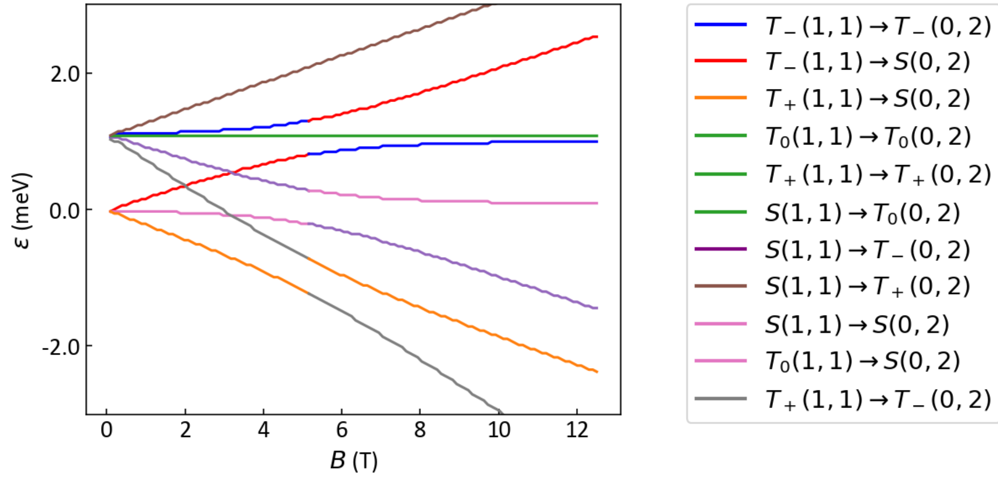

Figure 3.3: Results of tracking candidate transport transitions for a large magnetic field range

becomes visible due to bias heating.

At a magnetic field of 6 T we observe two other anticrossings between the purple ($S(1,1) \rightarrow T_{-}(0,2)$) and pink ($S(1,1) \rightarrow S(0,2)$) transitions and the orange ($T_{+}(1,1) \rightarrow S(0,2)$) and gray ($T_{+}(1,1) \rightarrow T_{-}(0,2)$) transitions. These transitions should show the anticrossing as well, however these anticrossings have never been experimentally observed. The $T_{+}(1,1) \rightarrow S(0,2)$ (orange) to $T_{+}(1,1) \rightarrow T_{-}(0,2)$ (gray) anticrossing can never be observed due to the Coulomb blockade, the $S(1,1) \rightarrow S(0,2)$ (pink) to $S(1,1) \rightarrow T_{-}(0,2)$ (purple) transition should be measurable, to obtain a better idea of when this anticrossing becomes visible a full density of states simulation has to be performed. The degenerate transitions: $T_0(1,1) \rightarrow T_0(0,2)$, $T_{+}(1,1) \rightarrow T_{+}(0,2)$,$S(1,1) \rightarrow T_(0,2)$ in green are triplet tunnelling transitions or in case of the $S(1,1) \rightarrow T_0(0,2)$ transition a higher order spin-orbit spin flip transition. Both of which are unlikely to happen either do to triplet-singlet relaxation or limited strength of the SOI.

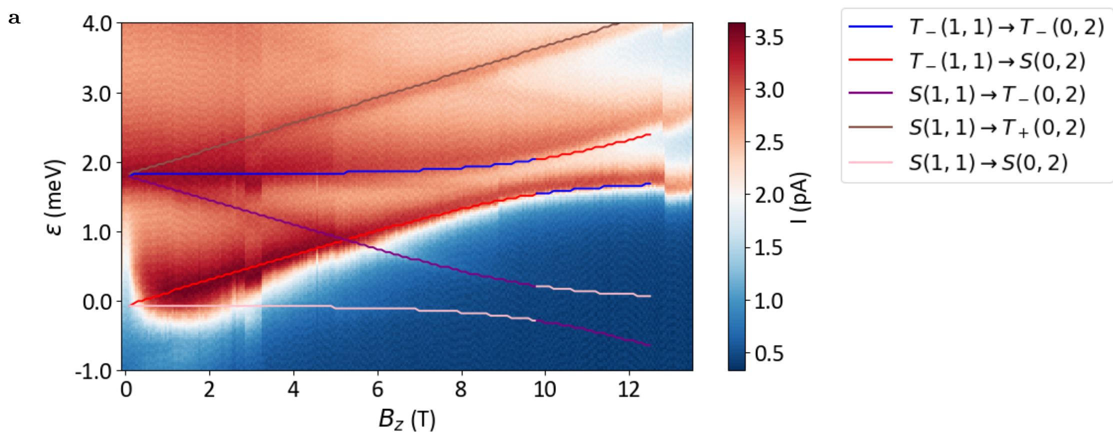

Figure 3.4: Overlay of the model on data taken in our group the data is overlaid with the model.

To show an application of this model we will overlay this simulation over data taken in the group. In figure 3.4 these results are plotted. The used parameters for this simulation can be found in appendix A. In figure 3.4 we see two lines diagonal lines originating from the flat line at 2 meV detuning, also there is a faint line visible going straight at the zero detuning line, these

transitions correspond almost exactly to our model. Another striking observation in this data is the slight bending of the transition which coincides with the $S(1,1) \rightarrow T_{-}(0,2)$ transition, this might be a faint sign of the spin-orbit anticrossing between this transition and the singlet-singlet transition (barely visible on the zero detuning line). This anticrossing is much lower in intensity due to the fact that the Singlet-Singlet will bend down and go in the Coulomb blockade and the $S(1,1) \rightarrow T_{-}(0,2)$ transition is a spin flip transition, so this is less likely to occur.

To conclude this chapter we can state that model presented in equation 3.5 can be used to identify unknown transitions in Pauli spin blockade measurements. It is however unable to predict what the intensity of these transitions is, for that we would have to implement a density of states approach and know all the relevant tunnel rates. This would require significant extra effort. For now this model can be useful for identifying charge transitions in experiments in a double quantum dot system with a strong spin-orbit coupling.

Chapter 4

Experimental setup

In this chapter, we explain the details of the setup used to perform the Pauli spin blockade measurements. We will also briefly discuss the types of devices used during this research. Finally, we will get into the details of setting up a variable temperature insert (VTI) for use as a cryogenic probe station and the custom software made for its operation.

4.1 Devices

The devices used in this work are based on the FinFET transistor architecture. Devices are fabricated at IBM in Zürich. The current state of the art for these devices is described in Geyer et. al. [29]. Most of this work is performed on an older simpler design procedure, however we will still shortly introduce the newer device lay-out for the context of this work.

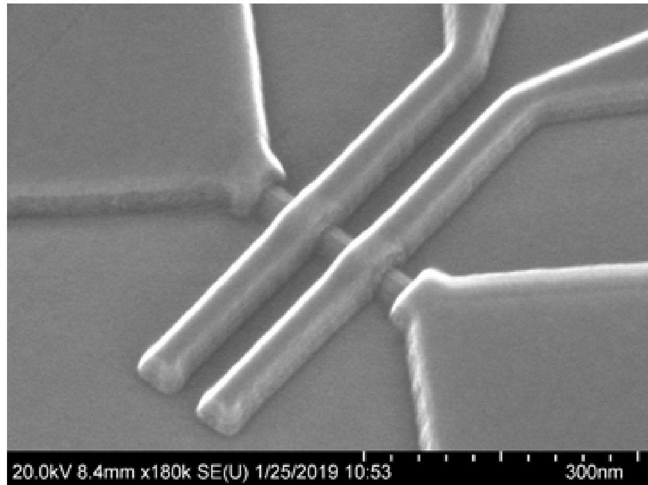

Figure 4.1: A SEM image of a single gate layer double quantum dot device.

The simplest and most used design in this work is a silicon fin with two nanogates positioned over the fin, as described in [28]. A scanning electron microscopy (SEM) image of such a single-gate layer double dot device can be found in figure 4.1. In this figure, we see the fin of the FinFET going from left to right, with two nanogates wrapped around. These nanogates are used to form the quantum dots by accumulation of charge carriers. At the ends of the fin there are two triangular lead gates visible. These gates accumulate a two dimensional hole gas to connect to source and drain to the fin. With this gate we also have rough control over the Schottky barrier between source/drain and the channel. Furthermore small deviations in the lead gates can lead to changes in the dot lead tunnel barrier.

A more complicated design contains two gate layers. In these single quantum dot devices with two barrier gates between the leads and plunger gate and operate it as a double quantum dot device. This is done by using the plunger gate as interdot barrier and accumulate the dots under

the barrier gates. This way there is only control of the tunnel rates in and out of the dots, through the lead gates, but there is control over the interdot tunneling rate. The fabrication procedure for these devices is described in Geyer et al. (2020) [29]. A tunnelling electron microscope (TEM) image of the crosssection along the fin of such a device can be found in figure 4.2. In this image, we see the two lead gates in L1/L2 and G2/G3 two barrier gates and G1 a plunger gate. To have more control over every experimental parameters, fabrication of devices with two plungers and three barriers is an ongoing process.

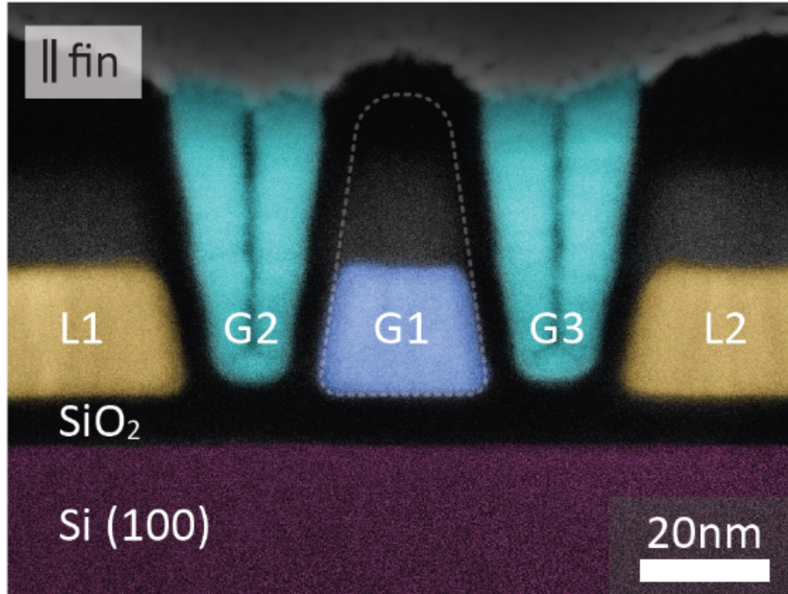

Figure 4.2: A crossectional TEM image along the fin of a double gate layer single quantum dot device. Figure taken from [29]

The silicides forming the ohmic contacts to the fin of the aforementioned devices come in two variants, with the most common one being PtSi which has a work function in the valence band. The other variant uses NiSi as silicide which has the work function in the band gap. The PtSi devices are preferably operated for holes (Applying a large positive voltage still enables use of the electron side) while the NiSi devices can be used as ambipolar devices operating for both holes and electrons.

The devices produced have different parameters for the spacing of the gates and gate lengths. Several devices where tested during this project. The device used to obtain the results in Chapter 5 is an ambipolar single gate layer double quantum dot device, with the following dimension: A gate length of 15 nm and spacing between the gates of 40 nm, and a fin width of 25 nm.

4.1.1 Tuning double quantum dots

To find Pauli spin blockade in a double quantum dot device, a stable regime for the double dot system has to be found. This stable regime differs from device to device depending on the device parameters and uncontrollable effects like local defects in or near the device.

To characterise our FinFET devices, we first check for gate leakage at room temperature. Then we check the pinch the channel with the nanogates and check for ohmic behaviour of the IV curve. If a device shows no leakage and its IV curve behaves ohmic, it is cooled down. Once the device is cold, measurements start by establishing the lead gate voltage for which the device turns on and

shows an ohmic IV curve. The next step is to take pinch off curves with each of the nano gates (all gates excluding the lead gates).

The pinch-off curves are use to determine the search range for a double dot regime. In a single-gate-layer-device we start by sweeping the plunger gates from just before the pinch-off to after the pinch off. This procedure is repeated for several lead gate voltages to find double dot features near the pinch-off voltage of the nanogates.

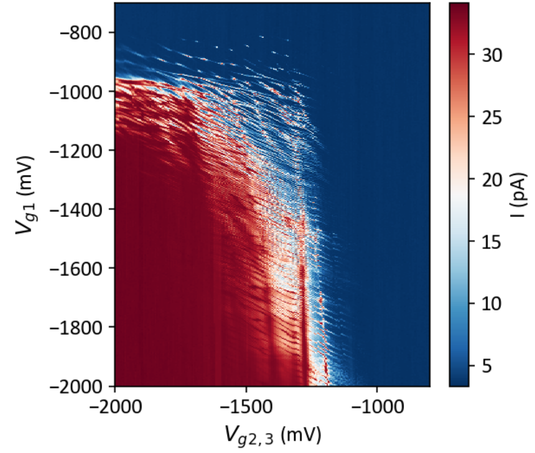

Figure 4.3: A barrier versus plunger gate voltage scan for a double-gate-layer single quantum dot device. The barrier gate is g_1 and $g_{2,3}$ are the plunger gates

For a double gate layer device the process starts by scanning the plunger gate versus the two barrier gates (usually one would scan the two plungers versus the interdot barier gate, but here the plunger gate acts as interdot barrier gate), an example of such a measurement is found in figure 4.3. In the bottom left, we see diagonal lines indicative of a single dot regime, in the middle at the top a few spot can be seen; this is the typical region where the double dot region is found. This can be understood by looking at the different regimes figure 2.3. In the bottom right the tunnel coupling between the two dots is so high, that in essence a big single dot is formed. In the top left of the graph a single dot is formed under the barrier gate with the outer (plunger) gates acting as coupling leads from the reservoir. In the spotted region the gates are tuned such that the middle gate acts as barrier and the dots form under the outer plunger gates.

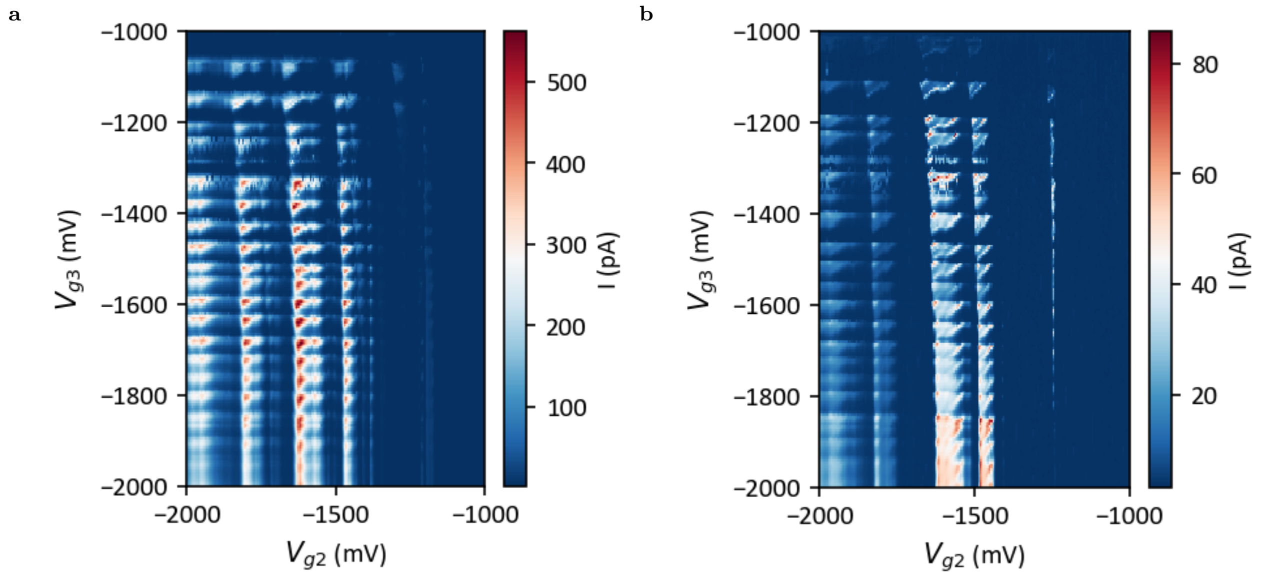

Figure 4.4: Examples of stability diagrams showing bias triangles. The difference between the two measurements is the tunnel coupling, in (a) the tunnel coupling is strong while in (b) it is weaker.

Once the double dot region is identified several plunger sweeps are attempted for different interdot barrier gate voltages. Two examples, of these sweeps are shown in figure 4.4. In figure 4.4a the interdot barrier gate is too transparent and there is a lot of inelastic tunneling and co-tunneling visible. This can be identified by the large tails and in general blurry areas around the bias triangles. In figure 4.4b a nice and typical double dot stability diagram is seen. This stability diagram is still not perfect as some local defect causes horizontal line of disorder at $V_{g3} \approx -1325$ mV. Also we see an abrupt cut off of the triangles at $V_{g2} \approx -1250$ mV, this is most likely a sign that the fewer hole regime transport is limited by tunnelling to the dots; for this plunger gate voltage the tunnel rate is suddenly quenched. On the right side we can also see the effect of orbitals on the stability diagrams. If a set of bias triangles is formed by electrons in the same orbital the spacing between the triangles is even, but here we see several large gaps indicating different orbital occupations.

4.2 MCK-76 dilution refrigerator setup

For the experiments on Pauli spin blockade, a MCK-76 dilution refrigerator from Leiden Cryogenics is used. The fridge is either operated at 4.2 K by dipping the inster in the liquid helium dewar. In most cases, the set-up is cooled down further to 500 mk by pumping on the 1K pot and circulating a small volume of He_3 through the mixing chamber.

The most important features of this setup are the magnet and the sample rotator. The dewar contains a 14 T magnet. Furthermore, the sample stage contains an attocube rotator to rotate the sample to different field directions. The sample stage can either be mounted in in-plane mode or out-of-plane mode. In both modes a 360 degree rotation can be made. During this project the standard configuration is using the out-of-plane magnetic field directions.

For data acquisition a National Instruments data acquisition card (NI-DAQ 6366). A Basel Instruments low noise high resolution (LNHR) DAC is used as a voltage source for the devices. Furthermore Basel Instruments IV-converters are used to amplify the current and convert it to a voltage signal from the device for the NI-DAQ. A diagram of the electrical set-up can be found in appendix B.

4.3 The cryo-prober setup

The Cryo-prober is a custom built probe station able to operate at cryogenic temperatures by attaching it to a variable temperature insert (VTI). In this section the adaptations to the VTI are explained as well as the set-up of the probe station it self. Finally, a short introduction is given to the tailor made software written for this set-up.

4.3.1 Variable temperature insert

A variable temperature insert (VTI) is a insert which is usually inserted in a bath of liquid helium to cool the sample to 4.2 K (the temperature of the helium bath). A VTI is usually equipped with a heater and a 1 K pot. By operating the 1 K pot, temperatures down to approximately 1.5 K can be reached. The heater can be used to have more precise control of the temperature, for our experiments the heater is not used.

The 1 K pot of a cryogenic systems works by opening a small needle valve at the inlet to slowly fill up the 1 K pot with liquid Helium. Then by pumping on the 1 K pot a flow is generated. With this flow heat is removed from the 1 K pot and it can cool the sample stage via a thermal

connection. By controlling the amount of liquid Helium flowing in and out of the 1 K pot (using the needle valve and pump speed) the temperature can be approximately set to a desired value.

The basis for the VTI used in this project is a 70 mm bore diameter VTI from ICE Oxford. The VTI is equipped with 32 wires, of which 16 are for DC measurements and the other 16 are low ohmic wires to control the piezoelectric positioners which move the sample stage. For the DC wires CuSn6 with a diameter of 0.125 mm is used. For the piezo positioners Ms90, a brass alloy (CuZn10), with a diameter of 0.25 mm is used. Especially the choice of wires for the piezo positioners is critical as low ohmic wiring is required to be able to properly operate the piezo steppers. However low ohmic wires usually have a high thermal conductivity, causing more heating at low temperatures.

4.3.2 Piezo positioners

To be able to reach multiple devices on a single chip, the chip is mounted on a stage with positioners made by Attocube. These positioners are rated for operation between 1 K and 370 K. The postioners are embedded in a sample cage which can be mounted to the insert or placed under a microscope. An image of the sample cage can be seen in figure 4.5.

For x and y movement Attocube ANPx341 slip-stick positioners are used. These, have a maximum range of 20 mm. However, due to the limited width of the cage, a maximum range of approximately 8 mm can be reached. With this range approximately 70 of the 192 devices on a 2 x 2 cm chip can be reached. To make contact with the chip the sample stage can be moved in the z direction using a ANPz102 positioner. An optional stage rotator of the type ANR101 can be installed to rotate the chip. For experiments during this project this rotator was not installed. The positioners are controlled using an ANC-350 controller, which can be operated manually using the controls on the controller or via software on the connected computer. The postioners are read-out using a resistive readout, in which the resistance of a variable resistor changes with position of the piezo positioner.

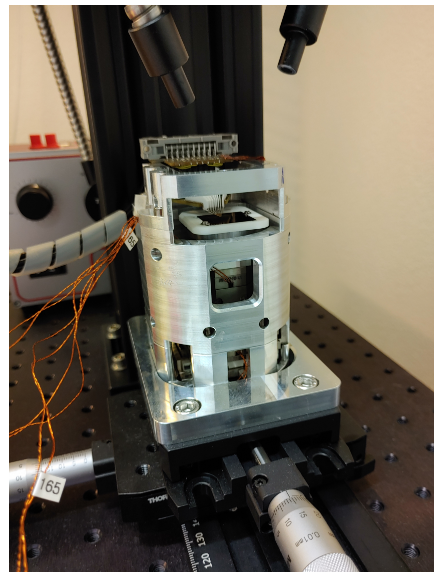

Figure 4.5: A photograph of the cryoprobers sample stage and cage. In white a ceramic, electrically insulating, chip holder. Slightly above the chip holder the probecard with needles. Hidden in the Titanium housing are the piezo positioners.

A probe card is mounted on top of the cage. This probe card is stationary and specifically designed for the bond pad lay-out used in our devices. An image of the probes and their layout can be found in figure 4.6.

4.3.3 Custom software

To be able to have full control over both the positioners and all the measurement equipment necessary to perform quantum measurements a custom software package was written. First, drivers for the different tools were written in python and tested. To have control over all these aspects a graphical user interface (GUI) was designed to enable use for all (potential) users. With this GUI,

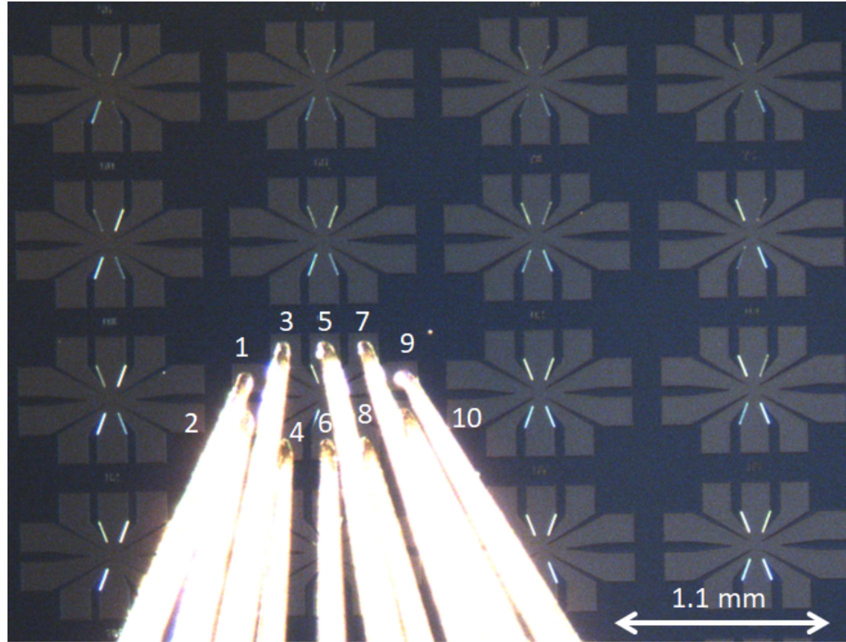

Figure 4.6: An image of the probes at the tip of the probe card above a chip with test structures, the numbers identify the different probes.

devices on a grid can be selected to be tested with a preferred measurement routine. The distance between the devices can be customized as well as the frequency and amplitude of the signal sent to the positioners. For a short overview of the GUI see appendix D.

Besides implementation of simple voltage sweeps two different device-finding algorithms have been designed. The first one can be used for, different types of metallic surfaces, either shorted devices or calibration squares. In this case a voltage of 100 mV (or any other arbitrary value above the noise fluctuations of the read out) is applied to one of the probes. To confirm contact with a metallic surface the other probes are read out. Full contact is assumed when all probes read out the same voltage as the applied bias. The second technique is based on the capacitive load of the probes when touching a metallic bond pad. This bond pads do not have to be directly connected to each other. By approaching the surface, while measuring the current on all the probes, contact with a metallic surface (bond pad or any other) can be detected. By measuring a capacitive loading of the probes. This capacitive loading can be detected by measuring a current spike when the surface is reached. A threshold current is set to differentiate between noise and an actual capacitive effect. This capacitive load signal is stronger on metallic pads than on the oxide surrounding them enabling us to distinguish between being on metal pads or landing on the oxide in between.

To perform these measurements again a LNHR DAC in combination with a NI-DAQ (6363) and Basel Instruments IV-converters are used. A diagram of the set-up can be found in appendix B.

4.3.4 Control and calibration measurements

To calibrate the cryo-prober, a series of measurements were performed on either a full metal chip or on a chip with the a shorted metal piece with the same bond pad lay-out as actual devices. With these tests we established the thermal expansion and contraction of the materials and shifts in readout due to temperature changes.

The first series of measurements was on a substrate with a 100 nm tungsten layer on a silicon substrate. This chip was measured twice at room temperature (RT) and twice at 4 K. Two similar measurements were performed using a different chip with a tungsten layer in a shorted bond pad layout. The different contact heights for these measurements can be found in table 4.1.

Table 4.1: Contact height measured for four different cooldowns using test chips with a Tungsten layer on the surface.

Cooldown	Room Temperature	4 K	Difference
1	1430 μm	1240 μm	190 μm
2	1435 μm	1250 μm	185 μm
3	1470 μm	1285 μm	185 μm
4	1473 μm	1288 μm	185 μm

In this case the electrical set-up shown in appendix B was changed, the IV-converters were removed and before the NI-DAQ a resistor with a resistance to ground of 100kΩ was placed. These resistors ensure that if the probes are out of contact the read out is zero. The measured heights are consistent with each other, a shift of $\approx 185\,\mu$m is found. However it should be noted that first probes came in contact $\approx 30\ \mu$m before the full signal was visible on all probes. In this intermediate region we think that the contact resistance between the some of the probes and the metal surface was relatively high, which leads to the formation of a voltage divider with the resistances to ground placed in the circuit before the NI-DAQ. This indicates that to make proper contact with a device some force needs to be applied to the bond pads.

The accuracy of the Attocube positioners was tested by performing a 1 mm step on each axis independently. After the step a 10 second waiting time is added after which the coordinates are set again. This is done, to minimize the overshoot in x/y after making a big step. These measurements were performed both in the positive and negative direction to check if the overshoot is isotropic. After such a step the position of the positioners was read out every 10 seconds for a 1000 second period. These test where performed at 4 K and 1.5 K. In the case of 1.5 K a pump is running to pump on the 1 K pot. To differentiate between thermal effects and vibrational effects at 4 K the measurements are taken with and with out the pump running as well as with and without exchange gas. The exchange gas ensures a better coupling between the LHe bath and the positioners while without exchange gas the positioners are thermally isolated from the LHe bath. For a step in the positive x-direction the results are plotted in figure 4.7, the other axis and direction can be found in appendix C.

While performing these measurements we have observed a temperature increase at the 1 K pot thermometer. The temperature increase at 1.5 K was minimal ($\approx$ 30 mK) while at 4 K the increase in temperature was significant up to 300 mK. This can be explained by a lack of exchange gas present at 1.5 K, which decouples the 1 K pot thermometer from the piezo positioners. The decay of the temperature back to 4.2 K (LHe temperature) in case of the measurement without exchange gas was 30-60 seconds while with the exchange gas the decay lasted for only 10 seconds. In figure 4.7b we see a time dependent read-out of the positioners at 1.5 K. We assume that at 1.5 K the read out resistor in the positioners heats up causing a wrong read out. As the positioner and resistor slowly decay back to equilibrium temperature the read out gets more accurate.

To mitigate these temperature effects in the read-out a longer waiting time between the two move commands is implemented. This ensures that after the big step we wait for the read-out to go back to its actual value after we use a small step to move the last 20 - 50 μm. Another option would be to install a temperature independent position read out, which for example could be realised by using laser interferometry. However laser interferometry would require fiber optics

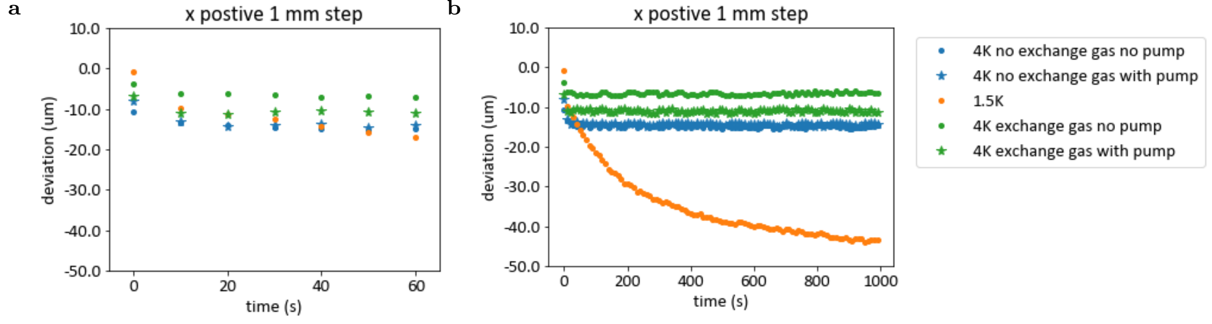

Figure 4.7: Deviations in the attocube position read out after a 1 mm step. Two move command were sent with a 10 seconds wait time in between to compensate for an initial deviation due to a big step. A zoom in of the first 60 seconds is shown in (a) the full measurement is shown in (b).

to enter the fridge which would complicate the design. A further disadvantage of using laser interferometry is the heating caused by the the presence of these lasers. For the current operation range this temperature effect is most likely minimal however if a similar set-up was built for mK temperatures the presence of lasers would most definitely cause extra heating.

To measure the thermal expansion and contraction in the x-y plane, a substrate with shorted bond pads was cooled down. By stepping over the chip with the needles the position of these bond pads was established. This is done by monitoring the voltage readout on the probes while a bias was applied to probe 1. The results of such a calibration measurement at RT and 4 K can be found in figure 4.8. In this figure the average read out voltage of all the probes is plotted for the position at which the measurement was taken. As the needles touch the bond-pads several combinations of voltage detection are possible. Only when all the needles are in contact with the structure a the applied voltage can be read-out on all probes. This is seen in figure 4.8a by the four positions at which a voltage $>$ 80 mV was detected. The positional data was obtained by measuring the position of the positioners while in contact.

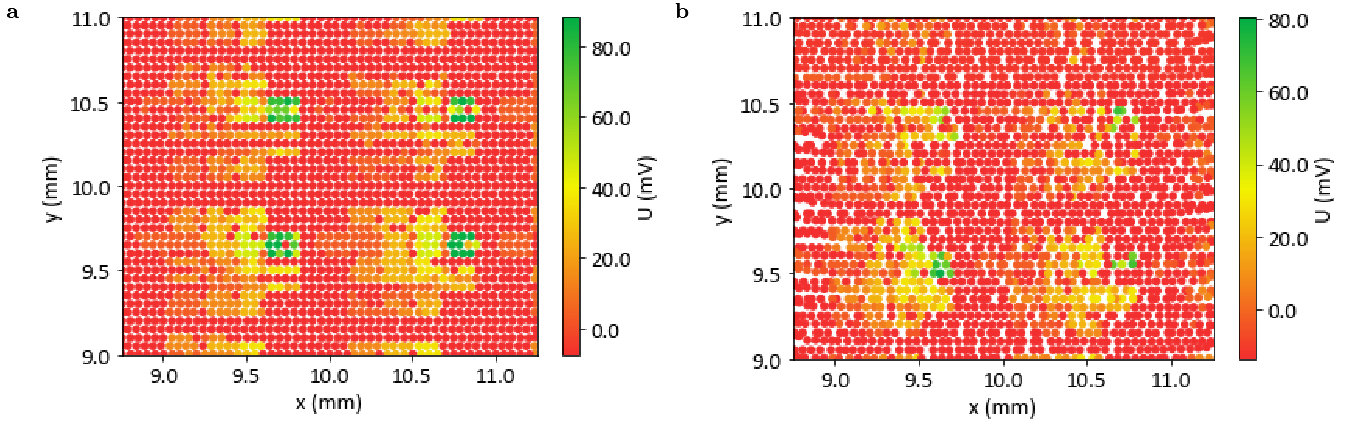

Figure 4.8: Step scan measurements over a substrate with shorted bond pads, at room temperature (a) and 4 K (b). A signal is measured when the probe, with the applied bias and any other probe is in contact with the structure. Only when all probes are perfectly aligned with the structure the average voltage read out from all probes is close to the applied bias. The green squares indicate the position of the structures.

We note two striking differences between the different maps: first off all the spacing between

the measured positions at 4 K is very chaotic and secondly the read out signal has deteriorated after cooling down. The first point is caused by the read out error in the positioners at lower temperature, as discussed above. In this case a zigzag pattern over the grid was made in 50 μm steps. It could be that, even with these small steps, local heating of the read out resistor is still be the cause of these issues, due to the rapid succession of the steps. The deterioration of the probe read out could be due to higher contact resistance between the needles and the substrate at lower temperature. Despite this deterioration of the probe read out, the shorted bond pads can still be located.

A similar measurement was performed on a chip with working devices. In this case the capacitive loading test was used to detect the devices. In this test, we approach the sample and wait for a capacitive load on the probes which signals contact with a metallic surface has been made. In figure 4.9 the results of these tests are found. Here, we observe again problems with the read out of the position and a deterioration of the capacitive read out. We further notice that two of the devices can not be detected at lower temperature. Upon investigation we found that the two devices on the right were broken and showed a lot of leakage between the lead gates and the source/drain, giving us a signal. However the capacitive loading signal was never detected. We further note that even on the broken devices the detection of a signal on the well isolated plunger gate was impossible. Further pointing towards the loss of capacitive signal at cryogenic temperatures. On working devices this signal, caused by the leakage between lead gates and source/drain, is not present meaning that these would be unfindable using this method. However due to the known distance between the devices the working devices can still be located. For a future chip design we suggest to put a few marker structures in the form of shorted bond pads on the chip to act as a guideline to find the actual devices.

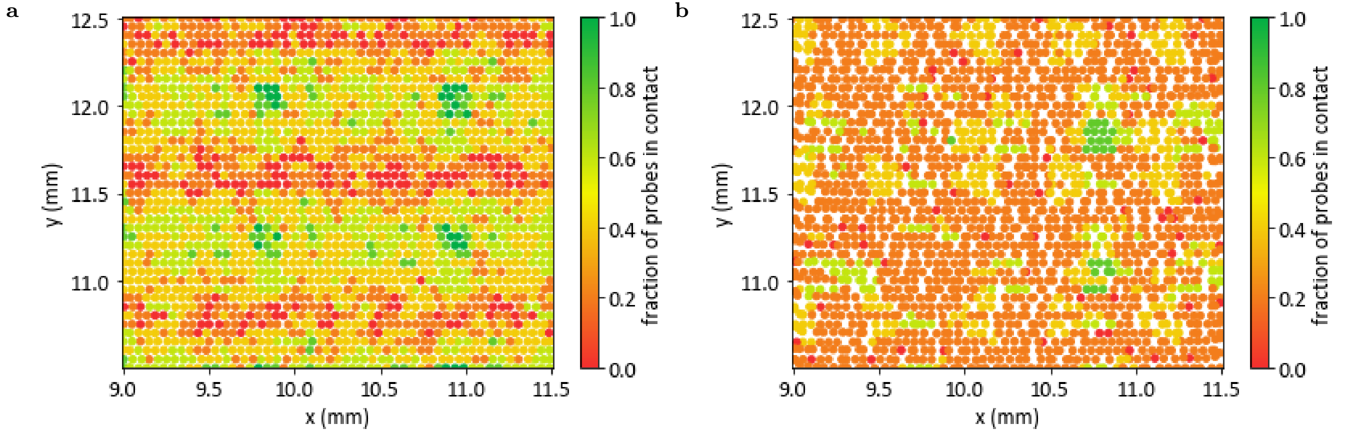

Figure 4.9: Step scan measurements over a substrate with real devices, at room temperature (a) and 4 K (b). In these plots the fraction of probes which show a current spike above the set threshold is shown.

If we compare the results of the room temperature and 4 K measurements we see that the shift in the xy plane is approximately 100 - 200 μm. Not enough tests have been performed to make a statistical analysis of the change in location of the devices after cooling down to cryogenic temperatures. To prevent the aforementioned issues with the localization of devices we recommend to add shorted bond pad structures as markers on future chips. If the probes are aligned with this marker structure at room temperature, using a microscope. A step scan measurement in a relatively small window around this structure can be performed to locate this marker. From there the spacing between the devices can be used to find working devices.

In this chapter we explained the geometry of the devices used in this work and gave an overview of the equipment used to do the measurements. Furthermore, we analysed the accuracy of the positioners and the thermal expansion of devices at cryogenic temperatures. With this information (automated) measurements with the cryo-prober should be possible and our experiments with the cryo-prober are discussed in the next chapter.

Chapter 5

Results

In this chapter we will discuss the results obtained during this project. We will start by looking at the two types of Pauli spin blockade lifting mechanisms in a single gate layer ambipolar double dot device. First introducing the electron side of the device and then having a more in depth look at the hole side and the spin-orbit interaction therein. Then we will look at the results of the cryo-prober measurements. Finally, all the different results will be discussed and placed into context with respect to other research.

5.1 Electron spin blockade

The electron spin blockade found in the ambipolar device is the first electron spin blockade detected in these devices and is of importance for characterizing the nuclear (Overhauser) field. In figure 5.1 a measurement of the bias triangle is shown, this is a bias triangle in a non-trivial position. So we do not know the amount of electrons in the dot during this measurement. We have overlaid the detuning axis along which we defined the detuning between the (1,1) and (0,2) state. This measurement is taken at zero field, but due to some residue flux in the superconducting magnet, the sample still experiences a small magnetic field of the order of a few mT. This explains why the baseline of the triangle is missing. We would expect that for electron spin blockade, which is lifted by the hyperfine interaction, to see the ground state transition at zero field. Furthermore we note that a bit of cotunneling is present between the used triangle and its neighbour (the neighbouring triangle is only partly visible at the top of the figure).

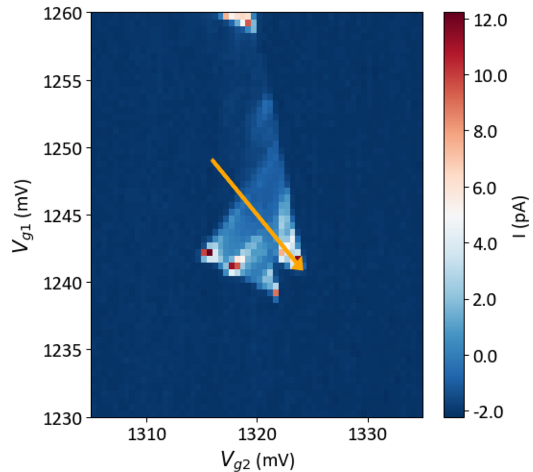

Figure 5.1: Scan of the spin blockaded bias triangle with the orange arrow representing a detuning axis

When we scan the detuning axis versus the magnetic field, we observed two different types of spin blockade lifting mechanisms. Both of these are presented in figure 5.2. In 5.2a we see the merging two peaks for a hyperfine mediated lifting of spin blockade. This behaviour is only seen in the small tunnel coupling regime. In this regime the Overhauser field mixes the S(0,2) state with the S(2,0) state, lifting the spin blockade. At higher detuning the Overhauser field is too small to

mix these states and the typical hyperfine peak at zero field is observed. In figure 5.2b we also see two different peaks but they do not merge and at the zero detuning line the peaks split up in two sub peaks. This becomes clearer when we look at the line cuts of both different blockade lifting types. These linecuts are displayed in figures 5.2c and 5.2d respectively.

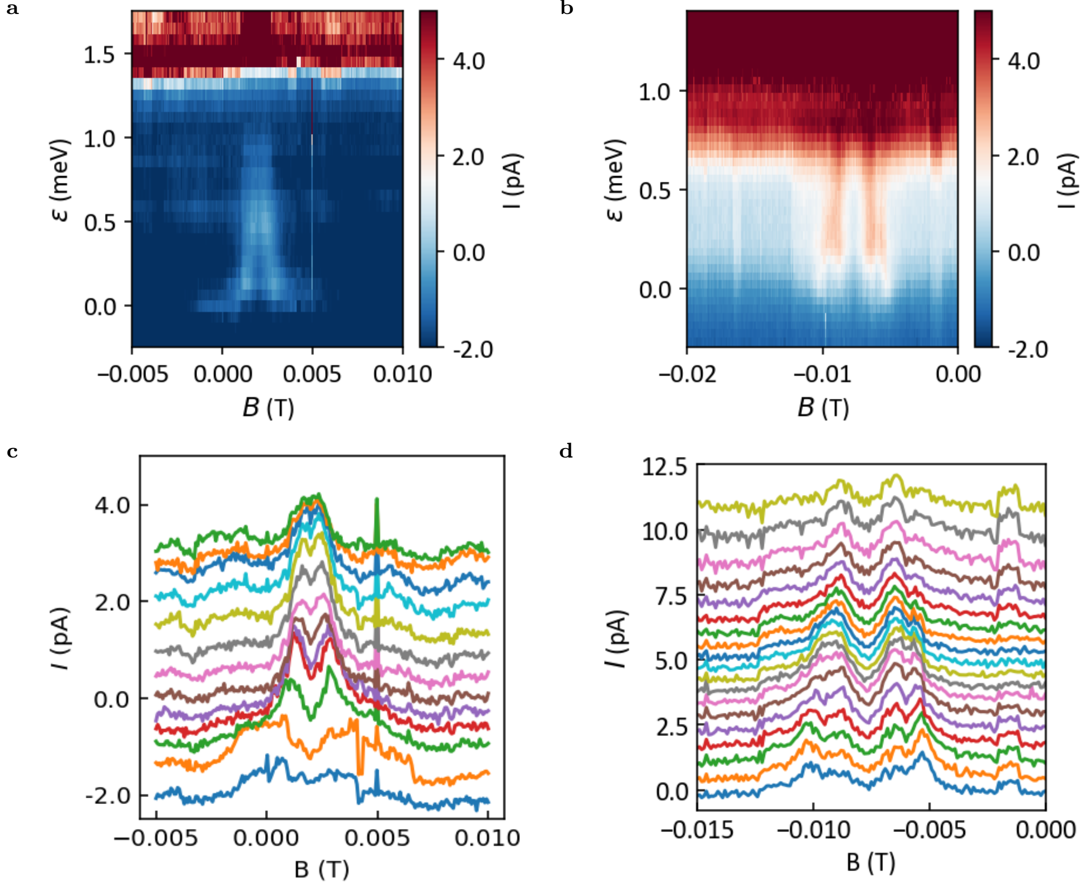

Figure 5.2: Blockade lifting features for Pauli spin blockade in a double quantum dot occupied by electrons. In 5.2a a typical hyperfine interaction lifting signature and in 5.2b new feature. In 5.2c and 5.2d the linecuts at fixed detuning axis of 5.2a and 5.2b, these linecuts are offset in current for clarity

From the linecuts, it becomes clear that the peaks at low detuning start out at a similar width of approximately 5 mT, where in 5.2c the peaks slowly start the merge and the valley in between them start to get smaller, while in 5.2d the valley (in between the peaks) remains of the same depth. Multiple attempts were made to consistently reproduce either feature. When we defined the detuning axes, the feature was switching randomly between measurements. Sometimes, this switching even occurred between two measurements with the same detuning axis.

From the V-shaped feature in figure 5.2a an exchange coupling can be extracted by fitting the peak separation versus the detuning. From this feature we can also extract the hyperfine field strength by fitting equation 11 of Jouravlev et al. [69] to the plateau formed by the merged peaks at higher detuning as visible in figure 5.2c. From the fits a effective hyperfine field of 0.5 mT was extracted and a tunnel coupling of 35 μeV was obtained. The fits and fitted parameters can be found in appendix E.

At higher fields another spin blockade lifting mechanism became apparent, an example of that

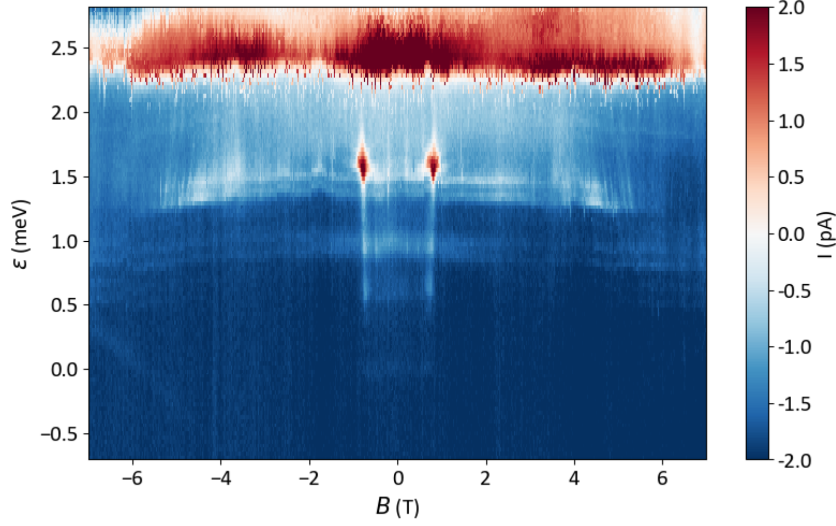

Figure 5.3: A high field sweep of the detuning axis versus the magnetic field, with a possible valley state spin blockade lifting mechanism.

can be found in figure 5.3. Two relatively wide peaks lift the PSB at approximately 0.6 T. We attribute these peaks to valley states which lift the spin blockade, these kind of peaks have previously been observed in Corna et. al. [52] and Hao et. al. [70]. The valley splitting in the quantum dot can be found by using $B_v = \frac{\Delta}{g\mu_B}$, in which Δ is the valley splitting and B_v is magnetic field at which the peak appears. Using DC transport methods, there is no direct way to measure the electron g-factor in the sample. This means that the valley splitting in this device can not be calculated. By assuming a g-factor of 2 the valley splitting was estimated to be 82 μeV, which is about twice as high as in Ref. [52]. The sample rotator was used to rotate the magnetic field. However, no significant change of either spin blockade lifting mechanisms was found.

5.2 Hole spin blockade

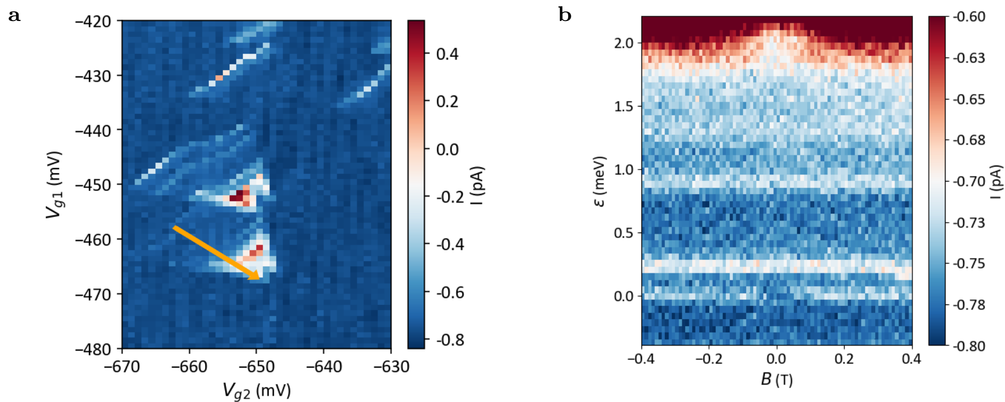

Figure 5.4: In 5.4a a measurement of the bias triangle showing spin blockade is shown, with the orange arrow representing a detuning axis. In 5.4b a magnetic field versus detuning sweep for the bias triangle showing spin blockade. The spin blockade is visible at zero field and zero detuning, but also at higher detuning.

In the same device as in the previous section, hole spin blockade was also found. This means that this is the first device that shows ambipolar spin blockade. In this section we will go through the results obtained on this blockade, and fit our model from chapter 3 to the obtained data.

In figure 5.4a, the blockaded bias triangle is shown. This scan is taken at zero field. We immediately notice that the current in the bias triangle is only of the order of a few hundred fA. Several attempts where made to use a lock-in measurement technique to improve the signal, however all of these attempts were unsuccessful. The spin blockade signature in this triangle is shown in figure 5.4b. The dip at zero field in the zero detuning line of the bias triangle is of the order of 100 fA, which is just above the noise threshold of the system. In this figure we can also observe that the singlet-triplet splitting is relatively small (≈ 0.25 meV). At high detuning another state shows a dip in current, which could be the next orbital showing spin blockade. From now on we will only focus on the lowest two states, as those can be modelled as the two electron states in chapter 3. To identify the other states, a more complicated model beyond the scope of this thesis is necessary.

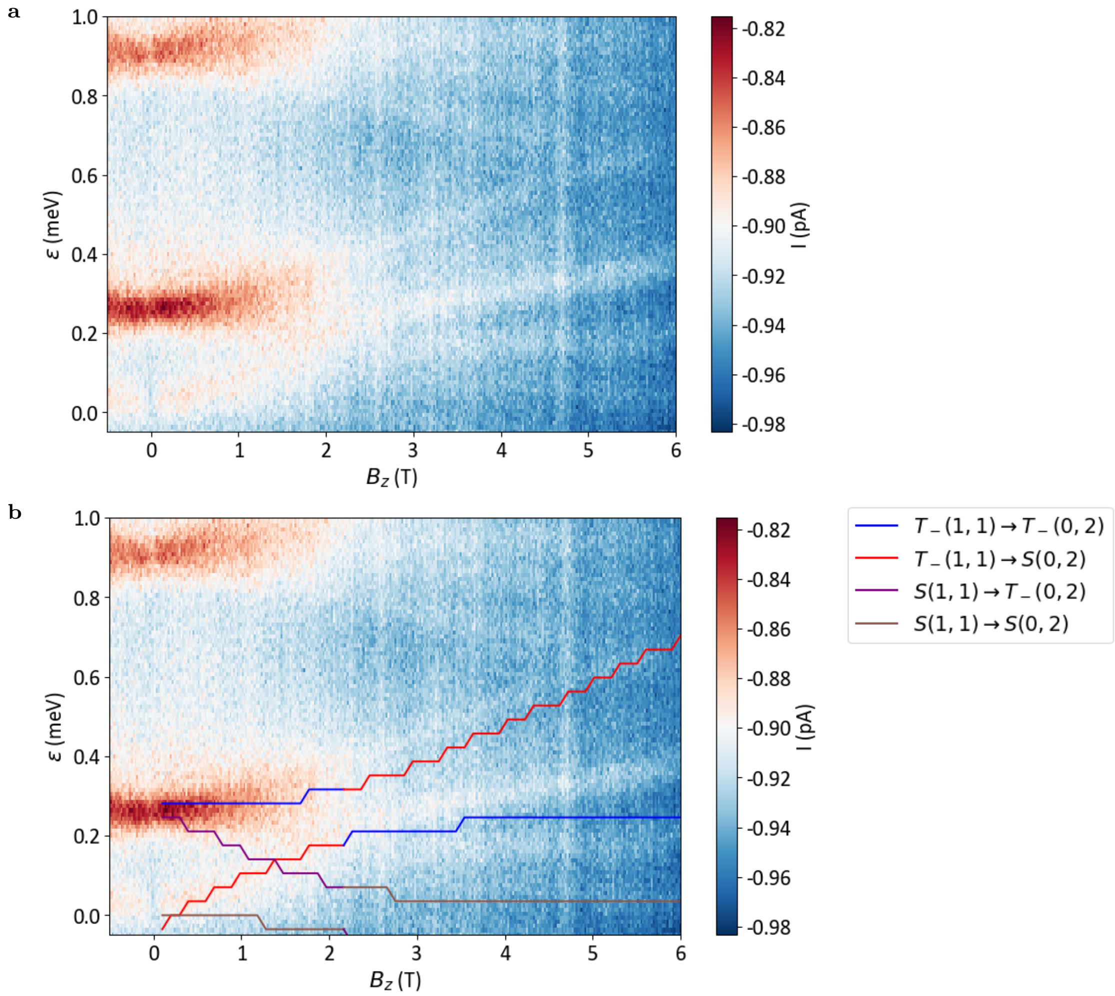

Figure 5.5: A high magnetic field sweep of the bias triangle showing Pauli spin blockade versus its detuning axis, also here we overlaid the model from chapter 3. The steps in the overlay are caused by the discrete steps taking during the modelling.

In figure 5.5a a high field sweep of the detuning axis versus the magnetic field can be found. At zero field we again observe the Pauli spin blockade dip. Furthermore, we observe the first

excited state transition at constant detuning until approximately 1.5 T were it starts to slope up. The ground state transition looks to slope upwards due to the Zeeman effect however it does not become a horizontal line after it anticrosses with the first excited state transition. This and the low current make it impossible to quantitatively analyse the spin-orbit anticrossing (see section 3.3). We assume the anticrossing happens around 2 T, which is supported by an overlay of the same measurement with the model from chapter 3. This overlay is shown in figure 5.5b. The used parameters for this overlay can be found in appendix A.

When comparing the model in figure 5.5b with the one in figure 3.4 we immediately notice that the fit of the data in 5.5b is worse than the fit in figure 3.4. We attribute this to the fact that we are almost certainly dealing with higher hole occupation. Orbital effects might play a larger role in the magnetic field dependence of these transitions. Note that orbital effects are not taken into account in our model. The signal to noise ratio in this measurement is relatively low which makes it difficult to identify the different transitions.

Although we were not able to extract the spin-orbit strength, we could measure the g-factor anisotropy. To measure the g-factor, five equally spaced points on the approximate center of the $T_{-}(1,1) \rightarrow S(0,2)$ transition are selected. A linear regression is performed with these points and from the slope the g-factor is extracted (see figure 5.5b). The results of these measurements are shown in figure 5.6. The magnetic field axis is completely out of plane for $\theta = 90$ and $\theta = 180$. In this figure we only report on the statistical errors, a systematic error could also be present. We estimate the systematic error in the read out of the angle to be 5°and for the g-factor we did not estimate the systematic error. We observe that the modulation of the g-factor is of the order of 30% and notice a periodic trend.

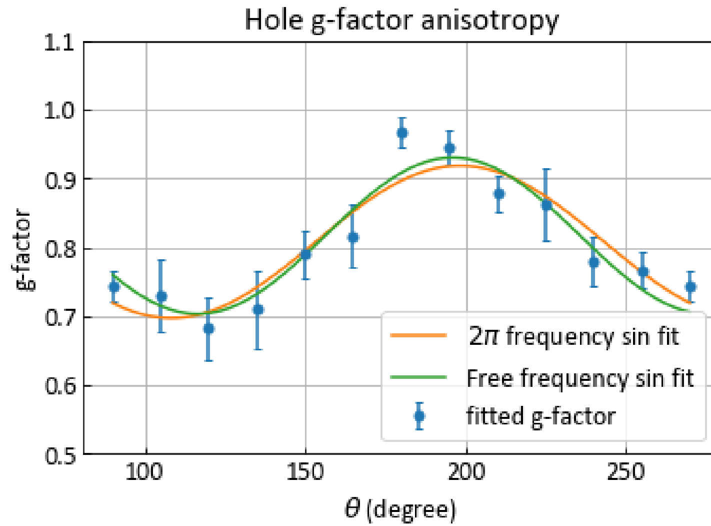

Figure 5.6: The g-factor anisotropy measured in this sample. $\theta = 90$ *and* $\theta = 180$ *are the angle for which the magnetic field is perpendicular to the sample plane. Once the magnetic field is in the sample plane (*$\theta = 180$*) the field is pointing perpendicular to the fin.*

The data is fitted using $A\sin(\theta \cdot f - \phi) + C$, where θ is the angle of the sample rotator. Shown in figure 5.6 are the fitted g-factors. The g-factors are fitted with two different fits: in the first fit, we used a fixed frequency of 2π and in the second we used a free frequency. The fit parameters for both cases can be found in table 5.1. In the fixed frequency fit we find a phase shift (ϕ) of 13 °, which leads to the strongest g-factor at an angle of 193 degrees or 13 °out of the sample plane. This might indicate that the spin-orbit vector is also pointing along that axis. To confirm this, an

investigation of the anisotropy of the spin-orbit strength is necessary. The g-factor modulation of 30 % found here is significantly smaller than predicted [1]. However this can atleast be partially attributed to the higher hole occupation in the quantum dots. Filled shells are known to influence the g-factor [26, 71].

Table 5.1: Fit parameters from fitting a sin function to the data in figure 5.6.

parameter	free fit	fixed frequency fit
A	0.1134 ± 0.0001	0.1106 ± 0.0002
ϕ	-5.7 ± 10.4 °	13.3 ± 0.2 °
C	0.8166 ± 0.0001	0.8078 ± 0.0001
f	2.26 ± 0.02	2

5.3 A discussion on Pauli spin blockade in ambipolar double quantum dots

The ambipolar spin blockade discussed in this thesis the first of its kind in these devices. This is important because it shows that, principl,e both electron and hole qubits can be formed in these devices. In previous works, the main focus in these devices has been on the hole side. However, a combination of the two exploiting the longer coherence time of the electron spin and the easier manipulation of the hole spin could be of use in the future.

We observed two different features while measuring the electron spin blockade. The conventional signature of a hyperfine lifted spin blockade in figure 5.2a and some new unknown feature in figure 5.2b. At the moment it is unclear what causes these differences in the features and no proper quantitative analysis has been performed. However, one hypothesis that there is a competition between the hyperfine field and the spin-orbit interaction, another option is the influence of orbital effects. To investigate this further, a sample with an occupation of only two electrons should be investigated to properly determine the nature of these effects.

The extracted effective hyperfine field of 0.5 mT gives us an upper bound for the coherence time of qubits in these devices, using $T_2^* = \frac{\hbar}{g\mu_b\sqrt{\frac{2}{3}B_N^2}} \approx 20$ ns [53]. This is significantly smaller than measured in electron spin qubits in silicon, however these spin qubits use purified silicon. Compared to natural silicon where the abundance of spin carrying Si-29 atom is 4.6 %, in purified silicon it is 800 p.p.m.. Taking this factor into account the coherence time we obtain an approximate coherence time of 1.2 μs. This value is still two orders of magnitude smaller than the highest achieved coherence times in electron spin qubits in silicon [72]. An explanation for this discrepancy could be that the effective hyperfine field as measured here, is for a dot with higher electron occupation, which means the dot is likely larger than for a dot with single electron occupation. This has an influence on the overlap with the magnetic nuclei. Another explanation for this estimate could be that spin qubits are not limited by nuclear noise but by charge noise. For holes the hyperfine field is usually an order of magnitude smaller [73], mainly due to the difference in wavefunction overlap with the nuclei. Plugging in the smaller hyperfine field we obtain an estimate of ≈ 200 ns, which is slightly longer than measured in hole spin qubits before [74]. These estimates are greatly influenced by the amount of nuclei overlapping with the electron/hole wavefunction and the coupling strength between them. Future measurements on qubits in these devices will give more information about the limiting effects of the coherence of hole spin qubits in these devices.

Due to the higher electron occupation in the quantum dot the estimated value for the valley splitting can be seen as an upper bound for the valley splitting in these devices. This can be ex-

plained by the fact that the effective g-factor in devices with higher electron occupation is usually lower than the predicted one electron g-factor. To establish electron spin qubits more accurate measurements of the valley splitting should be made to drive the qubit using these valley states [52]. This operation principle does not require the slanting magnetic field and AC strip line used in conventional electron spin qubits like in [75].

The hole spin blockade in this device is also measured in a higher charge carrier occupation than two. Due to absence of charge sensing in these samples no exact estimate of the amount of holes in the sample can be made. The combination of higher hole occupation and low current in the measured device we were not bale to estimate the spin-orbit strength. This multi-hole regime makes estimation of the spin-orbit strength difficult. However we might be able to make a qualitative argument about the spin-orbit vector given the direction of strongest g-factor. In 2016 Voisin et al. [76] extracted the g-factor anisotropy of a nanowire MOSFET and found that this anisotropy is also strongly electric field dependent. Since the electric field is related to the spin-orbit vector (via the cross product with k) knowing under which conditions and at which angles the g-factor is maximal the direction of the spin-orbit vector can be estimated. However the information currently obtained about the g-factor anisotropy is insufficient to make any clear statement about the spin-orbit vector, as we do not have access to the in plane field angles and a no tunable electric field (due to a lack of tunnel barrier gates).

These measurements of the g-factor anisotropy should in the future be supported by measurements of the spin-orbit strength, to be able to make quantitative statements about the modulation of the spin-orbit strength. Once the spin-orbit vector direction and strength is known, a hole spin qubit can be driven at its fastest possible speed by applying a magnetic field perpendicular to the spin-orbit vector. To further optimize a hole spin qubit in these devices a purified Si substrate can be used to further suppress the hyperfine interaction and, enhance the coherence time. It is also theoretically predicted that the spin-orbit interaction is about an order of magnitude stronger when the fin is parallel to the [001] crystal axis of the silicon substrate [1]. However, this remains to be be experimentally verified.

5.4 Cryo-prober measurements

In this section we used the cryo-prober to measure, several single gate-layer quantum dot devices. With these measurements, we demonstrate fast characterization of several devices at cryogenic temperatures. This quick characterization can be used to select a device with optimal device parameters to be further tuned into a stable regime. We will first analyse the transistor properties of these devices at 4 K and then investigate at the single quantum dot properties.

The devices were pre-characterized at room temperature right after fabrication. The selected devices after pre-characterization are found in figure 5.7. In this figure also the individual device parameters are given. Here gate spacing is defined as the space between the lead gates and the plunger gate.

After cooling down the chip devices: 3, 7, 9, 13, 24, 28 and 32 were found to be broken. Devices 1, 15 and 31 showed a high leakage current while the lead gate was pushed to our testing value these were thus also not considered in standardized analysis. Before the appearance of this leakage some measurements were performed. Proper contact with device 8 could not be made. This leaves us with 21 devices which have been fully tested and those results we will discus in this section. For devices 1, 8, 15 and 31 some initial measurements can be found in appendix F. This leads to a yield of 25/32 devices still working after storage and transport. This yield is better than when we wire-bond our samples, which results in a yield around 40 %. The lower yield for wire-bonded samples is most likely due to the presence of comparably high DC voltages on the tip of the wire-bonder.

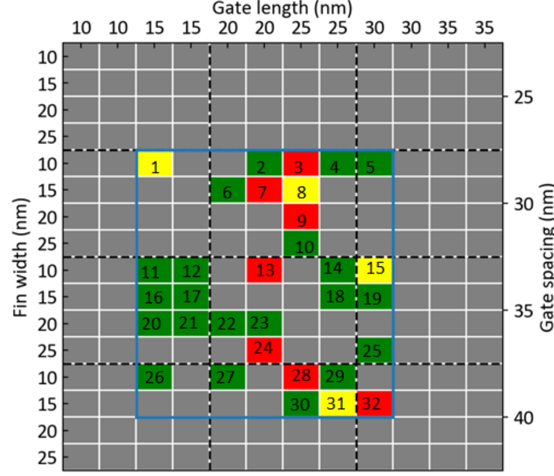

Figure 5.7: An overview of the different devices which made it through pre-characterization. The numbers act as labels for the devices. The gate spacing changes every four rows, this way for each fin width and gate length there are four different gate spacings. The blue square indicates the reachable area of the current set-up. In red color represents the devices which are found to be broken after cooling down and in yellow the device which showed early leakage or were impossible to contact and green indicates the fully tested devices.

5.4.1 Transistor properties

The quantum dot devices used in this work can operate as a transistor at low temperature. We will look at both the n and p-type properties of these ambipolar devices. The numerical values obtained with these measurements can be found in appendix F. At the end of this section, we showcase the room temperature (RT) transistor properties of similar devices, to show that the cryo-prober can also function as a RT characterization tool.

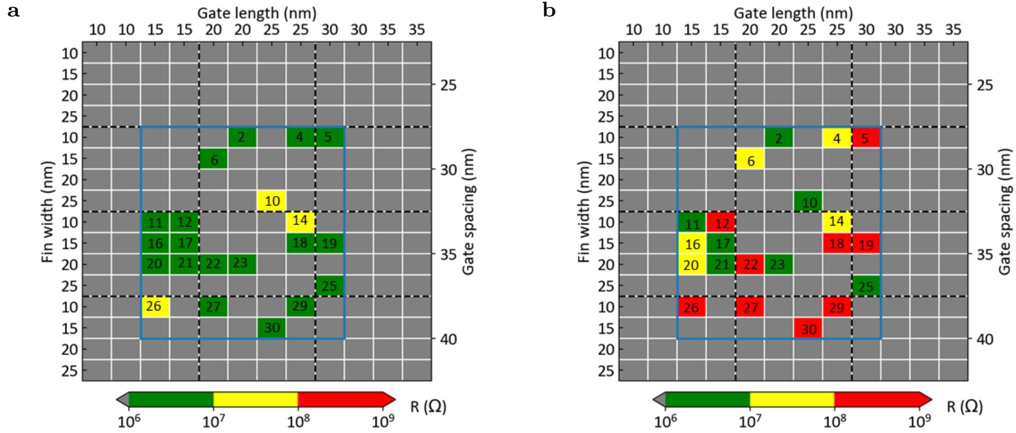

Figure 5.8: Classification of the channel resistance for both electrons (5.8a) and holes (5.8b). Values below 10^7 *are considered good for use for quantum dot operation. The devices in the yellow and red classification are considered to be intermediate or bad for quantum dot operation.*

The channel resistance of each device is measured for different lead gate voltages. The channel resistance is important for transistor and quantum dot operation. An overview of the obtained channel resistances for each device and for both types of operation can be found in figure 5.8.

Here, the shown data was obtained with a lead gate voltage of ±5.5 V.

We immediately note that for electrons the channel resistance in general is lower. This is expected as the electron effective mass in silicon is lower than the hole effective mass. This can be inferred from the Drude model in which mobility is inversely proportional to the effective mass. The effective mass for electrons in silicon is estimated to be $0.26m_0$, while for heavy holes the effective mass is estimated to be $0.49m_0$, in which m_0 is the electron rest mass. This gives a ratio of effective masses of 1.8. We used the data from 8 different devices to calculate the ratio of the channel resistances and found average ratio of 2.9. For the other 13 devices a ratio in excess of a 10 was found. This means that for these devices the difference in effective mass of the charge carriers is not the main cause for the difference in channel resistance thus these devices were not considered in this comparison. Even for the 8 devices with a low channel resistance ratio the average calculated resistance ratio is not close to the mass ratio of electrons and heavy holes. From this we conclude that the channel resistance in these devices can not be estimated using a simple Drude model. We think that scattering processes on impurities play a important role in the channel resistance for these devices.

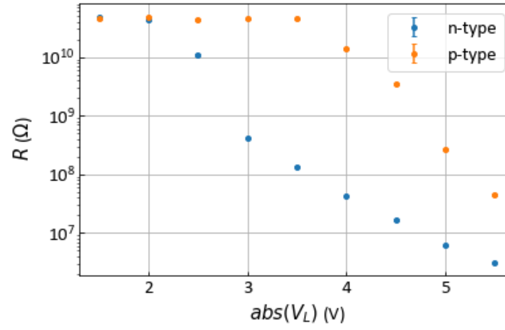

Figure 5.9: Sample channel resistance measurements of device 16, for both types of charge carriers.

To show the difference between electron and hole conduction a example resistivity measurement for device 16 is shown in figure 5.9. A linear fit on the bias dependence was performed to obtain the channel resistances. To facilitate transport the lead gates need to accumulate a certain amount of charge carriers. This means that at low lead gate voltages the resistivity saturates.

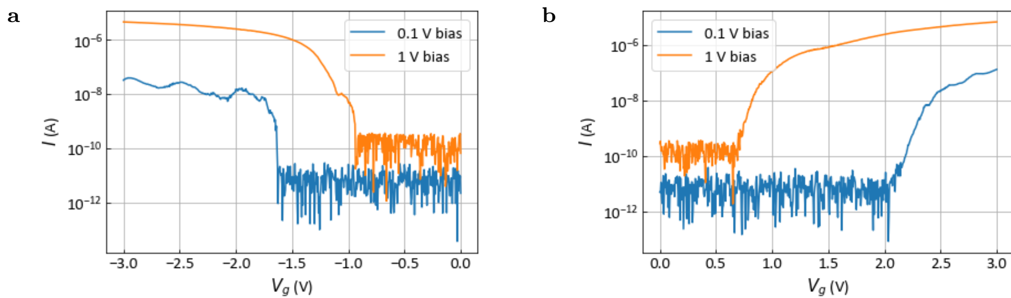

Figure 5.10: Transistor turn on curves for device 14, in a low bias (0.1 V) and high bias (1 V) regime. With in 5.10a the p-type side and in 5.10b the n-type side of the device.

In figure 5.10, exemplary transistor transfer curves can be found, as taken on device 14. While an overview of the measurements on all working devices is shown in figure F.4 (p-type) and figure F.5 (n-type). The difference in the offset at zero gate voltage in these figures is due to the different amplification settings used for both measurements: in the low bias regime a gain of 10^7 was used

while for the high bias measurements a gain of 10^6 was used.

A clear difference in threshold voltage is observed when comparing the low-bias regime to the high-bias regime. From such curves the threshold voltage, subthreshold swing and DIBL are extracted using the equations from section 2.1. The results of these calculations are summarized in figures 5.11, 5.12 and 5.13. These values are obtained at 100 mV bias, similar results for the high bias regime are shown in appendix F.

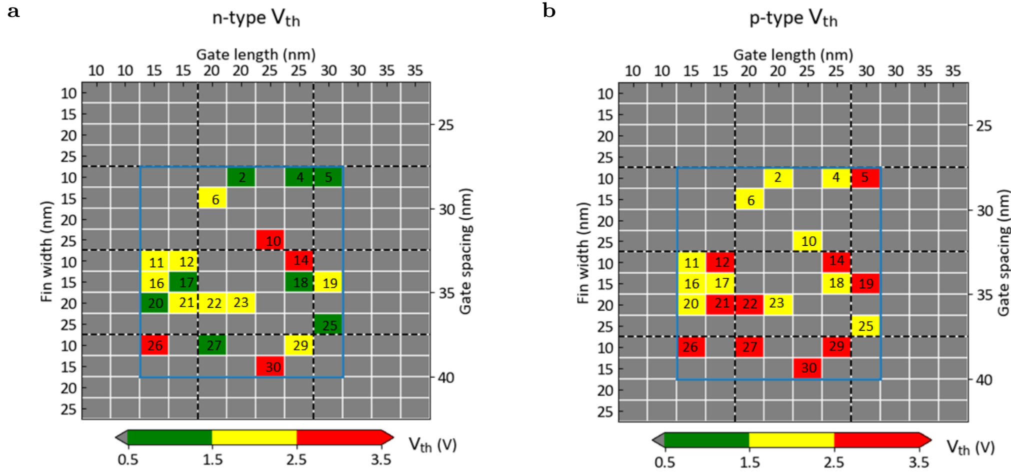

Figure 5.11: An overview of the threshold voltages at 100 mV bias in both n and p-type operation.

Again we note that n-type operation is advantageous as the threshold voltage is lower. However, we should note that a typical MOSFET has a threshold voltage around 0.5 V [39]. This means that our devices require significant more power to operate as a switch, compared to standard MOSFETs at cryogenic temperatures.

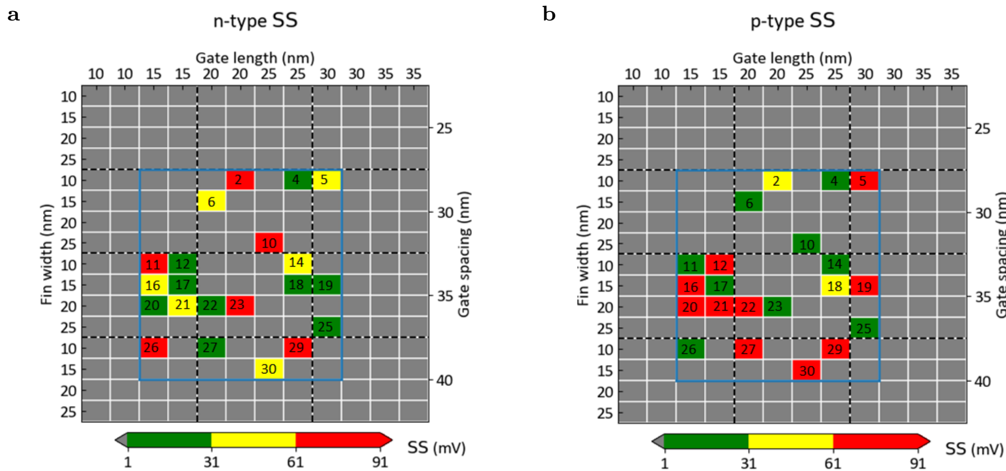

Figure 5.12: An overview of the subthreshold swing for the measured devices at 100 mV bias.

To obtain a single number out of the subthreshold swing (SS) calculations we looked for the subthreshold swing for which the current drops below 400 pA. If this point was never reached we used the last point before the background noise became visible in the SS. The subthreshold swing

as shown in figure 5.12, is comparable with typical MOSFETs at RT, however still far away from measured values at cryogenic temperatures and the theoretical limit at these temperatures (see equation 2.3) [40]. The calculated theoretical limit, according to equation 2.3, is 0.79 mV. This value is obtained for the ideal case in which $C_D = 0$.

The drain induced barrier lowering (DIBL) is calculated for both modes of operation, results of these calculations can be found in figure 5.13. Again we note that the values obtained for these devices are significantly higher than obtained with classical MOSFETs. Furthermore we do not observe a trend for the different gate spacings and thus channel lengths. The wide variety of gate lengths used in this thesis could be the cause of this.

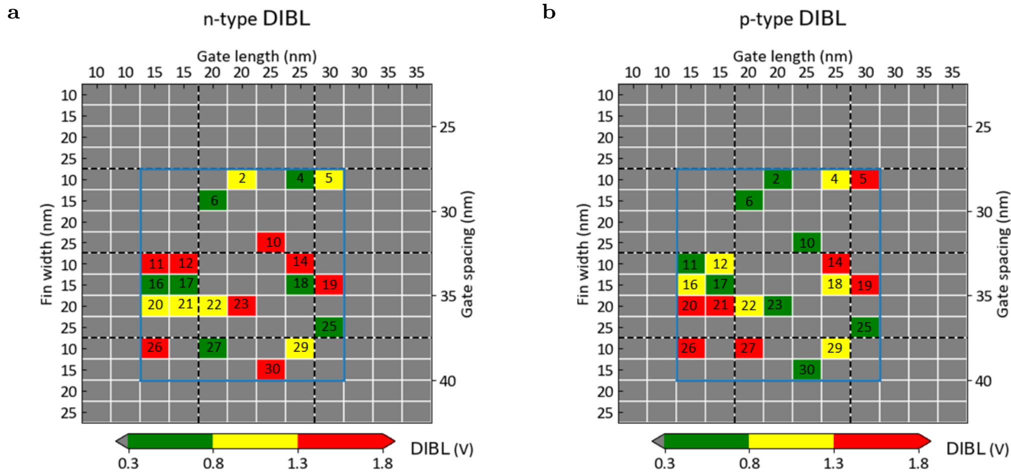

Figure 5.13: An overview of the drain induced barrier lowering in the measured devices.

Room temperature characterization using the cryo-prober

On the devices considered in this chapter the room temperature characterization has already been done directly after fabrication in the IBM cleanroom. Here we would like to show that the cryo-prober can also be used for this RT characterization. We therefore have measured a single device from a chip with the same devices but a PtSi as silicide. Therefore, these devices are in principle only suitable for p-type operation. In the future we can use the cryo-prober and its software to automate these measurements for several devices.

Our room temperature characterization starts with an analysis of the channel resistance of the transistor at RT, these measurements can be found in 5.14. In 5.14a the source drain sweeps for the different lead gates voltages are shown, while in 5.14b the resistance, obtained via a linear fit of the I-V cure, is shown. We observe that the channel resistances at RT drop to reasonable levels earlier than at 4 K (see figure 5.9), which is attributed to the abundance of charge carriers in the silicon at RT. Most of these charge carriers freeze out at 4 K, such that the lead gates need to be pushed to higher values to obtain similar channel resistances.

We also perform a characterization of the transistor curves. This is done by sweeping the plunger gate at a fixed bias (in this case 100 mV) for different lead gate voltages. In figure 5.15 the result of such a measurement is shown. We note that due to the PtSi contacts the transistor is not expected to open up for lead gate values above zero (the n-type regime). However this n-type operation still shows a turn-on of the transistor for positive plunger gate voltages, albeit very weak. Furthermore, due to the excess of holes present in the system for these lead gate voltages, the

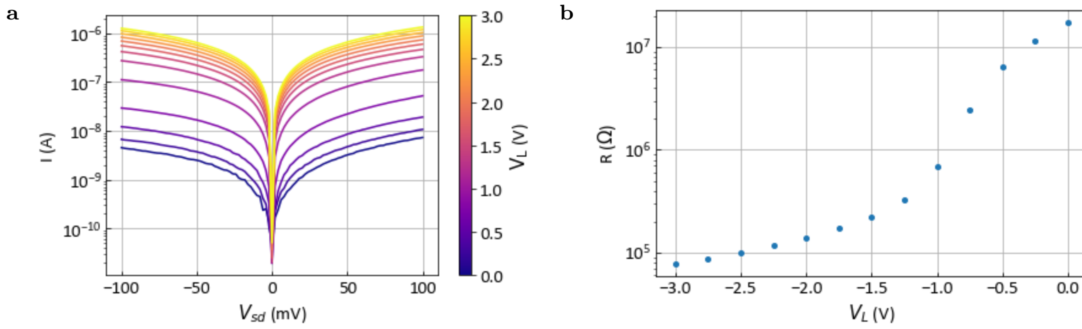

Figure 5.14: Source drain curves taken for different lead gate values in (a). In (b) the channel resistance as a function of lead gate voltage is plotted.

transistor also opens up at negative plunger gate voltages. We observe that for the negative lead gate voltages, the voltage dependence of the pinch-off curves is weak. This is due to the effect of the lead gates on the tunnel rates from source to drain. Despite this the nanogate is able to close the channel, albeit for lower lead gate voltages at positive voltages on the nanogate. However, in this case we still see a difference between the on and off state of 2 orders of magnitude. This in principle enough to function as a transistor but far from the achieved on off ratios in traditional MOSFETs [39], and also significantly less than the achieved ratios of 3-6 orders of magnitude at cryogenic temperatures in section 5.4.1.

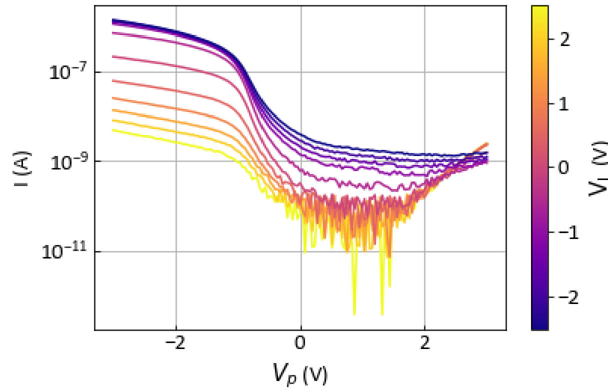

Figure 5.15: Transistor curves for different lead gate values recorded at RT using the cryo-prober.

These proof of principle measurements open the way for characterization of our devices at RT and at cryogenic temperatures using the same tool. In combination with the fact that no wire bonding is needed to use the cryo-prober, this makes this tool a perfect candidate for preselecting the best device out of a large batch of fabricated devices.

5.4.2 Quantum dot properties

In this section we will first give an overview of the pinch-off curves of the 21 devices and then focus on the hole side of device 14 to investigate the effect of the contact height of the needles on the measured pinch off. This is important to see if the contact resistance has an influence on the formation of quantum dots in these devices. In case of a high contact resistance the voltage will drop over the contact instead of the gate, such that the gate has no effect. an analysis of the electronic temperature will then be done based on the hole sides of devices 2 and 10 and the

electron side of device 25. Finally we will try to extract important quantum dot parameters of the electrons on device 25 and the hole side of device 2.

To asses the quantum dot properties of the tested devices we apply a small bias (1 mV) and sweep the plunger gate. We then identify isolated peaks in transport, which point towards the presence of coulomb oscillations. We combine this with information about the channel resistance and select a device to perform quantum dot measurements on. With the formed quantum dots we try to estimate the electron temperature of the sample. An overview of all pinch curves can be found in figure F.6. All these measurements are taken at $V_L = \pm 5.5$ V.

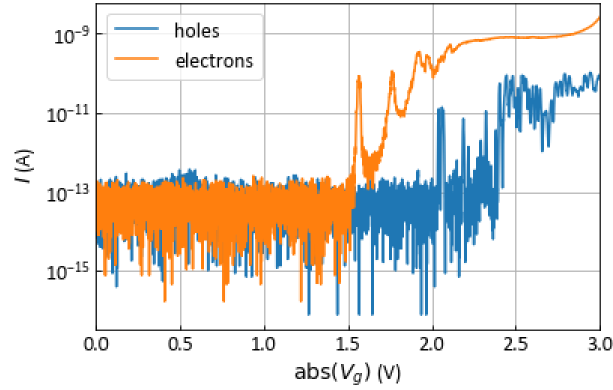

Figure 5.16: Pinch off curves of device 25, taken at 1 mV bias and $V_L = \pm 5.5$ *V.*

We note that most of the devices do not seem to form nice coulomb peaks. We also note that the threshold voltage is again relatively high, and 7/21 hole side sweeps do not even show any turn on before - 3 V on the gate. For electrons the devices seem to open up, which is also expected by looking at the channel resistance which are generally lower than for holes. However for the electrons the behaviour of the pinch-off curve resembles that of a scattering process on a potential well [77], a good example of this can be found seen in the curve for device 18 in figure F.6. A sample pinch off curve of device 25 is shown in figure 5.16.

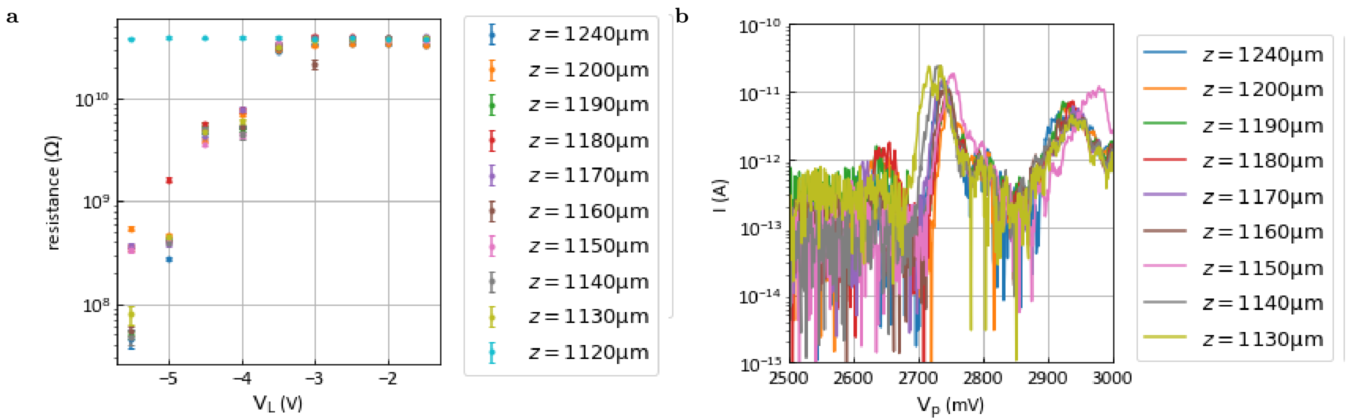

Figure 5.17: Measurements taken on device 14 to investigate the influence of contact resistance. We show the channel resistance for the different heights of the z-piezo 5.17a and the pinch-off curves at 1 mV bias 5.17b

In figure 5.17 the results of quantum dot measurement at different values for the z-positioner are plotted. In figure 5.17a the channel resistance is plotted for different positions. We note that for $z = 1120\,\mu$m the probes are out of contact as the channel resistance is constant at its maximum value for all the lead gate values. Furthermore we do not see a significant difference between the other heights used. For channels with a channel resistance much smaller than 1 MΩ the contact resistance might play a role. In general, this level is never achieved in these devices so we do not expect any problems for source drain sweeps. When looking at figure 5.17b we again observe no significant difference between the pinch off curves taken at the different heights – in this case the measurement at $z = 1120\,\mu$m is left out for clarity. The lack of significant difference between the different pinch-offs can be explained by the fact that the gate should operate as a near perfect capacitor, which means that the effect of the contact resistance to this gate is negligible, given a sufficiently long charging time.

To asses the electronic temperature of the devices, 3 independent devices were used and two different methods were applied. First we look at the width of the coulomb peak in the low bias regime, later we try to fit a Fermi-Dirac distribution to a coulomb diamond edge. Devices 10 (hole side) and 25 (electron) side are used to determine the temperature using the width of the coulomb peak method. On the hole side of device 2 we perform an independent temperature measurement using the Fermi-Dirac fit. These measurements can only give an indication of the electronic temperature in the devices. This is due to the lack of control over the tunnel coupling and the not perfect quality of the devices used. Furthermore, during these measurements the voltage noise in the system was still relatively high, this can be resolved by removing ground loops. In figure 5.18, linecuts from devices 10 and 25 at 0.5 mV bias were fitted to equation 6.7 of Beenhakker 1991 [78]. We should not that a bias of 0.5 mV corresponds to a temperature of 5.8 K. We do expect to see a bias broadened peak with these applied biases. In future measurements the signal-to-noise ratio should be improved to be able to measure at lower biases.

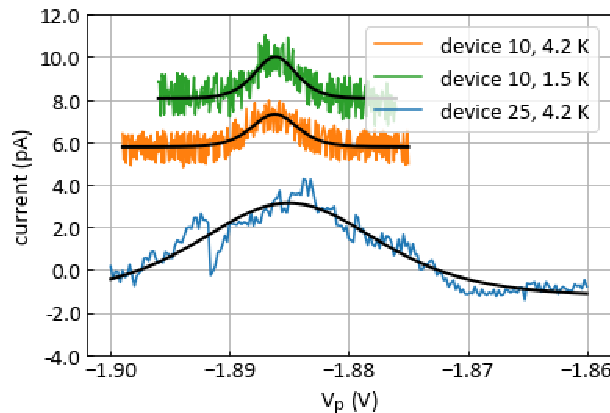

Figure 5.18: Temperature fits through the first visible coulomb peak at low bias (0.5 mV), in the legend we note the temperature as indicated by the 1 K pot thermometer. For device 10 holes were the charge carriers and in device 25 electrons were the charge carriers.

The data of device 25 is from a different run in which we made small improvements to the noise in the system. We further note that with the 1 K pot running, we were not able to obtain a data set at 1.5 K for device 25. At 4.2 K the the fitted temperature is 4.6 ± 0.2 K. For device 10 we were able to obtain measurements with and without the 1 K pot running, however there is no significant difference visible in the peak width. The fitted temperatures are 3.2 ± 0.4 K and 2.9 ± 0.2 K respectively. The deviation of the obtained values using this method from the expected values can partly be explained by a poor estimation of the lever arm, which is a crucial parameter in these fits. Other explanations could be a too open tunnel barrier or voltage noise. The peak

extracted from device 25 appears wider compared to device 10 due to a difference in the lever arm.

To compare whether these results are valid, we fit the edge of a coulomb diamond on the hole side of device 2 with the Fermi-Dirac distribution. The coulomb diamond and the fitted curves can be found in figure 5.19. The extracted temperatures using this method are 3.1 ± 0.4 K (at 4 K) and 4.6 ± 0.3 K (at 1.5 K).

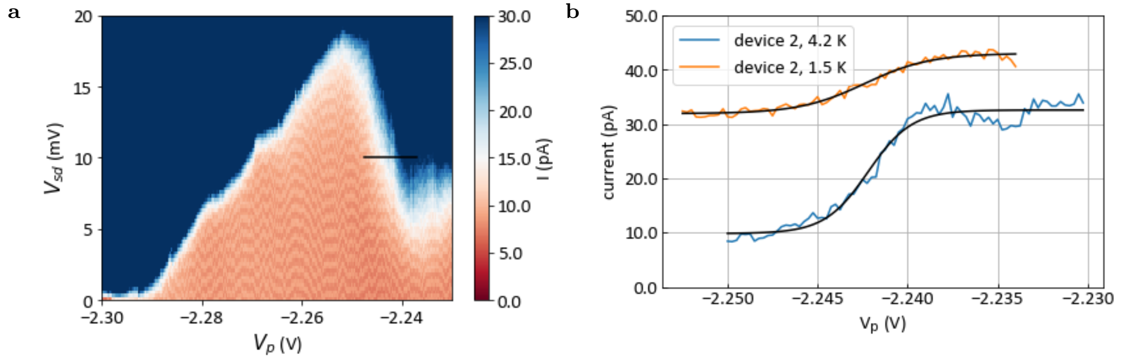

Figure 5.19: A zoom in of a coulomb diamond of device 2 in 5.19a, with the black line the linecut used to perform the fits in 5.19b. Without the 1 K pot running a temperature of 3.1 ± 0.4 *K is extracted while with the 1 K pot running a temperature of* 4.6 ± 0.3 *K is found.*

The results from the two methods of fitting at 4 K vary greatly from device to device. This can be explained by an error in the obtained lever arm which is then used for fitting the temperature. This error is caused by the relatively low resolution of the coulomb diamond measurements and asymmetry in the measured diamonds. While running the 1 K pot and lowering the temperature no improvement is seen in the electronic temperature, in the case of the Fermi-Dirac method the fitted temperature increased while running the 1 K pot. This can be caused by the increase of voltage noise while running the pump, and the bias broadening effect. We can however conclude from these results that in the current configuration with the 1 K pot running the signal-to-noise ratio is not good enough to perform measurements at 1.5 K. Further measurements in this report are therefore performed at 4 K.

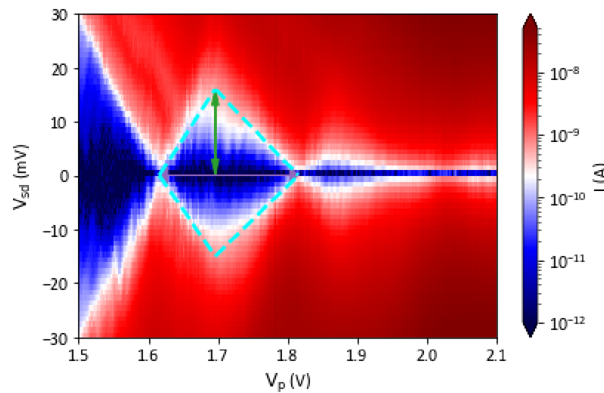

Figure 5.20: Coulomb diamonds formed in device 25 for the electron side, the dashed cyan lines mark the coulomb diamond, the green arrow indicates the ΔV_{sd}*. The purple arrow indicates* V_g*.*

Now we focus on the electron side of device 25, since this device showed some isolated coulomb

peaks in the pinch-off curve. In figure 5.20 the formed coulomb diamonds at $V_L = 5.5$ V are shown. We extract $\Delta V_{sd} = 16$ mV and $V_g = 199$ mV, with these values we find a lever arm ($\alpha = \Delta V_{sd}/\Delta V_g$) of 0.08 meV/mV, a gate capacitance (C_g) of 0.8 aF and addition energy (E_{add}) of 16 meV. We do see the formation of one clear diamond and one very small diamond. However the formed diamonds show some asymmetry, which makes estimate of the dot parameters difficult.

In figure 5.21 we show the measured coulomb diamonds for the hole side of device 2. We note that this device shows a lot of disorder and the diamonds do not fully close. This combination makes it impossible to extract important device parameters. From the last diamond the lever arm was found to be approximately 0.22 meV/mV.

For comparison a similar device (gate length 20 nm, fin width 20 nm and gate spacing 35 nm, similar to device 23 in this section) has been bonded and tested using a dipstick set-up in LHe. The results from these measurements can be found in appendix G. In summary we note that the pinch-off for electrons and holes in this device is found around 1 V, which is in line with previous results obtained in these devices [28]. The lever arm is approximately twice as high and the addition energy is similar. Furthermore, we have shown that two of these devices can be used to operate as a CMOS logic gate. Which could be important for future applications, in which the best devices are used as qubits and the others can be used for control electronics.

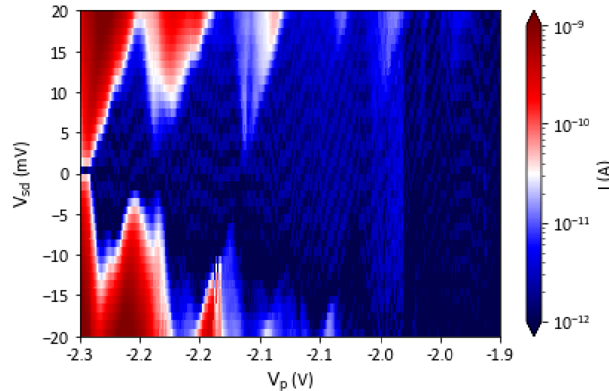

Figure 5.21: Coulomb diamonds formed in device 2 for the hole side, some diamond features are visible but we were unable to extract exact device parameters.

In all the measurements with the cryo-prober a lot of 50 Hz noise is visible, this identifiable through the background oscillations in the current. These are caused by ground loops in the setup. These ground loops can occur between the different instrument and then insert. For the future we plan to have a more detailed look in these ground loops to remove these from our measurements.

5.5 Fast testing technology for quantum devices a discussion

With this work we have made a large step towards a flexible rapid cryogenic quantum device probe station. 21 single quantum dot devices have been identified and measured in this first experiment with the cryo-prober. Furthermore, after localization of the devices we were able to automate the measurements and perform a standardized measurement sequence, to investigate the transistor properties of these devices. This the first potential demonstration of a laboratory scale autonomous cryogenic probe station. In the future we can use the distances between the devices to further automate this measurement procedure. Such that after a set of devices has been selected and a

measurement routine has been made, no human interference or supervision is necessary to complete a measurement run.

To perform these fully automated measurement sequences, a better understanding of the read-out problems of the Attocube postioners is required. We overcame these issues by applying a manual correction factor and implementing a wait time after a big step such that in the final step towards the device is smaller, and the effects of local heating of the resistor is minimized. For measurements at 1.5 K a significantly longer waiting time of more than 15 minutes would be necessary to fully compensate for the local heating issues (see figure 4.7). This defeats the point of our rapid testing set-up. Therefore an improvement in the read-out is necessary when characterization of devices at 1.5 K is the goal. This improvement could for example be achieved by using laser interferometry to read out the position of the positioners. This is however an expensive solution which also can cause heating of the sample stage at lower temperatures. At the moment implementation of the cryo-prober in fully fledged dilution refrigerators is not an option as the movement of the piezo positioners causes significant heating. Which means that after a device step a long waiting time has to be implemented to equilibrate the system to base temperature. This waiting time will be longer then the 15 minutes at 1.5 K recorderd here as the cooling power of a dilution refrigerator at base temperature is lower than the used VTI.

The system built here is significantly more flexible in use, given the interchangeable probe-cards, than currently available commercial systems [35, 36]. The large scale testing system as made by Intel [37] is more complex and expensive compared to our system. The Intel system has the advantage that the model can be integrated in large scale silicon foundries because it is capable to test full wafers. However we think that the full commercialization of silicon quantum computing is still a long term dream, minimizing the short term use of this apparatus. Our cryo-prober can be used in research environments where there is a need for rapid characterization of multiple devices. This of course involves research in silicon quantum computing devices. However, laboratories trying to upscale other quantum technologies which require rapid low temperature characterization. To for example obtain statistics about device operation, can also benefit from this development.

We used the cryo-prober to try to optimize gate-layout of our devices. In the future it can be used to quickly characterize devices in order to obtain statistics on the device parameters. This is important to test reproducibility and stability of the fabrication process. In the cryogenic CMOS research some studies have been done on CMOS devices at cryogenic temperatures [39]. Currently, this requires individual wire-bonding of the devices, which is a time consuming process. We have also showcased the room temperature capabilities of the cryo-prober, which can be used to further simplify the procedures for statistical measurements on CMOS transistors. Thus, we show that a single measurement device can be used to test properties of CMOS transistors at room temperature and at cryogenic temperatures.

The devices we tested with the cryo-prober show some shortcomings compared to devices tested using a more traditional wire-bonded setup. We find that the turn-on voltage of the cryo-prober devices is a factor two higher than obtained with bonded devices. We note that as expected the addition energy obtained in both types of measurements is similar. The lever arm – which is the capacitance – is device dependent but should not depend on the measurement method. Given that there are no additional capacitances present in the cryo-prober setup compared to a wire-bonded setup. Our finding that the transistor properties of the tested devices improve at higher biases is in line with what is found using bonded devices.

The bonded devices are from a different fabrication run which might explain some of the differences we found during this study. It could be that during the fabrication process of the chip currently used in the cryo-prober something went wrong causing these differences. To investigate this further, more devices and chips need to be cooled down in the cryo-prober. Another cause of

the observed problems with the cryo-prober could be poor contact between the probe needles and the devices. However we found no clear evidence for this in our tests; no influence of the amount of pressure applied on the needles on the pinch-off curves was found. Furthermore channel resistances recorded with the cryo-prober are comparable to wire-bonded devices (for both electrons and holes). We also note that theoretically the contact resistance compared to dot resistance is minimal. Furthermore no capacitive charging effects were observed in the measurements in which the plunger or lead gates were swept. This indicates that the waiting time between measuring and changing the voltage on our gates is sufficiently long enough to overcome the RC-time of the resistor capacitor-circuit formed by the gate and potential contact resistance.

The yield of working devices after pre-characterization using the cryo-prober was significantly higher than obtained using a traditional wire-bonded setup (78 % compared to 40 %). If the yield using a wire-bonder remains this low, we can implement RF lines and a RF probecard on the cryo-prober. In combination with a dewar with a magnet we can then potentially operate spin qubits using the cryo-prober. Here again we can use the flexibility of the cryo-prober to test multiple devices and test for reproducibility of the results.

Chapter 6

Conclusion

In this work we have performed measurements on Pauli spin blockade in doule quantum dot devices fabricated on silicon fin field-effect transistors. Furthermore a rapid testing technology, we named the cryo-prober, was developed for the characterization of the properties of silicon fin field-effect transistors at cryogenic temperatures. In this chapter we will summarise the most important results, draw conclusions and give an outlook on future possibilities with these results.

We have shown ambipolar Pauli spin blockade in simple double quantum dot devices. With this first demonstration of ambipolar spin blockade in these devices, we have shown that, in principle, both electron and hole spin qubits can be formed in these devices. For now the main interest for these devices lies predominantly in holes. However, electrons can be used to probe the hyperfine field and understand the nuclear spin noise environment in which the spin qubits reside.

We found an effective hyperfine field of 0.5 mT, which is about an order of magnitude smaller than in GaAs [79]. However, the extracted upper bound for the coherence time (20 ns) is rather low and orders of magnitudes smaller than in purified silicon spin qubits, even when accounting for the reduction in spin carrying Si-29 atoms. When investigating the hyperfine lifting of the spin blockade we also discovered a new type of spin blockade lifting feature. At this point we can only speculate about the origin of this feature, and a more quantitative analysis of this feature over multiple devices is necessary. It could be caused by a competition between the spin-orbit interaction and the hyperfine field. Valley effects were also uncovered at higher fields when investigating Pauli spin blockade. These valleys can in principle also be used to drive a qubit [52]. Further investigation are necessary to find the valley-splitting in these devices, a lack of experimentally verifiable effective g-factor prevents us from determining the valley-splitting.

The hole spin blockade we found in this device was observed in a regime with a very low current signal. We observe a zero-field current dip as predicted by Danon et. al. [60]. However the baseline of this bias triangle completely vanishes at zero field instead of showing 1/9 of the original current as it was predicted in Ref [60]. The low current in this sample might have obscured this factor 1/9, however other measurements performed on similar devices also do not show a residual current of 1/9 of the high field current [29]. We see some signatures of the characteristic spin-orbit anticrossing in this sample but it is was not possible to determine the spin-orbit strength. We do extract the out-of-plane g-factor anisotropy which shows 2π periodicity, with a maximum modulation of 30%, and a phase shift from the in plane direction of 13 °. We note that that this device could not be tuned to the two hole regime. Which means that further investigation of the g-factor anisotropy is necessary to exclude that orbital effects are the underlying cause of the observed anisotropy.

The results of the measurements on these devices are promising for future research in these silicon FinFET transistor quantum dot devices. In fabrication, progress has to be made to achieve

control over all the tunnel barriers and thus enable the tuning of the double quantum dots in to the two electron regime. The first steps of this progress have already been made in the form of a self-aligned second gate layer [29]. Further investigations to determine the anisotropy of the spin-orbit strength is necessary, but with this work we laid the groundwork for these future measurements. By providing a model to understand the charge transitions in a double dot system and some reference measurements.

In the second part of this thesis we have built and operated an automated probe station suitable for operation at cryogenic temperatures. With this so called cryo-prober, we have been able to perform automated measurements of 21 independent devices at 4.2 K. The results obtained show the potential of this technology for gaining statistical information about device operation at cryogenic temperatures. Which is of importance in the scaling up of spin qubit quantum computing platforms. Furthermore, there is potential for expansion beyond the realm of spin qubits with the interchangeable probe card and its ease of use.

The acquired results with the cryo-prober show discrepancies with earlier measurements with similar but wire-bonded devices. At the moment it is unclear what the cause of these discrepancies is. We have ruled out effects of poor contact between the needles and the device leading to high contact resistance. Another cause of these discrepancies could be a fault in the fabrication procedure involving this specific chip. Further investigation rounds is necessary to narrow down the cause of these discrepancies. We also note that thermal contact between the sample stage and 1 K pot was poor in our case which meant we were not able to cool the samples electronic temperature below 4.2 K despite the fact that the 1 K pot was operated and at 1.5 K. Besides this a full investigation of the voltage noise needs to be performed on the cryo-prober. With this the signal-to-noise ratio can be improved and measurements can be performed at lower biases, improving the results of the temperature measurements using the cryo-prober. Another open issue with the cryo-prober is local heating of the postioners, to be more specific the resistor responsible for the position read-out. This causes that in case for big steps the desired coordinates are not reached. To circumvent this a short waiting period (30-60 seconds) is implemented in the automated stepping procedure.

All in all we have shown a first working prototype of such a cryogenic probe staion and we think that most of the issues which came up during this work can be resolved with some minor tweaks in the set-up. We believe that this technology could assist in the scaling of quantum devices in particular in the field of silicon spin qubits.

Outlook

During the time this research was conducted, a hole spin qubit was formed and operated, in two independent silicon FinFET devices and the first results of these measurements are very promising. Several fundamental questions which are important for the control and operation of these qubits are still open. Mainly the direction of the spin-orbit vector, which we attempted to investigate in this work. The interplay between the hyperfine interaction and the spin-orbit interaction also needs to be further understood. To operate these devices at their full potential, the spin-orbit vector needs to be known. We recommended to investigate the spin-orbit strength using a double gate layer device such that there is more control over the tunnel couplings and a the two electron regime can be reached.

To gain more information about the charge state in the double dot charge sensing has to be implemented. The lowest footprint type of charge read-out is based on RF-reflectometry [12] and has already been implemented by several groups [19, 80]. The implementation of this technique will also improve read-out of spin states when operating a qubit enabling more complicated pulse sequences.

A device in the two-electron regime is necessary to understand the behaviour of the hyperfine spin blockade lifting mechanism. Understanding and, possibly being able to tune the hyperfine interaction [81], would be of great importance in increasing the coherence time of hole spin qubits in these silicon FinFet devices. This only helps if the coherence time is limited by nuclear noise and not by charge noise.

To better understand the plethora of transitions in the Pauli spin blockade regime we built a model. This model can be expanded with a density of states approach. This enables to also investigate and predict the relative visibility of the transitions during the measurements.

To improve the thermal contact between the sample stage and the 1 K pot in the cryo-prober a copper sample stage with copper braid connecting the sample stage to the 1 K pot has been fabricated, and mounted during the writing process of this thesis. This copper sample stage is currently being tested. During these tests it will also be determined if the discrepancies between bonded devices and the probed devices are due to a fault in the fabrication procedure or due to poor contact between the probe needles and the devices.

Longer term improvements for the cryo-prober involve a wider bore diameter, such that all the 192 devices on the the 2x2 cm chip can be reached. We estimate that a bore diameter of 90 - 100 mm should big enough to reach the all the devices. Another improvement could be the implementation of laser interferometry read-out of the position of the positioners. This solution is however relatively expensive and is optional as we have shown that with a slightly altered procedure automated operation of the cryo-prober is already possible.

In short, the future of the used silicon FinFET quantum dot devices is bright, whereas the formation of a qubit and a new project on RF-reflectometry are first steps towards a qubit unit cell [82] can be made. The cryo-prober can help in the scaling up towards a unit cell by operating as a fast characterization tool for selecting the best devices to use as a qubit. The cryo-prober opens the door for quick and affordable characterization of quantum devices, and thus can open the door for the commercialization of quantum technologies. The use of the cryo-prober is not only limited to silicon quantum computing. Any technology requiring cryogenic temperatures with the ambition for an industrial up-scaling, can benefit from the developed technology in this work.

Chapter 7

Acknowledgements

First and foremost I would like to thank Prof. dr. Erik Bakkers and Prof. dr. Dominik Zümbuhl whom gave me the opportunity to work on this inspiring project in Basel. The help and daily supervision of dr. Andreas Kuhlmann and Simon Geyer gave me a lot of energy to keep exploring new physics and technologies during this project. Furthermore I'd like to thank dr. Leon Camenzind for his help with MCK-76 and his great introduction to spin qubits through the virtual spin qubit meetings. Andreas, Leon and Simon also gave me a chance to explore and work on ongoing spin qubit measurements in the lab, which further deepened my understanding of spin qubits and their operation. I thank them for their introduction to this completely new type of experiment for me. Rafael Eggli was a very helpful project student and assisted me with several measurements throughout the year, I wish him all the best with the completion of his master thesis on RF-reflectometry in the FinFET devices. I would also like to take this opportunity to thank Micheal Steinacher from the electronics workshop for his help and patience while explaining the important principles of electrical wiring and measuring to me, while I was assembling and testing the cryo prober.

The rest of the Quantum Coherence Lab is thanked for all their help in and around the cryo hall. Despite Covid-19 I had a great year in Basel and the whole group contributed to this, the semi-weekly lab beers and our lunches together were a nice form of relaxation after and during a long week of running sometimes frustrating experiments.

Last not but least I would like to thank all my friends in Eindhoven, this includes but is not limited to the on discord active (oud-)Borreltenders, Annemarie, Mathijs and Lotte. Finally a special thanks to my parents who always supported me and my choices on this journey in Basel.

Appendix A

Simulation parameters

In this appendix the parameter used for the simulations in figures 3.4 and 5.5 are shown. These values can be found in table A.1.

Table A.1: The simulation parameters used for the two overlaid models in the main text.

Parameter	Simulation 1 (figure 3.4)	Simulation 2 (figure 5.5)
t	0.0215 meV	0.0215 meV
g	1.6	0.97
t_2	0.3t	0.3t
V	1 meV	1 meV
Δ_{so}	0.25 meV	0.065 meV
ΔST	1.8 meV	0.24 meV

Appendix B

Electrical wiring of setups

In this appendix the wiring diagrams for the two different set-ups are sketched. In figure B.1 the wiring diagram for the MCK-76 set-up is shown. In yellow a Basel Precision Instruments LNHR DAC to supply voltages to the sample, in purple a two low noise high stability I to V converters (SP 983c) also from Basel Precision Instruments. The red box is signal combiner box which subtracts the signals of the two IV converters before the signal is read out by that NI data acquisition card. This subtraction is giving us twice the signal flowing through source and drain, this is because we measure at both source and drain which have opposite polarity. The NI-DAQ model used in this set-up is an USB-6366, with 8 analog input channels of which just one is used.

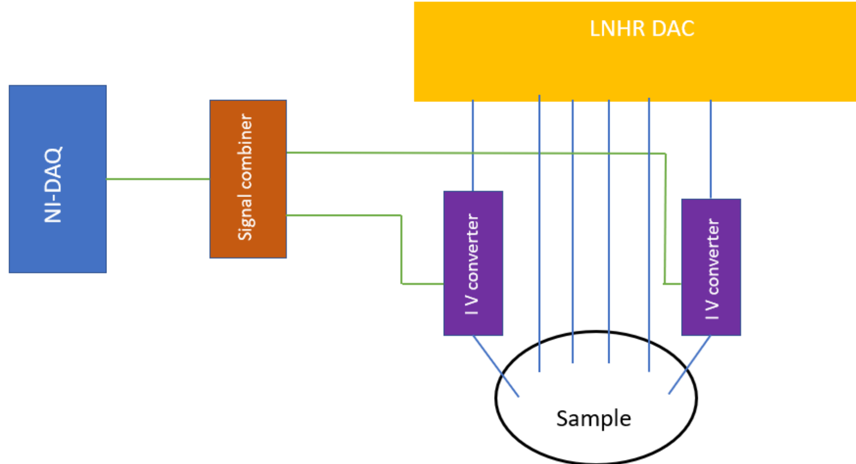

Figure B.1: A diagram of the electrical set-up of the MCK-76 dilution refrigerator. In blue are the lines towards the sample and in green the measurements lines.

In figure B.2, the wiring diagram for the cryo prober is shown. Here again the basis is a LNHR DAC from Basel Precision Instrument. We now use a so called Gate Leakage Measurement Box (GLMB), which is basically a box with 6 I to V converters on the inside, this box enables us to measure the leakage of every gate in our device while measuring a sample. We again have to SP 983C I to V converters for source and drain, these are used over the GLMB because they have a finer control over the amplification settings which is important for the measurements. The signal combiner in this set-up outputs the subtracted and added signal of the source and drain, this way we can measure both leakage and actual current at the source and drain. The NI data acquisition

card used in this set-up is a USB-6363 BNC with 16 analog input channels of which we use 5 in this case. This NI DAQ has enough channels to be able to measure the leakage on all gates on a double gate layer double quantum dot device, which would need 9 channels.

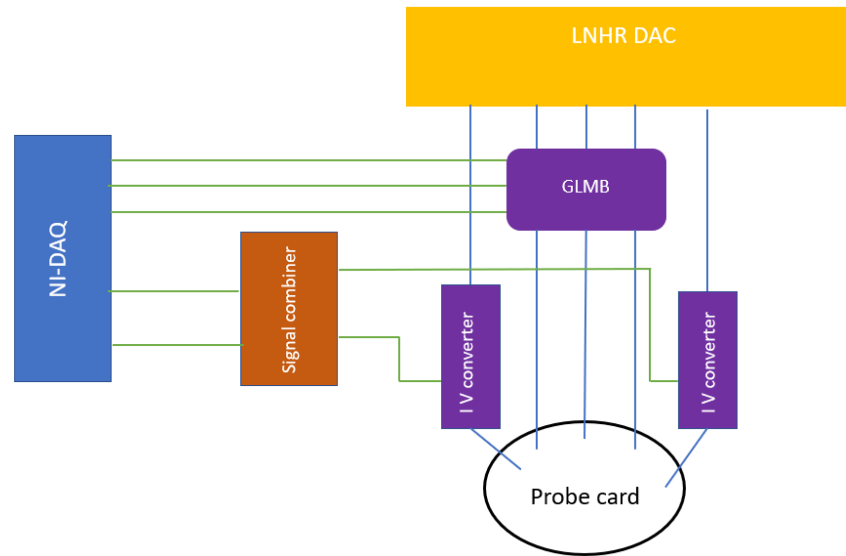

Figure B.2: A diagram of the electrical set-up of the cryoprober. In blue are the lines towards the sample and in green the measurements lines.

Appendix C

Deviation of positioners

In this appendix the data collected for the deviation of the positioners after a big (1 mm) step is shown. This data is obtained by sending a move command to the positioners then waiting 10 seconds and sending the same move command again, after which a measurement of the position is taken every 10 seconds. In figure C.1 the results for the x-axis are shown while figure C.2 shows the results for the y-axis. In both case we stepped in the positive and negative direction.

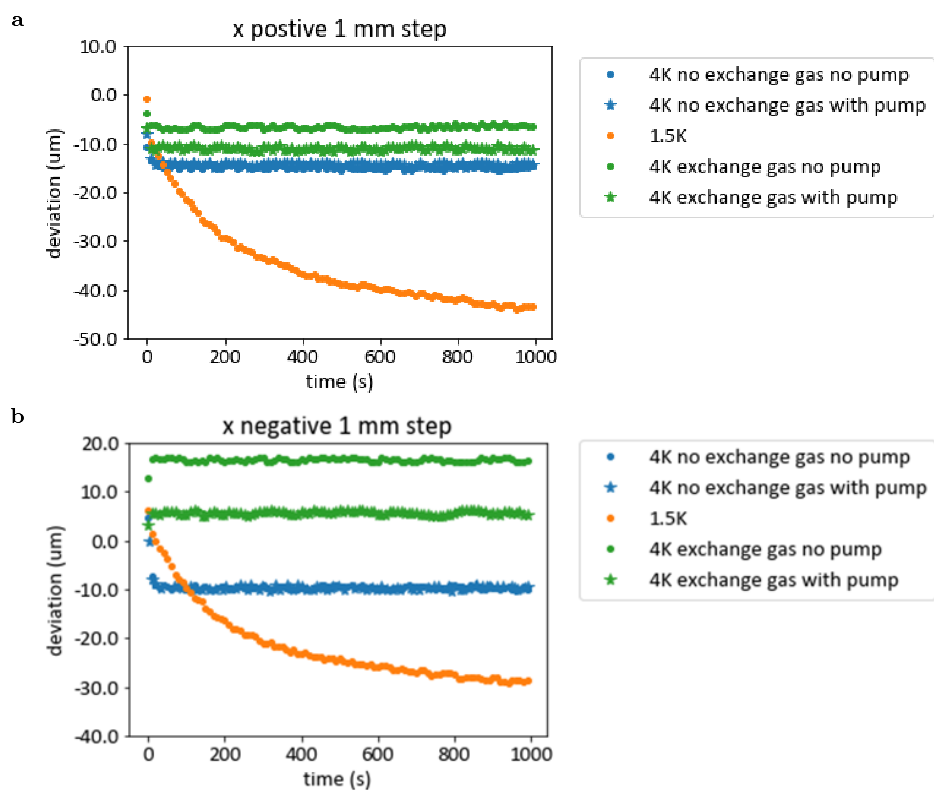

Figure C.1: Stability of the x positioner after a 1 mm step.

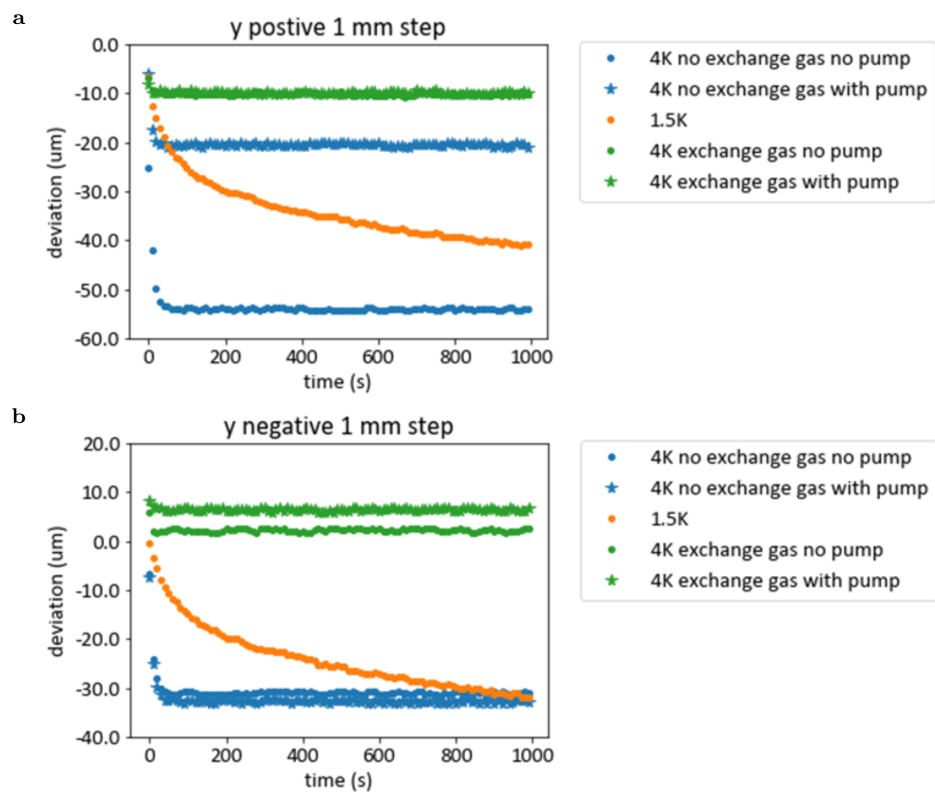

Figure C.2: Stability of the y positioner after a 1 mm step.

Appendix D

Overview of the cryo prober GUI

In this appendix an overview of the GUI built for the cryo prober is given, this overview can serve as a manual for operation of the cryo prober in its current state. The GUI is show in figure **??**, the numbers on the GUI are explained in the list below. The main goal of the GUI is to be able to automate measurements over multiple devices which are fabricated in a grid like structure. We can give a simple one measurement instruction or feed a more complicated sequence of measurements using a text file.

1. Here the distance between the devices can be set as well as the amount of devices shown on the grid at 17.
2. Here a continuous read-out of the positioners is shown.
3. In this part we can use to device on a horizontal line to calculate the angle of the chip with respect to the probes and use that data to correct the position of the devices.
4. Here we can specify the type of sequence and order in which the selected devices will be measured.
5. These controls move the z-positioner .
6. These controls move the x and y positioner.
7. Here important measurement parameters like, start value, stop value and amount of points taken can be added.
8. Here the settlingtime between the step on the DAC and the integration time for the measurement is set.
9. Here we look for a txt file with a sequence of measurement commands.
10. Here we select on which channels to measure.
11. here we select which channels to sweep during a measurement.
12. Here we can set the sampling rate of the NI-DAQ and integration time.
13. Here we set the measurement type desired to be taken.
14. Here we can select devices on the grid at 17 and also select which device acts as a reference device.
15. Here we set the position of the reference device, such that the coordinates of the other devices can be calculated using the data from 1 and 3.

16. Here we set the voltage and amplitude of the saw tooth signal for the positioners

17. This is the grid of devices, on this grid devices can be selected for measurement by clicking using the tools in 14, afterwards a sequential measurement over these devices can be performed.

Figure D.1: A screenshot of the GUI made for the operation of the cryo prober, the functions at the numbers are explained in the text.

Appendix E

Electron spin blockade fits

The fits for the hyperfine field and tunnel coupling from the electron spin blockade in 5.1 are worked out in this section. In figure the peak to peak separation is plotted, the peaks are obtained using a peak finding algorithm. Through these data points a standard equation for level repulsion is fitted [64]. The extracted fit parameters with standard deviation can be found in table E.1. In figure E.1b a linecut at 0.7 meV detuning is plotted and fitted with equation 11 of [69], which gives the Hyperfine field and tunnel rate, the fitted parameters can be found in table E.2

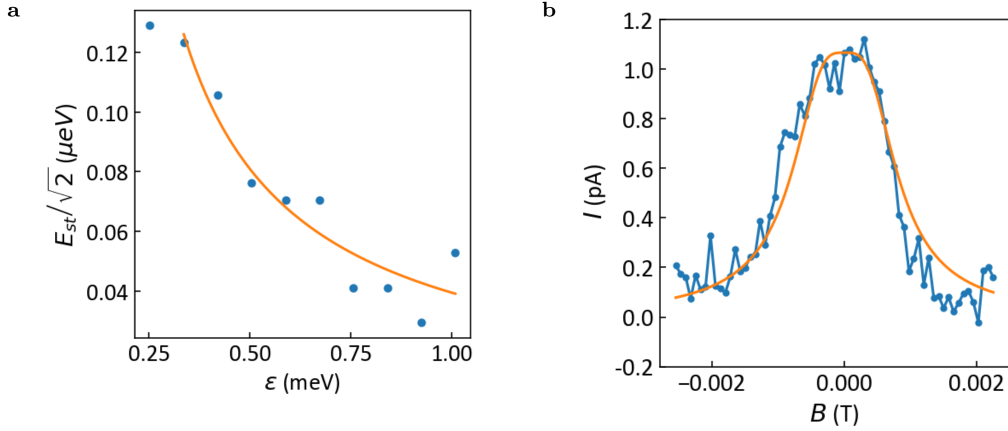

Figure E.1: In E.1a distance between the peaks figure 5.2c are plotted together with a fit of the standard anticrossing expression. E.1b shows the linecut at 0.7 meV detuning, showing a flat peak, this is fitted using equation 11 of [69].

Table E.1: Fit parameters of the fit in figure E.1a.

parameter	value
k	$(3 \pm 1) \cdot 10^6$
t	$(35 \pm 10)\ \mu eV$

Table E.2: Fit parameters of the fit in figure E.1b.

parameter	value
Γ	$(1.00 \pm 0.03) \cdot 10^7$ 1/s
B_N	$(5.0 \pm 0.1) \cdot 10^{-4}$ T

Appendix F

Cryo prober extra measurements

In this appendix we show some extra measurements taken with the cryo prober. In figure F.1 measurements of the leaky devices are shown. Table F.1 shows the extracted parameters for transistor operation. In figures F.2 and F.3 we plot the threshold voltage and subthreshold swing for the tested devices under high bias. Figures F.5 and F.4 show the transistor curves for all devices. Finally in figure F.6 we show the pinch-off curves of all tested devices for both holes and electrons at 1 mV bias.

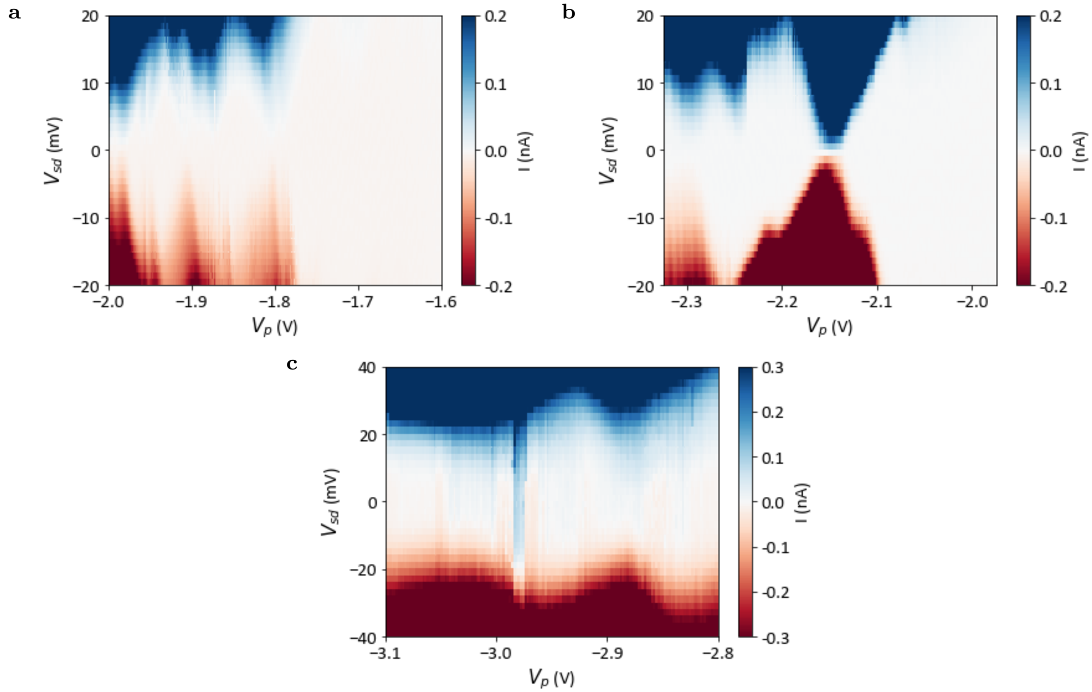

Figure F.1: Plunger versus bias sweeps on the devices 1 (F.1a), 8 (F.1b) and 15 (F.1c). These devices showed leakage between lead gate and source/drain before the final testing stage could be reached.

Table F.1: Overview of the transistor parameters for the 21 devices tested.

Device	**Electron low bias**		**Electron high bias**		**Hole low bias**		**Hole high bias**	
	Vth (V)	SS (mV)	Vth (V)	SS (mV)	Vth (V)	SS (mV)	Vth (V)	SS (mV)
2	1.476	65.48	0.752	13.47	-2.183	31.77	-1.472	30.7.0
4	1.223	8.05	0.519	118.5	-2.390	26.61	-1.273	26.39
5	1.310	52.72	0.433	10.35	-2.809	77.91	-1.160	9.82
6	1.794	55.79	1.222	32.30	-1.667	11.02	-1.371	119.00
10	2.619	65.23	1.092	19.35	-1.682	24.58	-1.013	119.62
11	2.089	104.32	0.765	50.84	-1.803	6.45	-1.143	8.49
12	1.712	21.15	0.370	7.37	-2.711	112.3	-1.716	99.33
14	2.841	42.66	1.610	20.62	-2.633	14.49	-1.221	10.78
16	1.872	38.69	1.212	54.00	-2.020	108.03	-1.059	11.34
17	1.104	19.94	0.565	28.89	-1.902	21.01	-1.331	101.31
18	1.238	18.77	0.554	2.97	-2.368	42.06	-1.339	30.91
19	2.243	26.84	0.467	15.59	-2.841	90.56	-1.432	8.08
20	1.472	20.72	0.519	5.94	-2.493	67.62	-1.178	57.75
21	2.050	47.57	1.133	45.98	-2.597	63.85	-1.382	27.87
22	1.756	8.12	0.725	58.25	-2.545	86.39	-1.393	9.92
23	2.291	86.26	0.905	25.95	-2.091	12.79	-1.422	86.75
25	1.406	5.24	0.763	13.68	-2.064	7.01	-1.673	52.67
26	2.897	177.35	1.703	61.40	-2.938	26.38	-1.300	24.4
27	1.117	21.74	0.526	3.57	-2.920	96.28	-1.433	143.59
29	1.846	97.21	0.997	15.52	-2.900	88.55	-1.801	36.78
30	2.611	57.39	1.335	35.59	-2.718	122.8	-2.102	41.99

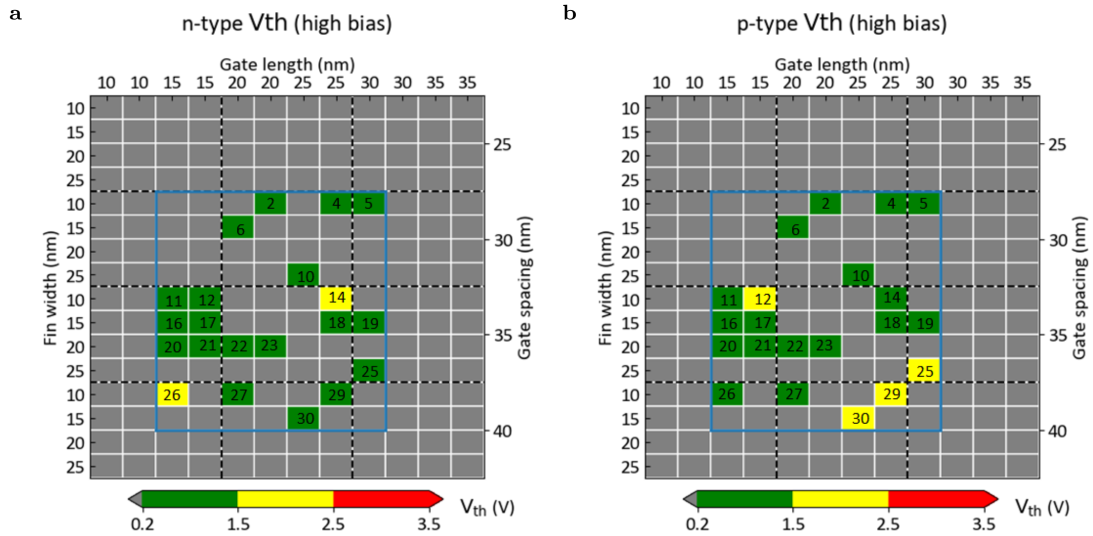

Figure F.2: Classification of the threshold voltage under high (1 V) bias.

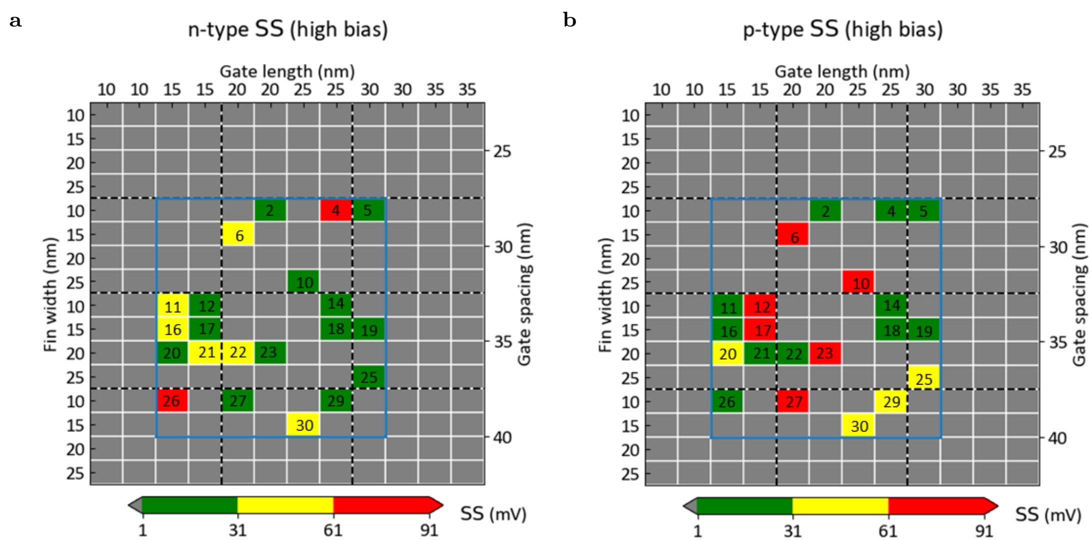

Figure F.3: Classification of the subthreshold swing under high (1 V) bias.

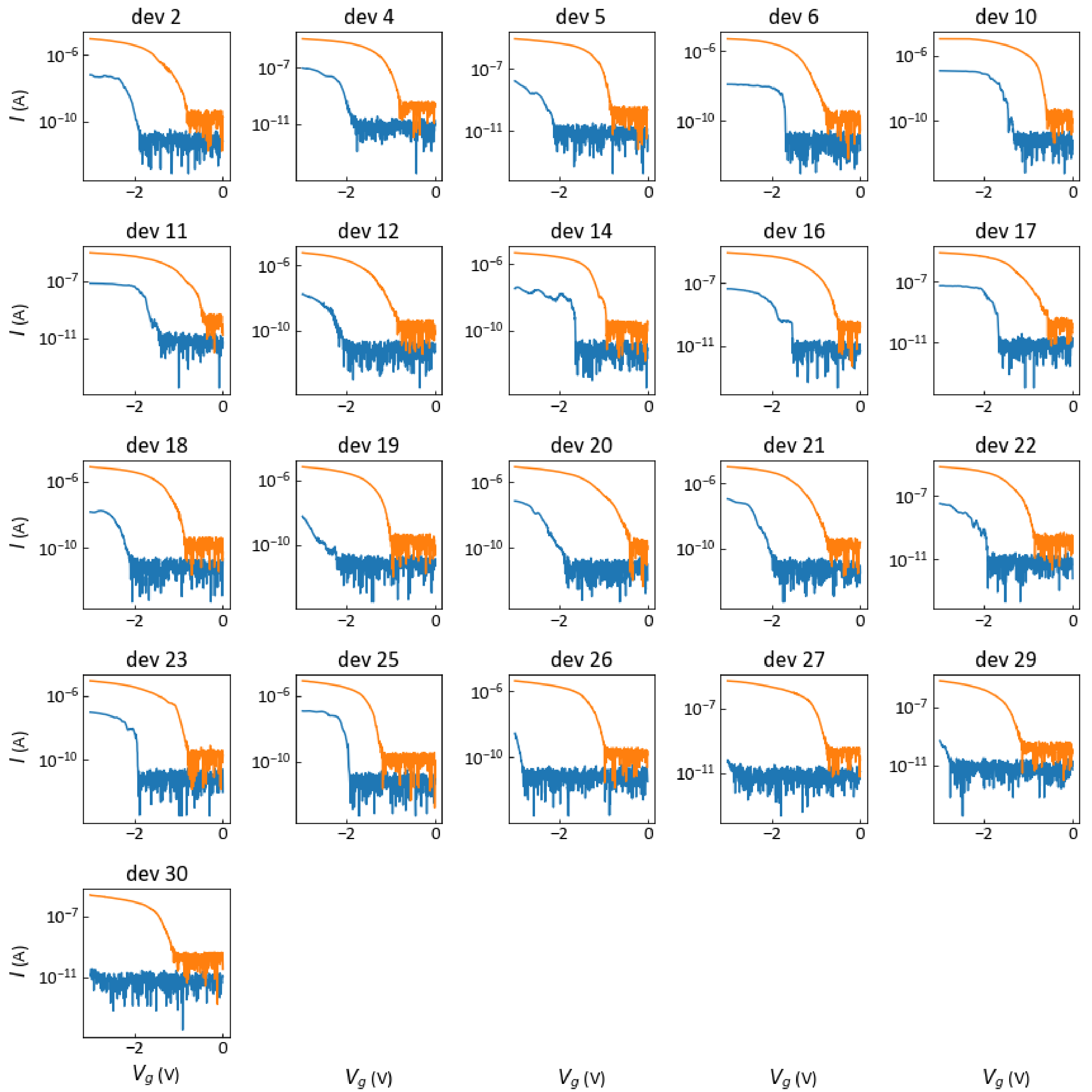

Figure F.4: P-type transistor IV curves in case of low bias (100 mV) and high bias (1 V) for 21 different devices. The low bias is shown in blue and high bias in orange.

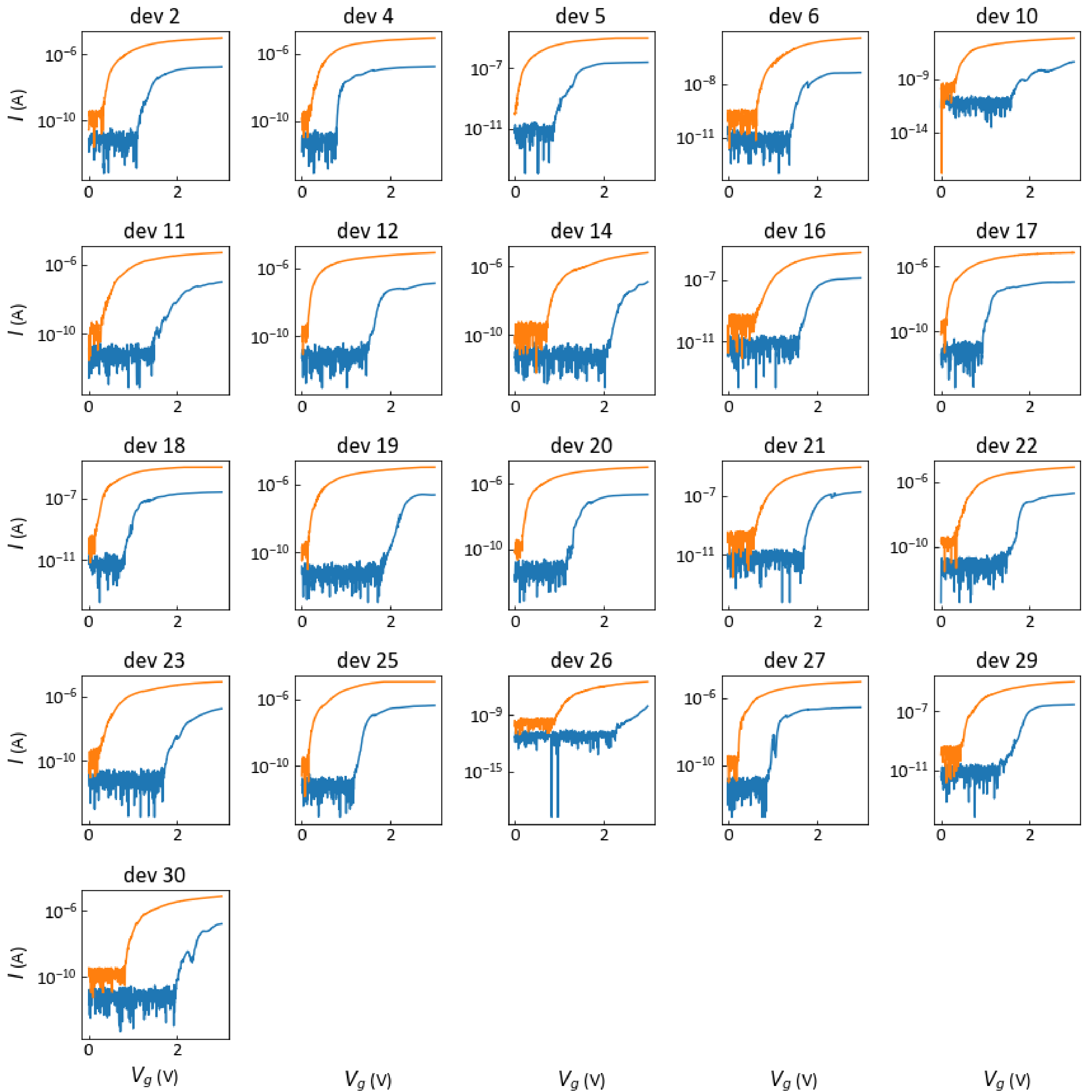

Figure F.5: N-type transistor IV curves in case of low bias (100 mV) and high bias (1 V) for 21 different devices. The low bias is shown in blue and high bias in orange.

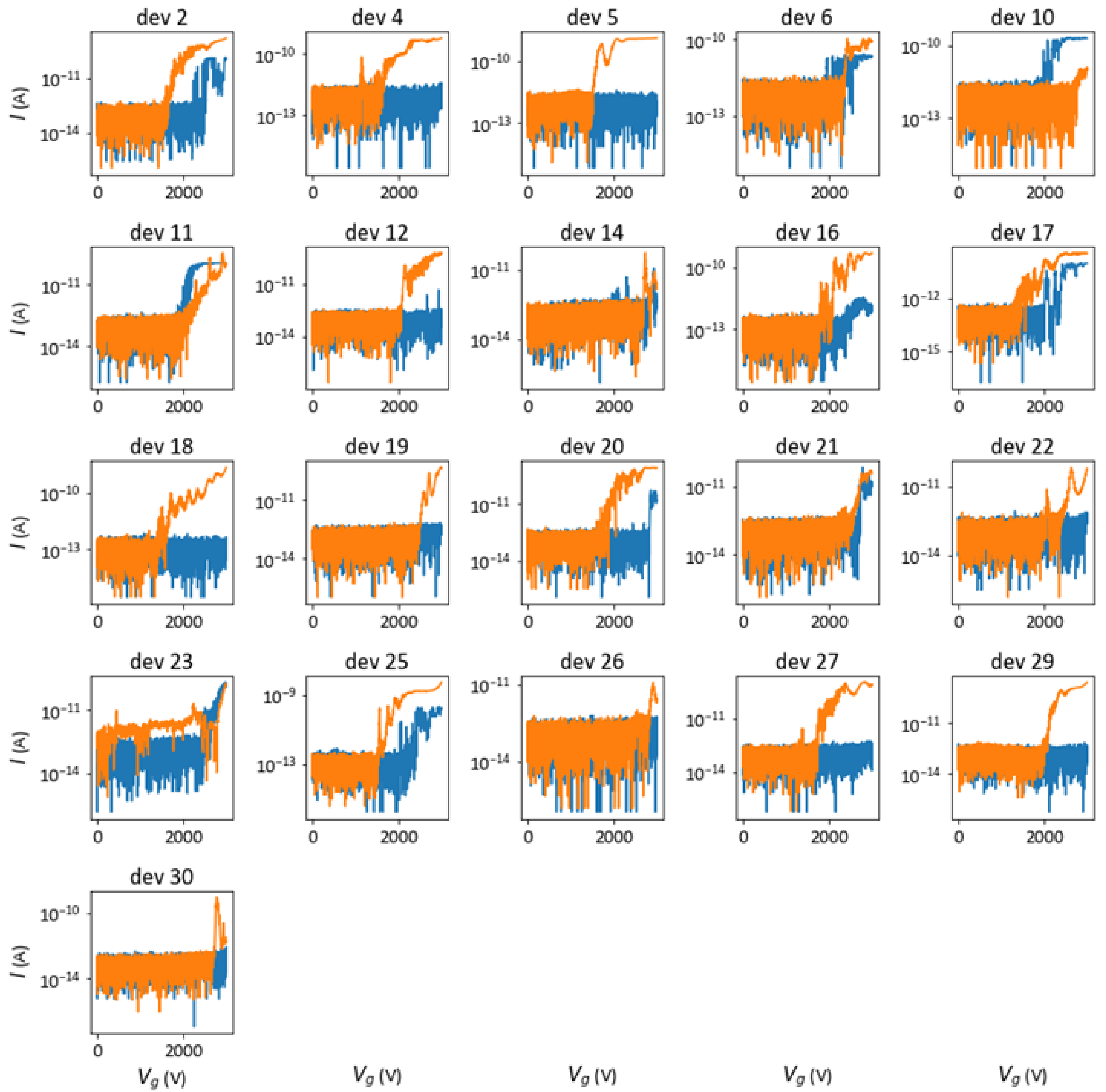

Figure F.6: Pinch curves at both the hole side (blue) and electron side (orange) taken at 1 mV bias.

Appendix G

Bonded benchmark devices

In this appendix we report on the results of a device, similar to device 23 from the cryo prober, while being bonded. The device parameters of this device are a gate length of 20 nm, fin width of 20 nm and gate spacing of 35 nm. These results could function as a benchmark for the the cryo prober. We will focus on the quantum dot performance of this device and in the end show that this device together with another device can function as a CMOS logic inverter.

In figure G.1a we show the coulomb diamonds formed on the hole side of this device. In this case multiple coulomb diamonds are visible, the first one fully visible is used to extract the relevant parameters (as marked by the cyan lines). We obtain a lever arm of 0.22, a gate capacitance of 2.3 aF and an addition energy of 16 meV. We observe that the first diamond appears at -0.8 V.

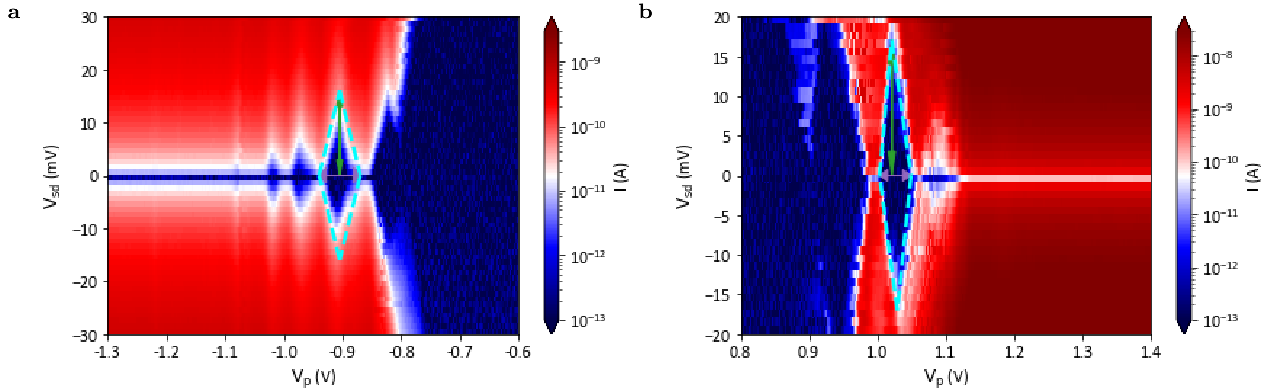

Figure G.1: Coulomb diamonds measured in this device for both the electron and hole side, the cyan marked diamonds are used to extract the parameters. Results are obtained at $\mathrm{V_L} = -4$ *V (holes) and* $\mathrm{V_L} = 5$ *V (electrons).*

In figure G.1b the coulomb diamonds for the electron side are plotted, this data is obtained at $\mathrm{V_L} = 5$ V. In this case only one clear diamond is visible, however here the first signals of diamonds are also visible around 0.9 V. From this diamond we obtain a lever arm of 0.34, a gate capacitance of 3.4 aF and an addition energy of 17 meV. These values are similar to the hole side of this device.

No individual transistor characteristics of this device are available, however in combination with another device this device was used in a standard CMOS inverter logic gate at 4 K. To do this we obtained the channel resistance of both used devices and tuned them such that the channel resistance of the point of measurement was similar for n and p-type. The used configurations and

resistances can be found in table G.1.

Table G.1: Channel resistances used for operation of the inverter gate

configuration	V_L p-type (V)	R p-type (Ω)	V_L n-type (V)	R n-type (Ω)	R_p/R_n
1	2.25	$9.7 \cdot 10^8$	-3	$7.5 \cdot 10^8$	1.29
2	2.75	$1.4 \cdot 10^8$	-3.5	$1.9 \cdot 10^8$	0.73
3	3.25	$3.2 \cdot 10^7$	-4.25	$3.0 \cdot 10^7$	1.06
4	3.5	$1 \cdot 10^7$	-4.75	$9.6 \cdot 10^6$	1.04

To characterize the inverter properties we look at the ratio of the maximum voltage and the input voltage and the inverter opening voltage. In the ideal case the first ratio is 1 and the second ratio is 0.5. In figure G.2a for higher biases and lower channel resistance the ratio V_{max}/V_{bias} gets closer to 1. Furthermore we find that the ideal ratio of V_{open}/V_{bias} is only approached in the case of a high bias (1 V), in other cases the inverter is far from ideal. Despite the non-ideal behaviour we have shown that these devices, given the right bias can operate in a CMOS inverter logic gate, which enables the use of these devices in cryogenic logic circuits necessary to operate qubits.

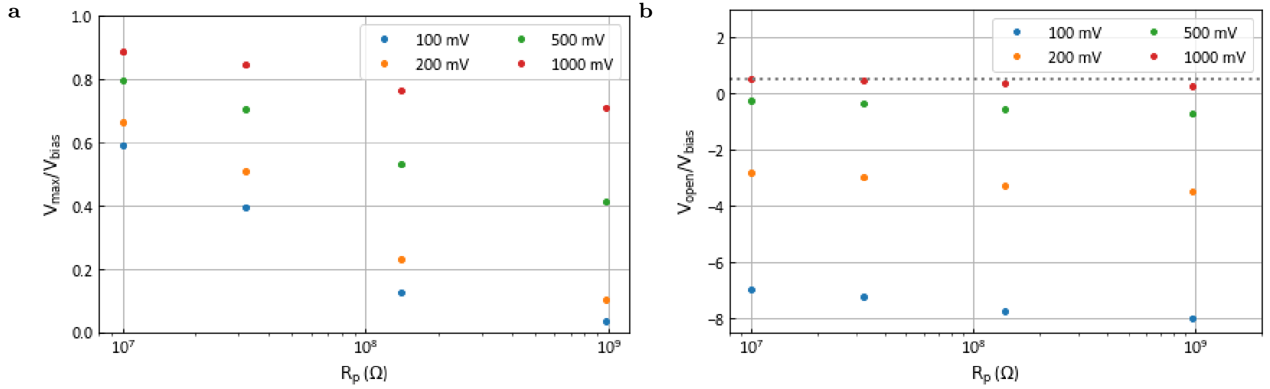

Figure G.2: Inverter properties of two single dot devices as an inverter logic gate at 4.2 K, with in G.2a the ration of the on-state voltage and the applied bias and in G.2b the ratio of the opening voltage and the applied bias, with in gray the ideal situation as a reference point.

In short we have quantified the quantum dot properties of these single gate layer single quantum dot devices for both electrons and holes. Furthermore we have shown that two of these devices together can operate as a CMOS logic gate, paving the way for more complicated circuits and applications at cryogenic temperatures.

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