Optimal tuning of Electrochemical Neuromorphic Organic Devices for on-chip neural network applications

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Master Thesis

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Abstract

Computers are an essential part in our modern digital life. Billions of transistors form the beating heart of these devices which need to solve increasingly more complex algorithms in order to satisfy our information appetite. Object detection in images, speech recognition and self-driving cars are a few examples of modern computing in our society but they consume a lot of power, because they rely on simulated artificial neural networks (ANN) in order to function properly. To reduce the energy consumption of these ANNs inspiration is drawn from the human brain which consumes just a fraction of the amount of energy ($\leq$ 20 Watts) while recognizing objects and faces effortlessly. To emulate this functionality in hardware, special devices called ENODes (Electrochemical Neuromorphic Organic Devices) can be used that mimic the functionality of a human brain synapse, resulting in a drastically reduced power consumption. The conductance of a single ENODe device can be tuned to directly resemble the synaptic weight in artificial neural networks as well as actual synapses between two neurons in a brain, thereby training the neural network. However, accessing individual devices in a network configuration can be problematic due to so-called sneak currents resulting in unintentional tuning and training.

This thesis investigates the feasibility of using light pulses to optically tune ENODes, aiming to overcome challenges that large hardware-based neural networks face. This is achieved by accompanying each ENODe with two solar cells that each have a dedicated LED to tune ENODe bidirectionally. Characterisation of this new device layout is carried out and based on these results a hybrid device which integrates the solar cells, ENODe and necessary circuitry is developed and fabricated which facilitates the testing of larger arrays in further research.

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Chapter 1

Background and problem definition

1.1 Introduction

These days, computers are an integral part of our modern digital society and we can not imagine a world without them anymore. At the heart of every computer are billions of transistors present that control the flow of electrons and thereby enable the execution of all sorts of software. One class of novel programs that is becoming increasingly popular are called artificial neural networks (ANNs) and this type of software is used in many areas like weather forecasting[1], stock prediction[2] and the diagnosis of breast cancer[3].

1.2 Artificial Neural Networks

Artificial neural networks consist of three components: i) an input layer of artificial neurons where the problem is inserted in the artificial neural network, ii) optionally one or more 'hidden' layers that process the input data, and iii) an output layer that is often used as a classifier layer (left side of figure 1.1). The processing of each input signal is done by applying different weights ($[0, 1] \in \mathbb{R}$) to every input value and comparing the systems output to the desired output and change the weights of every neuron in the neural network accordingly to better match the future output signal for a certain input signal. By feeding the network hundreds of times with novel information and penalize or reward the network for its decision, the network "learns" to recognize certain patterns and classify them correctly.

This software is built on principles similarly to a mammalian brain and is mostly run on (super) computers using the classical von Neumann architecture which has been the standard of computer architectures since 1960. This architecture physically separates data storage (RAM or ROM memory) from data processing (CPU) and uses a data bus as an interconnect between the two. For most traditional software programs this architecture is adequate but for ANNs this is a very ineffective way of computing as the physical distance between CPU and RAM limits performance and introduces the von Neumann bottleneck[4]. Additionally, common computers use Boolean logic in the form of FETs (Field Effect Transistors)(figure 1.2) whereas artificial neural networks use floating-point arithmetic in the form of vector-matrix multiplication to sequentially update weights which forces the use of multiple FETs to simulate this operation softwarematically to execute the algorithm.

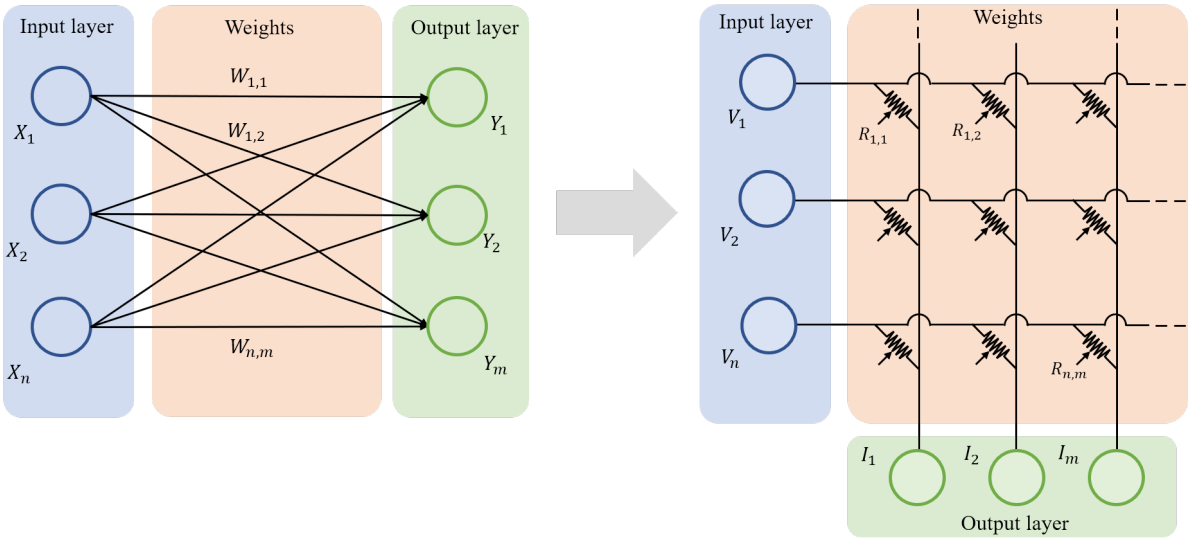


Figure 1.1: *On the left: an illustration of the inner-workings of a neural network when implemented on a software level using vector-matrix multiplication* $Y_m = \sum_n W_{m,n} X_m$. *On the right: the equivalent neural network altered to a hardware-based implementation using the equivalent vector-matrix multiplication in the form of Ohms law* $I_m = \sum_n G_{m,n} V_m$ *with* $G_{m,n}$ *being the conductance of the node. credits:*[5]

Implementing ANNs on a hardware level could resolve these issues. To achieve this, inspiration can be drawn from physical layout of the brain. The two basic computational units that make up the brain are neurons and synapses each serving their own purpose. Neurons perform computations by integrating signals from other neurons via synapses and generate spikes as a result. Synapses add to these calculations by changing the strength of the connection between neurons based on past activation[6]. Devices that inherit at least one of these two basic operations of the brain were first mentioned in 1990 by Carver Mead who introduced the term "neuromorphic systems"[7]. Over the past few decades, various attempts have been made to design neuromorphic systems by searching for materials and systems that use a hardware-based approach to emulate one of these functions into a device to improve the efficiency of ANNs.

One class of devices that emulate neural network functionality are called spiking neural networks (SNNs) which process information by means of changing spike timing and frequency[8;9]. These SNNs can already be found in some commercial products like Truenorth[10] or Neurogrid[11] and have already a power density reduction of 2500x compared to a normal PC CPU[10]. However their relative high manufacturing costs and the fact that backpropagation to train the network is difficult[8] also present some challenges. Nevertheless other researchers have attempted to address this issue[12].

Another class of devices that emulate neuromorphic functionality are called "memristors", or more accurately called memristive devices, and were first theoretically described by Chua in 1971[13] as "the fourth missing circuit element". Later Strukov et al. in 2008[14] identified this phenomenon, although it is still debated if a true/real/-genuine/perfect (all are used in literature) memristor can physically exist[15;16]. We thus use the more general term "memristive device" from now on, or "tunable resistor". These devices emulate synaptic activity instead of neuronal activity as is the case with SNNs. The function of a memristive device can be explained in its simplest form as a resistor that can change its resistance and remember this resistance for a longer period of time, hence its name, memristor[13]. Various switching mechanisms can be used that allow for memristive functionality with a wide range of materials, both organic and inorganic, to accomplish this.

When implementing these memristive devices into a hardware-based configuration as illustrated in figure 1.1 on the right side, a so called crossbar array is used which was demonstrated by Xia & Yang and others[17;18;19] which is the equivalent of a software-based artificial neural network, but then directly implemented into hardware.

1.3 Derived properties for neuromorphic arrays

As discussed in the previous section, to successfully emulate a neural network in a hardware-based neuromorphic array, two prerequisites are to be met. First, the ability for resistance switching must be incorporated into the device. This is important as different weights need to be assigned to various signals. Secondly, the resistance switching device must demonstrate non-volatile characteristics which is important when scaling to larger networks. This section elaborates on various tuning devices and builds up to the introduction of a device that is able to demonstrate both of these prerequisites. Most of the devices that can be used for non-volatile switching are based on basic transistors such as FET and OECT's, which will be briefly discussed first.

1.3.1 Field Effect Transistors

Figure 1.2 shows the standard layout of a FET. Their working principle relies on the generation of an electric field to control the flow of current in the device. A FET is a three-terminal based device with a source, gate and drain electrode. Between the source and drain electrode a channel is present that allows the flow of electrons under certain conditions. On top of the channel is an insulating layer called a dielectric present which acts as an insulator between the gate and the components below the gate.

FETs can be classified into two categories: Enhancing-mode and depletion-mode devices. When in enhancing-mode the transistor is in the low conductance ('off') state if no gate potential is applied and when applying a voltage to the gate, the conductance between the source and drain is lowered and the transistor is turned to the 'on' state. When the transistor is in the depletion-mode, the opposite effect takes place and the transistor is with no gate potential applied in the high conductance, or low resistance, ('on') state. Although FETs posses the ability to operate as a variable resistor (which is the so called linear-mode) and can be used as tuning device, this mode is volatile and dissipates relatively much power, leading to thermal runaway [20].

FETs can be fabricated from both organic as inorganic devices. Although the majority of FETs are fabricated from inorganic materials e.g. CPUs which use MOSFET technology, organic FETs (OFETs) are starting to become increasingly popular becasue they offer the possibility to produce devices on a large area, at low-cost, low temperature processing and onto flexible substrates [21;22].

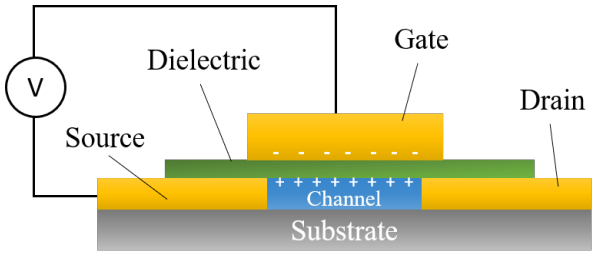


Figure 1.2: *Basic layout of a field effect transistor. By applying a negative voltage to the gate, holes are attracted to the gate creating a electron conducting layer between source and drain and thereby switching the device to the 'on' state.*

1.3.2 Organic ElectroChemical Transistors

A device that better demonstrates tunability is the organic ElectroChemical device (OECT) and is a popular example of a device that uses electrochemical doping to control the current, i.e. the resistance (or conductance, which is its reciprocal,) between a source and drain (figure 1.3a). A typical material that is used in OECTs is the conducting polymer PEDOT:PSS (poly(3,4-ethylenedioxythiophene) doped with PSS (polystyrene sulfonate)) [23]. OECTs based on this polymer work in a so called depletion mode. This means that when no voltage is supplied to the gate electrode, a current can flow from source to drain which is its ON state. If a positive biased voltage is applied to the gate electrode with respect to the source, positive ions (cations), present in the electrolyte, are injected into the PEDOT:PSS channel causing the negatively charged poly-anion backbone, which are available in the PEDOT:PSS, to be compensated resulting in a neutrally charged material and less conductivity. By controlling the voltage applied to the gate, the conductance between the source and drain can be controlled.

The advantage of using OECTs is that doping changes can occur through the entire volume as opposed to a thin interfacial layer between the electrolyte and channel as is the case with FETs[24;25;26]. This is due to the fact that the cations from the electrolyte can penetrate the active layer during the time a gate voltage is applied. This gives OECTs their very high transconductance for low gate voltages which is defined as the derivative of the channel current with respect to the gate voltage $g_m = \delta I_d / \delta V_g$[25;26]. It describes how sensitive a FET or OECT is to a certain applied gate voltage. Because of this high transconductance, OECTs are studied in a wide variety of applications like biological sensors, printed circuits[27] and neuromorphic devices[28;29].

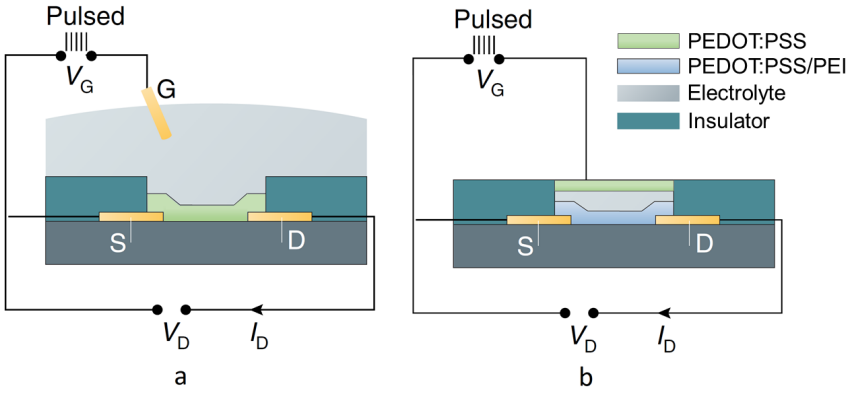


Figure 1.3: *a: A typical OECT structure with gate, source and drain. By changing the voltage on the gate, the conductivity between source and drain is modified and therefore a variable current flows. b: A modified OECT structure. With the addition of a second PEDOT:PSS doped with PEI a non-volatile OECT is created. credits: reproduced from reference*[5].

Upon applying a positive voltage to the gate, cations from the electrolyte[24] are forced into the channel and thereby dedope the PEDOT:PSS resulting in an increased resistance of the PEDOT:PSS between source and drain switching the device to the 'off' state. When switching the gate voltage to zero volts, the cations retreat into the electrolyte and the resistance resets to its initial value hence demonstrating the volatile nature of the device. The channel can be made from either organic[5;26;22;30] or inorganic materials[31] but the majority of ECTs use an organic channel as it allows for tunable electronic properties[26] in contrast to inorganic devices. OECTs can operate both in accumulation-mode or depletion-mode but most of the published work use devices that operate in depletion mode[24]. A commonly used organic material that works in depletion mode is PEDOT (poly(3,4-ethylenedioxythiophene)) which is p-type doped by negatively charged sulfonate groups present in PSS (poly(styrenesulfonate)) creating the highly conducting polymer PEDOT:PSS[23] yielding a device which is in the 'on' state if no gate voltage is applied.

1.3.3 Non-volatile switching switching methods

There are a number of different resistance switching mechanisms but the two most common organic resistive switching devices are based on charge trapping or ElectroChemical doping[16]. Charge trapping devices work through the mechanism of storing charge on nanoparticles that act as nanoscale capacitors which are embedded into an organic semiconductor[5]. The conductivity can be altered by charging or discharging the particles which causes an electrostatic force to repel or attract mobile holes in the semiconductor. Another method for resistance switching is electrochemical doping which uses the injection of ions, that are present in an electrolyte, into a semiconducting layer to control the drain current[16]. Figure 1.3a illustrates such an OECT device. They on the other hand, use an electrolyte that acts as an ion conducting and electron blocking layer between source and gate instead of a dielectric. When applying a voltage to the gate electrode, ions will be attracted or repelled from, or to, the gate[24] and migrate through the electrolyte into, or out off, the channel. Although their operation principle is similar to that of FETs their main identifying characteristic relies on ion penetration rather then an electric field effect and their main operation mechanism is therefore fundamentally different from OFETs[30].

1.3.4 Electrochemical neuromorphic organic devices

Although the OECT illustrated in figure 1.3a displays excelent tunability, it has a memory effect which is volatile, that is when the gate voltage is set to zero and the source and gate are disconnected, the doping state of the material changes back to its original state and its memory is lost. To create a device that satisfies both prerequisites, i.e tunable and can retain its memory (non-volatile), the device in figure 1.3a is slightly modified with the addition of an extra polymer, consisting of PEDOT:PSS partially reduced with PEI (poly(ethylenimine)) as illustrated in figure 1.3b. When applying a positive voltage to the gate electrode, the conductivity is increased and when applying a negatively biased voltage to the gate, the conductivity is reduced. This new neuromorphic device, called ENODe, with non-volatile characteristics was first demonstrated by van de Burgt and colleagues in 2017. He also demonstrated with a simulation, based on experimentally measured properties of ENODe, a neural network that could classify a data set of hand-written digits. Tuning of ENODe was achieved in an analogue fashion[32] and >500 distinct, non-volatile conductance states with extremely low noise levels could be demonstrated[29]. Other advantages of organic neuromorphic devices include: i) simpler fabrication techniques can be used that are accessible to smaller-scale laboratories and their manufacturability over large areas[26], ii) their bio-compatibility to implement them in biological systems[33], iii) they can be made flexible which enables new application possibilities like thin-film heaters[34], and iv) they operate with little power which makes them suitable for standalone battery-powered devices.

The working principle of ENODes is illustrated in figure 1.4. Situation a,c,e indicate when the device is disconnected from the external circuit at various resistance states illustrating the non-volatile behavior and the correlation between the doping state of the PEDOT:PSS and corresponding resistance between situation a,b,c. When a positive voltage is applied to the gate with respect to the source as shown in figure 1.4b, an electron deficiency is created and cations, or protons, are forced out of the presynaptic electrode to maintain electron neutrality[35] and are injected into the postsynaptic electrode increasing the resistance between source and drain. When applying a negative voltage, as shown in figure 1.4d, electrons are injected into, or holes are removed from, the presynaptic electrode and cations are attracted towards it from the postsynaptic electrode through the electrolyte to balance the discrepancy between charges resulting in a reduced resistance in the postsynaptic electrode. Essentially, ENODe acts as a concentration battery which can be charged and discharged. For this reason a switch between source and drain is necessary in order to maintain its non-volatility since it prevents the 'charged battery' from draining. Alternatively, a high resistance resistor can be used to slow down the draining process without the need for an extra physical switch and keeping the circuit closed as van de Burgt and colleagues used[29].

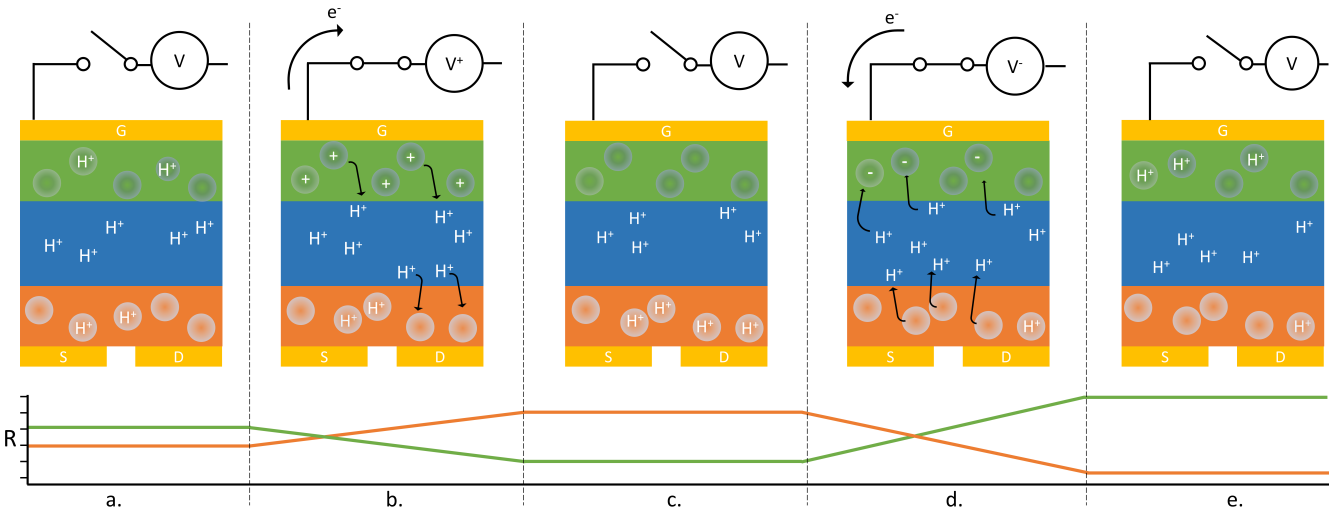


Figure 1.4: *Illustration sequence of the working principle of an ENODe shown in the top part of the figure. Below is the resistance trend illustrated for both the presynaptic electrode (green) and the postsynaptic electrode (orange) as reference.*

1.4 Light sensitive devices

To be able to optically modulate the conductance of ENODe, a dedicated photo-sensitive cell can be electrically connected to ENODe to modify its conductivity. These photovoltaic (PV) cells, better known as solar cells, exhibit the photovoltaic effect which convert the energy of light into electricity by creating electron-hole pairs and separating them to create a potential. An advantage of this method is that both ENODe and solar cell can be optimised independently of each other to demonstrate the desired characteristics offering flexibility during design. Although the first photovoltaic cell was already built in 1839 which demonstrated the photovoltaic effect, it took more then 100 years before the first practical solar cell was developed and patented by Chapin et al. in 1957[36].

Solar cells can be divided into three generations, first, second and third[37;38]. Solar cells of the first generation are the oldest and most popular type with 86% of the solar market in 2012[39]. The material used for these solar cells mainly consist of two or more layers of silicon that are p- and n-doped respectively. When photons hit the solar cell, an electron-hole pair is freed from the n-type and p-type silicon and when send through a conductor they recombine and produce an electric current[40]. Although their production costs are relatively high, they have relative high power efficiencies between 12 and 18%[38]. They are produced from silicon wafers with either a monocrystalline- or polycrystalline structure of which polycrystalline cells dominate the market for their cheaper production process[38]. Second generation solar cells are made using thin-film technology to fabricate solar cells. They are made from amorphous silicone (a-Si), Cadmium Telluride (CdTe) or copper indium gallium di-selenide (CIGS)[37]. Depending on the material used, their efficiency ranges between 4% for a-Si cells and 12% for CIGS cells. Although the efficiency of a-Si cells is low, they can be manufactured at a low processing temperature, deposited onto a wide range of substrates ranging from glass to (flexible) polymers, are very cheap to produce and widely used in for example solar-powered calculators[37]. Third generation solar cells are dedicated to new emerging technologies mostly based on thin-film technologies that are still in the research phase. These include, perovskites, nano crystal based solar cells, polymer-based solar cells, dye-sensitised solar cells and concentrated solar cells. Organic solar cells are of particular interest because they are made using polymers which makes them flexible and are expected to be relatively cheap to manufacture but this is still in development.

1.5 Illumination devices

To illuminate the solar cells, various light emitting devices can be utilized. However, as Light Emitting Diodes (LEDs) offer many advantages over other light sources, only this group of illumination devices are studied in depth. Some of the advantages of LEDs are that they are widely available, cheap to manufacture, they have a high efficiency and reliability, and come in countless shapes and specifications allowing for easy miniaturisation. They also posses diode characteristics which will be used to our advantage as will be explained in section 2.2. The energy-to-light conversion that LEDs utilise is inversely analogous to the light-to-energy conversion in solar cells as they use the same p-n junction technology[41]. Fabrication of LEDs is thus similar to solar cells. In order to maximize the available photon energy, white light can be used as it covers most of the electromagnetic spectrum in which solar cells are sensitive[40] thus maximizing power output.

1.6 Sneak currents in crossbar arrays

Because ENODe offers several advantages including low power consumption and low noise characteristics, these devices make ideal candidates for ANNs applications and implementation in a crossbar array as illustrated in figure 1.5.

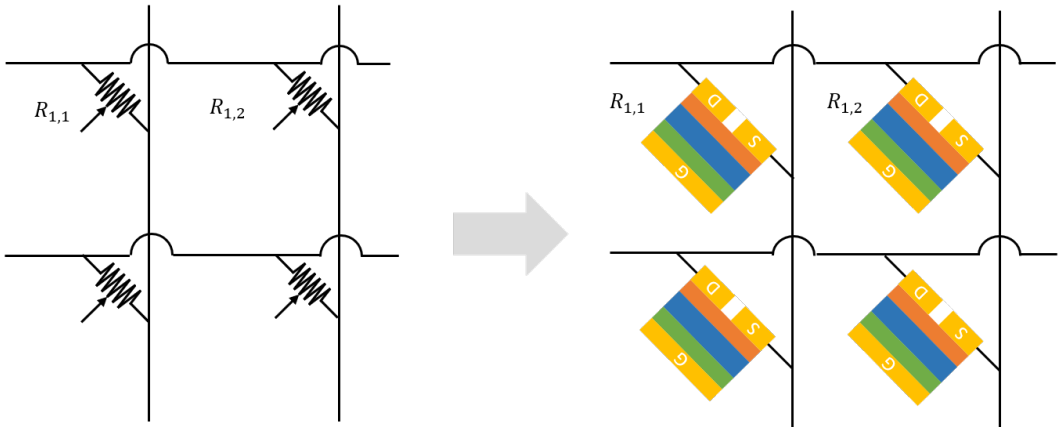


Figure 1.5: *Implementing ENODe in a crossbar array as a tunable resistive non-volatile memory element.*

However when arranging them in a crossbar array of connected ENODes, undesired effects during read and write operations, called "sneak currents", are introduced (figure 1.6). Sneak currents are unintended paths current will flow through parallel to the intended path [42] leading to a disturbed readout or programming of an individual cell. Most crossbar arrays use memristor-based components to mimic synaptic activity and several studies have recognised this issue and present numerous solutions for these arrays for either reading or writing issues. ANNs need training data and some sort of feedback system to update the weights in order for the network to learn which is why both reading and writing to a cell is necessary. Accurate reading without any additional components can be achieved when using the "multistage" reading algorithm but this is a slow and inefficient process of 1) measuring the cell, 2) switch the cell 'off' and measure again, 3) switch the cell 'on' and measure it, 4) compare measurements and 5) return memory to original state [43]. Another reading method that involves the use of an additional component is the unfolded architecture that uses separate CMOS multiplexors for each column to avoid sneak paths [44]. A disadvantage of this architecture however is that it drastically reduces the cell density as many extra wires are required [44]. Furthermore, there is the diode gating architect which incorporates a diode device in series with every memory cell without the need for additional wires and is therefore also called the 1D1M (1 diode 1 memristor) architecture. With the use of an extra diode, the read operation is made possible but writing of memristor-based crossbar arrays still requires the use of additional external circuitry to switch between a read and write operation [44].

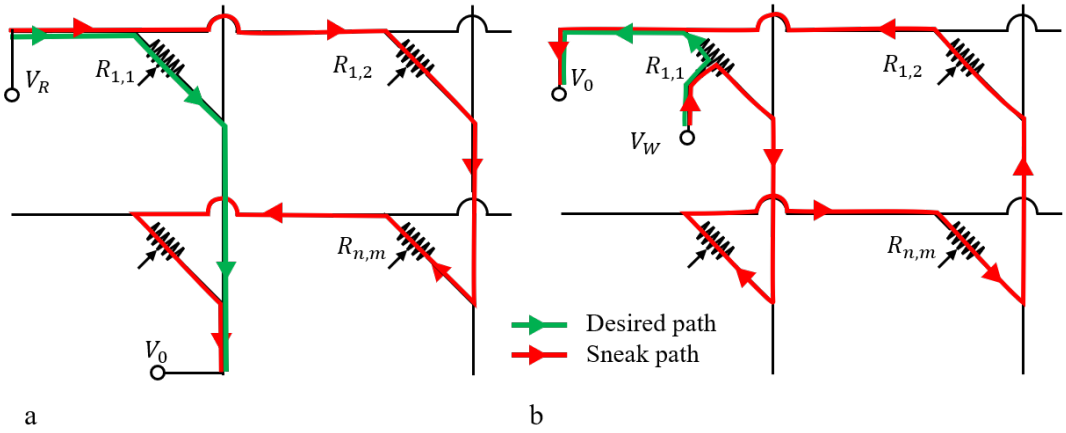


Figure 1.6: *a) current sneak path during a read operation. b) current sneak path during a write operation.*

1.7 Scope of this thesis

Tuning of ENODes is currently done by means of a physical electrode that is connected to the gate of the ENODe to alter the conductance between the source and drain. For a small number of ENODes this layout is manageable but when the number of ENODes in a network is increased, sneak currents are introduced and wire management becomes an issue which limits the scalability of the network. To address this issue and enable the development towards larger ENODe arrays, this project focuses on i) the development of a method which uses light that facilitates the tuning of ENODes and ii) the developement of a novel network layout that eliminates sneak currents for both read and write operations in a crossbar array. The use of light specifically as a tuning method carries several advantages such as i) the biological relevance of light on organic processes in nature and ii) its ability to serve as a wireless method for tuning ENODes in large networks as mentioned above.

In addition to the development of this method and to facilitate the production of larger networks of ENODes, a hybrid device which integrates both the photo-detector and the ENODe onto a single PCB layout is designed and produced which can be used in future research to study ENODe in a network configuration.

The goal of this project is to develop a light-tunable ENODe device and demonstrate the tuning of ENODes using light pulses. Additionally, a hybrid device that incorporates a photo-detector combined with an ENODe into a single device is developed and demonstrated. This hybrid device should be extendable to at least a 2x2 array of connected hybrid devices.

Chapter 2

Development of a light-tunable ENODe device

Tuning of ENODes is generally done by means of a physical wire or electrode. However this presents some challenges when scaling to larger networks where wiring schemes become increasingly more complex. By accompanying each ENODe with a dedicated photo detector that, when illuminated by a light source, can alter the conductance of the ENODe and thereby change the "weight" of the connection, the tuning of ENODes can be achieved in a wireless fashion and simplify the wiring scheme. First the manufacturing of ENODe is explained to continue with an elaborate overview of the prototype setup.

2.1 Manufacturing ENODe

ENODe is manufactured by spin-coating PEDOT:PSS onto a 1x1 inch glass ITO (Indium Tin Oxide) slide, which is a transparent conducting oxide and is illustrated by the four gold rectangles in figure 2.1a. After this, the presynaptic and postsynaptic electrode are created by ablating the non-blue area with a laser leaving two distinct blue rectangles. Then, a well, shown in gray, is attached onto the ITO slide to contain the ion-conducting/electron blocking liquid electrolyte creating ENODe. Full details regarding the manufacturing of ENODe can be found in appendix B.

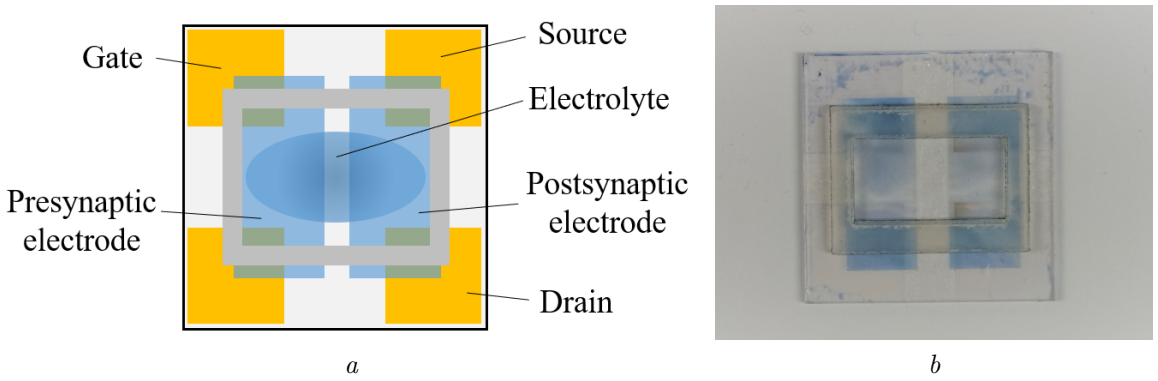


Figure 2.1: *Left, Overview of the produced ENODe showing an ITO slide with four quadrants and PEDOT:PSS spin-coated on top of that with a polymer well that contains the electrolyte. Right, a photograph of the fabricated ENODe device*

2.2 Prototype setup

Figure 2.2 illustrates the wiring schematic of the designed circuit consisting of two individual circuits. On the left side, a light generating circuit with two LEDs is illustrated and on the right side an ENODe circuit is shown. Powering the LEDs and measuring the resistance of ENODe is done using a Keithley 2602A SourceMeter which facilitates two individual channels, of which one is used to control the LEDs and the other is used for measuring conductance of ENODe. Data collection is done using a PC running MATLAB 2017a that is connected via an Ethernet cable to the Keithley and a custom built library (developed during this project) that is able to send commands and receive data at approximately 35 Hz using the TCP/IP protocol, is developed. More information on the achieved sampling frequency and the developed scripts used during data collection can be found in appendix C

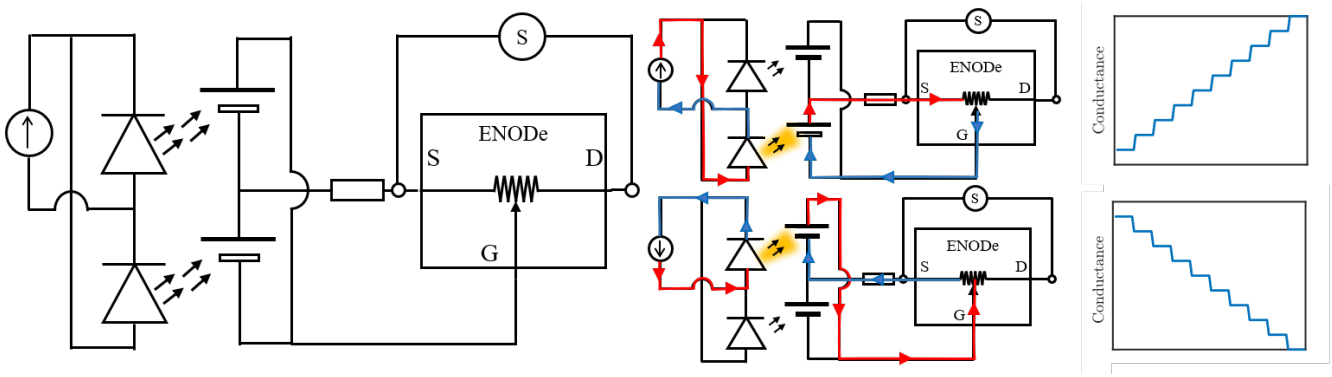


Figure 2.2: *Electronic circuit layout for tuning the ENODe using two LEDs that individually illuminate two separate solar cells. Resistance, R, of the channel is measured between source and drain. On the right is the current flow illustrated for tuning ENODe in both directions.*

The LED circuit consists of two LED symbols in a parallel configuration with each LED symbol representing four individual white LEDs which are connected in series as illustrated in figure A.2. Both LED symbols are oriented in opposite direction to purposely break the parallel configuration up into two individual loops since LEDs behave similarly to a diode and only allow the flow of current in one direction. This method allows the on/off switching of a single LED depending on if a negative or positive current is supplied by the SourceMeter. This mechanism has the advantage that no additional switch is required to turn the LEDs on and off and is visualized on the right side in figure 2.2 for both a positive and negative voltage. In the top figure, the top LED is illuminating the top solar cell resulting in a counter clock wise current through the ENODe and on the bottom the reverse process is visible. Actuation of the LED circuit is achieved using a Keithley 2602A SourceMeter with current control. Using current control in combination with LEDs linked in series is important since this imposes an identical current through each LED resulting in a similar brightness for all LEDs. Additionally, manufacturing tolerances and operating temperatures result in non-identical voltage drops across similar LEDs which leads to thermal runaway [45] that damages the LEDs, making LEDs connected in parallel without additional current-limiting components unreliable.

The ENODe circuit is built up out of two solar cells connected in parallel along with a 1M Ohm resistor in series and an ENODe device. Initially, an organic solar cell, that is currently being developed by PhD candidate Tom van der Pol at Eindhoven University of Technology, was initiated for this project because both ENODe and this solar cell are spin-coated during manufacturing which would simplify the production of a hybrid device. However, due to its inability to survive outside an inert atmosphere for extended periods of time, a different kind of solar cell was proposed. The solar cells that are used in this setup are thin film solar cells from a solar powered calculator as they are widely available, cheap, reliable and can be deposited onto flexible substrates as discussed in section 1.4. The configuration of the solar cells is chosen in such a way that is similar to that of the LEDs because they posses diode characteristics too and can therefore produce a positive or negative potential resulting in changing the resistance of the ENODe in both directions as illustrated in figure2.2. Additionally, a 1M Ohm resistor is included into the circuit since it acts as a load on the charged ENODe and prevents it from draining too quickly. This is an alternative to a switch as discussed in section 1.3.4 because it simplifies the wiring scheme and eliminates the need for an extra switch circuit while still demonstrating the functionality of the device. In series with the resistor is the ENODe connected in the loop. The ENODe in figure 2.2 is a three terminal based device consisting of a

source (S), drain (D), and gate (G). The conductivity of the ENODe is measured between source and drain with a Keithley SourceMeter. Detailed information of the fabricated ENODe can be found in appendix B

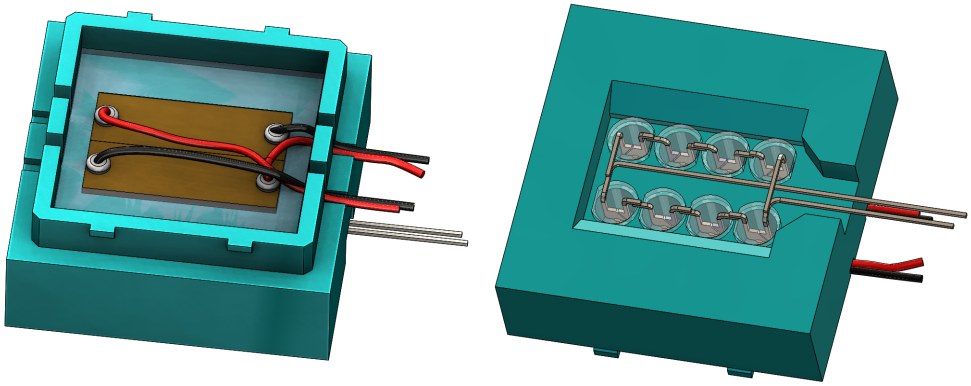


Figure 2.3: *3d CAD drawing of the lightproof box. In the left figure, the top view is shown without the lid mounted and two solar cells colored in gray are present. On the right is the bottom view of the box visible with eight LEDs soldered together.*

To accurately measure the influence of the light of the LEDs onto the solar cells, a lightproof box that shields the solar cells from any disturbing environmental light is designed and fabricated as shown in figure 2.3. By only allowing light from the LEDs to hit the solar cells accurate measurements can be carried out. The solar cells used in this setup each consist of 4 segments that are connected in series that need to be individually lid during actuation because they act as a resistor when no light hits the segment. Therefore a total of eight LEDs is required to fully illuminate every segment of the two solar cells as shown on the right illustration of figure 2.3.

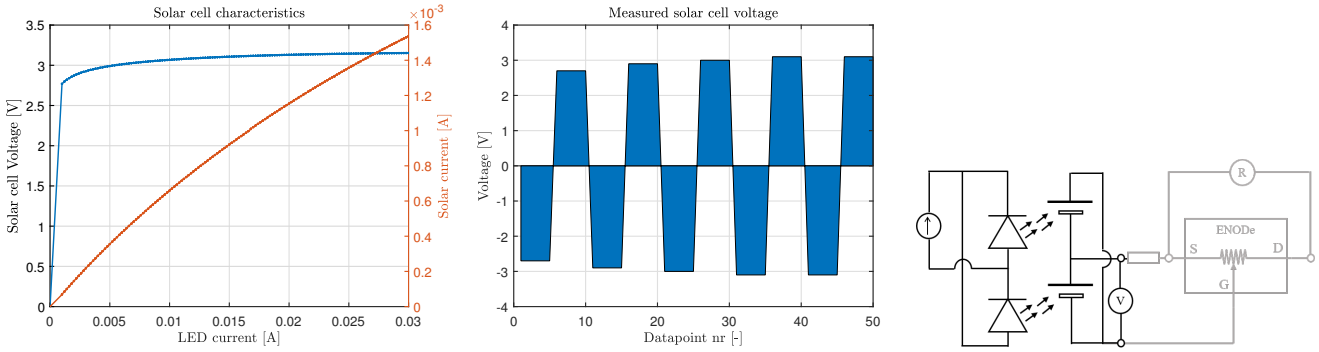
Chapter 3

Experimental methods and results

This chapter discusses the experimental results of the developed device as illustrated in section 2.2. First, the individual parts and the wiring scheme are validated to proceed with a full characterisation of the overall setup demonstrating the optical tuning capabilities that can be utilised to tune ENODe bidirectionally for neuromorphic computation.

3.1 Validation of solar array and wiring scheme

Before fabricating the designed setup as shown in figure 2.2, the individual solar cells are tested under LED illumination and their characteristics are verified using the wiring scheme in figure 3.1c. Utilizing the property that LED brightness is proportional to the supplied LED current [46;47], a current sweep can be used to modify the illumination level of the solar cell. Figure 3.1a illustrates the individual characteristics associated with the solar cell illustrating in blue the generated voltage by the solar cell and in orange the corresponding generated current for increasing LED currents. The current shows a linear relationship with the supplied LED current confirming that the solar cell is essentially a current source [48] while the voltage remains fairly constant over the supplied LED current. This result shows that a LED current between 5 mA and 30 mA would be a suitable range to produce a stable 3-3.1 Volts at the solar cell which is sufficient for tuning ENODe as illustrated in appendix A.1.



a b c

Figure 3.1: *a) Shows the measured characteristics of the elected thin-film solar cell. A clear linear relation between LED current and solar cell current is visible. b) Illustrates when two solar cells are set in parallel and with swapped polarity and wired together. Depending on which solar cell is illuminated either a positive or negative voltage is measured. c) Illustrates the wiring scheme used during validation measurement of a and b.*

As elaborated in section 1.3.4, the ability to bidirectionally tune ENODe depends on the polarity of the applied gate voltage with respect to the source. Therefore it is essential that the designed circuit is capable of generating both positive and negative voltages and currents in order to be able to lower or increase the conductivity of ENODe. To achieve this functionality, connecting the solar cells as depicted in figure 2.2 and illuminating one or the other solar cell, the diode properties solar cells possess when no illumination takes place [40] is exploited and both a positive

and negative voltage, as illustrated in figure 2.2, can be generated when measuring between gate and source as illustrated in figure 3.1b by the shaded area. The physics that makes this functionality possible is that a solar cells possess diode characteristics when in the dark which is a distinctive property of photovoltaic devices as an asymmetrical junction is required to achieve charge separation[40].

3.2 Validation of the overall setup

After characterisation of the individual components the complete setup is verified. To demonstrate the synaptic functionality of the developed device, which is an essential building block for neuromorphic computing and was first demonstrated by van de Burgt and colleagues[29], light pulses from the LEDs are used to to show the non-volatile tuning abilities of the ENODe. By supplying a positive or negative current to the lighting circuit, either one or the other LED illuminates its neighbouring solar cell producing a positive or negative voltage to the gate of ENODe resulting in a change of conductivity. Figure 3.2a illustrates the process of changing the conductance of ENODe using individual light pulses displaying 30 distinct non-volatile (see inset) conduction states. During illumination of the solar cell, the conductance of ENODe changes as illustrated by the diagonal line in the inset while the horizontal lines illustrate the intermediate states when the solar cell is not illuminated.

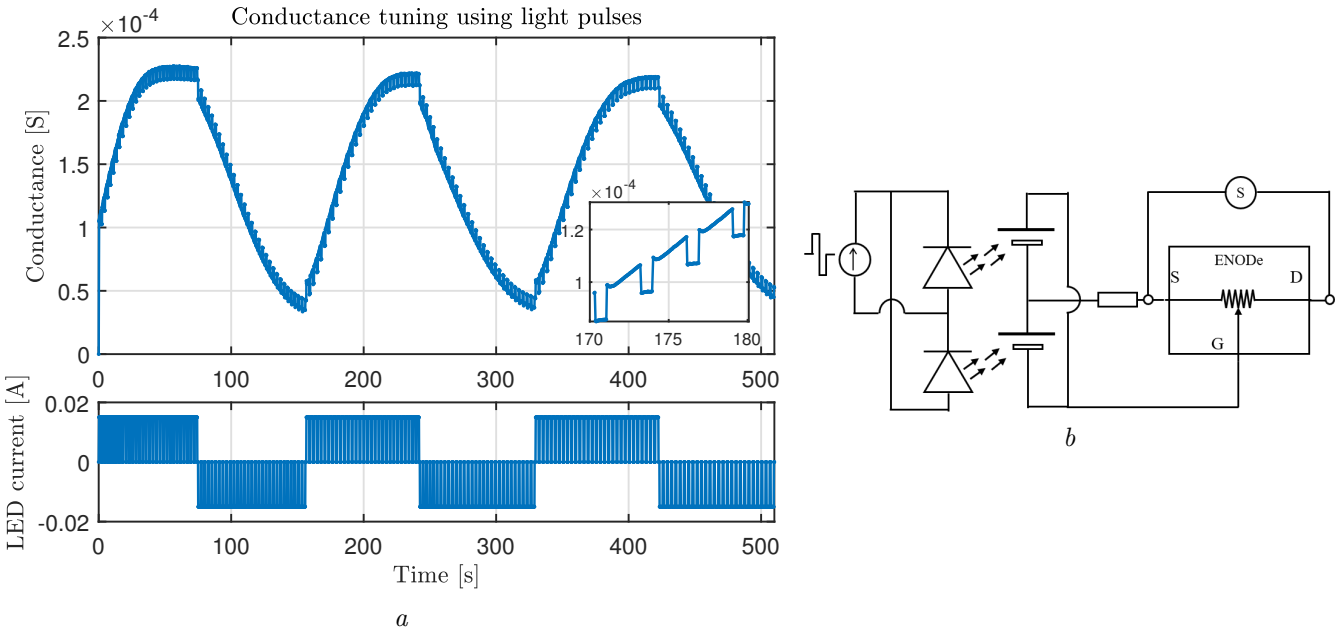


Figure 3.2: *a) Conductance tuning of ENODe using light pulses. The inset shows the available distinct non-volatile states of ENODe when no current is supplied to one of the LEDs. Depending on the direction of the current either one or the other LED illuminates light. b) Shows the used wiring scheme while conducting the experiment.*

Conductance modulation of ENODe is achieved by either varying the voltage between source and gate or by adjusting tuning time[29]. Since the voltage generated by the solar cells is almost independent of the current supplied to the LEDs as shown in figure 3.1a, conductance of ENODe can be modulated by varying the illumination time of the solar cells. Figure 3.3a illustrates how tuning time is related to the tuning rate of ENODe and figure 3.3b shows the circuit used during measurement. It illustrates that there is a linear relation between tuning time and conductance change and that tuning for longer tuning times reduces the deviation between measurements. In addition to that, when using tuning times shorter than 0.3 seconds, conductance change is minor to none. A possible explanation for this phenomenon is the counter-electromotive force that is induced by the capacitive nature of ENODe which is causing this reverse tuning behavior.

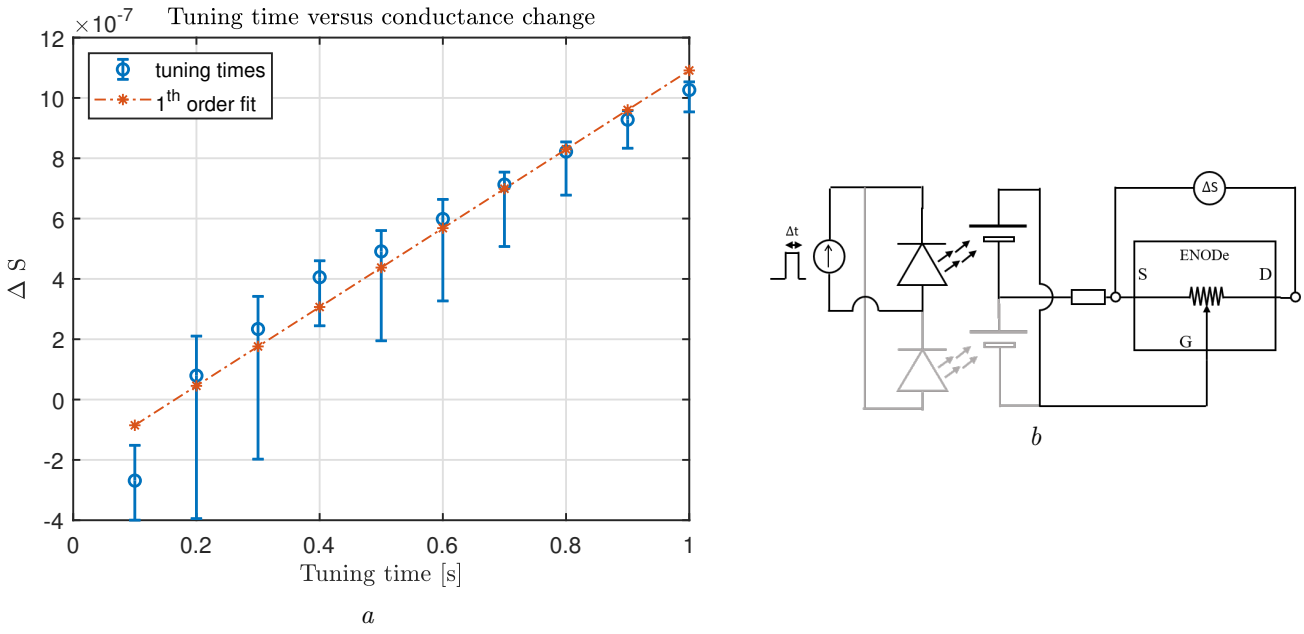


Figure 3.3: *a) Tuning time versus conductance change. A first order fit emphasises the linear relationship. b) The circuit used during measurement with varying tuning time pulse width.*

To demonstrate ENODes' capability of being used as a synaptic weight in an artificial neural network, six reproducible discrete states are defined into the postsynaptic electrode of ENODe as illustrated in figure 3.4). By using light pulses of 1 second at 15 mA these states can be reproducibly reached and showing the bidirectional tuning capabilities of ENODe.

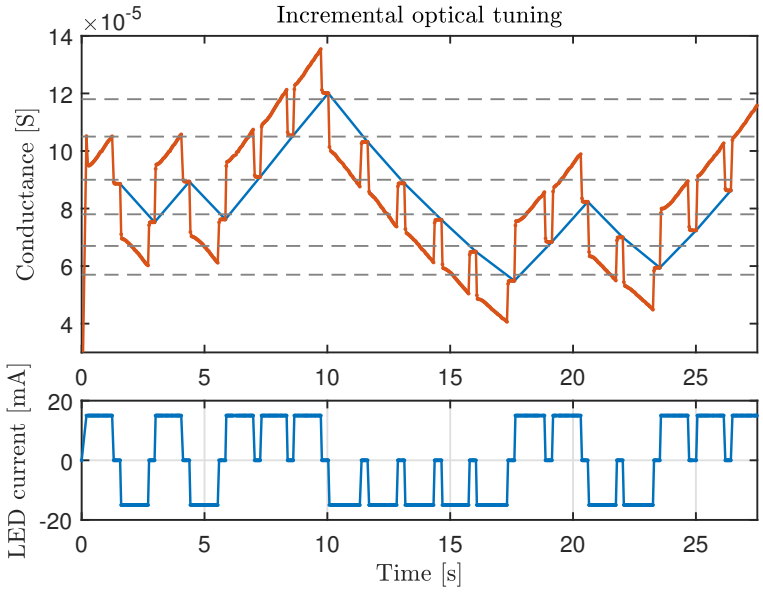


Figure 3.4: *Incremental tuning of ENODe to distinct states using constant time pulses. Demonstrating reproducible switching between 6 different states.*

Chapter 4

Design of a hybrid device and array configuration

After testing and validation of the developed light-tunable ENODe setup, a demonstrator device is developed and manufactured. This hybrid device incorporates two solar cells, an ENODe and the necessary circuitry onto a single apparatus. Doing so yields several advantages including easy up-scaling to a mass manufacturable process, portability and reliability improvements. Additionally, during the design phase of this device, a modular interface is developed that allows the creation of a two-dimensional array of connected light-tunable ENODes in a $m \times n$ configuration using source- and drain lines.

4.1 Electric layout

To scale from a single ENODe to a two-dimensional network of connected ENODes, the wiring scheme illustrated in figure 2.2 needs to be slightly modified. A solution can be found in the utilisation of a crossbar array as discussed in section 1.2. An advantage of this crossbar array is that it is a scalable and modular design approach and allows for vector matrix multiplications which forms the basis for deep learning algorithms[5;17]. Each individual device is connected via a source line and a drain line represented by the horizontal and vertical lines in figure 4.1 respectively creating a system of m inputs and n outputs.

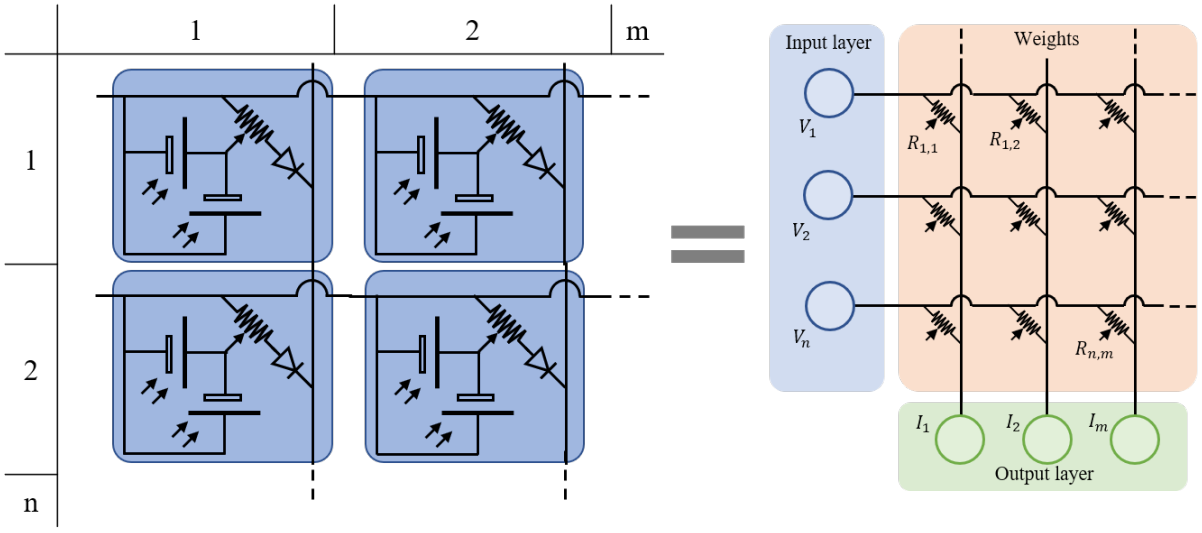


Figure 4.1: *Wiring scheme of a two-dimensional scalable modular crossbar array of ENODes in a $m \times n$ configuration.*

Figure 4.1 shows the designed wiring scheme which combines the crossbar array from figure 1.1 with the ENODe tuning layout from figure 2.2. From this figure it is clear that with the addition of a crossbar array and some minor

changes to the individual ENODe device, a modular and scalable array of connected ENODes can be created. Although there are multiple ways of gaining access to individual ENODes as presented in section 1.6, access to a single ENODe for accurate reading or low-power writing in an array configuration is handled by introducing a discrete non-linear access device in the form of a diode in series with the memory element at each crossbar. During this project, a diode is used since introducing non-linearities in PEDOT:PSS has not yet been demonstrated while a diode in series with the ENODe provides the same functionality and are widely available. A single diode at each node protects the array from sneak currents as shown in figure 4.2 that develop when ENODe is configured in a crossbar array preventing unintended tuning of nearby ENODe elements for both read and write operations, which is to our knowledge not yet demonstrated in this capacity.

During a read operation, as illustrated in figure 4.2a, current will as intended flow from V_R to V_0 while the diode at location 2,2 prevents the flow of current through a sneak path leading to a correct read out of device 1,1. During a write operation of device 1,1, shown in figure 4.2b, current will flow through the desired path highlighted in green and an unintended current shown in red is obstructed by the diode at location 2,1, resulting in only intentional tuning of device 1,1 and blocking any undesired programming of neighbouring elements.

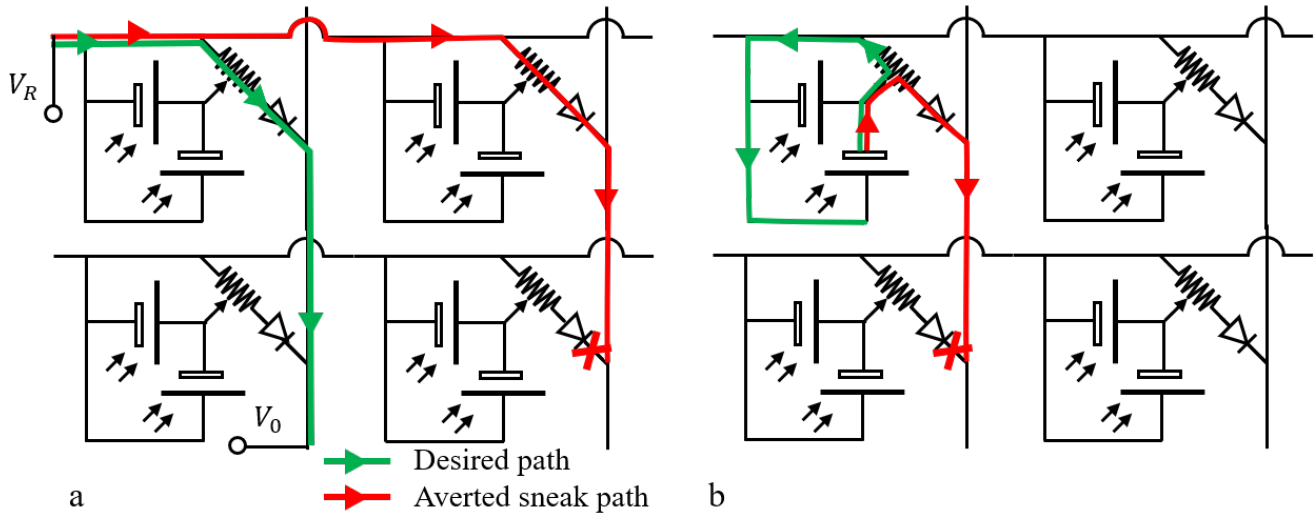
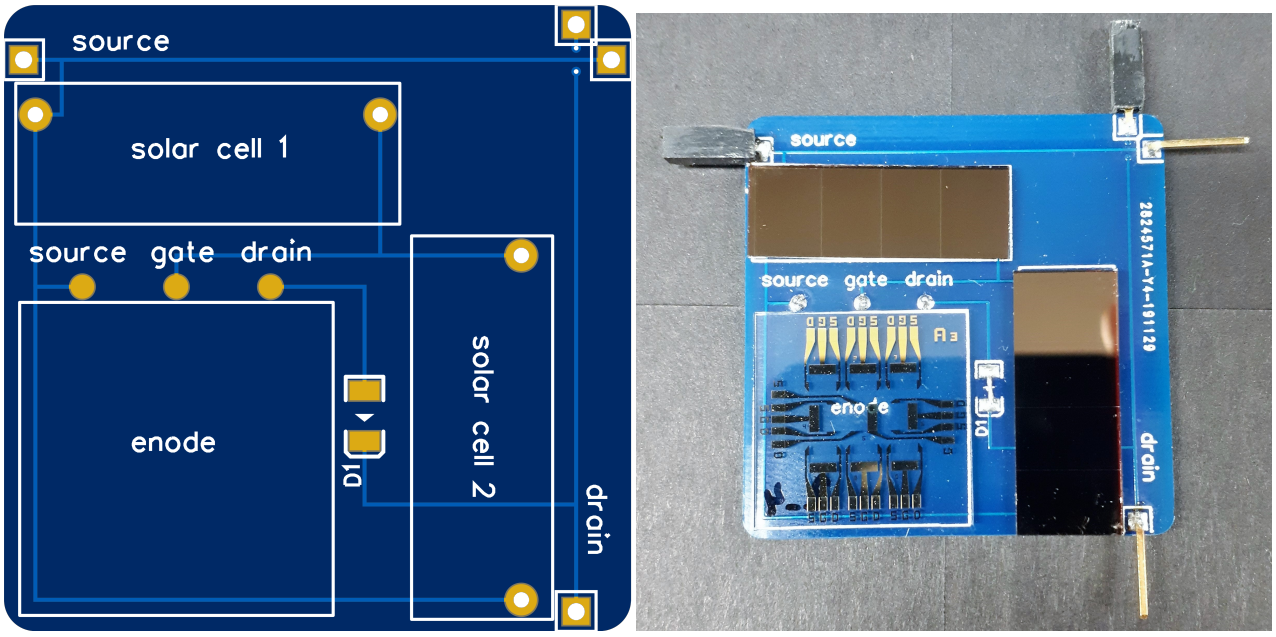


Figure 4.2: *a) During read operation the sneak current is obstructed by the diode at location 2,2 b) During write operation the sneak current is obstructed by the diode at location 2,1.*

4.2 PCB design

From the designed wiring scheme, a printed circuit board (PCB) is designed and fabricated. Figure 4.3a shows the final layout of the designed PCB and figure 4.3b shows the manufactured board together with the soldered male- and female headers to provide the interconnectability across different boards and an ENODe device attached to it. The typical layout of a PCB consists of several two-dimensional layers which are stacked onto each other to form a functional PCB. The developed PCB has 5 different layers each with their own functionality and are designed individually. Two routing layers are used of which the top routing layer contains most of the circuitry which is illustrated by the light blue lines in figure 4.3a. The bottom routing layer is solely used to accommodate for signal crossing of the source signal and the drain signal as shown by the half-circle hopping in figure 4.1 by using two through hole vias. Additionally, a solder mask layer, which is a negative layer, in combination with a solder paste layer is applied to both sides of the PCB to protect it from debris to prevent short circuiting which is the blue coating illustrated in figure 4.3b. The solder paste layer is applied to areas that require soldering of external components and is colored in gold in figure 4.3a. Finally, a silkscreen layer is applied to the top of the PCB which contains all the necessary information about the various connections on the board and only serves an informative purpose which is shown in white in figure 4.3a and b.



a *b*

Figure 4.3: *Layout of the designed printed circuit board incorporating two solar cells for tuning up and down and an ENODe onto a single hybrid device.* ***a****. Shows the design of the PCB with the trace layout visible.* ***b*** *Shows the manufactured hybrid device with two solar cell present (in brown) and an ENODe array of which one ENODe is connected to the PCB.*

Chapter 5

Conclusions and recommendations

5.1 Conclusions

In this work, the optical tunability of ENODe devices using light pulses is demonstrated. It has been found that when accompanying ENODe with a set of solar cells both a positive and negative potential can be generated allowing a bidirectional conductivity tuning of ENODe. This is accomplished by wiring two solar cells in parallel in opposite direction and exploiting the diode characteristics solar cells possess to create a circuit that when one or the other solar cell is illuminated by a LED, either a positive or negative potential is generated between source and gate of ENODe. This result is achieved with excellent tuning performance while maintaining the non-volatile characteristics that ENODe possess.

Additionally, a PCB (Printed Circuit Board) is designed and fabricated that incorporates two solar cells and ENODe into a single hybrid device. This device utilizes a crossbar array configuration which facilitates the extension to larger neuromorphic arrays and incorporates a diode in series with every tuning device. This designed circuitry in combination with the diode theoretically eliminates the sneak current problem that crossbar arrays suffer from in both read and write operations.

Finally, a software library is written from scratch in MATLAB that allows data transmission and acquisition to and from the SourceMeter allowing the extension to larger automated algorithms and act as an enabler for conducting future experiments. The designed functions are subdivided into three categories being ”Set”, ”Get” and connection commands, representing either the ability to set a current or voltage across ENODe, read the current or voltage value or initialize and close the connection between PC and SourceMeter.

5.2 Recommendations and future work

Based on the achieved results and gained knowledge during this project a number of recommendations can be proposed. This section is dedicated to provide a number of suggestions on how the current thesis can form the foundation of future work.

A first proposition for future research continuing on the results of this thesis would be the validation of the claim that with the presented circuitry sneak currents would be eliminated. Up to 9 PCB devices are manufactured which allows a maximum of 3x3 array configuration to be tested.

A second proposition to improve the functionality of ENODe is related to the draining effect ENODe suffers from when no mechanical switch between source and gate is used to to prevent ENODe from draining after tuning to prevent electrons reducing the accumulated potential in the presynaptic electrode and postsynaptic electrode. Currently, a 1M Ohm resistor is used to diminish the draining effect as a mechanical switch would require additional circuitry and actuation devices. A solution could be the use of 2 diodes with a breakdown voltage of 3V and preferably <100pA reverse current leakage arranged in a back-to-back configuration as substitute for the resistor. In this way when the solar cell is illuminated the generated voltage will exceed the breakdown voltage of the diodes and start to tune ENODe but when in the dark the back-to-back configuration will prevent the draining of ENODe.

Another proposition would be related to the scaling of the device. Miniaturizing the proposed setup in future research challenges relating to the scalability of the illumination of individual solar cells could be problematic due to light leakage to adjacent solar cells. A solution for this problem would the use of an optical fibre to transport the tuning light to a specific location on the board using total internal reflection.

In an effort to optimize device geometry and actuation conditions, a better understanding of the current-voltage characteristics involved for tuning ENODe is preferred by means of a dynamical model. Bernards and colleagues already demonstrated a model for describing OECT behaviour which could be extended to represent ENODe dynamics.

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Appendices

Appendix A

Additional illustrations and electric diagrams

This appendix contains images that support, clarify and substantiate the main content of this study but were not included into the predominant text as they serve as 'further reading' material.

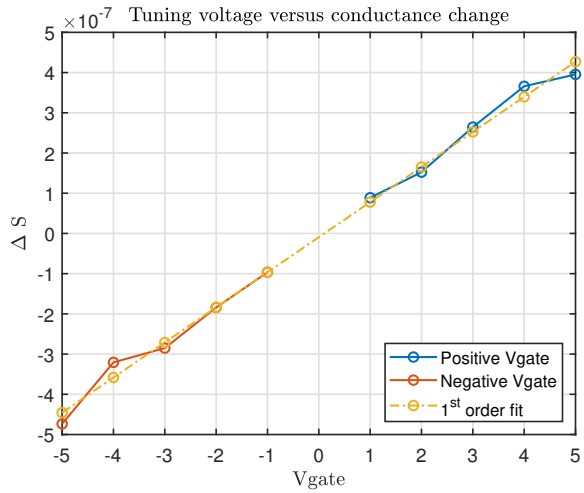


Figure A.1: *Tuning time versus conductance change. A first order fit emphasises the linear relationship/*

A.1 Solar circuit

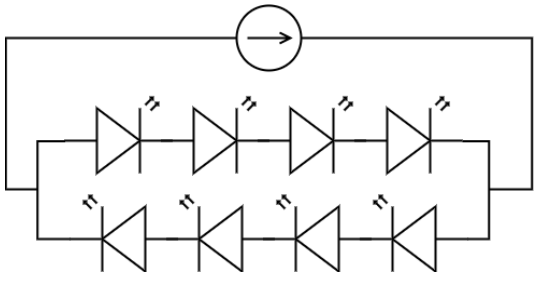


Figure A.2: *Actual LED configuration used during experiments.*

Appendix B

Fabrication of ENODe

Fabrication of ENODe is done using an in-house developed recipe and equipment and is as follows. The whole process for producing 3 ENODes takes around 4-5 hours from start to finish and costs approximately €5,-

1. Cleaning of ITO slide for 10 minutes in a ultrasonic cleaning bath using consecutively acetone, iso-propanol, de-ionised water and N_2 gas.
2. Put the ITO slides for 15 minutes under a ozon treatment to make the surface hydrophilic and enable dropcasting.
3. Mix PEDOT in a 1 to 4.5 volume percent ratio with Etyleneglycol
4. Mix 10 volume percent DEMTA (n-methyl 2,2 diaminodiethylamine) relative to the amount of PEDOT. Important to remember is that when adding the DEMTA the solution starts to gel quickly making the dropcasting process in the next step harder.
5. The solution is then squeezed through a filter and dropcasted onto the ITO slides.
6. Immediately spincoat the produced slides at a 500 RPM acceleration, 1500 RPM constant velocity and decelerate at 500 RPM velocity profile.
7. After that the slides are put onto the hot plate at 90 degrees C for 10 minutes to evaporate the solvents.
8. Finally the slides are partially ablated into a lasercutter machine forming two isolated PEDOT:PSS pads as shown in figure 2.1.

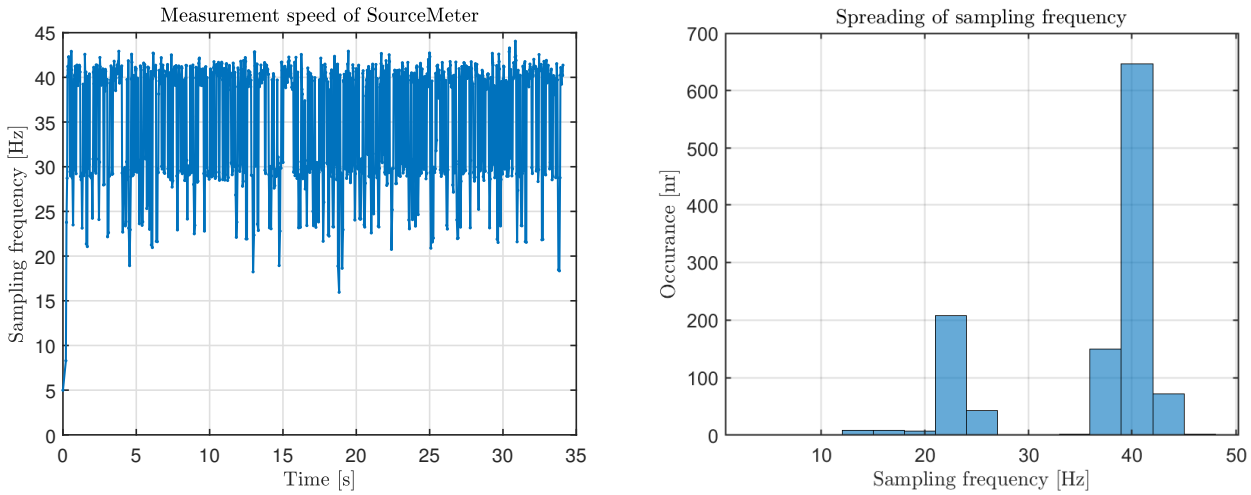
Appendix C

Data acquisition

This appendix presents the developed scripts and the achieved execution speed of commands developed during this project. Additionally it contains a small collection of the written MATLAB code used for data acquisition using the Keithley SourceMeter 2602A. It consists of a initialize and close connection with the instrument, a set command and a get command.

C.1 Performance

The performance of the written code is determined by measuring the time before and after execution of a measurement loop which includes the sending time from PC to the Keithley, execution of the command on the device, the send back time from device to PC and the plotting the newly acquired data point in a graph in MATLAB. On average a sampling frequency of 35 Hz is achieved with lows in the 25 Hz range and highs up to 40 Hz.



a *b*

Figure C.1: *Sampling speed of the SourceMeter. This includes measuring of a data point and sending the acquired data point to the computer to be plotted in real-time. On the left the sampling frequency is plotted over the course of 30 seconds illustrating an approximate sampling frequency of 35 Hz. On the right a histogram of the same data is plotted to illustrate the spreading of the values.*

C.2 Scripts

Initialze Keithley

```
%Initializes the Keithley measuring 2602A SYSTEM SourceMeter
%
% dev=initDevice()
% dev: is of type tcpip and is used to send commands to the Keithley
%      use eg. SetVdrain(dev,0.1) to apply 0.1 V to the drain (channel B)
%      and eg. value=GetVdrain(dev) to measure the drain voltage

% important: make sure the address of your network card is not the same as
% specified address. You can change this in the control panel under network
% and sharing options and then change adapter settings
%
% date:          modifications:
% aug-2019       Initial commit by Sjors and Eveline
% aug-2019       Added instrreset command to reset device if it is not properly
   closed previously
% nov-2019       Added a try catch structure to increase userfriendlyness
function dev=initDevice()
    instrreset
    address='192.168.0.2';
    port=5025;
    dev=tcpip(address,port);
    dev.transferdelay='off';                              %speeds up measurement
    dev.Timeout=2;
    try
        fopen(dev);
        fprintf(dev,'%s\n','smua.reset()');
        fprintf(dev,'%s\n','smub.reset()');
        fprintf(dev,'%s\n','smua.source.output = smua.OUTPUT_ON');
        fprintf(dev,'%s\n','smub.source.output = smub.OUTPUT_ON');
        fprintf(dev,'%s\n','smua.contact.speed = smua.CONTACT_FAST');
        fprintf(dev,'%s\n','smub.contact.speed = smub.CONTACT_FAST');
    catch ME
        disp(ME.message)
        disp('1: Make sure Keithley is turned on')
        disp('2: Press menu -> LAN -> apply_settings -> click yes')
        disp('3: Press status -> config/fault')
        disp('4: Wait and you see: starting manual config')
        disp('5: After 8 sec: manual config started')
        disp('6: Connection is okay now. Rerun initDevice()')
        dev=-1;
    end
end
```

Close connection with Keithley

```
%% function description and information
% This function closes the connection with the Keithley and resets all
% the outputs to zero. Additionally this function can be used as killswitch

% date      modification
% aug-2019  Initial commit by Sjors Dankers
% sep-2019  Added the reset() and lan.autoconnect option
%% implementation
function [] = CloseDevice(dev)
fprintf(dev,'%s\n','smua.source.output=0');
fprintf(dev,'%s\n','smub.source.output=0');
fprintf(dev,'%s\n','smua.source.levelv=0');
fprintf(dev,'%s\n','smub.source.levelv=0');
fprintf(dev,'%s\n','smua.source.leveli=0');
fprintf(dev,'%s\n','smub.source.leveli=0');
fprintf(dev,'%s\n','smua.reset()');
fprintf(dev,'%s\n','smub.reset()');
fprintf(dev,'%s\n','reset()');
fprintf(dev,'%s\n','lan.autoconnect=1');        %should help when initializing
   fails
fclose(dev);
end
```

Set a voltage over source and drain

```
%% function description and information
%{
Sets the voltage between source and drain to a specific value
[] = SetVdrain(device, value)
function requires the variable: 'device' which is returned by initDevice
and the requested voltage

function implemented on 12-aug-2019 by Sjors Dankers

note: smub corresponds to channel b on the scope
changelog:
date:           modifications:
Oct-2019        added OUTPUT_DCVOLTS
%}
%% implementation
function SetUdrain(device, value)
    %sets the corresponding channel to a voltage source
    fprintf(device,'%s\n','smub.source.func=smub.OUTPUT_DCVOLTS');
    %applies the requested voltage to the channel
    fprintf(device,'%s\n',strcat('smub.source.levelv=',num2str(value)));

end
```

Measure the current through the source-drain

```
%% function description and information
%{
Measures the current between the source and the drain
returns the measured current between Vsource and Vdrain

function implemented on 12-aug-2019 by Sjors

note: smua corresponds to channel a on the scope
changelog:
date:           modifications:
Oct-2019        added OUTPUT_OFF. otherwise measuring is not possible
Nov-2019        changed output_off to output_dcamps. when ONLY measuring,
                only volts or amps can be measured if wired accordingly
%}
%% implementation
function [Idrain] = GetIdrain(device)
    %sets the corresponding channel output off, making measuring possible
    %fprintf(device,'%s\n','smub.source.func=smub.OUTPUT_DCVOLTS');
    %requests a current measurement from channel b
    Idrain=str2double(query(device,'print(smub.measure.i())'));
end
```

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Declaration concerning the TU/e Code of Scientific Conduct for the Master's thesis

I have read the TU/e Code of Scientific Conduct[i].

I hereby declare that my Master's thesis has been carried out in accordance with the rules of the TU/e Code of Scientific Conduct

Date

20 - feb - 2020

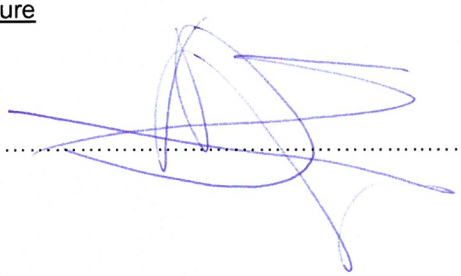
Name

Sjors Dankers

ID-number

1021687

Signature



Submit the signed declaration to the student administration of your department.

[i] See: http://www.tue.nl/en/university/about-the-university/integrity/scientific-integrity/
The Netherlands Code of Conduct for Academic Practice of the VSNU can be found here also.
More information about scientific integrity is published on the websites of TU/e and VSNU