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Thermoelectric properties of InSb nanowires

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BACHELOR FINAL PROJECT
3CEX0

Thermoelectric properties of InSb nanowires

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July 19, 2019

Abstract

Solid state thermoelectric generators use the Seebeck effect to convert heat to electrical energy. The efficiency of these devices is not high enough as of yet for large scale practical purposes. InSb nanowires are predicted to have an increassed efficiency due to quantum confinement effects as their diameter decreases. InSb nanowire field-effect transistors with a heating element are created. The temperature profile due to the heating elements is measured by resistance thermometers and thermal reflectance imaging. A COMSOl model is calibrated with these measurements, which makes it possible to calculate temperature differences. The Seebeck coefficient S and electrical conductivity σ of InSb nanowires with diameters from 81 to 160 nm are measured for temperatures ranging from 6 to 420 K. The field-effect, which is created by an applied back-gate voltage, is found to have an influence of the thermoelectric power factor $S^2\sigma$. An increase in the power factor is observed near room temperature, which is attributed to an increased conductivity from the field-effect. The mobility and carrier concentration are measured and determined from conductance measurements during back-gate voltage sweeps.

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1 Introduction

Human energy consumption from non-renewable fossil fuel sources has lead to a global temperature increase of 1 °C since the industrial revolution. It is estimated that this temperature increase continues with a likely additional increase of 1.5 °C if the current and projected usage continues. The rising global temperature is linked with sea level rises and other undesirable effects for humans [1]. A reduction of the usage of fossil fuels is needed to stop the rising temperature. This can be accomplished by using renewable sources, but also by increasing the thermal efficiency of current energy conversion methods.

In thermodynamics thermal efficiency is defined as the ratio of work produced and the energy being put in. The second law of thermodynamics limits the efficiency of all processes leading to a production of waste heat. That is heat being produced as a generally unwanted byproduct of a machine doing work. It is estimated that 72% of the global primary energy consumption is lost in heat after conversion [2]. This waste heat can be used for heating purposes of houses [3], or it can be converted to electric energy by use of thermoelectric generators.
Thermoelectric generators such as steam turbines are used in power plants as the main method of heat conversion to electric energy. They are quite large and require moving parts which makes them unpractical to use in cars, body heat scavenging methods or in combination with solar cells. For these purposes solid state thermoelectric generators are needed that make use of the Seebeck effect. Currently the efficiency of bulk material based devices is not high enough to be implementable in industry [4]. This can be improved by the use of small diameter nanowires as is predicted by theoretical work on thermopower dating back to 1993 [5]. InSb nanowires are a promising candidate to observe these improvements [6]. This project is therefore an experimental study on the thermoelectric and electrical properties of InSb nanowires for temperatures from 6 to 420 K and under the influence of the field-effect.

2 Theory

2.1 Seebeck effect

The Seebeck effect, named after German scientist Thomas Johann Seebeck, is a thermoelectric effect that describes the voltage difference created between two points in a material due to a temperature gradient in the material. The size of this effect is given by the Seebeck coefficient S, defined as in equation 1:

$$S = \pm \frac{\Delta V}{\Delta T}. \tag{1}$$

Where ΔV is the electrical potential difference and ΔT the temperature difference between two points. The potential difference is created due to transport of charge carriers, either electrons or holes, from the higher temperature side to the lower temperature side. This transport of charge builds up an electric field across the material.

The sign of S is dependent on whether the majority of nearly-free charge carriers are electrons which makes the sign negative or holes which makes the sign positive. For semiconductors this means that the Seebeck coefficient of a n-type doped materials will generally be negative while a p-type doped material will have a positive value.

The Seebeck effect has practical uses in thermoelectric devices where it is used for power generation by converting thermal energy to electrical energy. An example of such a device is listed in figure 2.1.

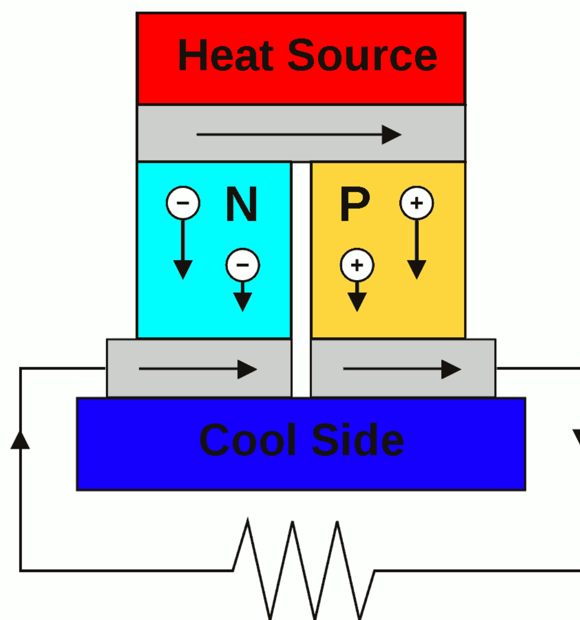


Figure 2.1: A schematic drawing of a typical thermoelectric device consisting out of a n- and p-type semiconductor. Adapted from Wikipedia commons [7].

These thermoelectric devices can also be used for cooling purposes where electrical energy is used to transfer heat. This type of cooling is known as Peltier

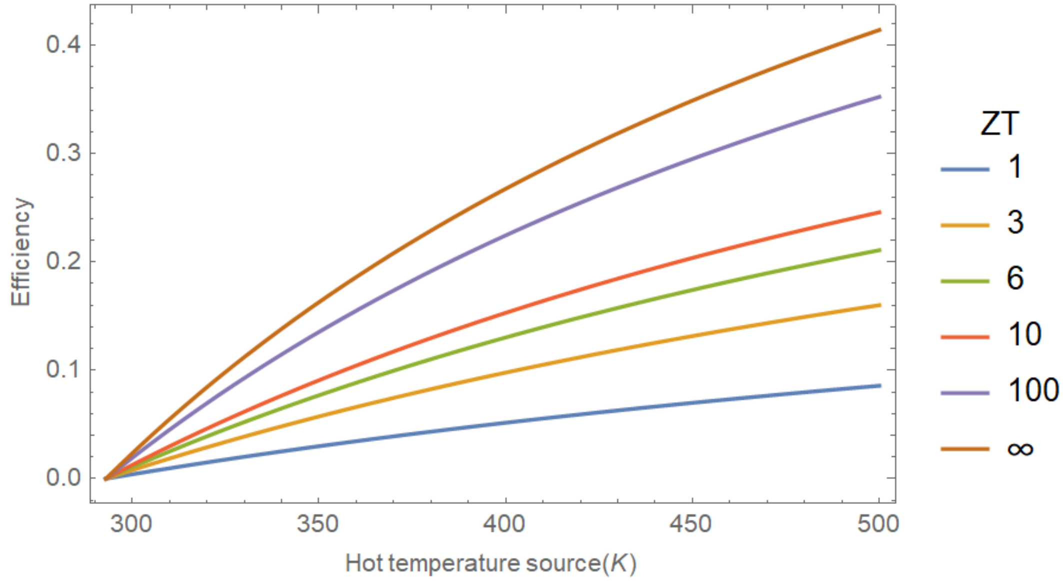


Figure 2.2: Efficiency curve plotted for several values of the TE figure of merit for $T_C = 293\text{K}$

cooling which makes used of the complementary Peltier effect. The suitability of a material to be used in thermoelectric devices can be largely characterized by its thermoelectric figure of merit.

2.2 Thermoelectric figure of merit

The thermoelectic figure of merit zT of a material is a measure of the efficiency at which heat energy can be converted to electrical energy. It is given by equation 2:

$$zT = \frac{S^2 \sigma T}{\kappa} \tag{2}$$

In which σ is the electrical conductivity of the material, κ is the heat conductivity of the material, T_H the temperature of the hot side, T_C the temperature of the cold side and S is the previously mentioned Seebeck coefficient. ZT is related to the Carnot efficiency η_C and the maximal obtainable efficiency for a TE device $\eta_{\max}$ by:

$$\eta_{\max} = \eta_C \frac{\sqrt{ZT_M + 1} - 1}{\sqrt{ZT_M + 1} + \frac{T_C}{T_H}} \tag{3}$$

Plotting this relation in figure 2.2 for multiple values of ZT shows that as ZT increases the efficient asymptotically reaches the Carnot efficiency and that at low values of ZT increases herein lead to relatively high increases of the efficiency. For practical purposes ZT ~3 is needed to be applicable at large scale.[4, 6]

From equation 2 it becomes clear that in order to achieve a high thermoelectric figure of merit, the electrical conductivity and the Seebeck coefficient must

be maximized while the heat conductivity must be minimized. The thermal conductivity of a material can be attributed to sum of two contributions: thermal conductivity due to electrons: κ_e and thermal conductivity due to lattice waves: κ_l. The electrical conductivity in a specific direction is the reciprocal of the resistivity ρ, which itself can be determined by measuring the electrical resistance R of a material:

$$1/\sigma = \rho = \frac{R * A}{l}. \tag{4}$$

In this equation A is the surface area perpendicular to the measured direction and l is the length over which the resistance is measured. Optimization of these parameters is hard due to the strong interrelation between them which becomes clear in the following section.

2.3 Boltzman transport equation for electrons

The parameters characterizing the thermometric performance can be described using Boltzman transport equations for each parameter respectively. These equations are valid in the diffusive transport regime of charge carriers, meaning that the mean free path of the charge carriers is way smaller than the lengths scale over which the transport takes place. From these equations the Mott expression for the Seebeck coefficient for metals and semiconductors can be derived and is given by:

$$S = \frac{\pi^2}{3}\frac{k_B}{q}k_\mathrm{B}T\left\{\frac{\mathrm{d}[\ln(\sigma(E))]}{\mathrm{d}E}\right\}_{E=E_\mathrm{F}}. \tag{5}$$

Wherein the electrical conductivity $\sigma(E)$ can be written as:

$$\sigma = n_e(E)\mu_e(E)e + n_h(E)\mu_h)E)e. \tag{6}$$

Here $n(E)$ and $\mu(E)$ are the energy dependent free carrier concentration and mobility of electrons and holes respectively and e is the elementary charge.

Substituting equation 6 into equation 5. gives the Seebeck coefficient in the following form:

$$S = \frac{\pi^2}{3}\frac{k_\mathrm{B}}{q}k_\mathrm{B}T\left\{\frac{1}{n}\frac{\mathrm{d}n(E)}{\mathrm{d}E} + \frac{1}{\mu}\frac{\mathrm{d}\mu(E)}{\mathrm{d}E}\right\}_{E=E_\mathrm{F}}, \tag{7}$$

revealing the dependence of S on n and μ and their respective energy derivatives. It should be noted that the Seebeck coefficient and the conductivity both depend on the same interrelated material properties. This makes it hard to increase the Thermoelectric figure of merrit in bulk materials for which equation 1 can be uses. In lower dimensional structures like nanowires, quantum effects become more prominent. This has an effect on the thermolectric properties of materials which will be discussed in the following section.

2.4 InSb nanowires for thermoelectric energy conversion

An increase of the so defined power factor $S^2\sigma$ nanostructure materials with respect to their bulk-sized counterparts was first predicted in a paper by Hicks

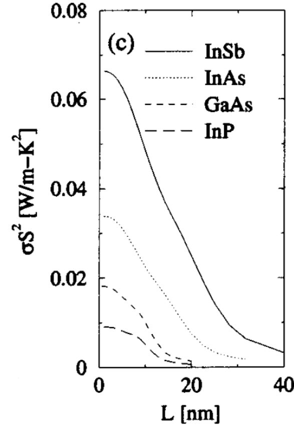


Figure 2.3: The theoretical power factors of a InSb nanowire and other wires plotted as a function of diameter. Graph adapted from N. Mingo 2004 [6].

and Dresselhaus in 1993 [5]. This increase is believed to be due to the influence of quantization and degeneracy in the energy bands of a material confined in a nanostructure. This causes a asymmetry of the density of states (DOS) around the Fermi-level, which leads to high values of the energy derivatives in equation 7. Theoretical predictions made by [6] indicate that InSb nanowires are a high potential candidate as a thermoelectric material due to the strongly increasing thermoelectric figure of merit as the diameter decreases to the order of 10's of nanometers. The power factor calculated by these predictions of a InSb nanowire is plotted together with other semiconductors in figure 2.3. The main reason for this high power factor is due to its its low effective band mass, which allows for a high mobility of the carriers [8][9]. This expected increase of the power factor in nanostructures has however not yet been shown in experimental studies [10]. Theoretical follow-up studies, which propose more sophisticated models, predict that this increase is only expected at temperatures at which the thermal energy is far lower than the bandgap between the lowest sub-bands. For InSb this means, using the band gap value 0.0015 eV from [11], that the temperature must be far below 174 K. At these temperatures a 1-band model is valid to use, from which a upper bound of the power factor can be determined: [12]

$$\left(S^2\sigma\right)_{\text{limit}} < \left(S^2G\right)_{\text{QB}} \times \frac{\lambda_{1,\text{max}}}{A}. \tag{8}$$

In this equation $\left(S^2G\right)_{\text{QB}}$ is the quantum power factor limit, $\lambda_{1,\text{max}}$ the maximal value of the mean free carrier path of the lowest sub-band and A the cross sectional area of the nanowire.

Modifications of the model used by Hicks and Dresselhaus that also include the thermal wavelength of the charge carriers predict that the diameter of nanowires should be decreased below the thermal wavelength to observe improvements of the power factor over bulk values [13].

The approach by Hicks and Dresselhaus is a single band model. Studies that take into account multiple sub-bands, which is more accurate at high temperatures and larger diameters, actually predict an decrease in power factor when the

diameter approaches the tens of nanometers [14]. An increase of the power factor is only expected when the diameter becomes small enough.

Nanowires are still an interesting structure for thermoelectrics despite the reservations on the increasing power factor. The introduction of nanostructures decreases the thermal conductivity. As the conduction of heat by the lattice is greatly reduced due to boundary scattering effects and lower phonon group velocity[15]. These reduction effects occur when the typical length scales of the material are below the mean free path of phonons [16]. For InSb this mean free path of phonons is estimated to be around 84 nm [17]. Doping has no significant effect on κ_L, thus optimization of ZT means optimization of the power factor [4].

2.5 Field-effect nanowire transistors

The measurement device used in this report consists out of a n-type doped semiconductor InSb nanowire embedded on silicon wafer over which a back-gate voltage can be applied. Device characteristics can be found in the experimental set-up section 3.2. This system forms a Field-Effect Transistor (FET). The electrical field created by applied the back gate voltage interacts with the charge carriers in the semiconductor. This causes a shift in the energy of the carriers, effectively shifting the Fermi level up for a positive gate voltage and down for a negative voltage. Metal-semiconductor junctions are formed between the Cr/Au top contacts and the InSb nanowire. Two types of junctions can be formed namely Ohmic and Schottky junctions. An Ohmic junction is formed when the Fermi level of the metal is higher than that of the semiconductor. As a result for a n-type material electrons accumulate on the semiconductor side increasing the conductivity while acting as a resistor. A Schottky junction is formed when the Fermi level of the semiconductor is higher. This has the result that charges move from the conduction band of the semiconductor to the empty states in the metal creating a depletion region inside the semiconductor. The depletion combined with the increased negative charge on the metal side creates a potential barrier or Schottky barrier.

The field-effect mobility can be calculated using the standard square law model that is used in other studies that use nanowire field-effect devices [18, 19, 20]. It is possible to extract the field-effect mobility and the carrier concentration from the FET device if the electrical transport takes place in the classical transport regime. The mobility of such a nanowire device with length L given by:

$$\mu = \frac{L^2}{C_{ox} \cdot V_{sd}} \left(\frac{dI_D}{dV_{bg}} \right)_{\text{max}}. \tag{9}$$

In this equation the fraction $\frac{dI_D}{dV_{bg}}$ is called the transconductance, which can be measured as the slope of a drain current-back-gate voltage sweep and V_{sd} is the applied voltage over the metal source and drain in contact with the nanowire.

C_{ox}, the gate-nanowire capacitance of the device is calculated from the model

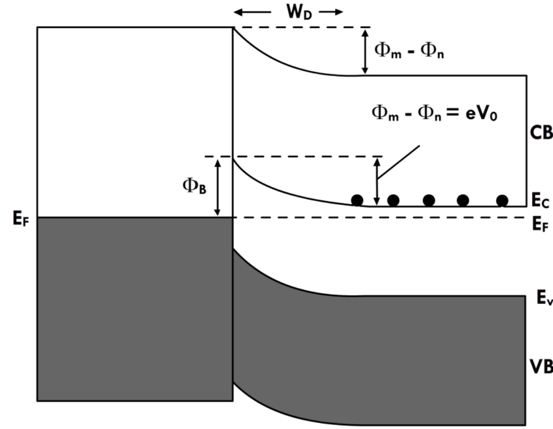


Figure 2.4: A Schottky junction which shows the band bending in the semiconductor of energy Φ_b. Also shown is the depletion region width W_d. Taken from: Principles of Electronic Materials - S.O. Kasap.

studied in [21]:

$$C_{ox} = \frac{2\pi\epsilon\epsilon_0 L}{a\cosh\left(\frac{d+2t_{ox}}{d}\right)}, \tag{10}$$

for a hexagonal shaped nanowire which is embedded in the dielectric substrate. ϵ is the dielectric constant of the embedding dielectric, ϵ_0 is the vacuum permittivity, d is the diameter which is for a hexagonal wire is here taken as the maximal diameter and t_{ox} is the thickness of the dielectric.

The effective charge carrier density n of the InSb nanowire can also be obtained, by measuring the threshold voltage V_{th} of the FET. It is calculated from equation 11

$$n = \frac{4C_{ox} \cdot V_t}{e \cdot \pi d^2 L}. \tag{11}$$

3 Experimental set-up

3.1 Nanowire fabrication and characterization

The nanowires used in this experiment are InSb nanowires grown on an (111) InSb substrate using the Vapor-Liquid-Solid (VLS) technique. The stemless InSb nanowires are grown at the surface pushing the gold catalyst particles in which In and Sb vapor is contained upward. This process takes place inside a horizontally orientated Aixtron 200 metal-organic vapor phase epitaxy (MOVPE) reactor. A prefabricated sample is annealed by heating it up to 510 °C, forming gold droplets on the substrate surface. These droplets are then introduced to a gaseous molecular mixture of In, Sb and methyl groups. The methyl groups will be separated from the the In and Sb molecules as In and Sb are absorbed by the gold particles. At some point the gold particles become saturated with the indium and antimony, which causes InSb to be shed under the gold particles pushing the gold particles upwards while creating an InSb nanowire. The fabricated nanowires have a zinc blend crystaline structure free of defects with a uniform diameter. SEM images of the InSb nanowires are shown in the appendix E.

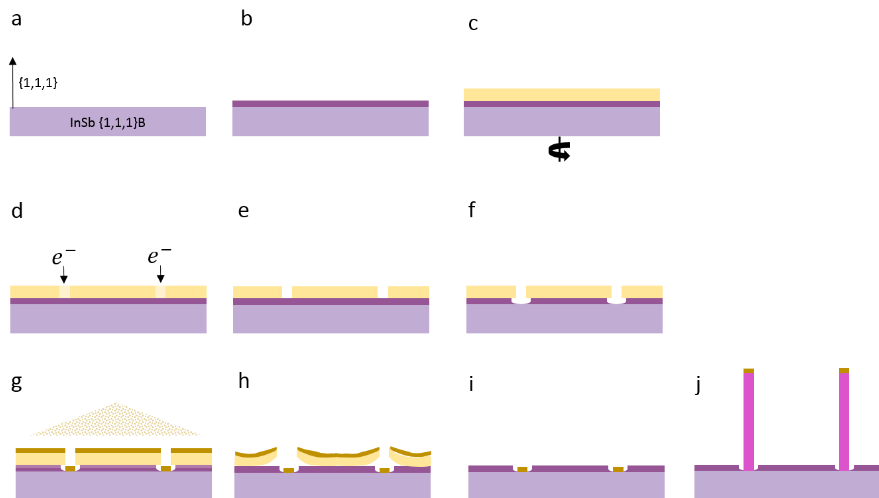


Figure 3.5: A schematic overview of the nanowire growth procedure. (a): A (111) InSb substrate is used as wafer. (b): Si_3N_4 is deposited on the substrate by use of plasma-enhanced chemical vapor deposition (PECVD). (c): A layer of spin resist is applied on top of the substrate after which the wafer is baked. (d): Electron beam lithography (EBL) is used to make holes in the resist. (e): Polymer segments are further removed by the use of a developer. (f): Si_3N_4 is etched from the holes by buffered oxide etchant. (g): Using electron beam evaporation, an 8 nm thick gold film is placed on top of the structure. (h): PRS3000 is used in the lift-off process to remove the gold film. (i): Gold catalyst droplets remain in the made holes. (j): The InSb nanowires are grown using the MOVPE growth process. The pictures are courtesy of G. Badawy and S. Gazibegovic.

3.2 Device fabrication

InSb Nanowire field-effect transistors are fabricated which makes it possible to also study the nanowire's field-effect dependent properties. Multiple InSb nanowires are embedded on top of a Si/SiO_2 wafer consisting out of a SiO_2 top layer with a thickness of around 100 nm, a heavily doped p-type Si++ and a thin Au back layer which ensures electrical conductivity with the back-gate. Contact pads are placed on the wafer on which probes can be placed that are connected to the measurement equipment. Gold lines are lead from the contact pads towards the nanowires to which they are connected by means of Cr/Au top contacts. To ensure good contact quality, sulfur passivization is used to clean the oxide layer on the wire and between the contacts. Heating structures made from gold lines, through which a current can be applied, are also embedded in the SiO_2 layer. The nanowire, contacts and silicon layers are shown in figure 3.6. And under it in figure 3.7 a sketch of the device from a top view is shown.

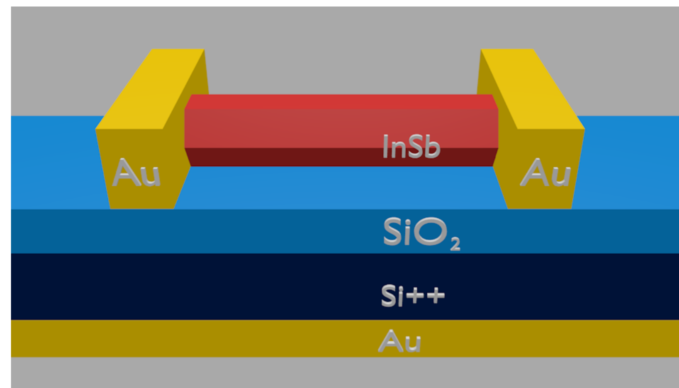


Figure 3.6: An image showing device components with their respective chemical notation. Image is not to scale, adapted from [22].

A list of all the steps performed to create the device is provided in appendix H. The fabricated device is then placed on a gold contact plate, inside a vacuum chamber which is held below room pressure by a pump. A voltage can be applied over the gold contact plate, forming the back-gate of the FET. Silver paste is used in between the gold contact plate of the vacuum chamber and the gold layer at the back of the silicon wafer to ensure a good back-gate contact. A heating element is present in the vacuum chamber that allows for increasing the temperature by a controller. Also present is an inlet/outlet for liquid helium that makes it possible to cool down the setup to temperatures below 10 K. Two probe arms with six probes each are inside the chamber. These probes can be placed on top of the nanowire device's contacts by using a translation stage that can position the probe arms. The probes themselves can be connected to other measurement equipment.

3.3 Calibration measurements of the temperature

The resistance of several pairs of thermometers embedded on the top layer are measured for a range of ambient temperatures from 300 to 420 K. The gold lines

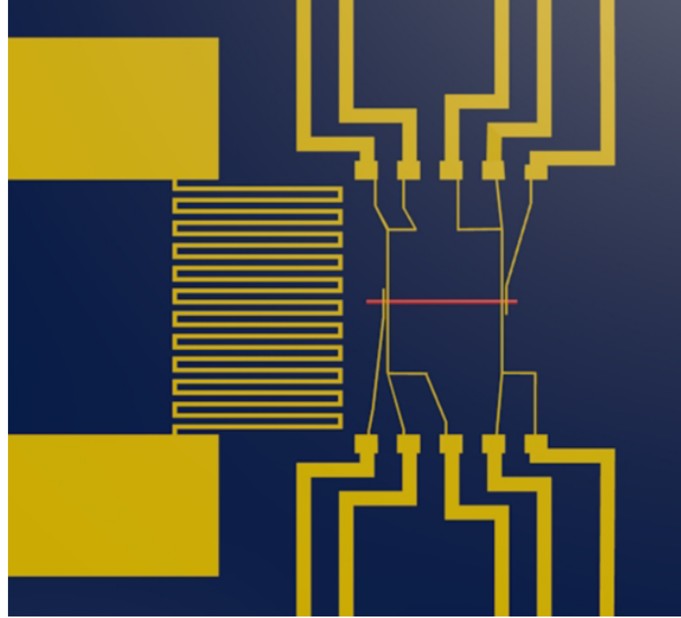


Figure 3.7: A sketch of the device from a top view showing the gold line structures and a red InSb nanowire. Image adapted from [22].

acting as resistance thermometers follow a linear resistance temperature relation. A linear fit is made through the measured resistances to determine the slope of this relation. The slope itself is needed to measure the temperature difference at the two ends of the nanowire when the sample is placed in a temperature gradient. In order to measure this temperature difference, the resistance of the two thermometers is measured subsequently when the current through the heating element is off and thereafter set at 12 mA. Dividing the resistance differences by the slopes from the linear fit gives the required temperature difference at the positions of the resistance thermometers. An example plot of the resistance temperature measurements of the two thermometers and a SEM (Scanning Electron Microscopy) image of a typical device used in this project are shown in figure 3.8 and 3.9 respectively.

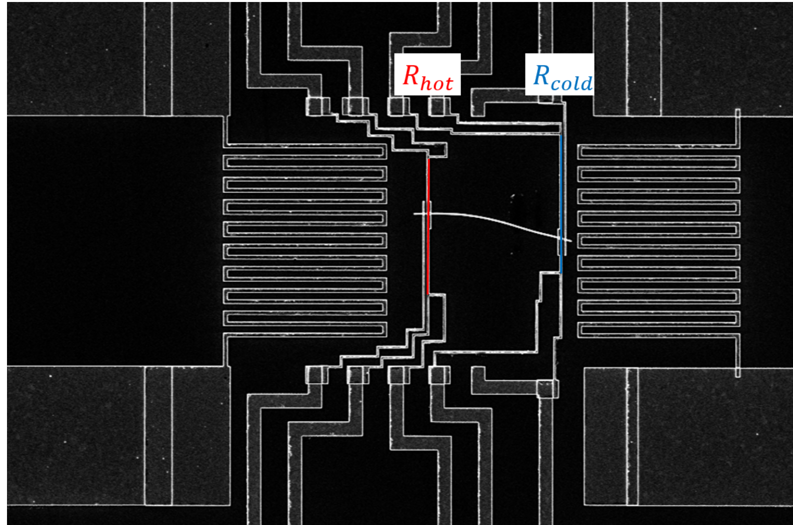


Figure 3.9: An SEM image of a device used to measure the temperature profile when the left heater coil is turned on. A red line is drawn over the thermometer of the hot side and a blue line is drawn over the thermometer of the cold side.

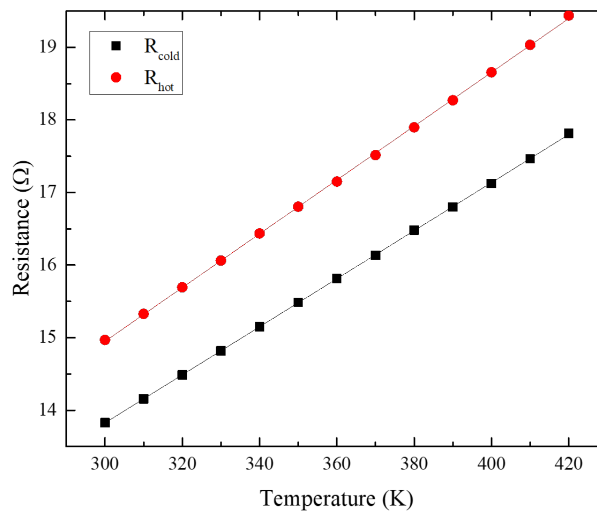


Figure 3.8: Resistance plotted for range of temperatures where R hot is the resistance of the thermometer closest to the heating and element and R cold the other thermometer. Linear fits are made through the data points: black line for R hot and red line for R cold.

A set of thermometers is measured four times to obtain a measure for the uncertainty of the measurements. It is noted that the presence of a nanowire is found to have no noticeable effect on the temperature profile. From the results shown in figure 3.10, can be seen that as a device is measured multiple times, the variation in the measured resistance decreases. This might be due to thermal annealing of the gold used in the contacts resulting in a change of crystal structure

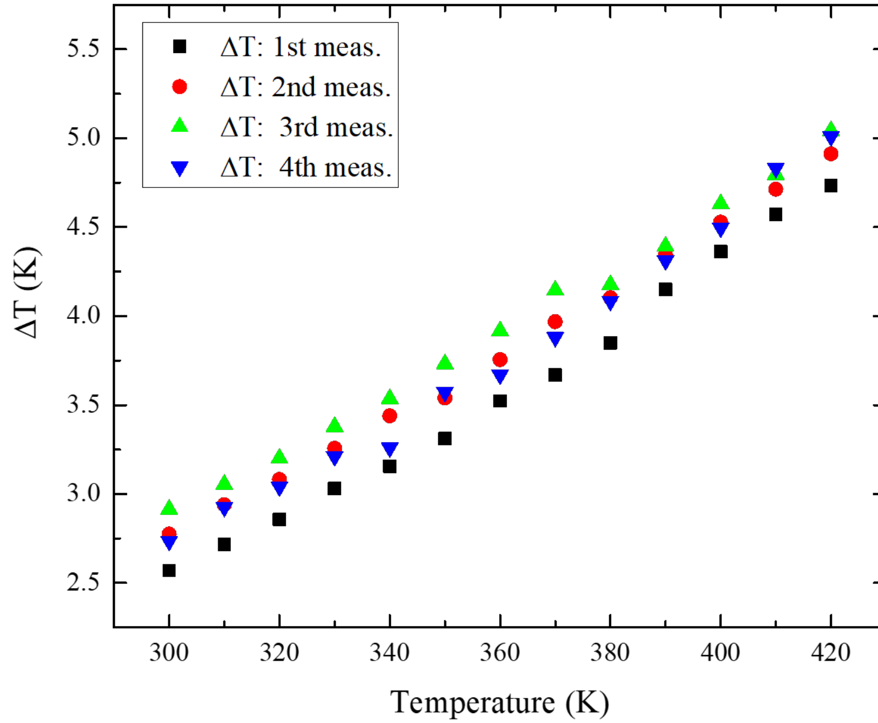


Figure 3.10: Measured temperature difference between the two thermometers on the measurement device, plotted for a range of ambient temperatures. The temperature difference is measured four times as listed in the legend.

and thus resistance.

The distances of the thermometers from the heating element and the distances between them are determined from SEM images. With the temperature difference and the distances known it is possible to establish a temperature profile over the microchip as a function of the distance from the heater. This temperature profile is further compared with a COMSOL model of the setup that is build with the assumption that the heat from the coil will mostly spread through the layer of SiO_2 in which the nanowire is embedded. These comparisons are performed using similar dimensions and device geometry in the COMSOL model. Modeling of the temperature gradient due to a heating element for thermoelectric purposes has been done before in other studies [12].

Further conformation of the validity of the COMSOL model is performed by thermal reflectance imaging of devices with a similar heating element and multiple gold square pads spread over the device. Gold square pads are used, because of its high reflectivity while the SiO_2 top layer is mostly transparant to the 470 nm wavelength light used to obtain the thermal reflectance image [23]. The temperature differences between the gold pads can thus be obtained which provides an indication of the temperature profile of the device. A thermal reflectance image obtained a device with just a heater, nanowire and contact lines is shown in fig-

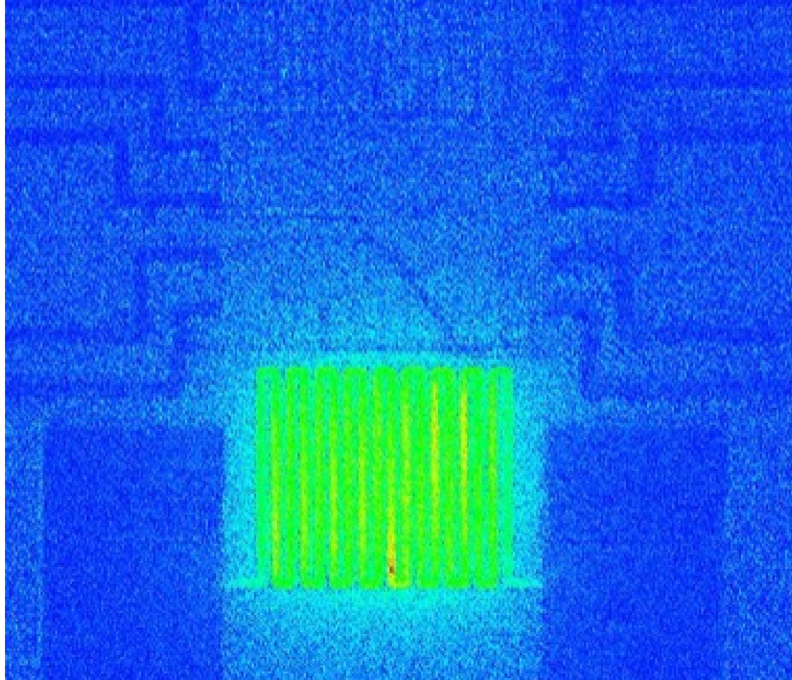


Figure 3.11: A thermal reflectance image obtained at room temperature of a device with a heater and nanowire. The color scale goes from high temperature: green, to lower temperature: blue.

ure 3.11. It is not calibrated with respect to a known temperature and shows that only the gold lines and nanowire are visible with this measurement technique. In appendix G the thermal reflectance set-up is shown together with more thermal images.

3.4 Thermoelectrical properties measurements

The electrical conductivity of InSb nanowires is measured and calculated, the method uses equation 6 which makes it possible to determine the conductivity of a nanowire by measuring the electrical resistance R. This is done by using a Keithley 4200 SCS unit forcing a constant current through the wire and measuring the voltage as a result over the wire. Ideally these measurements are performed using 4 probes which eliminates the influence of contact and lead resistances in the measurement setup [24]. The slope of the linear fit made from the I-V plots as shown in figure 3.12 is the resistance of the wire at a specific ambient temperature T. This method also requires the nanowire length and diameter which are estimated from the SEM images of the devices. From the linear fit, the offset ΔV is also determined by substracting the intersection values at zero current. These ΔV values are used to determine the Seebeck coefficient of the wires as defined in equation 1. The ΔT values are obtained from the calibrations/simulations of the temperature profile as described in the previous subsection. The ambient temperature of these measurements can also be set which makes it possible to study the temperature dependence of the InSb nanowire's thermoelectrical properties. And because the device measured is a MOSFET like structure a back-gate voltage

can be applied of which the effects on the conductivity and the Seebeck effect are thus also measured.

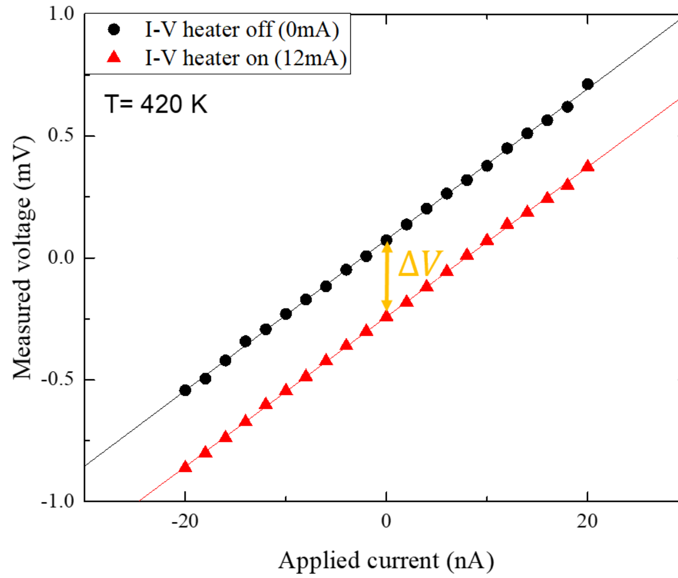


Figure 3.12: Plot of voltage measured over a InSb nanowire against the applied current. Data is plotted and fitted with: red triangles and without: black circles, a heating current of 12 mA applied through the heating element on the chip.

3.5 Mobility and carrier concentration

Back-gate voltage sweeps are performed in forward and backward direction by measuring the drain current through the wire at a constant drain voltage. The mobility and carrier concentration of the charge carriers in the nanowires are determined from these measurements by a linear fit method. This method relies on a linear fit tangent to the region of maximal transconductance ($\frac{dG}{dV_{bg}}$) as done in [18, 19, 20]. From the slope of this fit the mobility is calculated as described in equation 9, the carrier concentration is determined by equation 11 where V_{th} is taken as the gate voltage value at which the fitted drain current is zero. An example of this method is shown in figure 3.13

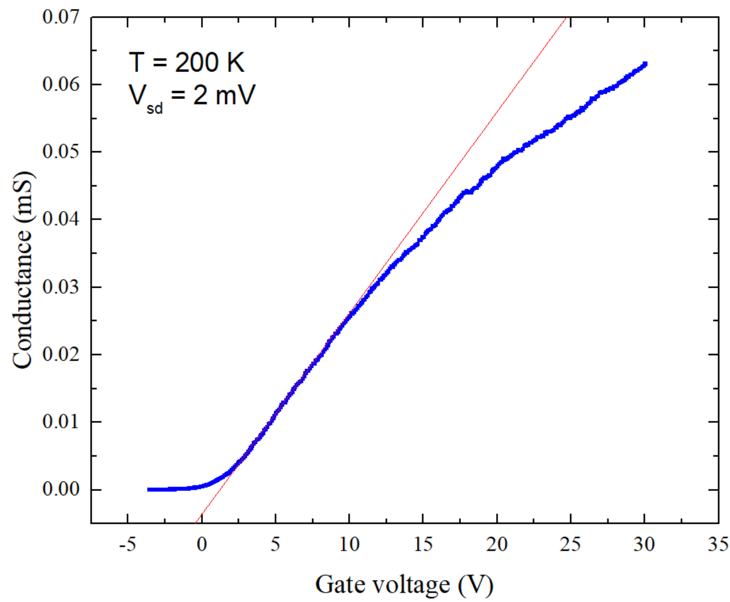


Figure 3.13: Conductance of an InSb nanowire plotted as a function applied back-gate voltage at an ambient temperature of 200K with an applied drain voltage of 2 mV. Through the data (blue) a red linear fit is plotted tangent to the maximal slope of the the conductance curve.

It is also possible to determine the mobility of the nanowires by fitting the conductance directly and determining the mobility as a fitting parameter. This method is further evaluated and compared to the linear fit method in appendix B. Fitting the conductance model directly proved to be difficult for some of the measurement therefore the values obtained in the result section are based on the linear fit method.

4 Results & Discussion

In this section measurement results of InSb nanowires of different dimensions are presented and discussed, starting with observations of the contact and nanowire characteristics.

4.1 Characterization of applied contacts and nanowire properties

4.1.1 Metal-semiconductor contact interface

The contact and line resistance is measured by comparing the resistance of a similar wire segment obtained by two probe measurements with the resistance obtained by four probe measurements obtained at an ambient temperature of 420K. This result is plotted in figure 4.14, from which is calculated that the contact and line resistance is found to be $(110\pm21)\Omega$.

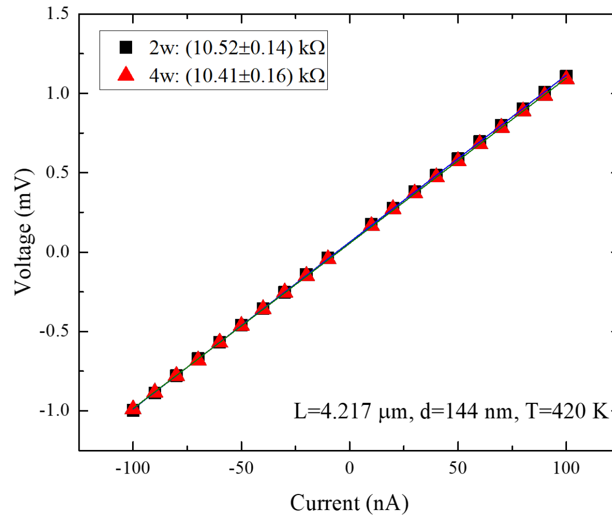


Figure 4.14: The I-V curve of a InSb nanowire connected to Cr/Au contacts, where the 2W curve is obtained by two point contact measuring and 4W is obtained with four point contact measuring. Resistance is obtained from the slope of the linear fit: blue for 2W and green for 4W. The measured resistance of the same wire segment is listed in the legend.

4.1.2 Signs of quantum interference

Back gate sweeps performed at 10 K and 6.1 K and the results are shown in figure 4.15. Oscillatory behaviour of the conductance of a short segment nanowire with a length of 220 nm and diameter of 85 nm is observed. Here the length is taken as the spacing between the contacts. These oscillations are not found at

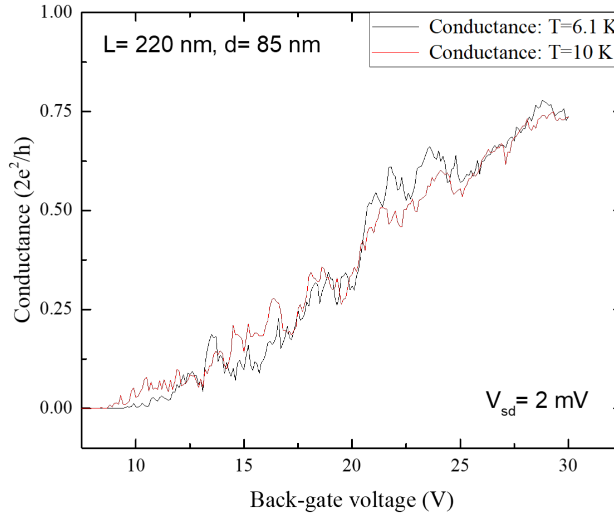


Figure 4.15: Conductances of a InSb nanowire segment of length 220 nm and diameter 85 nm plotted for the forward sweeping back-gate voltage. Data shown in black is measured at 6.1 K and red at 10 K.

higher temperatures or longer wire segments which might indicate that the electronic transport is taking place in the (quasi)ballistic regime. Conductance oscillations have been observed in other studies [25] where they have been identified as Fabry-Pérot oscillations. It is therefore likely to observe ballistic transport in InSb nanowires on devices with a shorter channel length and/or at a lower temperature.

4.1.3 Ambipolar electrical transport in InSb nanowires

Back-gate voltage sweeps in the forward and backward direction are performed subsequently while measuring the conductance of the nanowires. From these measurements can be seen in figure 4.16 that the wires can facilitate ambipolar transport. This is observed for temperatures of 200 K and below. It is therefore possible to measure the electrical and (thermoelectric) properties of both holes and electrons depending on the temperature and applied back-gate voltage. There is a small hysteresis observed between the forward and backward sweep direction. This can be caused by heating of the wire during the back-gate sweep or due to water on the silicon substrate acting as a polar field gate [19].

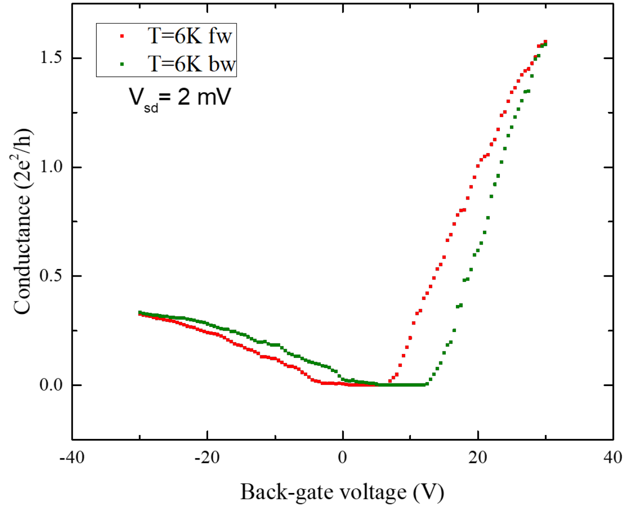


Figure 4.16: The electrical conductance plotted against the back-gate voltage. The red square data is obtained from the forward sweep direction and the green squares are obtained from the backward sweep direction.

4.1.4 The band gap extraction of InSb nanowires

The band gap energy between the valance and the conduction band can be extracted from the resistance temperature data which is measured to determine the electrical conductivity. The natural logarithm is plotted against 1/T of which the slope determined by a linear fit. For a n-type doped semiconductor dividing the slope by K_b, where K_b is the Boltzmann constant, gives the band gap energy in Joules. This method is based on the Boltzmann relation. Only 2 wires have a nice linear slope for all values. The plot of one of these wires is shown in figure 4.17. From these 2 wires the band gap is determined to be 0.22 ± 0.02 eV. This is in the same order as the literature value of 0.17-0.18 eV at 300 K [26].

4.2 Electrical Conductivity of InSb nanowires

The measured values of the electrical conductivity of the InSb nanowires for a range of temperatures from 300 to 420 K are shown in figure 4.18.

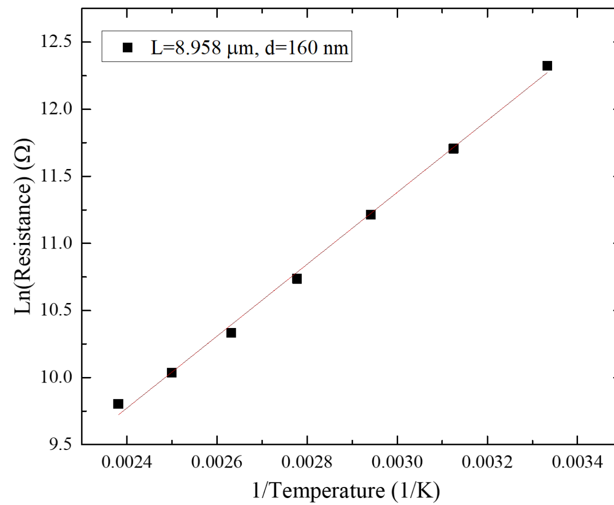


Figure 4.17: The natural logarithm of the resistance plotted against 1/T of a InSb nanowire. A red linear fit is made through the black data points.

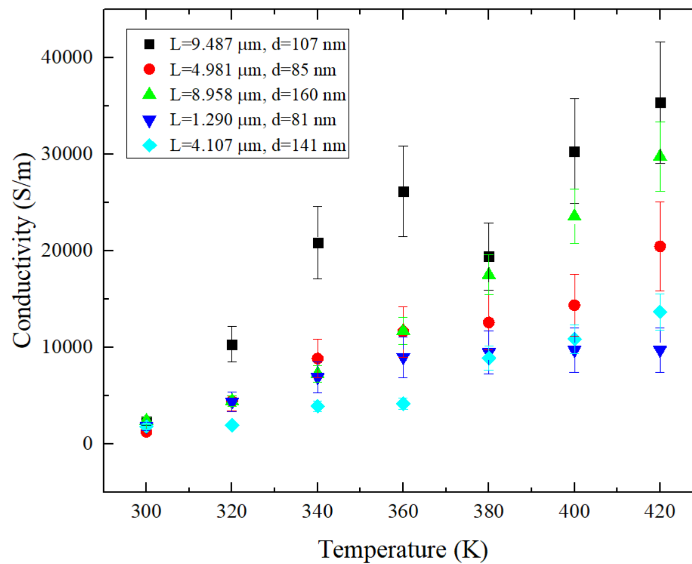


Figure 4.18: Electrical conductivity as a function of temperature for a range of nanowires.

The conductivity of these wires is higher than those of the previous generation [22]. With the highest measured value being $(35\pm6)\cdot10^3$ S/m at 420 K. Other studies on the conductivity of InSb nanowires show an increase in conductivity as the diameter decreases. Here, however, no clear relation between the conductivity and the measured diameter range is found as can be seen in figure 4.19.

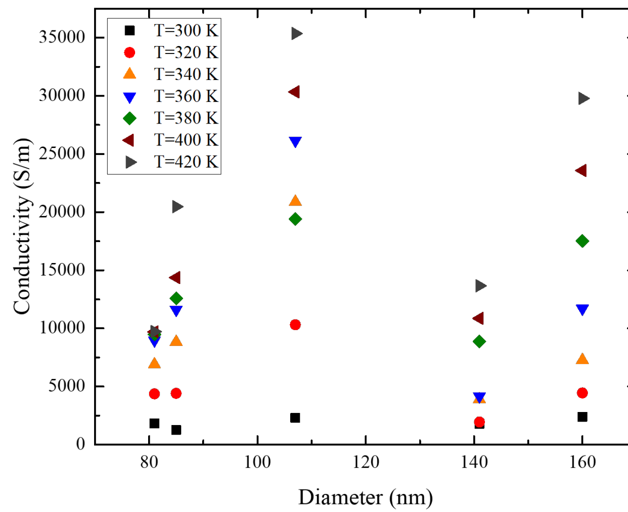


Figure 4.19: The electrical conductivity as a function of nanowire diameter, error bars are left out to increase readability.

4.2.1 Conductivity tuning with the field-effect

The influence of the back gate voltage on the electrical conductivity has been measured for temperatures ranging from 6 to 420 K. In figure 4.20 the change of the electrical conductivity caused by applying a gate voltage of 15 V is plotted for a range of temperatures.

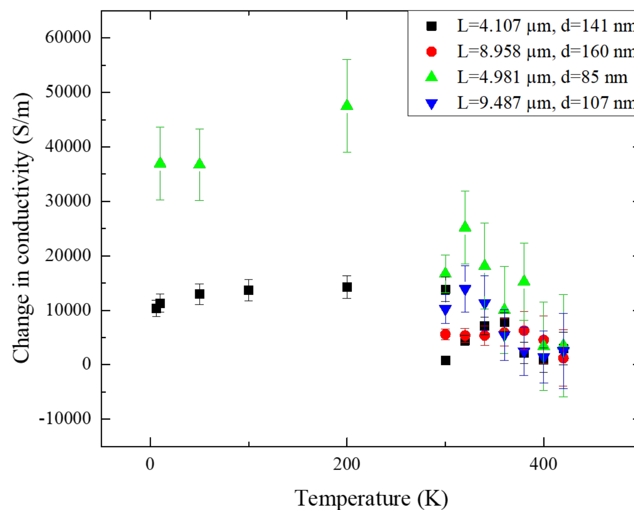


Figure 4.20: Change in conductivity due to an applied gate voltage of 15 V plotted for temperatures from 6 to 420 K.

Here an overall expected increase of the conductivity is observed as the pos-

itive gate voltage shifts the Fermi level up into the conduction band, increasing electron conductivity. In the lower temperature range this effect is strongest. This is mainly due to that the conductivity without an applied gate voltage is lowest at temperatures below 300 K as there are less thermally excited charge carriers. The highest absolute increase in conductivity is measured for wires with the smallest diameter. This might be explained by the geometry of the nanowire device as the smallest diameter wires are situated closer to the back gate, thus interacting with an overall stronger electric field [21]. The effect of applying a negative back gate voltage of -15 V is shown in figure 4.21. At temperatures below 300 K the effect of the negative gate voltage increases the conductivity whereas at temperatures above 300 K a general decrease of conductivity is observed. The increase at low temperatures can be attributed to electron hole facilitated conductivity as the negative gate voltage shifts the Fermi level to the valance band. The same shift downwards counteracts the thermally activated electron charge carriers that enable the conductivity at room temperature and above, causing a shift away from the conduction band. Here again the largest change in conductivity is observed for the smallest diameter wires.

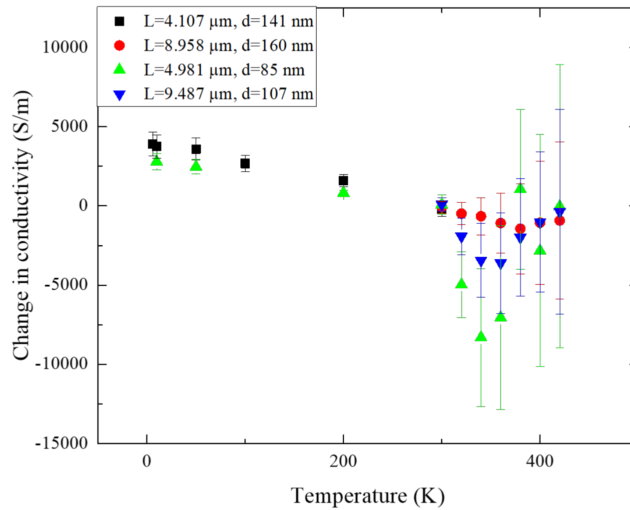


Figure 4.21: The change in electrical conductivity when a negative gate voltage of -15 V is applied plotted for a temperature range from 6 k to 420 K.

4.3 Mobility and carrier concentration

4.3.1 Mobility of InSb nanowires

The electron mobility calculated from the back-gate voltage sweeps for temperatures ranging from 6 K to 420 K k is shown in figure 4.22. These values are obtained for the forward sweep direction. The values found are comparable to other studies [27], but are smaller by a factor of ten compared to more recent studies on high mobility nanowires and the bulk value [28].

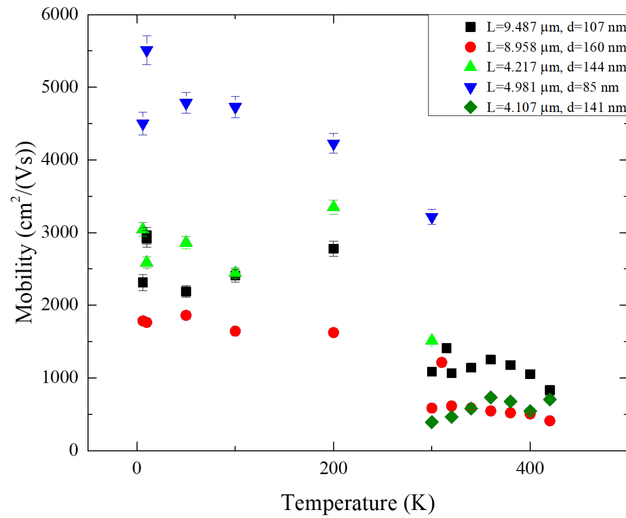


Figure 4.22: The mobility of InSb nanowires plotted as function of the ambient temperature ranging from 6 k to 420 K. At 300 K a shift can be seen for all wires due to different measurements conditions.

At around 300 K can be seen that there is a shift for all wires, this is likely because the high and low temperature data has been measured under different conditions inside the chamber. This is known to influence the mobility significantly [19]. This change in mobility is also observed for the measured nanowires at the same ambient temperature. The differences in conditions are the time and the temperatures the nanowire FET device experienced in the vacuum chamber before the measurements were performed. The suspected reason for this shift is the presence of water molecules accumulating on the surface of the top silicon oxide layer. The size of the shift in mobility can be seen in figure 4.23, where the mobility of a single nanowire has been measured two separate times denoted by the date of measurement. Between these dates the measurement sample has been in vacuum conditions being heated up to 420 K and after that cooled down to 6 K when measurements on a different wire were performed.

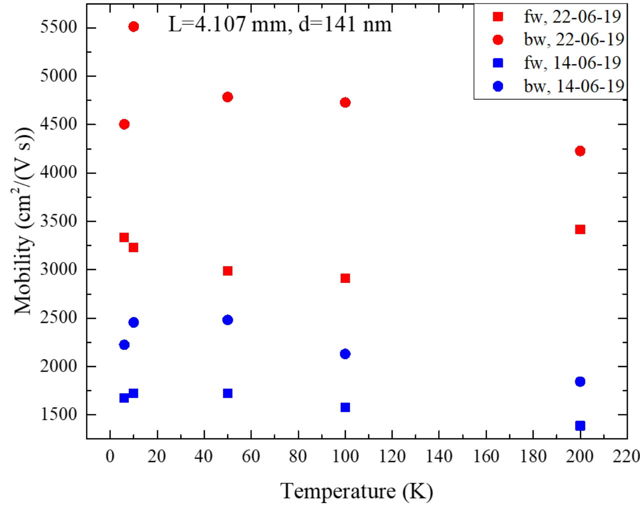


Figure 4.23: The electron mobility obtained by a forward (fw) and backward (bw) back gate sweep measured at two different instance, plotted against the ambient temperature ranging from 6 to 200K. An overall doubling of the mobility is observed after the wire has undergone a thermal cycle.

Usage of the found mobility in combination with other (thermo)electric properties is therefore limited to data obtained under similar conditions.

Below room temperature ambipolar transport is observed for all nanowires. The extracted mobility and carrier concentration of the electron and hole facilitated transport from the backward sweep directions are listed in the appendices C. The electron mobility of $(5.5{\pm}0.2){\cdot}10^3\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$ obtained from the backward sweep direction at 10 K is the highest found of all measured nanowires in this report. The highest hole mobility found from the same nanowire also obtained from the backward sweep at 10K is $633\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$.

The hole mobility of the nanowires is plotted in figure 4.24 for the forward sweep direction. The hole mobility is found to be lower than the electron mobility, this might be caused by the metal-semiconductor junction which can be less transmissible for holes or it is a material property of the InSb nanowires[29].

4.3.2 Carrier concentration of InSb nanowires

The carrier concentration of electrons in InSb nanowires measured from backgate voltage sweeps are shown in figures 4.25 for the forward sweep direction. The carrier concentration shows the expected exponentially increasing behaviour with temperature from about 200 to 420 K. The values found are also of the same order as the values calculated for InSb nanowires in [30]

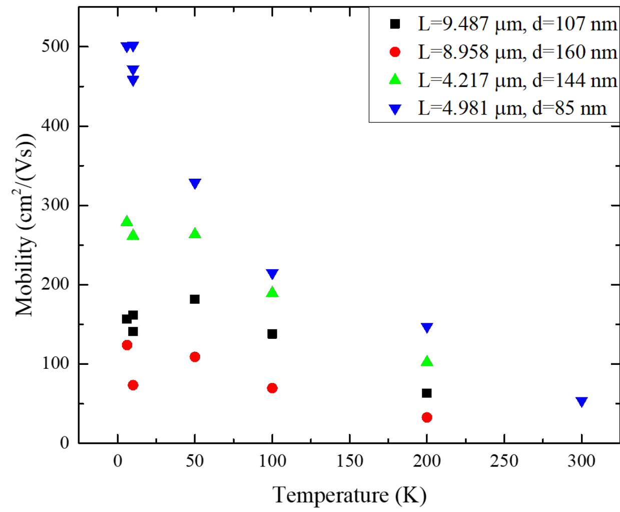


Figure 4.24: The hole mobility of InSb nanowires obtained from a forward back-gate voltage sweep, plotted for temperatures ranging from 6 to 420 K.

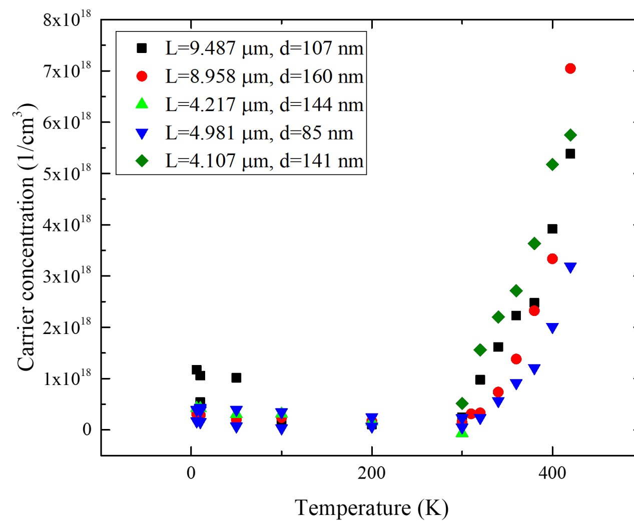


Figure 4.25: The carrier concentration of electrons in InSb nanowires obtained from the forward sweep direction plotted for temperatures ranging from 6 to 420 K.

4.4 Thermoelectric performance

4.4.1 Temperature profile

The temperature of the devices is measured with calibrated thermometers on the devices according to the method described in section 3.3. The results obtained from these measurements are shown in figure 4.26a. Next to it in figure 4.26b is the temperature profile calculated by the COMSOL model.

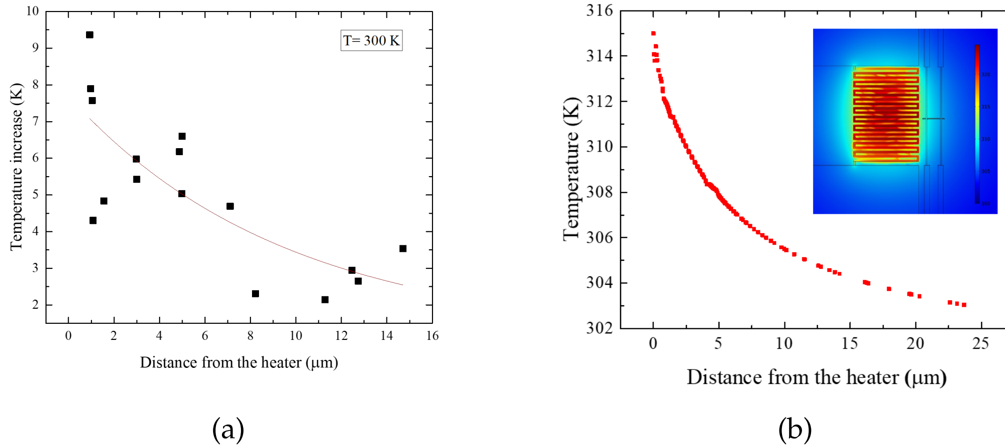


Figure 4.26: Temperature profiles obtained from measurements (a) and COMSOL modeling (b).

The temperature modelled in COMSOL decreases exponentially as a function of distance along a straight line perpendicular to the heater. The temperature along a similar line obtained by thermal reflectance imaging of a device depicted in figure 4.27b confirms the shape of this profile. In this figure the y-axis is not properly scaled as the true temperature at the heater is unknown. The data obtained by thermal imaging contains noise which is filtered out of it to make the shape of the profile more visible. Both profiles are calculated/measured at room temperature respectively.

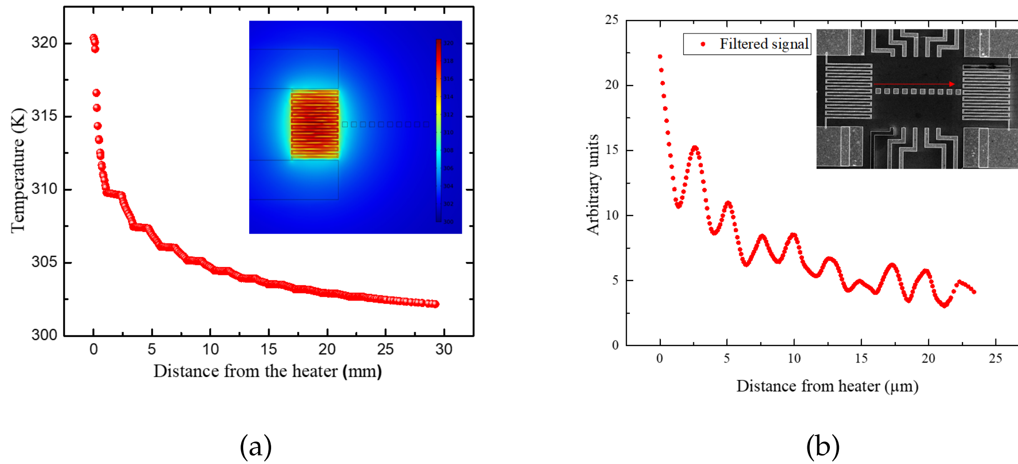


Figure 4.27: Temperature profiles obtained by COMSOL and thermal imaging shown next to each other. (a):The temperature profile calculated in the COMSOL model. (b): The temperature profile obtained by thermal imaging of the device which the SEM image is depicted in the upper right corner.

4.4.2 The Seebeck coefficient of InSb nanowires

Once the temperature profile of the device is known, it is possible to calculate the Seebeck coefficient. It is determined from the measured voltage offset and the temperature difference across the wire. Below room temperature measurements of the voltage shift have not been observed. This is likely due to a too low heating current combined with the decreased resistance of the gold heating element resulting a low heating power, therefore only Seebeck coefficient values of 300 K and above are measured. The temperature difference obtained with the thermometers is used if measurable, otherwise the COMSOL model is used. Seebeck coefficient values are plotted in figure 4.28 for temperatures ranging from 300 to 420 K. As with the electrical conductivity no clear diameter relation between the the Seebeck coefficient values is found. The highest absolute Seebeck coefficient value of (-0.265 ± 0.007) mV/K is found for a 160 nm diameter wire. This value is close to but smaller than the bulk value of -0.3 mV/K at 300 K [26]. No absolute increase of the Seebeck coefficient with decreasing diameters in the range from 160 nm to 81 nm is observed. This contradicts theoretical predictions made by early models based on single band transport [5]. Improved models of thermoelectric performance that take into account multiple-band transport predict absolute increases in the Seebeck coefficient as the diameter of the nanowires generally decreases below the diameters measured in this report. [14, 13].

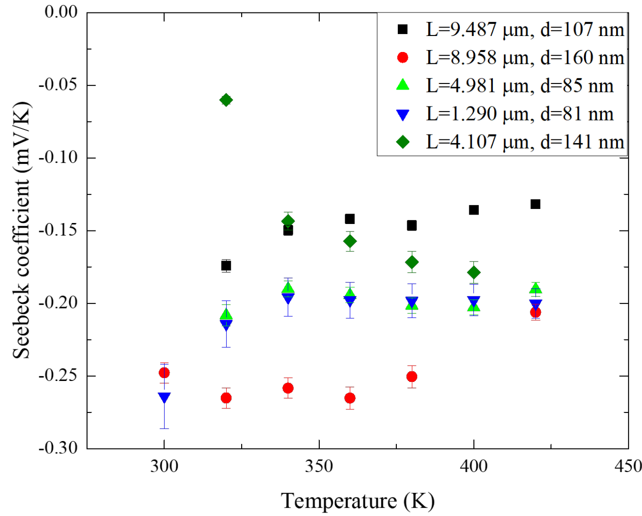
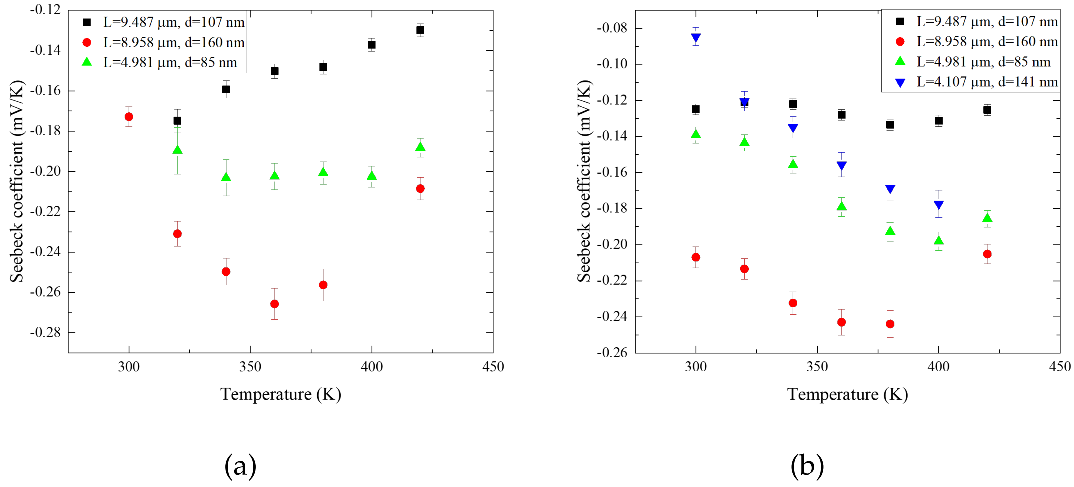


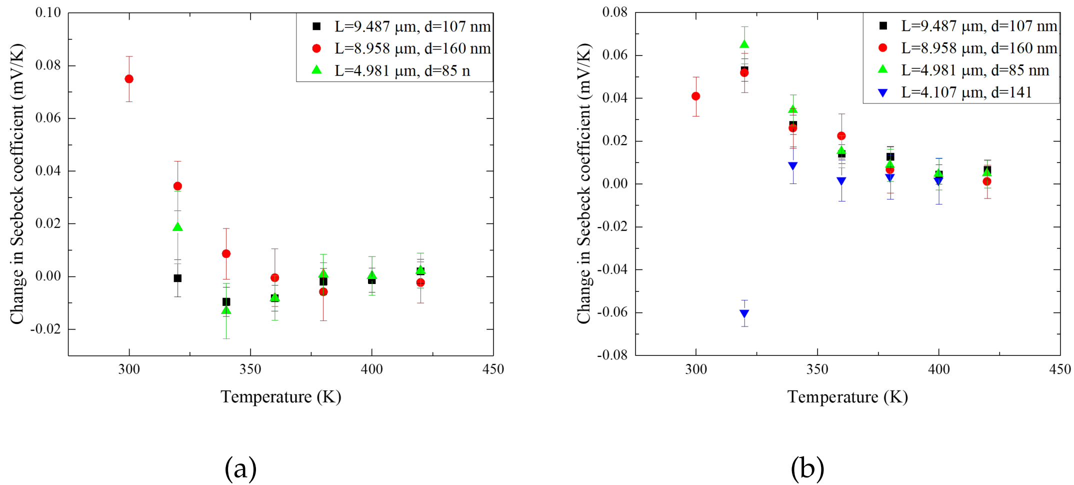
Figure 4.28: The Seebeck coefficient of several InSb nanowires plotted for temperatures ranging from 300 to 420 K.

The influence of the field-effect on the Seebeck coefficient is also measured and shown in figures 4.29a and 4.29b for an applied back-gate voltage of -15 V and 15 V respectively. There seem to be small changes in the Seebeck coefficient with respect to values obtained with no field-effect. This is further shown in figures 4.30a and 4.30b where the the change in the Seebeck coefficient is plotted. For a -15 V back-gate voltage the Seebeck coefficient becomes smaller or stays roughly the same whereas for a 15 V back-gate voltage the Seebeck coefficient generally becomes less negative by 0.02 mV/K. A theoretical curve from [31] is compared with the measured values of the Seebeck coefficient and the conductivity in appendix F



(a) (b)

Figure 4.29: The Seebeck coefficient measured under the influence of the field-effect plotted for temperatures ranging from 300 K to 420 K. (a): Seebeck coefficient of InSb nanowires measured with an applied back- gate voltage of -15 V. (b): Seebeck coefficient of InSb nanowires measured with an applied back- gate voltage of 15 V



(a) (b)

Figure 4.30: The change in the Seebeck coefficient measured under the influence of the field-effect plotted for temperatures ranging from 300 K to 420 K. (a): The change in the Seebeck coefficient of InSb nanowires measured with an applied back- gate voltage of -15 V. (b): The change in the Seebeck coefficient of InSb nanowires measured with an applied back- gate voltage of 15 V.

4.4.3 Power factor of InSb nanowires

From the electrical conductivity and the Seebeck coefficient data the power factor: $S^2\sigma$ is calculated. The power factor is plotted for a range of temperatures in figure 4.31.The highest power factor value measured with no back-gate voltage applied

is (1.4 ± 0.2) mW/(m · K^2) at 420 K for a nanowire with a diameter of 160 ± 9 nm. The power factors measured here average to 0.4 mW/(m · K^2) comparable to the values found from other studies at similar temperatures [32].

As with the Seebeck coefficient which is strongly related to the power factor, no clear relation with the wire diameter is found. This can be seen figure 4.32 where the power factor is plotted against the diameter.

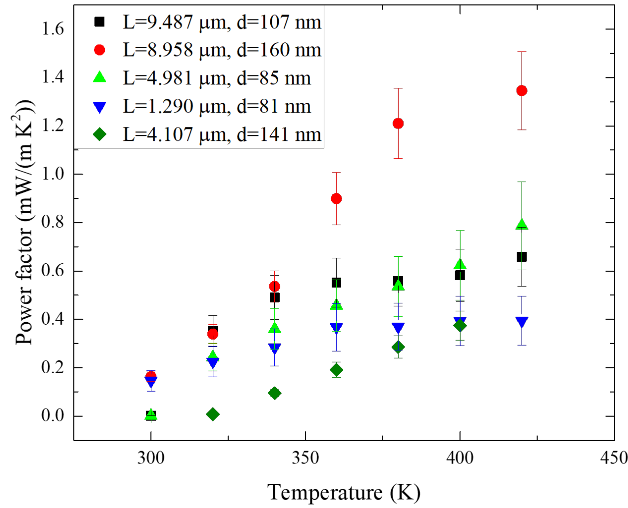


Figure 4.31: The power factor of several InSb nanowires plotted for temperatures ranging from 300 to 420 K.

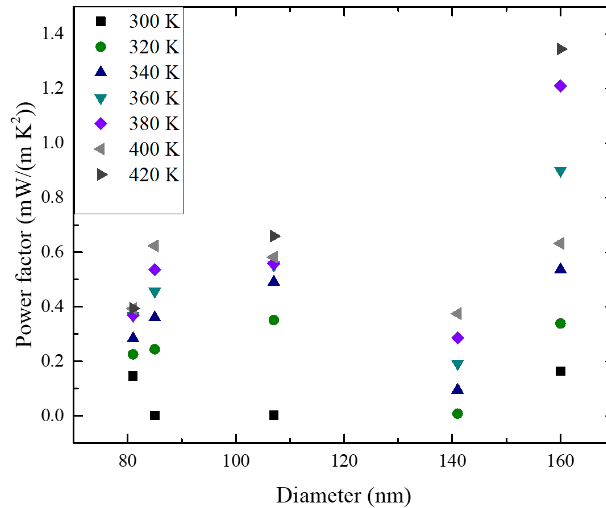
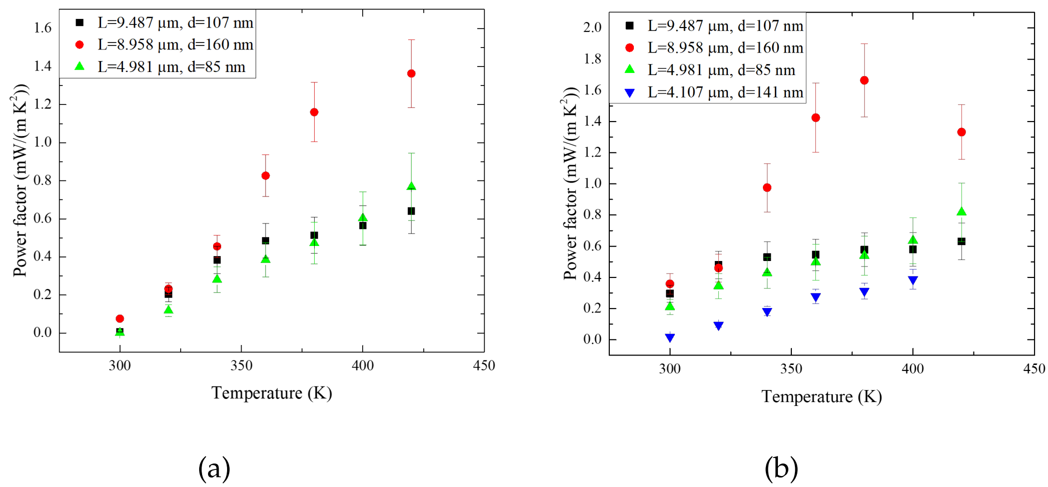


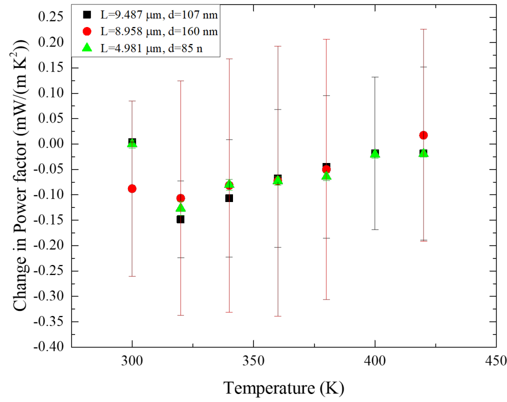
Figure 4.32: The power factor of InSb nanowires measured at temperatures from 300 to 420 K, plotted for their diameter. Error bars are left out to increase readability.

The influence of the field-effect on the thermoelectric performance is best seen in the power factor as both the electrical conductivity and the Seebeck coefficient are changed under it. The power factor calculated with an applied back-gate voltage of -15 V and 15 V is shown in figures 4.33a and 4.33b, respectively. Applying a positive gate voltage of 15 V leads to an increase of the power factor which can be further seen in figure 4.34b where the change in power factor is plotted due to a positive gate voltage. The highest measured value of the power factor is then $(1.70 \pm 0.2)\ \mathrm{mW}/(\mathrm{m} \cdot \mathrm{K}^2)$ at 380 K. This increase is mainly due to the increased electrical conductivity when a positive gate-voltage is applied. The relatively largest increases in the power factor are also observed around room temperature due to the increased conductivity.

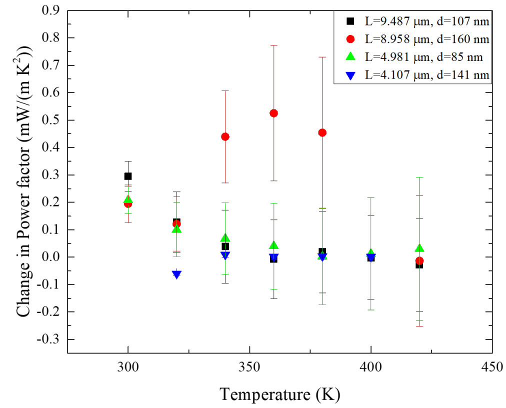


(a) (b)

Figure 4.33: The power factors calculated with field-effect modulated values. (a): Power factor of InSb nanowires measured with an applied back- gate voltage of -15 V. (b): Power factor of InSb nanowires measured with an applied back- gate voltage of 15 V



(a)



(b)

Figure 4.34: The changes in power factor by applying a back-gate voltage. (a): Change in power factor of InSb nanowires measured with an applied back- gate voltage of -15 V. (b): Change in power factor of InSb nanowires measured with an applied back- gate voltage of 15 V

5 Conclusion and outlook

Solid state thermoelectric generators can contribute to increasing the efficiency of processes by converting waste heat to electrical energy. Currently the efficiency of these devices needs to increase to become commercially viable. InSb nanowires are theoretical candidates to achieve this goal. In this report I-V scans and back-gate voltage sweeps are performed on FET devices containing n-type InSb nanowires. From these measurement thermoelectric and electrical properties are determined. Measurements are done for temperatures from 6 to 420 K to obtain a complete overview.

A temperature profile over the measurement device due to an on-chip heating element is established. This profile is measured by two independent measurement techniques: resistance thermometers and thermal reflectance imaging methods. A COMSOL model is also used to calculated the profile and is compared with the measurements.

With the temperature profile known, the Seebeck coefficient is measured for temperatures from 300 to 420 K. The highest absolute value is found to be (-0.265 ± 0.007) mV/K at 380 K, which is comparable to values found in literature [32], but below the bulk value of -0.3 mV/K [26]. Signs of an increase of the absolute value with decreasing wire diameters are not found. This indicates that the diameter of the nanowires might need to decrease, below the smallest diameter of 81 nm measured in this report, to observe the expected improvements. The field-effect is found to have no significant influence on the Seebeck effect at room temperature and above, when a back-gate voltage of -15 V and 15 V is applied.

From the performed back-gate voltage sweeps the mobility and the carrier concentration of the InSb nanowires are determined. The highest electron mobility found is $(5.5 \pm 0.2) \cdot 10^3 \mathrm{cm}^2/(\mathrm{V} \cdot \mathrm{s})$ The electron mobility is comparable to some studies [27] are in the same order, but significantly lower than more recent studies and bulk values of InSb [6].

The carrier concentration of electrons in the nanowires is calculated in the order of 10^{-18} which is in line with theoretical predictions [30].

The n-type wires are ambipolar meaning that have electrical conductivity facilitated by electrons and holes. The highest electrical conductivity found is $(35 \pm 6) \cdot 10^3$ S/m at 420 K. An overal increase of the conductivity compared to the wires of the previous generation [22] is seen. No correlation between the diameters, ranging from 81 to 160 nm, and the conductivity is seen in the measurements. A large influence of the field-effect on the conductivity is observed at room temperature. The conductivity increases significantly with an applied gate voltage of 15 V.

The Seebceck coefficient and the conductivity values are used to calculate the power factor: $S^2\sigma$. The highest value is calculated as (1.70 ± 0.2) mW/$(\mathrm{m} \cdot \mathrm{K}^2)$ at 380 K with an applied back-gate voltage of 15 V. The average power factor values are around 0.4 mW/$(\mathrm{m} \cdot \mathrm{K}^2)$ which is comparable to other studies [32]. The power factor is found to increase in the temperature range from 300 to 360 K when a back-gate voltage of 15 V is applied. This increase is attributed to the increased conductivity in the same temperature range.

The current devices allow for extraction of the properties of InSb nanowires under the influence of a back-gate voltage. Increasing the current through the heater element should also make it possible to measure the Seebeck effect below room temperature. Measurement conditions should also be regulated by letting the devices undergo thermal annealing at 420 K, enhancing the mobility and possibly other properties. The COMSOL model can be used to determine the temperature gradient across the nanowire, removing the need to use the resistance thermometers. This should increase the durability of the nanowires. Follow up studies should focus on measuring other promising nanowire materials or smaller diameter InSb wires as the theory suggests that these should have the largest increase of thermopower.

6 Acknowledgements

I would like to thank my daily supervisor Daniel Vakulov for all the work he has done for this project. Specifically for creating the measurement devices, preparing the set-up, making SEM images, assisting me during the measurements and measuring when additional data was needed and finally discussing the data and report with me. I would also like to thank Prof.Dr. Erik Bakkers for giving helpful comments during the progress meetings.

Appendix A. Uncertainty analysis

A.1 Electrical conductivtiy

The uncertainty of the electrical conductivity $d\sigma$ of is calculated from: the standard error in the resistance obtained from the linear fit dR, the uncertainty in the wire dimensions of the wire dl and dd for the length and diameter respectively. The uncertainty in conductivity is then calculated from the conductivity equation 12, as in equation 13. The uncertainty in the wire dimensions is taken as 9 nm as this value is found to be the smallest distinguishable length in the SEM images.

$$\sigma = \frac{8\mathrm{l}}{3\sqrt{3}\mathrm{d}^2\mathrm{R}} \tag{12}$$

$$\mathrm{d}\sigma = \sqrt{\frac{64\mathrm{dR}^2\mathrm{l}^2}{27\mathrm{d}^4\mathrm{R}^4} + \frac{64\mathrm{dl}^2}{27\mathrm{d}^4\mathrm{R}^2} + \frac{256\mathrm{dd}^2\mathrm{l}^2}{27\mathrm{d}^6\mathrm{R}^2}} \tag{13}$$

A.2 Seebeck coefficient

The uncertainty in the Seebeck coefficient dS is calculated from equation 14. dV is the standard error in the voltage offset obtained from linear fits, whereas the error of ΔT: dT is the error in the temperature profile which is either taken as the error in the resistance thermometer data when it is used or taken as 0.1 K when the model is used. This value is based on the comparison of the model data with the resistance thermometer data and the thermal reflectance imaging.

$$dS = \sqrt{\frac{dV^2}{T^2} + \frac{dT^2V^2}{T^4}} \tag{14}$$

A.3 Power factor

The uncertainty in the power factor stems from the error in the Seebeck coefficient and the error in the conductivity. The calculated values for the previous section are used in equation 15:

$$dPF = \sqrt{S^4 d\sigma^2 + 4S^2 dS^2 \sigma^2}. \tag{15}$$

A.4 Mobility

The uncertainty in the mobility *dmob* is calculated according to equation 16. Here also the error is caused by the uncertainty of the wire dimensions: *dl* and *dd* and the fit error of the slope of the linear fit *dTc*. The error in the capacitance is not evaluated in this report.

$$dmob = \frac{\sqrt{\frac{d^2(d+\text{tox})\cosh^{-1}\left(\frac{2\text{tox}}{d}+1\right)^2\left(\text{dl}^2\text{Tc}^2+\text{dTc}^2L^2\right)+\text{dd}^2L^2\text{Tc}^2\text{tox}}{d^2\text{E0}^2\text{ep}^2(d+\text{tox})}}}{2\pi} \tag{16}$$

Appendix B. Conductance fit model

Following other work on mobility extraction from FET nanowire devices [19], the mobility of holes is determined and compared to the values obtained from the linear fit method used in this report. The model fitted with the conductance fit is given in equation 2.35. The mobility values are shown in figure 2.35.

$$G\left(V_g\right) = \left(R_s + \frac{L^2}{\mu C\left(V_g - V_{th}\right)}\right)^{-1} \tag{17}$$

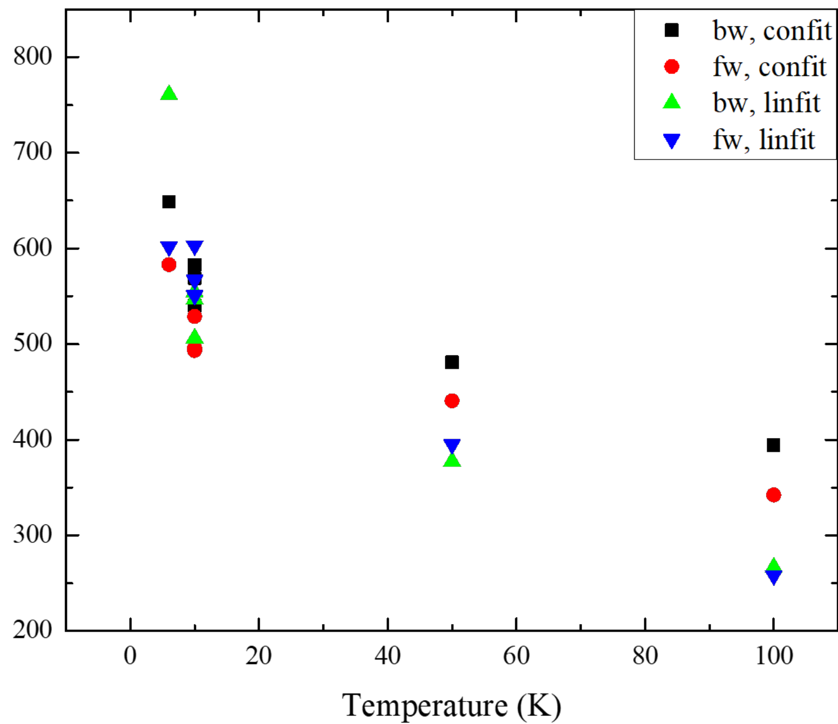


Figure 2.35: Mobility of holes plotted for a range of temperatures. Data obtained from two methods linfit is data from linear fit method and confit is data from conductance fit method. fw is forward sweep direction, bw is backward sweep direction.

Appendix C. Mobility of holes and electrons in InSb nanowires obtained by a backward sweep direction

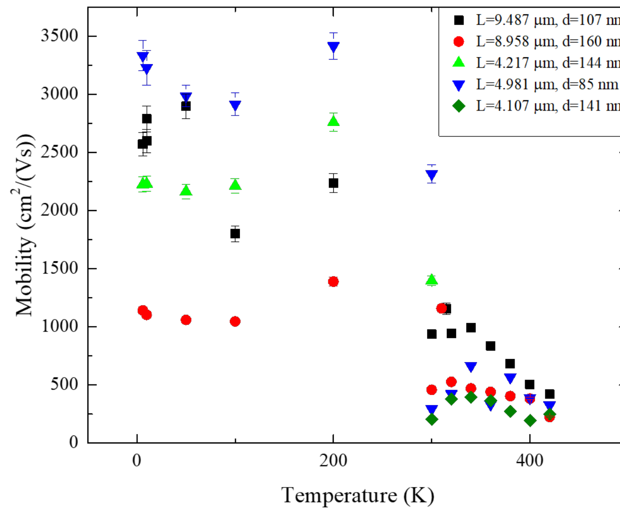


Figure 3.36: The electron mobility of several nanowires obtained by a backward sweeping back-gate voltage plotted for a range of temperatures from 6 K to 420 K

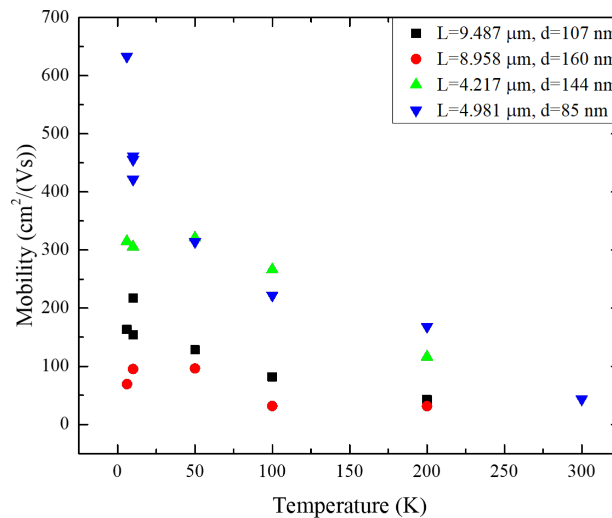


Figure 3.37: The hole mobility of InSb nanowires obtained from a backward back-gate voltage sweep, plotted for temperatures ranging from 6 to 420 K.

Appendix D. Carrier concentration of electrons in InSb nanowires obtained by a backward sweep direction

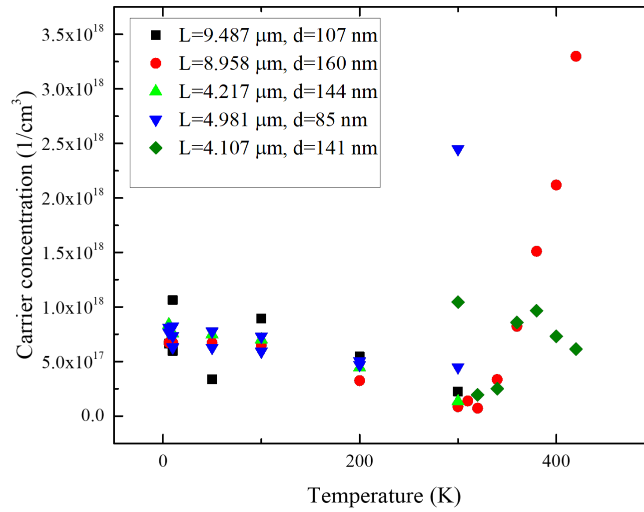


Figure 4.38: The carrier concentration of electrons in InSb nanowires obtained from the backward sweep direction plotted for temperatures ranging from 6 to 420 K.

Appendix E. SEM images of the InSb nanowires

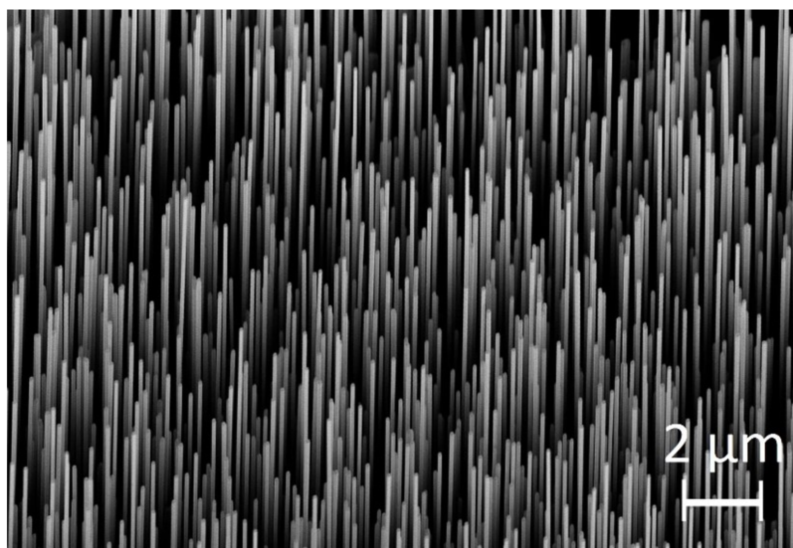


Figure 5.39: 45 °- tilted SEM image of an InSb nanowires array

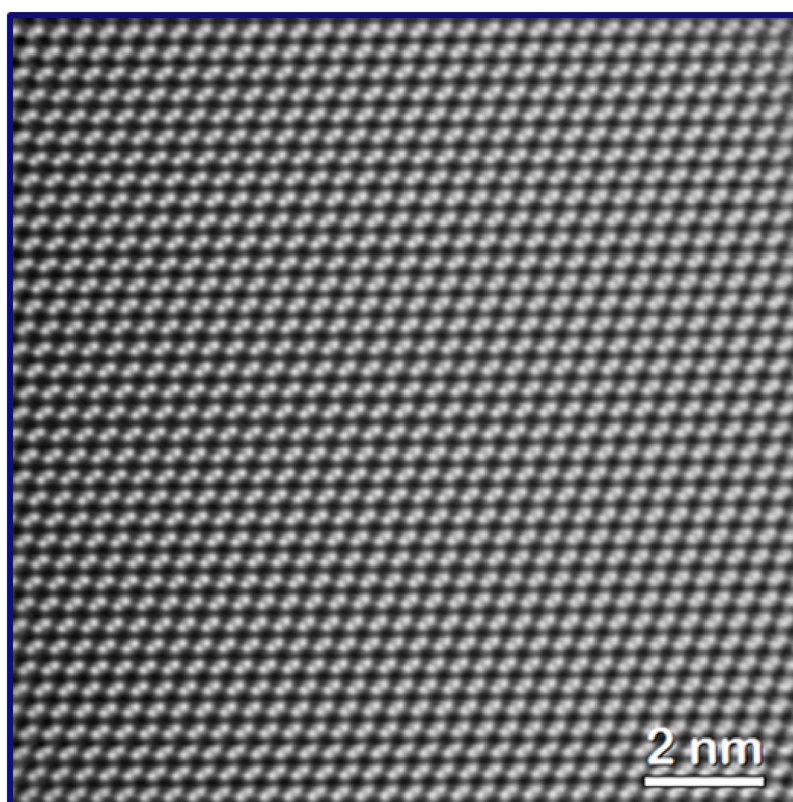


Figure 5.40: A high resolution TEM image showing zinc blende crystal structure of the InSb nanowires, and the absence of crystal defects.

Appendix F. Seebeck coefficient-conductivity curve

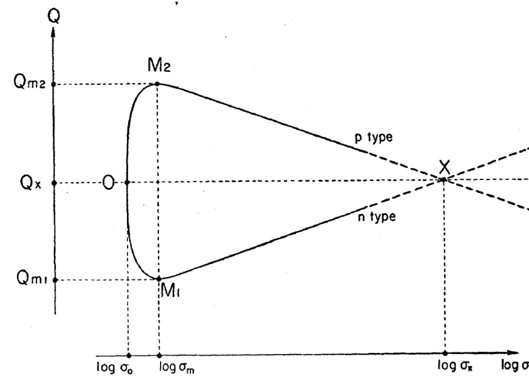


Figure 6.41: Theoretical curve from [31] where the Seebeck coefficient plotted against the conductivity

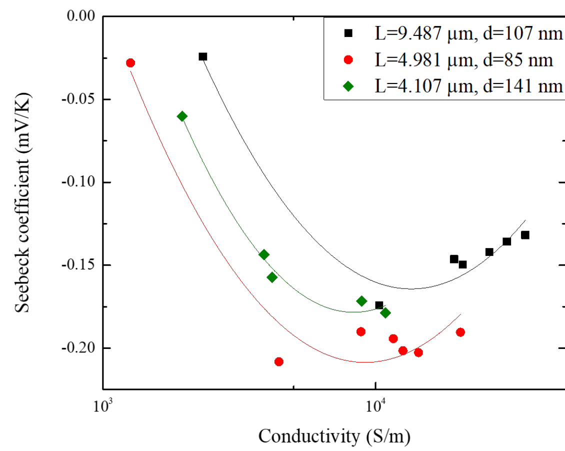


Figure 6.42: The measured Seebeck coefficient plotted against the conductvity of the nanowires.

Appendix G. Thermal reflectance set-up

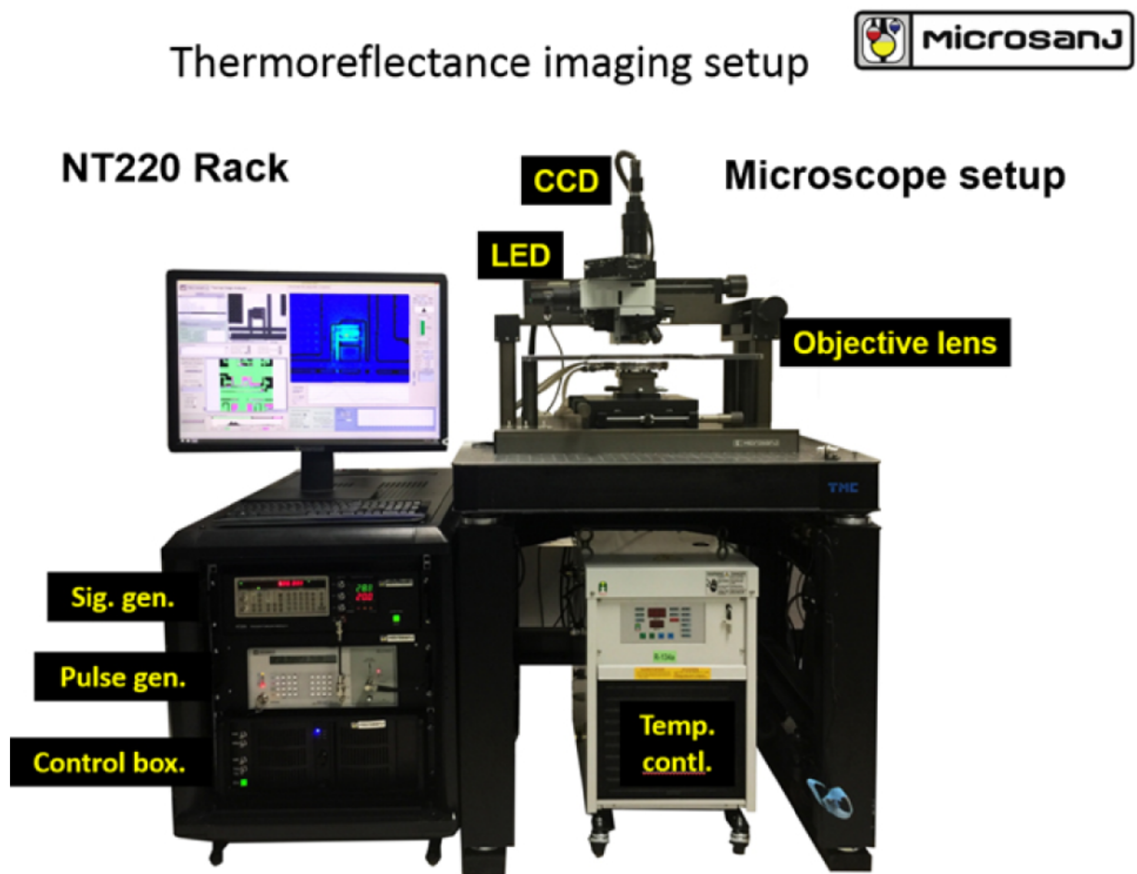


Figure 7.43: The Thermal reflectance set-up used in this project. Courtesy of Microsanj.

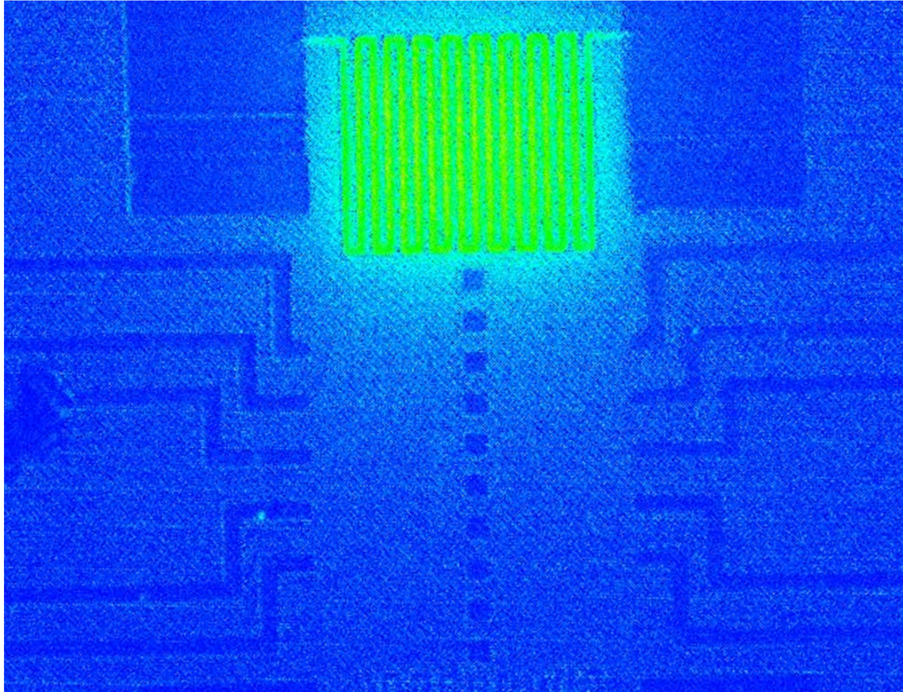


Figure 7.44: Thermal reflectance image of a device with gold squares.

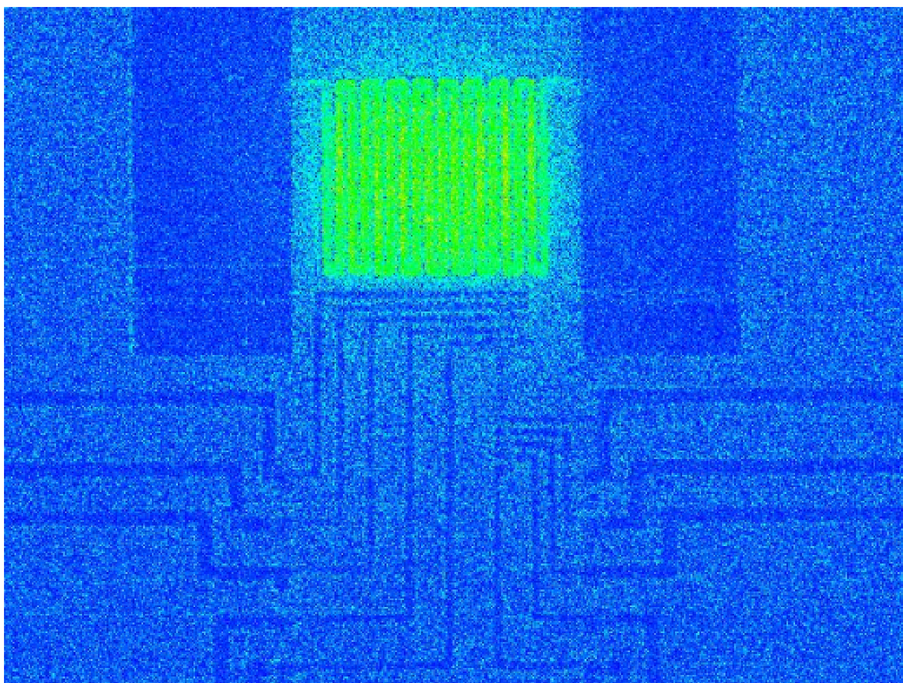


Figure 7.45: Thermal reflectance image of a device with nanowire and more gold contact lines than other devices measured.

Appendix H. Device fabrication steps

Step	
1	Spin 950K PMMA A11 2000RPM 30s, bake 180C 8 min
2	Nitride RIE, 7 min SWG recipe
3	BVR2000: 15nm Cr, 120nm Au
4	Acetone 30min
5	Polymer RIE PR etch 50W 1min
6	950K PMMA A6 3000RPM 30s, bake 180C 3min30s
7	EBL Main design
8	Develop: 80s MIBK:IPA for PMMA, 80s IPA
9	Descum: Polymer RIE PR etch 50W 10s
10	BVR2000: 15nm Cr, 120nm Au
11	Liftoff: 15min acetone vapor, 2h aceton, rinse with IPA
12	Transfer nanowires
13	SEM sample to find NWs
14	Polymer RIE PR etch 50W 1min
15	950K PMMA A6 3000RPM 30s, bake 180C 3min30s
16	EBL contacts
17	Descum: Polymer RIE PR etch 50W 5s
18	Sulphur passivation/ Other passivation
19	BVR2000: 15nm Cr, 200nm Au
20	Liftoff: 15min acetone vapor, 2h aceton, rinse with IPA

Figure 8.46: The steps performed to make the nanowire FET device

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