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Nanowire substrate fabrication

a comparison between reactive ion etching and wet etching with BHF of InP substrates with ZEP520A resist and SiNx masks for gold catalysed nanowire growth

Immel, Sam

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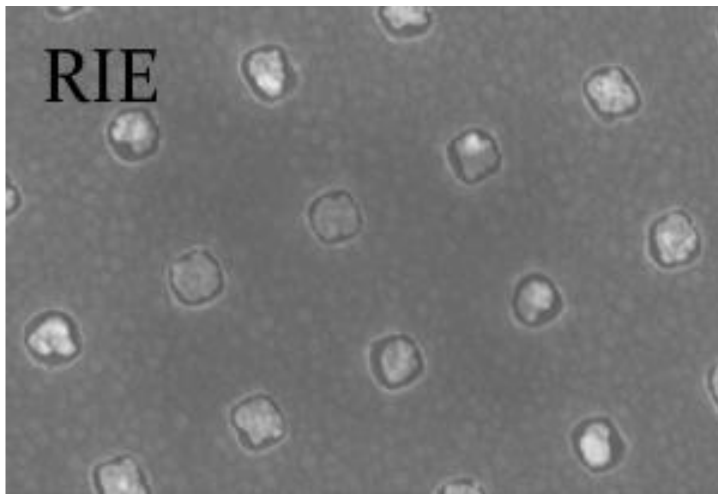
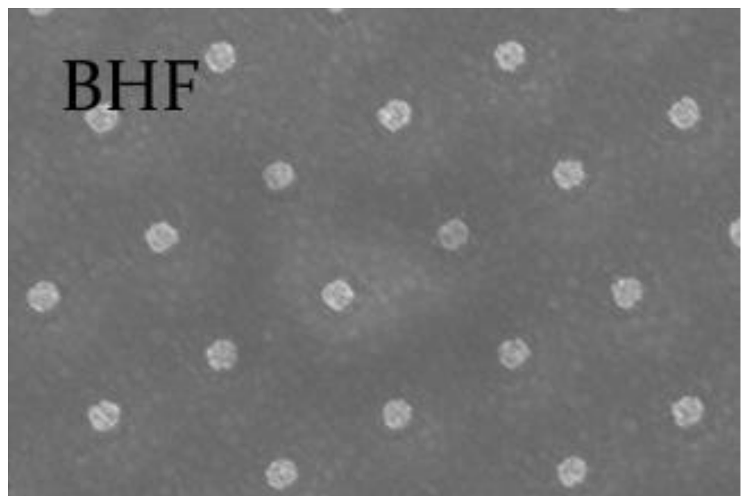
Nanowire Substrate Fabrication:

A comparison between reactive ion etching and wet etching with BHF of InP substrates with ZEP520A resist and SiN_x masks for gold catalysed nanowire growth





Sam Immel
0912367
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Abstract

In this experiment, three wet etched nanowire substrate samples and one dry etched nanowire substrate sample are compared. The wet etched samples were etched with buffered hydrofluoric acid. One of the wet etched samples shows strong signs of under-etching, while another one shows signs of over-etching. The third sample shows good results in terms of hole yield, the hole diameter however is a lot larger than intended. The dry etched sample was etched through reactive ion etching and differs distinctly from the wet etched samples. The general conclusion of this report is that further experiments with more samples are to be conducted in order to draw more solid conclusions regarding the cause of the final quality and yield of the holes from which the nanowires are grown.

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1. Introduction

The goal of this report is to analyse the difference between nanowire substrate samples which underwent wet etching with BHF and a nanowire substrate sample which underwent reactive ion etching. The main motivation behind this research is to give a basic overview of the nanowire substrate fabrication process as well as some general differences between the two etching techniques. What makes the fabrication of nanowire substrates so intriguing is that through conducting countless experiments, in which the many parameters involved across all different fabrication steps are fine-tuned, eventually a well-defined and reproducible recipe emerges. Through this, more insight is gained in the fabrication process and thus the door for nanowire technology to be implemented on larger, industrial scales opens a bit more.

The report is built up as follows: first, the theory is addressed, in which each step in the fabrication process is explained, and also contains a short elaboration on the management of particles in a cleanroom. Next, the methodology of the process is described, in which process parameters and techniques are defined. Then the results, in the form of scanning electron microscope (SEM) images, are shown and discussed. Finally there is a conclusion in which final conclusions are drawn regarding the experiment. Furthermore, future research is suggested and critique is given on the current experiment. Extra SEM images are added in the appendix.

2. Theory

2.1 Particles in a Cleanroom

The cleanroom, in which the sequential processes regarding the manufacturing of the nanowire substrate are done, is a class 1000 cleanroom. This means that in one cubic foot, approximately one thousand 0.5 micron diameter particles are present. A vertical laminar air flow is present throughout the entire cleanroom. This vertical flow significantly decreases the amount of horizontal vortices. This means that any particles dispersed, from for instance skin, will not be able to travel horizontally but are transported out of the room through the floor into a filter. Thus, the flow prevents many particles from contaminating nearby samples. The air flows in through grates in the ceiling and exits the room through holes in the floor. It then goes through a filter system. In the space between the inner and outer walls of the cleanroom, the air is led upwards again.

2.2 Cleaving

A wafer can be cleaved in multiple directions, for instance along the [100] plane or the [111] plane. The planes are indicated by a major flat and a minor flat. Which one is which, is indicated by the manufacturer of the wafer in question. When a small cut is made along the aforementioned planes with a cleaver, the cut propagates to the other side of the wafer, effectively cutting it in two. In general, the edges of cleaved silicon wafer pieces will be significantly less smooth than the edges of cleaved III-V wafers. The reason for this is that the silicon atoms in the cutting plane are not as well aligned as atoms of III-V materials.

2.3 Cleaning

RCA Cleaning Procedure

The most general method of cleaning a wafer was developed in 1965 by Werner Kern and is called the RCA clean [1], named after the Radio Corporation of America where Kern was employed at the time. The RCA clean consist out of 3 separate steps: standard clean no. 1 (SC-1), an oxide clean, and standard clean no. 2 (SC-2).

In SC-1 organic residues are removed from the wafer. This is done in a 5:1:1 H_2O:NH_4OH:H_2O_2 solution at a temperature of approximately 80 °C for 10 minutes. The wafer is then quenched under running deionized (DI) water for 1 minute and finally left in DI water for another 5 minutes. Due to the nature of the used solution, a thin oxide layer, originating from the peroxide, of about 1 nm is formed on the wafer surface. Furthermore, a certain amount of metallic contamination is deposited. Both of these layers are removed in the sequential steps.

In the oxide removal step, quite logically, any oxides are removed from the wafer. In this step, the wafer is put into a 1:50 HF-H_2O solution for 15 seconds. In these 15 seconds, the fluoride atoms react with the oxide effectively removing it. After the 15 seconds, the wafer is to be immediately transferred into running DI water in which it is moved around to remove the HF from the surface as quickly as possible in order to prevent further undesired damage.

The final step, SC-2, is a heavy metal clean in which any ionic contaminants are removed. The wafer is immersed in a 6:1:1 H_2O:HCl:H_2O_2 solution for 10 minutes at again approximately 80 °C. The wafer is then quenched in running DI water for 1 minute and left in DI water for another 20 minutes. It should be noted that in this step too, a thin oxide layer is formed. However, it now acts as a passivation layer, protecting the wafer from further contamination.

Deionized Water and Ionic Contamination

Every wafer cleaning step in the RCA process as well as in general include the use of DI water. The reason why this water is suitable in these processes is because it is highly purified and therefore almost completely exempt from any ionic, particulate and organic contaminations. The resistivity of the water is an indicator for the level of ionic contamination contained in it and therefore the ionic contamination can be measured accordingly. The theoretical limit for the resistivity of DI water at 25 °C is 18.3 Mohm-cm [2] , at which the water contains no ionic contaminants at all.

2.4 Barrier Layer Characteristics and Application

Barrier Layer

The barrier layer, or mask layer, is the first layer to be deposited onto a wafer destined to be covered by millions of nanowires. One possible barrier layer material is silicon nitride. It is this layer that separates the deposited gold dots from which the nanowires are to be grown, as shown in figure 1. The reason for the use of the silicon nitride layer is that any nanowire precursors which are deposited on it during the nanowire growth process will diffuse towards the holes with the gold. Evidently, the lack of such a layer would result in so-called parasitic growth, i.e. unintended nanowires with differing lengths and diameters at random positions, all over the wafer surface.

Figure 1: Schematic of a wafer just before the gold catalysed nanowire growth process.

PECVD

A method to deposit the barrier layer onto the wafer is by the use of Plasma Enhanced Chemical Vapour Deposition (PECVD). PECVD is a type of CVD which uses plasma [3]. This plasma gives PECVD a number of advantages over other forms of CVD. The first advantage is that PECVD requires a lower temperature in order to work: 300-350 °C. This results in a less temperature dependent process, ultimately leading to a more uniform layer. During a PECVD process a lot of ion bombardment takes place as well. More ion bombardment has shown to have mostly positive effects on the process: the film shows good adhesion, pinhole density is low and there is good step coverage. These reasons, as well as some others, are what led to the wide use of PECVD. A schematic of a PECVD reactor is shown in figure 2.

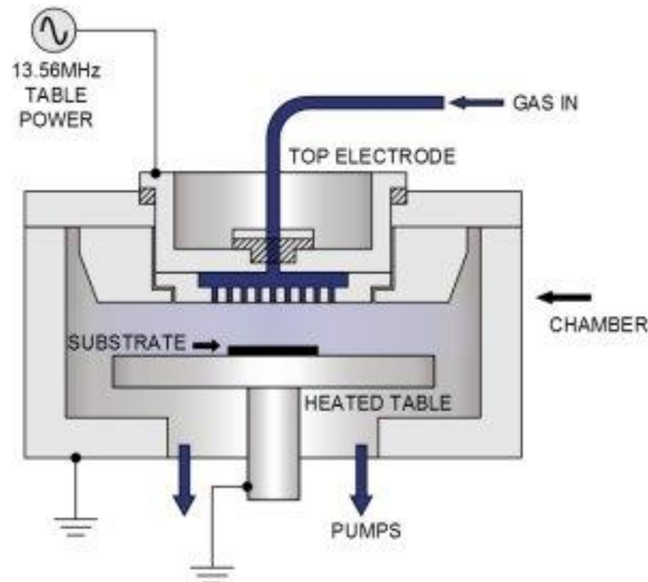


Figure 2: Schematic of a PECVD reactor. Source: https://www.oxford-instruments.com/products/etching-deposition-and-growth/plasma-etch-deposition/pecvd

Different reactor parameters have influence on the ultimate film quality and characteristics. Firstly, a lower pressure inside the reactor leads to a longer mean free path. This in turn allows for the ions, generated by the plasma, to gain more energy before impact with the sample surface and thus the effects of ion bombardment are more defined at lower pressures. Furthermore, experimental results show that at lower pressures the film density is increased, and therefore etch rates are decreased, and the stress in the film changes from tensile stress, leading to concave bending of the sample, to compressive stress, resulting in convex bending of the wafer.

Another parameter is the RF frequency used to generate the plasma. When the RF frequency is below the ion-transition frequency at approximately 3 MHz, at which the ions can still keep up, the ions experience the full amplitude, whereas at frequencies above 3 MHz the ion energy is determined by the time average of RF amplitude. Consequently, lower frequencies again result in a more pronounced bombardment effect and thus results in lower compressive stresses, lower etch rates and higher film densities.

An increase in RF power also yields more intense ion bombardment since the ion current is increased. At higher ion currents however, the deposition rate is faster as well. It is therefore that, rather than just the RF power, it is the ratio of power density and deposition rate which is to be evaluated in order to separate the effects of RF power on film quality on the one hand and growth rate on the other. From these parameters one can then conclude at which RF power level the film density is highest, and thus where the wet etch rate is lowest.

A final parameter is the temperature. A lower temperature results in a lower diffusion rate on the sample surface compared to the deposition rate of film precursors. The precursors are therefore more likely to form an amorphous film. Vice versa, a higher reactor temperature leads to the formation of a single crystalline structure. It is for this reason that PECVD, at typically 300-350 °C, yields higher quality films than for instance sputter deposition, which occurs at lower temperatures (< 200 °C).

2.5 Resist Spinning and Soft Baking

Resist types

There are two types of resists: positive resists and negative resists. Positive resists, when exposed to an electron beam, or light in case of photosensitive resists, have the crosslinks between the resist molecules broken by said beam. On the other hand, aiming an electron beam or light beam at negative resists causes them to crosslink at the exposed areas. Since this report mainly focuses on the use of positive electron beam sensitive resists, these resists will mainly be elaborated on.

Two examples of positive, electron beam sensitive resists are PMMA and ZEP520A with buckyballs, both polymers, as shown in figure 3, and each with their own set of characteristics. The PMMA resist comes in several variations regarding molecular weight and concentration. One particular type is 950-PMMA A2, in which the 950 indicates its molecular weight in kilo Daltons and A2 defines that there is 2% PMMA dissolved in a solvent called anisole. Some differences between PMMA and the ZEP resist with buckyballs, or ZEP C60, are their application methods and the soft baking step following after the resist has been spun onto the wafer. When applying PMMA, a regular pipette suffices, whereas ZEP requires the use of a syringe with a filter on it. The reason for this is that the buckyballs in the ZEP resist agglomerate. The filter, only allowing very small diameter particles to pass through, sees to it that the buckyballs are separated before the resist is applied to the wafer. Furthermore, whereas PMMA only requires a single heating step during soft baking, ZEP C60 needs two in order for the resist to harden as intended, the time periods of which are also specified by the manufacturer and are to be followed closely.

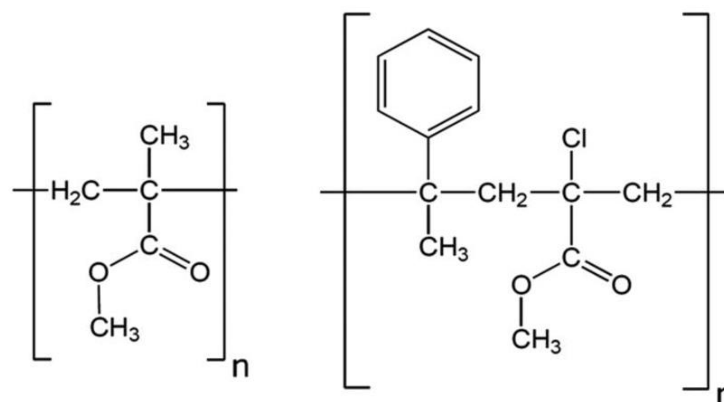


Figure 3: The PMMA monomer on the left and the ZEP monomer on the right. source: https://www.researchgate.net/figure/252200660_fig1_left-PMMA-and-right-ZEP-polymer-structures

Resist Spinning

The spinning process works as follows: after having placed the wafer onto a chuck, or mount, and having applied the resist to the wafer with either a pipette or syringe, the wafer is held in place by applying suction to it through a channel in the chuck. The wafer is then rotated at high speeds, typically some 1000-6000 rpm for thirty seconds or one minute, during which the resist is uniformly spread over the wafer surface. The relation between rotation speed and resist thickness is specified in spin curves supplied by the manufacturer of the resist. The spin curves for 950 PMMA are shown in figure 4.

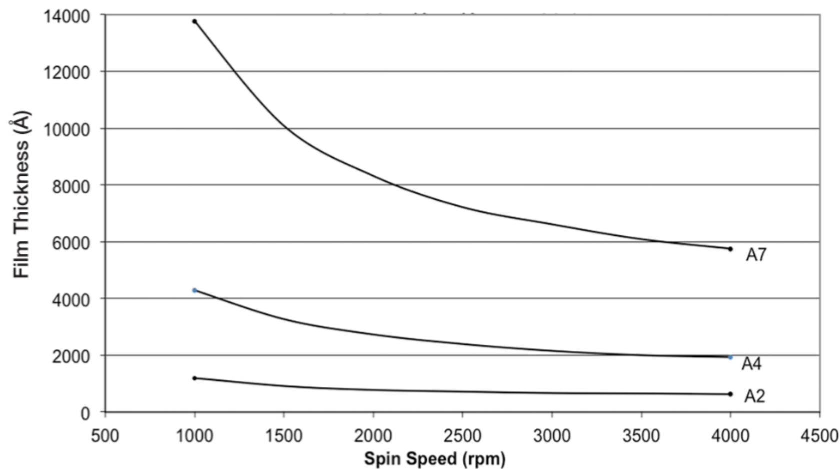


Figure 4: Spin curve for 950 PMMA. Source: http://microchem.com/pdf/PMMA_Data_Sheet.pdf

It should be noted that these spinning curves are only valid for whole wafers which were fully covered with resist before the beginning of the spinning process. When applying resist to smaller wafer pieces, the smallest viable for spinning being as small as 1x1 cm as determined by the chuck size, their shape as well as their size influence the final resist thickness and uniformity as edge effects play a significantly more important role.

Soft Baking

Soft baking, or prebaking, is the step sequential to resist spinning. During this step the adhesion of the resist is improved and any solvent still present in the resist is removed, hardening it. Typical times range from 10 minutes to half an hour. The temperature depends on the method of heating: in the case of an oven, typical temperatures range from 80 °C to 200 °C depending on the resist type, whereas when a hotplate is used, temperatures are notably higher since the sample is heated only from the bottom.

2.6 Electron Beam Lithography

Concept

Electron Beam Lithography (EBL) is a crucial step in the fabrication of nanowire substrates, since it allows for the writing of structures on the substrates. This is done by exposing the resist layer, either positive or negative, to an electron beam. In the case of a positive resist, the cross-links are broken in the exposed area, whereas, when dealing with a negative resist, the exposure to the electron beam actually causes the resist to cross-link.

The final result of the features created on a substrate through EBL are dependent on a large number of parameters. This intricate system of interconnections [4] between the quality and resolution of the features and the parameters will be elaborated on next as well as in section 2.7. First however, four electron transport phenomena are discussed.

Electron Transport Phenomena

In order to gain a better understanding of the influences of the EBL parameters, one should be aware of a number of electron transport phenomena within the sample, each of which are sketched in figure 5.

Firstly, there is forward scattering: upon entering the resist layer, the electrons experience low-energy elastic collisions with the resist molecules. The consequence of this is that the electrons are deflected somewhat, resulting in beam broadening.

The second transport effect is backscattering: most electrons pass through the entire resist layer and continue to penetrate into the underlying layers. In these layers, the electrons collide many a time, effectively having their path redirected back into the resist layer microns away from where they first entered it and unintendedly exposing that area. This is called the proximity effect.

Next, secondary electrons are generated in the resist layer. These electrons are a consequence of ionization of resist molecules by the electron beam. Although the secondary electrons typically only have a low range of a few nanometres, the resolution of EBL could ultimately be limited by this phenomenon.

Lastly, when dealing with insulating layers underneath the resist, electrostatic charge may build up at the bottom of the resist since there is no way for all the electrons to dissipate. This will disturb the path of newly incoming electrons and thus decrease the achievable quality and resolution of the features.

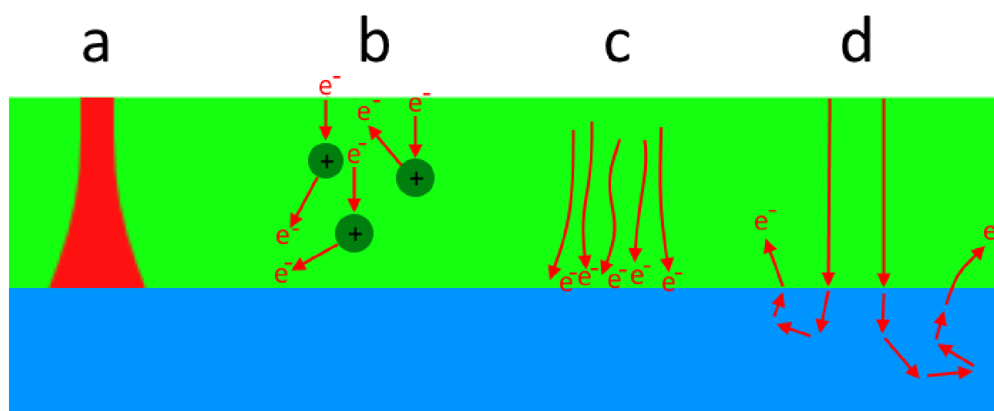


Figure 5: Four electron transport phenomena. a: forward scattering/beam broadening, b: secondary electrons, c: built-up electrostatic charge, d: backscattering/proximity effect. The green area is the resist, the blue area is an insulating silicon nitride layer.

Exposure Dose and Exposure Energy

The exposure dose, in units of C/m^2, indicates the number of electrons passing through the beam. The higher the dose, the higher its electron density. The exposure energy, with typical values of around 10 keV, is an indication of the kinetic energy of the electrons. In general, for a positive resist, using a higher exposure dose results in smaller sized resist fragments which in turn leads to a higher solubility in the developer allowing for higher quality features. However, a too high exposure dose, as well as a too high exposure energy, will lead to overexposure. Similarly, too small dosages and energy will result in underexposure. Figure 6 very roughly shows the effects of underexposure and overexposure as seen after development of the resist.

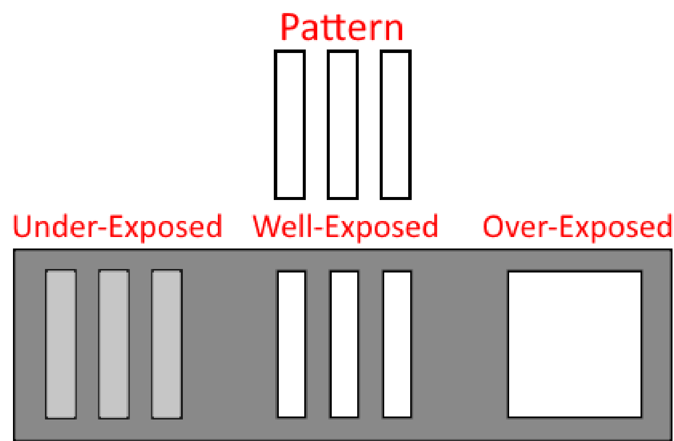


Figure 6: With underexposure, the resist layer cannot be removed entirely, leaving a thin layer of resist behind, whereas overexposure may ruin the intended patterns completely due to collapse of the walls between the trenches or actual exposure of the trenches.

Furthermore, an increase in the exposure energy causes a decrease in the collision cross-section of the electrons. In the case of a positive resist, this leads to less collisions per electron, effectively lowering the sensitivity of the exposed resist. This ultimately means a higher electron dose is necessary. However, an increase of the exposure energy also creates a wider dose window, i.e. a wider range of dosages can be used. This relation emanates from the fact that at larger exposure voltages, the electrons will not experience as much forward scattering, which in turn results in less beam broadening and thus a more concentrated beam of electrons.

Resist Characteristics

Besides the effects of the electron beam, certain characteristics of the resist also influence feature quality and resolution. Moreover, the appropriate exposure dosages and voltages change according to these characteristics. For instance, an increase in thickness of the resist results in more beam broadening. Furthermore, the denser the resist is, the higher the appropriate exposure dose and voltage. Lastly, there are various distinct differences between the use of a positive or a negative resist. One of these differences is that negative resists require overexposure since the crosslinking starts at the surface of the resist, making it harder for the electrons to penetrate and reach deeper into the resist. The consequence of this is that negative resists generally yield worse resolutions than positive resists.

2.7 Development

Process for PMMA and ZEP

After the desired pattern has been written onto the resist with EBL, the sample is developed. During this stage the areas which were exposed to the electron beam, which are now much more sensitive to the developer, are dissolved. Both dry development and wet development techniques exist. For this report, the sole focus will be on wet development in which the sample is immersed in a solution. One downside to wet development is that the resist tends to swell, a problem not encountered in dry development. During development, three solutions are used: a developer, a stopper and, if necessary, a rinsing solution. PMMA and ZEP each have their own developer and stopper. A widely used developer for PMMA is a 3:1 MIBK:IPA solution, a solution containing methyl isobutyl ketone and isopropyl alcohol. A stopper for MIBK:IPA is IPA itself. Since IPA is also used to rinse, development of PMMA requires no additional rinsing step. A general developer for ZEP is n-amyl acetate, a corrosive organic substance. And whereas MIBK:IPA is a developer for PMMA, it is the stopper for n-amyl acetate. In a third step, the MIBK:IPA is removed from the sample with IPA.

Correlation to exposure voltage and dose3

As mentioned in section 2.6, there is a strong correlation between the electron beam exposure dose and energy on the one hand and development time and temperature on the other [4]. For instance, at a development temperature of -10 °C the applicable dose window is significantly wider than at room temperature and thus allows for a higher resolution. However, a lower development temperature also causes the sensitivity of the resist to drop, hence creating a trade-off between resolution and sensitivity.

As for the development time, both the maximum and minimum applicable exposure doses go down for increased development time, while the dose window remains more or less stable. This is explained through the fact that if the developer is in contact with the resist for a longer period of time, it will affect not only the regions exposed to the ebeam for a longer period of time but also the unexposed regions.

2.8 Etching

With the desired holes now present in the resist layer, the underlying silicon nitride layer is ready to be etched. There are two types of etching: wet etching and dry etching. The wet etching technique described in this report is one including buffered hydro fluoric acid (BHF), whereas the dry etching method is reactive ion etching (RIE).

Wet Etching with BHF

During wet etching, the sample is immersed in a BHF solution, which consists of 1:7 $HF:NH_4F$. The fluoride atoms in the HF bond to the nitrogen atoms in the barrier layer causing the layer to be etched away. The ideal etching time depends on the thickness of the barrier layer and its density and is essentially experimentally determined. For instance, a barrier layer thickness of 25 nm requires an etching time of around 15 seconds. One second difference in etching time has dire consequences. A sketch of what the wafer looks like after the wet etching process is shown in figure 7. Since wet etching is an isotropic process, a so-called etch bias is created beneath the resist layer. In case of over-etching, the etching bias becomes larger, whereas in case of under-etching, the silicon nitride is not completely penetrated. If the barrier layer is made thinner, the etch bias becomes smaller since the exposed vertical area becomes smaller. Both the aforementioned PMMA resist as well as the ZEP resist are suitable for wet etching, whereas only ZEP is suitable for dry etching since PMMA is not resistant enough.

Figure 7: Sketch of wafer after wet etching process.

Dry Etching using RIE

The dry etching process takes place in a reactive ion etcher. Reactive ion etching, or RIE, is an etching technique involving both physical ion bombardment as well as chemical reactions between fluoride atoms and the barrier layer, similar to wet etching. The gases used during RIE are CHF_3 and , optionally, O_2. Once introduced into the chamber, the gas molecules are ionized, enabling them to collide with the sample as well as, in the case of the fluoride atoms, react with the barrier layer. Adding extra oxygen gas will make the etching process more aggressive than it would be when purely using CHF_3. The etching profile resulting from RIE differs somewhat from that resulting from a wet etch, as is made clear from their respective sketches. The RIE method induces almost no etching bias since it is a highly anisotropic process because the ions collide with the sample perpendicularly, leaving you with the profile as shown in figure 8. It should be noted that in the case of gold catalysed nanowire growth, the diameter of the wire is not determined by the diameter of the hole in the barrier layer but rather the hole in the resist. Unless the hole diameters become small enough at which point the gold shapes itself differently according to the hole diameter when turned liquid. In catalyst free growth however, the diameter of the nanowire always depends on the diameter of the hole. It is for this reason that RIE is the preferred method for catalyst free nanowire growth.

Figure 8: Sketch of wafer after dry etching process.

2.9 Evaporation: The Electron Beam Evaporator

Evaporators are used to deposit specified thicknesses of metal onto a substrate. One particular type of evaporator is the electron beam, or ebeam, evaporator. A sketch of this evaporator is shown in figure 9. In the e-beam evaporator, the metal which is to be deposited onto the samples is heated by an electron beam, which is bent and aimed at the evaporation material through the use of a magnetic field. The entire process takes place under very low pressure since any gases present in the chamber may cause a disruption. The evaporation material is heated up slowly during a number of steps. First there is a rising step, in which the power of the electron beam is gradually increased. The rising step is followed by a soak step, during which the beam power remains constant, allowing the evaporation material to adjust. Sequentially, another rise and soak step occur, bringing the beam to its intended power level. During this process, the electron beam spot circles over the evaporation material. The consequence of this process is that the evaporation material is heated isotropically and therefore yields better overall results.

After the top layer of the evaporation material, which contains possible contaminants, is deposited onto the shutter present between the material and the samples, the shutter opens and the metal is deposited on both the samples and a quartz crystal. In order to ensure isotropic deposition, the samples are continuously rotated as indicated in the figure.

The quartz crystal vibrates at its resonance frequency. This frequency changes the more material is deposited on the crystal. This allows for the deposited thickness to be monitored accordingly.

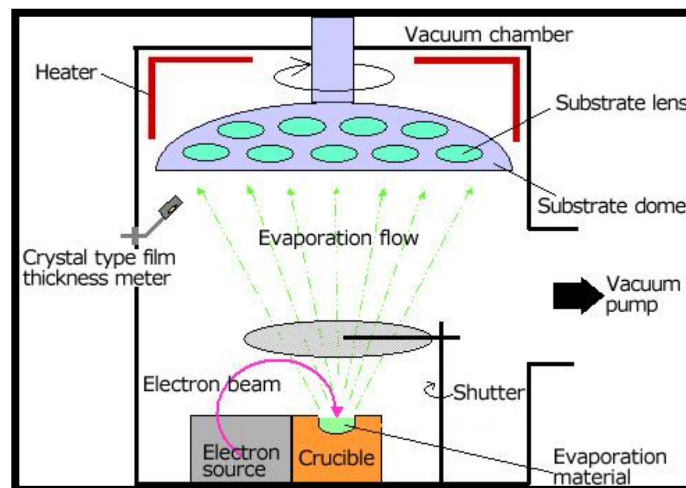


Figure 9: Sketch of an ebeam evaporator. Source: https://www.jeol.co.jp/en/science/eb.html

2.10 Lift-Off

The lift-off is one of the last steps in the nanowire substrate fabrication process. During this step, the resist is removed from the sample. This is achieved by putting the sample in a lift-off solution appropriate for the used type of resist. Once in the solution, the resist starts swelling and loses adhesion to the sample. To make the process more efficient, a magnetic steer bar can be added to the solution. Higher temperatures also help the process. However, one should take care when heating up a lift-off solution. For instance, in the case of acetone, heating up to above 50 °C will make it volatile. Moreover, when heating up positive resist stripper, or PRS, a reprotoxic substance, it may evaporate and end up in the air circulation and be inhaled. To remove the last residues of resist, a sonication bath filled with the same lift-off solution is used, which exposes the sample to ultra-sonic vibrations.

3. Methodology

The manufacturing process of the samples in this experiment will be discussed below per step. In figure 10, an overview is given of the entire process.

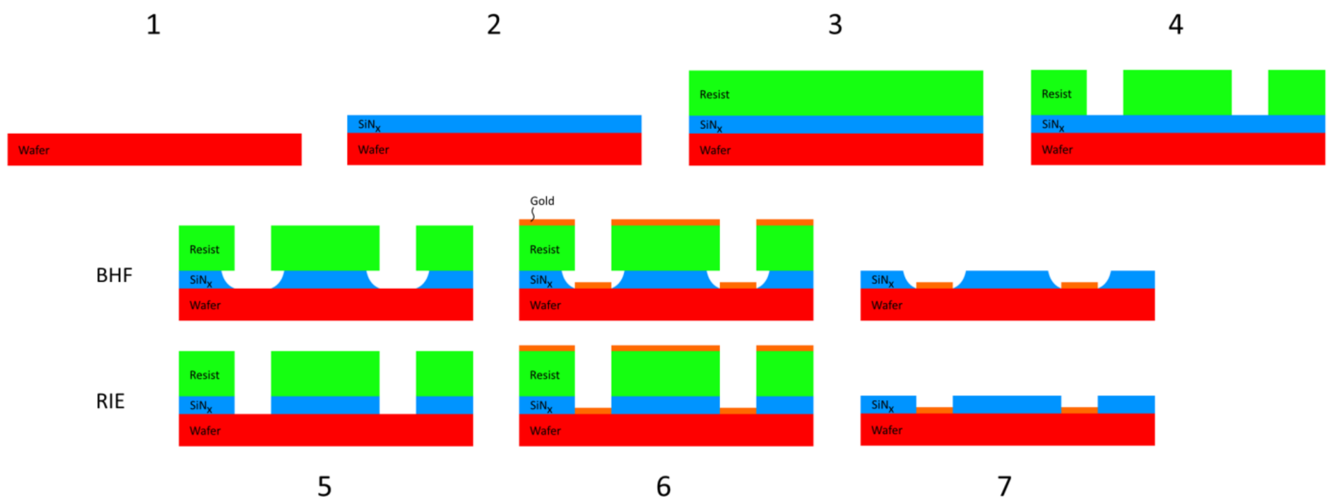


Figure 10: An overview of the manufacturing process. 1: a wafer is taken out of the box without cleaning procedures, 2: a silicon nitride layer is deposited onto the wafer by PECVD, 3: a resist layer is spin coated onto the SiN layer, 4: the resist is exposed to an electron beam and developed, 5: after the wafer has been cleaved into five samples, 2 samples are dry etched with RIE and 3 samples are wet etched with BHF, 6: gold is evaporated onto the resist layer and wafer, 7: the resist with gold on top is lifted off the sample.

3.1 PECVD

After having taken a new indium phosphide wafer out of the box, without any cleaning procedures, it is put inside the PECVD reactor. The used recipe is the 'SiN_wave guide_50nm' recipe which is stopped in time to reach a deposited SiN_x layer thickness of approximately 25 nm. The gases involved in this recipe are 17 sccm of SiH_4, 13 sccm NH_3 and 980 N_2. The nitrogen acts as a carrier gas in the process. The pressure is 650 mtorr, the high frequency power 20 W and the deposition time 100 s.

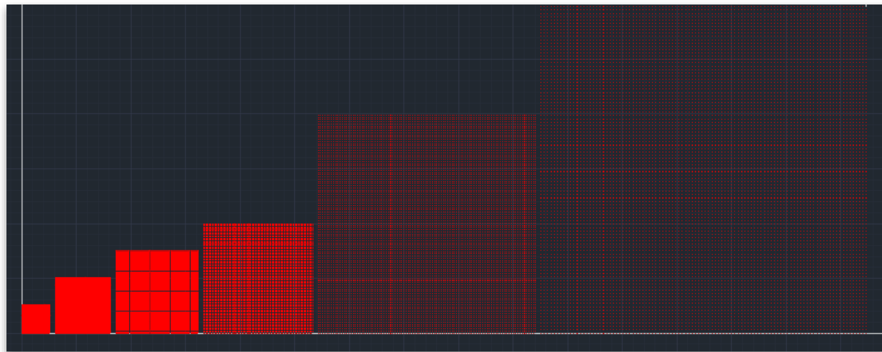
3.2 Resist Spinning and Soft Baking

The resist which is spin-coated onto the SiN_x layer is ZEP520A with buckyballs. This resist is known to work for not only for wet etching but also for dry etching, since the buckyballs strengthen the resist significantly, making it more resistant against ion bombardment. A syringe is used to apply the resist onto the wafer. The spin coat rotation speed is 2000 rpm and the recipe runs for 60 seconds. This yields a resist thickness of 100 nm.

After spin coating, the wafer is transferred to a hot plate with a temperature of 125 °C on which it remains for 4 minutes. The wafer is then transferred to a second hotplate having a temperature of 200 °C for an additional 2 minutes.

3.3 EBL and Development

During EBL, the wafer is exposed to an electron beam with an exposure dose of 1400-1900 µC/cm^2 and an exposure voltage of 100 kV. The pattern written onto the resist is shown below. The hole diameters are from red to light blue: 16 nm, 20 nm, 30 nm, 40 nm, 50 nm, 60 nm and 70 nm. The pitches between the holes are 250 nm, 500 nm, 750 nm, 1 µm, 2 µm and 3 µm.



After EBL, the wafer is immersed in the developer, n-amyl acetate, for 60 seconds while gently moving the wafer around. It is subsequently rinsed in a MIBK:IPA solution for 45 seconds and then rinsed in IPA for another 30 seconds. Lastly, the wafer is blown dry with an N_2 gun.

3.4 Cleaving

The wafer is now cleaved into smaller pieces using a scalpel. Four pieces are used in this experiment. After cleaving, any wafer residues are removed from the pieces using an N_2 gun.

3.5 Etching

Three out of four samples are used for wet etching. The samples are etched for 15, 20 and 25 seconds, respectively. After etching, the samples are immediately transferred into running DI water. In the DI water, the samples are moved around to remove the HF from the samples as fast as possible. After having moved around the samples for half a minute, they are left in the DI water for another 5 minutes. Although the resistance of the DI water has not been checked, the water had been running for at least 5 minutes.

The other sample is dry etched in the reactive ion etcher using the pure CHF_3 recipe for 150 seconds. The CHF_3 flow is 60 sccm, the forward power 50 W and the pressure 15 mtorr.

3.6 Evaporation

8 nm of gold was evaporated onto each of the five samples at a rate of 1 Å/s.

3.7 Lift-Off

During the first step of lift-off, the samples are immersed in PRS3000. The PRS is heated to 70 °C by the hotplate beneath the beaker and a stir bar is present in the beaker rotating at 380 rpm. The samples are left in the PRS for approximately 22 minutes. Next, the samples are immersed in acetone at room temperature inside a sonication bath for 5 minutes. The acetone removes the PRS residues. In order to remove the acetone residues from the samples, they are left to rinse in IPA for another two minutes.

3.8 Scanning Electron Microscope

Now that the samples are essentially ready for nanowire growth, nanowires will not be grown on them. Instead, they are examined in the scanning electron microscope, from which conclusions will be drawn regarding the comparison between dry etching and wet etching. The goal is to find all hole diameter fields (16 nm, 20 nm, 30 nm, 40 nm, 50 nm, 60 nm and 70 nm) at the 250 nm pitch and the 1 micron pitch.

4. Results and Discussion

4.1 BHF etch 15 seconds

Figure 11 shows the smallest diameter holes at the smallest pitch: 16 nm and 250 nm, respectively. The first conclusion drawn from this image is that the holes are not clearly visible. Furthermore, little to no gold was deposited in the holes since there are no visible white dots within the holes. Larger pitch fields were impossible to find since the larger the pitch becomes, the less densely populated the fields are. The 20 nm diameter field was similar to the 16 nm diameter field. It should be noted that the hole diameter, as mentioned beneath the figures, refers to the hole diameter as defined in the EBL pattern. The actual holes are in fact notably larger.

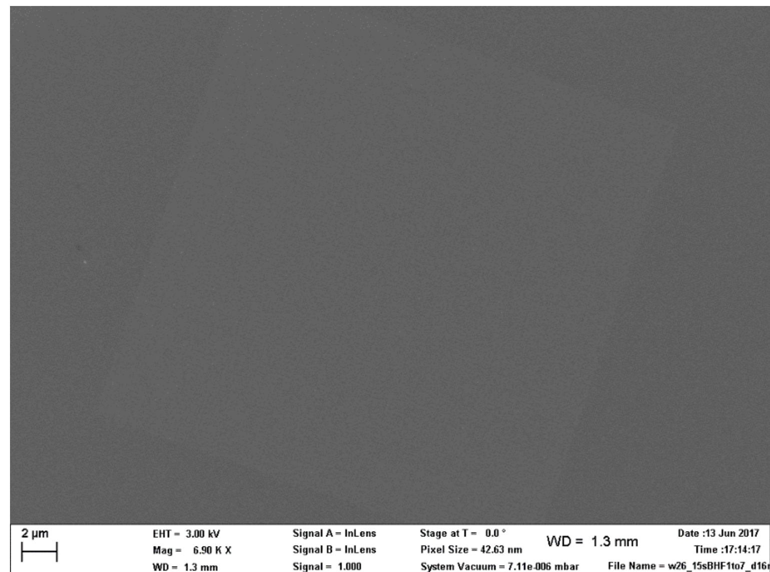


Figure 11: 16 nm diameter holes, 250 nm pitch

Figure 12 shows the 30 nm diameter field with again the 250 nm pitch. When comparing figure 12 with figure 11, one can conclude that, whereas there are no visible white specs in the 16 nm field, there is the occasional white spot in the 30 nm field. This indicates that a larger diameter allows for the holes to open more quickly and hence some gold was deposited within them.

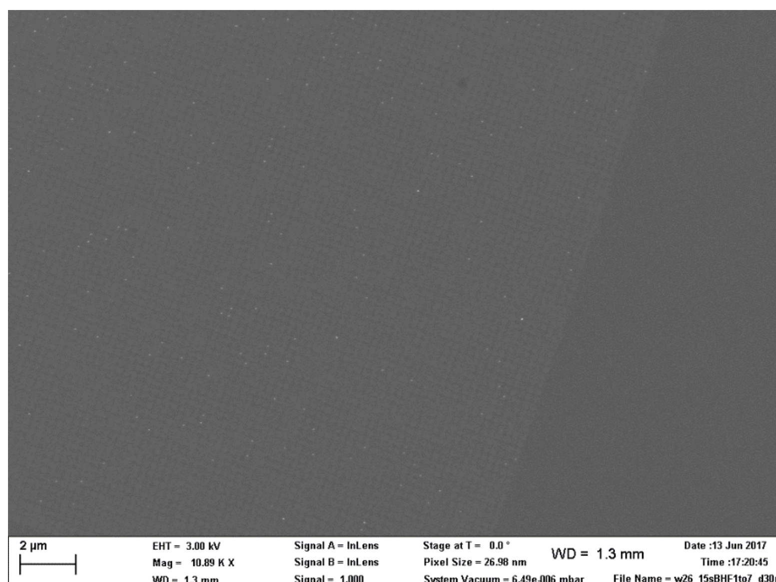


Figure 12: 30 nm diameter holes, 250 nm pitch

Figure 13 and 14 are images of the largest hole diameter field, 70 nm, with 250 nm pitch. Significantly more holes are open and have gold deposited in them than in the smaller diameter fields. However, the yield is far from one hundred percent. The most likely reason for this limited yield is that the etching time of 15 seconds did not suffice. However, earlier experiments have shown that 15 seconds was an appropriate etch time for a 25 nm thick SiN_x layer. Possible explanations for this difference could be that the BHF solution for this experiment came from another manufacturer or that the PECVD reactor deposited a layer with a higher density and thus a slower etch rate. A cause for the incomplete gold dots visible in figure 14 could be that some holes were only partially deep enough in order for the gold to stay in the holes during lift-off.

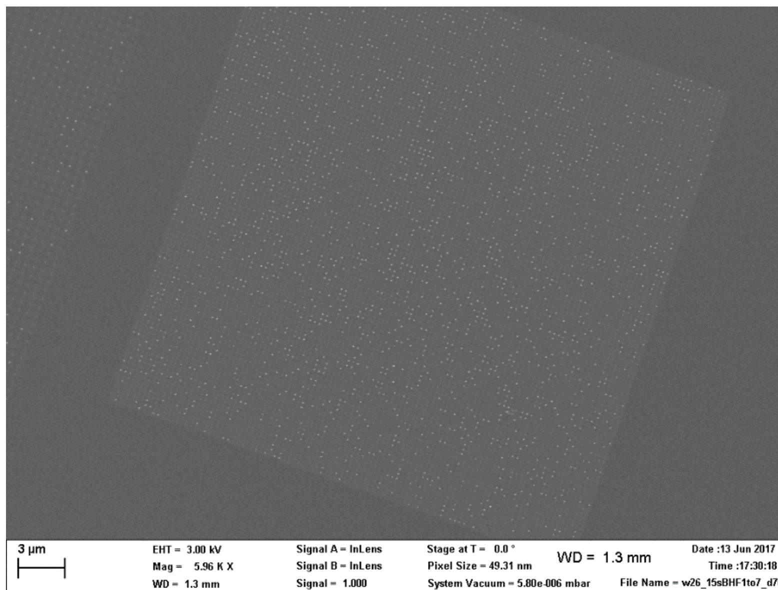


Figure 13: 70 nm diameter holes, 250 nm pitch

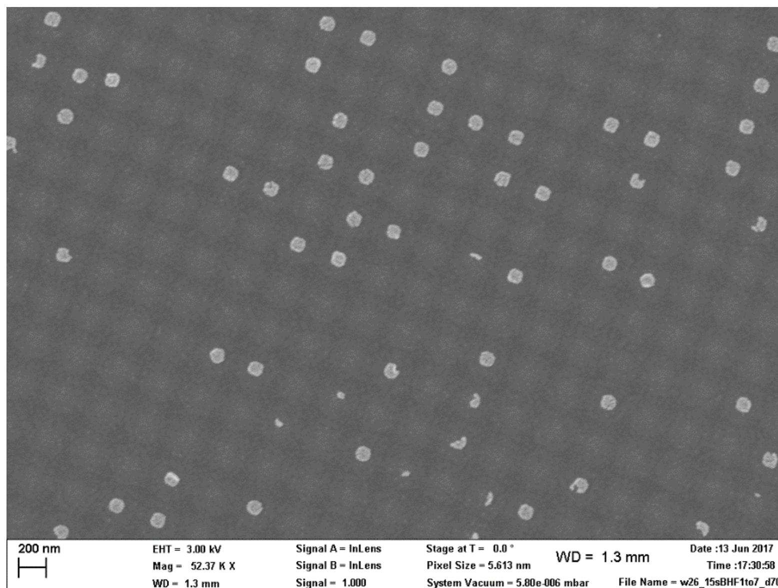


Figure 13: 70 nm diameter holes, 250 nm pitch, zoomed in

4.2 BHF etch 20 seconds

Figure 14 and 15 show the 50 nm diameter hole with 250 nm pitch field. The yield of these fields is a hundred percent. The other diameter fields show the same result, except for the 16 nm hole diameter 250 pitch (see appendix). This backs up the previous conclusion that 15 seconds of etching simply was not long enough for this particular wafer. Upon further inspection of figure 15, there are darker circles visible around the gold dots as well as some lighter circles around the darker ones. The darker area is most likely the part of the hole in which the indium phosphide wafer is fully exposed, whereas the lighter areas could indicate the part of the silicon which was affected by the BHF but was not fully etched away. A sketch of this hypothesis is drawn in figure 16.

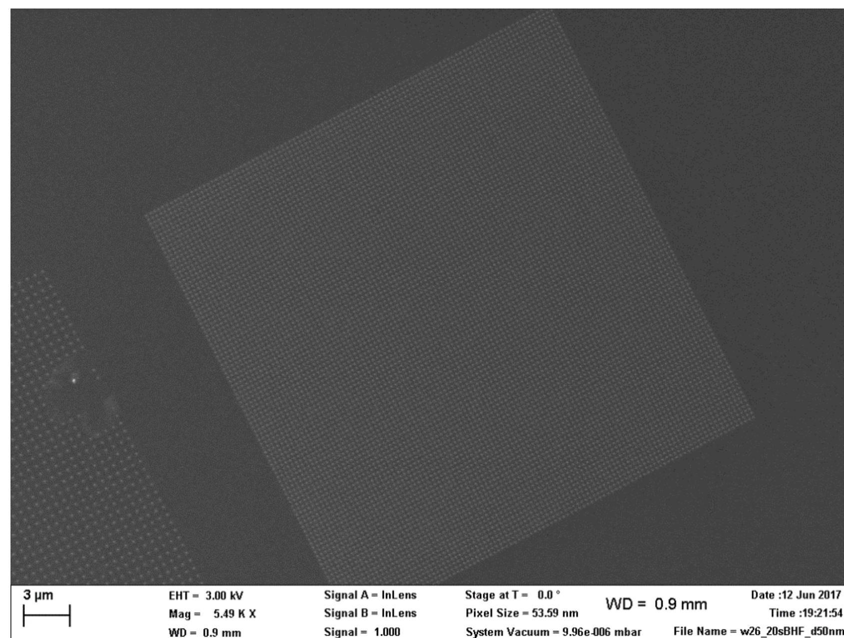


Figure 14: 50 nm diameter holes, 250 nm pitch

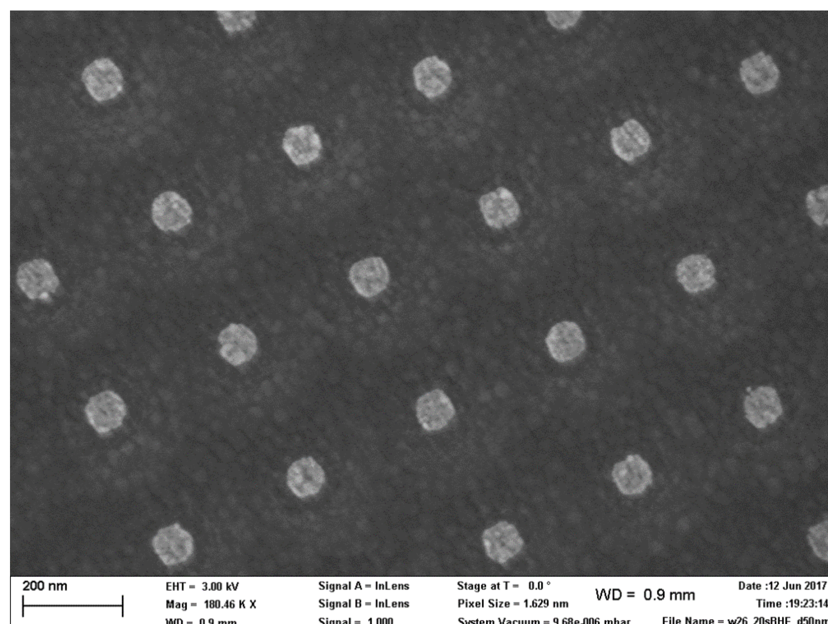


Figure 15: 50 nm diameter holes, 250 nm pitch, zoomed in

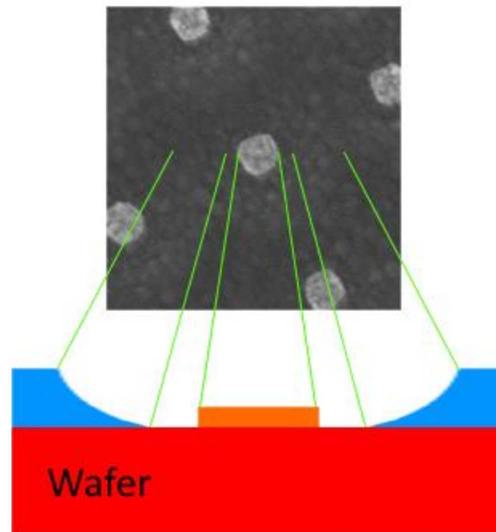


Figure 16: Speculated shape of holes and gold particles. The green lines indicate what part of the SEM image corresponds to what part of the sketch.

Figure 17 provides a rough measurement of both the gold and the hole diameters of the 40 nm diameter holes. From this image is derived that both the gold particle diameter as well as the actual hole diameter are larger than the intended 40 nm by approximately 12.5 nm and 64 nm, respectively. An explanation for the large hole diameter could be that the etching time of 20 seconds was too long and therefore caused quite a large etch bias. The reason for the gold particles being larger than the intended hole diameter is most likely due to the holes in the resist being too large and can thus be traced back to either the ebeam exposure or the development. The 1 micron pitch fields also had a yield of one hundred percent.

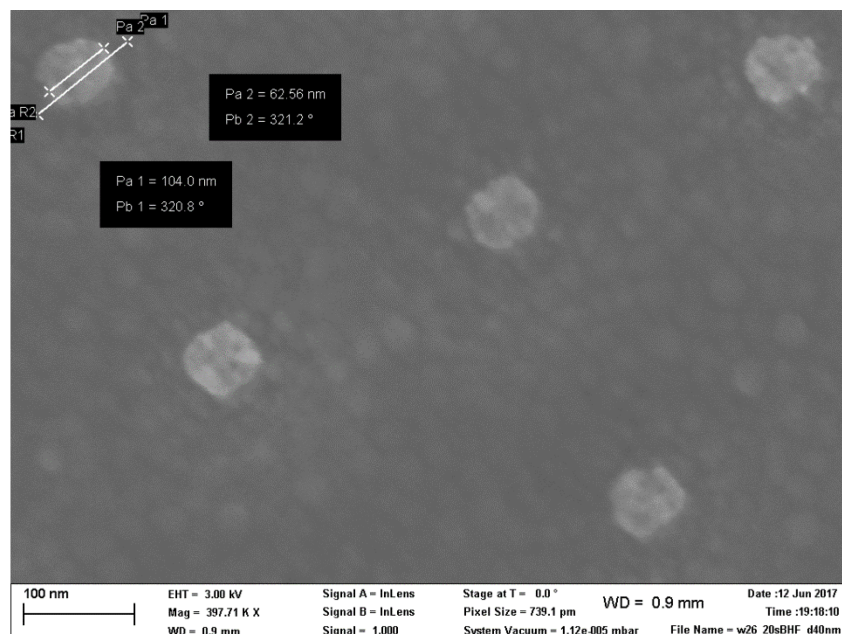


Figure 17: An attempt to measure the hole and gold diameter size. 40 nm diameter holes, 250 nm pitch

4.3 BHF etch 25 seconds

Figure 18 and 19 are the 250 nm pitch fields of the 30 nm diameter and 16 nm diameter holes, respectively. These fields are characterised by the lighter spots spread across them. Following the earlier conclusion that the lighter areas around the gold dots are in fact due to an etching bias, this is an indication of severe over-etching. It is worth noting that, although some of the etch biases appear to overlap, the resist layer on top did not collapse since the gold dots are still at the intended positions. A way to make sure that there is no silicon nitride in the lighter areas due to over-etching, is to examine whether any parasitic growth is visible in these areas after nanowire growth.

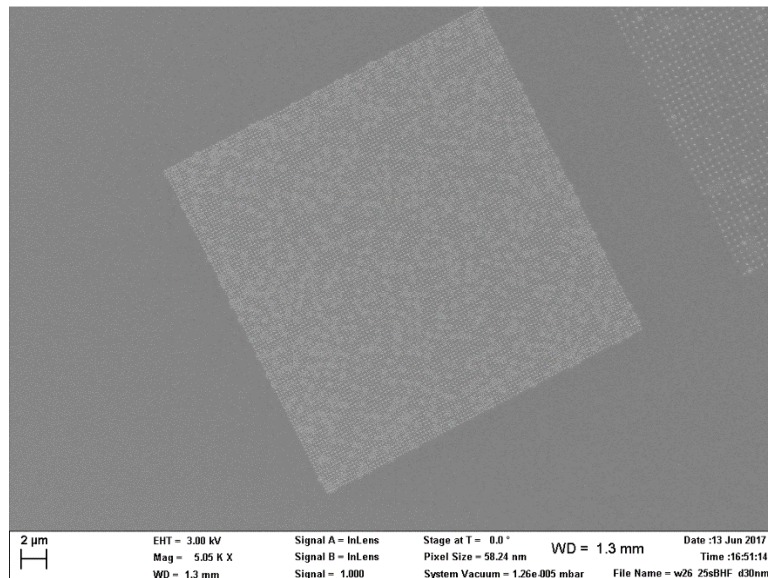


Figure 18: 30 nm diameter holes, 250 nm pitch

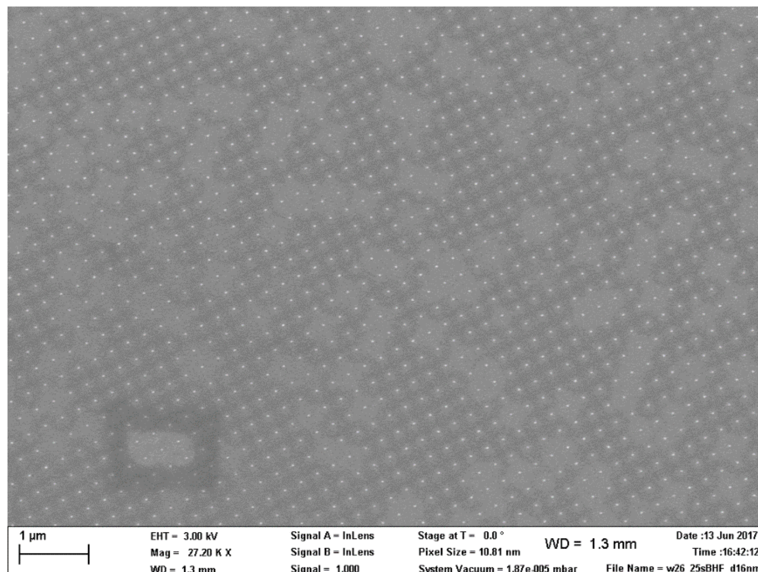


Figure 19: 16 nm diameter holes, 250 nm pitch

Upon inspection of the 1 micron pitch fields, the yield is not a hundred percent, whereas their corresponding 250 nm pitch fields were all opened. The 1 micron field of the 30 nm diameter holes is shown in figure 20. The number of unopened holes once again becomes less the larger the hole diameter becomes. The 50 nm diameter field with 1 micron pitch for instance, showed little to no unopened holes and the 60 nm and 70 nm are completely open. This is in accordance with an earlier conclusion about the relation between hole diameter and the yield.

It is strange that there are unopened holes at all since this sample was over-etched. The only difference between the 1 micron fields and the 250 nm fields is the pitch. So, most likely, there is a correlation between the pitch and the chance for a hole to open on an over-etched sample. Even stranger is the fact that these fields were entirely open for an etch time of 20 seconds and not for 25 seconds. Perhaps the holes were actually open but the resist had a greater chance of collapsing due to large etch biases for larger pitches and that impeded the gold from being deposited in some holes? It is unlikely that the problem arose during EBL or development since all five samples underwent the same treatment at the same time as they were still part of a complete wafer. It is not impossible however: the EBL may have given less power at certain times or the development may not have been entirely uniform.

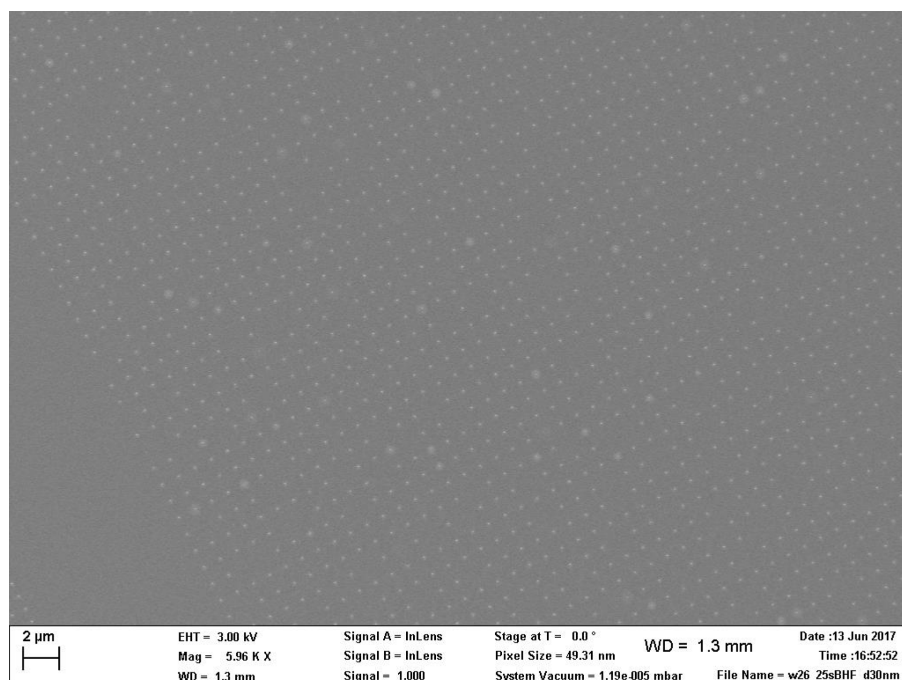


Figure 20: 30 nm diameter holes, 1 micron pitch

4.4 RIE 150 seconds

Figure 21 and 22 are images of the sample which underwent RIE for 150 seconds. Every field examined on this sample had one hundred percent yield, indicating that RIE is in fact an effective etching method. When comparing RIE to BHF wet etching, a first difference is the edge of the holes: the edges of the dry etched holes are much more defined than the edges of the wet etched holes. This is in accordance with the theory which says that RIE is a much more anisotropic process, thus leaving behind a much sharper edge. However, since a darker ring is present around the gold dots, indicating an empty space between the dots and the hole edge, it is also concluded that the cavities in the SiN_x had a larger diameter than the holes in the resist. This means that RIE is not an entirely anisotropic process, i.e. etching does not only occur perpendicular to the sample surface. This is again in accordance with the theory since during RIE both ion bombardment takes place, occurring perpendicularly, as well as reactions between fluoride atoms and the SiN_x layer, an isotropic process.

Another noteworthy difference is that the gold dots of the RIE sample have much more distinct shapes than the gold dots on the BHF samples. Since the shape and size of the gold is very dependent on the shape and size of the hole in the resist, the conclusion is drawn that the holes in the resist obtained rougher edges during the RIE process.

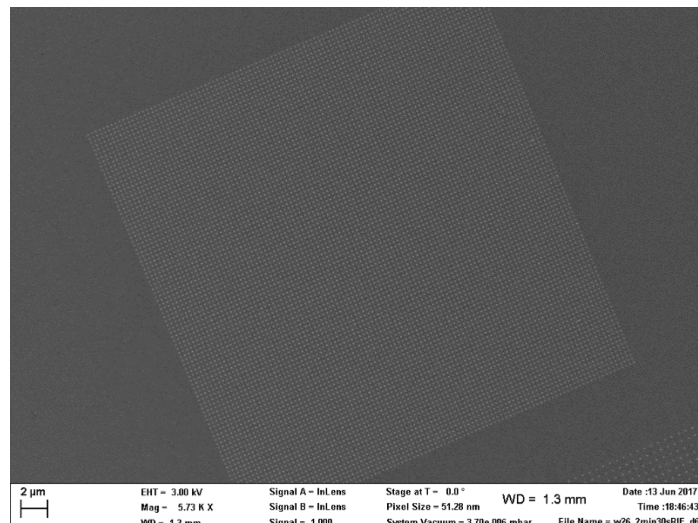


Figure 21: 70 nm diameter holes, 250 pitch

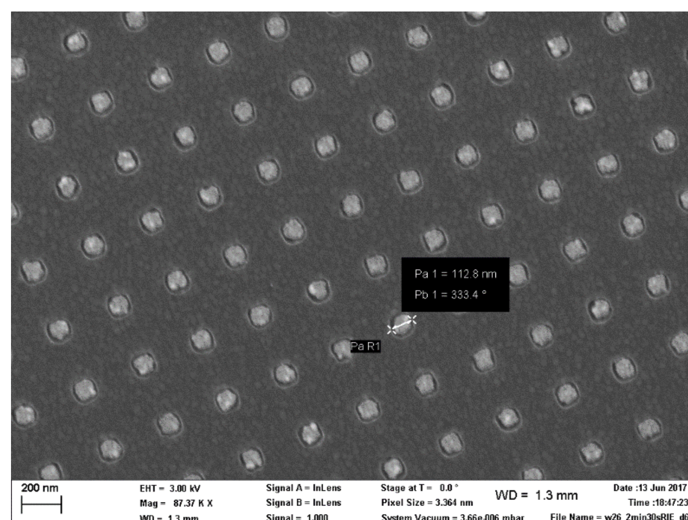


Figure 22: 70 nm diameter holes, 250 pitch, zoomed in

5. Conclusion

One difference between dry etching by RIE and BHF wet etching is very clear from this report: the holes of a dry etched sample have much more defined edges, whereas the holes of a wet etched sample shows quite large etching biases. Furthermore, for the wet etched samples, it is clear that 15 seconds of etch time was insufficient for this specific sample. It would be interesting to find out why for samples with the same resist thickness in earlier experiments, the 15 seconds etching time did suffice, by for example seeing if there is a difference in density between the new and the older samples. Next, the 25 second wet etched sample clearly shows signs of over-etching, indicating the importance of a precise wet etch time. No conclusions about the appropriate etch time can be drawn regarding the dry etched sample, since there was only 1 sample and there was no reference available with the same sample parameters. Another thing worth investigating are the differences among the nanowires of both the dry etched sample and the wet etched samples when grown on them.

In general, these experiments, in which quite a large set of process parameters influence the final outcome of the samples, require vaster sample sizes. This is because it is impossible to pinpoint the exact cause for, for instance, the hole diameter being much larger than intended or holes not opening. In other words: little solid conclusions can be drawn if multiple parameters differ between compared samples, whereas having only one parameter differ between samples would pinpoint a cause much faster. Besides a larger number of samples, repetition of the experiment is also of importance in order to show that the outcome of one experiment was not random as is so often the case in nanowire substrate fabrication.

6. Bibliography

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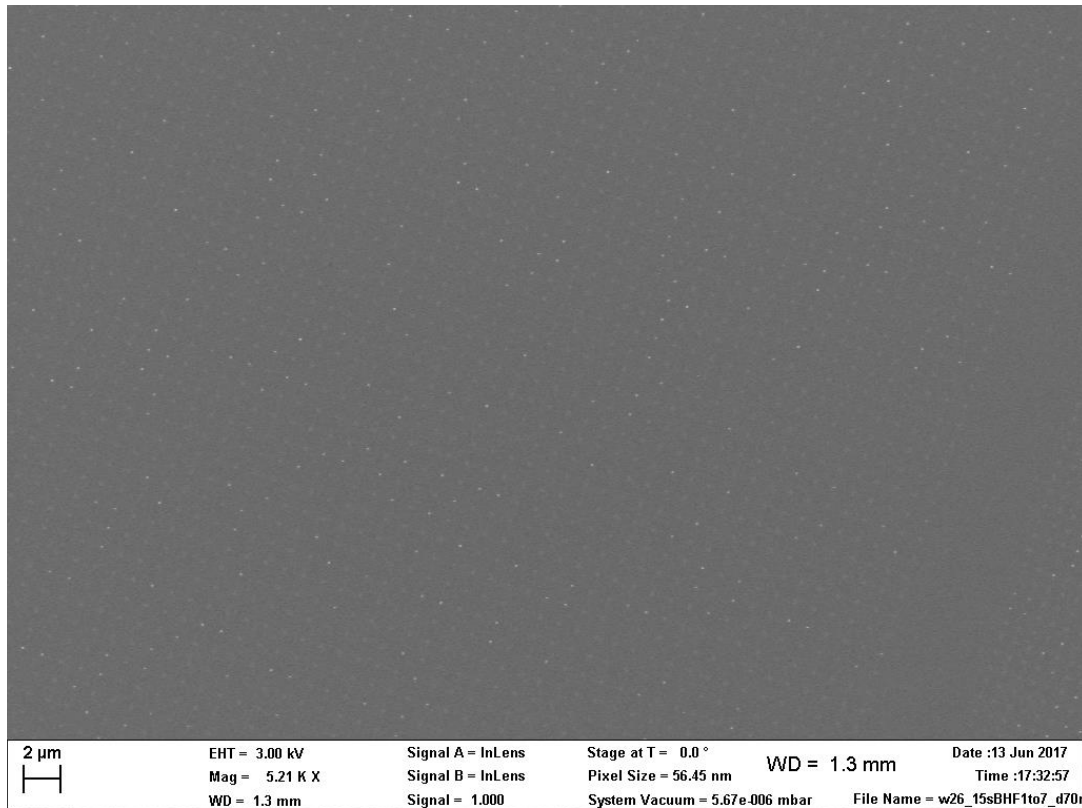
Appendix

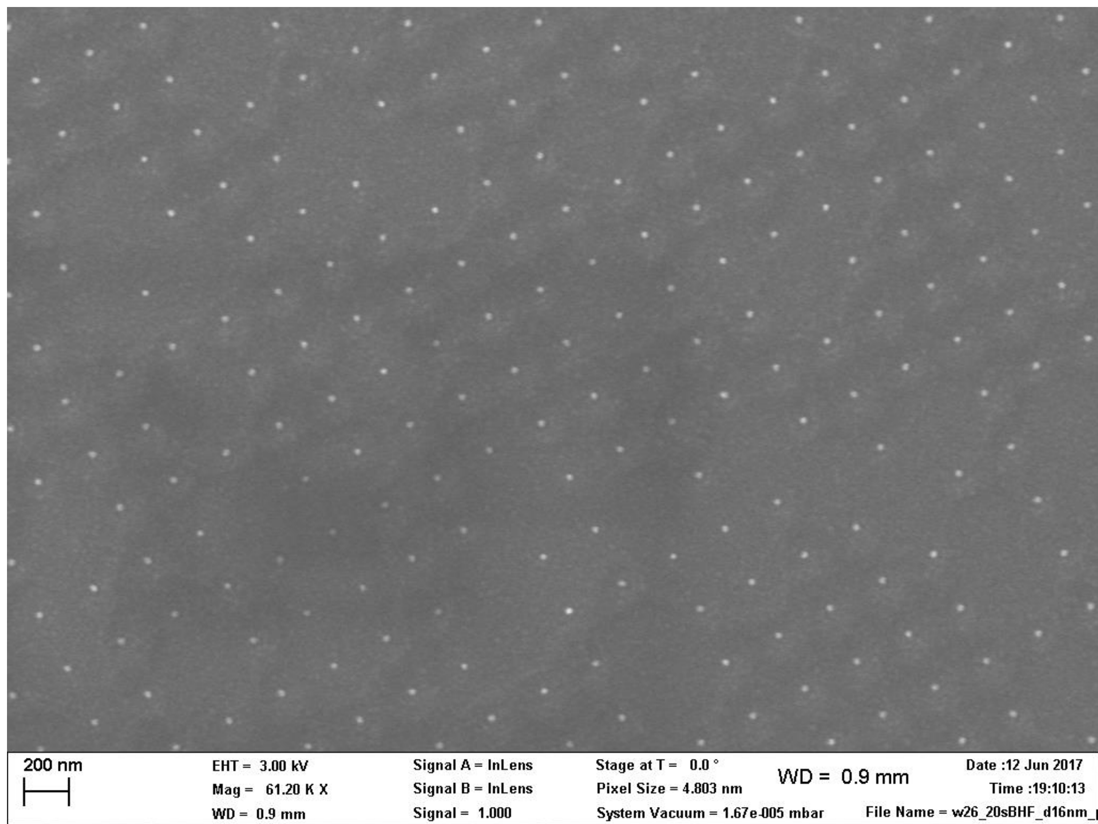
This appendix contains a selection of SEM images, not shown earlier in the report, for each of the four samples.

BHF etch 15 seconds

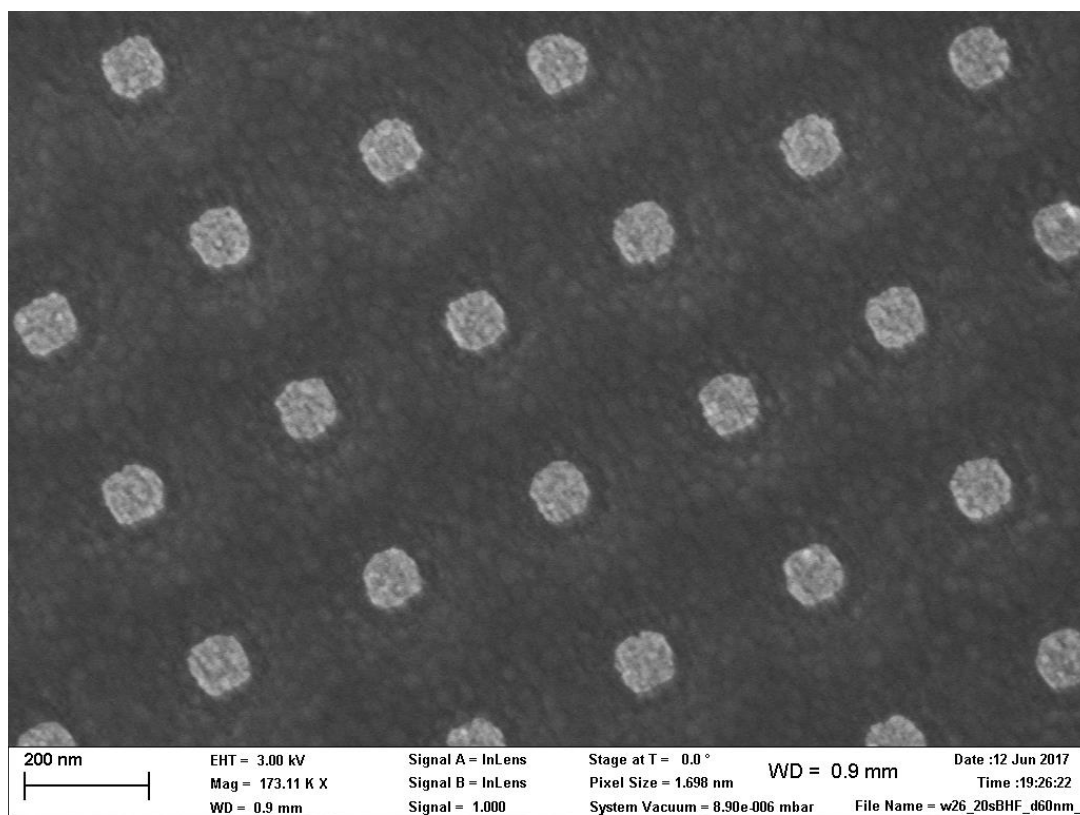


BHF etch 15 seconds, 70 nm diameter holes, 1 micron pitch

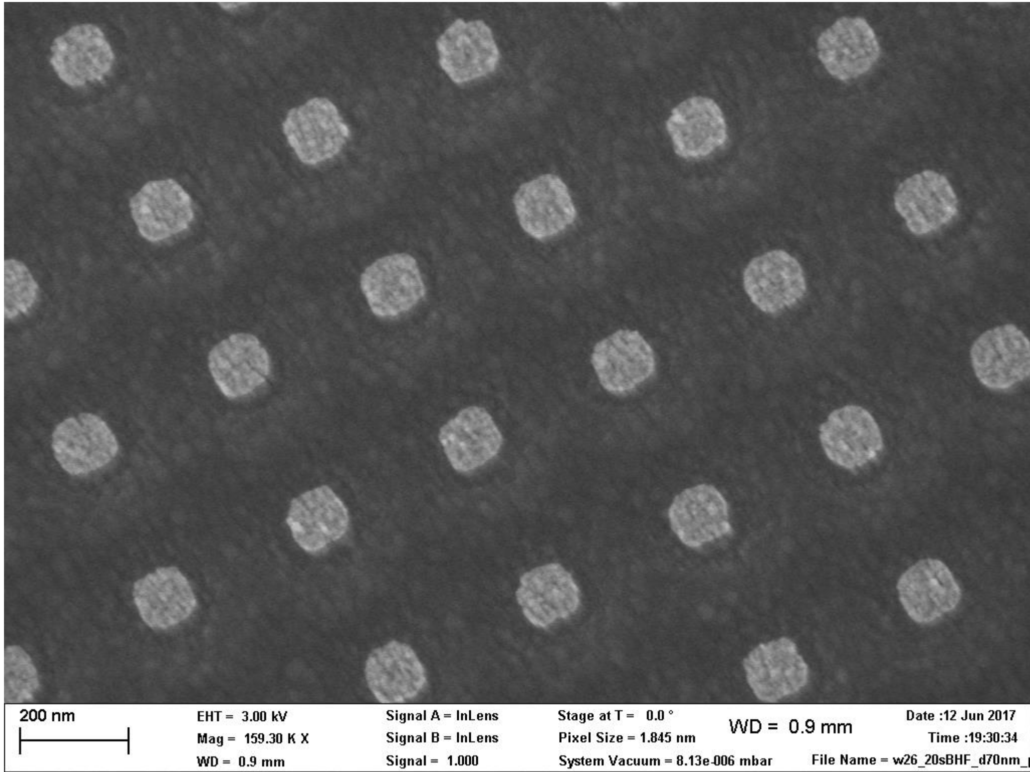
BHF etch 20 seconds



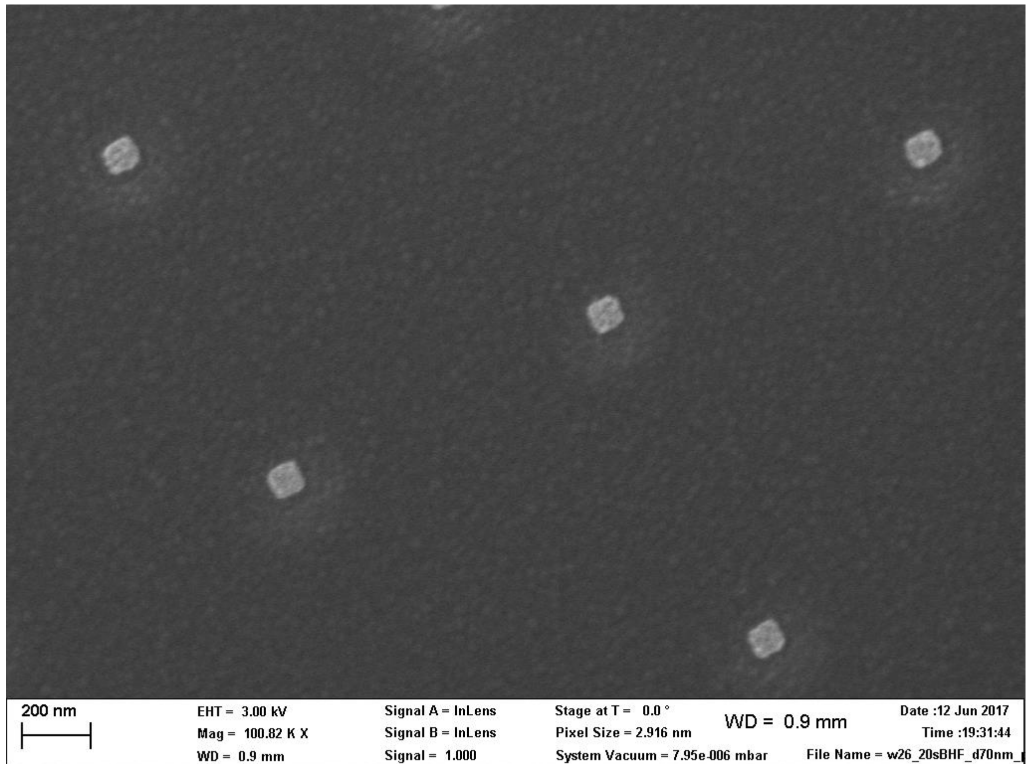
BHF etch 20 seconds, 16 nm diameter holes, 250 nm pitch



BHF etch 20 seconds, 60 nm diameter holes, 250 nm pitch

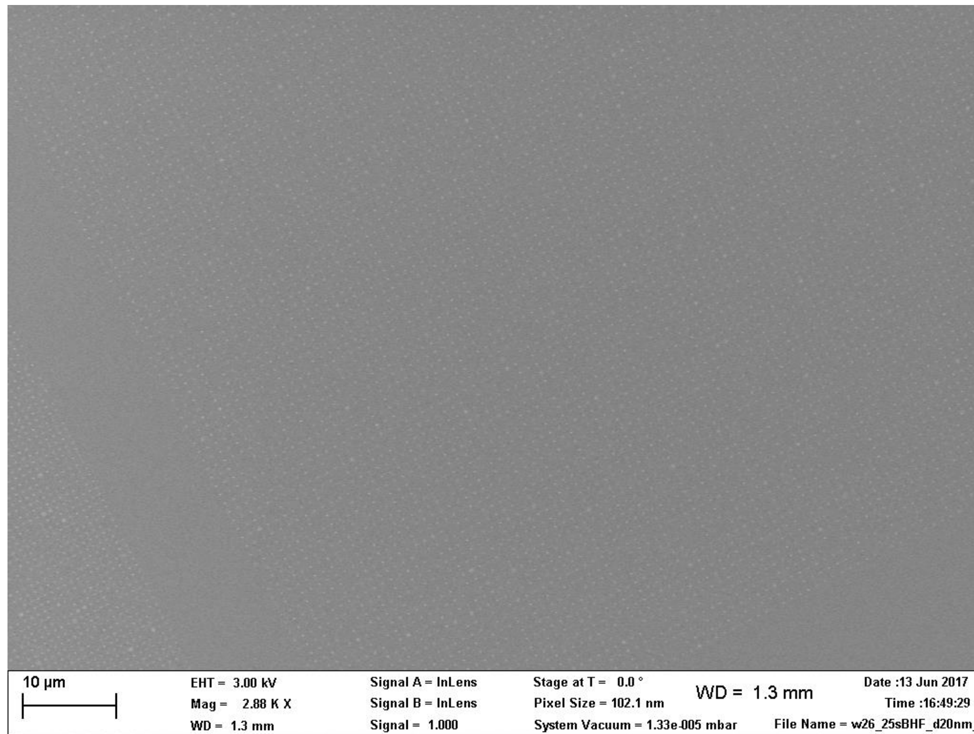


BHF etch 20 seconds, 70 nm diameter holes, 250 nm pitch

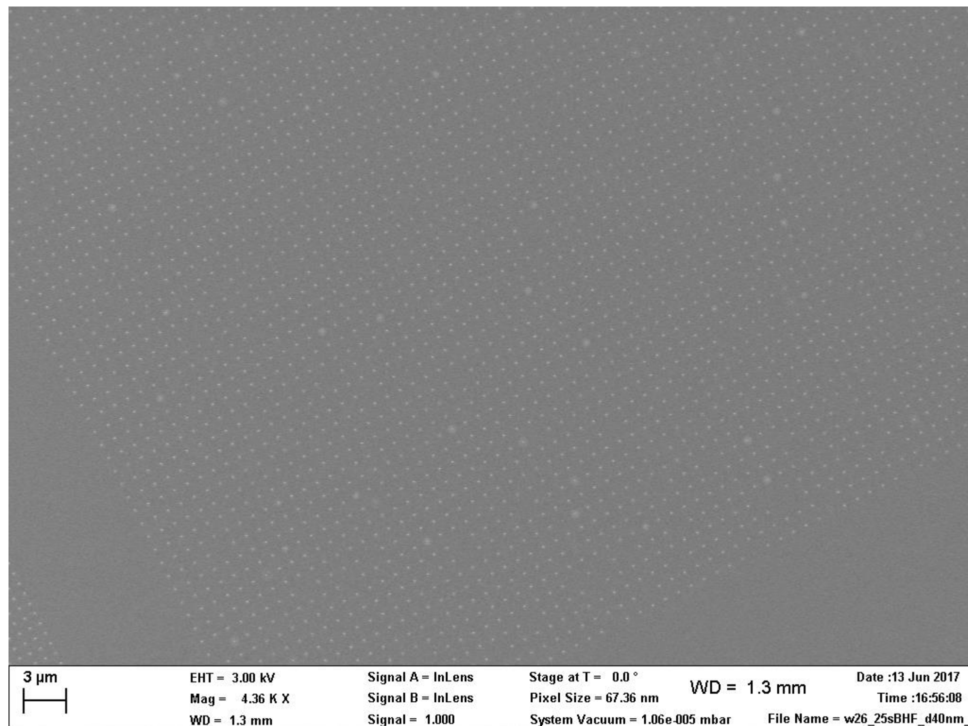


BHF etch 20 seconds, 70 nm diameter holes, 1 micron pitch

BHF etch 25 seconds

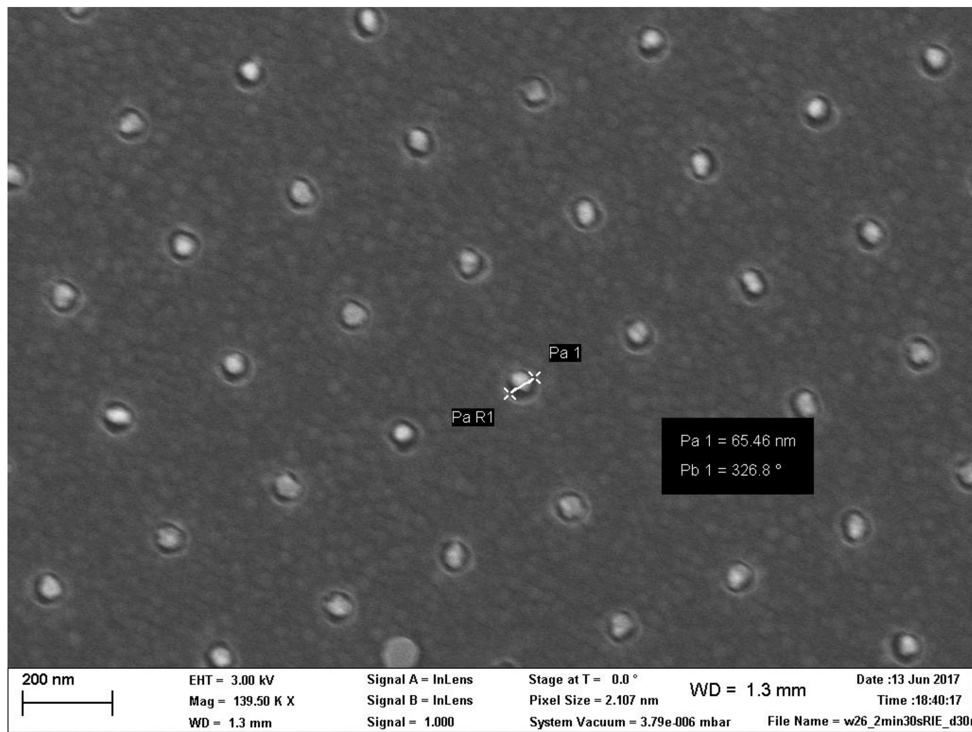


BHF etch 25 seconds, 20 nm diameter holes, 1 micron pitch

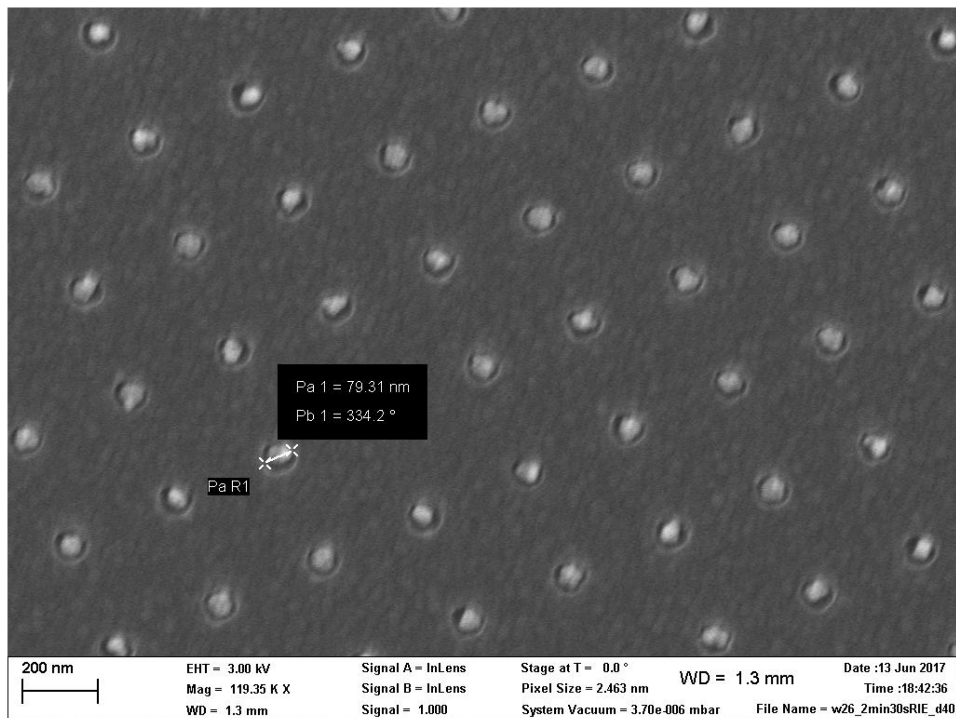


BHF etch 25 seconds, 40 nm diameter holes, 1 micron pitch

RIE 150 seconds



RIE 150 seconds, 40 nm diameter holes, 250 nm pitch



RIE 150 seconds, 50 nm diameter holes, 250 nm pitch