One cycle control used in a class-D power amplifier

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One Cycle Control used in a class-D power amplifier

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Abstract

Nowadays power converters such as computer batteries, television power supply units, audio amplifiers etc., are designed according to a switched-mode principle. This de- notes that the power conversion is achieved by switching the input voltage on and off with a certain ratio such that the desired output voltage is reached. These converters are usually controlled with Pulse Width Modulation (PWM). PWM is the control method whereby the switch on/of times (i.e pulse width) are adapted continuously to regulate the output voltage. Traditionally, this control method uses a linear feed- back to control certain state variables in the switched-mode converter.

This report presents a detailed analyse of the One-cycle control method. Theoretical analysis show that the controller is able to control the duty-ratio in real time such that in each switching cycle the average of the chopped waveform at the switch output is exactly equal to the control reference. These analysis include simulations of the OCC used to control a buck converter and a full-bridge amplifier. A detailed analyses for component sensitivity is also presented for the controller.

Beside the theoretical analyses, practical measurements are performed to verify the theoretical results. The OCC is designed and implemented on a PCB and used to control a class-D power stage. The performance of the OCC power amplifier is then compared to the UCD power amplifier. As a result the experiments have shown that OCC power amplifier performs slightly better than the UCD amplifier.

Finally the OCC power amplifier is extended with the addition of an output feedback. The output feedback is added to compensate for the disturbances in the output load and to reduce the offset in the output voltage.

Acknowledgements

I would like to express my appreciation and gratitude to the following people for their help in conducting the graduation project.

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Furthermore, I would like to extend my appreciation to the Philips Power Solutions employees for creating a pleasant work environment that is hard to forget. And spe- cial thanks goes to Marijn Uytdewilligen for his support with the PCB design.

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Chapter 1

Introduction

Nowadays power converters such as computer batteries, television power supply units, audio amplifiers etc., are designed according to a switched-mode principle. This denotes that the power conversion is achieved by switching the input voltage on and off with a certain ratio such that the desired output voltage is reached. These converters are usually controlled with Pulse Width Modulation (PWM). PWM is the control method whereby the switch on/off times (i.e pulse width) are adapted continuously to regulate the output voltage. Traditionally, this control method uses a linear feedback to control certain state variables in the switched-mode converter.

In this conventional feedback control, the duty-ratio is linearly modulated in a direction that reduces the error. When the power source voltage is perturbed, for example by a large step up, the duty-ratio control does not see the change instantaneously since the error signal must change first. Therefore a typical transient overshoot will be observed at the output voltage. The duration of the transient is dictated by the loop gain bandwidth. As a consequence, a large number of switching cycles is required before the steady-state is regained.

On the other hand, nonlinear control of PWM switch-mode converters, in comparison to linear feedback, has shown excellent improvements such as optimizing system response, reducing the distortion and rejecting power supply disturbances. One of these nonlinear control methods is *One Cycle Control (OCC)*.

The original OCC concept was proposed by Dr. Smedley in 1991[2]. The technique is conceived to control the duty-ratio in real time such that in each cycle the average of the chopped waveform at the switch output is exactly equal to the control reference. As a result the the OCC should be able to fully reject the perturbations in the power supply and follow the reference signal exactly [2].
Its fast response, low distortion and good power supply ripple rejection makes this control method interesting for many converters, especially for those that need accurate power supplies.

1.1 Objective and outline

The goal of this Master's thesis is *to provide a theoretical analysis and a practical verification of the One Cycle Control method used in an audio power amplifier.*

Purposely, an audio amplifier is chosen since this application is more sophisticated than other switched-mode applications. Furthermore, it needs to satisfy certain criteria such as a low THD and good PSRR (Power Supply Ripple Rejection). These criteria can be used to assess the performance of the One Cycle Controller.

This report presents the results of my graduation assignment, which consists of the following parts:

1. A literature research on the OCC method used in an audio class-D amplifier.
2. Evaluation of the control method of the OCC.
3. The design and implementation of the OCC in a class-D amplifier.

This report is structured as follows:

Chapter 2:
Description of the working and simulation of OCC principle.

Chapter 3:
Description of the improved OCC principle.

Chapter 4:
Simulation of the improved OCC.

Chapter 5:
Description of the implementation of the OCC in a class-D amplifier .

Chapter 6:
Presentation of the experimental results.

Chapter 7:
Description of the additional outer feedback loop

Chapter 8:
Conclusions of the graduation assignment and recommendations for future work.

Chapter 2

OCC theory

2.1 Principle of OCC

A circuit showing the principle of OCC is depicted in Fig. 2.1. A constant frequency clock is used to turn on the switch at the beginning of the cycle. The switched variable $y(t)$ is integrated and compared with a control reference. When the integrated value of the switched variable reaches the control reference, the comparator turns off the switch and resets the integrator to zero. This way, the integrated value of $y(t)$ equals the control reference within every cycle. As a result, the average value of $y(t)$, $< y(t) >$, is equal or proportional to the control reference, since the period of the switched variable is imposed to be constant.

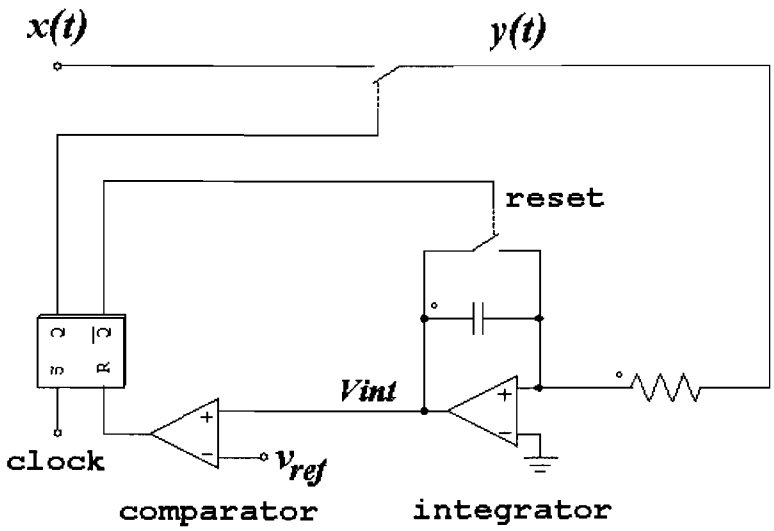


Figure 2.1: OCC constant frequency switch

The waveforms illustrated in Fig. 2.2 provide a good insight in the operating principle. As shown in the figure the input voltage $x(t)$ is a function of time and v_{ref} is chosen constant. As a result, the time (t_{on}) for the resetable integrator signal v_{int}

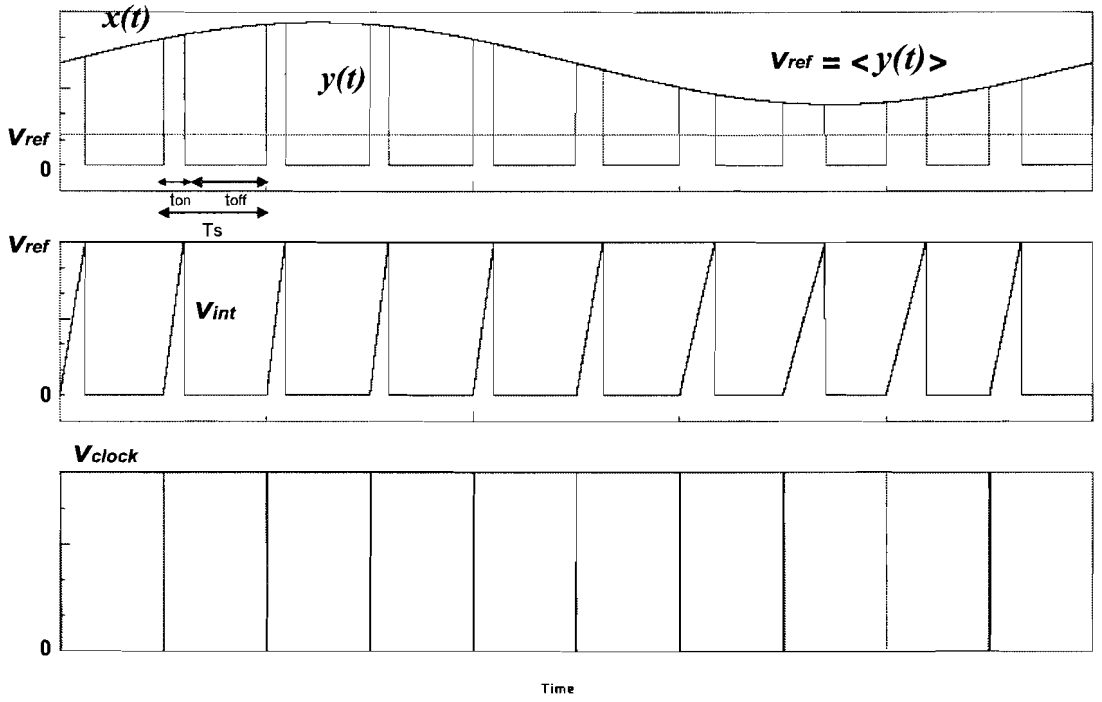


Figure 2.2: Waveforms of the One-cycle controlled constant frequency switch in case of a constant reference signal.

to reach the reference voltage v_{ref}, changes every cycle such that

$$\frac{1}{T_s}\int_0^{t_{on}} x(t)dt = \frac{1}{T_s}\int_0^{T_s} v_{ref}(t)dt \tag{2.1}$$

is satisfied every cycle. Consequently, the average of the switched waveform ($< y(t) >$) is equal or proportional to the average of the reference signal ($< v_{ref} >$) for every cycle according to

$$\begin{aligned} < y(t) > &= \frac{1}{T_s}\int_0^{t_{on}} x(t)dt \\ &= \frac{1}{T_s}\int_0^{T_s} v_{ref}(t)dt \approx v_{ref}(t). \end{aligned} \tag{2.2}$$

The key components of the OCC technique are the integrator and the reset circuitry (see Fig. 2.1). The integration starts at the moment when the switch is turned

on by the fixed frequency clock pulse. The integrated value,

$$v_{int}(t) = k \int_0^{dT_s} x(t)dt \tag{2.3}$$

is compared with the control reference $v_{ref}(t)$ instantaneously, where k is a constant and $d = t_{on}/T_s$ the duty-ratio. At the instant when the integrated value $v_{int}(t)$ reaches the control reference $v_{ref}(t)$, the switch changes from the on state to the off state. At the same time, the controller resets the integrator to zero. The corresponding duty-ratio can be determined by examining

$$k \int_0^{dT_s} x(t)dt = v_{ref}(t). \tag{2.4}$$

2.2 One-cycle control of a buck converter

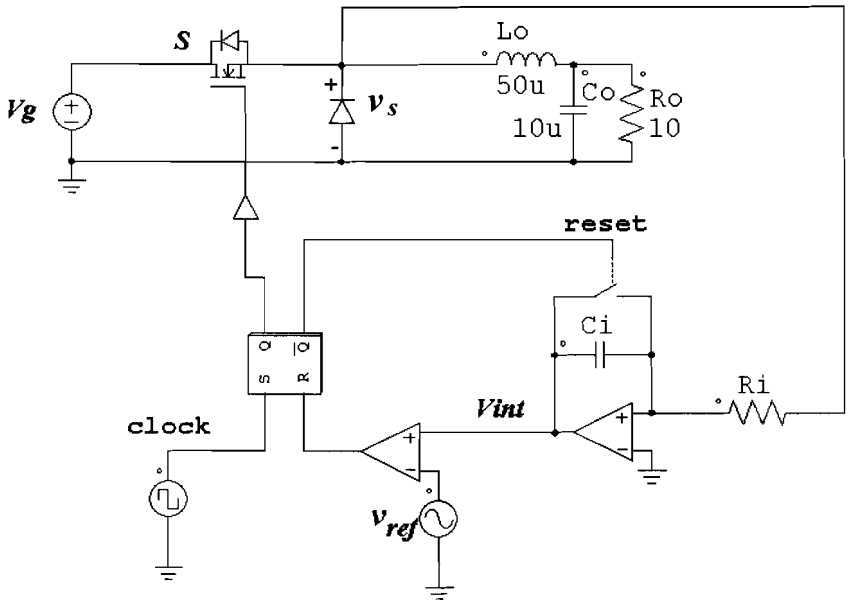


Figure 2.3: One-cycle control of a buck converter

To gain a better understanding a one-cycle controlled buck converter, shown in Fig. 2.3, was simulated with the simulation programme PSIM. The dc power source

voltage is V_g and the switch S are operated with a constant frequency. The converter works as follows. When the switch S is on, the diode is off, and the diode-voltage v_s equals the power source voltage V_g . When the switch S is off, the diode is on, and the diode-voltage, is zero. The power source voltage is chopped by the switch resulting in a switching variable v_s. The low-pass filter then attenuates the switching frequency and a dc output voltage, proportional to the reference input, is the result.

The MOSFET is turned on at the beginning of each switching period by a constant frequency clock. The diode-voltage is integrated and compared with a control reference, the comparator changes its state. As a result, the MOSFET is turned off and the integrator is reset to zero. The power source voltage V_g, diode-voltage v_s, reference control voltage v_{ref}, and clock signal are shown in Fig. 2.4 and Fig. 2.5.

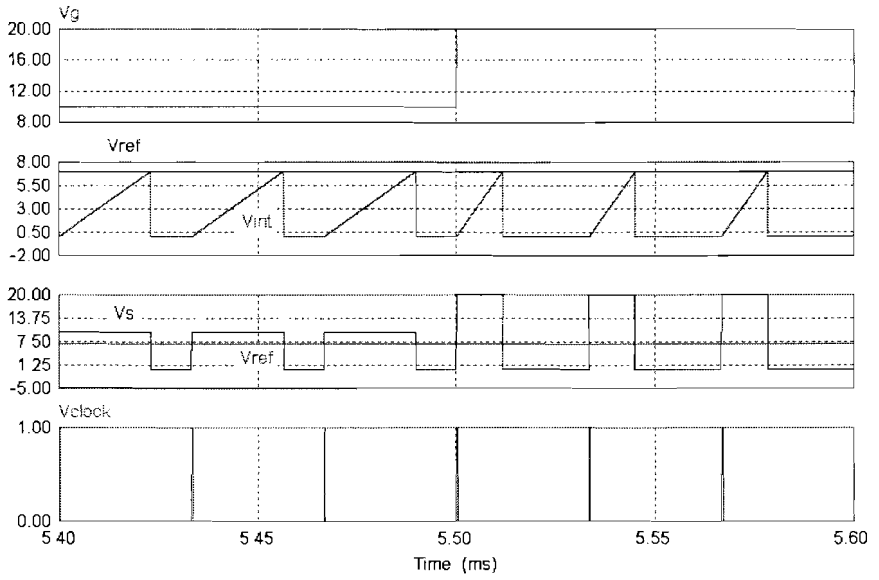


Figure 2.4: OCC buck converter, constant v_{ref}, step in V_g of $10V$, $Lo = 50\mu H, Co = 10\mu F, Ro = 10\Omega, Ri = 1k\Omega, Ci = 10nF, v_{ref} = 7V, V_g = 10V$

In the first simulation a step in the power source voltage V_g is introduced. The reference control voltage is held constant. As a result the duty-cycle decreases instantaneously, since the integrator needs less time to reach its reference voltage. Every time the integrated voltage v_{int} reaches its reference voltage the integrator is reset as can be seen in Fig. 2.4.

In the second simulation the power source voltage V_g is held constant and the reference control voltage V_{ref} is a sinusoidal function. From Fig. 2.5 it can be seen that the duty-cycle is modulated each cycle also.

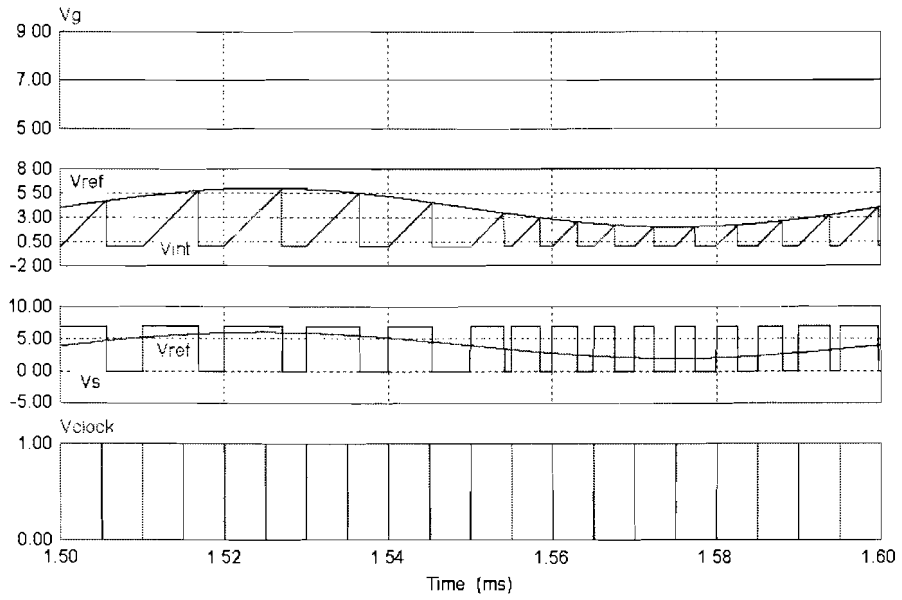


Figure 2.5: OCC buck converter, constant V_g, variable $v_{ref}, Lo = 50\mu H, Co = 10\mu F, Ro = 10\Omega, Ri = 1k\Omega, Ci = 10nF, v_{ref} = 4 + 2sin(\omega t), V_g = 7V$

2.3 Drawbacks of the conventional OCC

As mentioned above the OCC method has some good features such as fast dynamic response, excellent power source disturbance rejection, and a good tracking of the reference control signal. It takes advantage of the pulsed and nonlinear nature of switching converters and achieves instantaneous dynamic control of the average value of a switched variable; more specifically it takes only one switching cycle for the average value of the switched variable to reach a new steady- state after a transient. There is no steady-state error or dynamic error between the control reference and the average value of the switched variable. Though one-cycle control has many advantages, it has also some shortcomings.

First of all it presents infirmness with respect to load disturbance. Since the control takes place immediately after the switch it has no influence on load disturbances. Thus if the load is sensitive to disturbances another feedback controller is needed to compensate for this.

Another shortcoming of the OCC is the necessity of a fast resetting of the integrator. Since switching converters mostly are operated with high frequencies (above 100kHz), the resetting of the integrator can be a problem, especially when the duty-cycle is close to one. To overcome this problem the improved OCC is introduced which doesn't need a fast resetable integrator in the control loop. This improved method is discussed in the next chapter

Chapter 3

Improved one-cycle control

3.1 Theory

Fig. 3.1 shows the improved one-cycle control concept for any system where a switched variable $v_p(t)$ has to be controlled, and Fig. 3.2 shows the theoretical waveforms. Again one-cycle response is ensured by forcing the average of the switching variable $\langle v_p(t) \rangle$ over one cycle (switching period) to be equal to the reference voltage each cycle. However, this time the reset function in the control loop is left out and there is no clock-pulse generator which sets the switching frequency.

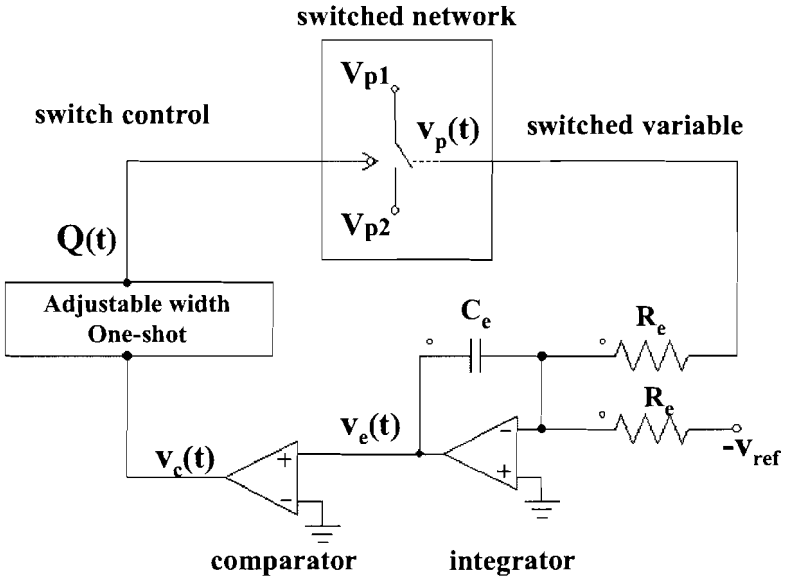


Figure 3.1: Improved one-cycle control concept

The switching control functional block *one-shot* has two functions. It needs to

adjust the width of the duty-cycle to ensure one-cycle response. Simultaneously it needs to keep the switching frequency constant.
At the start of a cycle $v_p(t)$ equals the upper rail V_{p1}, and the error integrator will integrate the difference between V_{p1} and V_{ref} until the end of the one-shot pulse. The switch then changes its state such that $v_p(t)$ equals V_{p2} and the error integrator will integrate the difference between V_{p2} and V_{ref} until the error equals zero at the end of the cycle. Then the comparator triggers another one shot and the next cycle is started.

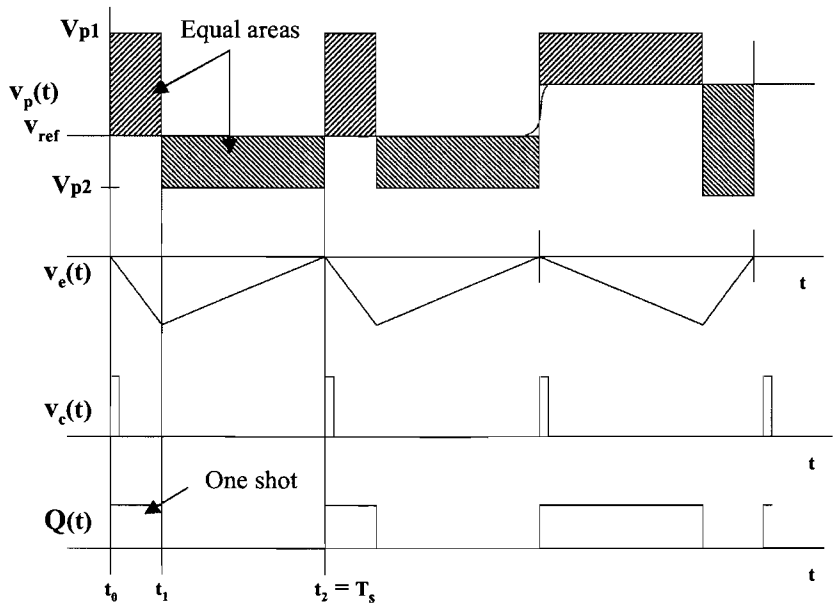


Figure 3.2: Waveforms of the improved control method

The required pulse width to maintain constant switching frequency for any V_{p1}, V_{p2} and v_{ref} can be found by examining

$$\frac{1}{T_e}\int_{t_0}^{t_1}(V_{p1}-V_{ref})dt+\frac{1}{T_e}\int_{t_1}^{t_2}(V_{p2}-V_{ref})dt=0 \tag{3.1}$$

where $T_e = R_eC_e$, and $T_s = t_2 - t_0$,(see Fig. 3.2). The first term describes the error integrator operation when $v_p(t) = V_{p1}$, and the second term describes the operation when $v_p(t) = V_{p2}$. If T_s is assumed to be constant, then the on time ($t_{on} = t_1 - t_0$) should satisfy

$$t_{on} = (\frac{V_{ref}-V_{p2}}{V_{p1}-V_{p2}})T_s \tag{3.2}$$

The conceptual diagram with the adjustable one-shot control is shown in Fig. 3.3. By rearranging (3.2) into a form that can be realized with a resetable integrator and comparator circuit, it is found that

$$\frac{1}{T_0}\int_0^{t_{on}}(V_{p1}-V_{p2})dt = \frac{1}{T_0}\int_0^{T_s}(V_{ref}-V_{p2})dt \tag{3.3}$$

$$\frac{1}{T_0}\int_0^{t_{on}}(V_{p1}-V_{p2})dt = V_{ref}-V_{p2} \tag{3.4}$$

Where $T_0 = R_0C_0$ equals T_s. When Q is set to 1, switch S_1 is off and $v_p(t) = V_{p1}$ the resetable integrator determines the exact duty-cycle. Otherwise, when $Q = 0$, switch S_1 is on and the output is reset to zero. Simultaneously, during a one-shot t_{on}, the loop integrator circuit integrates the input $V_{p1} - V_{ref}$. At the end of the one-shot, comp2 goes high and resets the flip-flop which will change the state of $v_p(t)$ to V_{p2} and the resetable integrator is reset. The loop integrator then integrates the input $V_{p2} - V_{ref}$ until comp1 sets the flip-flop at the beginning of the next cycle again. It should be noticed that int1 in Fig. 3.3 satisfies (3.1) with $T_e = R_eC_e = T_s$ and int2 satisfies (3.4) with $T_0 = R_0C_0 = T_s$.

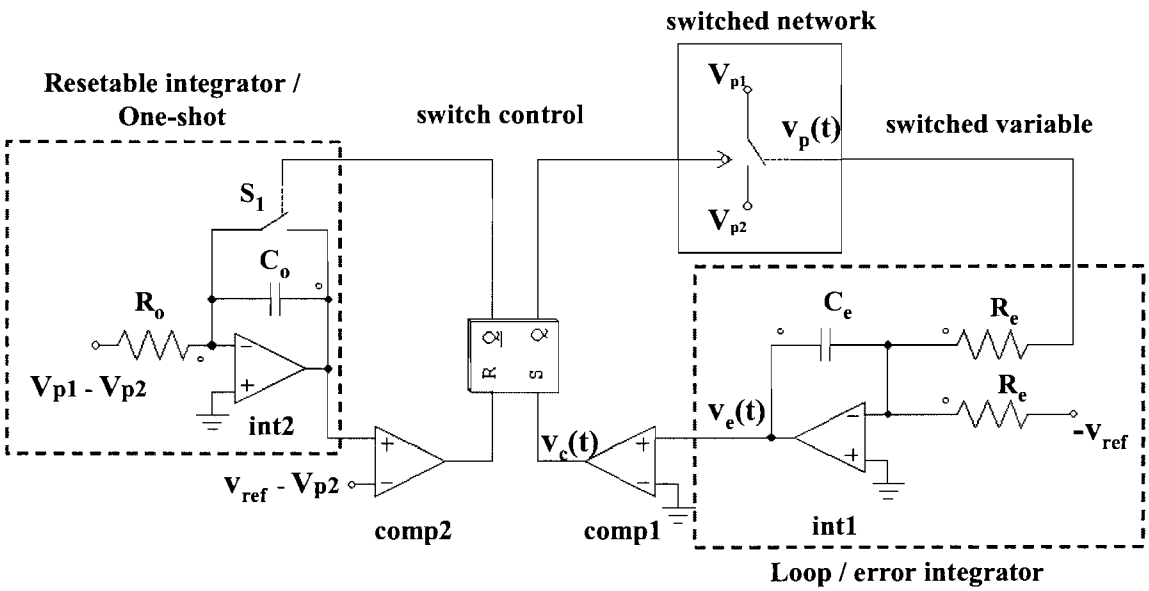


Figure 3.3: Complete OCC conceptual diagram

3.2 Pulse width modulation, double-edge

The stearing of the switches in the power converters is generally realized by pulse width modulation (PWM). The PWM could be applied in several ways (see Fig. 3.4):

- Leading-edge modulation(single-edge); the tail edge is fixed and the lead edge modulated,
- Trailing-edge modulation (single-edge); the lead edge is fixed and the tail edge modulated,
- Double-edge modulation; the pulse center is fixed in the center of the cycle and both edges are modulated
- Variable frequency modulation (fixed pulse width).

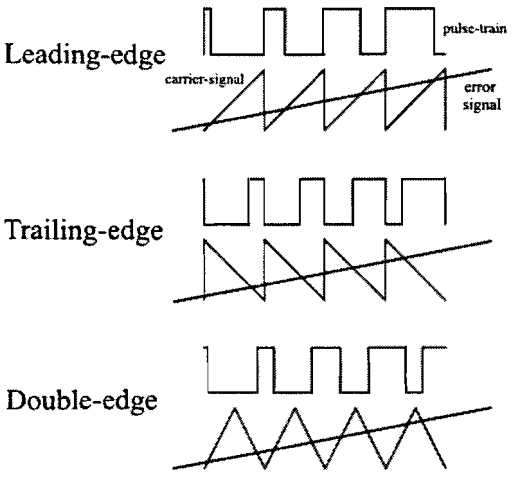


Figure 3.4: pulse width modulation types with fixed frequency

All the methods are able to reach zero steady state error in the output signal. However, their dynamic performances differ for each method. Generally, variable frequency operation is not desirable in power processing circuits, since the harmonics are unpredictable and therefore hard to eliminate. Especially in high fidelity audio amplifiers this is not desired.

Therefore the OCC is designed to operate with a constant switching frequency (single- or double-edge modulated). Normally the PWM constant frequency is realized by comparing a carrier signal (sawtooth or triangle wave) with an error signal and hence generate the pulse train (see Fig. 3.4). This is a linear control method.

However in the OCC technique the PWM is realized by comparing the control variable directly with its reference signal what gives the controller a non-linear character (see Fig. 2.2).

As discussed in the previous section the switching frequency in the improved controller is determined by both the resetable one-shot integrator and the loop integrator. The resetable one-shot sets the on time t_{on} and the loop integrator then determines the off time t_{off} such that the error is zero. In theory, when both the power supply voltage (V_{p1} and V_{p2}) and the reference control signal are constant and the circuit is free of delays, the switching frequency is constant. But in practice this is impossible and hence the switching frequency changes slightly.

In the conventional OCC the switch is controlled single-edge leading modulation as shown in Fig. 2.2. However in the improved OCC , the PWM is realized by double-edge modulation. Double-edge results in less switching frequency variation, which is preferable to achieve a lower distortion.
In case of single-edge modulation, the center of the pulses is modulated by the perturbation around the average center, since one edge of the pulses is locked with clock (see Fig. 3.5). This introduces a perturbation frequency component at the output spectrum, especially when the frequency is higher the effect becomes more severe. But, with double-edge modulation both sides are modulated while the center of the pulse is kept constant for each cycle (see Fig. 3.6). The pulse position modulation effect should be eliminated. This effect is illustrated in Fig. 3.5 and 3.6

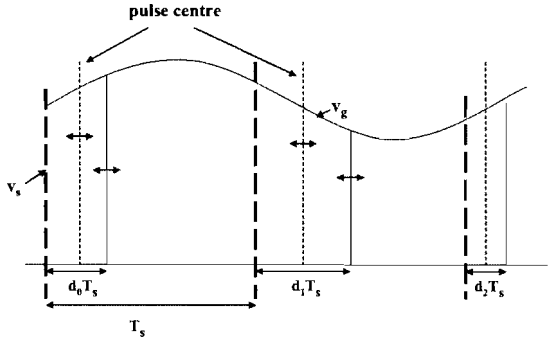


Figure 3.5: Pulse centre is modulated

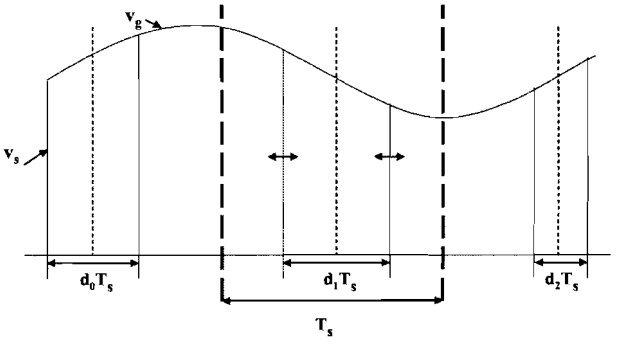


Figure 3.6: Pulse centre is fixed

The double-edge modulation could be realized by combining leading- and trailing-edge modulation on alternate half cycles (see Fig. 3.7).

If the input supply voltages V_{p1} and V_{p2} and the reference voltage V_{ref} are all constant then the switching frequency is also constant. A formula for the exact on time t_{on} to achieve constant switching frequency was derived in the previous section, equation(3.2). However, if the values for V_{p1}, V_{p2}, and V_{ref} are changing substan-

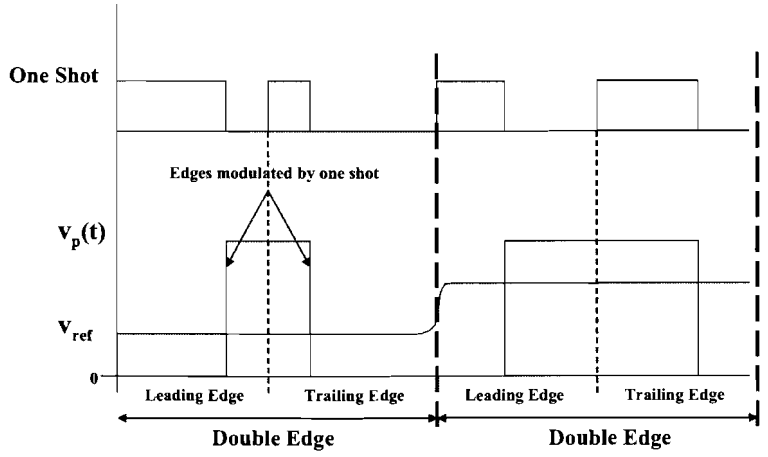


Figure 3.7: Double-edge modulation

tially during a switching cycle, the switching frequency will be affected. The exact switching period is found by rewriting (3.1) and (3.4) with V_{p1}, V_{p2}, and V_{ref} as a function of time

$$\frac{1}{T_0}\int_0^{t_{on}} (V_{p1}(t) - V_{p2}(t))dt = V_{ref}(t_{on}) - V_{p2}(t_{on}) \tag{3.5}$$

$$\int_0^{t_{on}} (V_{p1}(t) - V_{ref}(t))dt + \int_{t_{on}}^{T_s} (V_{p2}(t) - V_{ref}(t))dt = 0 \tag{3.6}$$

The period time T_s follows from (3.6) and the on-time t_{on} follows from (3.5). (3.5) refers to the one-shot resetable integrator, while equation (3.6) refers to the loop / error integrator. Since double-edge modulation consist of a leading-edge cycle and a trailing-edge cycle, the period time is twice T_s.

To show the improvement of double-edge modulation over single-edge modulation for the switching frequency variation both methods are considered and calculated numerically. In the first simulation variation in the switching frequency versus phase of the supply voltage and constant V_{ref} is plotted (Fig. 3.8). The fluctuation of the switching frequency is caused by a changing normalized power supply voltage given by

$$V_g(t) = 1 + 0.2\sin(\omega t + \phi) \tag{3.7}$$

In the second simulation variation in the switching frequency versus phase of the reference voltage V_{ref} and constant supply voltage is plotted. The fluctuation of the switching frequency is caused by a changing reference voltage given by

$$V_{ref}(t) = 0.8\sin(\omega t + \phi) \tag{3.8}$$

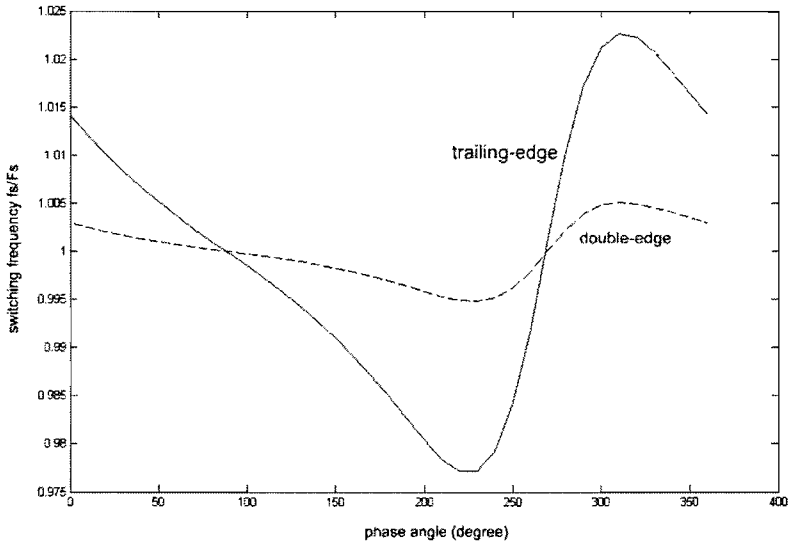


Figure 3.8: f_s variation caused by supply ripple

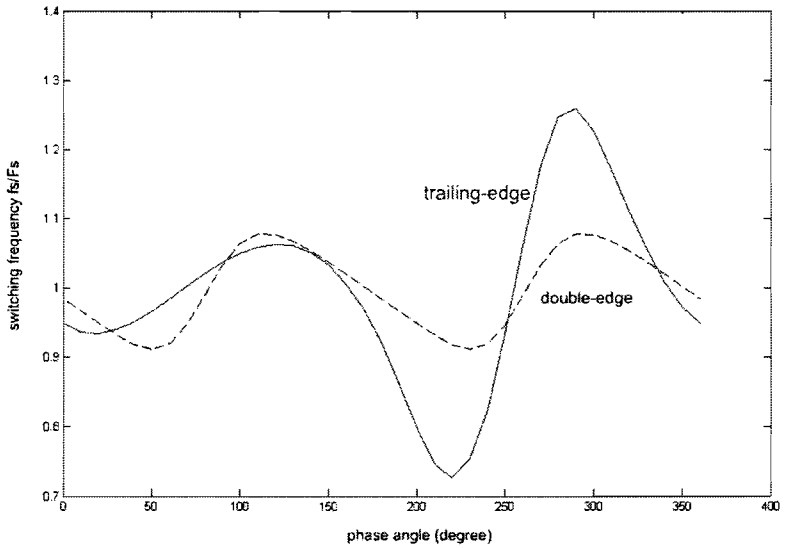


Figure 3.9: f_s variation caused by changing V_{ref}

Both Figures show clearly that double-edge modulation causes a considerably lower switching frequency fluctuation. When there is a 40% perturbation in the supply voltage the switching frequency fluctuation is ±2.25% and ±0.5% of the nominal value for trailing-edge and double-edge modulation respectively. The nominal switching frequency f_s is chosen 100 times greater than the supply voltage frequency. When the reference voltage is changing in time this has larger influence on the switching frequency fluctuation. However, double-edge modulation shows much less f_s variation (±8%) compared to trailing-edge modulation (±27%). The nominal switching frequency f_s is chosen 10 times greater than the reference voltage frequency.

3.3 Improved one-cycle control circuit

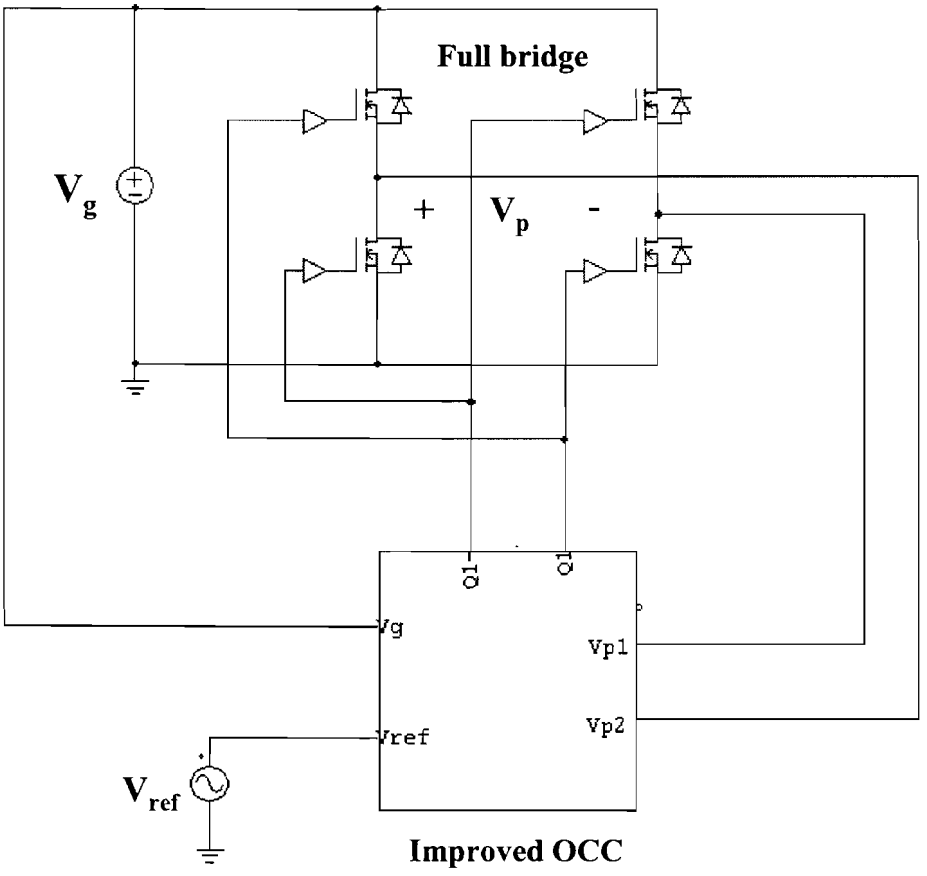


Figure 3.10: OCC used in a full-bridge amplifier

The final OCC circuit used to control a full bridge inverter circuit is shown in Fig. 3.10 and Fig 3.11 shows the actual improved controller. The output signal of the full-bridge is a differential square wave. This differential output signal is directly connected to the loop/error integrator of the OCC. The control circuit uses double-edge modulation which is realized by adding a second adder circuit in the controller. The theoretical waveforms of the circuit are shown in Fig.3.12.

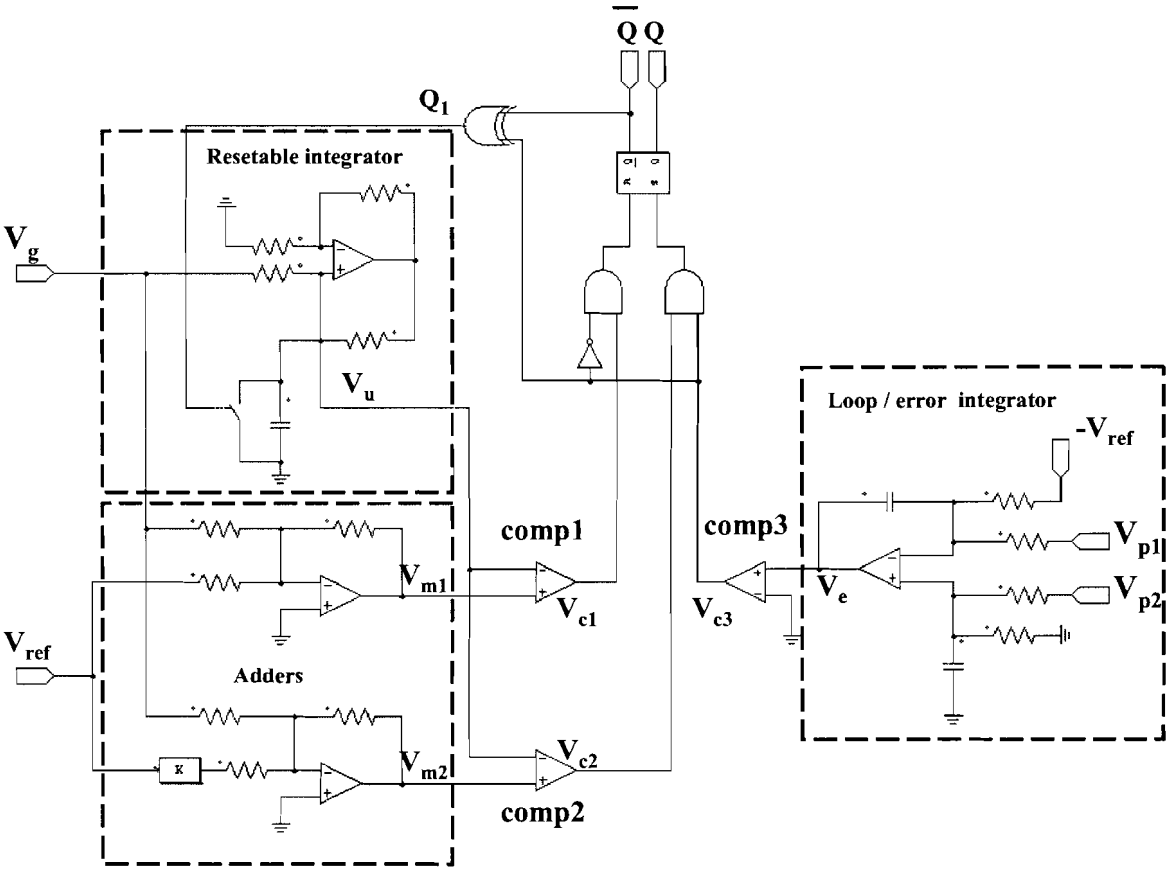


Figure 3.11: Double-edge modulated implementation of the OCC

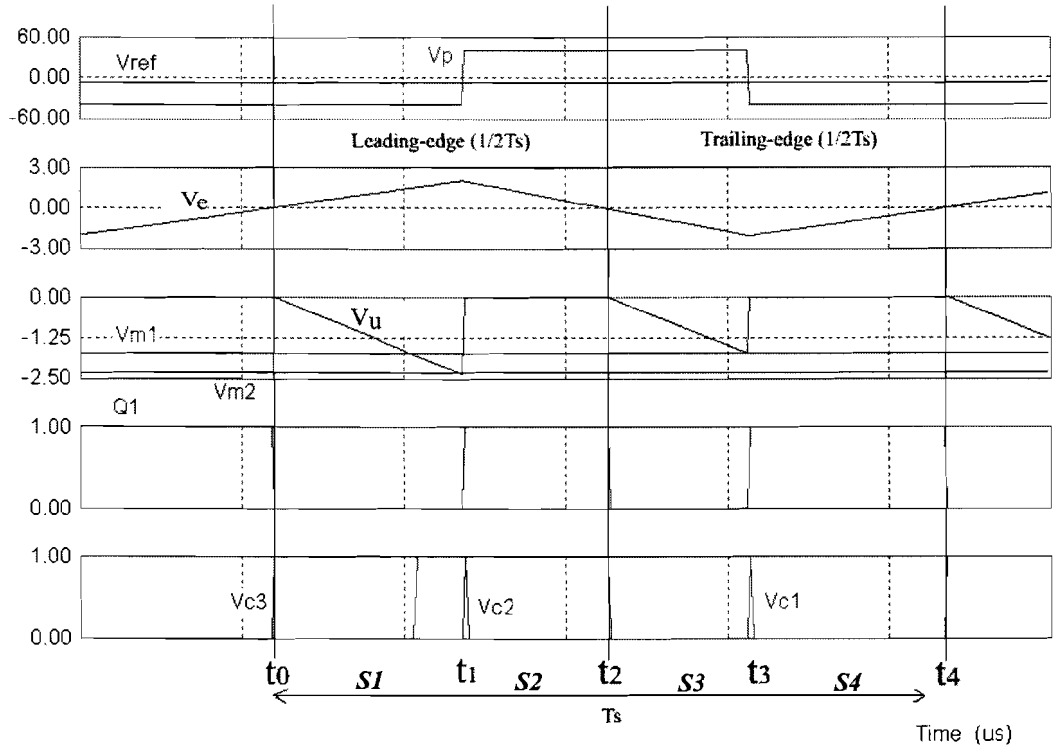


Figure 3.12: Double-edge modulation theoretical waveforms

The circuit operates as follow:
In one switching period four states can be distinguished. These four states are realized by the logic circuitry along with the outputs v_{c1}, v_{c2}, and v_{c3} of the comparators.

state S1 $[t_0,\ t_1]$

The first state is started when the switching cycle starts at t_0 when v_{c3} turns high. The resetable integrator starts a leading-edge modulated half cycle (see Fig. 3.12). During this stage Q and Q_1 are both low, $V_{p2} = V_g$ and $V_{p1} = 0$. The end of this state is reached when the resetable integrator reaches the reference level $V_{m2} = -(V_g - V_{ref})$, the comp2 goes high and Q and Q_1 change both to high.

state S2 $[t_1,\ t_2]$

This state is started at t_1. During this second state the resetable integrator is reset and remains 0. Now $V_{p2} = 0$ and $V_{p1} = V_g$ as Q and Q_1 both changed from low to high. The loop / error integrator integrates until it reaches zero at t_2 and comp3 becomes zero. The first half cycle is then ended and the next state is started.

state S3 $[t_2,\ t_3]$

At t_2 the third state is started and the resetable integrator is triggered again to start a trailing-edge half cycle. This time Q remains high and Q1 has changed to low. Thus the error integrator keeps integrating in the same direction. The end of this state is reached when the resetable integrator reaches the second reference level $V_{m1} = -(V_g + V_{ref})$ at t_3 and compl goes high and triggers to the last state in the cycle.

state S4 $[t_3,\ t_4]$

During this last state Q and Q1 both change to low and high respectively. $V_{p2} = V_g$ and $V_{p1} = 0$. The resetable integrator is kept zero and the error integrator integrates until it reaches zero again at t_4. Then the end of the second half cycle is reached and the whole operation is repeated cycle by cycle.

3.3.1 Resetable integrator

Fig. 3.13 shows the implementation of the resetable integrator. It is a so-called Howland current source with an additional capacitor. If the integrator is configured properly, a constant current, which is independent of the capacitor voltage, flows through the capacitor. As a result a precise linear voltage ramp can be generated.

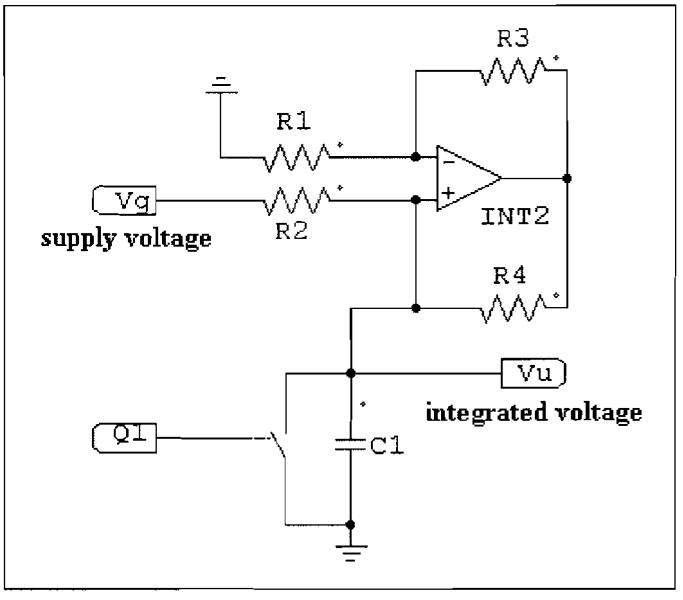


Figure 3.13: Resetable integrator circuit

Additionally, the integrator needs to reset every time the reference level is reached. When the duty-cycle ratio approaches unity, a slow reset time could cause the controller to work improper, for high switching frequencies.

The switching frequency is determined by both the slope of the voltage output ramp of the resetable integrator and the reference voltage level at which the integrator needs to be resetted. From Fig. 3.14 it follows that if the slope of the output voltage ramp V_u is changed, the switching time T_s changes simultaneously. Additionally, if the reference voltage level V_{m1} or V_{m2} (see Fig. 3.11) is adapted, it influences the time T_s too. Concluding, the switching time T_s can be changed by:

- Changing the current through the capacitor, by changing the resistors values of the resetable integrator
- Changing the value of the capacitor $C1$.
- Changing the reference voltage level V_{m1} or V_{m2}.

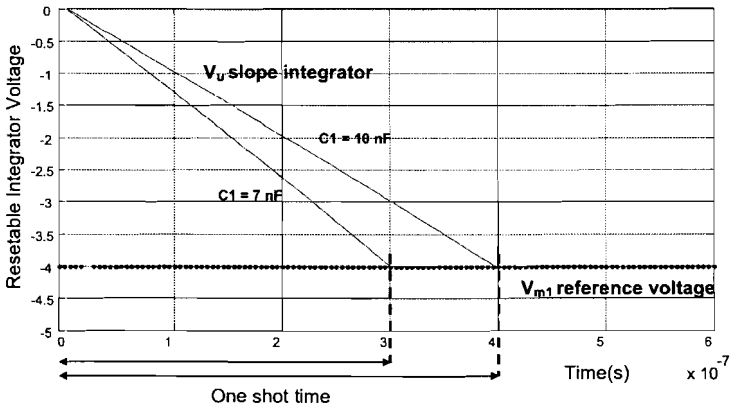


Figure 3.14: Resetable integrator output voltage ($R1 = R2 = 1k\omega, R3 = R4 = 200\omega V_g = 70 + 5 * sin(w * t)$)

Furthermore, the resetable integrator needs to be dimensioned such that for the maximum supply voltage V_g the voltage ramp V_u is kept beneath the saturation voltage of the op-amp. Additionally, a low maximum voltage V_u is advantageous to have a fast resetting of the capacitor.

When the switch is turned on the capacitor is short-circuited and V_u (voltage across the capacitor) becomes zero (reset). During switch off, the capacitor is loaded until it reaches its reference voltage level. The integrator can then be simplified according to Fig. 3.15.

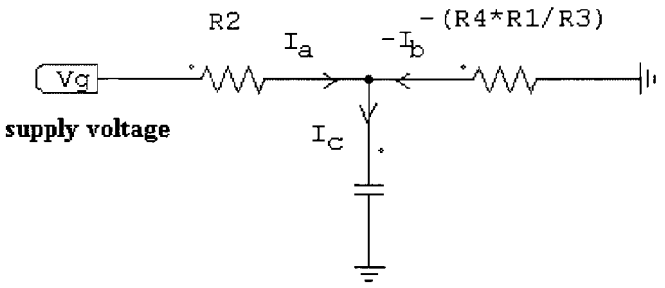


Figure 3.15: Simplified current model

The current through the capacitor is given by

$$I_c = I_a + I_b = \frac{V_g - V_u}{R_2} - \frac{V_u}{-R_1 R_4 / R_3} \tag{3.9}$$

So if $R2 = R4R1/R3$, then the current into the capacitor depends only on the input voltage V_g and $R2$

$$I_c = -\frac{V_g}{R_2} \tag{3.10}$$

and if the input voltage is not constant the capacitor output voltage is then

$$v_u(t) = \frac{1}{C_1}\int_0^t i_c(t)dt = \frac{1}{C_1}\int_0^t -\frac{v_g(t)}{R_2}dt = \frac{-1}{C_1 R_2}\int_0^t v_g(t)dt \tag{3.11}$$

If the supply voltage is assumed to be constant then the output capacitor voltage is given by

$$V_0 = -\frac{V_g t}{C_1 R_2} \tag{3.12}$$

Switching duty-ratio

From the analysis above the limitations of the duty-ratio can be easily calculated. In theory the duty-ratio has a physical limitation that is $0 < d < 1$. However, in practice the duty-cycle is more limited due to for example switch on/ off times or limitations which are the result of the controller. Therefore the duty-ratio limits are

$$D_{min} < d < D_{max} \tag{3.13}$$

Since the switching duty-cycle is determined by the resetable integrator is the duty-ratio is limited by the resetable integrator as well. The limitation is determined by the slope of the integrator voltage. This effect is depicted in Fig. 3.16. The maximum duty-cycle is limited by the minimum reset-time which is needed tot discharge the reset capacitor.

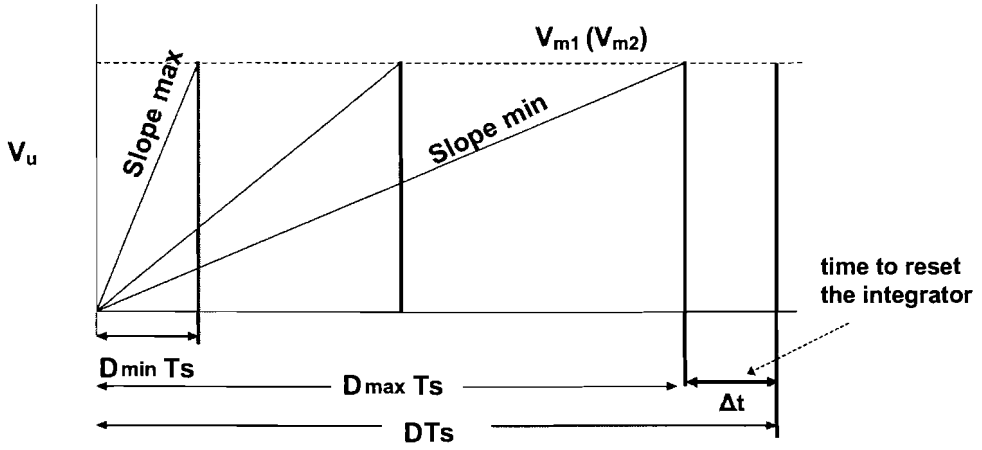


Figure 3.16: Limitation of the duty-ratio

The integrator voltage slope follows from equation (3.12) and is given by

$$\frac{dV_u}{dt} = -\frac{V_g}{C_1 R_2} \tag{3.14}$$

from this equation and from Fig. 3.14 it follows that if the integration constant R_2C_1 is constant the duty-ratio is determined by the supply voltage V_g and the reference voltage V_{m1} or V_{m2}. The minimum slope which sets the minimum duty-cycle is determined also by the slewing-rate of the integrator op-amp.

3.3.2 Error integrator

Fig. 3.17 shows the differential integrator. The integrator integrates the error signal and ensures that the error is zero at the end of every cycle. The error integrator is implemented using a differential op-amp with an additional reference input. Resistor

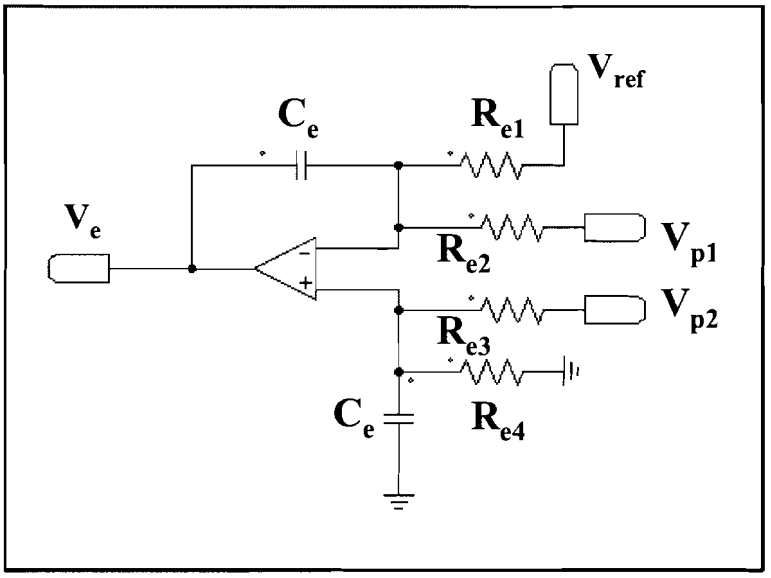
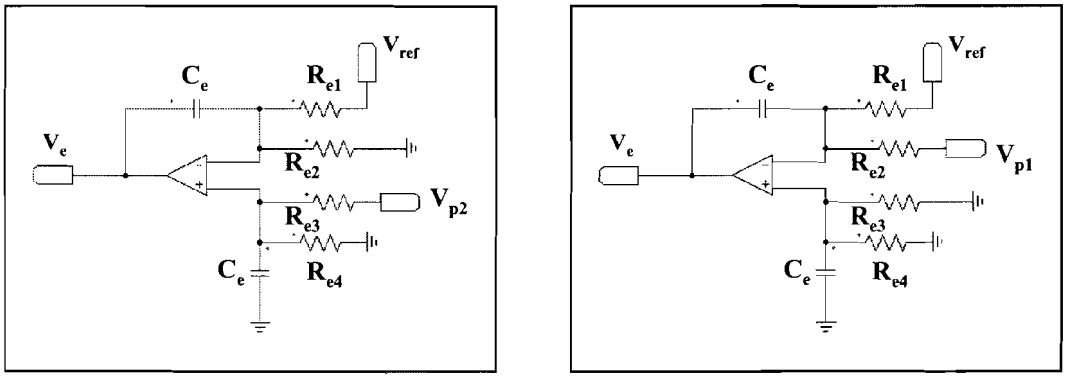


Figure 3.17: Differential error integrator

R_{e4} is added at the non-inverting input of the error integrator to preserve the symmetry. This circuit requires careful matching of the resistors and capacitors otherwise a poor common mode rejection ratio will result. The CMRR due to mismatch in components is given by

$$CMRR \simeq \frac{1 + sC_eR_e}{s\Delta(C_eR_e)} \tag{3.15}$$

where $\Delta(C_eR_e)$ is the difference in time constants between the inverting and non-inverting input.



(a) stage 1 (b) stage 2

Figure 3.18: Differential integrator operating stages.

To gain a better understanding of its operational principle, the differential inte-

grator can be split up in two stages. In the first stage, Fig. 3.18(a), V_{p1} is connected to earth and V_{p2} is high. In the second stage Fig. 3.18(b) V_{p2} is connected to earth and V_{p1} is high. Since the switching frequency is high we can assume that the input voltage V_g is constant during one switching cycle. Therefore we can write the following equations for stage 1 and stage 2 respectively

$$\Rightarrow V_{e(stage1)} = \left(1 + \frac{Z_{Ce}}{R_{e1}//R_{e2}}\right)\left(\frac{Z_{Ce}//R_{e4}}{Z_{Ce}//R_{e4} + R_{e3}}\right)V_{p2}T_{on} + \left(1 + \frac{Z_{Ce}}{R_{e1}//R_{e2}}\right)\left(\frac{Z_{Ce}//R_{e3}}{Z_{Ce}//R_{e3} + R_{e4}}\right)V_{ref}T_{on} \tag{3.16}$$

$$\Rightarrow V_{e(stage2)} = \left(1 + \frac{Z_{Ce}}{R_{e1}}\right)\left(\frac{Z_{Ce}//R_{e3}}{Z_{Ce}//R_{e3} + R_{e4}}\right)V_{ref}T_{off} + \left(1 + \frac{Z_{Ce}}{R_{e2}}\right)\left(\frac{Z_{Ce}//R_{e3}}{Z_{Ce}//R_{e3} + R_{e4}}\right)V_{ref}T_{off} - \frac{Z_{Ce}}{R_{e2}}V_{p1}T_{off} \tag{3.17}$$

with $Z_{Ce} = \frac{1}{sC_e}$

The summation of the two gives an expression for the error voltage during one half of the cycle. (leading or trailing-edge)

$$V_e = V_{e(stage1)} + V_{e(stage2)} \tag{3.18}$$

3.3.3 Adder circuit

The two adder circuits in the final circuit serve to realize the double-edge modulation. They provide two adapted reference voltages V_{m1} and V_{m2}. See the complete circuit depicted in Fig 3.11. Adapted reference voltage V_{m1} is needed to start the trailing-edge modulation in the first half cycle. Adapted reference voltage V_{m2} is needed to start the leading-edge modulation in the second half cycle half cycle. The summed voltage $V_g \pm V_{ref}$ is scaled down such that the resetable integrator can reach the voltage. For adder 2 the reference voltage must be inverted. Thus an additional inverting amplifier is needed, as shown in Fig. 3.19.

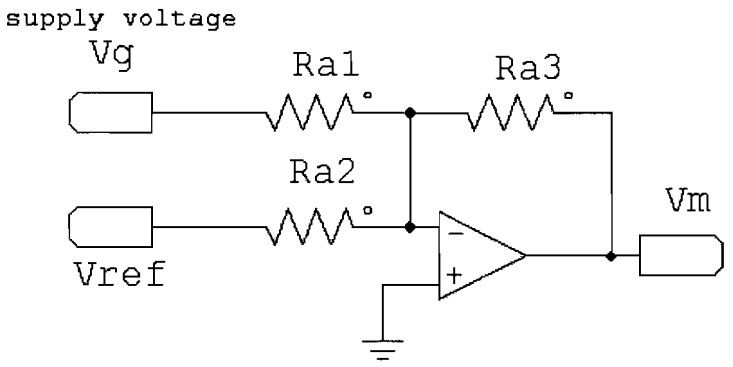


Figure 3.19: Adder circuit

3.4 Sensitivity of the controller

3.4.1 Error integrator

The most component-sensitive part of the OCC is the error integrator. The integrator is implemented with an additional input for the reference voltage. To operate properly, the integrator needs to be configured symmetrically, thus, components at the inverting input must be identical to the components at the non-inverting input. This is necessary to have the same RC time for the positive and negative slope, so that the error can be made zero every cycle.

Fig. 3.20 shows the influence of a 5% deviation in one of the resistors. It results in an error in the period time and thus in the switching frequency. A mismatch of 5% results in an deviation of 3.5% in the switching frequency.

A mismatch of opposite components in the differential integrator, due to their tolerance deviations has a larger impact on the performance. The power supply ripple rejection (PSRR) and the Total Harmonic distortion (THD) will suffer from it. Furthermore, there will be an error in the DC output voltage.

Since the PSRR is a good characteristic to measure the performance of the controller this characteristic is considered in the sensitivity simulations. The results are obtained by means of simulations as described in chapter 4. In Table 3.1 the PSRR versus different component tolerances are shown. The switching frequency is 245 kHz.

From Table 3.1 it is clear that a deviation in the resistors has a larger impact on the performance than the same deviation in the capacitor. This is obvious since the product of R_{e1} and C_{e1} determines the speed of the integrator and R_{e1} is much larger than C_{e1}.

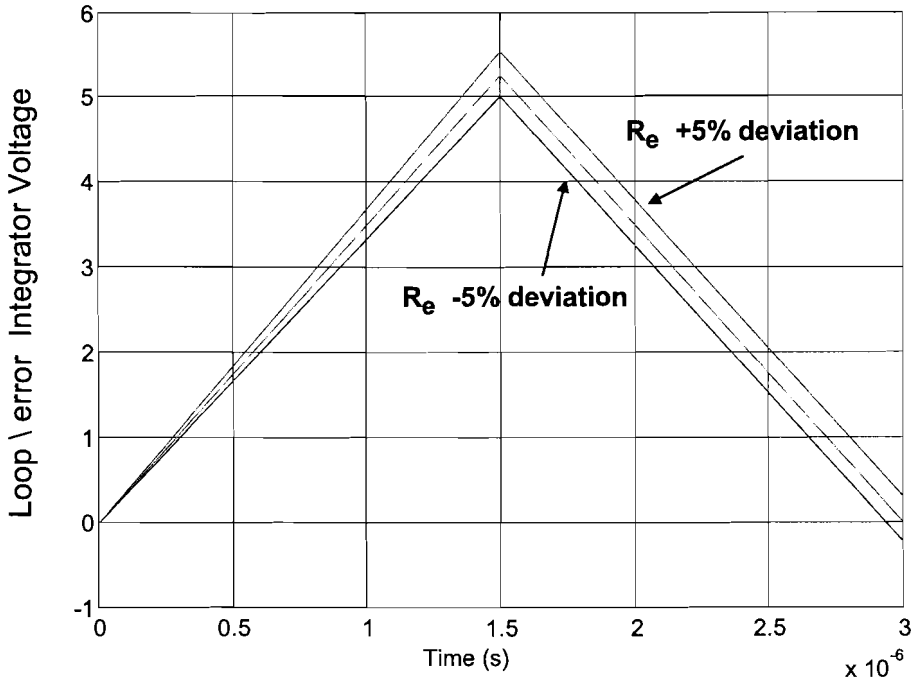


Figure 3.20: Error integrator fault

Table 3.1: PSRR (dB) for different component tolerances in the error circuit

	Ideal components	0.1%	0.5%	1%	5%	10%
R_{e1}	-92.31	-72.72	-58.28	-52.02	-38.13	-32.70
C_{e1}	-92.31	-90.22	-84.46	-70.02	-49.98	-42.60

3.4.2 Adder circuit

The adder circuit, however, is less sensitive to component (only resistor) deviations compared to the error integrator. A component deviation results in a change of the switching frequency. A pair of switches changes their state whenever the resetable integrator voltage reaches the adder voltage. If the adder output voltage changes, due to the tolerances deviations of the resistors it takes more or less time for the resetable integrator voltage to reach this adder voltage. Since there are two identical adders in the circuit a tolerance deviation results in a possible wider range of switching frequency variety. In Table 3.2 these effects are shown.

Table 3.2: PSRR (dB) for different component tolerances in the adder circuit

	Ideal components	0.1%	0.5%	1%	5%	10%
Ra1	-92.31	-90.05	-83.21	-86.94	-73.45	-67.83

3.4.3 Resetable Integrator

A deviation in the component value in the resetable integrator has the least impact on the performance of the circuit. Since the resetable integrator operates in its linear region a value deviation results in a slight change in the sloop of the integrator and therefore, a small change in the switching frequency. Except the change in performance of the controller due to the change in switching frequency the component value deviation has no other influence on the performance.

Table 3.3: PSRR (dB) for different component tolerances

	Ideal components	5%	10%
R1	-92.31	-86,00	-82.93
R2	-92.31	-84,00	-77.03

3.5 Delay time and its impact on the performance

Delay time in the control circuit directly influences the switching frequency and indirectly decreases the performance. The delays occur for example when the resetable integrator completes its one-shot (t_{on}) to reset the flip-flop which changes on its turn the state of the input signal V_p. This is depicted in Fig. 3.21 as $\Delta t1$. Thus from the moment that the one shot completes, it takes a small delay before the error integrator really changes its integration direction. Depending on the slopes of the error integrator this can have a relative small or large effect on the period time. This effect is depicted in Fig 3.21 as $\Delta t2$

The same effect can occur at the moment the error integrator equals zero and sets both the flip-flop to change the state of the bridge voltage and the resetable integrator to start integrating. As mentioned before these delays influence the switching frequency, by decreasing it. However, despite these delays the controller can still operate correctly but only with a lower switching frequency. To compensate these delays a small resistor can be added in the resetable integrator in series with $C1$ to make the one-shot slightly faster. Another solution is by simply increasing the frequency by choosing a smaller capacitor for instance. In the next chapter the impact on the PSRR caused by time-delays is quantified.

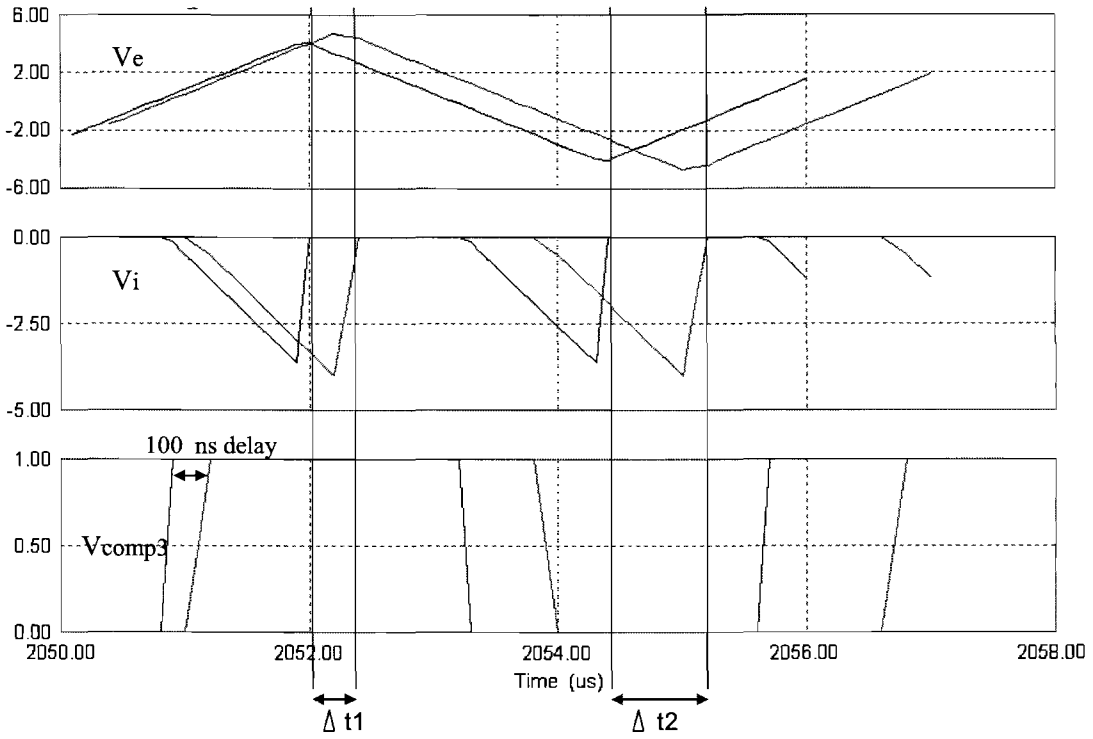


Figure 3.21: Influence of a delay in the error integrator

Chapter 4

Simulations

The OCC has also been simulated in the programmes PSIM and Matlab. The controller is used in the simulations to control a full-bridge power amplifier, as shown in Fig. 4.1. These simulations measure the power supply ripple rejection (PSRR), and how precise the reference voltage is followed. The PSRR is defined as the ability of an amplifier to maintain its output voltage as its power supply voltage is varied.

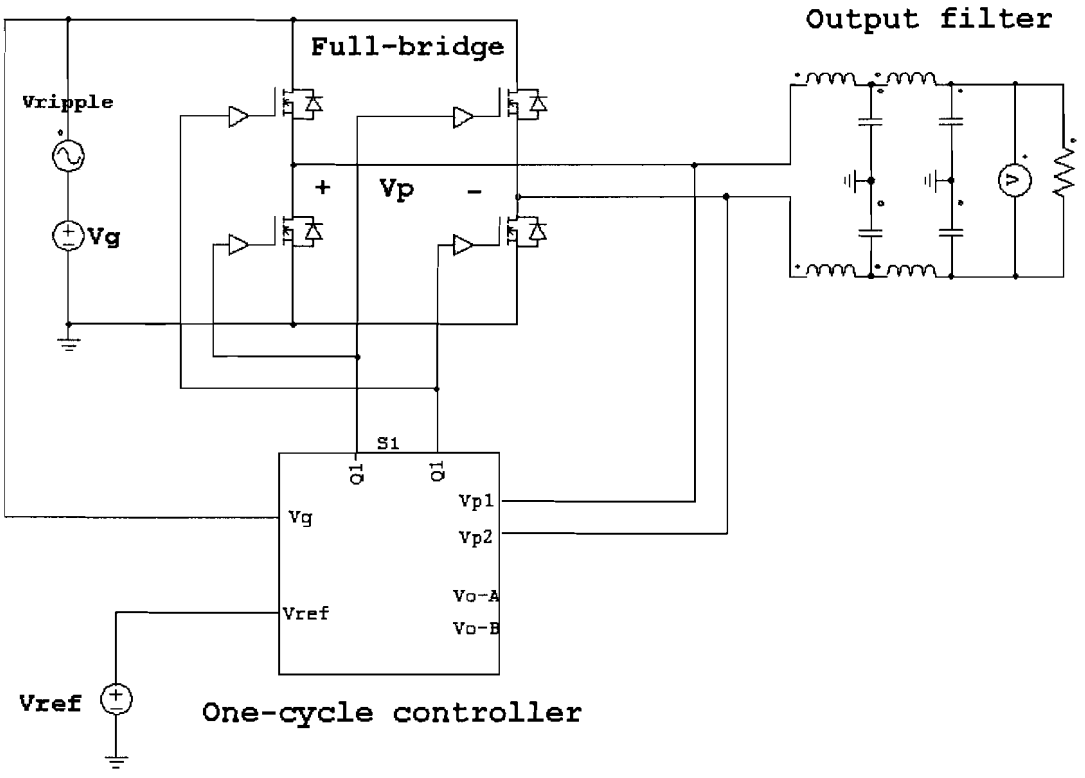


Figure 4.1: OCC used in a full-bridge amplifier

Primary, the full-bridge amplifier is simulated in PSIM. Through the time-domain waveforms, a good insight in the operating of the controller can be gained. After the simulations in PSIM, the PSRR are calculated in Matlab with the simulation data obtained from PSIM. Since the distortion in the performed simulations is mainly caused by the power supply ripple, the PSRR will be given in detail.

The first simulation that has been done aimed at the calculating the PSRR for different dc reference voltages. As a reference the full-bridge power amplifier has also been simulated in open-loop mode. The PSRR is then compared with the PSRR of the amplifier with OCC. This was done for different reference values. Fig. 4.2 shows the open loop simulation circuit. All these simulations were done for a switching frequency of 250 kHz, an input voltage of 60 Volt, and 10% -1 kHz ripple.

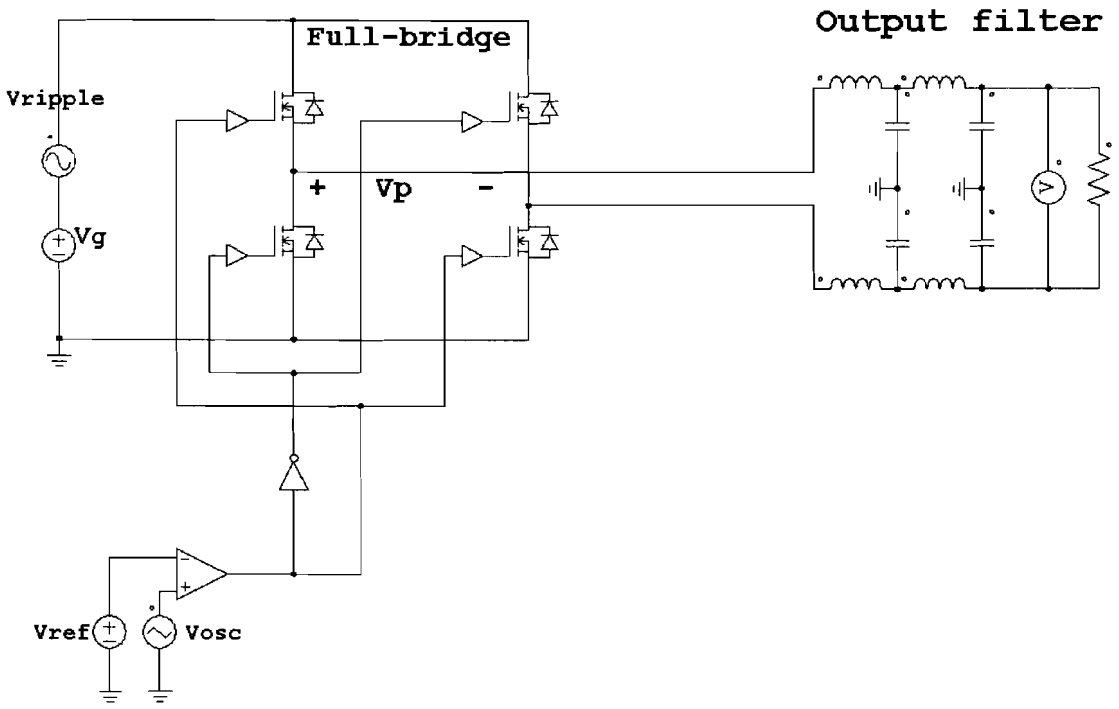


Figure 4.2: Open loop full-bridge amplifier

The results of these simulations (Fig. 4.3) show that OCC considerably improves the system performance if compared to open-loop control, especially when the reference voltage differs from 0 V (50% duty cycle).

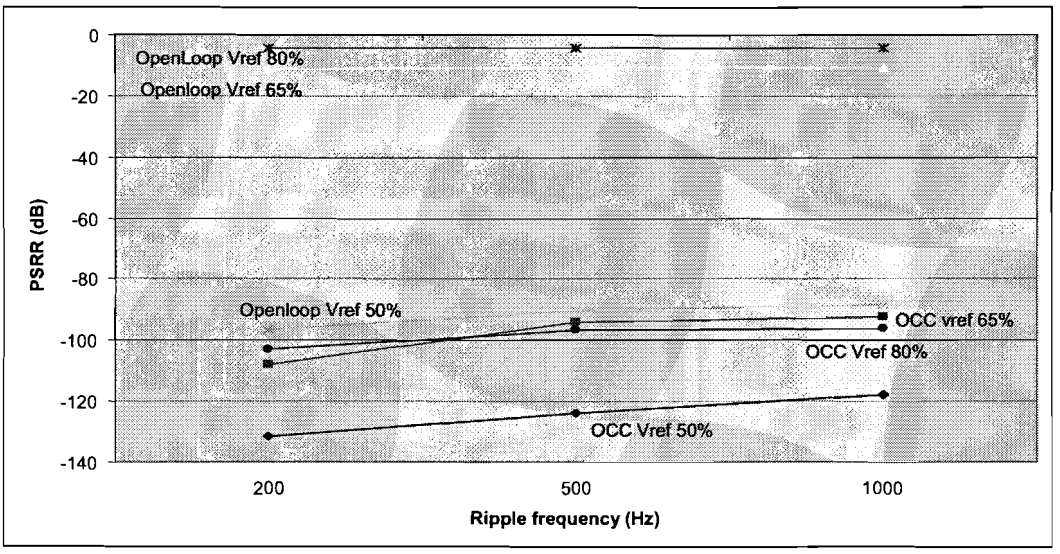


Figure 4.3: OCC compared to open loop control for different reference voltages

Further, the OCC was analyzed in more detail by means of simulations. Firstly, the performance of the controller for different switching frequencies has been simulated. The results are depicted in Fig. 4.4

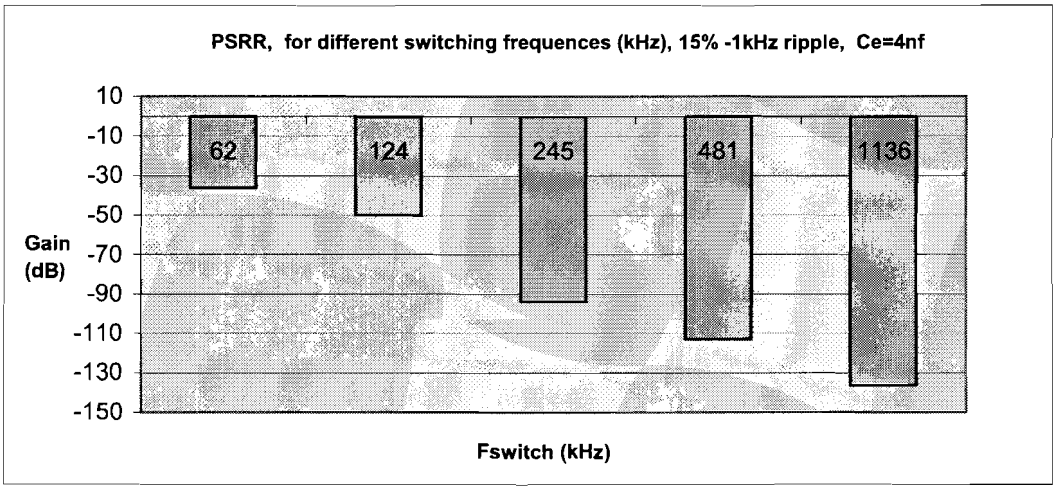


Figure 4.4: PSRR for different switching frequencies

The simulation time step has also some influences on the simulation results. These time steps are translated in the circuit as the rise times for the components (i.e. comparator, logic components). Typical rise times for logic components, comparators, etc., are in the range of $20 - 100$ ns. These time steps could also be seen as delays in

the circuit. The switching frequency is directly influenced when the time step (rise time) is adapted. This change in switching frequency has on its turn an impact on the performance of the controller. Fig. 4.5 shows the change in frequency as well as the PSRR for different time steps.

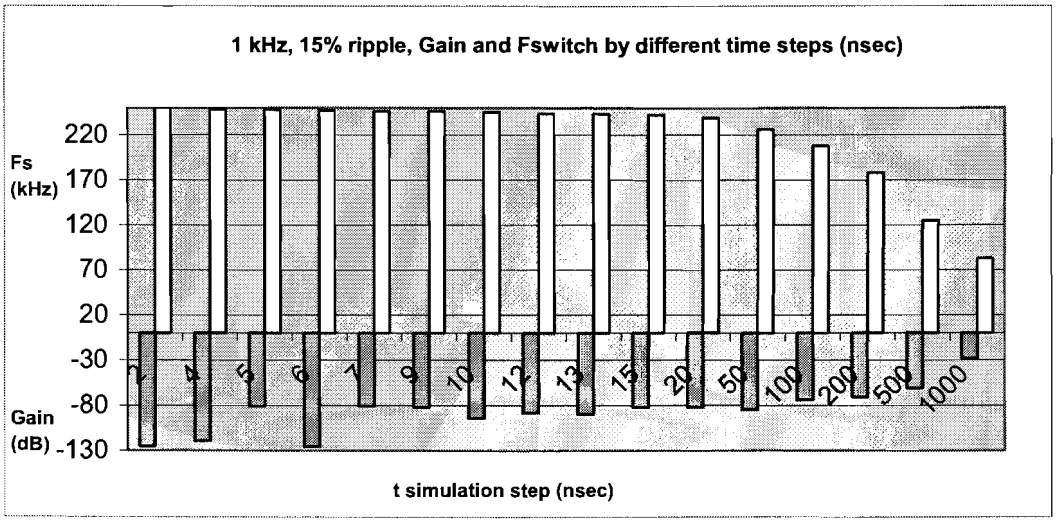


Figure 4.5: PSRR and switching frequency versus delay-time

Furthermore, the PSRR is also measured for different ripple frequencies in the range of 100 Hz - 5 kHz. Fig. 4.6 shows, as predicted, a decrease in the PSRR when the ripple frequency increases.

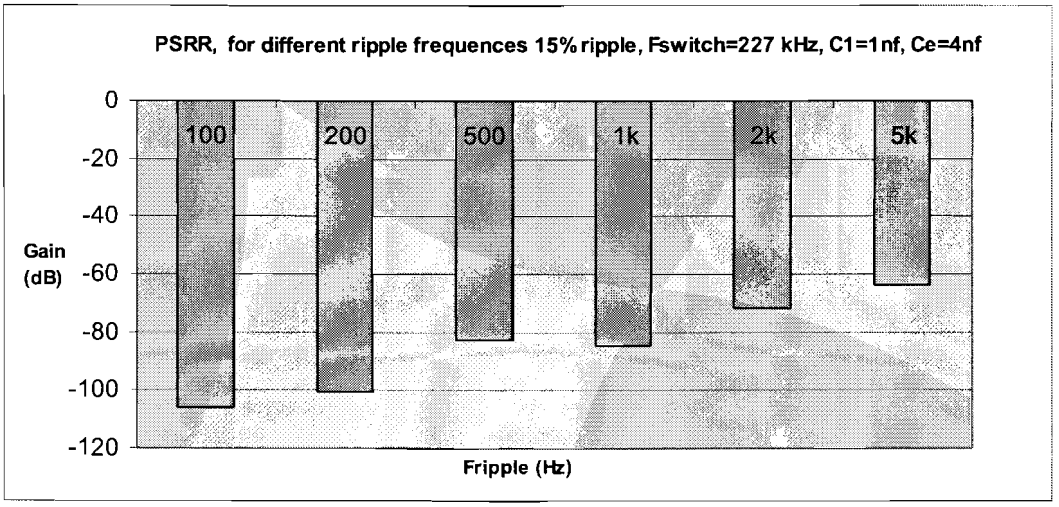


Figure 4.6: PSRR for different ripple frequencies in the input voltage

In conclusion, the OCC has shown good performances concerning the power supply ripple rejection. This was in accordance with the expectation. Since the main characteristics of the OCC is its ability to reject power supply disturbance. Further, simulations have shown that the switching frequency plays also a role in the performances of the OCC. The higher the switching frequency the better the OCC performs if the power-stage behaves ideal. The power supply ripple frequency has also some influence on the performance. As the frequency of the ripple is lower than the controller rejects this ripple better as expected.

Chapter 5

Practical Implementation

5.1 Controller implementation

Figure 5.1 shows the practical implementation of the OCC used in a class-D amplifier and Table 5.1 shows the system parameters. The final implementation consist of three parts, the controller(OCC), the power stage(UCD), and the outer feedback loop(discussed in chapter 7).

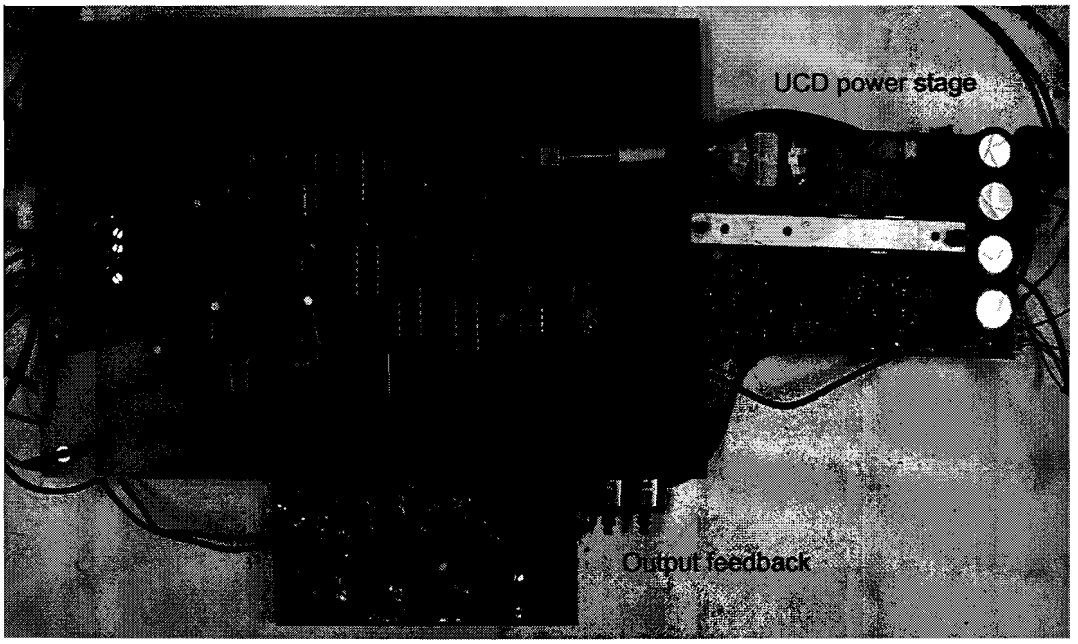


Figure 5.1: Implementation of the OCC power amplifier with output feedback loop

For the power stage of the implementation circuit, a commercially available unified class D (UCD) amplifier was used. The control part of the UCD amplifier is simply removed so that only the power stage remains and could be used for the OCC.

The results of the OCC amplifier are then compared with the performances of the self-oscillating UCD power amplifier.

Supply voltage	$V_{dc} = 60$ V
Maximum output power	$400W$ into 4 Ω
Switching frequency	$F_s = 200 - 400$ kHz
Output load	4 and 8 Ω
Amplification	$A = 27$ dB

Table 5.1: System parameters of the circuit

The first step in the practical design is the implementation and testing of all sub-circuits of the controller individually. This is primary done with a breadboard. This was useful to find out how the components needed to be connected and if the sub-circuit worked well. However, for a good and accurate functioning of the controller a PC board which is hand wired, was needed. After the PC Board was working properly and all the capacitor values, resistor values, etc. were finalized, a real PCB is designed in order to further improve the accuracy and to minimized transient currents, trace inductance and capacitance. The PCB is designed in the programme PCAD.

The most critical component used in the controller is the Operational amplifier. This component is used in all three the sub circuits(i.e resetable integrator, differential error integrator, and summers). Op-amp AD8055 is chosen for this purpose. Careful attention has been given to the selection and implementation of this component. The op-amp needed to have a low distortion, a low offset, and a high slew. The slew rate of the op-amp needs to be larger than the maximum output voltage swing of the resetable integrator. For the resetable integrator circuit the minimum output voltage swing is

$$\frac{dV}{dt} = \frac{5}{(2F_s)^{-1}} = 4V/\mu s \tag{5.1}$$

This is for the case when the resetable integrator needs a total switching half-cycle to reach its reference voltage. However, the resetable integrator should be able to reach its reference level faster depending on the duty-cycle and therefore the output voltage swing can be higher. This is effect is illustrated in Fig. 3.16. Thus the slew rate of the op-amp should be larger than the maximum output voltage swing of the integrator. Suppose that the resetable integrator should reach its reference with a dutycycle of 0.1 then the voltage swing would be 10 times $4V/\mu s$, or $40V/\mu s$. A minimum duty-cycle slewing time of several tenths % of the switching half-cycle is reasonable. As a result the op-amp slew rate should be at least larger than about

$SR > 100V/\mu s$

To reset the integrator an analog multiplexer 74HC4052 is used. The device is an high speed switch with low "on" resistance and low "off" leakage. For the logic circuitry, logic gates from the HEF series are used. And for the comparator the op-amp LM319 is chosen. These components were tested and found to be suited to be used in the controller. In appendix A a complete implementation scheme is added.

5.2 Time domain signal measurement

To evaluate the system performance, the OCC power amplifier circuit is measured according to the setup shown in Fig. 5.2. The figures in the following section summarize the fundamental time domain waveforms of the audio amplifier including the OCC.

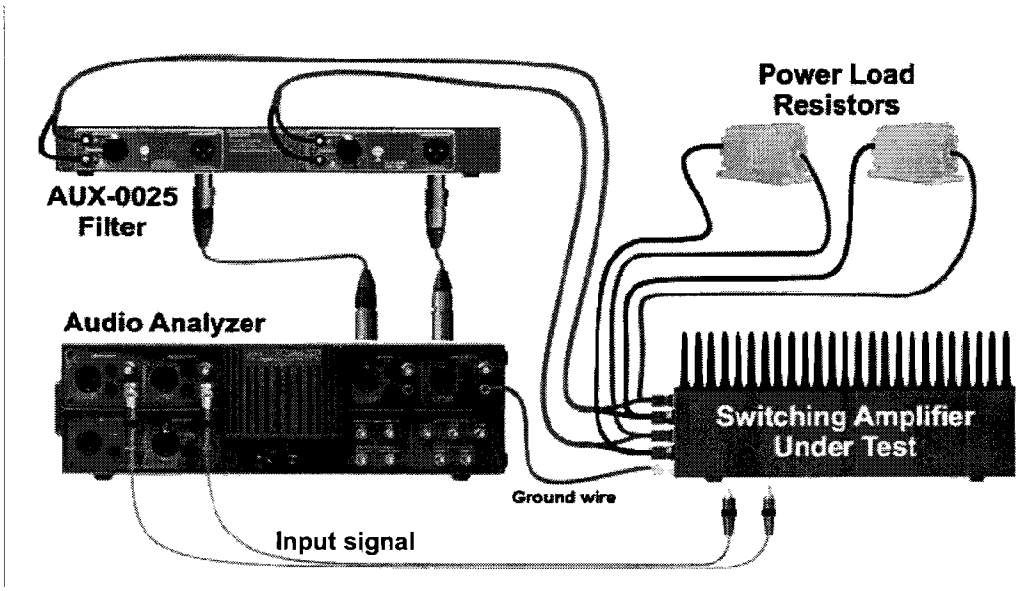


Figure 5.2: Measurement setup with the Audio Precision instrument

Fig. 5.3 shows a reference input versus amplified output signal for an output power of 30 W. The reference signal is a sinusoidal with a frequency of 1kHz and an amplitude of 0.8 Volt. The amplification is 27 dB.

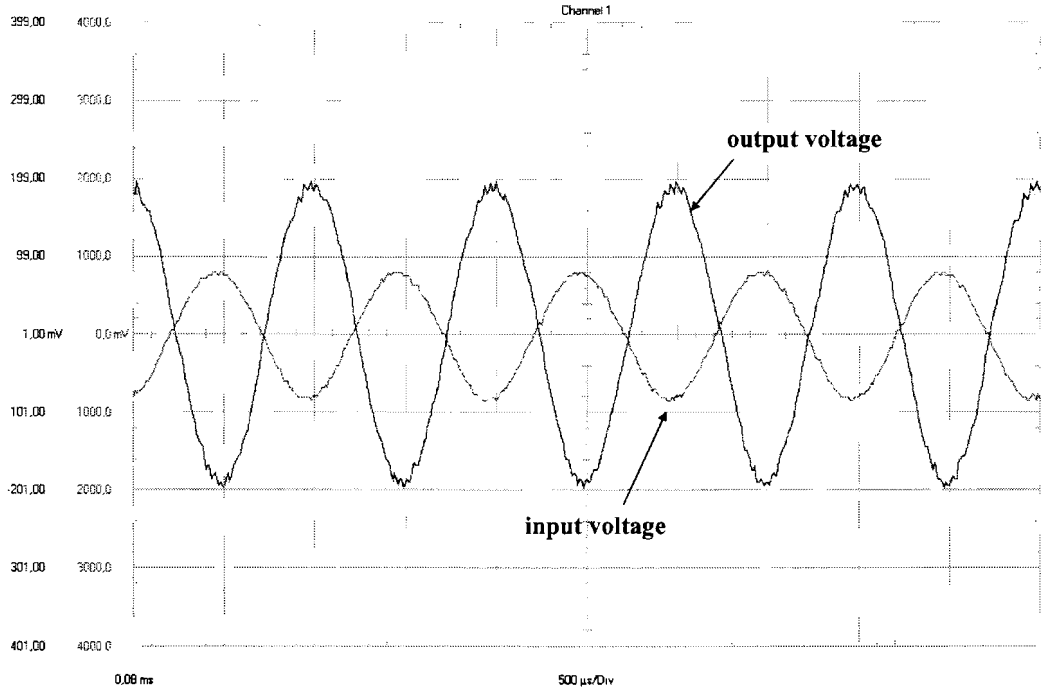
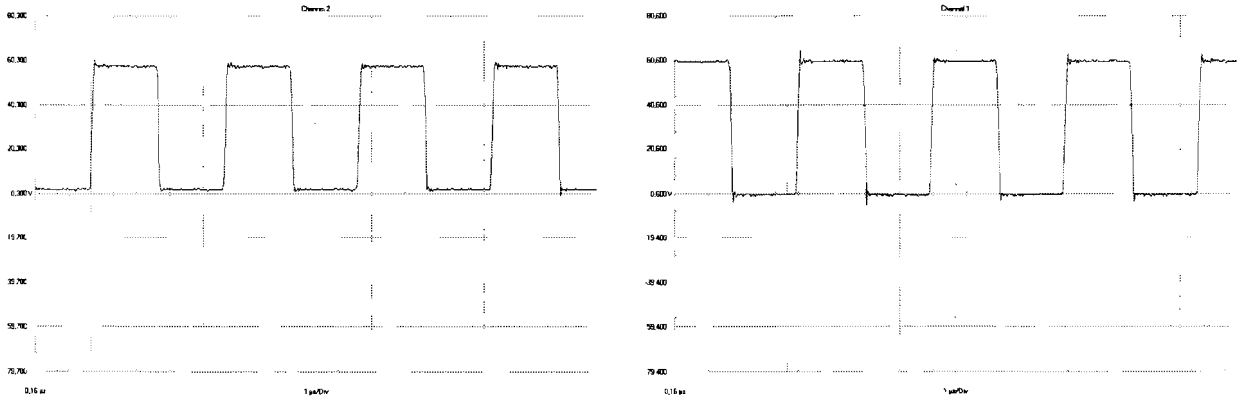


Figure 5.3: Input and amplified output voltage (50x attenuation), 30 W

The output voltage of both the full-bridge legs are depicted in Fig. 5.4. As can be seen from the figures, the maximum bridge voltage is 60 V. Furthermore, it can be seen that there is small deviation in the maximum voltage of both half-bridge legs. This deviation is the result of the asymmetry in the power-stage. However, this deviation should not influence the performance as the OCC takes out the difference.



(a) Left side output voltage (b) Right side output voltage

Figure 5.4: Square wave power stage voltage outputs .

In Fig. 5.5 the differential error integrator is shown. The signal is a triangle waveform generated by the the integration of the full-bridge differential voltage shown in Fig. 5.4. The waveform is distorted slightly at the tops, what is caused by the switching of the MOSFET's.

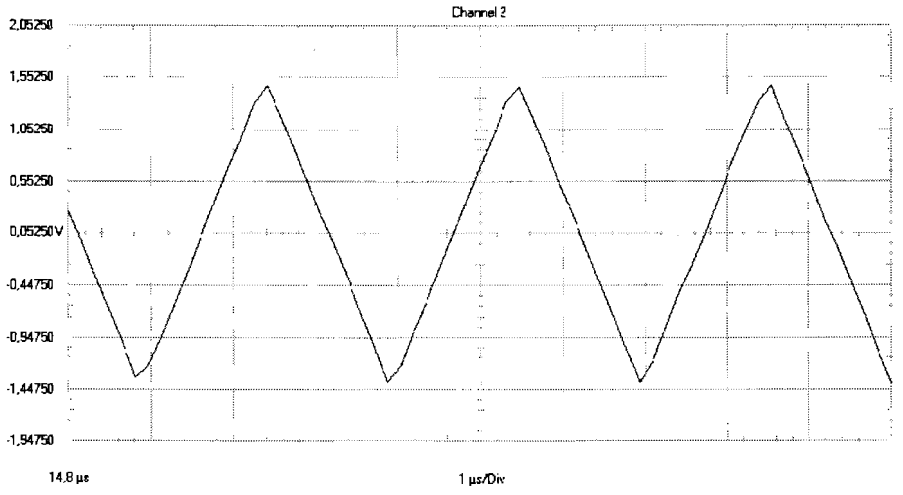


Figure 5.5: Differential error integrator voltage

The switch drive signal for the resetable integrator and the integrated output signal are depicted in Fig. 5.6. This measurement is done to test the resetable integrator. The drive for the integrator is a pulse-train with a frequency of 250 kHz in this picture. Every time the switch drive signal is high the resetable integrator is reset. The reset time takes about 100 ns.

In Fig. 5.7 the resetable integrator voltage and the comparator output voltage is shown while the amplifier is operational. From the figure it can be seen that the comparator is set high every time the resetable integrator reaches the reference voltage. Then when the resetable integrator is turned off again the comparator is set to low after a small delay caused by the logic circuitry.

In this figure the reference signal is not zero and therefore the resetable integrator has an alternating maximum level. There is also a small offset in the resetable integrator. This offset has some impact on the the switching frequency but does hardly influence the accuracy. However the switching frequency must be adapted to meet the desired switching frequency. This is the same effect as described in section 3.21. Furthermore, it should be noticed that the switching frequency of this signal is twice that of the bridge switches, namely 800kHz, in order to realize the double-edge modulation.

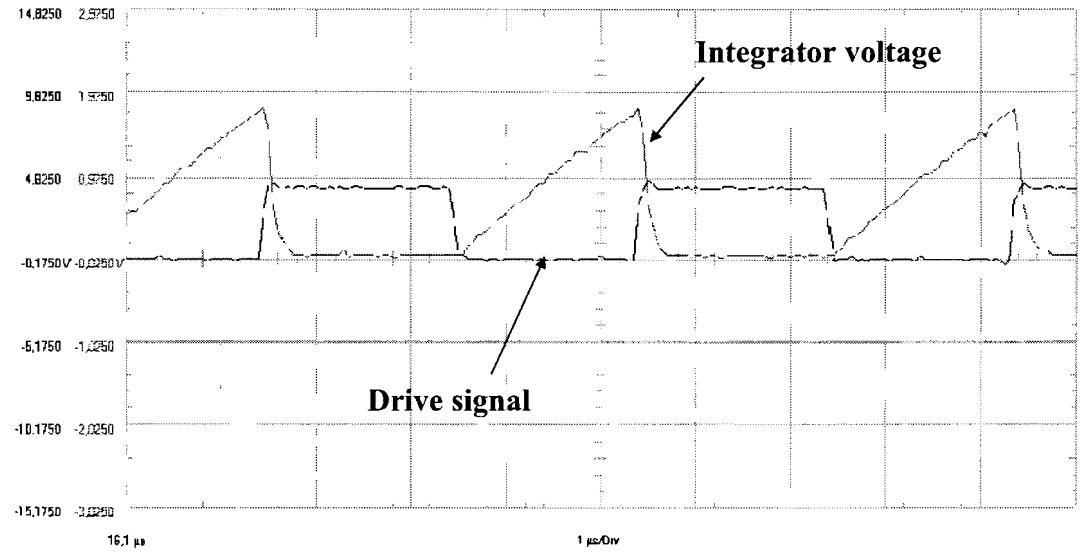


Figure 5.6: Resetable integrator voltage and switch drive signal

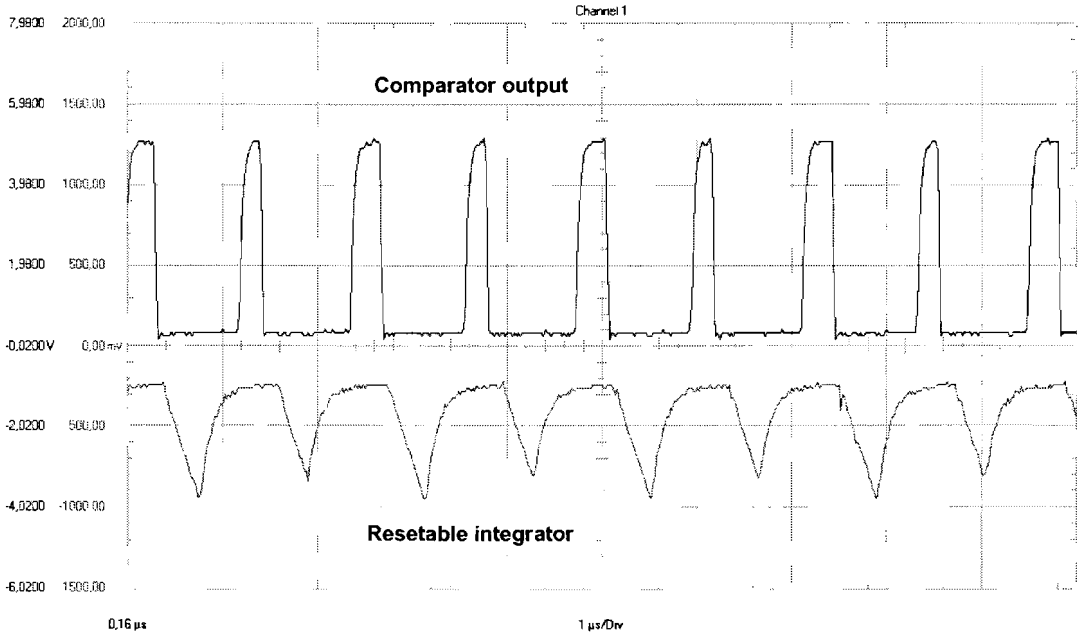


Figure 5.7: Resetable integrator voltage and comparator output voltage

Chapter 6

Results

6.1 THD+N measurement

The first measurement that was performed is the THD+N versus power. This measurement combines the effects of white noise, distortion, and other undesirable signals into one measurement and relates it directly to the fundamental frequency. The analog generator sweeps the input voltage amplitude from low to high at a fixed frequency of 1 kHz. The output signal harmonics are then measured at specified voltage steps, and the output power is calculated for a given load impedance value that is provided to the audio analyzer. This value is then divided by the amplitude of the fundamental frequency and graphed as a percentage of the fundamental.

The THD+N measurements are performed for different output loads, i.e 8 Ohm, 4 Ohm, and no load. For each case the OCC power amplifier (without output feedback) is compared with the UCD power amplifier and graphed in one plot. These three measurements are depicted in Fig. 6.1 to 6.3.

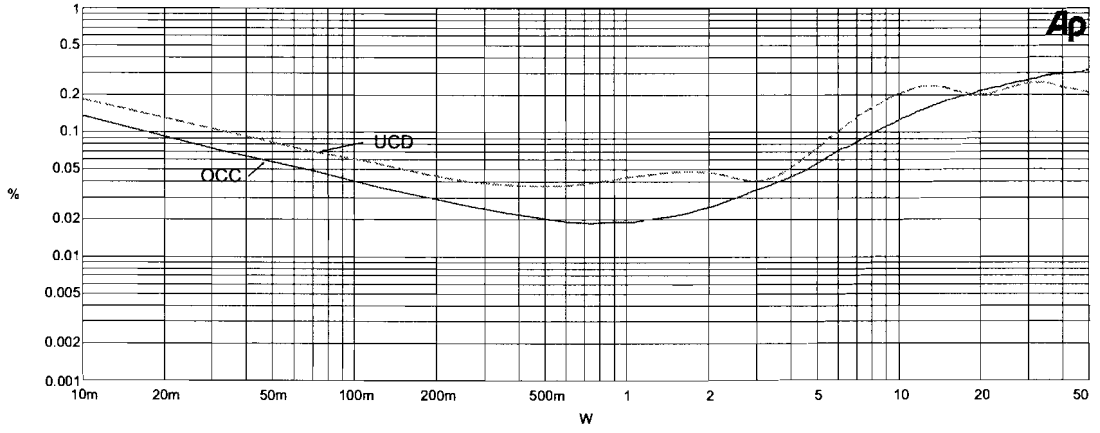


Figure 6.1: THD+N versus power, OCC and UCD power amplifier, 4 Ohm load

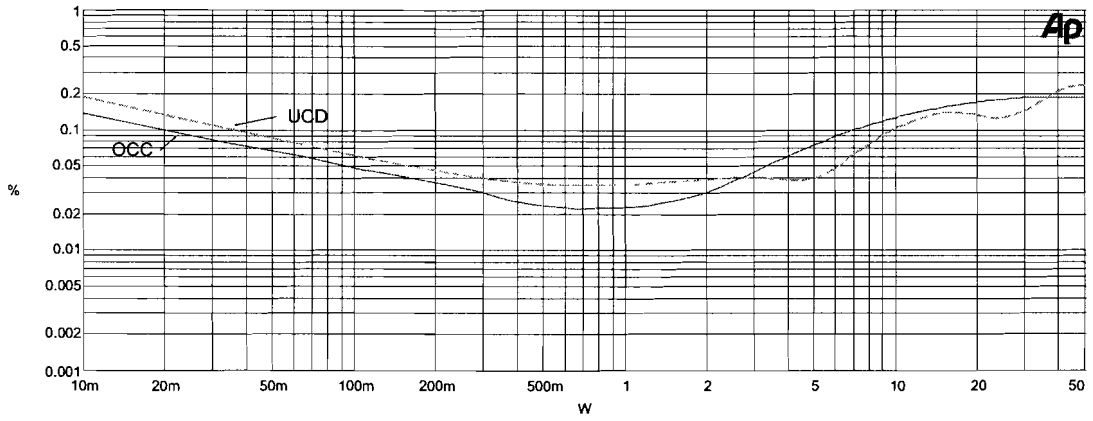


Figure 6.2: THD+N versus power, OCC and UCD power amplifier, 8 Ohm load

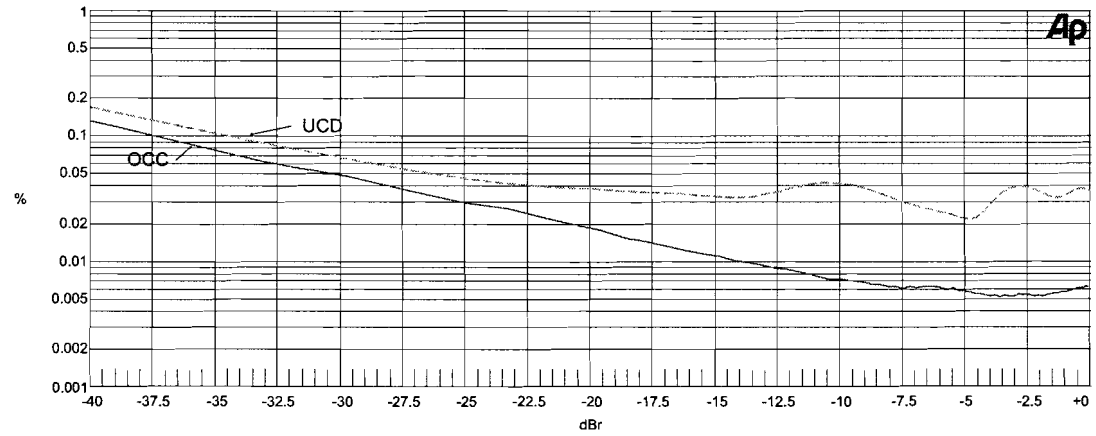


Figure 6.3: THD+N versus amplitude, OCC and UCD power amplifier, no load

Figures 6.1 and 6.2 show the THD+N versus power curve for both the UCD power amplifier and the OCC power amplifier for a load of 4 Ohm respectively 8 Ohm. Fig. 6.3 shows the THD+N versus audio level, since there was no load at the output and therefore no power is transmitted to the output.

From the Figures it follows that the OCC power amplifier has a slightly better THD+N reduction compared to the UCD power amplifier. Moreover these experimental results indicate that the one-cycle controlled switching power amplifier has a THD+N performance comparable to commercial high fidelity linear power amplifiers. When the power amplifiers are driven without load (no output current) it can be seen that the OCC power amplifier performs significantly better than the UCD power amplifier. This is depicted in Fig. 6.3

The higher distortion of both power amplifiers at low output power is due to the decrease in signal-to-noise ratio caused by the fixed noise floor. The measurement suffers also from some typical low frequent noise as will be clear in the FFT plots in the next section. In the design of the OCC and the implementation with the power stage not much attention is paid to signal routing. An improvement on this can result in a better performance.

Furthermore, it should be noticed that the THD+N increases also when the power increases. This could be caused by imperfection in the power stage such as:

1. The main cause of the nonlinearity in the power stage is the timing errors added by the gate drivers, such as dead-time and on/off-time. Especially the error due to the dead-time can affect the THD+N significantly when the power increases. During dead-time load current commutates through the MOSFET body diodes. The diode conduction during these dead times leads to a duty cycle error at the output of the power stage. This duty-cycle error increase when the modulation depth increases. Therefore the distortion will be larger with the increase of power.

2. Another cause is the presence of undesired characteristics in the switching devices, such as finite ON resistance, finite switching speed and ringing on transient edges.

3. Another cause is the non-linearity in the output low-pass filter. Since in the measurements there is no output feedback and therefore disturbance in the output are not rejected.

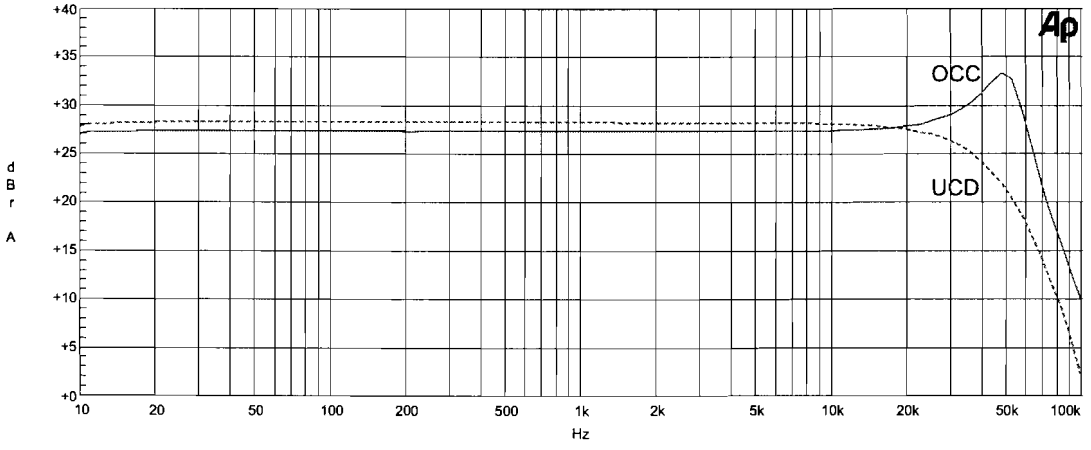


Figure 6.4: Gain versus frequency plot

The effect of the filter is also noticeable in Fig. 6.4 The Figure shows the gain versus frequency plot of the OCC power amplifier. The amplifier is under damped at the filter frequency. In Fig. 6.4 the same measurement is depicted for the UCD power amplifier. The high frequency gain amplification could be damped by an output feedback in order to improve the distortion.

To gain some more insight about the distortion FFT analysis are performed and discussed in the next section.

6.2 FFT analysis

The FFT provides a convenient way to examine the spectrum of noise to see which components are influencing or limiting the performance. Displaying the spectrum of the measured THD+N in the previous section gives a complete picture for the whole audio band. The frequency spectrum is measured for the output powers of 10 mW and 10 W. For the sake of comparison the FFT measurement is done for both the OCC audio amplifier and the UCD amplifier. The reference input voltage is a 1 kHz sine wave with different amplitudes. If there is no distortion the FFT plot should show only the original 1 kHz tone.

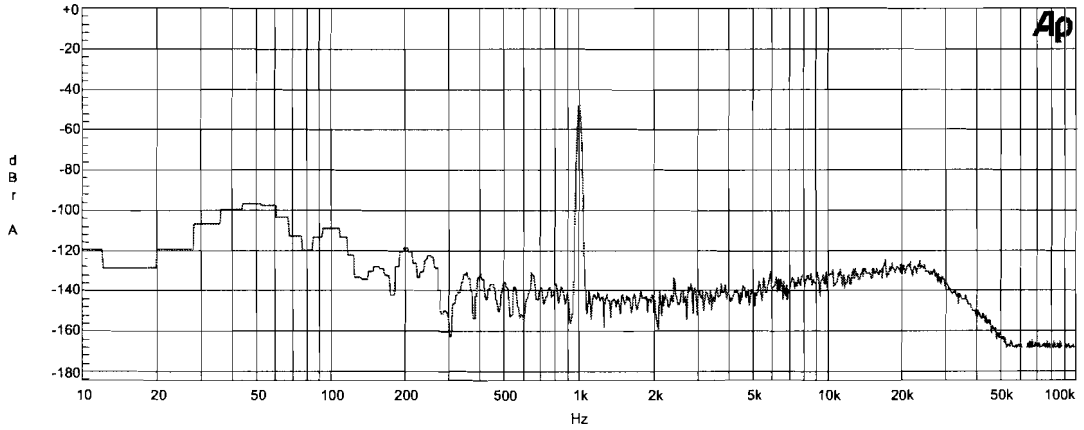


Figure 6.5: FFT of the OCC power amplifier, 10 mW, THD+N = 0.14%

From the FFT measurements in Fig. 6.5 and Fig. 6.6 it can be seen that the the distortion for both power amplifiers is mainly the result of low frequency distortion. This distortion is mainly caused by the noise around the amplifiers, such as the 50Hz power supply hum and other low frequent disturbing signals. There are no higher order harmonics at this power level of 10 mW. Furthermore it is noticeable that at the frequency close to 20kHz the distortion increases slightly for the OCC power amplifier. This could be caused by the low pass filter which is under damped for the OCC power amplifier (Fig. 6.4).

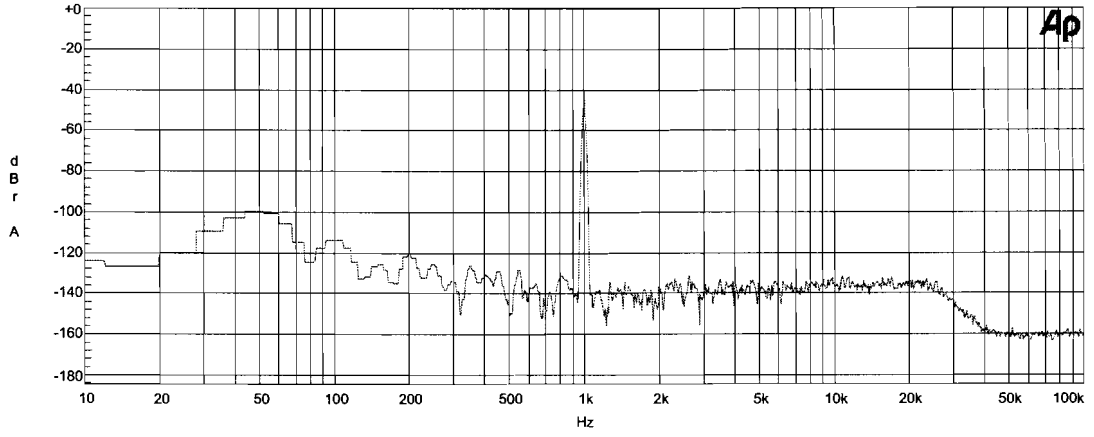


Figure 6.6: FFT of the UCD power amplifier, 10 mW, THD+N = 0.19%

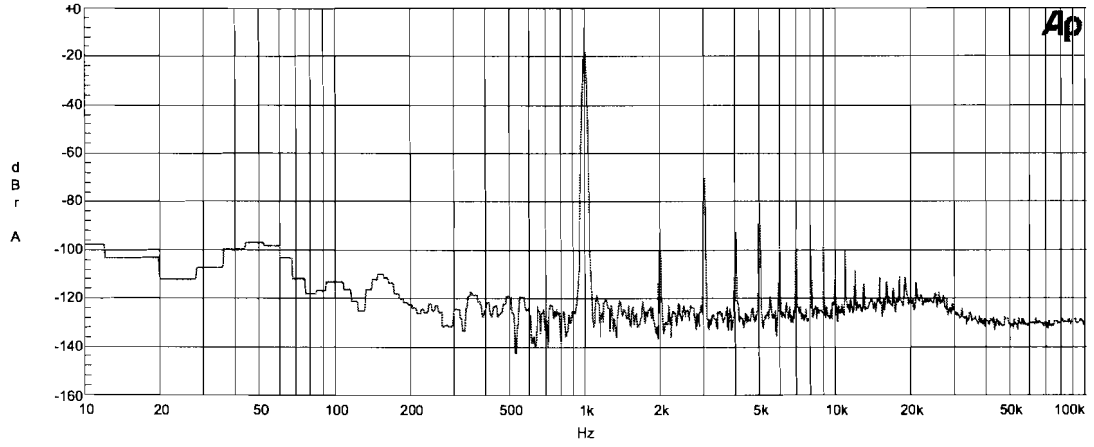


Figure 6.7: FFT of the OCC power amplifier, 10 W, THD+N = 0.14%

Figures 6.7 and 6.8 show the FFT plot for an output power of $10W$. In contrast to the FFT plots measured for an output power of 10 mW, these figures show higher order harmonics as wel. As the power increases these harmonics increase in amplitude as well. These higher order harmonics contribute to the THD+N increase with the increase of power as depicted in the THD+n plots in the previous section.

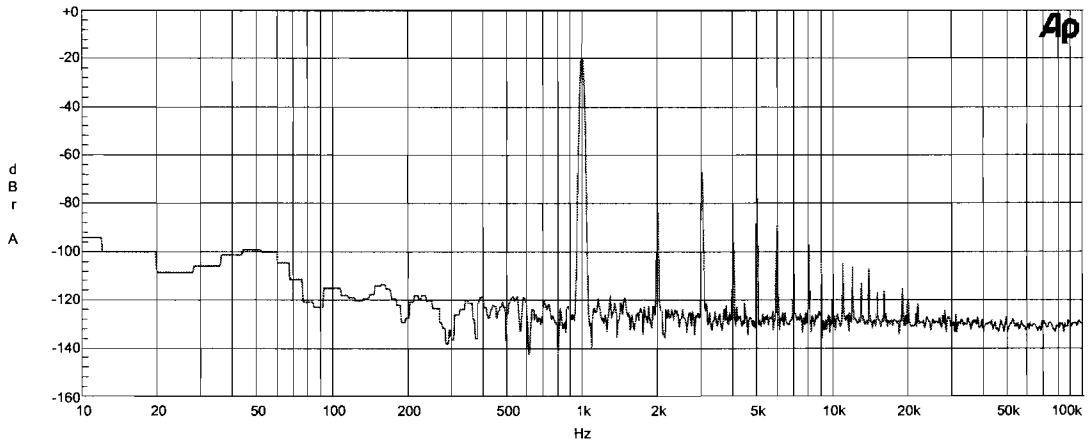


Figure 6.8: FFT of the UCD power amplifier, 10 W, THD+N = 0.21%

6.3 THD+N Icepower

Additionally a THD+N measurement is done for another audio power amplifier with a better performance than the UCD, namely the Icepower amplifier. The OCC is also implemented with the power-stage of this amplifier. The result of this THD+N measurement is depicted in Fig. 6.9. From the figure it can be concluded that the OCC performs again slightly better then the Icepower. The THD+N is also noticeably lower than the OCC with the UCD power stage.

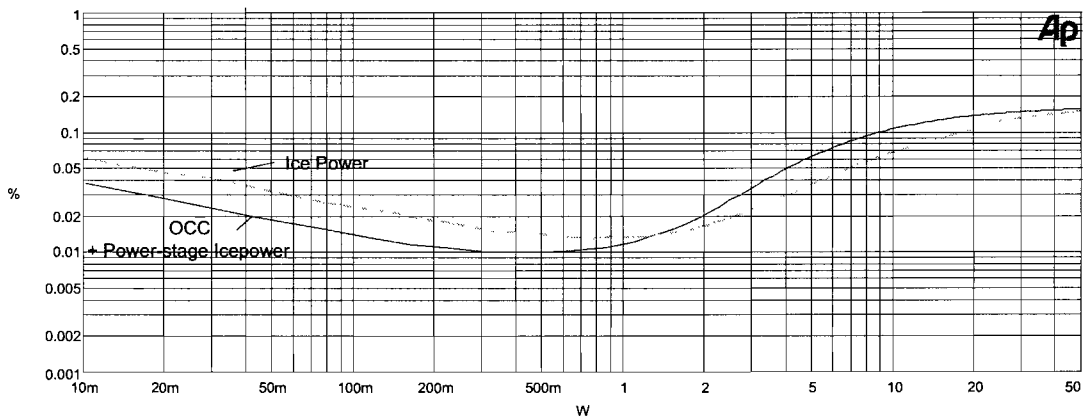


Figure 6.9: THD+N versus power, Icepower, 8 Ohm load

6.4 EMC and ground loops

Ground loops are unwanted signal paths that can occur during measurements of the power amplifier, which can result in a higher THD+N performance of the amplifier. During the PCB design little attention is paid to optimize grounding and signalling pads. Multiple grounding connections in the controller could easily create ground loops. The ground references of the OCC amplifier could have different potential due to random signaling. To prevent dc shifts between the different grounds all ground references must have same potential. In practice this can be done by choosing a star ground connection between power ground and signal ground (DC voltage shifts could otherwise occur through the large currents that flow through the power ground tracks).

Furthermore the distortion can also be reduced by reducing the EMC around the OCC amplifier. Fig. 6.10 shows that the THD+N improves considerably by reducing the EMC by means of good routing of the supply and input cables. The connecting cables are also made smaller. These regulations have resulted in a lower distortion as can be seen in the figure.

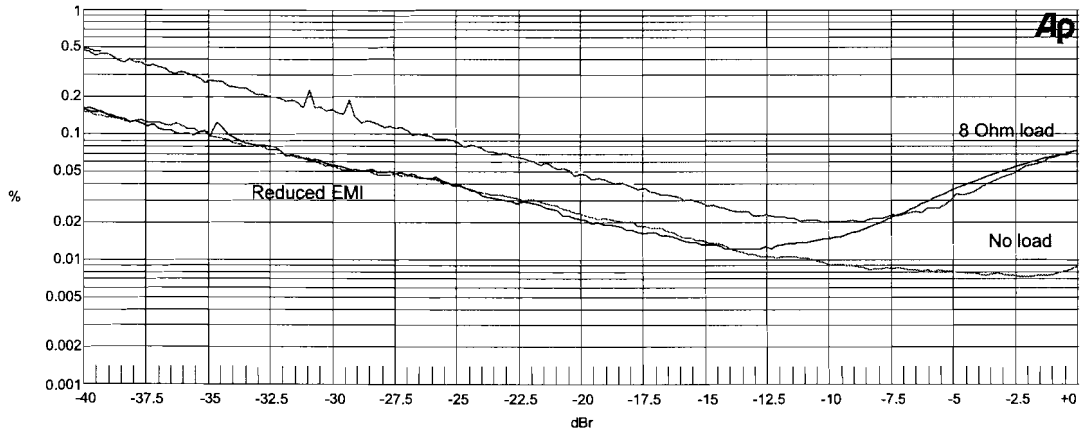


Figure 6.10: THD+N versus amplitude, influence of EMI on THD

The distortion could be decreased even further with a careful and good PCB design. Improvements could be made such as: PCB track as short as possible, strict supply decoupling, prevention of ground loops, current loop areas can be minimized and (parasitic) inductive and capacitive crosstalk between nets prevented.

Chapter 7

Closed loop control

7.1 Output feedback

When there is no feedback from the actual output, the non-ideal behavior of elements in practice and the dynamica of the output low-pass filter will influence the output signal. The output signal cannot follow the command (reference signal) exactly and therefore there is a steady state output voltage error (offset). Furthermore, disturbances in the output load are not rejected when there is no output feedback.

Thus in order to further improve the performance of the amplifier, a feedback loop from the output voltage is included. With the additional feedback loop both the THD of the amplifier and the steady state output voltage error should decrease. Fig. 7.1 shows how the output feedback can be implemented.

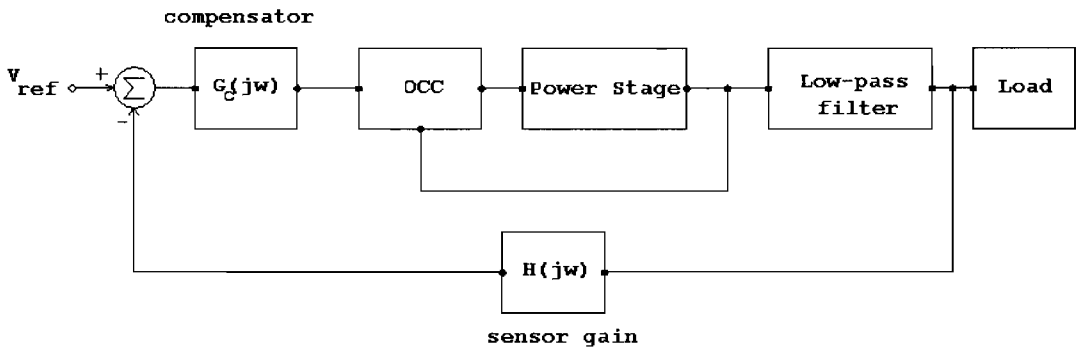


Figure 7.1: Closed-loop OCC amplifier circuit

When the loop is closed, the switching amplifier may become unstable or exhibit an undesirable transient response. The amplifier can be stabilized by the compensator network to increase the phase margin. At the same time, the compensator can

also serve to shape the loop transfer function to achieve a desired transient response. In order to design the compensator the open loop transfer function of the OCC power amplifier is analyzed first.

7.2 Low-pass filter

The open-loop transfer function of the system is mainly determined by the low-pass filter. The filter also plays a large role in maintaining stability. This filter is 2nd order, which means it has two cutoff frequencies. Together these two poles (low-pass cutoffs) add an additional $-90°$ of phase shift to frequencies above each of their cutoffs. If the open-loop gain at these frequencies, approaching $-180°$ phase shift, is not less than 1, or $0dB$, resonance may become a problem. It is further desirebale to leave enough phase margin, usually 40° is reasonable.

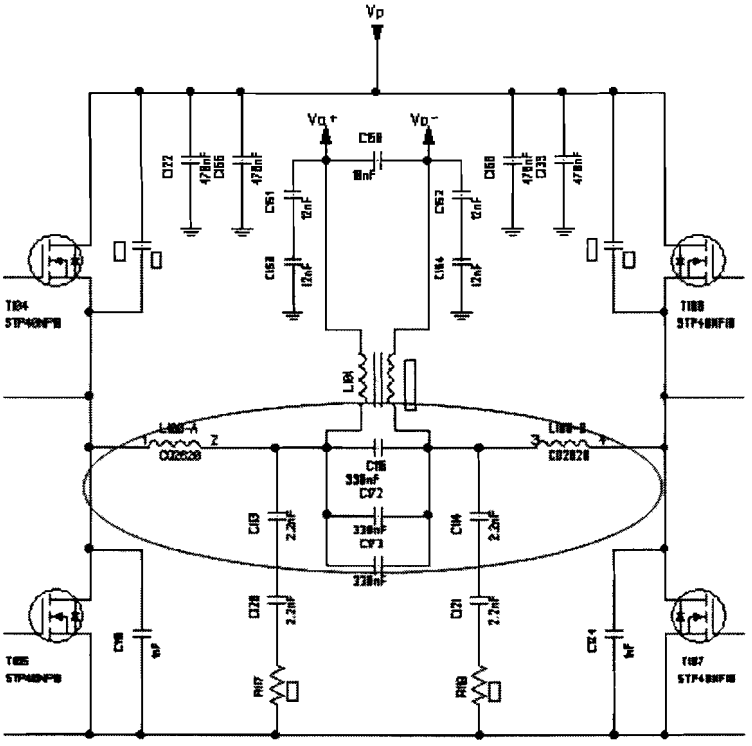


Figure 7.2: Circuit scematic of the UCD power-stage

As mentioned earlier the UCD power-stage is used for the OCC power amplifier. The filter schematic (encircled by the red line) of the UCD amplifier is illustrated in Fig. 7.2. The filter can be simplified according to Fig. 7.3.

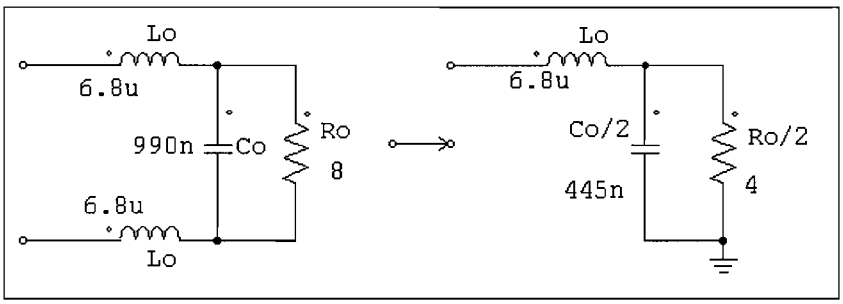


Figure 7.3: Simplified schematic of the low-pass filter

The transfer function of the filter is given by (as for a conventional second order system)

$$H(s)_{LP} = \frac{\frac{1}{LC}}{s^2 + s\frac{1}{RC} + \frac{1}{LC}} \tag{7.1}$$

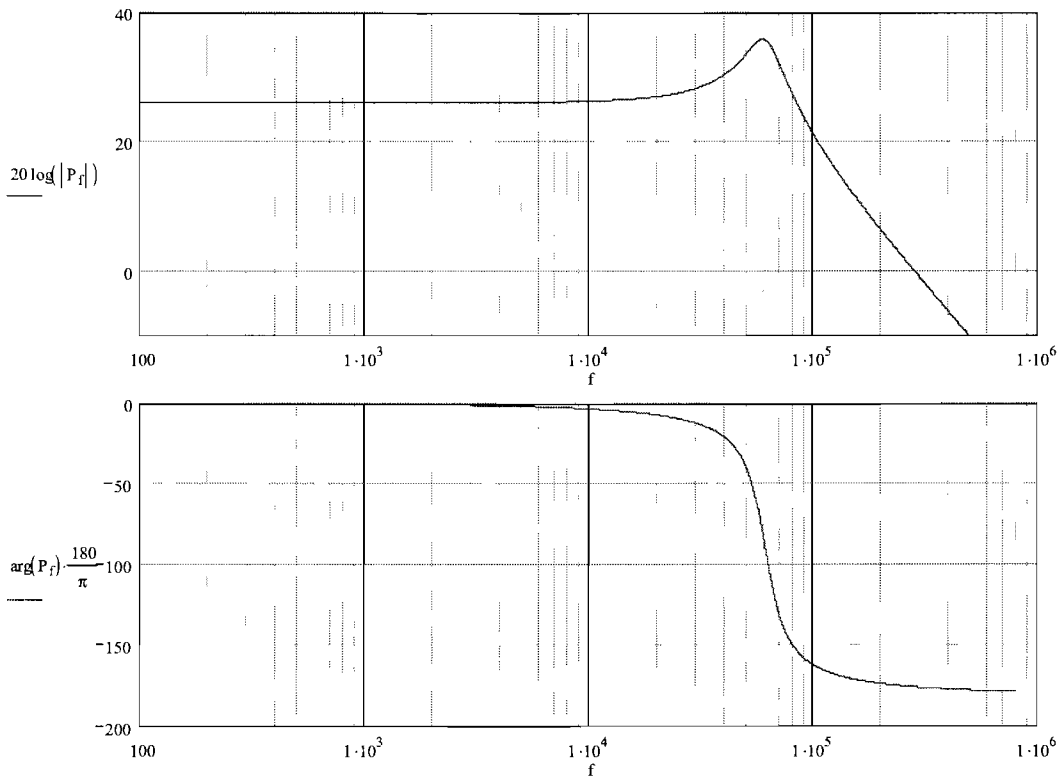


Figure 7.4: Open-loop bode plot for the OCC power amplifier, 8 Ω load

The Open and closed loop system is calculated and analyzed in the programme Mathcad. The resulting bode plot for the open-loop system (OCC + power-stage) is depicted in Fig. 7.4. The output load is an 8 Ω resistor.

The Bode plot for the OCC amplifier is also measured with a spectrum analyzer. And for the sake of comparison also the bode plot for the low-pass filter is measured separately. The bode plots are depicted in Fig. 7.5 respectively Fig. 7.6. The measurements are done for an output load of 8 Ω.

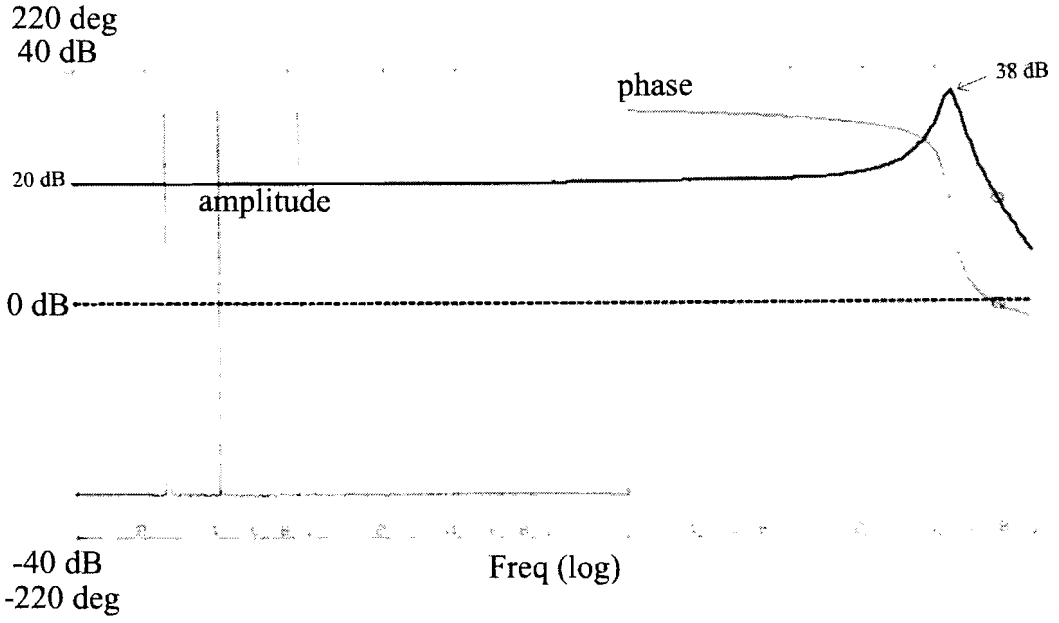


Figure 7.5: Open-loop OCC + power-stage measured with a spectrum analyzer

From the figures it can be concluded that the transfer function is mainly determined by the filter and that the controller together with the power stage only adds an amplification. The cut-off frequencies are calculated to ba at 44 kHz and 51 kHz for an 8 Ω load. The shape of calculated transfer function of the system corresponds with the measured open loop bode plot.

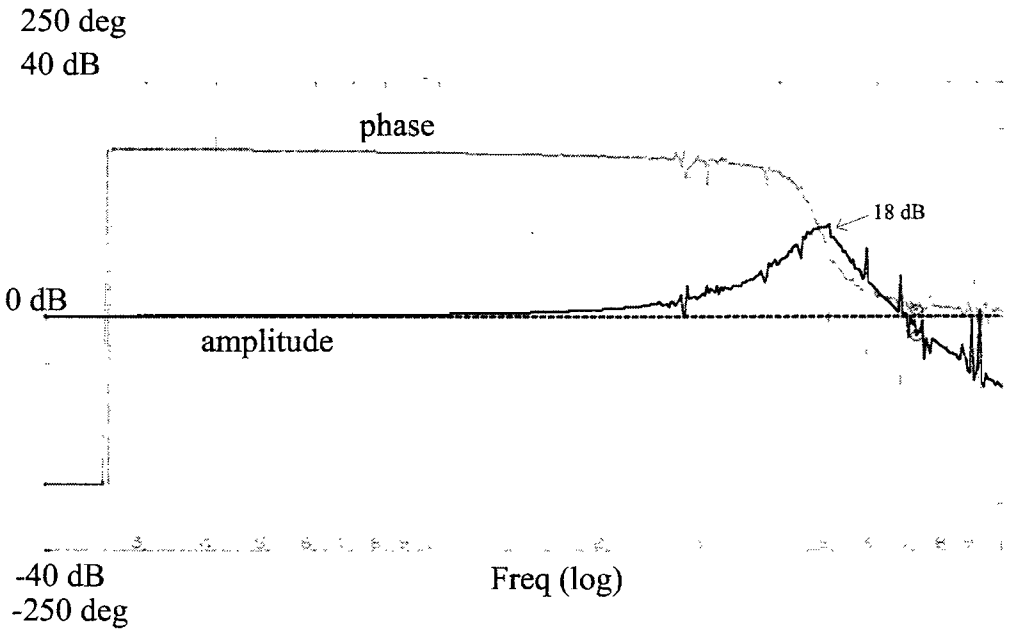
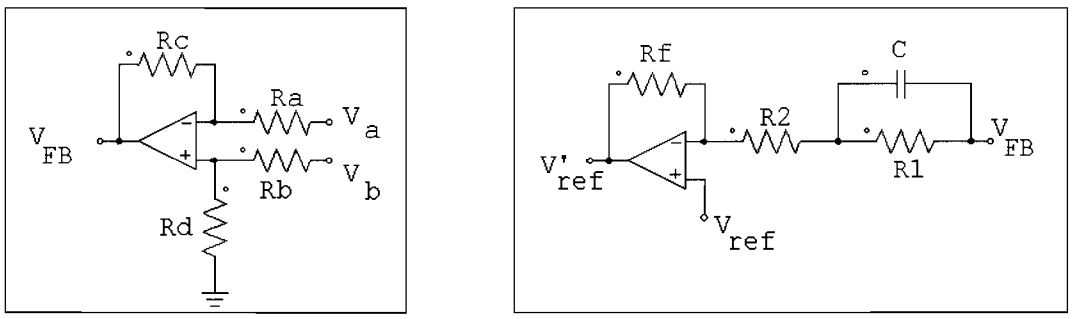


Figure 7.6: Open-loop low-pass filter measured with a spectrum analyzer

7.3 Phase lead compensation

Now that the open-loop system is described the loop can be closed by taking negative feedback from the output. The feedback consist of a sensor circuit and a conventional lead compensation network. The circuits are depicted in Fig. 7.7. The sensor (feedback attenuation) is simply realized by a differential amplifier that has been calibrated to the specific gain of the amplifier. The lead compensation is employed to attain enough phase margin and to alleviate the high frequency amplification. The implemented ciruit and an component list is included in Appendix B.



(a) Feedback sensor

(b) Lead compensation circuit

Figure 7.7: One-cycle control FFT plots.

The transfer function of the phase lead network circuit is given by

$$D(s) = K_{FB}\frac{T_1 s + 1}{\alpha T_1 s + 1} \tag{7.2}$$

where

$$K_{FB} = \frac{Rf}{R1 + R2} \quad , \quad T_1 = R1C \quad and \quad \alpha = \frac{R_2}{R_1 + R2}$$

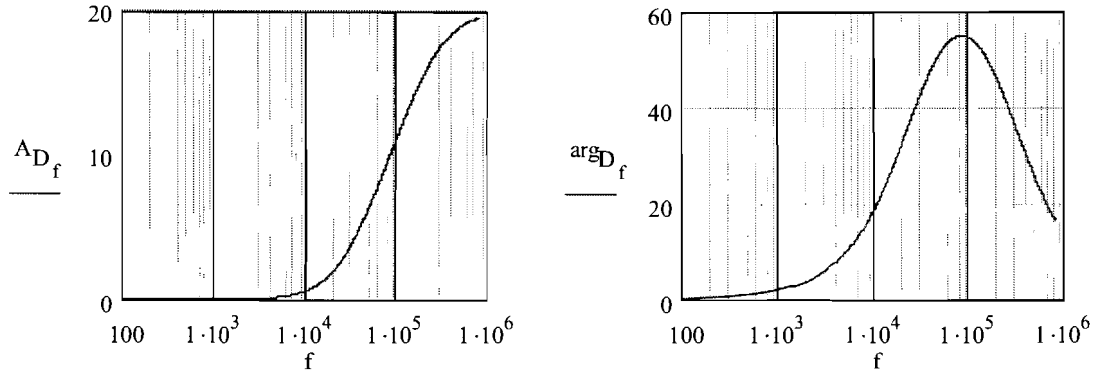


Figure 7.8: ucd THD verus power, 4 Ω load

Figure 7.8 shows the corresponding frequency response of the implemented lead compensator. When α is set to be 0.2 The compensator has one zero and one pole at $f = \frac{1}{2\pi R1C} = 26kHz$ respectively $f = \frac{1}{\alpha 2\pi R1C} = 132kHz$. The resistor values are chosen such that the flat band amplification is unchanged. $R1 = R2 = Rf/2 = 1k\Omega$ and $C = 2nF$

From Fig 7.9 one can see that the system is stable. This is justified by the phase margin of about 30. In this amplifier, the output filter relies on a 8 Ω load for stability. If the gain of the amplifier was increased or load changed to different impedance, the system may become unstable and hence the compensator should be adapted.

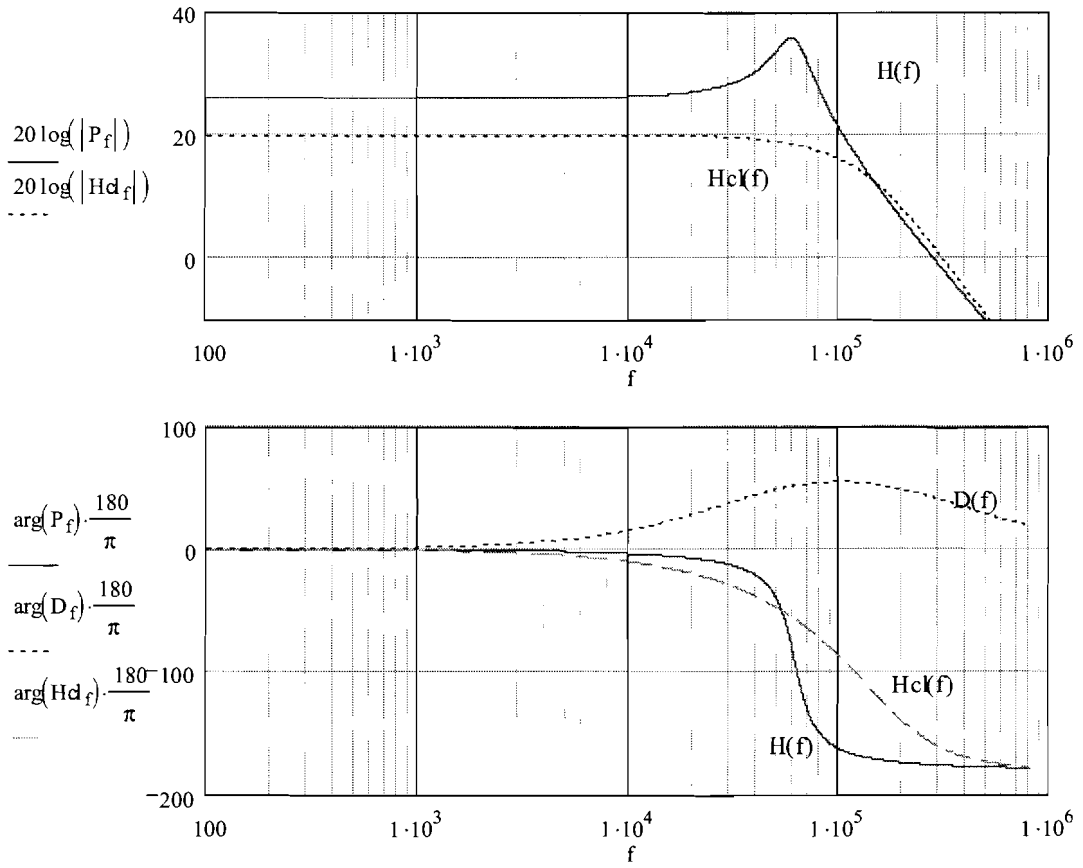


Figure 7.9: Closed-loop OCC + power-stage

After the output feedback loop is implemented in the OCC audio amplifier the THD+N is measured. This is done for different compensator feedback gains K_d. The result is shown in Fig. 7.10. The offset in the output voltage decreases as expected almost linearly with the feedback gain. This is shown in Table 7.1. The THD+N has also decreased compared to the OCC amplifier without the output feedback. However, the amount by which the THD+N decreases is not linearly rated to the feedback gain as expected.

Table 7.1: Offset in output voltage for different feedback gains

K_{FB}	Output offset
1	90 mV
2	49 mV
5	37 mV
10	16 mV

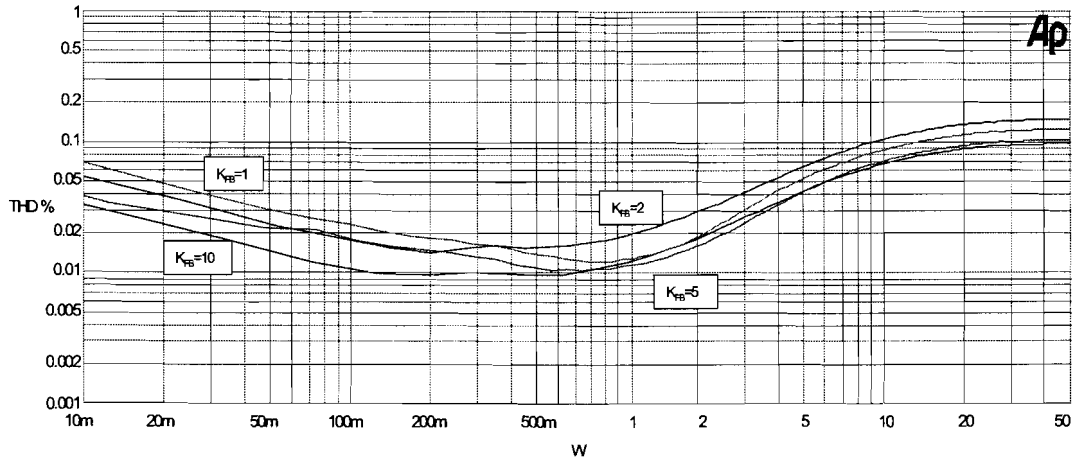


Figure 7.10: THD+N verus power for differnt closed-loop feedback gains, 8 Ω load

Figure. 7.11 shows the improvement of the THD+N when the output feedback is used in comparison with the OCC power amplifier without output feedback and the UCD power amplifier. From the figure it can be seen that especially at lower power(beneath 1 Watt) there is an substantial improvement. The decrease in DC offset and the ability to reject disturbances in the output decreases the signal distortion. Again at higher power (above 1 Watt), the THD+N increases due to the possible causes as discussed in the previous chapter (chapter 6)

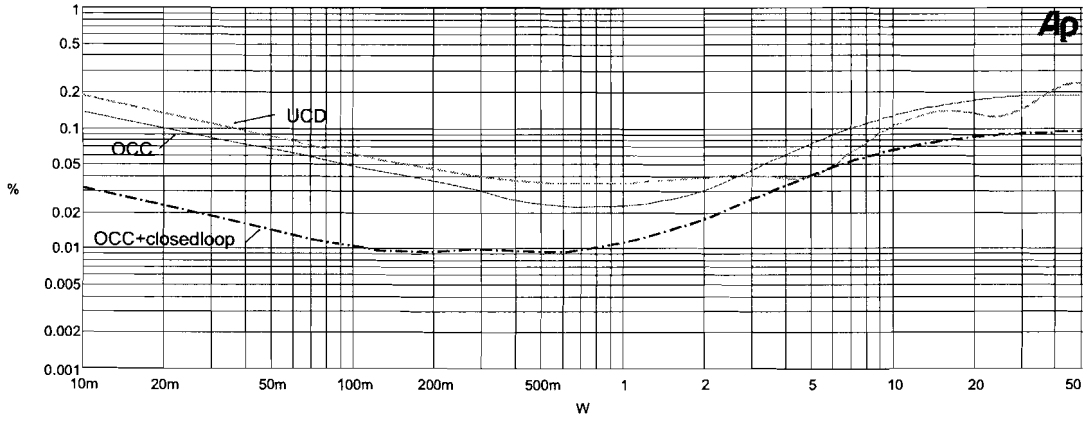


Figure 7.11: THD+N verus power OCC with and without output feedback and UCD, 8Ω load

Chapter 8

Conclusions and recommendations

This report has presented a detailed analyse of the One-cycle control method. Theoretical analysis have shown that the controller is able to control the duty-ratio in real time such that in each switching cycle the average of the chopped waveform at the switch output is exactly equal to the control reference. These analysis include simulations of the OCC used to control a buck converter and a full-bridge amplifier. A detailed analyses for component sensitivity is also presented for the controller. The double-edge modulation principle is also analyzed and implemented in the OCC to alleviate the switching frequency variation even more. Simulations of the OCC method used to control a full-bridge power amplifier (class-D amplifier) have shown good results for power supply ripple rejection. The immediate rejection of the power supply disturbance is the main characteristics of the OCC.

Beside the theoretical analyses, practical measurements are performed to verify the theoretical results. The OCC is designed and implemented on a PCB and used to control a class-D power stage. The performance of the OCC power amplifier is then compared to the UCD power amplifier. As a result the experiments have shown that OCC power amplifier performs slightly better than the UCD amplifier. The OCC power amplifier could perform even beter if the power-stage is designed well. This is verified by the use of the Icepower power-stage.

Finally the OCC power amplifier is extended with the addition of an output feedback. The output feedback is added to compensate for the disturbances in the output load and to reduce the offset in the output voltage. This has resulted in an improved THD+N performance of the OCC power amplifier.

Although the improvement resulted from the addition of the output feedback loop the performance could be improved even further especially for the higher output power. The power stage could be improved by decreasing the non-linearities in the stage. Furthermore, OCC design could be improved also. The PCB design can be improved such that the influence of disturbance is minimized and ground loops avoided.

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Feedforward techniques using voltage integral duty-cycle control (for power convertors)
PESC 92 Record. 23rd Annual IEEE Power Electronics Specialists Conference (Cat. No.92CH3163-3). Toledo, Spain, 29 June-3 July 1992. p. 370-7 vol.1.

[16] [LU-05] Lu, B., Brown, R., Soldano, M. ,
Bridgeless PFC implementation using one cycle control technique
Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC 2, art. no. 1453073, pp. 812-817

Appendix A

Pcad Schematic

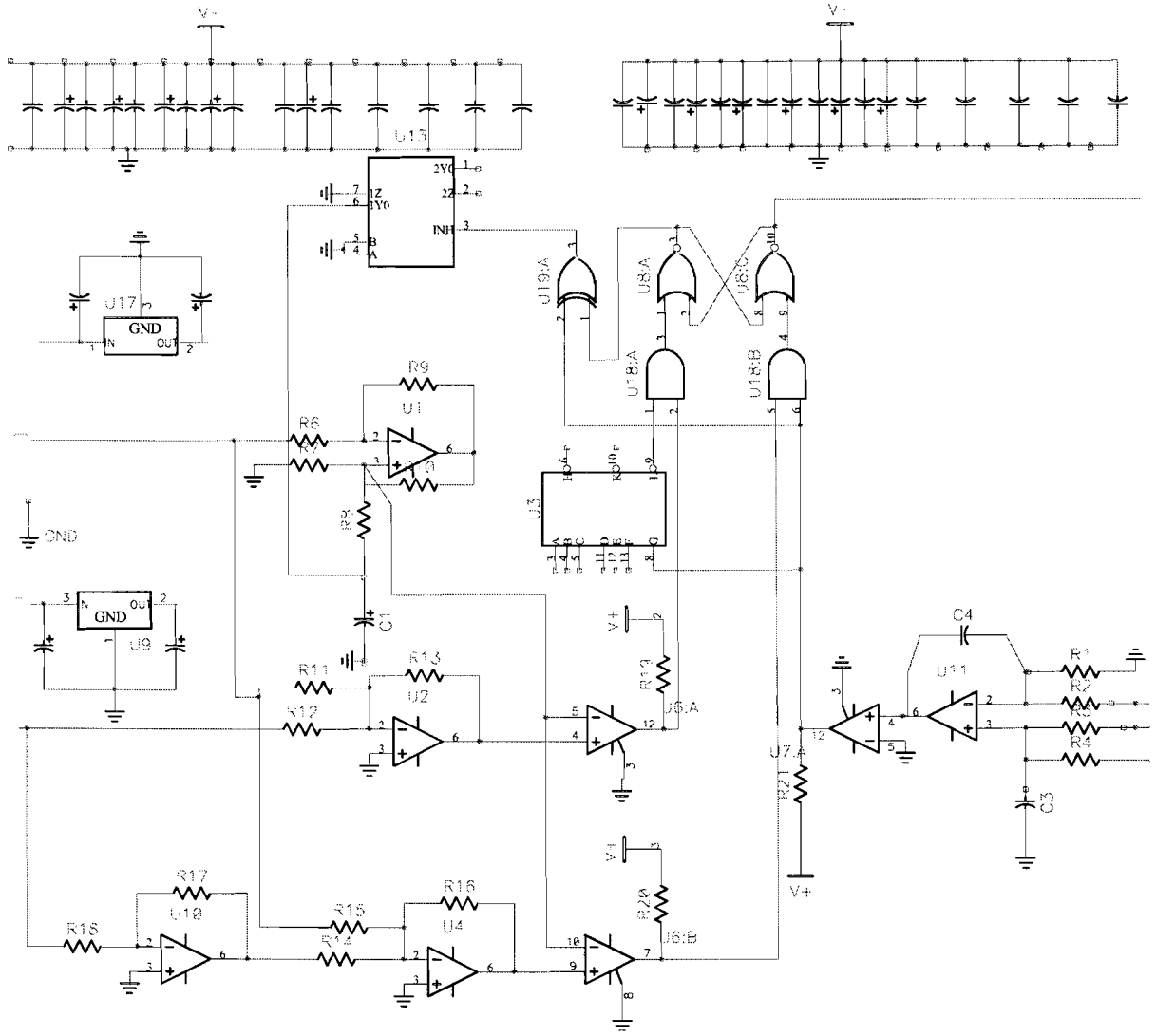

Figure A.1: Pcad schematic of the OCC

Table A.1: List of components in the OCC circuit

Component	name	value
Resistor	$R2$, $R3$	10 $k\Omega$
	$R1$, $R4$	500 Ω
	$R6$, $R7$	4.7 $k\Omega$
	$R8$, $R9$, $R10$	200 Ω
	$R11$, $R12$, $R14$, $R15$	10 $k\Omega$
	$R13$, $R16$	500 Ω
	$R17$, $R18$, $R19$, $R20$	1 $k\Omega$
Capacitor	$C1$	2 nF
	$C3$, $C4$	4 nF
Logic And	$U18A$ $U18B$	HEF4081BF
Logic Inverter	$U3$	HEF4000BF
Logic Nor	$U8A$ $U8C$	HEF4001BF
Logic Xor	$U19A$	HEF4030BEY
Operational Amplifier	$U1$, $U2$, $U4$, $U10$, $U11$	AD8055
Voltage regulator	$U9$	L79M05
	$U17$	L78M05
Comparator	$U6A$ $U6B$, $U7A$	LM319
Analog multiplexer switch	$U13$	74HC4052

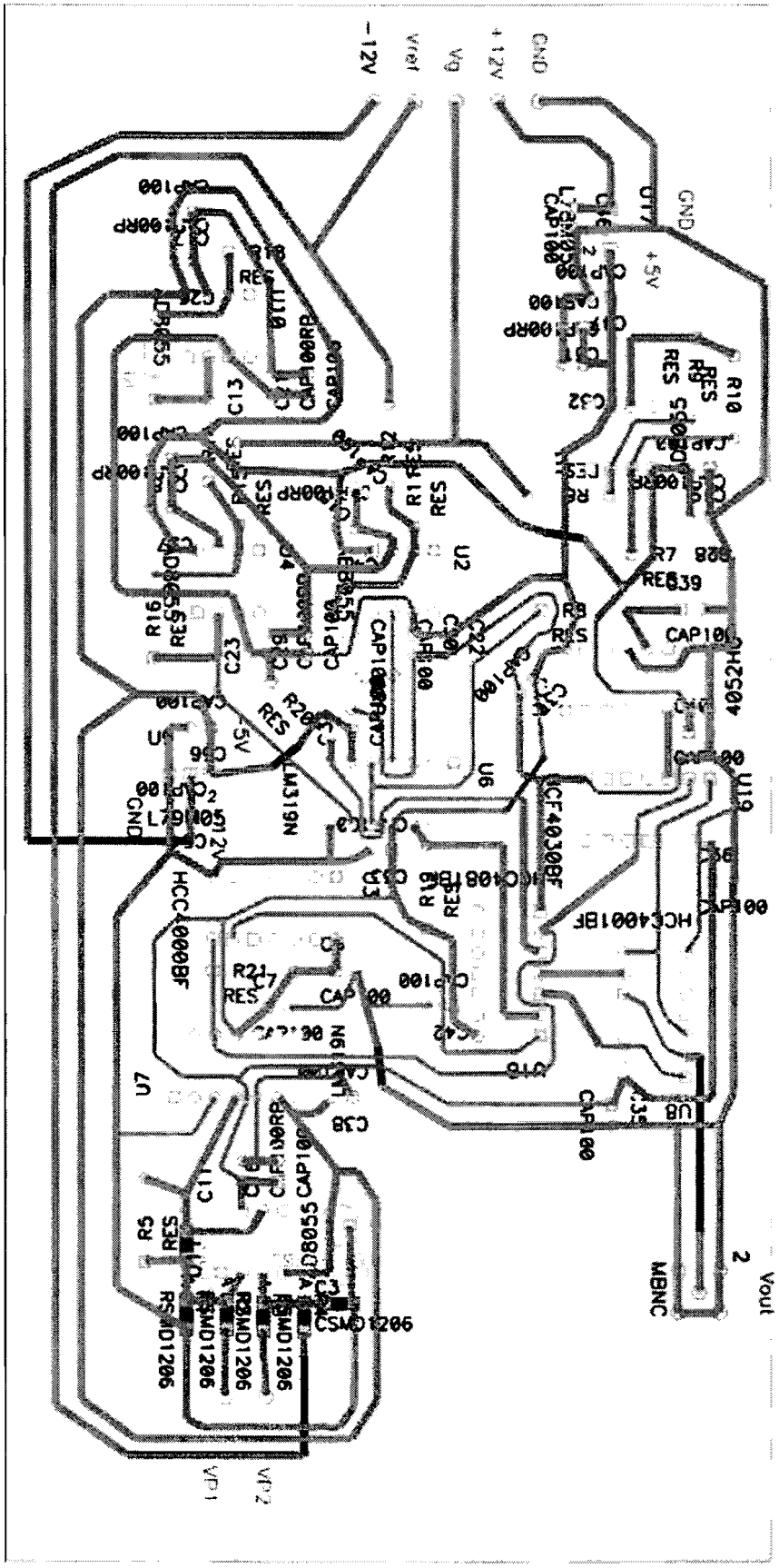

Figure A.2: Pcad PCB layout of the OCC

Appendix B

Closed loop feedback schematic

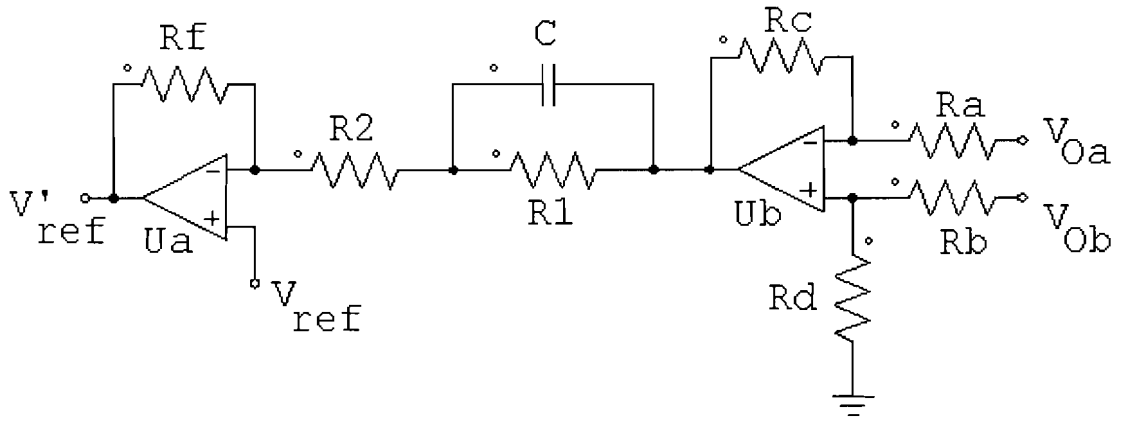

Figure B.1: Feedback schematic

Table B.1: List of components feedback circuit

Component	name	value
Resistor	Ra, Rb	10 $k\Omega$
	Rc, Rd	500 Ω
	$R1$	10 $k\Omega$
	$R2$	2 $k\Omega$
	Rf	1 $k\Omega$
Capacitor	C	2 nF
Operational Amplifier	Ua, Ub	AD8055

Appendix C

Matlab code: calculation of the resetable integrator voltage

```
function Y=Howland(R,R1,R2,R3,C1,T);

%Y=Howland(R,R1,R2,R3,C1,Vin,T)

f=1000;
w=2*pi*f;

% If R = (R1*R3)/R2, than the current into the capacitor depends only on
% the input voltage and R, not on the capacitor voltage.

Vc=0;
ta=0;
tb=0.05e-7;
t=0:0.05e-7:T;
i=2;
while i<length(t)+1
    Y(1)=0;
    Y(i) = 1/(C1)*QUAD(@fun,ta,tb,[],[],R,R1,R2,R3,Vc,w);
    Vc=Vc+Y(i);
    Z(i)=Vc;
    ta=tb;
    tb=tb+0.05e-7;
    i=i+1;

end

tz=0:0.05e-7:6e-7;
plot(tz,-4,'b.');hold
plot(t,Z);
axis([0 0.6e-6 -5 0]) ,grid,
ylabel('Resetable Integrator Voltage');  xlabel('Time');
```

```
%Total current into the capacitor

function Ic=fun(t,R,R1,R2,R3,Vc,w);

Vin=70 + 5*sin(w*t);
Ic =  (-Vin+Vc)/R + R2*Vc/(R1*R3);
```

Appendix D

Matlab code: calculation of f_s variation due to supply ripple

```
%Leading edge function to solve  switching time ta

function ta_L=taLeading(F0,phi,Vref)


for i=1:length(phi)
     ta_L(i)=fzero(@(t) Int_g(t,F0,phi(i),Vref),0);


end

function y=Int_g(ta_L,F0,phi,Vref)

%This is (1/T0)int_0^ta 2g(t)dt
y=quad(@g,0,ta_L,[],[],phi)*F0;
y=-2*y+g(ta_L,phi)-Vref;

function y=g(t,phi)
y=1+0.2*sin(2*pi*250*t+phi);

-------------------------------------------------------------------------

%Leading edge function to solve  switching frequence Fs

function Ts_L=TsLeading(F0,phi,Vref)
ta_L=taLeading(F0,phi,Vref);

for i=1:length(ta_L)
    Ts_L(i)=fzero(@(t) Int_eqn(t,ta_L(i),phi(i),Vref),0);

end
```

```
function y=Int_eqn(Ts_L,ta_L,phi,Vref)

%This is int_0^ta (g(t)-Vref)dt + int_ta^Ts (-g(t)-Vref)dt
y=quad(@X,0,ta_L,[],[],phi,Vref)+ quad(@Z,ta_L,Ts_L,[],[],phi,Vref);


function y=X(t,phi,Vref)
y= -(1+0.2*sin(2*pi*250*t+phi))-Vref;


function y=Z(t,phi,Vref)
y= 1+0.2*sin(2*pi*250*t+phi)-Vref;

-------------------------------------------------------------------------

% double edge modulation , summerizing Ts_T for the trailing edge and Ts_L
% for the leading edge

function Fs_Double_norm = double_edge(F0,phi,Vref)


Ts_T=TsTrailing(F0,phi,Vref);
Ts_L=TsLeading(F0,phi,Vref);


for i=1:length(Ts_T)
Fs_Double(i) = 1/(Ts_T(i)+Ts_L(i));

Fs_Double_norm(i) = Fs_Double(i)/(0.5*F0);
end
```

Appendix E

Matlab code: calculation of the loop / error integrator voltage

```
function [t,Y]=integrator(R1,R2,R3,R4,Vp,Vref,T,D);

w = 2*pi*2e5
C1 = 40e-9; C2 = 40e-9;

Zc2 = 1/wC2
Zc1 = 1/wC1


A1=(Zc2*R4/(Zc2+R4))
A2=(Zc2*R4/(Zc2+R4)+R3)
%Mode 1 Vp1 = 0 Volt en Vp2 = Vg;
A = (Zc2*R4/(Zc2+R4)) / ( (Zc2*R4/(Zc2+R4))+R3)
B = (Zc2*R3/(Zc2+R3)) / ( (Zc2*R3/(Zc2+R3))+R4)
C = (1 + (Zc1/(R1*R2/(R1+R2))))

AC=A*C
BC=B*C
J=-1/(C1*R2)

t=[0 : D*T :T]
%Vy = A*Vg  +  B*Vref;
Y(1) = -2.5;
Y(2) = C*A* D*T*Vp +C*B*D*T*Vref;
Y(3) = Y(2) - (Zc1/R2) * (1-D)*T*Vp +  C*B*(1-D)*T*Vref;
```