

MASTER

Buffer management at ASML manufacturing FASY and test

Pérez Zavala, B.

Award date:
2011

[Link to publication](#)

Disclaimer

This document contains a student thesis (bachelor's or master's), as authored by a student at Eindhoven University of Technology. Student theses are made available in the TU/e repository upon obtaining the required degree. The grade received is not published on the document as presented in the repository. The required complexity or quality of research of student theses may vary by program, and the required minimum study period may vary in duration.

General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain

Eindhoven, July 2011

Buffer Management at ASML Manufacturing: FASY and Test

by
Brenda Pérez Zavala

BSc Industrial and Systems Engineering – ITESM 2008
Student identity number 0729903

In partial fulfillment of the requirements for the degree of

**Master of Science
In Operations Management and Logistics**

Supervisors:

Dr. Ir.H.P.G. van Ooijen, TUE - OPAC

Dr. Ir. Zumbul Atan, TUE - OPAC

Jos op den Kamp, ASML- Production Planning

Peter Lipsch, ASML- Business Engineering

Walter Postma, ASML- Business Engineering

TUE School of Industrial Engineering.
Series Master Theses Operations Management and Logistics.

Keywords: Buffer management, service levels, planned lead times, MRP-based, serial systems, learning effects, capital intensive, and uncertainties control.

I. Abstract

This master thesis describes the challenge of planning manufacturing lead times in unreliable, unbalanced and sequential production systems subject to a target service level. By means of the buffer strategy proposed in this report, time buffers are estimated for attaining a target service level and consequently, enhancing the reliability of internal lead times. This buffer strategy is applied to ASML's manufacturing settings.

II. Executive Summary

This report is the result of a five month Master thesis project at ASML. ASML is the world leader equipment manufacturer in the semiconductor industry. In this regard, for being able to keep its market position, ASML is committed to provide customers with leading edge technology that is production-ready at the earliest possible date. Thus, since reliability in committed due dates to customers is important, enhancing the reliability in external and internal planned lead times becomes crucial. In doing so, the recognition of uncertainties effect on planning is required.

Although uncertainty is present in ASML at all levels, this thesis was concerned on the uncertainties diminishing the production plan's reliability. These uncertainties result from internal and/or external suppliers' lack of responsiveness, operators' failures at execution, lack of workforce capacity, the learning curve effect, customer changes, introduction of new technologies, etc. If any of the latter is not taken into account during planning, the system's performance may extremely deteriorate, and as a consequence, the targeted service level would hardly be met. Therefore, in order to protect the system against these uncertainties and consequently enhance the reliability of production plans, a course of action was needed to mitigate the variability in ASML manufacturing cycle times.

The purpose of this study is defined as follows:

“Design a buffer strategy for the planning of lead times in unreliable, unbalanced and sequential production systems subjected to a target service level and exposed to high capital risk.”

To fulfill the latter, the following questions were investigated:

- Why are buffers needed?
- Where and how to place buffers in the sequence?
- How to design a method for estimating buffers?

The buffer strategy designed in this study was applied to ASML manufacturing settings. Particularly, two manufacturing processes were in scope: FASY and Test. Furthermore, the products under study were the XT8X0H (standard product) and the NXT 1950 (variable product). Subjected to a target service level of 75%, the planning parameters used in ASML manufacturing, as of February 1st, were 36 days for the XT8X0H and 120 days for the NXT 1950 system. In this regard, by using the latter planning parameters, it was observed from last records that the 75% target service level was never achieved.

Results from the application of buffer strategy claim for the planning of longer lead times in order to attain the predefined 75% of service delivery. Particularly, it is advised to increase in 9% on average the time buffer used in the current planning parameters at ASML manufacturing. However, it is also shown that by implementing this buffer strategy not just the targeted service level can be attained, but more than a 50% of cost reduction can be expected for both products in scope.

III. Preface

Being awarded by the Monterrey Institute of Technology and Higher Education (ITESM) with a Bachelor degree in Industrial and Systems Engineering, this thesis represents the culmination of my study in Operations Management and Logistics at the Eindhoven University of Technology.

I believe this is the hardest page to write, I am afraid to forget mentioning an important contributor for the achievement of this personal goal.

First of all, I would like to thank Professor Henry van Ooijen, my primary TU/e supervisor, for how supportive he was throughout the execution of this project. He was always available for meeting, showed a lot of enthusiasm to my assignment and initialized my mindset into thinking “out of the box”. Furthermore, I would like to thank Zumbul Atan, my second TU/e supervisor. She demonstrated her support since the very beginning of this project and remained always available for questions.

I would like to thank Jos op den Kamp and Richard van Boxel for giving me the opportunity to conduct my master thesis project at ASML. Particularly, both supervisors, besides being good leaders, facilitated the execution of my project by providing me with the tools and all information required. Furthermore, I would like to thank Peter Lipsch, who helped me at all phases in this project and in doing so, always triggered challenging questions. Furthermore, I would like to thank Walter Postma and all colleagues of the Production Planning and Business Engineering department at ASML, since without their help I would not have been able to carry out this project in five months.

I would like to thank all my family. At this point I would need at least another 100 pages to give recognition to each special member. All, aunts, cousins, grandmas, sister, parents, uncles, nephews, etc., are, without a doubt, my engine. Particularly, I would like to thank my father, Rubén Pérez Capetillo, for being the best model of perseverance. He has taught me to go and struggle for anything I want. He believes in me and I believe in him. Furthermore, I would like to give special thanks to my mother, Ana Alejandra Zavala Nova, for being the best model of love. Thanks to my mother I know all good sides in life; she makes me dream. It is because of her and my favorite person Ana Nova Sandoval, my grandma, that I always try to be a better person in all fields.

I would also like to thank Sergio Padilla and all my friends in long and short distance that have provided me with a lot of support and joy throughout the last two years.

Last but certainly not least, I would like to thank my best friend, Mauricio Teillery Tello[†], for being the last inspiration in the culmination of my studies. This master thesis is dedicated to his memory, this was our goal and I would like him to know I kept that promise, our promise.

Brenda Pérez Zavala
Eindhoven, The Netherlands
July 2011

Contents

I. Abstract.....	iii
II. Executive Summary.....	iv
III. Preface.....	v
INTRODUCTION	ix
Choice of research context and case study	ix
Organization of the Master Thesis.....	ix
CHAPTER 1: Introduction to ASML.....	1
1.1 ASML description	1
1.2 The organization’s structure and responsibilities.....	3
Manufacturing & Logistics (ML).....	3
1.3 ASML manufacturing: FASY and Test.	4
FASY.....	4
Test.....	5
1.4 The challenge of planning FASY and Test lead times in ASML.....	6
CHAPTER 2: Research Design.....	7
2.1 Problem description.....	7
2.2 Research assignment	8
2.3 Research Questions	8
2.4 Research methodology	9
2.5 Research scope and deliverables	9
2.6 Solution Approach.....	10
CHAPTER 3: ASML manufacturing lead times planning	12
3.1 Cycle times, lead times and time schemes definitions in ASML.	12
3.2 Departments’ involvement in ASML manufacturing lead times planning.....	14
3.3 FASY and Test way of working and time schemes description.....	15
3.4 Environmental and system’s uncertainties present in the lead times planning at FASY and Test... 17	
3.5 Buffers as defined in ASML manufacturing	20
3.6 Current way of estimating buffer time in FASY and Test.....	21
3.7 Current planning parameters and delivery performance records from the last systems.	22
CHAPTER 4: Buffer strategy for the planning of reliable lead times in serial production systems subject to a targeted service level.	24

4.1 General Assumptions.....	25
4.2 The need to buffer.....	26
4.3 Alternatives for enhancing lead times reliability.....	27
4.4 Buffer Strategy.....	29
4.4.1 Determination of a cost efficient target service level.....	31
4.4.2 Placement of time buffers in sequence.....	32
4.4.3 Estimation of time buffer sizes under a minimal quotation approach.....	33
Computation of costs.....	39
Preferred method.....	40
CHAPTER 5: Case study. ASML Manufacturing FASY & Test.....	41
5.1. Recalling ASML characteristics.....	41
5.1.1. ASML manufacturing settings.....	41
5.1.2. Current parameters and performance in ASML planning.....	41
5.2. The buffer strategy in ASML FASY and Test.....	42
5.3. Performance analysis.....	43
Cost analysis.....	46
5.4. Scenario analysis.....	50
CHAPTER 6: Implementation concerns.....	51
6.1. Data collection and analysis.....	51
6.1.1. The data sources.....	51
6.1.2. Identification of outliers.....	51
6.1.3. Distribution Fitting.....	52
6.2. The periodicity for reviewing planning parameters and sample size N.....	53
6.3. Determination of input parameters.....	54
6.3.1. How to determine the learning percentage (k)?.....	54
6.3.2. How to determine the number of orders to predict (u)?.....	55
6.4. Organizational constraints.....	55
CONCLUSIONS AND FURTHER RECOMMENDATIONS.....	57
REFERENCES.....	59
APPENDIX A: ASML Industry framework.....	60
APPENDIX B: Manufacturing & Logistics.....	61
APPENDIX C: Time categories.....	63

APPENDIX D: Integral Manufacturing flow	64
APPENDIX E: Company's characteristics	66
APPENDIX F: Related works for the setting of lead times in serial production systems.	68
APPENDIX G: Buffer strategy application in ASML Manufacturing FASY and Test.	70
APPENDIX H: Scenario analysis	77
APPENDIX I: Data sources and reliability assessment.	84
APPENDIX J: ASML recommended data source	86
APPENDIX K: Periodicity example and application.	87
APPENDIX L: Example of outlier's detection	88
APPENDIX M: Example for determining the learning percentage	89
APPENDIX N: Buffer Strategy Implementation- Process flow.....	91

INTRODUCTION

The dynamism characterizing nowadays economy claim planners in manufacturing systems to consider uncertainty in the setting of their production plans. In this regard, and particularly in the case of semiconductor equipment manufacturers, demand and lead time fluctuations stand at the heart of the planning of these complex systems, which, associated to their capital intensive nature, makes the use of time buffers along the production line, crucial to achieve a target service level. In this regard, time buffers should be regarded as the average disturbance time included in the lead time planning of production lines.

Choice of research context and case study

The literature study conducted for the buffer management in manufacturing firms (Pérez, 2011) revealed that in planning, several factors besides demand and lead times uncertainty are in place. Thus, the particularities of each manufacturing setting undermine all efforts from researchers in operations and inventory management to come up with a robust mathematical model to represent real time problems in unbalanced and unreliable production lines characterized by stochastic demand and processing time. Particularly, there is a lack of research run in the semiconductor industry and if found, studies are aimed to serve mostly semiconductor manufacturers interests, letting aside its supply chain partners which, if located at the upstream stages, exposure to uncertainty is enlarged and worsened by the capital intensive nature of its products and the high level of responsiveness expected from semiconductor manufacturers. In this regard, planners in equipment manufacturers need to come up with reliable production plans capable to mitigate system uncertainties. In doing so, the placement of buffers in the production line stand as crucial and necessary for enhancing each order delivery performance within internal and to external customers. However, the obsolescence risk and capital nature of these products claim the usage of time rather than stock as the buffer principle to be used. In this regard, the special case of capital intensive, high-risk low-volume products with short life cycles and with organizational specificities underlying the performance of an unbalanced production line were not found to be jointly discussed in the literature study conducted, neither for semiconductor industries, nor for the capital goods planning. Therefore, since previous studies in the field lack a strategy to estimate time buffers under these particular settings, the motivation of this practical study is to extend previous studies and narrow this gap in literature.

Organization of the Master Thesis

The remainder of this Master Thesis is as follows. Chapter 1 is aimed to provide the background information related to the company under study. Therein, the organizations' industry, functionalities and overall planning challenges are presented. Chapter 2 defines the problem, the research approach to undertake in this study so as the research questions to work with and solution approach to follow up. Chapter 3 is aimed to provide a more detailed explanation of the terminology and current way of planning ASML's manufacturing lead times. Thereafter, Chapter 4 presents the buffer strategy suggested

for the planning of time buffers in production lines subject to high variability and a targeted service level. Thereon, Chapter 5 brings this time buffer strategy into the planning of time buffers in ASML manufacturing: FASY and Test. Chapter 5 gives evidence of the better off resulting from the application of this strategy in comparison to the current planning parameters in ASML. Thereafter, Chapter 6 is aimed to provide advises for the further implementation of this strategy. This master thesis report finalizes providing conclusions and further recommendations to both, ASML and the academy.

CHAPTER 1: Introduction to ASML

This chapter is aimed to provide an overview of the company partner of this master thesis: ASML. In doing so, Section 1.1 will be devoted to describe the role ASML plays in the semiconductor industry so as its current market position, products and future challenges in committing to customers expectancies. Then, Section 1.2 presents the current ASML organizational structure along with the departments directly involved in this research. Thereafter, being FASY and Test the two production units under study; Section 1.3 provides a deep explanation about them. Finally, Section 1.4 describes the challenges planners face in the setting of lead times in ASML manufacturing.

1.1 ASML description

ASML is the world leader manufacturer of advanced technology systems for the semiconductor industry¹. ASML major competences are the design, development, integration, marketing and service to customers' advanced systems meant to create chips that power a broad array of electronic, communications and information technology products. Founded in 1984 and headquartered in Veldhoven, the Netherlands, the company is publicly traded under the symbol ASML on Euronext Amsterdam and NASDAQ. Since its foundation, ASML has steadily increased its market share, going up to 67% as of 2009 market records, see Figure 1.1 below.

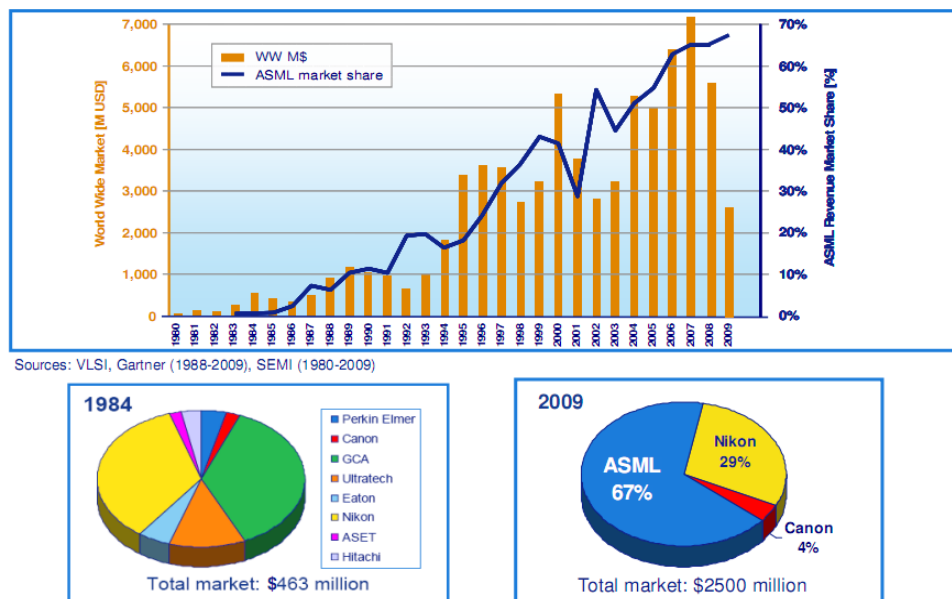


Figure 1.1 ASML's market share as of 2009

¹ Refer to Appendix A for a description of ASML's Industry framework.

As a rebound from 2009 economic downturn, 2010 ASML books record sales of 4.5 billion Euros thanks to electronic gadget innovations (such as smartphones) which enhanced chip manufacturers' need of capacity, and eventually boosted ASML moves to cope with the resultant demand. Figure 1.2 depicts ASML's product roadmap as of September 2010. For this project main interest, solely the NXT 1050i and XT 8X0H systems will be under analysis. The latter is due to the possibility of further generalization into other ASML products, where the NXT stands as a sample for a variable system and the XT8x0 as a sample for the most stable product. The XT 860 system started to be produced since September 2010 as a standardized configuration, in which no customization is carried out in ASML facilities but at customers. Regarding ASML main clients, TSMC and Samsung stand as the drivers for the XT8x0 and INTEL as the driver for the NXT1950 system production.

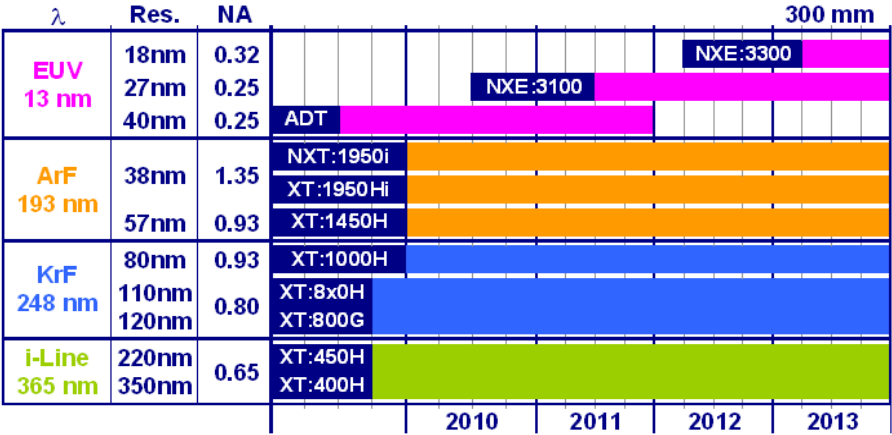


Figure1.2 ASML's product roadmap, September 2010

As time passes by, the complexity of production integrated circuits with more functionality increases, so as the level of responsiveness claimed by customers does. In this regard and despite ASML is at the head from competitors, the company is committed to provide customers with leading edge technology that is production-ready at the earliest possible date. Due to the latter, the accuracy in strategic, capacity and execution planning becomes crucial for attaining customers' requirements in time where despite the different levels of aggregate planning, communication between and within departments at all levels is essential in pursuing a high service level to customers.

1.2 The organization's structure and responsibilities

As of February 1st, 2011, the Organizational structure in ASML is as follows. Four main divisions stand at the highest level of the organization, namely, "Support", "Product", "Operations", and "Market", all from which for this project purpose the "Operations" division will be solely addressed.

"Operations" is responsible for the actual manufacturing of machines. Figure 1.3 depicts ASML manufacturing, therein is shown that the external and internal provision of supplies are necessary for getting the final assembly of a machine started. Whereas the external suppliers provide the "buy parts", the internal suppliers, namely "ASSY", are in charge of producing those parts regarded as core components in ASML complex systems, namely "modules"². Furthermore, while ASSY takes place in several work centers working in parallel (Electrical, Illumination, Wafer Stage, etc.), FASY, Test and Packing are executed sequentially in the same facility, namely "cabin". Thus, once a machine order is released, a cabin is assigned to this order wherein FASY, Test and Packing take place. From the latter, FASY and Test are in this project scope and thus, are the main focus in this master thesis report.

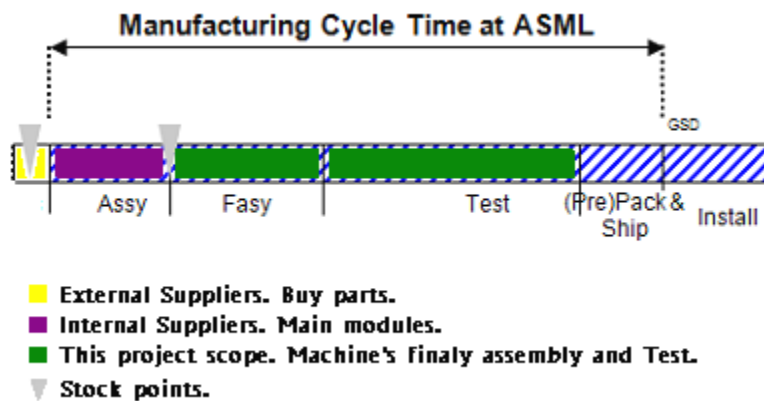


Figure 1.3 ASML Manufacturing

"Operations" is supported by the Industrial Engineering, Manufacturing & Logistics, Quality & Process Improvement, and Sourcing subdivisions, this project having its main impact on the Manufacturing & Logistics subdivision.

Manufacturing & Logistics (ML)

The Manufacturing & Logistics (ML) subdivision manages the internal production processes in ASML and is supported by several departments of different nature such as Facility Mgt, Real Estate, Global Logistics, etc. (See Figure 1.4). Particularly, the outcomes of this assignment affect directly the Building

² The terms "modules", "components" and "assemblies" will be interchangeably used in the reminder of this Master Thesis report.

Operations, Delivery Operations, Manufacturing Engineering and Business Services units which functionalities are briefly described in Appendix B.

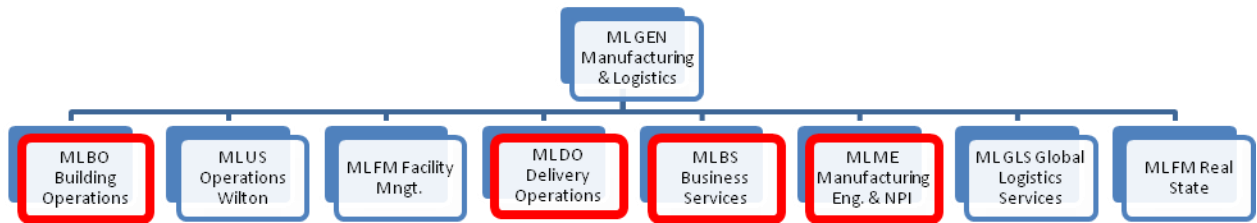


Figure 1.4. ASML's Manufacturing & Logistics structure.

1.3 ASML manufacturing: FASY and Test.

In a broad sense, a machine production order relies on the execution of two stages: FASY and Test. At this point it should be remarked that contrary to ASML assemblies' manufacturing (ASSY), in which components move within work centers until the assembly is ready to be transferred to FASY; a system is produced in the same facility (namely cabin) and teams with different competences come sequentially to carry out their respective job from the sequence defined by Mechanical Engineering. Thus, although FASY and Test share some resources (facility resources), they should be regarded as two different production units managed by two different organizational divisions. Particularly, while FASY is under the Building Operations manager jurisdiction, Test is managed by Delivery Operations authorities, giving the sense of an internal, but formalized, supplier-customer relationship.

FASY

Once a machine production order is ready to start in a cabin, the *Prepare* process takes place. Therein, all cleaning, tooling allocation, and overall system's specific arrangements are carried out for FASY Start ends. Besides preparation, the FASY production unit is comprised by three main operations: *Build*, *System*, and *Init/Elmic*. These operations differ in functionalities, timing, and overall, in team competences. Figure 1.5 depicts FASY sequential actions which each completion has been recently labeled as 'milestone'. Therefore, finishing Prepare, Build, System or Elmic means a milestone has been achieved.

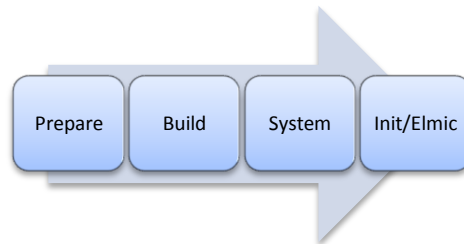


Figure1.5 Sequence in FASY

In *Build* all ASSY modules are built in the machine. The arrival time of the modules into the cabin differs and is thought as to bring the most expensive ones to the latest possible moment to be built in the machine. The building operation starts with the main frame and ends up with the wafer stage. During building all ASSY orders are merged into one order, the machine order.

In *System* the switch is “turned on”. Therein all water and air flows are checked in the circuits running through the bottom and upper part of the machine. During this operation all flows are arranged so as to make sure the machine works on temperature.

Finally, during *Init/Elmic* all bundles are verified to be connected correctly in such a way that none miscommunication between modules exists. The proper definition of this operation is to *initialize* the modules.

The complexity and deviations immersed during the execution of these operations differ and can be considered independent from each other. Thus, the cycle time (CT) in System does not depend on the CT in Building, and so on. Although diverse definitions stand for CT between and even within ASML departments, the FASY CT is the time comprised from FASY Prepare Start until the Test Start date.

Test

Test operations are split into milestones. A milestone is related to a defined part of the sequence and currently is based on competences; for instance, one milestone addresses all work referred to the reticle stage (RS), next milestone all referred to the Wafer Stage (WS), and so forth. For all systems, except XT 8x0H, customization is carried out in Test, in CODP and MS12. Figure 1.6 and 1.7 depict XT8x0H and NXT 1950 milestones in Test, respectively.



Figure 1.6 XT 8X0 sequence in Test.

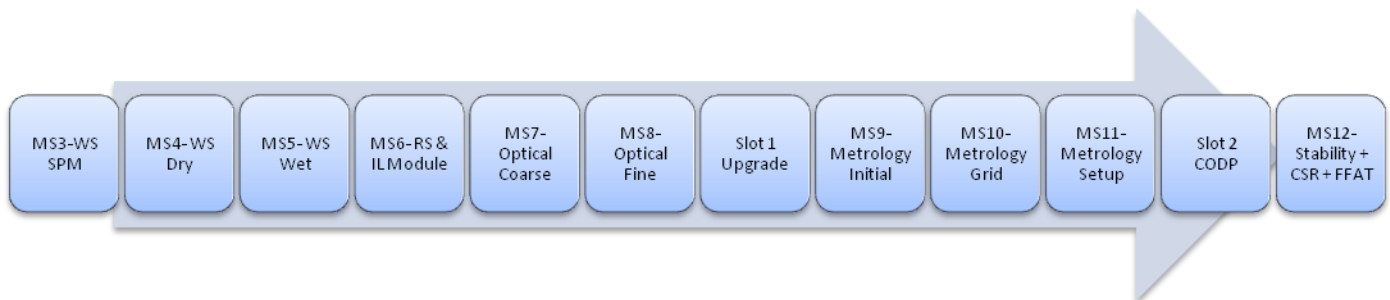


Figure 1.7 NXT 1950 sequence in Test.

1.4 The challenge of planning FASY and Test lead times in ASML

ASML works within an MRP framework and as remarked in Buzacott (1994), lead time and safety stock/time stand as the two management parameters that can be set to determine the system's performance. However, Buzacott (1994) also states that the appropriate values of these parameters are influenced by the forecasts nervousness, the variability of the processing times, and the cost of inventory and shortages; all of which are core features in ASML settings. Thus, the system's and environmental uncertainties lived in ASML make the planning of manufacturing lead times be a huge challenge for planners. Furthermore, being several departments dependent on the production plan as an input, the reliability of the latter can be regarded as crucial factor for the overall organizational performance. Moreover, the capital intensive nature of ASML products together with cabin space restrictions at the shop floor, make safety lead time preferable to safety stock as the buffering technique used to absorb variations in production.

Although uncertainty is present in ASML at all levels, this thesis will be concerned on the uncertainties diminishing the production plan's reliability. These uncertainties result from internal and/or external suppliers' lack of responsiveness, operators' failures at execution, poor definition of procedures in sequence, lack of workforce capacity, unexpected quality issues, the learning curve effect, customer changes, introduction of new technologies, etc. If any of the latter is not taken into account during planning, the system's performance may extremely deteriorate, and as a consequence, the targeted service level would hardly be met. Therefore, in order to protect the system against these uncertainties, a course of action is needed to mitigate the variability in ASML manufacturing cycle times. In doing so, reliable lead times would support production plans stability and consequently, the targeted service level would be attained.

A production plan is stable if the planned start/due dates are aligned to execution; thus, no need for planners to reallocate/reschedule capacities/orders. A remark is needed at this point, where despite the fact this project scope comprises ASML FASY and Test solely, the instability lived in these units' plans is spread all over the planning of ASML manufacturing; including ASSY. For instance, being components in FASY not assembled at once, whenever a delay is observed at an early step in final assembly, subsequent components are needed later; and consequently, ASSY planners either have to reassign these components to another order, or have to keep them on the factory halls due to space constraints in the work center. In line with the latter, an instable plan in Test (thus, being early or tardy from the original plan) also affects FASY and ASSY instability. In this regard, finishing early or later directly affect the rescheduled of subsequent orders in FASY (hence, ASSY). Finally, despite most of the times customers are eager to receive their order earlier, the reader should be aware that some exceptions occur and worsen off the instability of production plans. The latter is due to the fact that if a customer is not ready to receive its order, in trying to avoid keeping systems as stock, planners have to reassign this order to another customer. Therefore, planning ASML's manufacturing lead times requires the awareness of all cost tradeoffs resulting from production plans' stability (hence, avoiding reschedules/reallocations) and the service delivery performance.

CHAPTER 2: Research Design

This chapter is aimed to present a brief description of the design and objectives of this research project. In doing so, Section 2.1 defines the problem under investigation jointly with the objective of this research. In Section 2.2 the research assignment is stated and followed by the research questions in Section 2.3. Thereafter, Section 2.4 describes the research methodology to follow up. Section 2.5 states this master thesis scope and enlists its deliverables, and finally Section 2.6 presents the solution approach to carry on for the completion of this research project.

2.1 Problem description

Currently, the main planning tool employed by production planners in ASML is based on the system CT and buffer time definition provided by mechanical and business engineers, respectively. Regardless of the type of system being planned (either standard or not), the estimation of time buffer for each system is carried out without addressing the impact of system's uncertainties, known as "disturbance" in ASML. In fact, the computation of safety time in ASML manufacturing (FASY and Test) relies at the most on the median gotten from the last systems' records. Thus, this buffer time estimation lacks the recognition of learning curves and the costs immersed in rescheduling these expensive systems. Furthermore, many of the promised dates for delivery are hardly met, and as a consequence, the reliability on planning parameters is low, claiming for a course of action to mitigate the effect of uncertainty in ASML manufacturing lead times.

In the introduction a number of gaps found in literature for the buffer management problem in manufacturing firms have been stated. Particularly, in the literature study conducted by Pérez. B (2011) it was stated that there is a lack of studies addressing the estimation of safety lead time in manufacturing firms characterized by capital intensive, high-risk low-volume products with short life cycles and with organizational specificities underlying the system performance targets. In this regard, a modest amount of studies were found for the estimation of time buffers in multi-stage systems with stochastic lead times. However, all solution approaches in those few were aimed to minimize the total costs coming from earliness and tardiness, and assumptions failed to deal with many of the uncertainties stated in Section 1.5. In addition, it was not found in literature a single research run in a company exposed to the variability lived in a semiconductor equipment manufacturer, such as ASML, in which competence groups are moving and assigned to a specific production order. Particularly, this latter makes the estimation of accurate MRP parameters become crucial for: 1) the stability of production plans, 2) the lowering of operators' and systems' start reschedules 3) the reduction of the amount of capital put on hold when capacity shortages occur. In this regard, previous studies ignore all latter discussed, and instead, they mostly assume highly predictable processes along with a predefined service level in which the capital exposed in avoiding tardiness is relatively low compared to opportunity costs involved in the settings of this research project.

Thus, the buffer time management problem at ASML together with the lack of a robust model in the literature for addressing the uncertainties on the planning of high-risk low-volume products, gave rise to the definition of this research assignment.

2.2 Research assignment

Design a buffer strategy for the planning of lead times in unreliable, unbalanced and sequential production systems subjected to a target service level and exposed to high capital risk.

2.3 Research Questions

1. Why are buffers needed?
2. Which are the main factors affecting the buffer time definition in sequential production units?
 - a. What is the definition of CT and buffers in each production process and operation? Which are the dependent and independent variables involved?
 - b. How to assess the relevance and feasibility of studying the variables identified?
 - c. Which is the dependency relationship standing among the selected factors?
3. Where to place time buffers in a sequence line holding predefined milestones and managerial constraints? Within, between, end, or hybrid?
 - a. How do the organization structural boundaries affect the allocation of buffers in the production line?
 - b. How do workload and competences affect the setting of buffers in milestones in the production line?
4. How to design a method to estimate cost-efficient time buffers in production units subject to a predefined service level?
 - a. How to model the relationships identified?
 - b. How to measure the production line performance regarding service delivery, throughput, and cost?
 - c. Is this tool presenting a better off from the current situation?
 - d. Is this tool friendly for users?
 - e. Is the model robust enough for generalization?

2.4 Research methodology

This project can be classified by Van Aken et. al (2005) as a design-focus and theory-based business problem solving (BPS). Regarding the latter, although researchers in the field would define this study as prone to be relevant rather than rigorous, the “theory-based” in Van Aken’s approach refers to the reliance on comprehensive, critical, and creative state-of-the-art literature instead of a formalized way of referring to rigorousness. Furthermore, the BPS approach as stated by these authors “improves the performance of a business system, department or a company on one or more criteria. Usually, the actual objectives of a BPS project are of operational nature, related to the effectiveness and/or efficiency of operational processes”, all latter being aligned to this practical study aims.

Moreover, the selection of this research approach is supported by Van Aken et. al. (2005) statement: “if academic research is irrelevant, practitioners will look elsewhere for solutions”. Therefore, this study is meant to focus on the major requirements of our client company by designing a tool aimed to give support to the planning phase of specific production units in this manufacturing setting. Furthermore, this study is intended to meet Van Aken et. al (2005) criteria by being design-oriented, client-centered, performance-focused, theory-based, and able to be justified.

2.5 Research scope and deliverables

This master thesis research scope was defined and agreed by all partners involved, namely, the student, the academic supervisor, and the ASML representatives. The latter can be summarized in the following table:

Scope	In	Out
Product	<ul style="list-style-type: none"> • NXT 19X0 • XT 8X0 	<ul style="list-style-type: none"> • NXE • PASS • XT 14X0 • XT 1000 • XT 400 • XT 1950
Processes	Planning concerned to: <ul style="list-style-type: none"> • FASY • Test 	<ul style="list-style-type: none"> • ASSY • Prepack • Cabin • Procurement • Material Ordering • Suppliers • Inbound logistic • Warehouse

		<ul style="list-style-type: none"> • Customer install • Individual manpower assignment • Workforce planning • Tooling planning
Location	Veldhoven	Tempe, Wilton, Ace
<p>Note: The setting of buffer time in shifts is out of this project scope.</p>		

Thereon, the deliverables of this master thesis will be:

1. Literature review conducted for buffer management in manufacturing systems subject to environmental and system uncertainties. (Perez, B., 2011)
2. An overview of the factors influencing the buffer time estimation for a particular manufacturing setting.
3. General planning tool for the estimation of time buffers subject to a predefined service level.
4. Performance analysis for the tool.
5. Scenario analysis.
6. Recommendation for:
 - a. Periodicity of setting parameters in SAP.
 - b. Implementation (stakeholders specific).
7. Master Thesis report.

2.6 Solution Approach

Aligned to the logic of BPS projects setup, this study will follow the classic problem-solving cycle characterized by five basic process steps (problem definition, analysis & diagnosis, plan of action, intervention and evaluation) triggered by an initial problem mess (Van Aken, 1997). The latter, undertaken jointly with the reflective cycle as in Van Aken (2005), brings the overall solution approach for this research project. See figure 2.1 for a better understanding of this study solution approach.

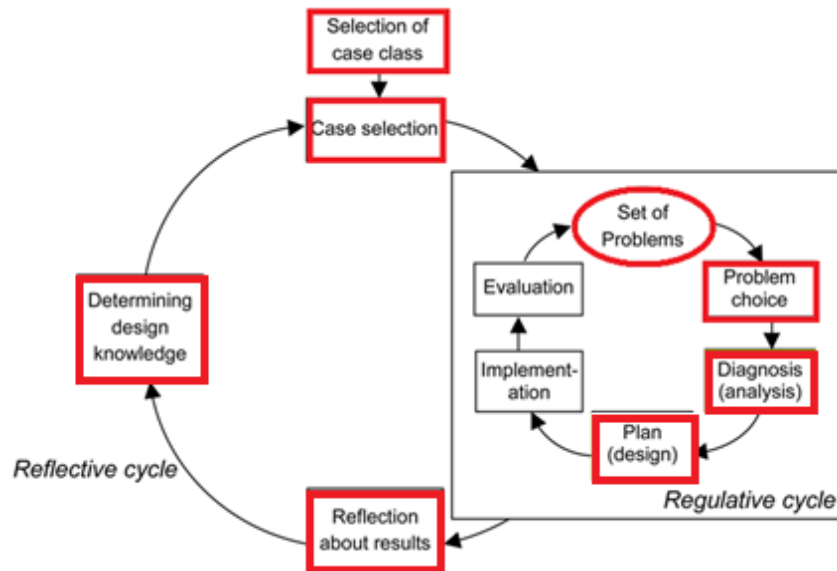


Figure 2.1 Reflective and regulative cycle (Van Aken, 2005)

Due to time restrictions, red remarks shown in figure above stand as a way to depict the basic steps needed to take towards the completion of this research project. At this point, some of the latter have been described already in this report. For instance, the selection of case class made jointly with this thesis supervisor along with the case selection made from the gaps found in the literature research conducted, triggered the initial set of problems from which the definition of our actual problem was made. The problem definition step can be regarded as the driver of this study due to the agreement of all parties involved; namely, the student (the author of this proposal), the principals of the project, and this thesis supervisor. Therefore, next chapters in this master thesis are aimed to report the diagnosis, plan, the reflection about results, and the overall knowledge gotten from this research project. All in all, the Design part stands as the main focus of this master thesis and is supported by the red remarks depicted in the regulative cycle in Figure 2.1.

CHAPTER 3: ASML manufacturing lead times planning

The aim of this chapter is to provide a detailed description of the current way of planning lead times in ASML manufacturing. In doing so, Section 3.1 gives an explanation of cycle times and lead times definitions in ASML. Thereon, being several departments involved in the setting of lead times Section 3.2 depicts a process overview explained further in Appendix D. Thereafter, the two production units in scope (FASY and Test) are presented in Section 3.3; therein, their way of working is described together with the time schemes they use. Later, the environmental and system's uncertainties underlying the lead time planning of these units are presented in Section 3.4. Therefore, the purpose of Section 3.5 is to present the buffer levels used in ASML manufacturing for coping with those uncertainties. Thereafter, Section 3.6 explains the current way of buffers estimation in FASY and Test for our two products in scope. Finally, Section 3.7 depicts the current planning parameters and the delivery performance resulting from those.

3.1 Cycle times, lead times and time schemes definitions in ASML.

As explained in previous chapters, Manufacturing in ASML is comprised by ASSY, FASY and Test. These units pertain to a particular organizational division (BO or DO) and are responsible for reporting weekly performance indicators. Therefore, the setting of unique cycle times (CTs) definitions in manufacturing requires the agreement of several parties holding diverse interests. As of February 1st, the bargaining between divisions and units is still an ongoing process, resulting in several definitions supporting the performance "achieved" in each dependency. For this master thesis endings, the CTs definitions in FASY and Test, so as the overall ASML manufacturing LT definitions, are based on the GID document³ and the input gotten from several interviews run within the departments involved in this project.

The general cycle time and lead time definitions in ASML follow:

- *Order lead time*.- "The time between ordering (purchase order) and the confirmed delivery date. It is a (commercial) agreement between a customer and a supplier (internal or external)."
- *Routing lead time*.- "The planned time a job takes to traverse a routing, including the expected variability. This value is used for planning purposes."
- *Cycle time*⁴.- "The actual time a job takes to traverse a routing, from begin to finish."

³ The GID_Cycle_Time_Definition is not an official document in ASML, it is still a draft version.

⁴ *Note*: Cycle times are measured in calendar days. Therefore, whenever data was extracted from sources using takts as the reporting unit, a translation into days was needed. For the aim of this project, FASY and Test units' conversion will be explained:

In both machines, XT 860 and NXT1950, FASY works 2 shifts/day during the week and one shift/day on weekends; thus, 12 shifts/week. Thereon, 1 shift =0.58 days.

ASML manufacturing cycle time definitions are quoted below:

- *Manufacturing cycle time.*- “The time between the start of the first work order for a work center and sign-off of the system by the customer including the CSR’s and option of that system.”
- *Cabin cycle time.*- “The time between the start of the machine order / start of FASY for a system until the finish Prepack in test cabin (i.e. cabin utilization).”
- *FASY cycle time.*- The time between the start of FASY Prepare and Test start.
- *Test cycle time.*- “The time between the start of a system test with ATP as a result.”

Furthermore, CTs in ASML FASY-Test manufacturing are divided into milestones and these latter, into takts. Explanation follows:

Milestone.- regarded as the elapsing time in which a specific competence is allocated within a machine sequence. Be aware FASY and Test are two sequences, each holding more than one milestone.

Takt.- work package contained in a shift. Takts are settled in such a way that an operator is enabled to carry out predefined processes steps for an operation within 8 hours. Therein, breaks and processing time’s variability are accounted for.

Moreover, within ASML processes the definitions of A, B and C times need to be understood. See Appendix C for the depiction of this time categories. According to the GID document⁵, these time definitions follow:

A-time (Planned).- “Normative, minimum elapsed time under normal conditions between start and finish of a process. Where normal conditions are: Normal staffing, Normal operation, Skilled technicians, Normal working speed, Availability of qualified material, tools, procedures, and facilities.”

B-time (Not planned).- “Elapsed time for disturbances during manned hours between start and finish of an activity. Examples: logistical issues, reliability issues, incorrect procedures, etc.” In addition, eight types of disturbances are identified within the B-time category:

- B1 – Material missing
- B2- Materials quality issue
- B3- People issue
- B4- Tooling issue
- B5- Facility issue
- B6- Documents/Pack not Ok
- B7- Procedures issue
- B8- Technical issue

XT8X0 Test works 3 shifts/day during all week; thus, 21 shifts/week. Thereon, 1 shift will be regarded as 0.33 days.
NXT 19X5 Test, as FASY, works 2 shifts/day resulting on 1 shift =0.58 days.

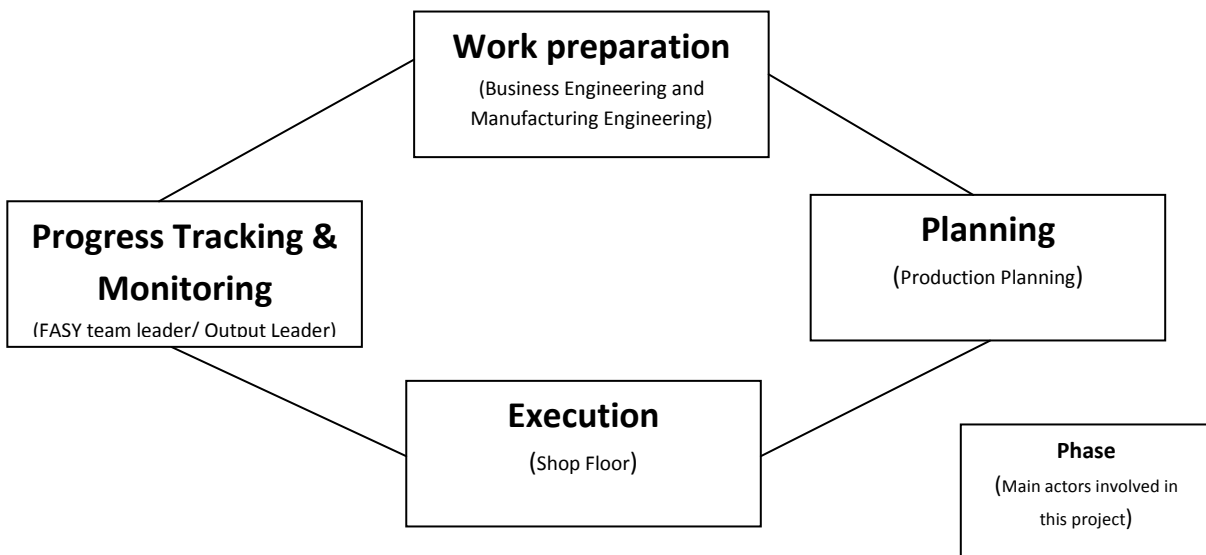
⁵ The GID_Cycle_Time_Definition is not an official document in ASML, it is still a draft version.

C-time (Planned).- “non-progress time, idle time. Examples: holidays, idle time during shifts and nights, lunch breaks.”

While the A-time and C-time are regarded as planned and defined for each process step in SAP, the B-time is not, therefore, the mitigation of disturbances’ effect on the actual CT stands as one of the main objectives in this study. Moreover, it should be remarked that in ASML even the planned cycle time without disturbances (thus, A+C) can be considered as unreliable. The latter due to the continuous introduction of upgrades, the effect of learning by doing, and all customer-related time due to the MTO framework to which this company is moving towards. Therefore, data analysis and calculations in this master thesis project will be based on the actual CT reported without making any A, B and C time categorization within CTs.

3.2 Departments’ involvement in ASML manufacturing lead times planning.

ASML Integral Manufacturing flow is shown below, although solely the main contributors in this project are shown and described below for each phase.



ASML Manufacturing works throughout four phases: work preparation, planning, execution and progress monitoring. As depicted above, work preparation is conducted by Business Engineering (BE) and Manufacturing Engineering (ME). The latter conjointly work brings the lead times used in the planning of orders releasing in the Planning phase by production planners. Thereon, based on the orders released and the lead times parameters introduced in SAP, the execution is carried out at the shop floor by competence teams, where progress is tracked and monitored by the group leaders of each production unit. The latter output serves for the analysis of next periods lead times by BE and ME, and the flow goes all over again. Refer to Appendix D for a more detail explanation of each phase.

3.3 FASY and Test way of working and time schemes description.

As mentioned in previous chapters, in ASML Manufacturing two divisions lead a systems production: BO and DO. Due to the latter, being FASY pertaining to the former and Test to the latter, so as in the definitions' case presented in section 3.1, difficulties arise whenever these divisions try to find commonalities in their way of working. These difficulties coming up from the different level of complexity handled in each sequence, so as the capacities needed, and their level of interaction with different departments within ASML organization. A description of FASY and Test way of working follows:

FASY

Once a system production order is released (thus, the FASY Start day in SAP) by the FASY planner, a cabin is assigned for this specific order by a cabin planner and a FASY team is allocated to that system. However, this plan is hardly met. In reality, few orders start according to their former start day, and instead, they are frequently rescheduled out in the FASY production plan. The latter coming as a result from predicted delays in components, anticipated capacity shortages, or simply, the cabin to which this order was formerly assigned is still occupied by a previous order that was expected to be finished by then. These possible obstacles are discussed in everyday meetings where participants from BE, PP, FASY and Test, communicate their status and since these departments are interdependent, their own interests are expressed for being able to achieve progress, and eventually achieve reliability in all dependencies. Therefore, bargaining takes places until a final agreement is reached. For instance, the FASY team leader would say the status for machine order 1234 is better than predicted and that a good progress in previous day would enhance the possibility of needing some components sooner, thereon, the FASY planner (which is aware of ASSY performance) would say how realistic it is to get these components sooner or if eventually the machine will be "on hold" due to an anticipated material shortage.

Whereas the FASY sequence for the XT8X0 system is, as of May 1st, divided into 4 milestones: Prepare, Build, System and Elmic; for the NXT 19x0, currently 2 milestones are considered: Prepare/Building and System/Elmic. Since in Section 1.4 it was explained the main processes carried out in each operation, this section is aimed to describe the way in which milestones and buffers are handled at FASY execution.

In a system's routing, each milestone in FASY is comprised by a predefined number of takts⁶. These takts accounting for both, the amount of takts needed if no disturbances were to occur and the takts needed for mitigating expected disturbances. The usage of these "protecting" takts varies between departments; for instance, FASY planners move these takts to the end of their planning for enhancing in this way the probability of supplies being available when needed. On the other hand, in the FASY progress Gants, these margins are settled between operations for protecting them from variations during execution. Although the "protecting" takts are used differently by departments, eventually, the

⁶ Takts in FASY are filled in accounting for both, planned minutes without disturbances and "protective" minutes in case of those.

planned cycle time for this operation, and consequently, the planned start date for the next operation, is the same.

Each operation in FASY is carried out by different teams, which hold different competences. Thus, a team working on Building is not skilled for working on System and so on. The latter is due to the complexities and experience required on each operation. Despite the latter, these teams are assigned to a machine order in such a way that the communication within operations is fluent in case any difficulty occurs further in the sequence and a rework is needed. For instance, there are N teams for each operation, and each are labeled accordingly, like P1, P2.. Pn for Prepare; B1, B2, .. Bn for Building; S1, S2,.. ,Sn for System; and E1, E2,.. En, for Elmic. Therefore, for a machine order xxxx, teams are planned together such as: P1, B1, S1 and E1. Assigning teams under this structure improves communication so as the level of commitment to deliver on time to the next operation. In this regard, each operation works according to predefined KPIs reviewed weekly in FASY. Currently, the target delivery performance varies per operation, being the latter justified in interviews by the level of complexity required and the variability underlying each operation.

Test

An order start day for Test is planned forward from the FASY start day shown in the AMSL file⁷. At the beginning of this project the execution of Test for standard and non standard machines was reported since Milestone 3, and thereon, the sequence of milestone continue until the ATP was run. As of 1st May, the latter has changed and Test will start from Milestone 5 onwards, the latter is due to the recently introduction of two new milestones in FASY.

All milestones in Test require different expertise and thus, the allocation of capacity within the sequence matters. However, contrary to FASY, the progress in Test milestones is not due to competence team performance, but due to one tester performance which is jointly responsible for reporting to the output leader their takt status and the notification of any disturbance, if occurred. Moreover, an ongoing project is aimed to enhance the flexibility of capacity in Test in such a way that if succeeded, all testers will be able to perform all milestones, and eventually the CT will be reduced due to no more manpower capacity shortages.

ME, at a takt level, defines the A-time in which an employee should be able to address progress in one shift. In this regard, contrary to the way FASY does, the decision was to keep all takts full for TEST. Therefore, disturbances are supposed to be eventually mitigated by “protecting” takts in milestones.

In both, FASY and Test, takts are fixed and as a consequence if the execution of a takt takes less time than as the one planned, operators are able to go home; otherwise, the takt is registered as lost and the operator coming for the next shift has to finish it. Thereon, if he succeeds in less time than a takt, the remaining time this operator is idle.

⁷ The AMSL- Advanced Machine Status List excel file is used within PP for the overall tracking of manufacturing orders

Moreover, a final note for FASY and Test way of working is required due to the impact this has on the production schedule and the overall service delivery performed on a system. In the current way of working, although takts are fixed and the idle time is accounted for in there; operations are not. Thus, in case a milestone is finished without disturbances and no “protecting” takts were used, the competence team or tester for the next milestone, if available, will come over to the machine without waiting for their formerly planned start day. The latter is possible due to the anticipation of this event from the daily review of the takt progress report by planners, FASY, and Test output leaders. Therefore, although the cycle time reported in a milestone is independent from the cycle time reported in the next milestone, the overall performance of a system order can be compensated. The same can be concluded at a sequence level, see figure 3.1. In this picture, although Test performance was far from the planned one, since FASY was earlier than planned and the latter was anticipated by Test, the latter started earlier and eventually, the overall planned order performs good do to the compensation gotten from both sequence’s performance.

Planned CT FASY		Planned CT Test	
Actual CT	Actual CT	Test	
Planned CT System			

Figure 3.1 Performance compensation

3.4 Environmental and system’s uncertainties present in the lead times planning at FASY and Test.

The planning of lead times for a system needs to account for the uncertainties coming from both, the environment and the manufacturing system itself. In the remainder of this section, system’s uncertainties will be regarded as those occurred within FASY and Test, and environmental uncertainties will be regarded as those coming from the market, and the variability inherent in the performance of suppliers. Particularly, this section identifies the elements enlisted below as the main drivers for the variability present in ASML FASY and Test cycle times.

Drivers for variability:

- B time and the learning curve effect,
- Economic trends effect,
- Product maturity,
- MTS / MTO framework,

B time and the learning curve effect.

As stated in section 3.1, ASML manufacturing CTs have an A, B and C time categorization where the B time stands as the non planned time in which the machine order is not having progress. Thereon, it was also explained ASML works with 8 B time types, those referred below, and for level of analysis purposes are classified into internal and external variables:

Internal factors:

- People shortages (B3)
- Tooling (B4)
- Facilities (B5)
- Packaging (B6)
- Procedures (B7)
- Technical issues (B8)

External factors:

- missing material (B1)
- material quality (B2)

Disturbances reported for XT8X0H and NXT19x0 last systems were analyzed for both, FASY and Test. If data were reliable, and thus, no FASY and Test output leaders' interests were involved in those reports, two conclusions can be obtained: 1) FASY cycle times are directly affected by both internal and external factors. Where the system's uncertainty is mainly due to manpower capacity and the external uncertainty is due to missing material from suppliers, namely, ASSY. 2) Test cycle times are completely affected by system's uncertainties due to manpower capacity, procedures, tooling, and above all, technical issues in execution.

For illustration purposes, Table 3.1 depicts the case of XT8X0. Therein, disturbances records for the last 35 systems are summarized; an example for interpretation follows. In the case of Build it is shown that 71 % of the cases a disturbance occur, if so, in 30% of those cases B1 contributed for a machine being "on hold", 27% B2, 33% B3, and so on. However, since one order could be "on hold" several times and due to different causes during a milestone, percentages can sum up above 100%. Overall, the average contribution each B time has on the reported duration of disturbances for FASY is shown at the lower row in the table; therein B2 and B3 are presented as the main causes of disturbances in FASY cycle times. Furthermore, following the same pattern for interpretation, Test disturbances are mainly caused due to B8 followed by B3.

Furthermore, it should be noted that the learning curve effect on these systems could be measured by regarding the trend of disturbances presented overtime. The latter is due to the steady introduction of upgrades and new procedures in manufacturing which make difficult the estimation of the impact it has on a system CT the benefits of learning by doing and the expertise gotten by repeating tasks.

Milestone	Prob. of success	Prob. of disturbance	FASY							
			B1	B2	B3	B4	B5	B6	B7	B8
Prepare	90,3%	9,7%	100%	0%	0%	0%	0%	0%	0%	0%
Build	29,0%	71,0%	30%	27%	33%	6%	3%	0%	3%	0%
Sys	22,6%	77,4%	3%	42%	30%	6%	3%	0%	6%	18%
Init	22,6%	77,4%	9%	52%	42%	9%	0%	0%	21%	12%
		Av	10%	23%	20%	4%	1%	0%	6%	6%

Milestone	Prob. of success	Prob. of disturbance	Test							
			B1	B2	B3	B4	B5	B6	B7	B8
MS3	0,0%	100%	6%	9%	37%	14%	3%	3%	26%	97%
MS4	0,0%	100%	3%	11%	49%	9%	6%	0%	17%	97%
MS5	3,0%	97%	17%	11%	77%	40%	3%	0%	29%	97%
MS6	0,0%	100%	0%	9%	49%	49%	17%	3%	43%	100%
MS7	0,0%	100%	6%	6%	34%	31%	6%	0%	49%	100%
		Av	6%	9%	49%	28%	7%	1%	32%	98%

Table 3.1 XT8X0 Disturbances' percentages.

Moreover, Figure 3.2 depicts the probability density functions of the XT 8X0H CT and disturbance duration. Therein, it is shown that both data sets fit a Gamma distribution, holding a positive skew of 0.15613.

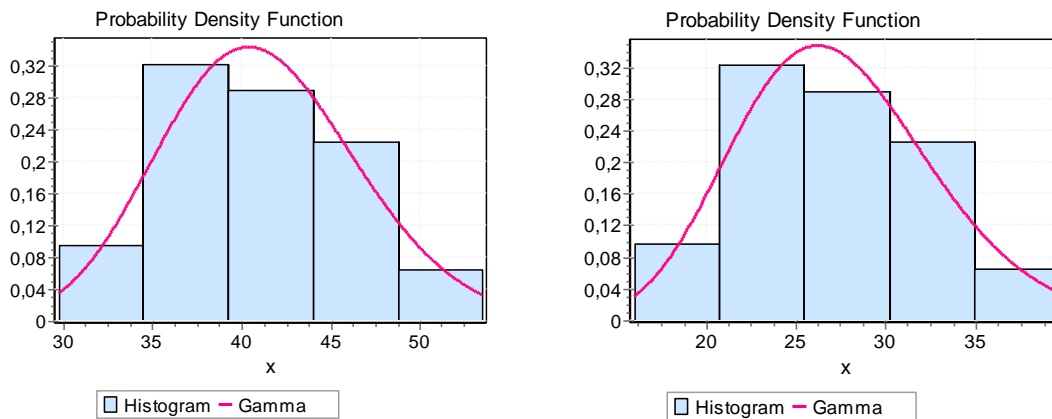


Figure 3.2 PDF XT 8X0H CT duration (left) and PDF XT 8X0H disturbance duration (right).

Economic trends effect

Manufacturing lead times are defined according to a target service level. However, this latter is entirely influenced by the economic trends affecting the semiconductor industry to which ASML pertains. In this regard, two scenarios are identified, both providing a different effect on the lead time planning in manufacturing: an industry upturn and downturn.

Industry upturn.-

Since an upturn means high demand, ASML's aim during this period is to produce as much as possible at the lowest cost. In doing so, lead times quotation should be both, minimal according to a target service level and accurate enough for keeping production plans stable and reliable.

Industry downturn.-

On the other hand, during a downturn, the target service level can be kept relatively low to an upturn due to several reasons: customers are not eager to receive their orders; many suppliers keep their own target service low; or even, on extremely cases, the latter declare themselves on bankruptcy.

Product maturity

Depending on the level of maturity a system has, so is the expected frequency of CT reviews and the protecting time needed at each level. The more mature a product is, the fewer procedures and upgrades are prone to be introduced, and if so, their impact on the system's routing would be significant just when reviewing longer periods of time. Furthermore, since operators, and overall the organization, become more expertise in their roles, disturbances duration are shorter, resulting on lower variability on operations compared to the high variability characterizing new routings.

MTS/MTO frameworks

The fact that systems in ASML are tailored increases the level of variability in some milestones. Except for the XT860, which customization is done at the field, all other systems have their CODP at the end of Test. Based on Sales order information, a MTO is connected to a MTS order, new work instructions are created, and the MTS machine is connected to the system's routing. The latter encloses information concerning the substeps required per process step for a customer-specific machine. Therefore, building the new options claim the adherence/deletion of materials, and thus, the awareness of high variability in the CTs of those Test milestones.

3.5 Buffers as defined in ASML manufacturing

Four levels of buffers support the execution of each order in ASML. Before getting into these levels description, it should be reminded that manufacturing in ASML works under a takt system, being a takt regarded as the work package for one shift. The latter brings us to the lowest level in buffer, the "takt idle time". This takt idle time is aimed to mitigate the effect of deviations in the planned A time in such a way that the work package can be finished in one shift. If the takt idle time is not enough, the takt should be enlisted as "lost", and gives rise to the next level of buffer. In this regard, the second level of buffers concerns to "buffer shifts" or "milestone buffer", aimed to mitigate the effect of takts "lost" in the compliance of a Milestone, which are regarded as a group of takts referred to same labor competences. Thereon, since a system order consists of several milestones, the third level of buffer, known as "order margin", enhances the possibility of the order to be finished in time if any milestone was delayed. Finally, a "CAL margin" is set by the board of directors for preventing customer delays in case the order margin were not sufficient to cope with the deviations encountered along the line. Since the Cal margin is out of these project stakeholders' responsibilities, it is automatically out of this project scope as well. Furthermore, it will be assumed the work packages are well defined, and thus, buffers in

takts will be also out of this research project scope. Figure 3.2 depicts the first three levels of buffer in an order.

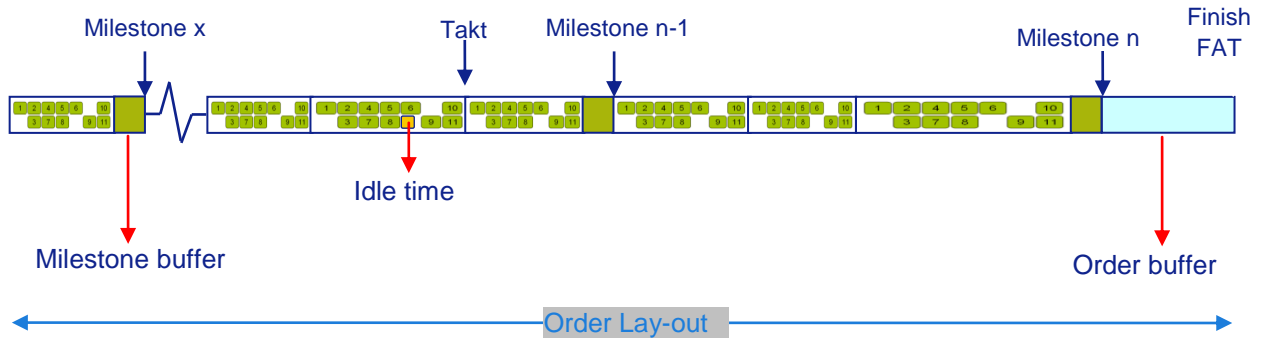


Figure 3.2 Buffer levels (Source: Four levels of buffer in takt system routings.ppt)

As the current way of work in ASML, BE is in charge of setting the Order buffers and ME is responsible for setting buffers at the takt and milestone level.

3.6 Current way of estimating buffer time in FASY and Test.

The current way of buffer estimation differs severely among departments in ASML.

FASY

From interviews it was stated that FASY way of buffer estimation is based on FASY team leader experience jointly with discussions and predictions gotten from the daily meetings with FASY planners. Therefore, FASY team leader, being aware of suppliers' reliability and the variability observed on each operation from last systems, lead him on the estimation of buffer sizes for each milestone. Thus, as of 1st May, neither a tool nor any specific calculations underlies the setting of buffer sizes in FASY. Furthermore, the takt idle time is set by the FASY sequence owner according to the estimated time breaks and team meetings will take.

Test

In Test there are different methods for specific systems. In this regard and for the milestone buffer setting specifically, the case of XT 8X0 and NXT 19X0 can be discussed. For the former, since the XT 860 system is not customized in test, milestones are hold as in a MTS system, where the respective buffer is calculated by the use of a ratio or proportion from the number of shifts available after the order buffer was taken off from the "Aspiration CT", which is the improvement target CT used for planning and set by

TEST group leaders. Thus, as stated by the sequence owner in TEST, buffers in milestones are a consequence of playing with numbers, from the time left after the Aspiration CT. Contrary to this methodology, since a 75% of delivery performance is pursued in Test, the milestones buffer calculation method for NXT 19X0 makes use of a factor based on the third percentile of the system's Box plot resulting from the analysis of the last 12 CT recorded. Finally, the order buffer (or system buffer) is the time left for a system to be delivered to a customer after the Aspiration CT has been set by Test group leaders. No extra computations underlie this latter.

Therefore, as of 1st of February, neither FASY nor Test makes use of a special tool for addressing the variability underlying this manufacturing setting.

3.7 Current planning parameters and delivery performance records from the last systems.

This section present the planning parameters used in FASY and Test as of 1st February. Since data was collected in takts, a translation in days was necessary accounting for the number of shifts under which each sequence and product type works. Tables below depict the latter.

	Planned CT TAKTS					Planned CT DAYS			
	XT 860		NXT 19x0			XT 860		NXT 19x0	
	PT	Buffer	PT	Buffer		PT	Buffer	PT	Buffer
Prepare	1		2		0,58		1,16		
Building	6		8		3,48		4,64		
Buffer - MS1	0			9				5,22	
System	3		5		1,74		2,90		
Init	3		4		1,74		2,32		
Buffer - MS2		6		8		3,48		4,64	
MS3	4	9	5	8	1,32	2,97	2,90	4,64	
MS4	3	7	8	9	0,99	2,31	4,64	5,22	
MS5	4	9	7	12	1,32	2,97	4,06	6,96	
MS6	5	10	5	3	1,65	3,30	2,90	1,74	
MS7	3	7	5	5	0,99	2,31	2,90	2,9	
ATP	0	16	-	-	0,00	5,28	-	-	
MS8	-	-	8	1	-	-	4,64	0,58	
Upgrade	-	-	0	12	-	-	0,00	6,96	
MS9	-	-	8	5	-	-	4,64	2,9	
MS10	-	-	8	5	-	-	4,64	2,9	
MS11	-	-	8	2	-	-	4,64	1,16	
CODP	-	-	12	12	-	-	6,96	6,96	
MS12	-	-	11	13	-	-	6,38	7,54	

Note: the current target service level is 75%.

By using these parameters and data collected from week 35 2010 to week 2 2011 for XT8x0 and from week 15 2010 to week 40 2010 for NXT 1950, the following performance was observed. In the case of XT 860, FASY delivered as planned in 48% of the cases while for the same system, Test delivered as planned 36% of the cases, resulting on a 30% of delivery performance for this system. In the case of NXT 1950, FASY never delivered as planned and Test did so in just 14% of the cases; resulting on a system's delivery performance of 11%. The latter figures result from analyzing the performance of the whole data set collected from a time scope of 4 and 6 months for the XT860 and NXT1950, respectively. However, if the periodicity for reviewing norms (hence, CTs) in ASML is followed and the CTs for 3 months were addressed, the delivery performance for those production units follows. In the case of XT860, FASY and Test delivered 27% of the cases in time with 144 days delayed. As for NXT1950, FASY and Test delivered 11% of the cases in time with 506 days delayed.

CHAPTER 4: Buffer strategy for the planning of reliable lead times in serial production systems subject to a targeted service level.

The aim of this chapter is to propose a buffer strategy for the planning of lead times in production lines characterized by unreliable, unbalanced and sequential stages exposed to high capital risk. In doing so, a targeted service level is pursued while the costs coming from production plan's instabilities are kept as low as possible.

The objective: Quote minimal time buffers for a system incoming orders such that a certain level of service is achieved. Service level is defined as the percentage of orders delivered in time.

General approach: approximate the lead time for all orders released in period t by the analysis and adjustment of data from period $t-1$, until a predefined service level is achieved by the determination of cost efficient time buffers in production lines subject to environmental and system's uncertainties.

This chapter is comprised by four sections. Section 1 presents the general assumptions to be accounted for in this chapter. Therein, in pursuing reliability in the lead times planning Section 2 explains the need for buffering in companies producing under customers' committed agreements. In doing so, Section 3 provides buffer alternatives for improving lead times reliability, wherein the usage of time buffers is observed as preferable for the settings assumed in this study. Finally, Section 4 provides a time buffer strategy for the estimation of reliable internal lead times for the planning of the assumed manufacturing settings in Section 1.

Moreover, the reader should be aware this chapter is aimed to provide a general method where the usage of a certain number of parameters is required. The way for determining the values of these parameters, in general, depends on the production situation under study. Due to the latter, Chapter 6 devotes a section to discuss general ways to compute those values, and for this master thesis purpose, discusses the way choices were made and parameters were calculated in the application of this buffer strategy in ASML manufacturing settings (See Chapter 5-Appendix G).

4.1 General Assumptions.

For the remainder of this chapter, be aware of the following general assumptions.

- The capital intensive sequence is from the type:

Stage j			Stage j+1		
Milestone i stage j	Milestone i+1, j	Milestone n, j	Milestone i stage j+1	Milestone i+1, j+1	Milestone n, j+1

- All levels in sequence are independent. Thus, the duration of stage j+1 does not depend on stage's i duration. Similarly, the duration of milestone i+1 does not depend on milestone's i duration.
- Execution is run by competence teams associated to each milestone.
- Milestones are run under an "as soon as possible" framework. Therein, milestone i+1 starts right after milestone i was completed.
- The distribution of milestones and sequence duration is known.
- The average processing time for each milestone is known.
- Manpower capacities can be reallocated. Thus, no idleness costs are immersed.
- The tardiness cost is measured at the end and not at intermediate levels.
- Customers expect their orders as soon as possible.
- Production is triggered by customers' commitment agreements.

Moreover, the content of this chapter can be directed to companies holding the characteristics enlisted below. Refer to Appendix E for a more detailed explanation of each one.

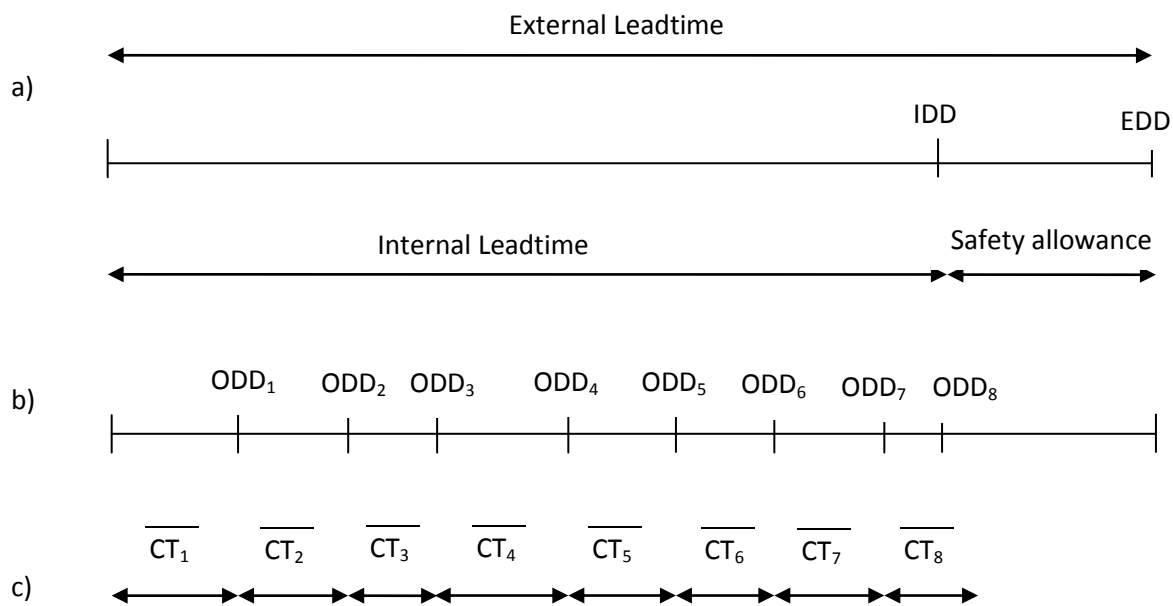
- 1) Exposed to operators' and organization's learning curves effect.
- 2) Characterized by the continuous introduction of new technologies (R&D-oriented), e.g. high tech systems, capital goods, etc.
- 3) Working under periodic lead times.
- 4) Characterized by a sequence comprised by m serial stages where predefined n milestones are found.
- 5) Working under a fixed "tacted" scheme.
- 6) Executing "as soon as possible".
- 7) Can be distinguished by their capital intensive, low- volume high-risk production.
- 8) The effects of rescheduling are spread all over manufacturing plans. (See Section 1.4)

4.2 The need to buffer.

There are typically two aspects that planners regard as a goal when planning the lead time for next period's orders. Particularly, a low lead time and high delivery reliability are desirable. In this regard, meeting the later objectives goes aligned to an enhanced internal performance which makes feasible the eventual attainment of customers' expectations. Regarding the latter, a special distinction is needed here between two types of lead time quotations: the internal and the external one (See Figure 4.1.a). Under these manufacturing settings, whereas the internal lead time is regarded as the one accounting for the average processing time and the average disturbance time along the sequence routing of a product; the external lead time, based on Bertrand (1983) definition, comprises the time from the sequence start up to the quoted due date to the external customer. Thus, the difference between the external due date (EDD) and the internal due date (IDD) stands as the delivery safety allowance which in this study is assumed to be determined according to the interests of several dependencies, besides manufacturing, in the organization.

Attaining an internal due date (IDD) requires the previous attainment of all operations' due dates (ODD) along a sequence routing (Figure 4.1.b). In addition, the reader should be aware that meeting an ODD under these variable settings requires an accurate prediction of operations completion times; hence, operations lead times. Furthermore, the awareness of uncertainties all over a product sequence claims for the recognition of an average disturbance time in the planning of operations lead time; being the latter regarded as the major part of operations' throughput times.

Moreover, it is assumed that this manufacturing setting work under a deterministic MRP framework; wherein, average lead times account for uncertainties. Due to the latter, the average cycle time of an operation includes its average processing time and the average time for disturbances (Figure 4.1.c). In this regard, since the average processing times are assumed to be known, the achievement of internal due dates is influenced mainly by the accurate (hence, reliable) estimation of disturbance time in operations. The operation level comes as the elementary level for this estimation due to the variable nature of this setting and the high worse off resulting from rescheduling subsequent due dates. As for this latter, being early and tardy at intermediate levels: 1) reflects a poor prediction of operations completion time, 2) requires additional hours spend in planning, 3) minimizes the internal delivery performance, and above all, 4) increases the probability of not achieving following DDs. All in all, being reliable to customers depends severely on an accurate estimation of the internal lead time (hence, buffers); being the latter regarded as the main focus of this study.



Where $\overline{CT}_i = \overline{PT}_i + \overline{DT}_i$

Figure 4.1. Time schemes management.

4.3 Alternatives for enhancing lead times reliability.

Lead time approximation can be done in a number of different ways, although a number of these approaches can be regarded as ineffective or not practical. For instance, the possibility of adjusting a lead time for each independent order. This alternative would mean an “every day” adjustment on MRP parameters and a higher degree of responsiveness and coordination among global and internal supply chain actors would be required. Furthermore, management costs would be huge, so as the capital risk involved; especially for those firms producing under customers commitment agreements. Being the latter referred to the releasing of production orders without their respective purchasing order being entirely assured.

An alternative approach is to approximate lead times by developing a function defining the relationship between the lead time and the duration of disturbances as reported from execution in the last period. Whichever alternative for estimating lead times is chosen, the aim is to improve the internal lead time reliability in production plans. Particularly, this goal becomes crucial when processing times are exposed to high variability due to disturbances, learning curves effect and the steadily introduction of new

processes. Therefore, planners are obliged to make a choice among the several ways of increasing lead times' reliability before working on their estimation.

How to improve the reliability of lead times in production plans? How to buffer?

There are several ways in which companies can deal with the uncertainties encountered in production and thus, be able to pursue the timely delivery of orders. In this regard, four alternatives for buffering uncertainties are discussed: 1) Safety stock, 2) Safety time, 3) Overtime, and 4) Overcapacity.

1) Safety stock.-

The main objective of safety stocks is to absorb variations in demand / supply and to buffer errors in the inventory records occurred during manufacturing. Making use of this alternative requires the recognition of high costs associated to holding components in a capital intensive production line, as the one assumed in this study. Due to the latter, this alternative will be regarded as the least attractive among the others.

2) Safety time.-

When comparing the usage of safety stock and safety time in the planning of lead times, Molinder (1997) observed that in the case of high variability in demand and high variability in lead time, the lowest cost is gotten by means of safety time. The latter is a result from the possibility of working with more stable production plans and thus, a better performance of associated departments which base their planning on the production plan's due dates.

3) Overtime.-

For the case of high variable production lines working with competence teams, operating under a 24/7 framework requires either a high degree of flexibility among resources in manufacturing or the frequent reallocation of those. The fact that both latter are too costly and that high variability is assumed as underlying the cycle time of operations, make this alternative not attractive if used in isolation from any of the others .

4) Overcapacity.-

In this regard, capacity is referred to the manpower, tooling, facilities, and all physical resources used in production besides the materials coming from suppliers. By assuming high variability in demand and the usage of competence teams working in production, increasing capacity would require the frequent hiring and firing of personnel, which can be associated to high managerial costs. Furthermore, any benefit expected from product maturity and learning curves effect, will be diminished by the continuous and costly training of new employees. Moreover, investing on more facilities and tooling can be regarded as unfeasible due to the demand uncertainty characterizing these settings, in which high depreciation costs are immersed.

Although it is clear that service can be improved by any of the just mentioned, as advised in literature and from our own analysis, attaining a cost efficient service level in high variability- capital intensive production lines, is preferable by means of safety time rather than any of the other alternatives discussed. From now on we will refer to safety time as the time buffer needed to be allocated for enhancing the reliability of planned internal lead times in production plans seeking the achievement of a targeted service level.

4.4 Buffer Strategy

Based on the lack of studies⁸ conducted on manufacturing settings such as the ones assumed in Section 1, this section is aimed to propose a strategy for the estimation of time buffers in the planning of lead times. In doing so, it should be recognized that time buffer sizes can be determined in a number of different ways. Two approaches are discussed here: the detailed and holistic approach.

1) Detailed approach. “The sum of the parts”.

Since all levels in the sequence are independent, this alternative determines a time buffer for each level (namely, milestones or stages) by considering its local behavior. For instance, if time buffers were to be allocated at stages, under this approach a time buffer would be determined for each stage in the sequence without regarding the overall behavior. Thus, the total time buffer in the sequence would be the addition of the time buffer determined for stage 1 + the time buffer determined for stage 2, and so on.

2) Holistic approach. “The whole into parts”.

Contrary to the detailed approach, this alternative directly grasps the whole without consideration of the parts. Therefore, the analysis of the total sequence behavior comes prior to the assignation of time buffers at each level. For instance, if time buffers were to be allocated at stages, under this approach a time buffer would be firstly determined for the total sequence and then spread among stages.

Undertaking the detailed approach in this buffer strategy would bring the risk of overestimating the usage of time buffer at each level, resulting on a lot much higher overall delivery performance than the predefined one. For instance, consider the case of a sequence comprised by 3 milestones. If the target service level (t.s.l.) is 70% and each milestone set the latter as their own t.s.l., the overall service level will always be above 70% and adjusting each for attaining an overall target close to 70% would mean a lot of time due to the trial and error approach needed. Therefore, the buffer strategy presented in this master thesis will regard the holistic approach as the most suitable for estimating time buffers in these manufacturing settings subject to a targeted service level.

⁸ Refer to Appendix F for the related work on the setting of lead times in serial production systems.

Moreover, it should be remarked that throughout this buffer strategy a minimal quotation approach is followed. Therein, the planned time buffer (hence, planned lead time) is kept as short as possible with the aim of lowering the cumulative early days at execution; and thus, keeping the associated earliness and instability costs as low as possible. Furthermore, the suggestion of this minimal quotation approach is based on Parkinson's Law, which states: "where safe estimates are used, the execution of a task, as a rule, consumes the entire time available anyway, and even delays occur along the way."

The buffer strategy described in this chapter is based on the following steps, all from which an explanation comes further in this chapter.

Step 1. Determination of a cost efficient target service level.

Step 2. Placement of time buffers in sequence.

Step 3. Estimation of time buffer sizes under a minimal quotation approach.

4.4.1 Determination of a cost efficient target service level.

The cost efficient target service level for a sequence will be computed based on the optimization model presented in Hnaien et. al (2008) for the lead time planning of serial production systems. The latter motivated by the similarities found between these authors considerations and many of the assumptions presented earlier. Particularly, in Hnaien et. al (2008) it was considered:

- The production system for one type of product.
- Serial levels working under periodical planned lead times.
- The semi-finished product is processed throughout the levels and the finished product is produced at the last level.
- The lead time distribution for all levels is known.
- There are no stocks at intermediate levels.
- Execution is run under the “as soon as possible” framework.

Due to the backwards planning in which MRP works, the release date of the first operation is the one optimized in Hnaien. The expression below is the optimality condition in Hnaien et.al for the discrete version of the Newsboy model. Therein, the cumulative distribution function $G(.)$ of the total lead time is used.

$$G(L_{pt}^* - 1) < \frac{b_{pt}}{h_{pt} + b_{pt}} < G(L_{pt}^*)$$

In this expression the backlogging and holding cost at the last level is the criterion used for optimization. For this buffer strategy purpose and aligned to the assumptions described in Section 4.1, the terminology in this criterion will be modified and the backlogging and holding costs will be replaced by the tardiness and earliness cost, respectively. Therefore, in this expression, h_{pt} represents the unit of cost coming from each day an order was earlier than planned and b_{pt} represents the unit of cost from being one day delayed from the original plan.

Thus, the cost efficient target service level (t.s.l.) for a product sequence follows:

$$\alpha_{pt} = \frac{b_{pt}}{h_{pt} + b_{pt}}$$

A remark at this point is needed before getting further into this buffer strategy. The expression above advises a cost efficient target service level for the sequence of product p in period t. Despite the latter, the reader should be aware that in practice, management decisions are prone to influence the target under which many production lines work on, due to the converging of several organizational interests in its setting. Nevertheless, this chapter will refer to the target service level for product p in period t as the one resulting from the expression above; thus, α_{pt} .

Once the t.s.l. has been computed, the total buffer size for the sequence can be determined, however, for presentation purposes, keeping the flow in section 4.4.3 requires first the place of buffers to be addressed in next section.

4.4.2 Placement of time buffers in sequence.

This buffer strategy continues by making a recommendation for the placement of time buffers in the production of p type of product. In doing so, it should be reminded that all milestones in this production sequence are assumed to be executed by humans. Thus, the objective of this buffer strategy is to mitigate the effect of disturbances due to both, capacity shortages (supplies, facilities, tooling, people, etc.) and human-related risks such as the untimely execution of operations. For capital intensive production environments, as the ones assumed in this study, the stability of execution of all elements in the production plan becomes crucial to avoid the costs immersed in rescheduling the plans of internal, and eventually external, supply chains. The latter together with the high variability characterizing the duration of manufacturing operations in high tech sequences, and the assumption of competence teams assigned to them, claim for a buffer arrangement which would guarantee production stability and the meeting of contractual deadlines for the individual production phases; thus pursuing the reliability in the planned internal lead times. Three scenarios were studied in order to come up with the best placement of buffers in serial sequences holding the particularities of these manufacturing settings. Therein, the costs immersed in whether to set the buffer at the end, between stages or in each milestone, were analyzed and are briefly discussed here.

- Buffer at the end.-

This analysis involved the usage of production plans in which all resources were scheduled according to the planned processing time as if no disturbances were to occur in period t ; thus, following a best case approach. In doing so, if actual disturbances do happen, the buffer settled at the end was consumed progressively and aimed to attain the target service level in the sequence. This approach can be expected to minimize the actual lead time and eventually improve the throughput by being ready to start a milestone due to the “already” available resources. However, in practice, the variability underlying the duration of operations and stages in these manufacturing settings, end up increasing the instability costs of reallocating people and all sort of resources in manufacturing.

- Buffer in stages.-

This scenario was run considering buffers at the end of each stage j in the sequence. Therefore, milestones within those stages were planned according to the best case approach in such a way that resources were available if operations were carried out on time. As in the “buffer at the end” case, the instability costs of rescheduling, coupled this time with an enlarged tardiness cost presented in this scenario, made this alternative the least beneficial for these production settings.

- Buffer in milestones.-

This case was studied by allocating buffers within stages. Thus, each milestone lead time comprising a time buffer aimed to protect the stability in the planning of subsequent milestones if disturbances occur. In doing so, the instability costs are reduced so as the tardiness costs in the sequence due to the actual mitigation of capacity shortages by the realistic approach this planning has. Thus, by setting time buffers in milestones the target service level can be attained holding lower instability and tardiness costs than in any of the two scenarios discussed before.

Due to the latter, it is appropriate to allocate a time buffer in each milestone to protect both, production plans and the timely execution of a production order. However, being aware the variability accounted for each milestone in the sequence differs, this time buffer spread will not be even but instead, a procedure for estimating each milestone time buffer will be explained in next section.

4.4.3 Estimation of time buffer sizes under a minimal quotation approach.

The estimation of time buffers sizes for the planning of lead times can be done in a number of different ways. This subsection will describe three possible methods: the Regression-based, the Distribution-based, and the Project view-based method. The steps to be undertaken in each of the just mentioned will be described and followed by a brief assessment regarding their level of accuracy and feasibility for further implementation.

Method 1- Regression - based

- 1) Define the target service level for product p in period t.

$$\alpha_{pt} = \frac{b_{pt}}{h_{pt} + b_{pt}}$$

- 2) Find the regression model for product p in period t and compute the first estimates for the total lead time L_{pt} and buffer size B_{pt} for this sequence.

For predicting a first good estimate for a product's sequence buffer, find the regression model for product p in period t from period t-1 records. This regression model showing the dependency relationship between the average duration of disturbances in period t-1, d_{pt-1} , and the actual cycle time reported at the sequence level for that same period, A_{pt-1} . Thus,

$$A(d_{pt-1})_{pt-1} = X_{pt-1} + m * (d_{pt-1})$$

where X_{pt-1} stands as the planned processing time without disturbances and $m * (d_{pt-1})$ is the contribution the average duration of disturbances has on the actual cycle time of a system. Thus, m is the beta coefficient in the regression model depicting the units of time the cycle time A_{pt-1} increases whenever the average disturbance duration d_{pt-1} does in one unit.

Thereon, the first estimate for the planned lead time of a sequence for product p in period t is based on the planned processing time without disturbances and the predicted time for disturbances coming from the regression model. In this regard, since disturbances are aimed to be mitigated by time buffer (hence, safety time), in the expression below, B_{pt} represents $m * (d_{pt-1})$, which aligned to the holistic approach chosen for determining buffers sizes in this study, stands as the first estimate of total buffer size in the sequence of product p in period t .

$$L_{pt} = X_{pt} + B_{pt}$$

- 3) Validate L_{pt} with historical data A_{pt-1} and adjust accordingly.

Since our objective is to mitigate the effect of disturbances while attaining a cost efficient service level, α_{pt} , the planned lead time for product p , L_{pt} , should be compared with the actual cycle times, A_{pt-1} , coming from last records. In doing so, the following steps should be taken.

- a. Find the number of orders, e , that based on L_{pt} are not delayed among the historical data.
- b. Calculate the current service level, SL%, using $SL\% = e/N$. Where N is the size of the data set.
- c. Is service level met?

Since the idea is to quote the minimum buffer B_{pt} for a target service level α_{pt} , the estimation of buffers will be based on the adjustment factor k . See expression below.

$$L'_{pt} = X_{pt} + k * B_{pt}$$

where,

$$B'_{pt} = k * B_{pt}$$

The procedure to calculate k is briefly described. As a start point assume $k = 1$, if the service level is not met, increase k value, otherwise lower it. k is assumed with two decimals and with an incremental value of 0.01. Repeat the latter until the service level is attained by keeping the planned lead times as minimal as possible. In the expressions above, L'_{pt} and B'_{pt} , represent the adjusted lead time and buffer size, respectively, in the sequence of product p in period t .

- 4) Estimate milestones buffer size B_{ijt} based on the adjusted total buffer size B'_{pt} and each milestone weight priority wpa_{ijt} .

Aligned to the holistic approach described at the beginning of Section 4.4 for the determination of buffers, regard B'_{pt} as the total amount of buffer to be spread within the milestones comprising the total sequence of product p . However, being aware the variability accounted for each milestone in the sequence differs, this time buffer spread will not be even but the priority weight wpa_{ijt} will serve to define the preference a milestone has in the assignation of time buffers among the other milestones. The calculation of this weight priority is based on each milestone's average duration of disturbances, d_{ijt} . The latter, divided by the sum of all average disturbances duration in milestones, represent the proportion of buffer time, from the total adjusted one B'_{pt} , a milestone in that sequence needs. The following expression represents this proportion.

$$wpa_{ijt} = \frac{d_{ijt}}{\sum_{j=1}^m \sum_{i=1}^n d_{ijt}}$$

Where,

$$\sum_{j=1}^m \sum_{i=1}^n wpa_{ijt} = 1$$

Once all milestones wpa are determined, use the adjusted sequence buffer size B'_{pt} computed in 3) to estimate each milestone buffer size B_{ijt} .

$$B_{ijt} = wpa_{ijt} (B'_{pt})$$

Thus, for period t, each milestone buffer size is:

$$\begin{aligned} B_{11} &= wpa_{11} (B'_p) \\ B_{12} &= wpa_{12} (B'_p) \\ &\vdots \\ B_{nm} &= wpa_{nm} (B'_p) \end{aligned}$$

- 5) Compute the planned lead time for each milestone L_{ijt} . Thereon, find the planned lead time for the total sequence of product p, L_{pt} .

$$L_{ijt} = X_{ijt} + B_{ijt}$$

Thus,

$$L_{pt} = \sum_{j=1}^m \sum_{i=1}^n L_{ijt}$$

Method 2: Distribution-based

- 1) Compute α_{pt} , L^*_{pt} , B^*_{pt} at the sequence level.

So as for defining a cost efficient service level, this method takes the model in Hnaien et. al (2008) as a baseline for estimating the optimal lead time in the sequence of product p in period t, L^*_{pt} .

$$G(L^*_{pt} - 1) < \frac{b_{pt}}{s_{pt} + b_{pt}} < G(L^*_{pt})$$

Where,

$$\alpha_{pt} = \frac{b_{pt}}{h_{pt} + b_{pt}} \text{ and } L^*_{pt} = G_{A_{pt-1}}^{-1}(\alpha_{pt})$$

The expression above shows that by making use of the G distribution from the cycle times reported in last period, A_{pt-1} , and the target service level defined for the sequence, α_{pt} , the optimal lead time for product p in period t can be gotten. Moreover, by subtracting the total planned cycle time as if no disturbances occur, X_{pt} , to the optimal gotten from Hnaien's expression, L^*_{pt} , the cost efficient buffer size, B^*_{pt} , can be determined.

$$B^*_{pt} = L^*_{pt} - X_{pt}$$

Thus,

$$B^*_{pt} = L^*_{pt} - \sum_{j=1}^m \sum_{i=1}^n X_{ijt}$$

- 2) Adjust B^*_{pt} to learning curve effects.

The cost efficient buffer size computed in 1) relies on the analysis of the actual cycle times reported from last systems, and thus, neglects any possible effect coming from operators and organizational learning. Therefore, being aware that the more times an operation has been performed, the less disturbances will occur (hence, the less buffer time will be required on each subsequent period), the adjustment of the cost efficient buffer size B^*_{pt} to the learning percentage k are required for the prediction of the time buffer size needed to produce first u^{th} systems. The following expression summarizes the latter.

$$B'_{pt} = B^*_{pt} \left(\frac{1}{1 + \log k} \frac{u^{1 + \log_2 k}}{u} \right)$$

Where,

k is the learning percentage

u is the number of systems

B'_{pt} is the predicted buffer size needed to produce first u th systems. The adjusted sequence buffer size.

B^*_{pt} is the current buffer size needed

3) Compute each milestone coefficient of variation CoV_{ijt-1}

A milestone's CoV_{ij} depicts the absolute variability present from the media of duration in an operation's actual cycle time A_{ij} . The CoV shows the relation σ/μ .

$$CoV_{ijt-1} = \frac{\sigma_{ijt-1}}{\mu_{ijt-1}}$$

Thus, the higher the CoV, the higher the variability in the duration of disturbances. In this regard, a milestone presenting a coefficient of variation lower than 0.05 says that the cycle time reported is "almost always" as the planned one without disturbances, X_{ijt} . Therefore, although it was recommended to estimate a time buffer in each milestone, whenever the $CoV_{ijt-1} < 0.05$, the corresponding buffer in next period, B_{ijt} , should be directly zero.

4) Estimate the buffer size for milestones holding a $CoV_{ijt-1} > 0.05$

As in the Regression-based method, we will regard B'_{pt} as the optimal amount of buffer to be spread within the milestones comprising the total sequence from product p . Furthermore, being aware that the variability accounted for each milestone in the sequence differs, this time buffer spread will not be even but the priority weight wpa_{ijt} will serve to define the preference a milestone has in the assignation of time buffers among the other milestones. The calculation of this weight is based on the proportion of buffer needed in each milestone compared to the sum up of all time buffers needed for all milestones as if the analytic approach were followed. Therefore, as if each milestone were by itself aimed to achieve the target service level defined

for the complete sequence. In this regard, it should be reminded that due to the compensation effect explained earlier in this chapter, it is actually needless the definition of service levels within the sequence. Thus, this buffer needed will be used solely to determine the proportion of buffer each milestone needs according to its variability contribution to the sequence, and wherein its duration and distribution are accounted for.

How to compute wpa_{ijt} ?

Assuming the G distribution of A_{ijt-1} is known. Given B^*_{pt} and α_{pt} from 1), compute

L^*_{ijt} and B^*_{ijt} as follows.

$$L^*_{ijt} = G_{A_{ijt-1}}^{-1}(\alpha_{pt})$$

$$B^*_{ijt} = L^*_{ijt} - X_{ijt}$$

Thereon,

$$wpa_{ijt} = \frac{B^*_{ijt}}{\sum_{j=1}^m \sum_{i=1}^n B^*_{ijt}}$$

Where,

$$\sum_{j=1}^m \sum_{i=1}^n wpa_{ijt} = 1$$

Once all milestones wpa are defined, use the adjusted sequence buffer size, B'_{pt} , computed in 2) to estimate each milestone buffer size, B_{ijt} .

$$B_{ijt} = wpa_{ijt} (B'_{pt})$$

Thus, for this period ($t=0$), each milestone buffer size is:

$$\begin{array}{ll} B_{11} = wpa_{11} (B'_p) & \text{if } CoV_{11} > 0.05 \\ B_{12} = wpa_{12} (B'_p) & \text{if } CoV_{12} > 0.05 \\ \cdot & \cdot \\ \cdot & \cdot \\ B_{nm} = wpa_{nm} (B'_p) & \text{if } CoV_{nm} > 0.05 \end{array}$$

- 5) Compute the planned lead time for each milestone L_{ijt} . Thereon, find the planned lead time for the total sequence of product p, L_{pt} .

$$L_{ijt} = X_{ijt} + B_{ijt}$$

Thus,
$$L_{pt} = \sum_{j=1}^m \sum_{i=1}^n L_{ijt}$$

Method 3: Project view- based.

For this method a particular assumption is done: due dates to customers are loose. Therefore, the attainment of intermediate due dates can be regarded as less crucial, so as the estimation of time buffers for each milestones in the sequence of product p. In such situation, the buffer at the end becomes more beneficial and its estimation is suggested to be done based on the project scheduling literature (Van de Vonder, et. al., 2007). Therein, it is advised to set the sequence lead time 30% above the minimum duration schedule using the average activity duration, or in this study settings, the average milestone duration.

Computation of costs.

At the end of period t, the computation of cost resulting from the buffer strategy applied follows.

The costs immerged in this buffer strategy are basically coming from:

- 1) The additional organizational costs due to rescheduling or reallocating internal and external resources,
- 2) The tardiness cost representing the penalty cost for being delayed according to plan, and if any, the penalty cost associated to customers' dissatisfaction.
- 3) The earliness cost representing the penalty costs associated to planning longer lead times than the actual needed; thus, the penalty coming from planning resources and a budget for an event that never occurred.

All in all, costs can be computed from the actual cycle time reported in period t.

$$A_p = \sum_{j=1}^m \sum_{i=1}^n A_{ij} \quad \text{"Actual Cycle Time"}$$

Thereon, the expressions for the instability and tardiness and earliness costs follow:

- $SC(P_{pt}^R, P_{pt}^O)_{pt} = w_t * Ins\%$ "Instability/Mgt Cost"

$$Ins\% = \frac{(\sum_{o=1}^N \sum_{j=1}^m \sum_{i=1}^n |L_{ij} - A_{ij}|)}{N * L_{pt}} = \frac{\# Rescheduled days}{\#Planned days}$$

- $TC(P_{pt}^R, P_{pt}^O)_{pt} = \sum_{o=1}^N b_{pt} \cdot \max(A_{op} - L_{pt}, 0)$ "Tardiness Cost"
- $EC(P_{pt}^R, P_{pt}^O)_{pt} = \sum_{o=1}^N h_{pt} \cdot \max(L_{pt} - A_{op}, 0)$ "Earliness Cost"

Note: N stands as the number of actual cycle times under analysis.

Therein, the costs from the production plan in period t are measured by comparing the production plan coming from the planned lead time parameters P_{pt}^R , and the executed plan P_{pt}^O in period t. Moreover, w_t stands as the instability cost factor coming from the additional number of hours spent in planning during period t due to one percentage of instability in the original production plan.

Preferred method.

In this subsection three methods for the estimation of buffer sizes in serial unreliable and unbalanced systems were discussed. As can be recognized from above, choosing any of them will depend mainly on:

- 1) The availability of data a company holds,
- 2) The expected effect from learning on future cycle times,
- 3) The flexibility in the promised due date to customers, and
- 4) The cost that would be expected for next period. The latter resulting from the costs considered in each method.

Therefore, if due dates are not loose, no learning effects are predicted and disturbances were accurately recorded and tracked for each milestone, the high level of predictability coming from regression analysis would claim this method as the preferred one among the other two. However, in practice, 1) huge companies find difficult to keep track and make use of disturbances records due mainly to both, the large amount of organizational layers/filters found before this information can reach the analyst, and the high probability of finding this information unreliable if the company is not an automated system and disturbances are human-inputted. Furthermore, 2) companies are subject to the effects of learning even when manpower is not the main capacity resource, the latter is due to the fact that companies keep the improvement of processes as one of the main goals in the organization. Therefore, being aware that in practice disturbances' records are either unavailable or unreliable, and the effects of learning can detriment the regression model level of predictability, method 2 and 3 were also proposed. Where using any of the latter depends on the looseness of due dates and the expected effect of learning in a period. In this regard, method 2 would be the preferred one whenever the internal lead time reliability is crucial and the effect of learning by doing affects the planning of next periods lead times. As a consequence, method 3 would be used solely in those cases when due dates are loose and the effects of instability and learning do not influence the planning of lead times in next period.

CHAPTER 5: Case study. ASML Manufacturing FASY & Test.

This chapter is aimed to present the results gotten from the application of the buffer strategy described in Chapter 4 into a real manufacturing setting. Particularly, the case of ASML Manufacturing FASY - Test was studied. Although ASML's manufacturing settings have been introduced in Chapter 1 and specified in Chapter 3, this chapter will start in Section 5.1 with a recapitulation of ASML characteristics. Therein, the particularities of ASML are stated along with the parameters and performance of planning as of February the 1st, when this project was initiated. Section 5.2 presents the results from taking the buffer strategy described in Section 4.4 into practice. Thereafter, Section 5.3 evaluates the performance of this buffer strategy when comparing it to the current situation. Thereon, based on the reliability concluded for this buffer strategy, Section 5.4 presents the results from the analysis of different scenarios by means of this buffer strategy.

5.1. Recalling ASML characteristics.

As stated before, the purpose of this section is the recapitulation of ASML manufacturing settings jointly with the planning parameters and performance as of February the 1st, when this case study started.

5.1.1. ASML manufacturing settings.

Despite the fact that the characteristics presented in this subsection are ASML specific, for robustness purposes, they will be enlisted in a generalized way as in Chapter 4. The reader should refer to Appendix F for a more detail explanation of each.

- 1) Exposed to operators' and organization's learning curves effect.
- 2) Characterized by the continuous introduction of new technologies (R&D-oriented), e.g. high tech systems, capital goods, etc.
- 3) Working under periodic lead times.
- 4) Characterized by a sequence comprised by m serial stages where predefined n milestones are found.
- 5) Working under a fixed "tacted" scheme.
- 6) Executing "as soon as possible".
- 7) Can be distinguished by their capital intensive, low- volume high-risk production.
- 8) The effects of rescheduling are spread all over manufacturing plans. (See Section 1.4)

5.1.2. Current parameters and performance in ASML planning.

For uniformity purposes and aligned to ASML reporting, throughout the remainder of this thesis, the time unit in usage will be days. Keeping the latter in mind, as of February the 1st, 36 days stand as the planned lead time for the XT860 systems. Therein, 13.81 days represent the average processing time and 22.62 days the average time buffer. As for the NXT19X0 system, 121 days is the average total lead

time, wherein 60.32 days represent the average processing time and 60.32 days the average time buffer. In addition, two remarkable points come out from the current planning in ASML:

- 1) For XT 860 FASY, the planned time buffer as of February 1st was considered solely at the end; thus, neglecting the instability coming from rescheduling milestones in that stage.
- 2) For NXT 1950 FASY, two time buffers are considered, one after Build and the second at the end of this stage.

Moreover, an important note at this point refers to the amount of data gathered for this study along with the delivery performance observed from the number of systems delivered as planned in a month. Thus, for further performance analysis purpose, the delivery performance of one month was computed and is depicted in Table 5.1.

	XT860	NXT1950
Data collected		
From seq. nr. ⁹	1183	1109
To seq. nr.	1264	1209
Data size	34 orders 4 months	34 orders 6 months
Performance (in 1 month; t.s.l 75%)		
Data evaluated	1246, 1249, 1250, 1253, 1258, 1259, 1262, 1264.	1193, 1194, 1195, 1199, 1205, 1209.
Cum. days delayed	30.38	63.44
FASY-Test Delivery performance	38%	50%

Table 5.1 Data figures and delivery performance.

5.2. The buffer strategy in ASML FASY and Test.

The buffer strategy presented in Chapter 4 was applied to ASML manufacturing settings. Please refer to Appendix G for a detail explanation and depiction of each step in Section 4.4. Therein, results showed that for a target service level of 75% the total lead for the XT8X0H sequence should be 44 days and for

⁹ Seq. nr in this table refers to the sequenced four digits number used for internal communication in ASML. This number, when combined with a 4 digits random number, gives a system's order its uniqueness.

the NXT1950, 153 days. Moreover, it is also shown that 30 and 93 days of time buffer should be used to the XT8X0H and NXT1950 sequence, respectively.

5.3. Performance analysis.

In this section we will study the performance of this buffer strategy. For comparison purposes, results from the current planning parameters and methodology are shown followed by the results gotten from the application of this buffer strategy in the prediction of u (as defined in Chapter 4) systems. Be aware this assessment requires u sample to be the same in both methods.

Being the reliability of production plans the main objective for the setting of time buffers in ASML FASY and Test, it will be regarded as the key performance indicator in this section. The latter is due to the fact that, in planning, success is defined by the number of orders delivered as planned as a consequence of determining reliable lead times; and thus, reliable due dates to internal and external customers.

Below the case of NXT 1950 will be addressed and followed by the XT860 case. Remind the targeted service level, in both cases and for both type of systems, is 0.75.

NXT 1950

Before getting further into these methods comparison, be aware the following sequence numbers were expected to be predicted by the respective planning parameters in each method: 1193, 1194, 1195, 1199, 1205 and 1209. Furthermore, remind the objective of the buffer strategy described in Chapter 4 is to determine planning parameters that can predict more accurately than the ones currently used towards the attainment of a 75% delivery performance.

Current parameters results

Applying the current NXT 1950 planning parameters on the execution of those 6 consecutive systems, a 50% delivery performance and a 55.1% of production plan instability came out as a result. The latter means that from those 6 systems released in a month, by using the current planning parameters just 3 systems were in time; thus, their actual cycle time was less than the planned 120,64 days.

	MS1	MS2	FASY	MS3	MS4	MS5	MS6	MS7
Delivery Performance	0,33	0,50	0,17	0,83	1,00	0,67	0,50	0,50
Lead time	11,02	9,86	20,88	7,54	9,86	11,02	4,64	5,80
Time Buffer	5,22	4,64	9,86	4,64	5,22	6,96	1,74	2,90

	MS8	Upgrade	MS9	MS10	MS11	CODP	MS12	Test	TOT
Delivery Performance	0,50	0,17	0,67	1,00	0,50	0,83	0,17	0,50	0,50
Lead time	5,22	6,96	7,54	7,54	5,80	13,92	13,92	99,76	120,64
Time Buffer	0,58	6,96	2,90	2,90	1,16	6,96	7,54	50,46	60,32

Buffer strategy results

Applying the buffer strategy's NXT 1950 planning parameters on the execution of those same 6 consecutive systems, a 100% delivery performance and a 44.1% of production plan instability came out as a result. The 100% states 6 out of 6 systems were in time; thus, their actual cycle times were less than the planned 153.53 days.

	Prepare	Building	System	Init	FASY	MS3	MS4	MS5	MS6	MS7
Delivery Performance	0,67	0,50	1,00	0,67	1,00	0,83	1,00	0,83	0,67	0,33
Lead time	0,82	11,68	10,26	6,18	28,94	11,83	12,04	15,85	7,37	4,97
Time Buffer	-0,34	7,04	7,36	3,86	17,92	8,93	7,40	11,79	4,47	2,07

	MS8	Upgrade	MS9	MS10	MS11	CODP	MS12	Test	TOT
Delivery Performance	0,67	0,50	0,67	1,00	0,50	0,67	0,83	1,00	1,00
Lead time	6,33	12,90	6,60	6,08	6,56	9,79	24,27	124,59	153,53
Time Buffer	1,69	12,90	1,96	1,44	1,92	2,83	17,89	75,29	93,21

In summary, the application of this buffer strategy advises the usage of a longer lead time that can cope better with 1) attaining the predefined target service level, and with 2) enhancing the reliability of internal lead times. In doing so, provides a better performance in comparison to the poor 50% achieved with current parameters. Moreover, this buffer strategy brings a more stable production plan by extending the number of planned days and minimizing the additional hours/ week production planners spend in rescheduling and reallocating resources all over manufacturing.

XT 860

So as in NXT1950, be aware the following seq. nrs. were used for the XT860 performance analysis: 1246, 1249, 1250, 1253, 1258, 1259, 1262, and 1264.

Current parameters results

By applying the current XT860 planning parameters on the execution of the above 8 consecutive systems, a 38% delivery performance and a 40.5% of production plan instability came out as a result. The 38% represents the fact that just 3 out of the 8 systems considered in this study were executed in less than the planned 36.52 days.

	Prepare	Build	System	Init	FASY	MS3	MS4	MS5	MS6	MS7	ATP	Test	TOT
Delivery Performance	0,75	0,00	0,00	0,00	0,50	0,75	0,88	0,50	0,38	0,75	0,56	0,38	0,38
Lead time	0,58	3,50	1,75	1,75	11,06	4,29	3,30	4,29	4,95	3,30	5,33	25,46	36,52
Time Buffer	0,00	0,00	0,00	0,00	3,48	2,96	2,30	2,96	3,28	2,30	5,33	13,80	22,60

Buffer strategy results

On the other hand, when applying the buffer strategy's planning parameters on the execution of the 8 consecutive XT860 systems, a 75% delivery performance and a 37% of production plan instability came out as a result. In this regard, the 75% of delivery performance indicates that 6 out of the 8 systems released in that month were executed in less than the planned 44.08 days.

	Prepare	Build	System	Init	FASY	MS3	MS4	MS5	MS6	MS7	ATP	Test	TOT
Delivery Performance	0,75	1,00	0,88	0,63	0,75	0,50	1,00	1,00	0,38	0,75	0,75	0,88	0,75
Lead time	0,58	4,99	3,10	3,77	12,44	3,99	3,09	5,86	5,90	4,10	8,71	31,65	44,08
Time Buffer	0,00	1,49	1,35	2,02	4,85	2,66	2,09	4,52	4,23	3,10	8,71	25,31	30,17

In summary, as in NXT 1950 case, the application of this buffer strategy advises two things: 1) the usage of a longer lead time for attaining the predefined 0.75 target service level and 2) the setting of buffers at each milestone instead of merging milestone buffers in FASY. In doing so, provides almost 40% of better delivery performance than the one achieved with current parameters. Moreover, this buffer strategy brings a more stable production plan by extending the number of planned days and minimizing the additional hours/ week production planners spend in rescheduling and reallocating resources all over manufacturing.

Cost analysis

Attaining performance indicators is generally associated to planning, manufacturing, capacity, etc., costs. In this regard, working towards achieving a predefined 75% service level in ASML manufacturing FASY – Test, requires the awareness of the following costs:

Costs involved			
<i>Production cost</i>	NXT 1950	XT 860	
Cabin depreciation	€ 17.000	€ 11.800	Eur/week
Cabin cost	€ 2.429	€ 1.686	Eur/day/system
WACC	0,11	0,11	%/year
	0,00030137	0,00030137	%/day
Carrying cost	€ 20.000.000	€ 6.500.000	Eur/system
Cost of capital	€ 6.027	€ 1.959	Eur/day/system
Salary	€ 54	€ 54	Eur/hr
Test working hrs	16	24	hrs/day/system
Test/Init workforce	2	2	people/system
People Test	€ 1.728	€ 2.592	Eur/day/system
Production costs	€ 10.184	€ 6.237	Eur/day/system
<i>Instability costs</i>	NXT 1950	XT 860	
Additional hrs for MR=			
6	1,2948	1,2948	hrs/wk/%
Planning costs	€ 54	€ 54	Eur/hr

Thereon, for addressing the associated costs in this buffer strategy, the identification of the earliness, tardiness and instability costs was required. In this regard, while the instability cost was based on current CRP planning factors; the tardiness and earliness costs, as known in literature, were vague when taken them into ASML manufacturing settings. This lack of clarity in costs can be explained from a broad sense by the following:

- 1) ASML can be regarded as the preferred one among competitors. Thus, if tardy, the order is not lost and the customer keeps the purchasing commitment on.
- 2) Since just one customer (INTEL) occasionally penalizes ASML for being delayed, customer-related penalization should be neglected.
- 3) Earliness costs are hardly distinguishable due to the “as soon as possible” framework explained earlier in this thesis. The latter is due to the fact that once a system is foreseen to

be completed earlier, resources and orders are rescheduled in such a way that the earliness costs coming from idleness can be avoided.

- 4) In case an order is finished earlier than the promised date to a customer, the system is never kept as stock, so no capital or resources on hold can be accounted for as earliness cost. The latter is due to both: 1) usually, customers want their orders as soon as possible; 2) for those few cases in which customers are not ready to receive their order, the latter is reassigned and sent to an urgent client.

Although these costs assumptions were explained by regarding “customer’ as the external one, for this thesis scope purpose (FASY and Test), these principles can be extended for the definition of tardiness and earliness costs when regarding “customer” as the internal customer (Prepack). Therefore, due to the ambiguity in considering these costs, further calculations and scenarios’ description in this master thesis will be supported by assuming the following definitions for Tardiness and Earliness costs in ASML manufacturing:

Tardiness Costs: the total production cost per each day delayed. This cost including the cabin cost/day + people cost/day + cost of capital/day. Production cost can be regarded as a penalty cost since it represents an extra cost from the original budget you forecasted for the former production plan.

Earliness Costs: The interest rate lost or opportunity cost from not investing in a risk free asset, and instead, attaching this financial resource to your planning budget for an expected WIP that never occurred.

Thereon, the tardiness cost per day delayed is €10,184 for the NXT 1950 system and €6,237 for the XT 860 system. The earliness cost will be computed by assuming an interest rate of 5% monthly. Therefore, being aware the carrying cost for the NXT1950 is €6,027 and for the XT 860 is €1,959, the earliness cost per day is €381 and €98, respectively.

Moreover, the instability cost is:

$$0.2158 \text{ hrs/week/\%} * (\text{Move Rate}) * \% \text{ instability} * \text{planning cost/hr} * \# \text{ weeks in horizon}$$

Therein, 0.2158 stands as the factor taken from CRP planning which represents the additional amount of hours per week production planning spend in re-planning due to one percentage of change in the production plan when the move rate is one.

Once all costs are defined, the costs resulting from this buffer strategy can be compared to the cost resulting from the usage of the current planning parameters. Below the NXT 1950 and XT 860 results are depicted and are followed by a brief cost assessment.

NXT 1950

Current parameters results

Rescheduled days	399.08
Planned days	723.84
Instability %	0.551
hrs/wk additional	71.39
hrs/wks in plan	356.93
Instability cost	€ 19,274
Days tardy	63.44
Tardiness cost	€ 646,071
Days early	28.67
Earliness cost	€ 8,640
Total Cost	€ 673,986

Buffer strategy results

Rescheduled days	406.64
Planned days	921.15
Instability %	0.441
hrs/wk additional	57.16
hrs/wks in plan	285.79
Instability cost	€ 15,433
Days tardy	0.00
Tardiness cost	€ 0
Days early	163.32
Earliness cost	€ 49,220
Total Cost	€ 64,653

XT860

Current parameters results

Rescheduled days	118.26
Planned days	292.19
Instability %	0.405
hrs/wk additional	52.41
hrs/wks in plan	262.03
Instability cost	€ 14,150
Days tardy	30.38
Tardiness cost	€ 189,489
Days early	16.57
Earliness cost	€ 1,623
Total Cost up	€ 205,262

Buffer strategy results

Rescheduled days	129.44
Planned days	352.68
Instability %	0.367
hrs/wk additional	47.52
hrs/wks in plan	237.61
Instability cost	€ 12,831
Days tardy	5.58
Tardiness cost	€ 34,804
Days early	52.26
Earliness cost	€ 5,118
Total Cost up	€ 52,754

In both systems this buffer strategy brought better quantitative results than those coming from the current planning parameters. The latter is due to the fact that by planning longer lead times, this buffer strategy enhances the possibility of reaching the predefined service level of 0.75 while the tardiness costs are kept as low as possible and the instability in the production plans improves. In addition, the low penalty cost associated to be early in the “as soon as possible” framework in which ASML works, ends up supporting the idea of planning longer and more reliable internal lead times.

In summary, for a target service level of 75%, by estimating a 68% of buffer (or 2.16 times the average processing time) instead of the current 62% (or 1.62 times the average processing time) in the lead time planning of the XT860 system, the target service level is met and the overall costs is improved in about 75%. Thus, adding 7 days of buffer to the current planning parameters is less costly and enables the

attainment of a 75% target service level. As for the case of the NXT 1950, by estimating a 61% of buffer (or 1.5 times the average processing time) instead of the current 50% (or 1 time the average processing time) in the lead time planning of the NXT1950 system, the target service level is met and the overall cost is improved in about 90%. Thus, under a targeted 75% of service level, adding 30 days of buffer to the current planning parameters is less costly and enables the attainment of the targeted service level.

Until now it has been proved that the buffer strategy proposed in this master thesis outperforms, in cost and service delivery, the current parameters used in ASML manufacturing. The latter has been concluded by validating this strategy with real sample data from one month period. In this regard, from Figure 5.1 it can be stated that this conclusion holds for the whole spectrum of possible different cycle time values to occur within a period. Particularly, Figure 5.1a shows that attaining a 75% of service level requires 44 days as the planned lead time for XT 8X0 and 154 days for the NXT 1950. Otherwise, by using the current lead times of 36 and 120 days, the expected service level is less than 21% and 22%, for the XT 8x0 and NXT 1950 systems, respectively. Furthermore, Figure 5.1b shows that by using this buffer strategy, a 78% of cost reduction can be expected from the planning of the XT 8x0, and 84 % for the planning of the NXT 1950 system.

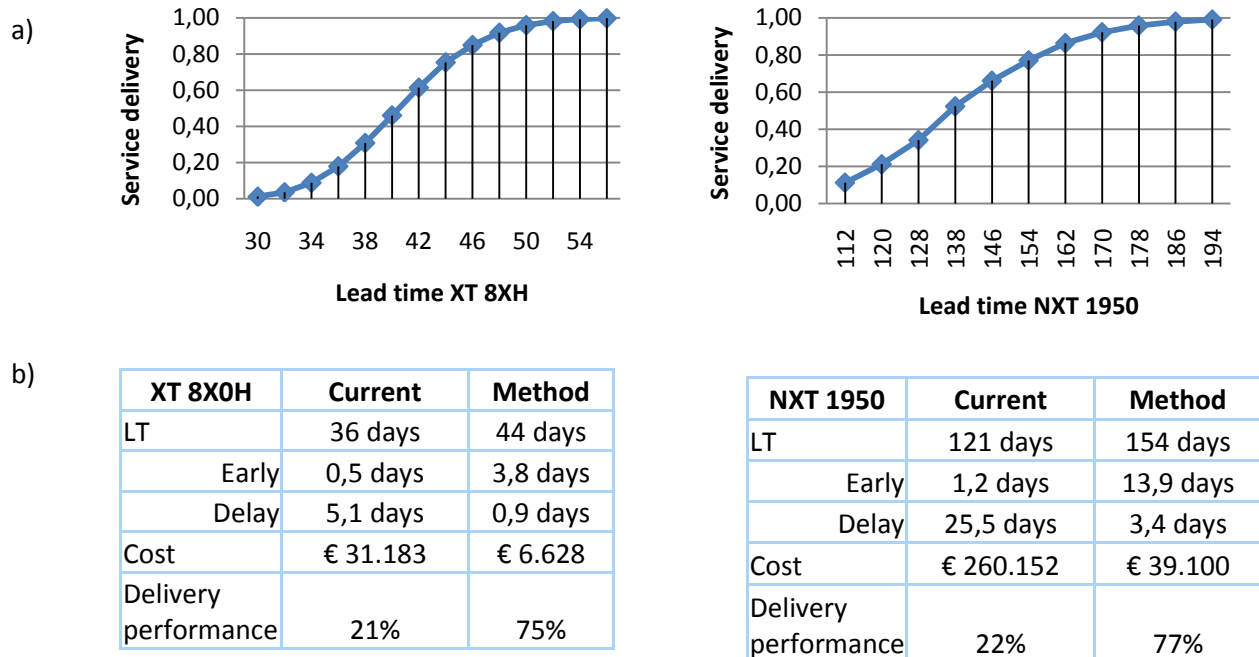


Figure 5.1 Performance: Current vs. Buffer strategy parameters.

5.4. Scenario analysis.

Once the performance of the buffer strategy proposed in Chapter 4 has been validated with real data, this section provides a brief summary for the analysis of different scenarios to which our sample data was subject to. Therein, input parameters such as service level, move rate, interest rate, learning percentage, orders to predict, etc. were modified, refer to Appendix H for a more detail explanation.

The first scenario considered the idea of changing the target service level in the planning of both systems' lead times. Results showed that for the case of NXT 1950, planning a lead time under a targeted service level of 0.65 results to be the least costly. The latter is due to the fact that by setting this t.s.l., a makespan of 145 days enables planning to fulfill all orders in time, the tardiness cost is avoided and the instability and earliness costs are kept low. In this regard, the suggestion for XT8X0H is kept as the one recommended in literature, where a 0.98 target service level appears to be a cost efficient target brings low earliness, tardiness and instability costs. Thereafter, the second scenario considered the idea of changing the move rate was analyzed and it was concluded that whenever the move rate rises above 6, earliness should be penalized higher due to the influence it has on further managerial decisions such as the building of new facilities. Third scenario studied the impact a change in the interest rate has on the cost efficient service level for both systems. Results from this scenario showed that the interest rate considered does not influence the service level recommended. Thereafter, next scenario considered the effect of a change in the learning percentage. Results showed that the more learning percentage, the more standard a product is, and thus, the more orders can be predicted without losing level of accuracy. Finally, last scenario addressed the effect the number of orders to predict (u) has on the involved costs. Results showed that without mattering the product's level of maturity, it is always better to overestimate, rather than subestimate, this input parameter.

CHAPTER 6: Implementation concerns.

This chapter is aimed to provide recommendations for the implementation of this buffer strategy. Firstly, Section 6.1 discusses the reliability of data sources and presents a methodology for identifying outliers and the distribution that best fits to our data. Once methods for data collection and examination are advised, Section 6.2 provides a methodology for determining the periodicity for reviewing MRP parameters and the sample size required on analysis. Thereafter, Section 6.3 describes how to determine the learning percentage and the number of orders to be predicted for next period. At this point all decisions concerning data analysis and estimation of input parameters were advised, and still a section for addressing the organizational concerns is needed. Therefore, Section 6.4 is aimed to give recommendations for a successful implementation of this buffer strategy in ASML Manufacturing.

6.1. Data collection and analysis

For ASML implementation purposes, this section gives advice about: 1) the data sources to use, 2) the methodology for detecting outliers and, 3) the procedure for determining data distribution.

6.1.1. The data sources

Several data sources stand in ASML for reporting CTs¹⁰; particularly, the OBIIE database and the progress tracking excel files stand as the most important data sources. In this regard, due to the input gotten from several interviews in the data collection phase of this project and the several mismatches found in OBIIE data with the real cycle times; it was concluded that for now and until OBIIE CT recordings hold exactly the same information as in the manually-inputted excel files, the excel files can be regarded as the most reliable source of data for this buffer strategy usage. In this regard, the later recommendation is kept on for the short-term implementation phase of this buffer strategy. Appendix J provides a summary for the recommended data sources for both systems together with the file name, owner and main users in ASML manufacturing FASY and Test.

6.1.2. Identification of outliers.

Once the sample size N has been identified and the N actual cycle times have been extracted from the advised data source, outliers must be detected and removed to assure the robustness of the used estimators.

¹⁰ Refer to Appendix I for a detailed description and assessment of ASML data sources.

In ASML settings, univariate outliers will be regarded as those cases in which an unusual CT was reported at milestones level OR sequence level. In this regard, each milestone CT record should be analyzed independently from its respective total CT (hence, sequence CT). For instance, a CT record in System could be considered as an outlier for the computation of System's statistics without having to be considered as an outlier for the total sequence. The same works the other way around; detecting an outlier in an actual CT from the total sequence does not mean all respective milestones' are outliers.

The detection of outliers in this study was and is advised to be based on the "rule of thumb" taught in the "Research Design and Data Collection", a TU/e master statistic course with code 1ZM30. Therein, it was stated that for a sample size smaller than 80 cases (hence, $N < 80$), an outlier will be identified if a case standard score, z , is ± 2.5 or beyond. A brief example taken from the NXT 1950-MS5 case is given below in Appendix L.

6.1.3. Distribution Fitting

Once the collected data has been filtered from misleading outliers, it is possible to find the distribution that best describes the frequency of possible CTs in a period. For doing so, two options are discussed here: option 1: graph the respective histogram and determine the distribution that best fits to it; or, option 2: make use of distribution fitting softwares. Option 1, although good, has several problems: 1) distributions that are almost the same can look different depending on the number of bins used in the histogram, 2) small variations in CT are magnified, 3) is error sensitive, and 4) is time consuming. On the contrary, option 2 allows to automatically fit a large number of distributions, reduces the time spend on analysis, and ensures high quality in results. Therefore, option 2 was chosen for finding the best distribution fit to our CT data. Particularly, the EasyFit software, which can be used with Microsoft Excel, was employed. In doing so, still two particular decisions are advised to be made in order to narrow the number of distributions for making a final choice. Particularly, the first concern is to determine the data domain to which our data pertains. Thus, it is necessary to determine whether our data is continuous or discrete. In this regard, it was decided to choose continuous distributions, since they frequently provide much better fit than the discrete ones. Thereon, the second decision made for narrowing the whole spectrum of distributions was based on the additional information known about our data. For instance, since our data represents CT recordings, due to the nature of the latter, it would not have made sense to fit distributions which can take on negative values (such as the Normal distribution) to our data set. Therefore, after taking out all discrete distributions and allowing just nonnegative distributions to be analyzed, the Erlang, Exponential, and Gamma distributions were the most representative and showed the best fit to our data set. However, since the two formers are a special type of Gamma distribution, this latter was regarded in this project as the unique distribution assumed in our calculations.

6.2. The periodicity for reviewing planning parameters and sample size N.

As mentioned earlier in this report, ASML works under a deterministic MRP framework where the lead time parameter is set and reviewed quarterly and conjointly by several departments in ASML Manufacturing. Therein, the CT behavior in each system is discussed and the new MRP parameters are settled for the upcoming production period. According to Buzacott (1994), the appropriate values of these parameters are influenced by the forecasts nervousness, the variability of the processing times, and the costs of inventory and shortages. Being aware all latter fluctuate over time according to product's maturity and organizational learning effects; it is important to match those fluctuations with the periodicity of resetting MRP parameters. In doing so, it is recommended to analyze the systems historical data and observe the frequency of meaningful changes in the mean cycle time reports over time. In this regard, it is suggested the use of polynomial models for getting both, the adequate number of observations for the estimation of buffer sizes in period t , and the frequency for reviewing these parameters in MRP. Therefore, by plotting the relationship between a dynamic cumulative average of size N and its respective average cycle time from a data set elapsing (n) months, the periodicity will be established from the order level (m) in the polynomial model; thereon, the sample size to use is gotten from the number of cycle time averages that ensure a $R\text{-square} = 1$ in the model. In summary, take records from n months, determine the order level m from the polynomial model, and compute the periodicity as $p=n/m$ months. Moreover, it should be remarked that even if the product level of maturity and learning percentage would claim for a frequent review, organizational and procedural constraints would make inappropriate to review these parameters too often in the system. These constraints referred basically to work preparation complexities and the effect this review has in the communication and coordination needed within internal and external supply chain actors. Therefore, it is advised to determine a polynomial model with $m \leq n$. Furthermore, for being able to observe a trend over time, n must be greater than the average lead time of that particular system. A general example for this suggested method and an ASML application to the XT860 system is provided in Appendix K. Finally, a recommendation for reviewing this periodicity assessment is given below.

Review periodicity:

- 1) Whenever the sequence has a meaningful change.
Consider the case of a product moving its customization to the field instead of in the factory.
- 2) Whenever the learning percentage stabilizes in 1.
Consider the case of a product becoming standard.
- 3) Whenever organizational changes would affect severely CT fluctuations.
Consider the case of changing from fixed to dynamic takt framework.
Consider the case of outsourcing processes.
Consider the case of changing contractual agreements with supply chain partners.

6.3. Determination of input parameters

Implementing this buffer strategy requires the awareness of how to estimate input parameters other than those coming from the actual CTs statistics. Particularly, this section provides a recommendation for a way to determine learning percentages, k , and the number of orders to predict for next period, u .

6.3.1. How to determine the learning percentage (k)?

In the theory of learning it is well known that the repetition of the same operation results in less time and effort expended on that particular operation over time. In this project, the learning percentage is the input parameter used for calculating the learning curve effect from the repetition of procedures at execution. There are several ways to compute this number, some advised from theory and some from practice. In this regard, the learning percentage can be computed based on: 1) the observed cost reduction in manufacturing once the production quantity is doubled; 2) based on expert advice or rule of thumbs used in practice such as: aerospace 85%, shipbuilding 80-85%, repetitive electronics manufacturing 90%-95%, etc. and, 3) based on the observed reduction on time from last records. For this project purposes, due to its better level of accuracy and the already data available for analysis (instead of having to analyze costs separately) option 3 was chosen. A brief explanation for this procedure follows.

The learning percentage of a system can be gotten from analyzing the learning behavior of the actual CTs used for prediction. In doing so, it is advised to calculate the moving averages of CT following the same procedure as in Section 6.2., where the periodicity of reviewing norms was advised. Below the procedure to follow is described and is complemented by the example provided in Appendix M.

Start by computing the average from record # 1 to record N-1, then from record # 2 to N.

- a. If average 1 > average 2, decrease the number of records accounting in the average and now compute the average of N-2. This time 3 averages will be computed. If average 1 > average 2 > average 3; repeat the same procedure until the averages gotten do not decrease steadily¹¹ in time. Once this later occurs, go one step back to the last steadily decrease and divide the last average by the first average computed in this round. The later step provides the learning percentage to use for the estimation of next period's time buffers.
- b. If average 1 < average 2, this means no learning but instead the possible introduction of upgrades, process improvement, etc. resulted in a CT enlargement. In this regard, it is advised to use a learning percentage = 1. The latter comes from the minimal quotation approach described in Section 4.3.

¹¹ A steadily decrease in averages means there was a true reduction in cycle times throughout the production of those systems; reflecting the effect from learning over time.

6.3.2. How to determine the number of orders to predict (u)?

Previous sections gave recommendations regarding 1) the cost efficient learning-related number of predictions to be made in a period (refer to Appendix H.), and 2) the better off in cost coming from overestimating instead of underestimating the number of orders to predict for next period (refer to Appendix H). By keeping those two in mind, this section provides a way for determining the number of predictions to be made on a period.

The number of orders to be predicted can be determined either by observing releasing patterns from last periods or by looking into the planned releases for next period. For ASML specific, it is advised to determine the number of orders to predict based on the information hold in the production plan. The latter is due to the fact that orders in this company are planned lot much in advance and therefore, this information can be regarded as reliable. Therefore, the reader should be aware that the “number of planned releases in a month” for a specific system refers to the “number of orders to be predicted” in Chapter 4 and 5.

6.4. Organizational constraints.

As described in Chapter 3, the setting of lead times in ASML manufacturing FASY and Test requires the interaction of several dependencies in the organization. Particularly, Production Planning, Business Engineering, Manufacturing Engineering, FASY and Test, came up to be the main actors in this process. Due to the latter, before going into the implementation of this buffer strategy, the awareness of certain organizational constraints that can detriment the quality in results is needed. Such constraints standing mainly for:

- 1) The unclear definition of roles.
- 2) The unclearness of customer for some actors.
- 3) The unclear definition of terms.
- 4) The different reporting sources.
- 5) The diverse interests in place.
- 6) The low process knowledge.

Due to the latter, the implementation of this buffer strategy in ASML Manufacturing FASY and Test would firstly claim for the resolution of the enlisted ones. Furthermore, the problems stated above are based on the perception gotten from the interviews conducted along this project; therefore, the presence of some additional constraints might also be considered. In this regard, it would be advised to use the Nominal Group Technique and the Interactive Structural Modeling processes developed by J.F. Warfield to identify and give solution to this problematique situation. The methodologies proposed here were developed in Systems theory for designing and improving complex organizational systems. In doing so, the actively participation of stakeholders along several sessions would be required. Due to a time constraint in this project, bringing these methodologies into practice is unfeasible and furthermore, out of this project scope.

Therefore, the purpose of this section is solely to discuss these organization constraints and provide a recommendation for the resolution of those from which a good insight was gotten throughout this project.

From constraints enlisted above, it should be remarked the enhanced importance constraint 5) has among all others. Particularly, solving constraint 3) requires firstly the resolution of constraint 5). Constraint 3) claims for the urgent definition of terms in ASML manufacturing. In this regard, throughout several interviews it was notable how unclear for some stakeholders the duration of some milestones in Test is. Therefore, the sooner the interests' bargaining between divisions comes to an agreement, the sooner the definition of terms can be settled. In line to the latter, the clearer the definitions for all stakeholders are, the more involvement can be expected from them; and consequently, the better the implementation of this strategy can be.

Regarding constraint 4), since in the short term the OBIIE database is expected to be the only source of data for CT reporting in BE, no recommendations will be given, and instead, from now on it will be regarded as the unique source for importing CT records.

Finally, a recommendation based on the Knowledge Process Management theory is given here for the jointly resolution of constraints 1), 2) and 4). In this regard, the mapping of processes is suggested as an effective technique for sharing knowledge in the organization. Therein, the main responsibilities, customers and the process itself should be depictive enough for enabling not just the good performance of stakeholders but, the easy understanding of this process at all organizational levels. (See Appendix N)

CONCLUSIONS AND FURTHER RECOMMENDATIONS

This master thesis was focused on designing a buffer strategy for the estimation of reliable lead times in the planning of ASML Manufacturing FASY and Test. In doing so, three methods were discussed in Chapter 4 for the setting of buffers in serial unreliable and unbalanced capital intensive production lines subject to a predefined service level and executed under an “as soon as possible” framework. Particularly, the Regression-based, Distribution-based, and Project view-based methods were described. In this regard, the Distribution-based method was the most suitable to ASML manufacturing settings due to its higher level of predictability coming from the recognition of learning curve effects in its estimations. Chapter 5 provided the results gotten from the application of this method, therein, it was concluded that for the current target of 75% service level, using 68% and 61% of time buffers in the planned lead times of the XT860 and NXT1950, respectively; the service level was met at a lower cost than by using the current planning parameters in ASML which considered 62% and 50 %, accordingly. Furthermore, regarding costs, it was concluded that by using this buffer strategy planning related costs are expected to be reduced in more than 50% for both systems in scope. Several insights were gotten from the application of the buffer strategy in Chapter 5 and the implementation suggestions stated in Chapter 6. All in all, the following conclusions can be drawn from this master thesis project:

Conclusion 1: About the allocation of buffers in ASML sequence.

- Setting time buffers in milestones is less costly than doing so at stages or leaving all at the end. The latter is due to the lowering costs coming from rescheduling and the reduction of tardiness due to the accessibility of more stable internal and external production plans.
- The more reliable the estimation of internal due dates is required, the more reliable the estimation of milestones’ lead times should be. Therefore, time buffers at milestones enhance the overall system’s reliability.

Conclusion 2: About the makespan, service level, and interest rate.

- The higher the service level, the higher the makespan and the higher the earliness and instability costs immersed in variable systems. Therefore, increasing service level comes to be expensive for variable/NPI systems.
- The interest rate considered in the earliness penalty cost does not influence the cost efficient service level recommendation. Furthermore, the higher the interest rate and the higher the service level, the higher the total cost. The latter is due to a longer makespan associated to a higher service level.

Conclusion 3: About the learning percentage, the number of orders to predict and the product maturity.

- The closer the learning percentage is to 1, the more standard a product is, and the higher the amount of orders that can be predicted without losing level of accuracy.
- Regardless the learning percentage and the product level of maturity; it is less costly to overestimate than subestimate the number of orders to be predicted for next period.

In Chapter 6 several recommendations were done for the further implementation of the time buffer strategy (TBS) proposed in this master thesis. Therein, the establishment of a unique and reliable data source and the enhancement of knowledge sharing among ASML dependencies, stand at the core of these recommendations. However, once this buffer strategy is implemented, several actions can be taken with the aim of improving cycle times duration, processes, and the overall performance of the Manufacturing organization. Particularly, insights from the application of TBS can serve for determining the target for moving towards if a reduction in CTs is the aim. Consider the case of observing a milestone holding a high standard deviation; therefore, if actions were to be taken for reducing sequence variability, this milestone would be regarded as the starting point to do so. Which actions to take? It would depend on the disturbances recorded for that specific milestone in that specific period. Concerning the latter, another recommendation for ASML would be to track carefully disturbances reported during execution, and for doing so, operators should be trained and taught about the importance and contribution this has on the better performance of the organization. All in all, the application of TBS can be concurrently carried out with ongoing projects towards the achievement of several goals. Despite the latter, the reader should be aware that TBS gives solution to the estimation of time buffers in FASY and Test and ignores the ASSY production unit, which is at the head of ASML manufacturing; thus, further research will be focused on the development of a methodology to coordinate the buffers in ASSY with the buffers in the subsequent production units, otherwise an overestimation of buffers would end up increasing the instability in production plans and the costs coming from being early. Moreover, although TBS estimates average lead times considering customization variability, TBS neglects the benefits from a company holding known/few customers. Thus, another path to explore deals with the development of a methodology for estimating buffers not general (as in TBS), not by order (as in a job shop), but by customer. Therein, the tradeoffs with increasing management costs should be assessed. Finally, since TBS is able to predict solely one period, further research can focus on the development of a multi-period method for the estimation of time buffers in unreliable, unbalanced and human-based production lines.

REFERENCES

- ASML internet site, *Company About ASML*, ASML Profile, <http://www.asml.com/asml/show.do?ctx=272&rid=362>. Last retrieved on 15.02.2011.
- ASML intranet site. Last retrieved on 15.02.2011.
- ASML, *100802 Timecard M&L v.3.ppt*, Last retrieved on 15.02.2011.
- ASML. (2010) *Four levels of buffer in taked system routings.ppt*, Last retrieved on 15.02.2011.
- Buzacott JA, Shanthikumar JG (1994) *Safety stock versus safety time in MRP controlled production systems*. Management Science 40: 1678–1689
- Elhafsi M., (2002). *Optimal leadtimes planning in serial production systems with earliness and tardiness costs*. IIE Transactions, 34, pp. 233-243
- Hnaïen & Ould Louly (2008). *Planned lead time optimization in MRP environment for multilevel production systems*. Journal of Systems Science and Systems Engineering,132-155.
- Molinder (1997). *Joint Optimization of lot-sizes, safety stocks and safety lead time in an MRP system*. International Journal of Production Research, 35: 4, 983 — 994
- Perez, B. (2011). *Buffer Management under environmental and systems uncertainty: Literature Study*, in Operations Management and Logistics, Eindhoven University of Technology.
- Van Aken, J.E., Berends, H., and van der Bij, H. (2005) *Problem solving in organizations: a methodological handbook for business students*, Lecture handout.
- Van de Vonder, Demeulemeester, and Herroelen (2007), *A classification of predictive-reactive project scheduling procedures*. Journal of scheduling. 10:3, 195-207.
- Yano, C.A. (1987a). *Setting planned leadtimes in serial production systems with tardiness costs*. Management Science, 33(1): 95-106.

APPENDIX A: ASML Industry framework.

Once the fabrication of semiconductors emerged as a viable business in the early 60s, the semiconductor industry came formally into place and has been characterized since then as a technology enabler which global revenue in 2010 reached 302 billion and is projected to climb steadily up to approximately 357.4 billion in 2014. However, last figures are the result of an upward trend coming just after the worst of the recession lived recently from an economic downturn. Although demand variations affect all supply chains in the semiconductor industry, their impact varies through stages so as the level of obsolescence and opportunity risks.

As known, the aim of any supply chain is to provide products to customers in the right time, in the right quantity, at the best possible condition and in the most cost-effective manner. However, contrary to more predictable industries such as the transportation and healthcare ones, for the semiconductor industry it is more difficult to keep a match between demand and supply due mostly to the lack of visibility across the supply chain partners, operation constraints, incapability to react to demand fluctuations, smaller product lifecycles, and the longer lead times in place. Due to the latter, companies pertaining to this industry recognize the crucial role played by demand planning, production planning and scheduling in attaining and retaining business competitiveness.

The supply chain in the semiconductor industry is extremely complex with several drivers affecting its planning processes. Specifically, these factors refer to a company business profile, type of product, environmental considerations, inter/intra company level of system integration & hardware, and level of trust and commitment in supply chain relations. In this regard and for this study purpose, the semiconductor equipment manufacturer factors analysis follows.

The semiconductor equipment manufacturers, being at the upstream stage of the semiconductor supply chain are the most sensitive to demand fluctuations, and thus, their high risk-low volume products are dependent on advanced planning for responding on time in full to customers.

APPENDIX B: Manufacturing & Logistics.

The “Build Operations” (BO) unit in ML is represented by Assembly (ASSY), Manufacturing Logistics, Production Planning (PP) and Final Assembly (FASY). The PP department is in charge of creating feasible production plans for all production units: ASSY, FASY and Test. Their planning is triggered by the Master Production Schedule, in where all machines planned to start to be built for the next 5 weeks are hold. Being ASSY planning out of this project scope and FASY part of the BO unit, FASY planning description follows. FASY planners make use of a file named “Start Progress Twinscan” to release planned orders weekly in SAP. Furthermore, based on the Planned Start date for FASY and the predefined lead time parameters, namely the planned processing time and safety time of a system, FASY planners update manually the “AMSL” (Advanced Machine Status List) and the “Start Progress Twinscan” files, to which everyone in PP has access for scheduling forward their respective orders by regarding the FASY Start date of an order either as the target for completion (in the case of ASSY planners), or as the basis for setting the planned start date of Test (in the case of Test planners). See Figure B for an overview of the CT and lead time definitions at ASML (Source: Timecard M&L v.3. ppt). Note that “cabin Cycle time” can be regarded as the baseline for planning the releasing of new orders in the “Start Progress Twinscan” file.

The “Delivery Operations” (DO) unit in ML is represented mainly by Test, Prepack, System Install Engineering, and Volume Install support; being the first one of our special interest. DO main function is to calibrate, qualify and install ASML’s products at customers’. The planning for Test is done forward based on the Planned Finish date of FASY, which consequently becomes the planned Start date for Test. A remark regarding the organizational structure at ASML is needed at this point, since although the PP department is allocated to BO, Test planners pertain to the DO unit and thus, to a different management sector.

The “Business Services” (BS) unit in ML is comprised by Means & Methods, Business Engineering, Business Reporting and Projects. Business Engineering (BE), being one of the main stakeholders in this study, is in charge of executing and improving control processes with the aim of optimizing the use of all production factors and the flow of materials through manufacturing. Based on machine’s cycle time, Business Engineering can determine the feasibility of expanding production volume along with the workforce required for it.

Finally, the “Manufacturing Engineering & NPI” (ME) is divided into NXE program, NXT program, litho+ program, NPI delivery, volume engineering, and People & knowledge. As a broad description, engineers in ME are responsible for creating a production blueprint, determining a production sequence, planning work centers, defining routing processes, doing norm analysis, and updating quarterly their sequence SAP parameter (CT and ST) used by PP and BE for their short and long term planning.

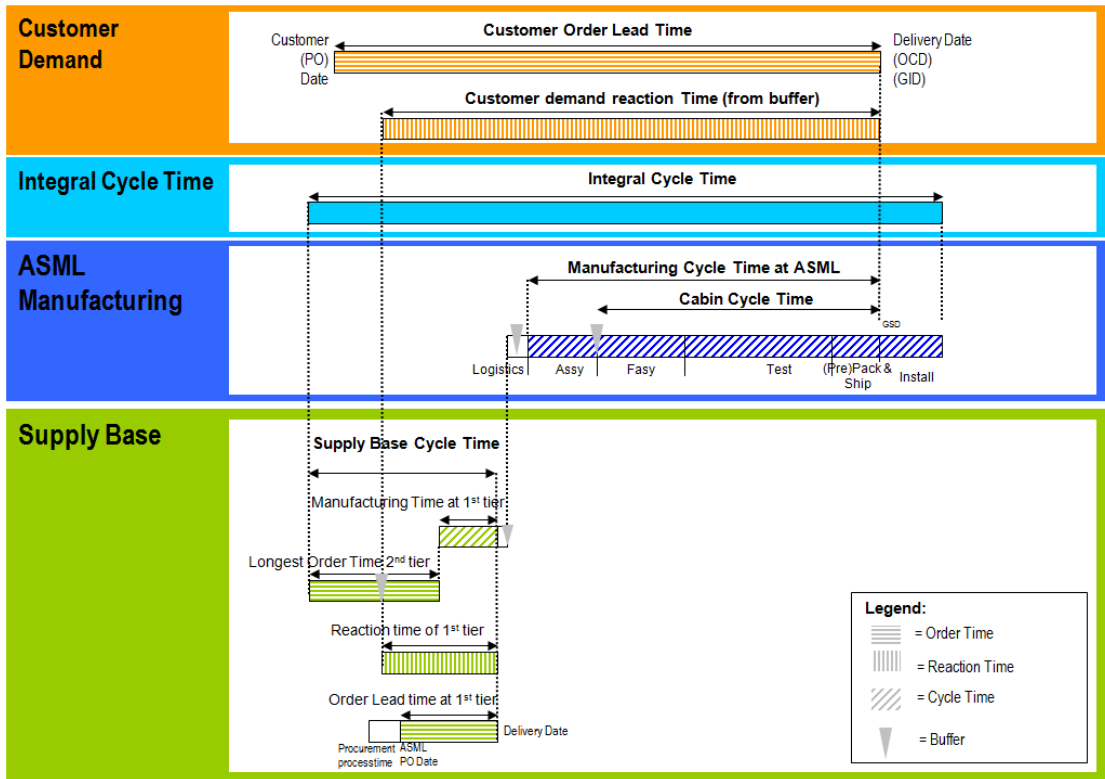
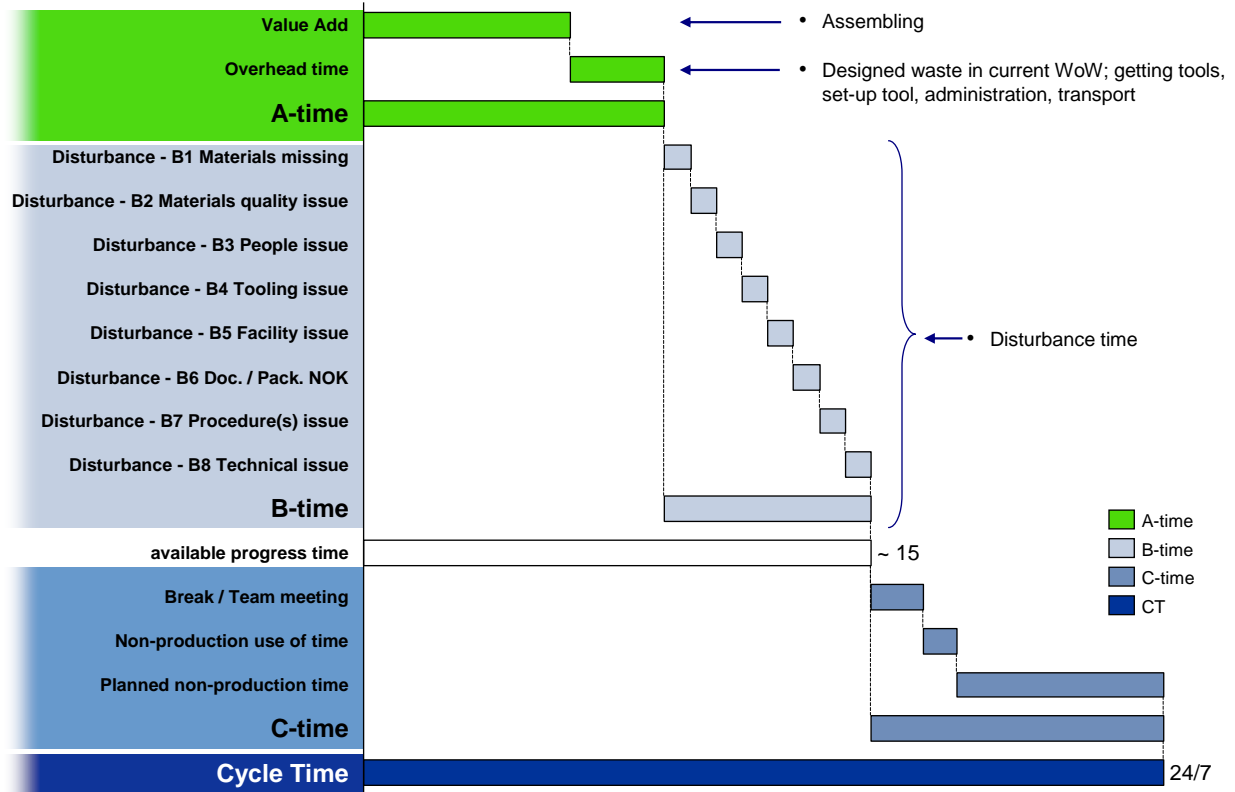


Figure B. CT and LT definitions at ASML (Source: Timecard M&L v.3.ppt)

APPENDIX C: Time categories.



APPENDIX D: Integral Manufacturing flow.

Work preparation

Before the planning of lead times is possible in ASML, the definition of the system's routing is necessary. In this regard, *Manufacturing Engineering* (ME) is responsible for creating a production blueprint, determining a production sequence, defining routing processes and doing norm analysis. In doing so, ME receive the input from *Business Engineering* (BE). BE performs systems' cycle time reports for the last three months; therein, the learning curve effects so as the feasibility of increasing the throughput by means of manpower capacity is assessed. Thereon, based on BE analysis, ME reviews the existing routings and decides whether the amount of workload within a system sequence is well spread, or should takts and milestones be redefined in the sequence. Furthermore, ME defines the work content and time buffer within takts and milestones. In this regard, while FASY and Test NXT sequence owners fill in takts with A,B and C time; Test XT sequence owner together with BE decided to fill in fully the takts in the volume product by disregarding the setting of buffers in there. Therefore, the outcomes in this phase are: 1) ME: the MRP routing (takts and milestone definition) and 2) BE: the definition of short and long term capacity constraints (manpower and cabins).

Planning

Production Planning (PP) is responsible for releasing a production order, planning a cabin for FASY, creating a production plan, planning testing, and assigning resources (materials and manpower) to each order. In doing so, FASY and Test planners make use of the processing time (A time+ C time) and safety time (B time) defined in the work preparation of a system; being the latter the core parameters in their production plans. In this regards, besides the BE and ME outcomes, the Master Production Schedule stands as the main input for PP.

The FASY production plan in the AMSL¹² is determined 12 weeks ahead a system's start date. The feasibility of this plan is discussed in weekly meetings by Production planners, Supply Chain managers, Central Planners and the Master Planning Representative. The Startmeeting Progress file records the output of this meeting, where the reliability of the FASY production plan is measured and the modules' overall progress is depicted. Aligned to the latter, a cabin is planned 5 weeks ahead to a machine's start date referred to the AMSL Machine plan. Twice a week the cabin progress meeting discusses the feasibility of the former plan depending on the possible escalated issues raised by machines currently in the cabins. FASY production order is opened in SAP 3 weeks ahead the starting day of the machine. Thereon, based on FASY start day, Test planners schedule materials forward and keep track of each milestone completion in such a way that all supplies will be on time for the execution of next operations, wherein the MTO ones receive special attention. Therefore, the outcomes in this phase are basically the

¹² The AMSL- Advanced Machine Status List excel file is used within PP for the overall tracking of manufacturing orders.

creation of a feasible production plan that will trigger the planning of ASSY, Test, and other external and internal supply chains.

Execution

The actual execution of the production plan is done at the shop floor. Therein, production orders are run in predefined¹³ cabins by operators making use of the takted routing provided by ME. In such a process, the operator contributes to the recording of system's CT for one of the data sources assessed further in this chapter, OBIIE. A brief explanation of this CT way of recording follows:

Manufacturing Execution System (ZMES)

Operators make use of a SAP tailored transaction called ZMES. They display their takts "to do" list and execute ZMES by enabling the Start button of the Process Step related to the operation(s) assigned. Executing ZMES is a straight forward procedure, therein, a work instruction (WI) is displayed for each process step in the takt, and whenever the operation is paused due to any discrepancy from the former procedure, a disturbance notification is made by the operator. It should be noticed that if the disturbance in execution escalates, the machine is changed to "Hold" status until a root cause and solution is given to that problem.

The outcome from Execution is basically the recordings of the shifts and overall machine status, thus, the most important input for the planning and analysis run in all Manufacturing departments.

Progress Tracking and Monitoring

Although machines statuses are tracked by all departments in Manufacturing, for the *FASY team leader* and the *Output leader* in Test, this is one of their main responsibilities. The latter perform reports at all levels: per machine, per week, per takts, in such a way that their reports can be used by all departments. Thus, these reports are the main input for the CT analysis run in BE, for the routing maintenance done in ME, for the review of the production plan in PP, and so on.

Therefore, for this project purposes, the outcomes of this phase are the status reports performed at all levels.

¹³ Not all type of systems can be produced in all cabins,. Thus, cabins are system-specific, and support solely the execution of one machine at the time.

APPENDIX E: Company's characteristics.

1) Exposed to operators' and organization's learning curves effect.

Where the operator's learning effect on processing times is understood as the advantages immersed in the repetition of same procedures by the same operator. Thus, an effect on the overall cycle time is expected over time as a consequence of operators' expertise being enhanced. Aligned to the latter, the organization's learning curve effect refers to the benefit gotten in departments' work, from which functionalities expertise allows a higher degree of prediction and eventually, the minimization of organizational costs due to departments' better performance.

2) Characterized by the continuous introduction of new technologies (R&D-oriented), e.g. high tech systems, capital goods, etc.

Companies pursuing a competitive advantage in industry are aware of the role innovation plays in the process. Innovation brings them to invest in R&D. In this regard, the steady upgrades in products/components come along the definition of new procedures which eventually affect the cycle time at the shop floor, having a direct impact on the planning of several internal/external supply chain partners.

3) Working under fixed lead times.

Where the lead time for each type of system is reviewed periodically and updated into the deterministic MRP framework in which these companies work on. The MRP relies on the definition of two important parameters: the lead time and safety time. Thus, being the items calculated on the MPS based on the Bill of Materials and planned lead times introduced in MRP, the accuracy of these parameters underlies the reliability of production plans, and eventually, the service delivery performance to external customers.

4) Characterized by a sequence comprised by m serial stages where predefined n milestones are found.

Stage j			Stage j+1		
Milestone i stage j	Milestone i+1, j	Milestone n, j	Milestone i stage j+1	Milestone i+1, j+1	Milestone n, j+1

n

In ASML:

FASY			Test		
Milestone 1, stage 1	Milestone 2,1	Milestone n, 1	Milestone 1, stage 2	Milestone 2,2	Milestone n,2

5) Working under a fixed “takt” scheme.

Where a takt is regarded as the work package contained in a shift. Furthermore, this model will assume the workload is well spread among takts, and natural disturbances, such as operators “breaks” and natural variability in raw processing times, are accounted for in this takts’ setting.

6) Executing “as soon as possible”.

Under this framework, milestone $i+1$ starts right after the completion of milestone i and stage $j+1$ does it right after j . In doing so, if milestone i , or stage j , finishes earlier than planned, the holding and idleness costs resulting from milestone $i+1$, or stage $j + 1$, having to wait for its originally planned start day, can be avoided and quantified at the most as an interest rate lost for not attaching this financial resources to a planning budget.

7) Can be distinguished by their capital intensive, low- volume high-risk production.

Therefore, attaining a cost efficient service level is preferable by means of keeping safety time rather than costly safety stock in planning.

APPENDIX F: Related works for the setting of lead times in serial production systems.

Although none of the published papers fully addresses the environment posed by the manufacturing settings assumed in this study, this section will describe briefly the most relevant publications found in literature for the setting of optimal lead times in serial production systems subject to uncertainties.

Yano (1987a) used an analytic approach to address the problem of optimizing planned lead times in a serial production system in which the actual processing times were stochastic. The objective of this model is to minimize the sum of inventory holding costs (h) resulting from early completion and tardiness costs (p) involved in two stage systems. In this regard, Yano (1987a) believed the tardiness costs should be considered solely for tardy delivery instead of intermediate stages. An extension of this study into two and three stages was found in Yano (1987b). Therein, the objective was to minimize the sum of inventory cost, rescheduling costs and backlogging costs for the finished product, although a difficulty was found in bringing the objective function to a close form once there are more than two stages. Despite Yano (1987) was criticized in some subsequent papers, as in Gong and de Kok (1994), his study represents the first step towards gaining intuition to the setting of optimal safety time buffers.

To surmount Yano's difficulty, Elfhasi (2002) developed a recursive scheme for determining the optimal planned lead times in a production system consisting of N processing stages. The objective function in this study is to minimize the sum of the inventory holding costs resulting from early completion, tardiness costs resulting from late completion at the preceding stage and backlog costs resulting from a late delivery of an order at the last stage. In this regard and based on practice, the tardiness penalty is assumed to be proportional to the holding costs; specifically, $p_i = 5h_i$. Finally, since for a large number of stages the computing time increases relatively quickly, Elfhasi (2002) proposed an heuristic in which only a subset of production stages are analyzed at the time.

Hnaïen, et.al (2008) generalized the approach in Yano (1987a) and provided a mathematical model to deal with the problem of planned lead time calculation for a multi-level serial production system, for one-type product, in an MRP environment, under stochastic lead times. In doing so, it was assumed that the actual lead times are independent discrete random variables and that the distribution probabilities in each level have finite upper values. The optimal value of the planned lead time (X_m^*) is given by:

$$F(X_m^* - 1) \leq \frac{b}{b+h} \leq F(X_m^*)$$

Hnaïen's (2008) expression provides evidence for the equivalence of this model to the well known discrete Newsboy model where the cumulative distribution function $F(\cdot)$ of the total lead time is used. Although Hnaïen's (2008) can be regarded as the most valuable contributor for this study, this paper neglects the effect the rescheduling and reallocation of supplies and manpower at intermediate levels, have on the total lead time planning of a product. Therefore, since previous studies in the field lack a

strategy to estimate time buffers on the particular manufacturing settings assumed in Section 4.1, the aim of this study is to extend previous works and provide a robust time buffer strategy for unreliable, unbalanced and serial sequences subject to a targeted service level and working under predefined milestones.

APPENDIX G: Buffer strategy application in ASML Manufacturing FASY and Test.

Data characteristics

- Data size.- As stated in Section 5.1.2, the actual cycle times from 34 systems in XT and 33 systems in NXT, stand as the input for all calculations in this section.
- Outliers.- Although outliers were identified at milestones' level of analysis, none were found at the sequence (or order) level, neither for XT 860 nor for NXT 1950. (Refer to Chapter 6 for the recommended method to identify outliers)
- Distribution.- The CT distribution at each level (namely, milestones, stages and total sequence) was found by using the EasyFit software in Excel. Results shown that for almost all levels, the Gamma distribution stands as the best fit, and for some exceptions, the Exponential distribution was the best one. In this regard, since the Exponential Distribution is a special case of a Gamma distribution, the Gamma distribution will be used as the unique distribution for further calculations. Figure G.1 and G.2 depict the probability density function for the XT860 and NXT 1950 total cycle times; thus, at the sequence level.

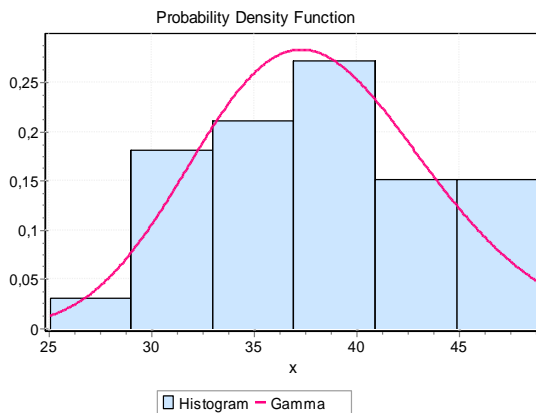


Figure G.1 XT 860 CT distribution

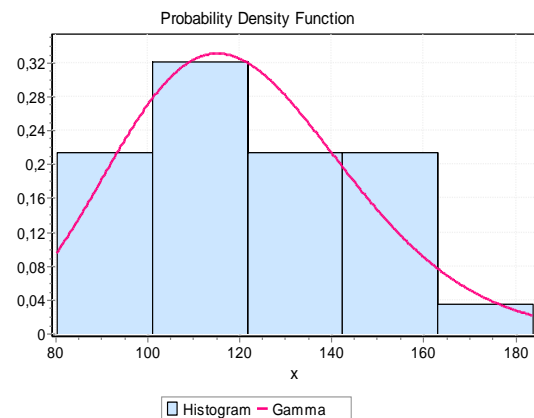


Figure G.2 NXT 1950 CT distribution

Statistics

Having collected data for 34 XT 860 systems, it was decided to use the statistics of the first 26 orders (Refer to Chapter 6 for recommendation on this decision) for the application of this buffer strategy. Therefore, the remaining 8 records will be used in Section 5.3 for measuring the level of predictability this method has in comparison to the current planning parameters. Thus, 26 actuals will serve for the

determination of the values for the different parameters needed in the planning of 8 subsequent volume systems. In the case of NXT 1950, the analysis from actual case no. 7 till actual case no. 28 (thus, 21 systems) is used for the determination of the parameters used in the planning of 5 subsequent systems.

The statistics for both systems are depicted below, for the special case of NXT, the statistics of the make to stock (MTS)¹⁴ are shown separately from the make to order part of the sequence (MTO) due to the high variability distinctive in this latter. Later on this will be addressed in detail.

NXT1950	Prepare	Building	System	Init	FASY	MS3
min	0,58	7,00	4,67	2,33	16,33	5,00
max	1,17	18,67	17,50	8,75	50,75	23,00
mode	0,58	9,33	11,08	5,83	23,92	12,00
mean	0,64	11,29	9,77	5,86	28,71	10,95
Stdev	0,18	3,03	3,42	1,86	8,87	4,82
variance	0,03	9,18	11,71	3,46	42,52	23,25
Distribution	gamma	gamma	gamma	gamma	gamma	gamma
alpha,k	12,77	13,88	8,15	9,95	19,38	5,16
beta,Θ	0,05	0,81	1,20	0,59	1,48	2,12

NXT1950	MS4	MS5	MS6	MS7	MS8	Upgrade	MS9
min	4,00	6,00	2,00	2,00	2,00	5,00	2,00
max	25,00	27,00	15,00	8,00	11,00	34,00	12,00
mode	6,00	13,00	6,00	3,00	4,00	5,00	4,00
mean	10,43	14,60	6,33	4,30	5,33	11,90	5,50
Stdev	5,94	6,54	3,75	1,95	2,37	7,06	2,72
variance	35,26	42,78	14,03	3,80	5,63	49,78	7,42
Distribution	gamma	gamma	gamma	gamma	gamma	gamma	gamma
alpha,k	3,08	4,98	2,86	4,87	5,05	2,84	4,08
beta,Θ	3,38	2,93	2,22	0,88	1,06	4,18	1,35

¹⁴ Be aware MTS does not refer, as in literature, to the production of systems aimed to be kept in a warehouse before a purchase order is released. In this regard, "MTS" stands as the terminology used in ASML to represent the part of a product's sequence in which a system configuration is still standard. Therefore, "MTO" refers to the remaining part of the sequence where customization is carried out; thus, customer's options are build in.

NXT1950	MS10	MS11	CODP	MS12	TEST	MTS	MTO	TOT
min	2,00	3,00	0,00	9,00	87,00	80,33	17,00	110,33
max	14,00	11,00	15,00	38,00	162,00	159,17	46,00	191,17
mode	3,00	4,00	8,00	17,00	138,00	-	27,00	-
mean	4,85	5,65	8,00	21,62	114,86	113,90	29,00	144,19
Stdev	2,92	2,25	3,74	7,92	21,32	21,70	8,25	22,42
variance	8,56	5,08	14,00	62,75	454,63	470,75	68,00	502,76
Distribution	gamma	gamma	gamma	gamma	gamma	gamma	gamma	gamma
alpha,k	2,75	6,28	4,57	7,45	29,02	27,56	12,37	41,35
beta,Θ	1,76	0,90	1,75	2,90	3,96	4,13	2,34	3,49

XT860	Prepare	Building	System	Init	FASY	MS3
min	0,58	3,50	1,75	1,75	8,17	2,00
max	0,58	7,00	5,25	6,42	18,08	8,00
mode	0,58	3,50	2,33	2,92	18,08	2,00
mean	0,58	4,57	2,78	3,34	11,85	3,49
Stdev	0,00	1,07	0,93	1,35	3,13	1,74
variance	0,00	1,15	0,86	1,83	9,82	3,01
Distribution	cons.	gamma	gamma	gamma	gamma	gamma
alpha,k	0,00	18,13	8,98	6,09	14,29	4,05
beta,Θ	0,00	0,25	0,31	0,55	0,83	0,86

XT860	MS4	MS5	MS6	MS7	ATP	Test	TOT
min	1,33	1,33	1,00	1,67	2,00	20,33	33,25
max	4,67	10,00	9,67	9,67	20,00	39,67	50,17
mode	4,33	4,00	5,00	2,00	3,00	-	42,75
mean	2,83	5,32	5,25	3,60	7,69	29,00	40,85
Stdev	1,06	2,32	2,45	1,90	5,00	5,54	5,13
variance	1,12	5,36	6,00	3,61	25,02	30,64	26,31
Distribution	gamma	gamma	gamma	gamma	gamma	gamma	gamma
alpha,k	7,12	5,28	4,60	3,60	2,36	27,45	63,42
beta,Θ	0,40	1,01	1,14	1,00	3,25	1,06	0,64

Determine a target service level

As mentioned earlier in Chapter 3, ASML manufacturing FASY and Test work under a predefined target service level of 0.75. In this regard, since further in this chapter a comparison of this method with the current situation is aimed to show the performance of this strategy, it was decided to keep this target as the one to achieve in this section. Despite the latter, a recommendation for a cost efficient target service level will be given in Section 5.4.

The placement of buffers in sequence.

Time buffers in ASML manufacturing can be placed at different levels in the sequence: takts, milestones, stages, and at the end of the total sequence. At this point a reminder is needed regarding time buffers in takts. In Chapter 3 it was decided to assume the distribution of time buffers at this level is well done by ME, and thus, was taken out of this project consideration. The latter triggered by the high level of complexity involved if getting into this level of detail.

Therefore, due to the fact that:

- 1) Buffers in takts require huger amount of data.- the more dependencies are involved the more data sources stand, and the more gathering is needed. Moreover, being aware data mismatches are prone to be found along the way, this scenario seems unfeasible for this project timing.
- 2) Workload allocation analysis is needed- getting into takts level would require a further investigation regarding how well the work packages in ASML manufacturing are defined. Being the latter a research topic by itself, makes unfeasible to get into this level of detail.
- 3) The high volatility in the organization together with the time consuming of this scenario, enhances the probability of an efficient time buffer being outdated once launched.
- 4) The main purpose of this study is the estimation of the average time for disturbances when the average processing time is given. The latter accounting already for the natural time for variations in process steps, all regarded at the takt level.

allocating time buffers in takts was not studied.

Where to put buffers in ASML sequences was decided by analyzing the feasibility of setting buffers in milestones, at the end of both stages (FASY and Test), or at the end of the complete sequence. In this regard, results showed it is less costly allocating buffers at the milestones level. The latter is due to the fact that the other two scenarios, by merging milestones (buffer at stages) and stages (buffer at the end), the instability in planning increases, so as the probability of being delayed.

Allocating buffers at milestones brings 25% less costs than at stages, and 24% less than at the end. Thus, being aware the worst option is “at stages” and then “at the end”, the best option for allocating time buffers in ASML manufacturing is at milestones level.

The estimation of milestones' buffer sizes under a minimal quotation approach.

The estimation of time buffer sizes for all milestones in FASY and Test will be concurrently carried out in this section for both systems in scope: the standard system XT 860, and the customized system NXT1950. In this regard, a special remark is needed about the sequence in NXT 1950. This remark says that despite the fact that a customer commitment agreement triggers the releasing of a system order in manufacturing, the customized milestones are actually identified at the end of this system's sequence. Therefore, previous milestones follow a standard sequence. The latter with the aim of facilitating the re-assignment of a system to another customer in case the original one retracts from its commitment or any other eventuality occurs while the system is in progress. As a consequence, all customer options are built in the system at the end, in the MTO part of the sequence. In this regard, since the high variability characterizing the MTO milestones was spread all over the sequence when the total buffer was computed, the estimation of time buffer sizes for NXT1950 was based on the consideration of two subsequences: MTS and MTO. Whereas the MTS sequence comprises FASY and all milestones in Test before, and not including, Milestone 11; the MTO sequence is represented by the CODP (Customer Order Decoupling Point in ASML terminology) and Milestone 12.

Below the steps enlisted in Chapter 4 for the description of this buffer strategy are restated and followed up.

- 1) Compute $\alpha_{pt}, L^*_{pt}, B^*_{pt}$ at the sequence level.

		XT 860	NXT 1950
	Ch4 reference		
Target SL	α_{pt}	0.75	0.75
Recommended sequence lead time	L^*_{pt}	44.18	MTS - 127.69 MTO - 34.06
A time sequence	X_{pt}	13.92	MTS - 46.98 MTO - 13.34
Recommended sequence buffer for the current situation	B^*_{pt}	30.26	MTS - 80.71 MTO - 20.72

Above, the A time of 13.92 stands as the number of days it would take to produce one XT860 system if no disturbances (other than team meetings and breaks) occur in manufacturing. The 19.25 days, so as the corresponding 46.98 and 13.34 days for NXT 1950 systems, were taken from the system's sequence defined in SAP by Manufacturing Engineering.

2) Adjust B^*_{pt} to learning curve effects

		XT 860	NXT 1950
	Ch4 reference		
Recommended sequence buffer for the current situation	B^*_{pt}	30.26	MTS - 80.71 MTO - 20.72
Learning percentage	k	0.998	MTS - 0.90 MTO - 1
Orders to be PREDICTED	u	8	6
Adjusted Sequence Buffer	B'_{pt}	30.17	MTS - 72.49 MTO - 20.72

The learning percentage figures above were obtained by analyzing the cumulative average from the last 26 actuals for XT and 21 for NXT. In this regard, a 0.90 learning percentage shows there was an improvement of 10% from the cumulative average of those actuals, meaning people at the factory, and in general, the Organization, learned by doing over time. Therefore, as expected, the XT volume system presents a smaller learning effect than the high variable and customized NXT system.

Moreover, due to the fact that this company works under a deterministic MRP framework in which updating planning parameters too frequently would not be appropriate, the application of this buffer strategy is with the aim of predicting the buffers needed for the in- time production of a predefined number of future systems. In this regard, 8 and 6 systems stand as the number of orders to be predicted. In Chapter 6 recommendations are given regarding the latter. Therein, it is advised to review CT monthly instead of quarterly. Therefore, if such recommendation were followed, the 8 and 6 systems would be the advised ones.

3) Compute each milestone coefficient of variation CoV_{ijt-1}

XT 860		NXT 1950			
Milestone	CoV	Milestone	CoV	Milestone	CoV
Prepare	0,00	Prepare	0,28	Upgrade	0,59
Building System	0,23	Building	0,27	MS9	0,50
Init	0,33	System	0,35	MS10	0,60
MS3	0,41	Init	0,32	MS11	0,40
MS4	0,50	MS3	0,44	CODP	0,47
MS5	0,37	MS4	0,57	MS12	0,37
MS6	0,44	MS5	0,45		
MS7	0,47	MS6	0,59		
ATP	0,53	MS7	0,45		
	0,65	MS8	0,45		

4) Estimate the buffer size for milestones holding a $CoV_{ijt-1} > 0.05$

XT 860			NXT 1950		
Milestone	wpa _{ij}	B _{ij}	Milestone	wpa _{ij}	B _{ij}
Prepare	0	0	Prepare	0,00	-0,34
Building	0,05	1,49	Building	0,10	7,04
System	0,04	1,35	System	0,10	7,36
Init	0,07	2,02	Init	0,05	3,86
MS3	0,09	2,66	MS3	0,12	8,93
MS4	0,07	2,09	MS4	0,10	7,40
MS5	0,15	4,52	MS5	0,16	11,79
MS6	0,14	4,23	MS6	0,06	4,47
MS7	0,10	3,10	MS7	0,03	2,07
ATP	0,29	8,71	MS8	0,02	1,69
			Upgrade	0,18	12,90
			MS9	0,03	1,96
			MS10	0,02	1,44
			MS11	0,03	1,92
			CODP	0,14	2,83
			MS12	0,86	17,89

From above all milestones need buffers with the exception of "Prepare" in XT860 system. Therefore, by calculating each milestone weight priority (wpa_{ij}) and using the adjusted sequence buffer B'_{pt} computed in 2), the buffer needed for each milestone can be estimated by assigning a proportion of B'_{pt} to each. For instance, the time buffer size in MS3 (B_{1,2}) for NXT1950, is equivalent to 12% of the B'_{pt} value; thus, B_{1,2}=0.12*72.49 = 8.93.

5) Compute the planned lead time for each milestone L_{ijt} . Thereon, find the planned lead time for the total sequence of product p, L_{pt} .

XT 860			NXT 1950		
Milestone	ASML A time	Milestone's Leadtime	Milestone	ASML A time	Milestone's Leadtime
Prepare	0,58	0,58	Prepare	1,16	0,82
Building	3,50	4,99	Building	4,64	11,68
System	1,75	3,10	System	2,90	10,26
Init	1,75	3,77	Init	2,32	6,18
MS3	1,33	3,99	MS3	2,90	11,83
MS4	1,00	3,09	MS4	4,64	12,04
MS5	1,33	5,86	MS5	4,06	15,85
MS6	1,67	5,90	MS6	2,90	7,37
MS7	1,00	4,10	MS7	2,90	4,97
ATP	0,00	8,71	MS8	4,64	6,33
			Upgrade	0,00	12,90
			MS9	4,64	6,60
			MS10	4,64	6,08
			MS11	4,64	6,56
			CODP	6,96	9,79
			MS12	6,38	24,27

Total LT = 44,08 days

Total LT = 153,53 days

APPENDIX H: Scenario analysis.

Target service level

In Chapter 4 it was recommended from literature to determine the target service level based on the tardiness and earliness costs immersed from planning. However, it was observed throughout the performance analysis of this buffer strategy that this recommendation holds solely for the standardized products characterized by low variability in execution. Thus, the relation $[\text{tardiness cost}/(\text{tardiness cost} + \text{earliness cost})]$ can still be considered as a recommendable cost efficient target service level for the XT860 system.

Below, a recommendation follows for the setting of a cost efficient target service level for the lead time planning of both systems. These recommendations come as a result of analyzing the associated instability, earliness and tardiness costs for the same sample data subjected to different target service levels.

NXT1950

If as in literature, the cost efficient relation stated above is taken into consideration, 0.97 would be the recommended target service level. However, subjecting to such target would increase the makespan and, although no tardiness costs would be involved, the instability costs and earliness costs would be so high that would end up making this service level one of the least cost efficient among all others. The high instability costs would be the result from the frequent reschedules associated to longer and overestimated makespans. In line with the latter, being committed to comply 97% of the cases in time would not just make most of the orders to be earlier, but due to the high variability in this system (coming mostly from customization) there are cases in which a system is finished lot much earlier than the average ones, and those costs are extended as the service level (hence, makespan) does. Table H.3 summarizes the latter tradeoffs.

It can be concluded from Table H.3 that planning a lead time under a targeted service level of 0.65 results to be the least costly among the other targets, and thus, stands here as the recommended service level to work under if the organization seeks a reduction in costs. The latter is due to the fact that by setting this target service level, a makespan of 145 days enables planning to fulfill all orders in time, the tardiness cost is avoided and the instability and earliness costs are kept low. Figure H.3 depicts the latter.

Target SL	Rescheduled (days)	Early (days)	Tardy (days)	Makespan (days)	Total Cost = E+T+I
0,55	363,72	79,42	11,92	137,56	€ 160.734
0,6	370,99	92,23	3,1	141,16	€ 74.679
0,65	381,3	111,91	0	144,96	€ 49.053
0,7	393,18	136,38	0	149,03	€ 56.473
0,75	406,64	163,32	0	153,53	€ 64.653
0,8	422,900	193,99	0	158,64	€ 73.996
0,85	442,940	230,63	0	164,74	€ 85.171
0,92	486,480	302,63	0	176,74	€ 107.242
0,94	506,360	332,87	0	181,78	€ 116.547
0,95	518,690	351,35	0	184,86	€ 122.234
0,96	533,720	373,34	0	188,53	€ 129.008
0,97	553,310	400,77	0	193,10	€ 137.476
1	769,730	677,55	0	238,23	€ 222.940

Table H.3 NXT Service levels costs (Sample size: 6 systems)

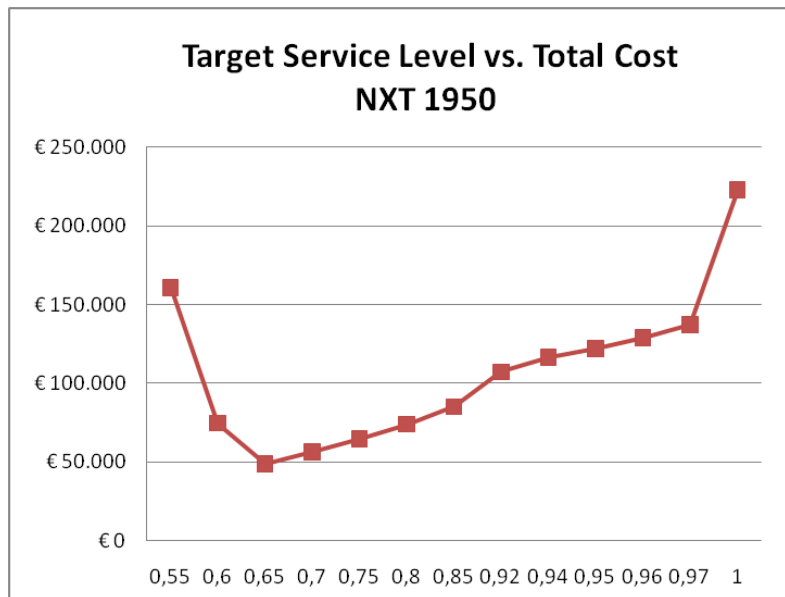


Figure H.3 NXT Target service level recommendation (65%)

XT 860

The target service level suggested for this standard system is closer to the one recommended in literature. This is due to the less variability underlying its execution. In literature, a 0.98 target service level would be advised for planning lead times. Although the latter recommendation would bring cost efficient results, in Table H.4 and Figure H.4 it is demonstrated that cost efficiency can be obtained along a range of target service levels. In this regard, non significant differences stand between the cost coming from a 92% tsl and a 98% tsl. Therefore, it is recommended to set a target service level pertaining to this

range if the organization is pursuing not just reliability in lead times, but the lowest costs coming from earliness, tardiness and instability.

Target	Rescheduled days	Early	tardy	Makespan	TC= I+E+T
0,55	122,61	35,38	11,84	41,19	€ 90.314
0,6	123,99	38,87	10,04	41,85	€ 79.368
0,65	125,65	43,02	8,66	42,54	€ 71.129
0,7	127,45	47,43	7,19	43,28	€ 62.355
0,75	129,44	52,26	5,58	44,08	€ 52.750
0,8	132,360	57,7	3,77	44,99	€ 42.019
0,85	136,120	65,2	2,69	46,06	€ 36.076
0,92	143,490	79,72	0,61	48,14	€ 24.639
0,94	147,290	85,99	0	49,00	€ 22.039
0,95	149,630	90,17	0	49,52	€ 22.036
0,96	152,400	95,12	0	50,14	€ 22.599
0,98	161,110	109,51	0	51,94	€ 23.281
1	226,670	194,58	0	62,57	€ 34.888

Table H.4 XT860 Service levels costs (Sample size: 8 systems)

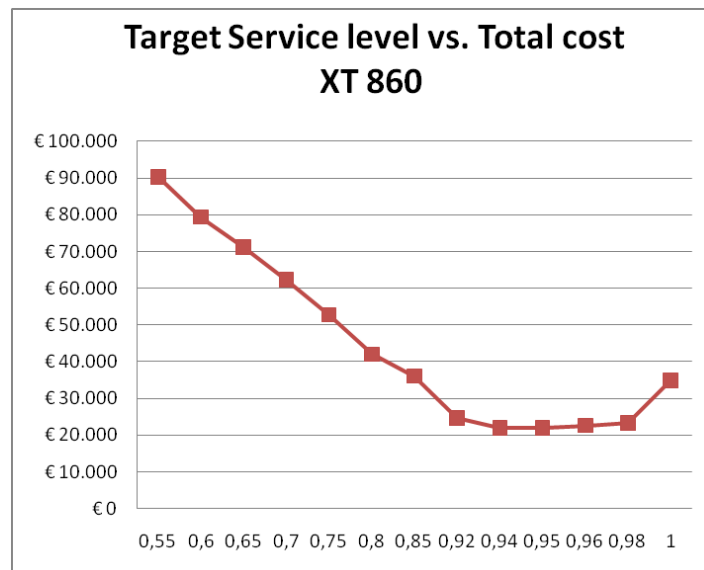


Figure H.4 XT860 Target service level recommendation (92% - 98%)

Move Rate

The move rate is strongly associated with 1) the additional amount of hours spent in rescheduling due to one percentage change on production plan instability, and 2) the number of orders to predict for the upcoming period. As for the instability related, the higher the move rate, the more orders in progress, and the more additional hours would have to be spent in rescheduling due to a percentage of change in plan. Furthermore, the higher the move rate is, the larger the number of orders needed to be predicted.

A special remark needs to be done at this point. As for now, all costs assumptions have neglected the influence the move rate can have on the estimation of lead times (hence, buffer times) and managerial decisions in ASML when it raises above what ASML capacities can cope with. In this regard, managerial decisions referred to the opening out of a new. Therefore, for move rates greater than 6, managers would face the decision of whether opening new cabins (factory extension) or not. This decision is strongly influenced by the planned lead time of the systems. In this scenario, being early is penalized severely due to the possible mistaken expensive decision of extending capacities. Therefore, the planning of longer lead times than the actual needed would be reflected on the unnecessary building of new cabins and an associated higher earliness cost. This scenario was studied for both systems. Therein, it was observed that the lowest cost was achieved when the target service level was settled as 80% in the XT860 system and 60% in the NXT1950. As a conclusion, whenever the move rate goes beyond 6, penalized earliness with the investment lost in building new facilities (thus, the new cabin cost per day), and if the lowest cost is pursued by the setting of the target service level, use 80% in the standard system and 60% in the NXT1950 system.

Interest Rate

As mentioned at the end of Section 5.3, the interest rate is assumed to provide the opportunity lost from not being able to invest in a risk free asset and instead, attaching those financial resources to the budget forecasted for that planning horizon. For comparison purposes, in the costs analysis, it was assumed this interest rate is 5% and is paid monthly. However, investing on low risk assets is also possible for representing the interest rate lost in a period, and considering them, would claim for the analysis of different interest rates (IRs). The cases of $IR=0.05$, $IR=0.10$ and $IR=0.15$ were addressed for both systems. See Figure H.5 for the XT 860 scenario and Figure H.6 for the NXT 1950 scenario.

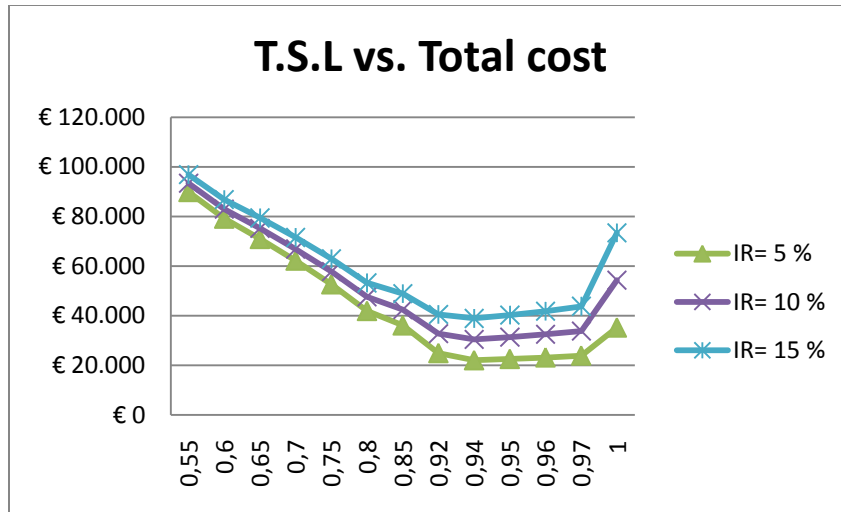


Figure H.5 XT860 Target service level recommendation for different IR.

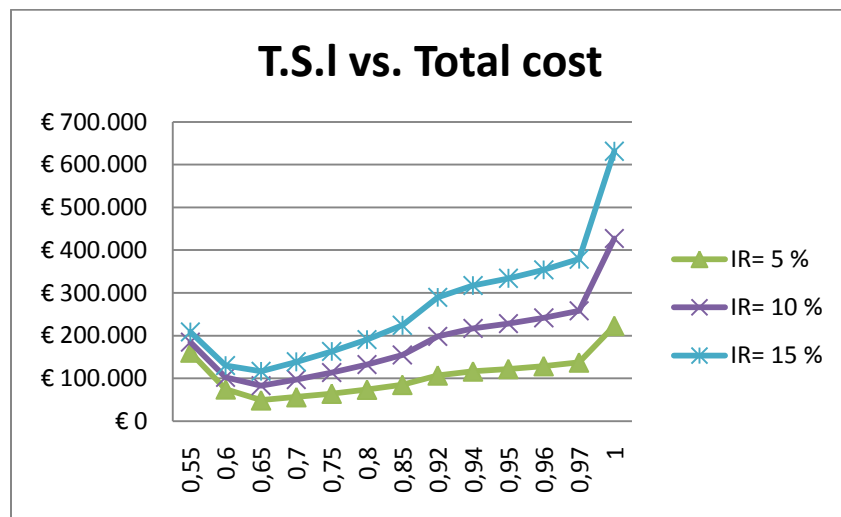


Figure H.6 NXT 1950 Target service level recommendation for different IR.

Figures above show that the interest rate considered does not influence the service level recommendation. Therefore, the opportunity cost from not investing in any kind of asset (low/moderate/high risk) would bring the lowest total cost in a period when the service level is between 92% and 98% in XT860 and 65% in the NXT 1950 case. Moreover, figures above show that the higher the interest rate considered, and the higher the service level, the higher the total cost. The latter is due to a longer makespan coming from the higher service level; and thus, the more instability cost coming from rescheduling these variable systems.

Learning percentage

The learning percentage directly influences the amount of buffer required for next period. In this regard, the higher the learning percentage, the less learning and the more standardized the system becomes. Furthermore, besides adjusting the level of buffer required for next period, the learning percentage highly influences the number of orders to predict. Particularly, if the learning percentage is close to one, the more orders can be predicted without losing level of accuracy.

For the case of XT860, cost efficiency in a period for a determined learning percentage (0.998) is reached when more than 6 systems are predicted (See Figure H.7). As for NXT1950, predicting this system comes to be cost effective for 7 orders, if predicting more (or less) the tardiness costs (or earliness costs) increases due to the assumed learning effect throughout the period (See Figure H.8).

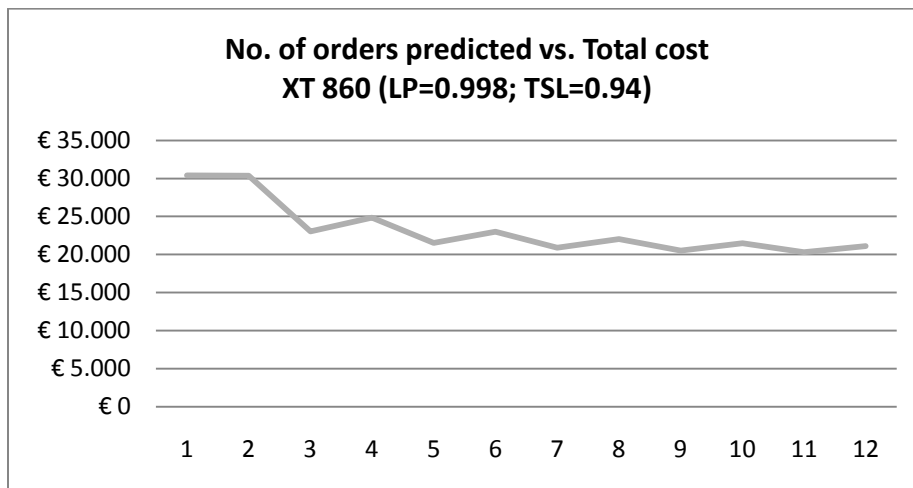


Figure H.7 XT860 cost efficient number of orders to be predicted in a month. ($u > 6$)

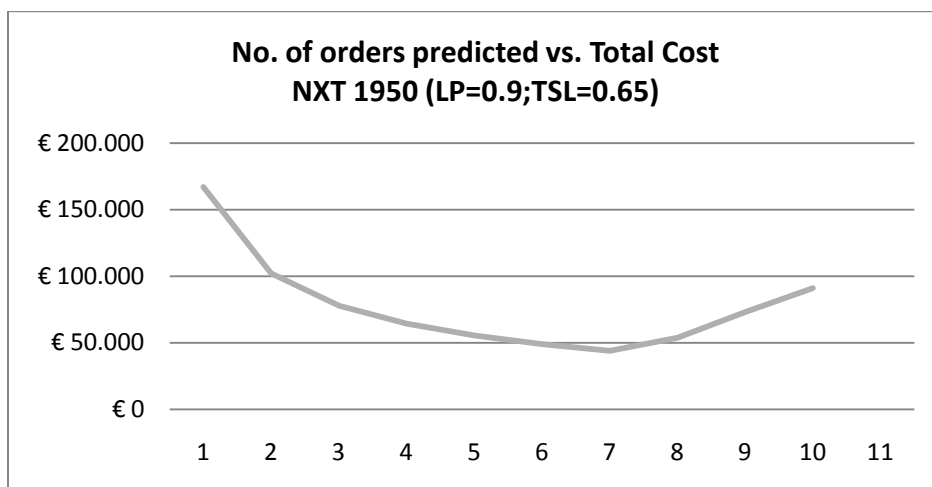


Figure H.8 NXT1950 cost efficient number of orders to be predicted in a month. ($u = 7, \pm 1$)

Orders to predict

Before it was stated a sample size of 6 and 8 orders (NXT 1950 and XT860, respectively) was used for analyzing the performance of the buffer strategy presented in Chapter 4. Although in Chapter 6 a recommendation is aimed to provide a way to estimate the number of orders to be predicted in a month, in this section the same sample size was used for addressing the cost behavior due to a period over/sub estimation of orders to be predicted. Tables below show that cost efficiency can be reached whenever overestimation is preferred. Therefore, if 6 orders were predicted and just 5 happened, the immersed cost was lower than if 6 orders were predicted and eventually 7 happened. This conclusion holds for both systems, the standardized and customized one.

NXT 1950 (65% t.s.l)				XT860 (94% t.s.l)			
No. orders predicted	Makespan	No. of orders occurred	Cost	No. orders predicted	Makespan	No. of orders occurred	Cost
6	144,96	5	€ 45.242	8	49,02	7	€ 20.398
6	144,96	6	€ 49.052	8	49,02	8	€ 22.053
6	144,96	7	€ 58.977	8	49,02	9	€ 25.751

APPENDIX I: Data sources and reliability assessment.

As of 1st May, several sources of data hold CT reports for all systems. However, the reliability of those is diverse, so as the way records were done. In this section two data sources will be described, so as their level of reliability for further analysis.

OBIIE

OBIIE is a database which extracts information from SAP. Therein, CTs are reported based on the time stamps done by operators at the shop floor through the manufacturing execution system (ZMES) described earlier in this chapter. However, these time stamps are not reliable at this moment due to operators' unreliable way of making use of the ZMES transaction. For instance, the operator registers solely whenever a takt is started and finished, without deploying a detailed description of any disturbances if occurred; furthermore, some takts are logged on while a former takt has not reported to be finished yet or even worse, eventually the second takt is not completed fully. Figure below illustrates an OBIIE report per takt duration. Moreover, being aware that no parallel takts can exist and the inaccuracy resulting from OBIIE CT roundup/down, past CT data extracted from OBIIE will be regarded at this moment as unreliable; and thus, useless for this project data analysis.

Excel (GANTTs and Takt status report)

Besides OBIIE, each machine progress is tracked and monitored daily by FASY and TEST output leaders.

In just one Excel file, the FASY team leader reports takt status for all systems on a Gantt chart. Therein a takt appears as on Hold, or accomplished; if on hold, a reason is stated together with its corresponding disturbance type. Although on several interviews it was stated this data source is, above all, the most reliable in manufacturing; the notification for disturbances can still be considered unreliable for analysis due to any possible information being filtered for FASY interests. Nevertheless, this data source was used for the recordings of CTs, without addressing disturbance notices.

In Test, Output leaders employ two excel files to report this daily progress. Firstly, they make use of a GANT chart from which green highlights depict the number of days spend for each milestone completion. Secondly, at a lower level of detail, OL register takts status per milestone, where the latter can be reported as "Finished", "on Hold", or "Lost". Whereas the on Hold status is possible to be found in ongoing orders, once a machine is finished and kept in records, the takts status in finished systems recordings depict solely the number of takts lost and finished per milestone, since after on Hold the takt status changed either to Finished or Lost. All this information is manually updated by Output leaders in another excel file known as "Takt status reports", in which all takts disturbances are explained and allocated to a B category. The latter allowing us to consider these excels as our main source of data for Test.

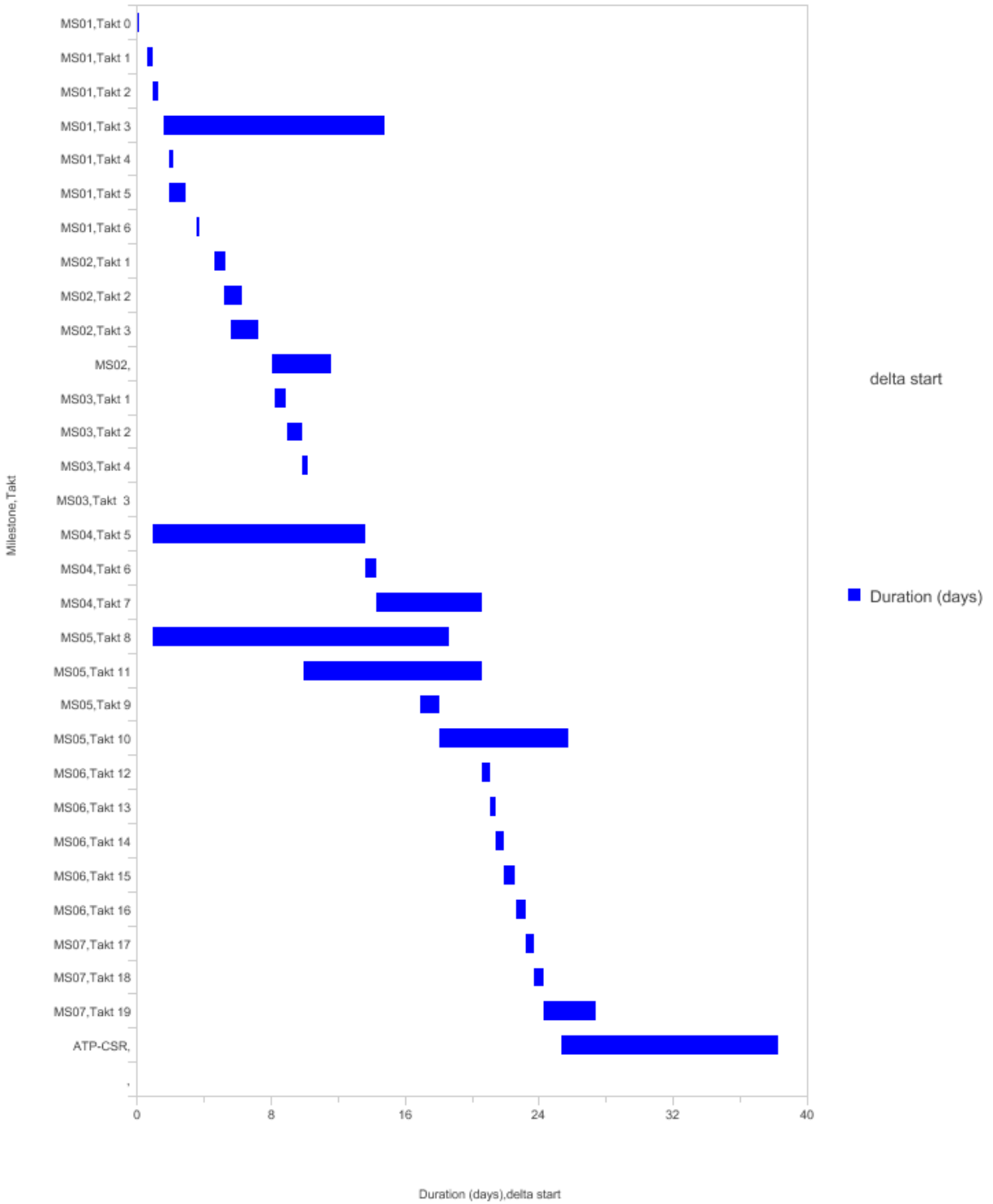


Figure I. OBIIE report per takt

APPENDIX J: ASML recommended data source.

Recommended data source for actual CT records		
	XT 860	NXT 1950
FASY		
File name	Progress_ATPFA_&_amp;_OIP	Progress_ATPFA_&_amp;_OIP
File owner	FASY- BWAA	FASY- BWAA
File main users	FASY, BE, PP	FASY, BE, PP
Test		
File name	Takt_status_overview	NXT_CycleTimePerformancePoster
File owner	Test - MAEI	Test- OVEN
File main users	Test, BE	Test, BE
Recommended data source for system's A time		
	XT860	NXT 1950
FASY	ME - BSMF	ME - BSMF
TEST	ME- CBET	ME-MIDI

APPENDIX K: Periodicity example and application.

Example. Assume 30 actual cycle times for the last 6 months are available for analysis. Let's consider firstly a sample size of 10, thereon, start by plotting the average cycle time from observation 1 to 10, then from 2 to 11, and so on, till 21 to 30. Add the trend line for this graph and keep increasing the order level from this polynomial, if the R-square from the polynomial reaches 1, then stop; otherwise, increase the sample size or its order level. Let's assume $R^2=1$ until the sample size turned to be 18 and the polynomial model was from the type $y= a+ bx+cx^2+dx^3+ex^4+fx^5+gx^6$; holding the order level = 6. Since there were 6 meaningful changes in 6 months, the latter would recommend reviewing the lead time parameters in MRP monthly, by means of a data set=18.

ASML application. This application is based on the XT860 case presented in Chapter 5 (therein, referred to Appendix G). Therein, the reason for deciding to use 26 actual cycle times for getting statistics of this system follows. As of February 1st, 31 actual cycle times of the last 4 months were available for analysis¹⁵. As a starting point the cumulative average of 25 systems was considered; thus, an initial sample size of 25. When plotting this dynamic cumulative average, the polynomial model of order 6 predicted in less than 1 (see figure K.1) and therefore it was decided to increase the number of actuals considered in the cumulative average in one. Thereon, the dynamic average of 26 actuals brought a polynomial model from order 5 with a level of predictability of 1 (Figure K.2). Therefore, since there were 5 meaningful changes in 4 months, it can be recommended to review these norms by means of a data set = 26 actuals, every $4/5=0.8$ months, or for the organization's simplicity purposes, once a month.

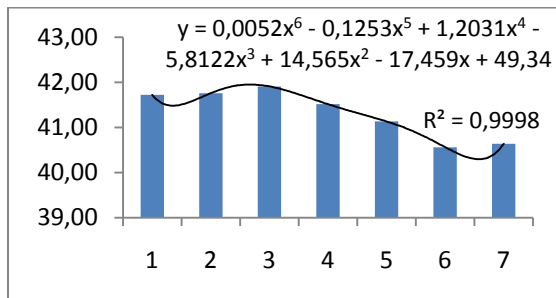


Figure K.1. Sample size 25, $R^2 < 1$

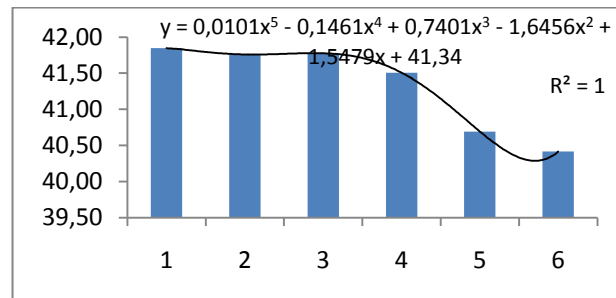


Figure K.2. Sample size 26, $R^2 = 1$

¹⁵ However it should be remarked that throughout the execution of this study more cycle times were recorded and later used for the performance analysis of this buffer strategy in Chapter 5.

APPENDIX L: Example of outlier's detection.

MS5 actual CT record # 9 = 42 days.

	MS 5
μ - Average (N=21)	15.90
σ - Std dev. (N=21)	8.74

Is record # 9 an outlier? Is the abs $[(X - \mu) / \sigma] > 2.5$?

$$\begin{aligned}Z &= (X - \mu) / \sigma \\Z &= (42 - 15.90) / 8.74 \\Z &= 2.98 \\ \text{Result: } &2.98 > 2.5\end{aligned}$$

Conclusion: MS5 actual CT record # 9 is an outlier and should be removed from MS5 data set.

APPENDIX M: Example for determining the learning percentage.

The case of NXT1950 studied in Chapter 5 (therein, referred to Appendix G) will be addressed. Therein, the learning percentages of 1 and 0.90 for the MTO and MTS sequences, respectively, were used. Below it is shown how these learning figures were calculated. In doing so, it should be reminded 21 actuals were used in this study for prediction of 6 orders.

The MTS learning percentage.

MTS		MTS	
Record No.	Actual CT	Record No.	Actual CT
1	122	11	130
2	157	12	102
3	103	13	90
4	117	14	127
5	112	15	131
6	112	16	117
7	145	17	102
8	105	18	87
9	159	19	80
10	107	20	94
		21	93

Table M.1 MTS Actual CTs (NXT 1950; Sample size = 21)

						Av.13	
						Av.14	120
					Av.(1-14)	121	121
					Av.(2-15)	121	119
					.	118	120
				Av.18		118	118
			Av.(1-18)	118	...	116	117
			Av.(2-19)	116		114	114
	Av.(1-20)	115	...	Av.(3-20)	112	.	113
	Av.(2-21)	111		Av.(4-21)	112	Av.(8-21)	109
							k= 0.90

Table M.2 Moving averages MTS Actual CTs.

Table M.1 enlists the actual CTs for the 21 samples under study, be aware the order in that list is according to records' FASY start day. In addition, being just the MTS sequence considered, the actual CTs there account for the sum up of the actual CT of the total sequence minus the CODP and MS12 CT (being the sum of those latter the MTO CT). Therefore, MTS CT = Prepare CT+ CT Build + CT System + CT Init + CT MS3 + CT MS4 + CT MS5+ CT MS6 + MS7 CT+ MS8 CT+ Upgrade CT + MS9 CT + MS10 CT + MS11 CT.

Table M.2 presents the moving averages procedure explained earlier in this section and followed in this study for the estimation of time buffers in Chapter 5 (or Appendix G). This table depicts how the number

of records in average kept decreasing until it was realized the moving averages weren't falling steadily (120, 121... 109). Therefore, a step back was taken to the last moving averages decreasing steadily (121, 121, 118... 109) and thereafter the learning percentage was computed by dividing $109/121 = 0.90$.

The MTO learning percentage.

Record No.	MTO	Record No.	MTO
	Actual CT		Actual CT
1	24	11	42
2	17	12	46
3	27	13	27
4	18	14	38
5	56	15	27
6	30	16	26
7	22	17	37
8	29	18	23
9	32	19	33
10	18	20	40
		21	24

Table M.3 MTO Actual CTs (NXT 1950; Sample size = 21)

	Av.20
Av.(1-20)	31
Av.(2-21)	31
	k = 1,01

Table M.4 Moving averages MTO Actual CTS

As in the MTS learning percentage, Table M.3 enlists the 21 MTO CT records under study. Thereon, Table M.4 depicts the moving average procedure followed in the estimation of the learning percentage used in Chapter 5(or Appendix G). Results there show a learning percentage of 1.01 occurred along the production of those 21 systems; therefore, since there was not a learning effect, and in line with the minimal quotation approach explained earlier in this thesis, in this case, a learning percentage of 1 should be used.

APPENDIX N: Buffer Strategy Implementation- Process flow.

