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MASTER

60 GHz wireless power transfer - system analysis and Doherty power amplifier design
4-stage Doherty power amplifier

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60 GHz wireless power transfer - System analysis and Doherty power amplifier design

4-stage Doherty power amplifier

Lennaert Bronts

July 2014

TECHNISCHE UNIVERSITEIT EINDHOVEN

Abstract

Department of Mathematics and Computer Science
Department of Electrical Engineering
Mixed-signal Microelectronics Group

Master thesis

60 GHz wireless power transfer - System analysis and Doherty power amplifier design

4-stage Doherty power amplifier

by Lennaert Bronts

The aim for this thesis is to specify and design a power amplifier that is able to charge a 60 GHz battery-less sensor tag. This sensor tag has the capability to harvest energy wirelessly from an RF source in order to charge itself. With the use of lab equipment it currently is possible to charge the RF tag at very close proximity. A power amplifier situated in a base station would eliminate the use of this setup.

This thesis consists out of a system analysis to determine the specifications for the base station power amplifier and the transmit antenna array. The PAs with antenna array need to be able to create a pencil like beam so that enough power is delivered to charge the sensor node. To verify the system design the circuit design an initial circuit design is started.

From several architectures the 4-stage Doherty PA is chosen as most promising architecture. This architecture is able to support a wide range of output powers while maintaining high efficiency and variable directivity. High efficiency is achieved by dynamically modulating the loads presented to the PAs so that the voltage swing is maximized.
Analytical calculations and simulations in the system designing process show promising results although further research is required. Further research comprises out of the analysis in the impedances presented by the load modulating network, near field analysis and the node input power. Compared with impedances required from load line analysis and calculation of efficiency show that the 4-stage Doherty PA is very suitable as power amplifier in this application.

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There are a number of people whitout whom this thesis could not have been written, with this I would like to express my gratitude towards their help.

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Contents

Chapter 1

Introduction

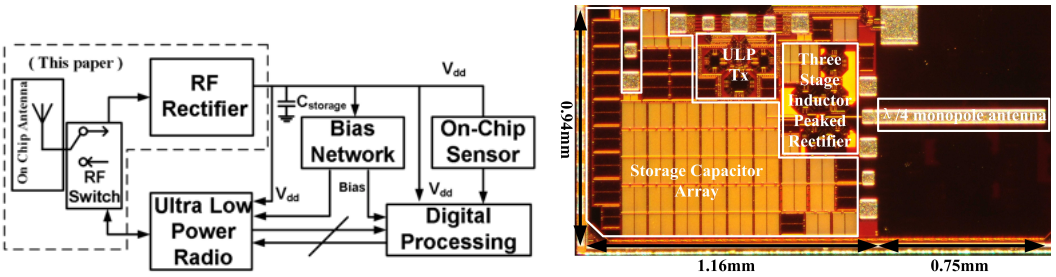
1.1 Problem Description

Recently wireless sensor networks based on ultra-low-power architectures have received a lot of attention. These sensor nodes should have the following properties:

1. Small feature size. This is better to achieve at high frequencies, i.e. 60 GHz. At these frequencies antenna integration is possible due to small antenna sizes.
2. Low maintenance. The sensor node has to be able to operate for a very large period of time without maintenance. Battery-less operation is desired.
3. The production costs of these sensors must be cheap. When produced in CMOS the production costs is lowered.

Therefore these sensor networks require reliable, battery-less, miniaturized, low-cost sensor nodes. An RF-power source is a reliable source to power these sensor nodes.

Within the Mixed-signal Microelectronics group a CMOS integrated 60 GHz battery less temperature sensor has been developed. Figure 1.1 shows a block diagram and die photograph of this sensor. The temperature sensor has the ability to harvest energy wirelessly from an RF source in order to charge itself and conduct a temperature measurement. The temperature of the sensor node will be determined by the frequency of the integrated Local Oscillator (LO) of the sensor tag. This LO signal is is transmitted back to the base station. Thereby the frequency of the received signal is a direct measure of the node temperature.



(A) Sensor block diagram [1]. (B) Sensor die photograph [2].

FIGURE 1.1: Sensor node.

The charging of the sensor node is currently done with lab equipment, the ultimate goal is to develop a base station that is capable of eliminating the use of this lab setup. Together with various sensor tags this base station will be capable of reading the temperature, humidity, etc. in a room. This setup is depicted in Fig. 1.2. The base station has a phased array antenna that has the capability to create a pencil shape beam. These pencil shaped beams make it possible to direct the power sent from the base station into the direction of the nodes. In this way a higher power density is incident on the node and the charging of the node is more efficient.

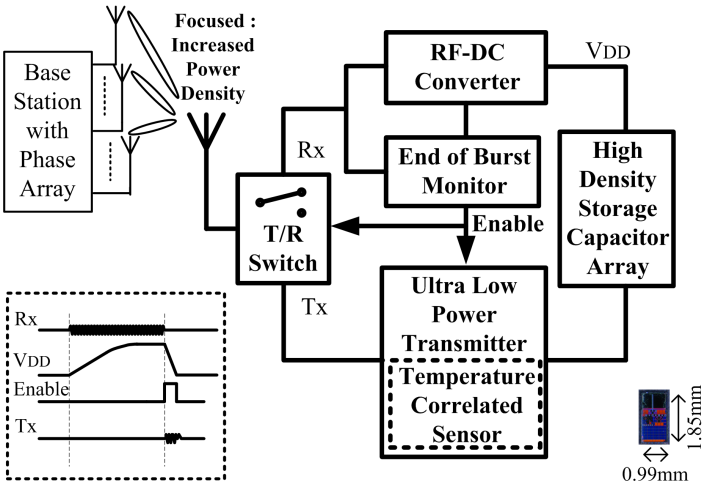


FIGURE 1.2: System overview [2].

The idea is to deploy the sensor in a domestic environment, e.g. in paint or wallpaper amongst others, so that the sensor tags are placed at arbitrary positions throughout the room. The base station will then, with the help of a pencil shaped beam coming from the phased array, scan for and charge the sensor nodes.

Within the base station a power amplifier (PA) resides that ensures an appropriate amount of power is emitted so that the target devices can be charged and read out. The

work done in this project is based on a literature study of [3] where the state of the art of 60 GHz PAs is investigated and compared. With this state of the art research it is clear where the boundaries are with regard to metrics such as output power and power added efficiency.

1.2 Aim of the thesis

The aim of this thesis was initially to develop a high output power PA that together with a phased array has the capability of charging the sensor nodes. During the system analysis of this PA it became clear that such a system would emit more power than allowed by the rules and regulations set by each country. Therefor the aim of the thesis has been redefined:

1. The system design of the base-station to sensor node power transfer.
2. The architecture and initial design of the base station PA.

1.3 Scope

The work presented in this thesis focuses on the system design of a wide output power range high efficiency 60 GHz PA. This system design aided by circuit design forms the first building block of the base station. The other components such as phase shifters and mixers amongst others that make up the rest of the base station fall outside the scope of this thesis.

1.4 Outline of this thesis

In this work a system design of the base station to sensor node power transfer is realized. Based on this design a 60 GHz 4-stage Doherty PA system is designed based on the current state on the art. The outline of this thesis is briefly explained here:

In chapter 2 the PA is briefly explained together with the main design specifications such as: Output power, bandwidth, power gain, efficiency and the 1-dB compression point. These specifications together with the specifications coming from the sensor node form the initial PA specifications formulated in this chapter.

Since these specifications were far from complete at the beginning of this thesis, a system design is started to specify the remainder of the specifications (chapter 3). In this chapter

the system is divided into two parts, the array and the power amplifier. In the system design of the array the rules and regulations, array diffraction patterns, received power and array size trade offs are investigated.
Based on these investigations the system design of the PA is started. The main trade offs that are investigated are:

1. High output power vs. a wide output power range.
2. Efficiency and complexity of various topologies.

Out of three topologies the Doherty PA architecture is chosen and investigated in detail. The chapter is concluded by the completed list of specifications.

Based on this system design with specifications a circuit design is started. This is described in chapter 4. This circuit design covers the chosen structure together with the general unit PA topology that form the Doherty PA architecture. Based on this general topology the carrier, peaking 1, peaking 2 and peaking 3 PAs are designed. Of these PAs the carrier and peaking 1 PA are partly designed. Both PAs consist out of a two-stage cascade, a third stage still needs to be added in order to fulfill the power gain requirement. This design stage is not completed since the aim of the system design phase of this project shifted from high output power to a wide output power range during the project. For that reason there was not enough time to do both the complete circuit design and system design.

The conclusions and recommendations are formulated in chapter 5. This chapter summarizes the conclusions and recommends future research in order to successfully design this PA. The chapter is concluded by an evaluation of the thesis.

1.5 Own contributions

This work has new contributions on two levels. First, the system analysis of the power transfer between the base-station and the nodes, taking the regulations into account has been done for the first time. This has resulted in the system specifications of the base station as well as to future recommendations on new sensor node requirements.
Secondly, a 60 GHz 4-stage Doherty PA system based on the current state on the art is proposed. To the authors knowledge up to the point of writing there is no 60 GHz 4-stage Doherty PA published yet.

Chapter 2

PA metrics

2.1 PA

The purpose of a Power Amplifiers (PA) in the RF-path is to increase the power level of the signal at its input to a defined power level at its output. This signal is transmitted via the antenna and optionally a phase shifter to the target devices. It is the task of the PA to ensure that sufficient output power is generated. The main design specifications for PAs are its output power, frequency, bandwidth, power gain, efficiency (PAE) and 1-dB compression point.
These specifications are in conflict with each other, hence the design of a PA is the result of the trade-off in trying to fulfill these requirements.

2.1.1 Output power

The output power is an important design specification in PA design.

$$P_{out} = \frac{1}{2} I_{out} V_{out} \tag{2.1}$$

The power delivered at a specified operating frequency to an external load, usually 50 Ω, is determined. Common methods achieve this are based on load-pull or conjugate matching together with transistor sizing. These methods consist of providing an appropriate load impedance at the output of a transistor to match it to the external load of the device.
Both matching techniques have their advantages. The conjugate match will have a higher gain at the cost of a lower maximum output power. The load-pull match will have a larger output power at the cost of a lower gain. These effects are depicted in Fig. 2.1.

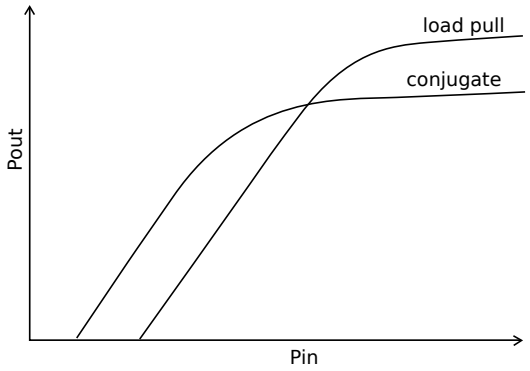


FIGURE 2.1: Output power based on matching.

Designing matching networks, especially if a wide band match is required, can be a challenge. In general the fundamental operating frequency determines the type of matching network. So are for example transmission lines a sensible choice at high frequencies, because the lengths of transmission lines are shorter for high frequencies than for low frequencies in matching networks. At low frequencies lumped components can be chosen to minimize the device size. The networks can thus consist out of lumped components, transmission lines or transformers.

2.1.2 Bandwidth

At 60 GHz the allowed bandwidths range from 2.5 GHz in Japan to 9 GHz in Europe [4]. This means that if a bandwidth of 2.5 GHz is used the system is allowed to operate globally. The focus of the base station lies on charging the sensor tags. This means that the sensor tag needs to be located and then charged with a sufficiently high RF power. When a wide band signal is chosen to charge the sensor tag a high data stream can be send. However to charge a sensor tag with enough RF power a wide band signal is not necessary. For charging purposes a narrow band signal is more convenient since the power transmitted is more concentrated to a smaller bandwidth resulting in higher voltage swings. Furthermore no communication bandwidth is used and alleviates the complexity of the matching network for the PA.

2.1.3 Power gain

Power gain is defined as the ratio between input and output power.

$$G_P = \frac{P_{out}}{P_{in}} \tag{2.2}$$

The power gain of a PA depends on several aspects. These aspects are the size of the transistor which determines the maximum unity gain frequency, f_t, of the short circuit current gain. The maximum oscillation frequency f_{max} which specifies the practical upper bound for useful circuit operation. Furthermore, the biasing of the PA which determines in which class the PA operates.
F_t and f_{max} are parameters that can only be influenced by the transistor size and technology. The biasing can actively manipulate the power gain of the PA. So is the power gain of a transistor biased in class-A about 6 dB higher than the same transistor operating in class-B [5]. This is because the conduction angle of the drain current in a class-A biased transistor is 360° while a transistor biased in class-B has a conduction angle of 180°. Therefore the transconductance of in class-B is only half of that in class-A resulting in 6 dB less power gain. This can schematically be seen in Fig. 2.2.

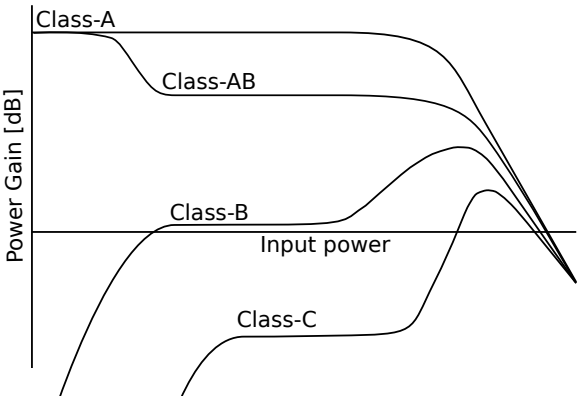


FIGURE 2.2: Power gain.

2.1.4 Efficiency

The need of high output power levels is the main drive in the selection of active devices composing the PA. To limit the overall power consumption and increase efficiency, power amplifiers are typically operated in such a way that they fully swing from rail to rail. If this efficiency is not of importance a sufficiently large device can be selected, resulting in more linear behavior while the device dissipates large amounts of DC power [6].
The efficiency can be considered in two ways, one is the drain efficiency where the whole output power is considered.

$$\eta_{drain} = \frac{P_{out}}{P_{DC}} \tag{2.3}$$

The second is the Power Added Efficiency (PAE) where the input power is subtracted from the output power to get a more honest representation of the PAs efficiency.

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out} - \frac{P_{out}}{G}}{P_{DC}} = \eta_{drain}\left(1 - \frac{1}{G}\right) \tag{2.4}$$

The maximum of these efficiency points will be reached when the PA is operated in saturation and has maximum voltage and current swing in combination with minimum DC power consumption.

2.1.5 1-dB compression

The majority of PAs has a fixed gain for a set frequency range. When the output power is compared with the input power a linear relation can be observed i.e. the amplifiers gain. As the input signal increases in power the PA starts to saturate causing the gain to compress and deviate from the linear slope. As soon as this deviation from the linear slope has reached 1-dB the 1-dB compression point is reached. If the input power then increases more the gain flattens and the amplifier becomes more nonlinear and produces harmonics and signal distortion.
This 1-dB compression point has become a representative number in the determination of linearity of the power amplifier.

2.2 Specifications

Since the sensor tags are placed at various places across the room, the location of the sensor tags is not known beforehand. So the base station has to be capable of scanning to reach the sensor tags with sufficient power. The RF-signal that is received by the sensor tag also needs to be strong enough to charge the target device.
Since domestic rooms have a large diversity in shapes and sizes, the system needs to be able to operate in most domestic situations. It is therefore necessary to have a system that can operate at various distances, at maximum 10 m, while the target devices remain to be charged. At these distances it must be able to charge as many as possible individual target devices present in the room.

From the measurements of the current sensor node of the Premiss project, the input power required for charging of the node, as well as the charging time are known. With future improvements of the sensor node, lower required power levels are targeted. The base station thus needs a power amplifier that is able to power the current target device with the following specifications. At the start of the project only the specifications of

the sensor tag, in order to charge itself, are known. These specifications are given in Tab. 2.1.

Specification	
Received Input power	5−7 dBm
Charging time	4.1 ms[1]
Discharging time	7 μs[1]

TABLE 2.1: Target specifications [2, 7, 8].

Based on these sensor specifications the specifications of the PA in the base station can be formulated. Since the sensor tag needs to be located and charged only, communication is not of concern at this moment so the bandwidth can be narrow band. The linearity is therefore not of concern in this project. The specifications are given in Tab. 2.2. Specifications such as output power, power gain, input power, and PAE were not specified at the beginning of this project. A system study had to be done in order to determine these specifications (Chapter 3).

Specification	Initial specifications
Operating frequency	60 GHz
Power received at target	5 dBm
Operating distance	$0 - 10$ m
Technology	40 nm CMOS
Output power	T.B.D.
Power gain	T.B.D.
Input power	T.B.D.
PAE	T.B.D.
Linearity	-
Bandwidth	narrow

TABLE 2.2: Design specifications.

In this thesis the system design (Chapter 3), circuit design (Chapter 4) and recommendations (Chapter 5) for future projects are described. During the system design it will become clear what values the output power, power gain and efficiency will need to have.

[1]The charging and discharging times are extracted from the 71 GHz wireless temperature sensor. These charging and discharging times are also assumed in the 60 GHz case.

Chapter 3

System design

Locating and charging sensor nodes individually is challenging. With an omnidirectional antenna a very high power needs to be transmitted to charge the sensor tag. Also beam steering to charge individual sensor nodes independently is impossible with an omnidirectional antenna.
Allowing beam steering by using an array increases the directivity of the base station. The beam directs the transmitted power to allow independent charging of the sensor nodes. This focus is strongly dependent on the array size.
Until now most attention was given to the development of the sensor node. The system design of the power transfer between the base station and the sensor nodes is the basis for deriving the specifications of the base station. This includes the requirements for the phased array antenna as well as for the power amplifiers.
In order to find the correct specifications with the PA inside the phased array of the base station an analysis of the array and PA need to be conducted. In paragraph 3.1.2 the diffraction patterns of different arrays are investigated in order to determine the resulting spot size, scanning time and whether the node lies in the far or near field. Paragraph 3.1.1 investigates the rules and regulations set by different countries. Based on these rules and regulations the optimized power transfer conditions can be determined so that the system can be deployed in as many countries as possible. Based on these rules and regulations, together with free space path loss formula the maximum operating distance of different array sizes is determined in paragraph 3.1.3. On this basis trade offs between large element and small element arrays are elucidated in paragraph 3.1.4.
Based on these array analyses the system design of the PA can be made. In Appendix D it is concluded that a high output power PA is not a good starting point for the system due to rules and regulations. It is shown that a PA with a wide output power range at high efficiency is a better choice (paragraph 3.2.1). In this paragraph a topology selection is made out of several suitable topologies. Based on the selected topology, a

multistage Doherty PA, the operation principle is investigated. Based on this investigation further analysis in back off output power is conducted by assessing two multi-stage Doherty PAs. One of these PAs is selected and its transmission line matching network, load modulation, power contribution of the several PAs and efficiency of the chosen topology is analyzed.
The result of my work presented in this chapter is concluded in paragraph 3.2.3 where the missing specifications that where found during the system design are filled in. These results are the input for the next chapter that focuses on the circuit design of the PA.

3.1 The impact of the array

The number of antenna array elements has a significant impact on the directivity, beam steering and scanning time amongst others. In this section, these parameters will be analyzed in the specific context of the power transfer from the base station to the sensor nodes. From this investigation design decisions for the power amplifier and overall system can be made.

3.1.1 Rules & regulation

This section discusses the worldwide regulation for the 60 GHz band. An overview in bandwidth and transmit power is given to give more insight in the operating ranges in countries across the world. Also the antenna gain and Equivalent Isotropically Radiated Power (EIRP) play a significant role.
These three parameters are related but have different specs. Therefore, in most cases, it is sufficient to meet two of the three specifications in order to comply with the rules and regulations.

Antenna gain

Antenna gain is a figure that describes the directivity of the antenna. The antenna gain specifies how well the antenna converts the power put in into radio waves transmitted into a certain direction.
The antenna gain is dependent on the number of antenna elements in the array. When the antennas are all powered with the same in phase signal, the electrical and magnetic fields of these antennas will all have the same phase in forward direction. Because the fields of these signals are all in phase they will add up resulting in electrical and

magnetic fields that are N times higher than that of a single antenna. Here N is the number of antenna elements. The power transmitted then increases quadratically, so with an increase of N antenna elements the antenna gain increases by N^2 with regard to an omnidirectional antenna [9].
This is convenient since the same power can be reached with lower input power in the case of an antenna array. Antenna gain of an array is quantified by:

$$G_{array}\ [dBi] = 10 \log_{10}(N) \tag{3.1}$$

Equivalent isotropically radiated power

EIRP is the power density of an array that corresponds to the amount of power that is transmitted by an omnidirectional antenna on the same distance, frequency and receive antenna. EIRP is quantified by:

$$EIRP\ [dBm] = P_T + G_{array} \tag{3.2}$$

here P_T is the transmit power of the total array in dBm and G_{array} the antenna gain of the array in dBi.
A phased array with an EIRP of 40 dBm generates the same received signal with less transmit power as an omnidirectional antenna with 40 dBm transmit power [9].
The transmit power for an array with an EIRP of 40 dBm is dependent on the antenna array size. If the array consists out of 1000 elements the antenna gain is 30 dBi. For the same received transmit power in the forward direction, the transmit power reduces from the 40 dBm of the omnidirectional antenna to 10 dBm for the entire array.

Transmit power

The transit power is the total output power of the array. It also describes the power that remains when the antenna gain is subtracted from the EIRP.

$$P_T\ [dBm] = EIRP - G_{array} \tag{3.3}$$

If the EIRP is limited, an increased antenna gain requires a reduction in the transmit power.
If the antenna gain is e.g. 30 dBi. This corresponds to 1000 times more power on the receiver antenna as in the same setting with an omnidirectional antenna. The total transmit power is thus focused 1000 times better than that of the omnidirectional antenna [9].

As in the previous section (*Equivalent isotropically radiated power*) already is calculated, the transmit power for a 1000 element array with 40 dBm EIRP is set to 10 dBm for the entire array.

Transmit power per antenna element

The transmit power described in the previous section specifies the transmit power for the entire array. The transmit power per antenna element is derived by dividing the array transmit power by the number of array elements.
In the previous example of a 1000 element array, with 40 dBm EIRP, 30 dBi antenna gain and 10 dBm transmit power the element power can be calculated as follows. The total transmit power of the array needs to be divided over the array elements. This means that the 10 dBm transmit power needs to be divided over 1000 elements, or equivalently the antenna gain needs to be subtracted again from the transmit power:

$$Element\ power\ [dBm] = EIRP - 2G_{array} \tag{3.4}$$

so for the array of the example each element needs to have an output power of -20 dBm.

Regulations summarized

The bandwidth, transmit power, EIRP and antenna gain regulations differ worldwide. In Tab. 3.1 a summary of the regulations is given for a number of countries. It's advantageous if the system can be deployed in as many countries as possible. This means that the most stringent rules per specification apply in order to support this deployability. Korea has very strict regulations, which make it improbable that such a system would be feasible there. Therefore Korean specifications are excluded from this discussion. Without this country the system is allowed to have a maximum antenna gain of 30 dBi, maximum EIRP of 40 dBm and a maximum transmit power of 10 dBm. Note that the EIRP has only a 40 dBm average limitation in the USA/Canada. However 40 dBm is maintained as maximum. This is because the EIRP, transmit power and antenna gain are dependent on each other. With a maximum of 10 dBm transmit power and 30 dBi antenna gain one can only have a maximum of 40 dBm EIRP. This is to guarantee the safety of the eyes. As more than 40 dBm power can potentially harm the human body. The antenna gain does not specify any power contribution but does have the ability to focus the power coming from the elements to a certain spot.

Region	Unlicensed bandwidth (GHz)	Transmit power	EIRP (dBm)	Maximum antenna gain (dBi)
USA/Canada	7.0	500 mW or 27 dBm (max)	40.0 (ave) 43.0 (max)	33.0 (max) when 10.0 dBm TX power is used
Japan	7.0[(1)]	10 mW or 10 dBm (max)	58.0 (max)	47.0
Korea	7.0	10 mW or 10 dBm (max)	27.0 (max)	17.0
Australia	3.5	10 mW or 10 dBm (max)	51.7 (max)	41.8
Europe	9.0	20 mW	57.0 (max)	30.0

TABLE 3.1: Legislation overview [4].

3.1.2 Fraunhofer far-field diffraction

With the rules and regulations known the first thing that is worthwhile to investigate is the impact of the number of array elements on the transmitted beam pattern. This investigation can be done with an analysis of the diffraction of the RF-signals from the array. Diffraction is the phenomenon described as the bending of waves around small obstacles and the spreading of waves through small openings. This wave spreading is depicted in Fig. 3.1.

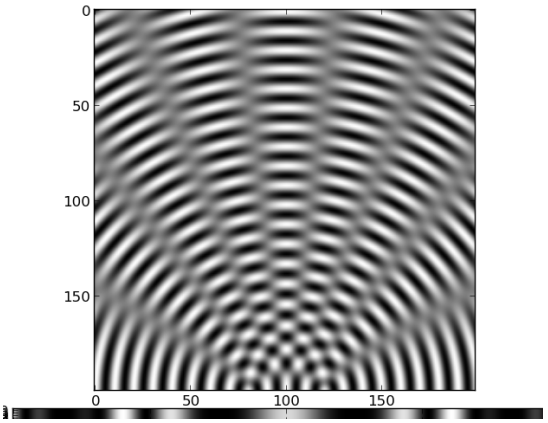


FIGURE 3.1: Schematical representation of double slit diffraction pattern [10].

The diffraction pattern is determined by the number of slots, their size, distance and the wavelength of the signal. Together these factors contribute to the beam width i.e. the angular width of the most dominant beam. The intensity distribution is given by

[1]Maximum bandwidth allowed is 2.5 GHz.

[11]:

$$I_\Theta = I_0 \frac{sin(\beta)^2}{\beta^2} \frac{sin(N\gamma)^2}{N^2 sin(\gamma)^2} \tag{3.5}$$

where

$$\beta = \frac{\pi w sin(\Theta)}{\lambda} \tag{3.6}$$

and

$$\gamma = \frac{\pi d sin(\Theta)}{\lambda} \tag{3.7}$$

Here N is the number of antenna elements, I_0 is the starting intensity, λ is the wavelength, Θ the angle in radians, w the slit width and d is the slit spacing.
With Eq. 3.5 the effect of the number of antenna elements on the diffraction pattern can be analyzed. The beam width decreases as the number of array elements increases. Figure 3.2 shows such a diffraction pattern for a 10 element linear antenna array, spaced at $\frac{\lambda}{2}$ distance. It can be observed that the beam width at full beam width for this array is 0.2 rad or 11.5°.

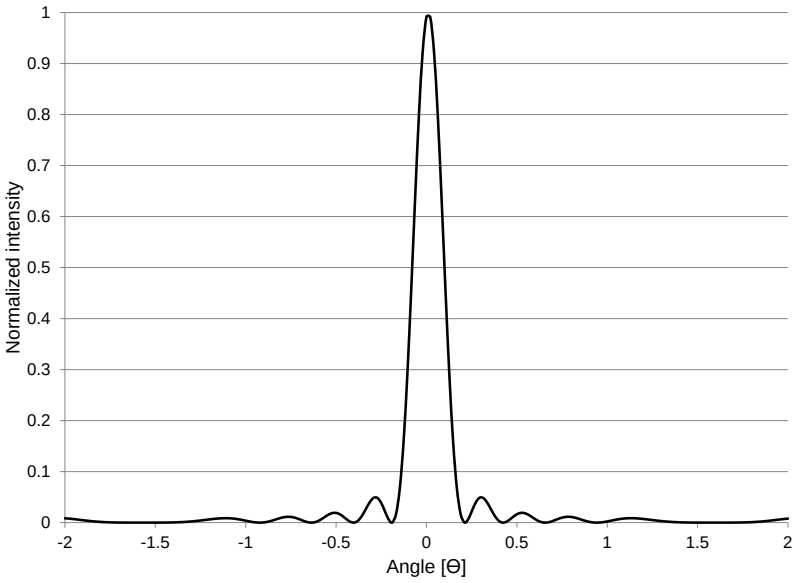


FIGURE 3.2: Normalized diffraction pattern of a 10 element linear array.

Spot size

Since every array has a different diffraction pattern, thus a different beam width, the spot diameter at a certain distance can be calculated. Figure 3.3 shows the spot diameter as a function of the beam-opening angle at a distance of 10 m.
Mathematically the diameter of the beam at a distance d is determined by the beam opening angle θ_{beam} is given by:

$$Spot\ diameter = d \tan(\theta_{beam}) \tag{3.8}$$

where θ_{beam} is the beam opening angle in degrees, the spot diameter and distance have meters as unit.

As the antenna array is built out of discrete elements only discrete values of θ_{beam} can be realized in practice. Figure 3.3 compares the actual beam diameter and beam opening angle of an NxN array to the calculated beam diameters from Eq. 3.8. It can be concluded that the granularity of the spot size gets finer with larger antenna arrays. However at a distance of 10 m, spot sizes cannot have a width much smaller than 65 centimeter. This is because the antenna gain of an array is not allowed to exceed 30 dBi in Europe, which corresponds to a 1000 element array. Since a 31x31 array already has 961 elements. The spot size diameter of this array is approximately 65 centimeter. This forms the lower bound, because increasing the array to 32x32 would exceed the maximum allowed number of elements, in terms of spot size diameter and an upper bound in terms of maximum square antenna array.

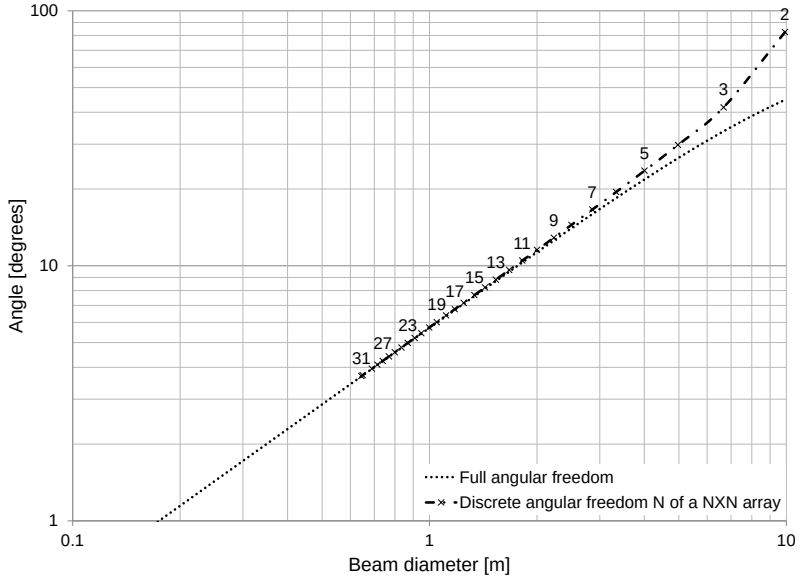


FIGURE 3.3: Spot size and spot angle at a distance of 10m.

Scanning time

Another interesting analysis can be made in the time it takes to scan a room. If for ease of analysis the assumption is made that the spot size can be made arbitrary small. When a room is scanned and every spot is lit for 5 ms [2] to charge the node[(2)] it can be calculated how long it takes to scan a room where it is not known where the target nodes are:

[2]With this analysis only the charging time of the node is taken into account. In reality a 7 μs [2] waiting period needs to be added per scanning spot to read out a potential node.

$$Scanning\ time\ [min] = \left(\frac{180}{angular\ step}\right)^2 \frac{5 \cdot 10^{-3}}{60} \tag{3.9}$$

Figure 3.4 shows this scanning time in combination with the spot size. The analyses assumes that the base station is in the center of the room and it has 180° of freedom in the X direction as well as in the Y direction at a distance of 10 m. The spot sizes range from the smallest spot possible i.e. 1 mmx1 mm[3] to 1 m. It can easily be observed that a spot size from 1 mmx1 mm is not a realistic spot size since it would take 57 days and 2.8 hours to scan a room at such a small granularity. A small spot size has a great directivity and can charge individual targets that are very close to each other without charging the surrounding nodes, but it takes extremely long for a full scan.
When more realistic spot sizes, i.e. sizes larger than 65 centimeter, are taken in consideration the scanning time is reduced drastically. With a spot size of 65 centimeters it takes approximately 14 seconds to scan for and charge the nodes in the room.
This is the maximum scanning time for the entire room. When the nodes are located in the environment their position can be saved. The next time a node is then accessed the base station aims the beam coming from the array directly at the node reducing the scanning time drastically.

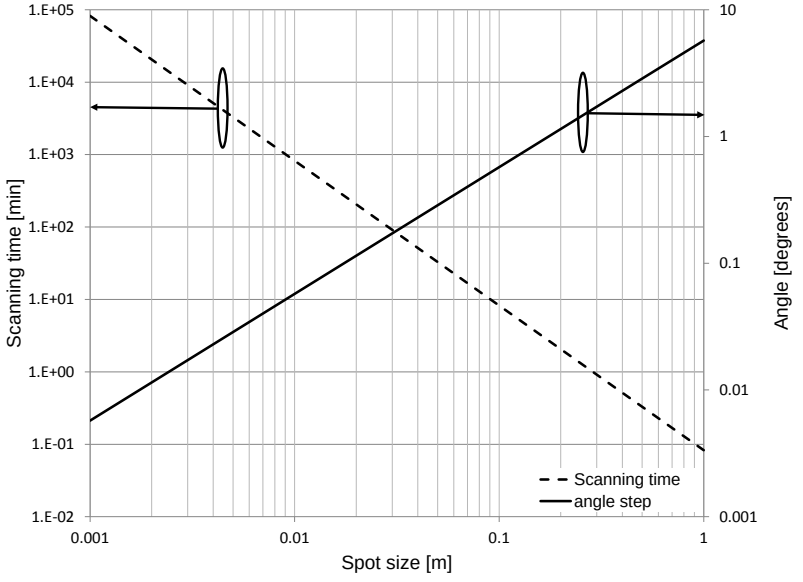


FIGURE 3.4: Scanning time, scanning angle and spot size at 10 m.

Near-field or far-field

The size of the antenna array has influence on the near- and far-field. Because of this influence the distance of the nodes and array size distinguishes if the node lies in the

[3]Since the target device has a size of approximately 1 mmx1 mm

near or the far-field of the base station. The diffraction analysis made earlier in this chapter assumes that all nodes lay in the far-field region. When this is not the case the diffraction analysis does not apply anymore and a near-field analysis needs to be conducted. This however is outside the scope of this thesis and should be analyzed in future research. It is on the other hand interesting to know where the far-field is situated.

The distance R at which the far-field distribution is valid is given by:

$$R \geq \frac{2D^2}{\lambda} \tag{3.10}$$

Where D is the antenna array size:

$$D = \lambda\frac{1}{2}(N-1) + \lambda\frac{1}{4}N \tag{3.11}$$

So

$$R \geq 2\lambda\left(\frac{1}{2}(N-1) + \frac{1}{4}N\right)^2 \tag{3.12}$$

and

$$\lambda = \frac{c}{f} \tag{3.13}$$

Here R is the distance to the antenna array in meters, c the speed of light i.e. $3 \cdot 10^8$, N the number of antenna elements in a NXN array and f the operating frequency i.e. 60 GHz.

Figure 3.5 shows the far-field distance as a function of the array size. Interesting is that the far-field starts at relatively large distances. It can be observed that the far-field distance for an array of 31x31 elements is at 5.5 meters.

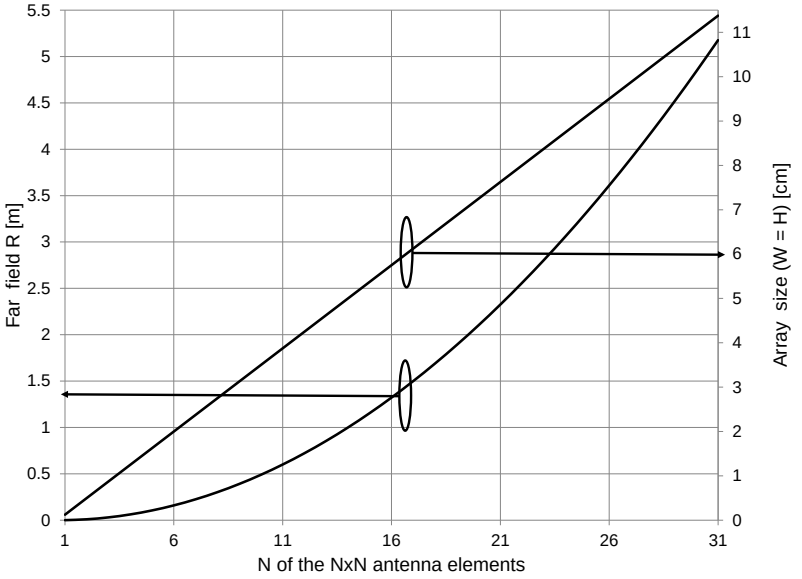


FIGURE 3.5: Array size and far-field distance.

3.1.3 Received power

To fully charge the current target node, an input power of at least 5 dBm [7] is needed. Since the legal limit in the USA/Canada for the EIRP of the transmitter is set at 40 dBm, the maximum distance to charge the target device is limited.
This limitation is given by the Friis transmission formula and it relates the free space path loss, antenna gain and wavelength to the received transmit powers.

$$\begin{aligned} P_r &= P_t + G_t + G_r + 20\log_{10}\left(\frac{\lambda}{4\pi R}\right) \\ &= P_t + G_t + G_r + 20\log_{10}\left(\frac{c}{4\pi R f}\right) \end{aligned} \tag{3.14}$$

From this equation it can be observed that for the same receive and transmit gain and transmit power more power is lost as the frequency increases. At 60 GHz this is an apparent problem when 5 dBm power needs to be received.

When the legislation in transmit power, EIRP and maximum antenna gain are taken into consideration the distance can be calculated where 5 dBm input power can be received. This is depicted in Fig. 3.6. From the graph it can be concluded that the maximum distance that the target can be spaced from the array is approximately 2 cm[4] with an array of 1000 elements.
The legislation in transmit power, EIRP and maximum antenna gain in combination with a needed input power to charge the target severely limits the operation distance of the system. This will result in that the overall system does not meet the required specifications. Improving the operating distance of the system, so that the 10 m distance requirement is met means, that some of the before mentioned metrics need to be changed. Because the transmit power, EIRP and maximum antenna gain are requirements set by governmental legislation the only variable that can be altered is the input power that is needed. If a distance of 10 m is needed the target device needs to be able to at least have an input power of -48 dBm or lower to fulfill the system requirements.

[4] To be more exact this distance would be 2.23 cm.

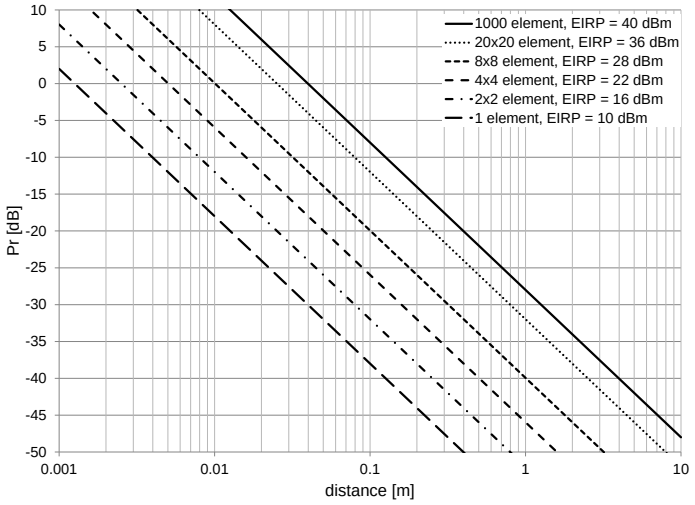


FIGURE 3.6: Received power for different array sizes at 60 GHz.

3.1.4 Array size trade offs

In the preceding sections the impact of the array size on the spot size, scanning time, path loss and the far-field distance became apparent. These are not the only factors that need to be taken into consideration when choosing an array size. So may the array size have consequences on the element power i.e. the output power of the driving PA. With a small array this driving power needs to be much higher making the design of such a PA more challenging than with a large array. On the other hand a large array reduces the PA complexity but increases the array assembly complexity and phase-shifter complexity. These factors are summarized and listed in Tab. 3.2.
Also a large array is more expensive because it needs more PAs, phase shifters, antennas and surface area. A possible solution to decrease some of these costs is to create PAs that can power multiple antenna elements.

trade offs	Low N	High N
EIRP	$<$ 40 dBm	$\leq$40 dBm
Element power	↗ ☹	↙ ☺
scanning time	↙ ☺	↗ ☹
Resolution/spot size	↙ ☹	↗ ☺
assembly complexity	↙ ☹	↗ ☺
PA complexity	↗ ☺	↙ ☹
Flexibility	↗ ☺	↙ ☹
Size	↙ ☺	↗ ☹
Application	T.B.D.	Premiss
Phase-shifter complexity	↙ ☺	↗ ☹
Cost	↙ ☺	↗ ☹

TABLE 3.2: Design specifications.

3.2 The power amplifier

Based on the array analysis from the previous paragraph, a system analysis of the power amplifier can be made. This section describes the system analysis for a high power, high efficiency PA with a large output power range.

3.2.1 Wide output power range constant efficiency

Since the output power of the system in previous section is too large, the power output determination needs to be revisited. During this analysis it will become clear that it is more desirable to design a PA that is capable of supporting multiple array sizes to increase the system flexibility.

Output power for a worldwide system

Since the transmit power can't exceed 10 dBm an analysis needs to determine the PAs output power. In this power determination, that is depicted in Fig. 3.7, the array output power remains constant at 10 dBm to accommodate almost global deployment. The EIRP in this case is dependent on the antenna gain and output power per element. The problem that arises with the 10 dBm array power is that only at a 1000 element array 40 dBm EIRP is achieved. For prototyping situations such a large array is inconvenient and a smaller array is more practical. This means that the power amplifier needs to be able to support a range of array sizes with high efficiency. Creating a new PA every time a new array size is needed is practically not feasible.
Attaching multiple elements to a single high output PA causes the design complexity of the array to increase drastically, since all signals need to arrive in phase at the antenna elements. The large PA needs to be optimized for higher output powers. For smaller output powers, or when larger arrays are powered with the same PA, the PA needs to be driven in back-off power. This will deteriorate the efficiency of the PA. Especially with large arrays this problem becomes more evident, since more PAs operate with bad efficiency.
The need for a PA that is capable of an output power range to support an abundance of array sizes with high efficiency is evident. If this PA is capable of supporting an output power range from -20 to 0 dBm at constant PAE of approximately 15%, array sizes ranging from 9 to 1000 elements can be realized. Such a PA increases the flexibility greatly.

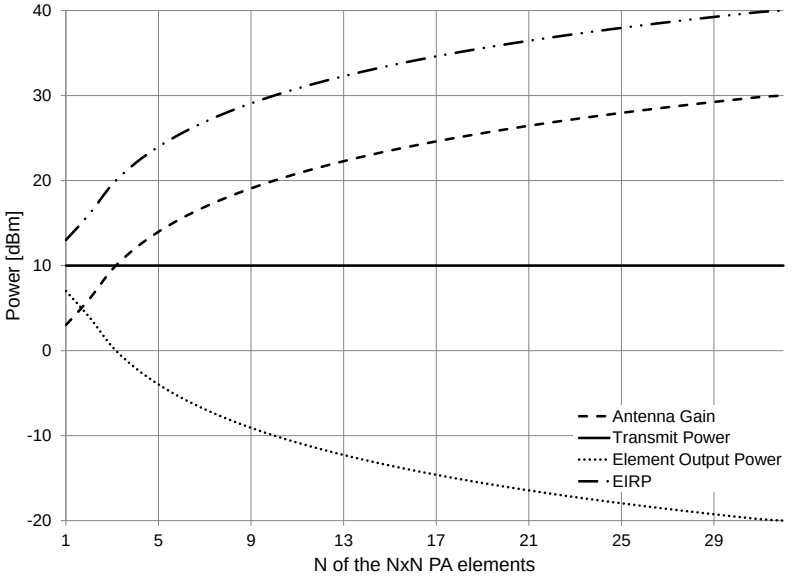


FIGURE 3.7: Power per element based on the array size.

PA topology

In order to design a PA that is capable to generate output powers ranging from -20 to 0 dBm at approximately 15% PAE a suitable topology needs to be selected. Three topologies are considered. With each topology having its own strengths and weaknesses a comparison is made between the topologies to select the best candidate for this application.

Single cell PA

The first candidate is a single cell PA that is capable of achieving the output power range by driving the PA at back-off power. As mentioned in previous paragraph this negatively affects the efficiency. To overcome this and maintain constant efficiency an adaptive load can be implemented. This adaptive load consists out of multiple loads that maximize voltage and current swing so that the efficiency at several back-off power levels is maximized. To realize this load adaptation a switching network is necessary to load the PA with the right matching network at the selected back-off power.
However the size of the PA needs to be large enough to accommodate the high output power regions. This means that the parasitics, that are larger for larger devices, remain large even for low output powers, deteriorating the PAE.

The challenge for this topology is the maximization of the voltage swing at the back-off power levels in order to maximize efficiency. Multiple loads need to maximize this

voltage. If a maximum voltage swing of 0.46 V[5] for a common source stage is assumed. With this voltage swing, when a purely resistive load is assumed, the load needs to have an impedance of approximately 100 Ω at 0 dBm output power and approximately 100 $k\Omega$ at -20 dBm output power. However the magnitude of the drain source resistor of the transistor plays a major role in the PA efficiency at back-off output powers. A first order approximation of this resistor is to simulate and calculate it from the Y-parameters [12].

$$R_{ds} = \frac{1}{real(Y_{12}) + real(Y_{22})} \tag{3.15}$$

For a PA that is capable of 0 dBm output power this drain source resistance is approximately 5 $k\Omega$. This means that the load at this power level is dominant. At a power output of -20 dBm the drain source resistance is dominant over the load causing a drop in efficiency. At back-off powers the PA efficiency will drop from ≈ 20% to 1% or 2%. This drop in efficiency at back-off powers makes the single cell PA not a suitable candidate.

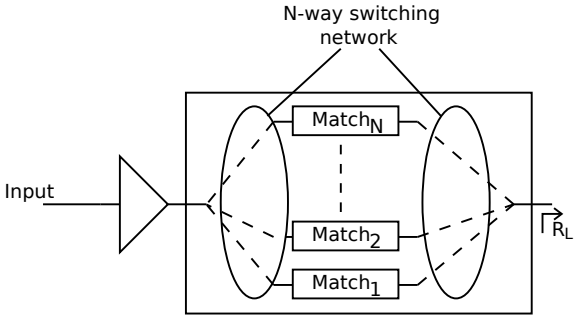


FIGURE 3.8: Single cell PA topology.

Distributed active transformer

The Distributed Active Transformer (DAT) topology combines the power coming from multiple PAs with a transformer. The DAT uses a multistage transformer that acts as power combiner and also modulates the load seen by each unit amplifier. The advantage of using a DAT to combine the powers of the different PAs is that differential unit PAs can be used in the design. This results in virtual grounds between the active devices that eliminates large currents running through the substrate.

The overall system operates by switching the power cells on and off according to the desired output power [13]. In the high output mode i.e. 0 dBm all the active devices are turned on while in the lower power modes only certain cells are turned on [13]. Just as in the single cell PA the switching network adds undesired overhead, most likely reducing the overall PAE.

[5]With a $V_{ds,max}$ of 1.35 V, a $V_{DS,sat}$ of 0.42V and $V_{ds,DC}$ of 0.885 V the maximum voltage swing allowed is 0.465 V.

DATs share a common problem regarding the inequality of input impedances [14]. This inequality can occur between the values of differential input ports as well as between the individual nodes of those ports. Inequality in individual node impedances leads to unbalanced voltage swings at the output of differential amplifier stages. Impedance inequality in differential ports impose unequal voltage swings among the differential amplifier stages due to unequal load-line terminations [14].
Although the inequality of input impedances can be overcome, together with the overhead imposed to the system by the switches turning on or off the unit PAs make that the topology using a DAT seems not such a desirable candidate.

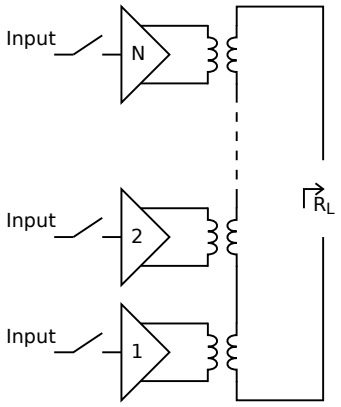


FIGURE 3.9: DAT PA topology.

Multistage Doherty
The multistage Doherty PA originates from the Doherty amplifier proposed by W. H. Doherty [15]. The Doherty amplifier uses an impedance transforming network to convert the load impedance seen by the PA. This impedance transformation network, different from most PAs, modulates the load in such a way that high efficiency is achieved at backed off power as well as at peak power [16]. The standard Doherty configuration consists out of a carrier PA and a peaking PA. Together these PAs form a back-off power of -6 dBm while maintaining high efficiency. This back-off power can be increased by adding two more stages so that a desired value of back-off power of 3·(-6)=-18 dBm is achieved.
Unlike the previous topologies the multistage Doherty PA does not rely on an overhead switching network to change the load or switch on or off the peaking PAs. The load modulation adjusts to the input power. The peaking PAs are biased in such a way that they turn on at the input powers where they are expected to be turned on, resulting in the desired output power and load modulation.
However because quarter wave transmission lines are used in the power combining network the PA size can become quite large. Also transmission lines have a small bandwidth. For wireless charging purposes this is no problem since a narrow band signal is

very suitable to charge a sensor node. When used for communication this could become more challenging as a larger bandwidth is possibly needed by the sensor node. Replacing the transmission line network by a distributed transformer can possibly solve this. Replacing this structure needs further investigation and falls outside the scope of this project.
The lack of a complex switching network together with the dynamic load modulation and high efficiency makes the multistage Doherty PA an interesting candidate for further investigation.

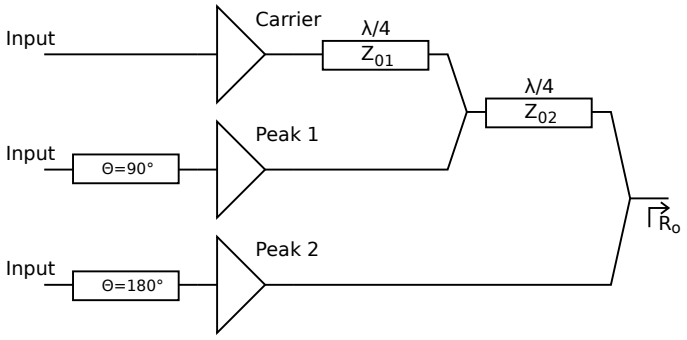


FIGURE 3.10: Multistage Doherty PA topology [17–20].

3.2.2 4-stage Doherty PA

Because of the advantages of the dynamic load modulation, the high efficiency at back-off powers and the automatic on and off turning of the peaking amplifiers the multistage Doherty is worth wile to investigate further. The investigation is described in this section and consists of a closer look at the topology, a load-line analysis to see what loads are needed, an investigation of the load impedances present at the output of the amplifiers looking into the power combining network, the comparison between the load-line analysis and calculated load impedances, a theoretical analysis in the efficiency of the 4-stage Doherty PA and an investigation of the power combining network.

Doherty principle

The Doherty amplifier in essence is composed out of 2 PAs and is primarily an efficiency enhancement technique. The two PAs illustrated in Fig. 3.11 have their own function. For large output powers, both devices contribute to the output power. When the output power goes below a certain value, the auxiliary amplifier shuts down and does not contribute to the total RF power anymore. This is typically at 6 dBm from the maximum composite output power when same size ratios are used for both PAs. So at back-off

output power lower than 6 dBm back-off, only one device is active which improves the efficiency of the complete amplifier.

Next to that, the Doherty amplifier uses dynamic load-pulling. This dynamical load-pulling causes that the carrier device can stay close to maximum efficiency. This happens in the upper 6 dBm of the output power range by maximizing the voltage swing. The load-pulling is caused by the current contribution to the load in combination with a $\frac{\lambda}{4}$ transmission line. A $\frac{\lambda}{4}$ transmission line has as property that it inverts the load impedance that terminates the transmission line. A higher load terminating the transmission line will be converted to a lower load looking into the transmission line. This can also be observed from the theoretical impedance transformation of the $\frac{\lambda}{4}$ transmission line of Z_{01} characteristic impedance:

$$Z_{in} = \frac{Z_{01}^2}{Z_L} \tag{3.16}$$

The load impedance Z_L seen by the transmission line is dependent on the current contribution of both amplifiers. The load is then:

$$Z_L = \frac{V_L}{I_c} = R_o \frac{I_c + I_p}{I_c} \tag{3.17}$$

This is where the dynamic load modulation sets in. As soon as the current from the peaking PA goes to the load the impedance seen by the transmission line increases. Because of the effect from the $\frac{\lambda}{4}$ transmission line the impedance seen by the carrier PA decreases. The impedance seen by the carrier PA is then:

$$Z_c = \frac{Z_{01}^2}{R_o \frac{I_c + I_p}{I_c}} \tag{3.18}$$

This effect will thus dynamically pull the load of the carrier down so that it maintains maximum voltage swing in the output power range higher than 6 dB back-off. This has as consequence that the overall efficiency of the Doherty PA increases and gets an extra peak at 6 dB back-off output power.

The $\frac{\lambda}{4}$ transmission line has a side effect that it shifts the phase of the signal coming from the carrier PA by 90°. To assure correct power combining the signals coming from the PAs need to be in phase. Phase correction is done by a phase shifter in front of the peaking PA ensuring in phase power combining.

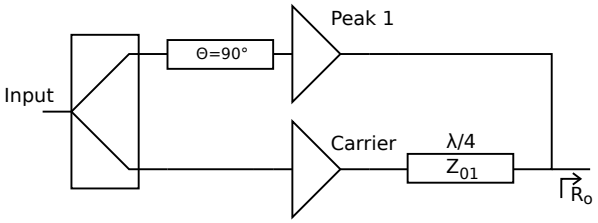
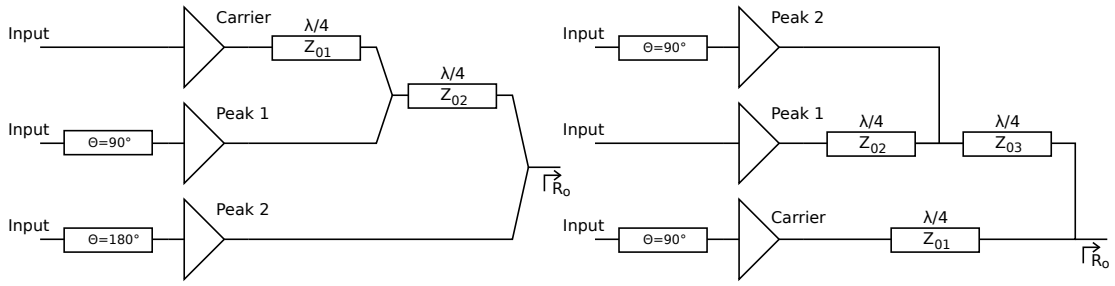


FIGURE 3.11: Doherty PA topology.

The Doherty architecture can be adapted to fit the needs of the specifications set for the PA. It is possible to expand the number of peaking amplifiers to increase the output power range. These peaking amplifiers are setup such that they turn on and off each at predefined regions. The expansion of the Doherty structure generally is done with one of two basic architectures. These architectures are shown in Fig. 3.12. Both architectures have advantages and disadvantages.

The Doherty-I architecture used in [17–20] is easily scalable to a N-stage architecture. A major disadvantage of this architecture is that at every even number of peaking PA a $\frac{\lambda}{2}$ or multiple of $\frac{\lambda}{2}$ transmission line increases the load instead of decreasing it. This is an undesired effect and causes loss in efficiency. In section *Load impedances* of this chapter this effect will be explained in more detail.

The Doherty-II architecture used in [9, 16, 21–23] uses a topology that is not easily scalable to an N-stage architecture. Figure 3.12b shows the three stage Doherty variant. Although it is inevitable that $\frac{\lambda}{2}$ transmission line paths will reside in higher N-stage architectures the effects can be shifted to other amplifiers. This is what is done with the Doherty-II architecture. The transmission line network is here setup such that there won't be a $\frac{\lambda}{2}$ transmission line path between the peaking PAs and the carrier PA. This makes sure that the voltage swing of the carrier will be maximized.



(A) Three-stage Doherty-I architecture. (B) Three-stage Doherty-II architecture.

FIGURE 3.12: Basic Doherty expansion architectures.

4-stage Doherty topology

The 4-stage Doherty power amplifier consists out of a carrier PA and three peaking PAs. The input signal is split to every PA, as shown in Fig. 3.13 [23][(6)]. Depending on the magnitude of the input signal the peaking PAs contribute to the output power and load modulation. The carrier PA remains always on and ensures that the first high efficiency point is reached at -18 dBm back-off power. The turning on of the peaking PAs dynamically modulates the load imposed by the transmission line power combining network so that maximum efficiency is reached again at -12, -6 and 0 dBm back-off power.

Maximum efficiency points are controlled by the load modulation caused by the power contribution of the individual PAs. When these PAs are set up such that the peak efficiency points are -18, -12, -6 and 0 dBm back-off power, high efficiency over the output power range is achieved. This means that the PAs need to turn on at different input magnitudes independently. Turning the PAs on and off is controlled by adjusting the biasing in such a way that each PA is switched on or off such that the back of output powers and peak efficiency points are met.

The quarter wave transmission line network modulates the load such that maximal current and voltage swings are reached at the specified back-off powers. The transmission line network causes phase shifts in the signal coming from the PAs. This phase shift needs to be compensated for, to ensure in phase power combining. Adding phase shifters in front of the PAs will ensure that signals coming from the PAs will combine in phase.

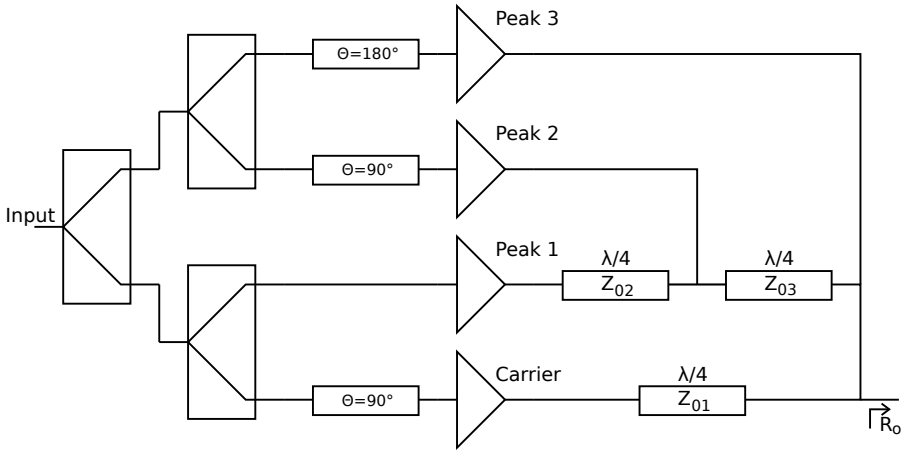


FIGURE 3.13: 4-stage Doherty PA topology.

[6]Only the topology is used from this research. Since the calculation of the load impedances and efficiency contains errors the load impedances, efficiency and calculation of transmission lines is done differently.

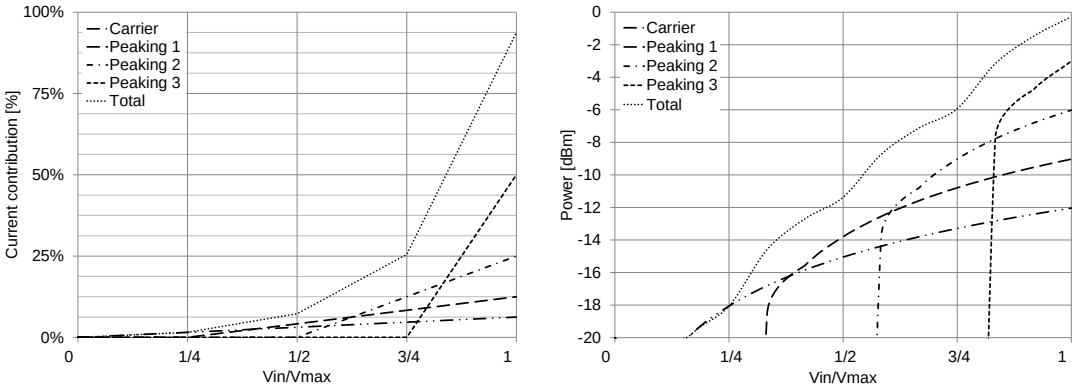
Power contributions per PA

If the operation ranges of the overall PA are evenly distributed, the individual PAs could each be assigned a quarter of the input range $\frac{V_{in}}{V_{max}}$. The carrier PA in this case will be active in the entire input range, while the peaking 1 PA starts contributing to the output power and load modulation at $\frac{1}{4}$ of the input range, the peaking 2 PA at $\frac{1}{2}$ of the input range and the peaking 3 PA at $\frac{3}{4}$ of the input range. So all PAs are turned on in the $\frac{3}{4}$ to 1 $\frac{V_{in}}{V_{max}}$ region. This can be observed in Fig. 3.14a.
To guarantee correct back-off powers so that the -20 to 0 dBm output power range is achieved the sizes of each PA differ. In fact every subsequent PA has two times the power contribution compared to its predecessor. When the four amplifiers have a power ratio of $\frac{1}{16}$:$\frac{1}{8}$:$\frac{1}{4}$:$\frac{1}{2}$ of the maximum output power, the output power can range from approximately -18 to 0 dBm. This is shown in Fig. 3.14b. The figure shows the power contribution based on the current contribution of Fig. 3.14a. Here the power is calculated as follows:

$$P_{PA}[dBm] = 10 \log \left(I_{PA} V_{DC} \right) \tag{3.19}$$

Where V_{DC} is assumed to be 1V for analysis purposes and I_{PA} is the current contribution per PA.
The carrier has in this case a saturated output power of -12 dBm, while the peaking 1 PA has a saturated output of -9 dBm. The peaking 2 PA then has a saturated output power of -6 dBm and the peaking 3 PA has a saturated output power of -3 dBm.

Since the power combining does not have a 100% efficiency some power will be lost. This power needs to be compensated by the PAs. At this point it is not known what the efficiency of the power combining network will be exactly. If an efficiency of approximately 60% is assumed [24] every PA needs to put out 2 dBm more to achieve the same output power range. The carrier has than -10 dBm, the peaking 1 has -7 dBm, the peaking 2 has -4 dBm and the peaking 3 PA then has a saturated output power of -1 dBm.



(A) Fundamental current profiles per PA. (B) Power contribution per PA [dBm].

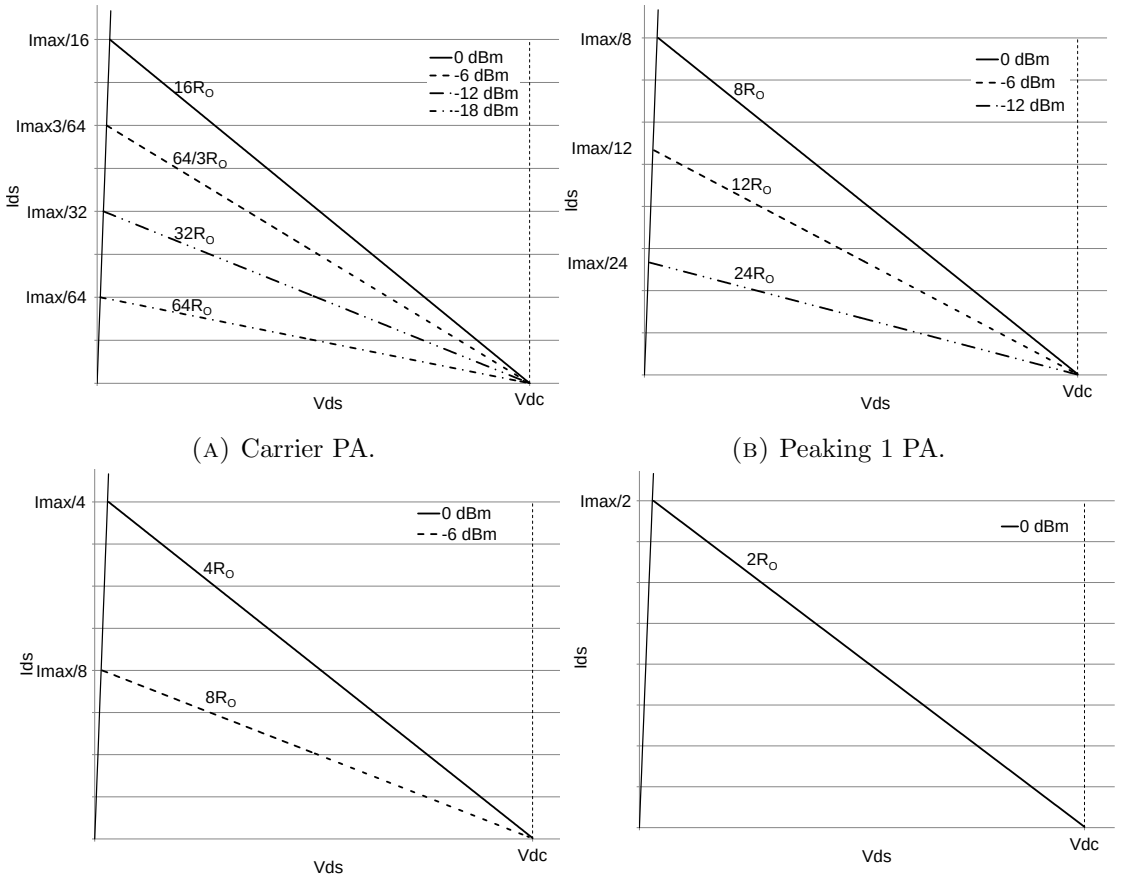
FIGURE 3.14: Power contribution per amplifier ($\frac{1}{16}$:$\frac{1}{8}$:$\frac{1}{4}$:$\frac{1}{2}$).

Load-line analysis

To achieve maximum efficiency the load presented at each PA needs to be equal to its optimum load impedance. The optimum impedance is reached when full voltage swing is achieved at a given current swing. Determining the optimum load impedance can be done with a load-line analysis. The load-lines of the PAs are illustrated in Fig. 3.15. Figure 3.14 shows the operation regions of each PA.

In the $0 - \frac{1}{4}\ \frac{V_{in}}{V_{max}}$ region just the carrier PA is turned on. At a $\frac{1}{4}\ \frac{V_{in}}{V_{max}}$ the carrier PA contributes $\frac{1}{64}$ of the total current the system can deliver. This means that if the efficiency has to be maximized at this point the load impedance needs to be scaled. For full current contribution the optimum system impedance is R_o. When $\frac{1}{64}^{th}$ of this current is contributed, maximal efficiency is achieved when R_o is scaled to $64R_o$ in this region. Then the first peaking region is reached at -18 dBm output power, where the power contribution can be observed in Fig. 3.14b. When the carrier PAs load-line reaches it's knee voltage, full voltage swing is achieved and the first maximum efficiency point is reached at a $\frac{1}{4}$ of the $\frac{V_{in}}{V_{max}}$ region.

When the input increases to the $\frac{1}{4} - \frac{1}{2}$ region the first peaking PA is turned on. As soon as this occurs the power combining network ensures that the loads of the PAs are modulated. The load of the carrier will be converted to $32R_o$ while the load of the peaking 1 PA will be converted to $24R_o$. When the loads of the carrier and the first peaking PA are converted to these values the second peaking region is reached at -11.37 dBm output power, here the power contribution per PA can be observed in Fig. 3.14b. This happens when the carrier and peaking 1 PAs load-lines reach their knee voltages. Full voltage swing is achieved for the second time and the second efficiency point is reached at $\frac{1}{2}$ of the $\frac{V_{in}}{V_{max}}$ region.



(A) Carrier PA.

(B) Peaking 1 PA.

(C) Peaking 2 PA.

(D) Peaking 3 PA.

FIGURE 3.15: Load-lines of the 4-stage Doherty PA.

If the input then increases to the $\frac{1}{2} - \frac{3}{4}$ region the second peaking PA will turn on. In this region the power combining network modulates the loads of the PAs again. The load of the carrier converts to $\frac{64}{3}R_o$, the load of the peaking 1 PA converts to $12R_o$ and the load of the peaking 2 PA will be converted to $8R_o$. When the loads of the carrier, peaking 1 and peaking 2 PAs are converted to these values the third peaking region is reached at -5.9 dBm backed off output power, where the power contribution per PA can be observed in Fig. 3.14b. This occurs as soon as the carrier, peaking 1 and peaking 2 PAs load-lines reach their knee voltages. Full voltage swing is achieved for the third time and the third efficiency point is reached at $\frac{3}{4}$ of the $\frac{V_{in}}{V_{max}}$ region.
If then the input increases from $\frac{3}{4}$ to the full input region the third and final peaking PA will turn on. In this region the power combining network again modulates the loads of the PAs. The load of the carrier PA modulates to $16R_o$ since it contributes a $\frac{1}{16}^{th}$ of the total current. The load of the peaking 1 PA is modulated to $8R_o$ since it contributes an $\frac{1}{8}^{th}$ of the total current. The load of the peaking 2 PA is modulated to $4R_o$ since it contributes a $\frac{1}{4}$ of the total current and the load of the peaking 3 PA will be modulated to $2R_o$ since it contributes a $\frac{1}{2}$ of the total current. As soon as the loads of the carrier,

peaking 1, peaking 2 and peaking 3 PAs are converted to these values the fourth and final peaking region is reached at -0.28 dBm backed off output power, where the power contribution per PA can be observed in Fig. 3.14b. This output occurs when the PAs load-lines reach their knee voltages. Full voltage swing is achieved and the last maximum efficiency point is reached at full input.

Load impedances

To generate the load modulation a power combining network is used. This network needs to be able to modulate the load as well as combine the powers. For this a transmission line combining network is chosen. With the transmission line combining network the impedances presented at the different PAs can be analyzed. These impedances are calculated with the help of the operational diagram given in Fig. 3.16.

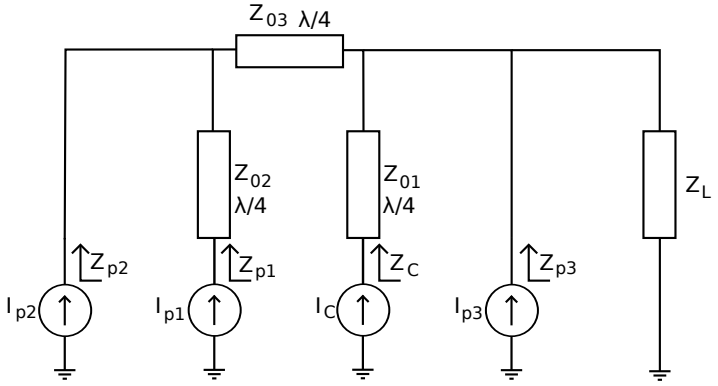


FIGURE 3.16: 4-stage Doherty PA operational diagram.

With this operational diagram the load impedance for the carrier, peaking 1, peaking 2 and peaking 3 PAs will be:

$$Z_c = \frac{Z_{01}^2}{\left(1 + \frac{I_{p1}+I_{p2}+I_{p3}}{I_c}\right) Z_L} \tag{3.20}$$

$$Z_{p1} = \frac{Z_{02}^2}{Z_{03}^2} \frac{I_c + I_{p1} + I_{p2} + I_{p3}}{(I_{p1} + I_{p2}) \left(1 + \frac{I_{p2}}{I_{p1}}\right)} Z_L \tag{3.21}$$

$$Z_{p2} = \left(1 + \frac{I_{p1}}{I_{p2}}\right) \frac{(I_{p1} + I_{p2})}{(I_c + I_{p1} + I_{p2} + I_{p3})} \frac{Z_{03}^2}{Z_L} \tag{3.22}$$

$$Z_{p3} = \left(1 + \frac{I_c + I_{p1} + I_{p2}}{I_{p3}}\right) Z_L \tag{3.23}$$

An exact derivation of these impedances can be found in Appendix A. As expected the load impedances change per PA depending on the input $\frac{V_{in}}{V_{max}}$ region, because the

load modulation depends heavily on the power combining network. If this network is designed carefully it is able to approach the desired impedances determined in the load-line analysis. When the transmission lines are scaled as follows [6]:

$$Z_{01} = XR_o \tag{3.24}$$

$$Z_{02} = YR_o \tag{3.25}$$

$$Z_{03} = ZR_o \tag{3.26}$$

When the load impedance Z_L is assumed to be R_o, the impedances can be rewritten as:

$$\begin{aligned}
Z_c &= \begin{cases} X^2R_o & \frac{V_{in}}{V_{max}} = \frac{1}{4} \\ \frac{1}{3}X^2R_o & \frac{V_{in}}{V_{max}} = \frac{1}{2} \\ \frac{1}{7}X^2R_o & \frac{V_{in}}{V_{max}} = \frac{3}{4} \\ \frac{1}{15}X^2R_o & \frac{V_{in}}{V_{max}} = 1 \end{cases} \qquad
Z_{p1} = \begin{cases} \infty & \frac{V_{in}}{V_{max}} = \frac{1}{4} \\ \frac{3}{2}\frac{Y^2}{Z^2}R_o & \frac{V_{in}}{V_{max}} = \frac{1}{2} \\ \frac{7}{18}\frac{Y^2}{Z^2}R_o & \frac{V_{in}}{V_{max}} = \frac{3}{4} \\ \frac{5}{6}\frac{Y^2}{Z^2}R_o & \frac{V_{in}}{V_{max}} = 1 \end{cases} \\
Z_{p2} &= \begin{cases} - & \frac{V_{in}}{V_{max}} = \frac{1}{4} \\ \infty & \frac{V_{in}}{V_{max}} = \frac{1}{2} \\ \frac{9}{7}Z^2R_o & \frac{V_{in}}{V_{max}} = \frac{3}{4} \\ \frac{3}{5}Z^2R_o & \frac{V_{in}}{V_{max}} = 1 \end{cases} \qquad
Z_{p3} = \begin{cases} - & \frac{V_{in}}{V_{max}} = \frac{1}{4} \\ - & \frac{V_{in}}{V_{max}} = \frac{1}{2} \\ \infty & \frac{V_{in}}{V_{max}} = \frac{3}{4} \\ \frac{15}{8}R_o & \frac{V_{in}}{V_{max}} = 1 \end{cases}
\end{aligned} \tag{3.27}$$

If all the PAs are matched to R_o at $\frac{V_{in}}{V_{max}} = 1$ then the expressions from Eq. 3.27 can be used to calculate the variables X, Y and Z that define the transmission line impedances.

$$\frac{1}{15}X^2R_o = 16R_o \tag{3.28}$$

$$\frac{5}{6}\frac{Y^2}{Z^2}R_o = 8R_o \tag{3.29}$$

$$\frac{3}{5}Z^2R_o = 4R_o \tag{3.30}$$

The transmission lines will then have the values.

$$Z_{01} = XR_o = \sqrt{15}R_o \tag{3.31}$$

$$Z_{02} = YR_o = \sqrt{\frac{5}{3}}R_o \tag{3.32}$$

$$Z_{03} = ZR_o = \sqrt{2}R_o \tag{3.33}$$

With the values for the transmission lines known, the load impedances for each PA can be plotted. This is shown in Fig. 3.17. The graph clearly shows the impact of the turning on of the peaking PAs. Note that the impedance of the peaking 1 PA increases in the $\frac{3}{4}$ to 1 $\frac{V_{in}}{V_{max}}$ region. This is an undesired but unavoidable effect. When Eq. 3.21, Fig. 3.16 and Fig. 3.14a are reconsidered this becomes obvious. Quarter wave transmission lines modulate the load in such a way that when the transmission line is terminated with a high load a low input load is presented at the device:

$$Z_{in} = \frac{Z_{TL}^2}{Z_{Load}} \tag{3.34}$$

This characteristic can be seen in Fig. 3.17. When two quarter-wave transmission lines are cascaded they lose the modulating property because the load gets modulated twice:

$$Z_{in} = \frac{Z_{TL_1}^2}{Z_{TL_2}^2} Z_{Load} \tag{3.35}$$

From Eq. 3.21 and Fig. 3.16 it can be derived that the load presented at the transmission line is dependent on the currents of all PAs. Z_{Load} from previous equation will then correspond with:

$$Z_{Load} = \frac{I_c + I_{p1} + I_{p2} + I_{p3}}{(I_{p1} + I_{p2})\left(1 + \frac{I_{p2}}{I_{p1}}\right)} Z_L \tag{3.36}$$

From this load it can be easily understood that as soon as the peaking 3 PA starts contributing current (I_{p3}) the impedance presented at the peaking 1 PA will increase.

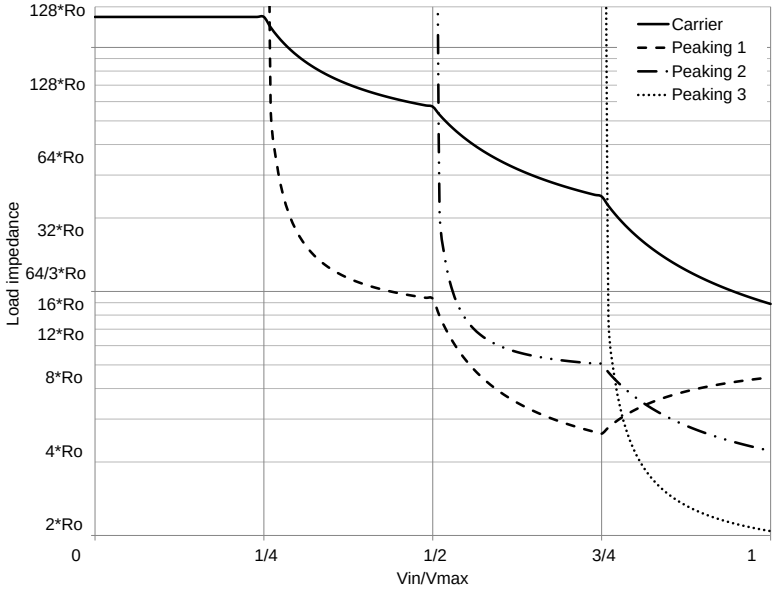
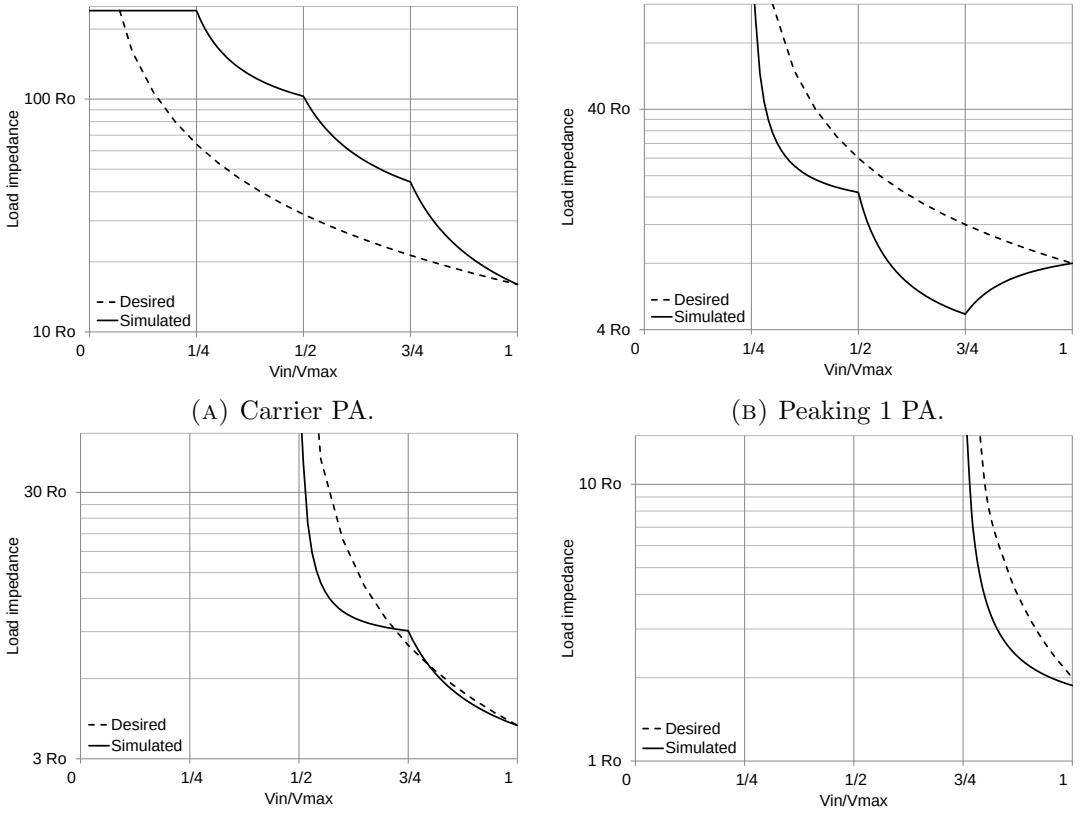


FIGURE 3.17: 4-stage Doherty PA load impedances (PA ratio: $\frac{1}{16}$:$\frac{1}{8}$:$\frac{1}{4}$:$\frac{1}{2}$).

Comparison between load-line and load impedances

If the results from the load-line analysis and load impedances at the PA output are compared in Fig. 3.18 it can be noted that the load modulation impedances follow the trend of the ideal load-line impedances. As calculated the power combining network to presents optimum load at full $\frac{V_{in}}{V_{max}}$ input. At back-off power levels this load however is not achieved and the presented loads differ from the optimum loads. This is because the optimum presented load can only be calculated at one point. In this case it is thus at full input and since the presented loads are dependent on the current relations per amplifier it is hard to closely follow the optimum load curves for all PAs.
Since these impedances differ from the optimum load-line impedances, efficiency is lost in the regions where the loads differ from the optimum loads. It might be worth while to investigate which is the most likely back-off power region where the 4-stage Doherty PA will be used. The power combining network can then be adjusted such that the presented load maximizes the efficiency at that back-off power level.



(A) Carrier PA.

(B) Peaking 1 PA.

(C) Peaking 2 PA.

(D) Peaking 3 PA.

FIGURE 3.18: 4-stage Doherty PA load impedances compared (PA ratio: $\frac{1}{16}$:$\frac{1}{8}$:$\frac{1}{4}$:$\frac{1}{2}$).

Efficiency

Since constant efficiency is a key issue in the 4-stage Doherty PA it is prudent to investigate the PAs impact on the efficiency. Because high efficiency is desirable, amplifiers biased in class-B and -C region are convenient since theoretical efficiencies of 78.5% and higher can be reached [5]. In this analysis the assumption is made that all amplifiers are biased in class-B for ease of calculation. The ideal drain efficiency of the 4-stage Doherty PA is derived in Appendix B. The efficiency can be calculated by:

$$\eta = \begin{cases} \frac{\pi}{4}\frac{\frac{V_i}{V_{max}}}{p_1} & 0 \leq \frac{V_i}{V_{max}} \leq p_1 \\ \frac{\pi}{2}\frac{\left(\frac{\frac{V_i}{V_{max}}}{p_2}\right)^2}{3\frac{\frac{V_i}{V_{max}}}{p_2} - 1} & p_1 \leq \frac{V_i}{V_{max}} \leq p_2 \\ \frac{3\pi}{4}\frac{\left(\frac{\frac{V_i}{V_{max}}}{p_3}\right)^2}{5\frac{\frac{V_i}{V_{max}}}{p_3} - 2} & p_2 \leq \frac{V_i}{V_{max}} \leq p_3 \\ \pi\frac{\left(\frac{V_i}{V_{max}}\right)^2}{7\frac{V_i}{V_{max}} - 3} & p_3 \leq \frac{V_i}{V_{max}} \leq 1 \end{cases} \tag{3.37}$$

Where p_1, p_2 and p_3 are $\frac{1}{4}$, $\frac{1}{2}$ and $\frac{3}{4}$ respectively.
This efficiency is plotted in Fig. 3.19. It can be observed that the theoretical efficiency is relatively constant and between 70% and 80% after the first peaking point $p_1 = \frac{1}{4}$, is reached.
Note that this efficiency calculation assumes that all amplifiers are operated in class-B, while the peaking amplifiers are actually biased in the region between class-B and class-C to ensure that the PAs turn on in the right region. Because these classes differ from the calculation, the theoretical efficiency increases when the peaking PA's are turned on.
However since parasitics play an important role at 60 GHz these theoretical efficiencies can't be reached. Efficiencies lower than the range between 70% and 80% are expected when the 4-stage Doherty PA is implemented.

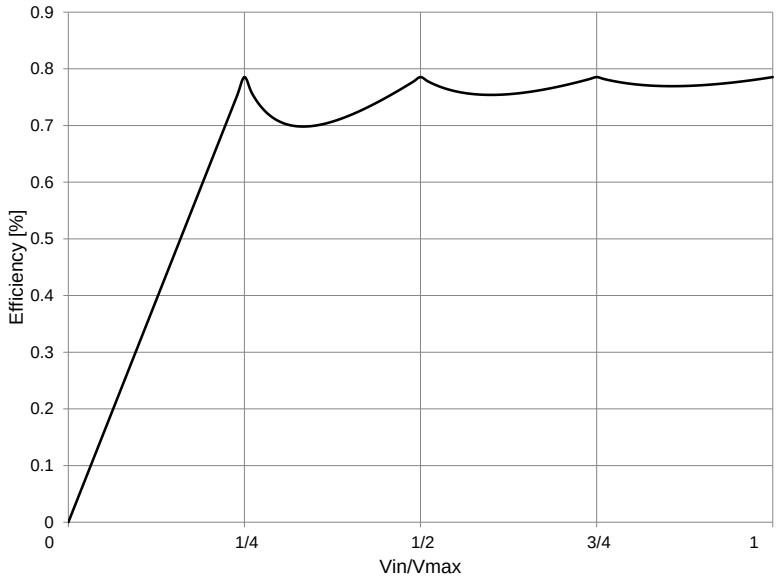


FIGURE 3.19: 4-stage Doherty PA theoretical efficiency.

Power combining network

As described in the previous sections, the power combining network is an essential component of the 4-stage Doherty PA. Without this power combining network it is not possible to reach such large back-off powers with high efficiency. However the power combining network does not have to consist off transmission lines, it can consist of lumped components or transformers. It is worthwhile to investigate this power combiner but this lies outside the scope of this project.

3.2.3 Specifications revisited

With the analysis and system design completed the specifications for the system and the PA can now be completed.

Operating distance

Because the current target device needs 5 dBm input power the operating distance needs to be reconsidered. Since it is not allowed to exceed 40 dBm EIRP the maximum operating distance lies in the centimeter range. In fact with a 1000 element array and 40 dBm EIRP a maximum distance of 2.23 *cm* can be achieved. At distances larger than this it can't be guaranteed that 5 dBm power is received. For this matter the operating distance for the current sensor node needs to be decreased to 2 *cm*.

Output power

Since a 1000 element array is not a practical array for first prototypes and flexibility in this array is desired, it is convenient that a single PA can support multiple array sizes at high efficiency. To support these different arrays different output powers at high efficiency are needed. When the output power ranges from -20 to 0 dBm, arrays ranging from 9 to 1000 elements can be supported.
To support this the carrier PA has to have a saturated output power of -10 dBm, the peaking 1 PA an output power of -7 dBm, the peaking 2 PA an output of -4 dBm and the peaking 3 PA an output power of -1 dBm.

Power gain

Enough gain is necessary to minimize the impact of the driving pre-amplifier on the system efficiencyf. When a gain of 10 dB is chosen the impact of the pre-amplifier is not negligible. In fact approximately 10% of the PAE depends on the pre amplifier if a gain of 10 dB is used. However this pre-amplifier needs to drive the PA then with an output power ranging from -30 to -20 dBm. During simulations it turned out that a minimum size cascode stage has a saturated output power that already exceeds -20 dBm. When efficiency is taken into account 10 dB in gain would be a reasonable choice since otherwise the efficiency of the pre-amplifier lowers the overall efficiency.
Before the signal from the pre-amplifier reaches the PAs it needs to be split. With every split the signal decreases 3 dB in power. In fact the signal needs to be split two times before it reaches the PAs. Therefore each PA has 6 dB lower input power. When an efficiency of approximately 60% is assumed [24] per power splitter this input power decreases to a total of 10 dB. So the input signal per amplifier lies somewhere between 6 to 10 dB lower than the pre-amplifier puts in. This needs to be compensated by the gain. When the gain is then increased to a range of 15 to 20 dB this signal loss is compensated. The effect of the pre amplifier on the total PAE is then reduced to approximately 1% of the total PAE.

Power added efficiency

In the study of the state of the art [3] PAEs ranging from 3% to 28% are common practice in 60 GHz PAs. These efficiencies all belong to power amplifiers that are not designed to have large back-off output powers. Since the large output power range is already quite challenging it is a sensible idea to have a constant efficiency at around 15%.

Specifications revisited

With the analysis system design and PA architecture choice done in the sections above, the specifications can be summarized in Tab. 3.3.
As mentioned before, the operating distance decreases remarkably. It is desired to have a larger operating distance than the centimeter regime. This is however not possible since the current sensor node needs at least 5 dBm of input power. As already was concluded in *Received power* (Chapter 3.1.3) of this chapter and revisited again in the section *Operating distance* of this paragraph it is not possible to increase the operation distance. This is due to the rules and legislation in transmit power, EIRP and antenna gain. These rules and regulations described in *Regulations summarized* severely limit the operating distance. This problem can't be solved by the base station and needs to be solved at the sensor node by allowing lower input powers.

Specification	Initial specifications	Revisited specifications
Operating frequency	60 GHz	60 GHz
Power received at target	5 dBm	5 dBm
Operating distance	0 - 10 m	2 cm. max.
Technology	40 nm CMOS	40 nm CMOS
Output power	T.B.D.	-20 − 0 dBm
Power gain	T.B.D.	15 − 20 dB
Input power	T.B.D.	(-40 − -35) − (-20 − -15) dBm
PAE	T.B.D.	≈15%
Linearity	-	-
Bandwidth	narrow	narrow

Table 3.3: Design specifications revisited.

Chapter 4

Circuit design

Typically Doherty and especially multistage Doherty PAs are used in frequency bands much lower than 60 GHz. Typical operation frequencies for multistage Doherty PAs are the UMTS frequencies or WCDMA band [17, 19, 22, 25], the DVB-T frequency band [23] or in the WIFI/WIMAX frequency band around 2.4 GHz [9, 16, 18, 21].
To the authors knowledge no 60 GHz multistage and especially 4-stage Doherty PA exist up to the moment of writing. However the development of such a PA at 60 GHz is necessary based on the system analysis and design made in chapter 3.
In this chapter the design considerations and simulations on the 4-stage Doherty PA structure at transistor level are discussed. First the advantages and disadvantages of two single ended structures are discussed, followed by the general unit PA structure. Then the influence of the power gain per stage on the total PAE is investigated. The simulation results on the general PA structure together with a short discussion in what still needs to be done conclude this chapter.

4.1 Design

Since the 4-stage Doherty structure is already a quite comprehensive structure to implement, certain design restrictions need to be imposed to minimize the design complexity. For that matter it is more convenient to use a single ended structure over the differential structure. A differential structure would need a differential power combining network that would increase the design complexity tremendously.
Out of the three basic topologies i.e. Common Source (CS), Common Gate (CG), Common Drain (CD), the CS topology is the best suited candidate for PA purposes. This is because it has good isolation and high gain in comparison with the CS which has a bad isolation and the CD which also has good isolation but poor gain.

Of the CS two variants of topologies are interesting, the common source as is and the cascode stage. Each topology has its advantages and disadvantages that will be discussed in the following sections.

4.1.1 Common source

The common source stage, schematically depicted in Fig. 4.1, has as strength that it maximizes the voltage and current swings [26, 27]. This maximization of the voltage and current swings results in a maximization of the output power that is higher for the same biasing voltage compared to a cascode device [28, 29]. On the other hand the topology has a parasitic capacitor, C_{gd}, between the input and output. Since the output of the CS stage is a high power output, the Miller effect of this topology causes power to leak back from the drain to the gate, a weak isolation [26, 29, 30] is present which decreases the stability of the device.

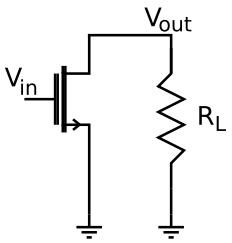


FIGURE 4.1: Common source structure (biassing not shown).

4.1.2 Cascode

The cascode stage, schematically depicted in Fig. 4.2, increases the output impedance of the structure which leads to an increase in gain [26, 29, 30]. Another effect that the CG causes is that the high output power node is not directly connected to the drain of the CS transistor. This reduces the Miller effect and the reverse isolation is noticeably higher [26, 29–31]. Because the reverse isolation is increased the stability is considerably higher than the common source stage [26, 29, 30].

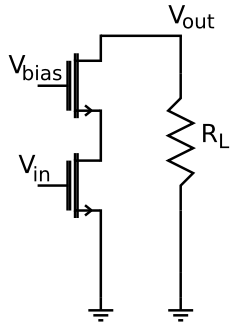


FIGURE 4.2: Cascode structure (biasing not shown).

Since the CS and CG transistors are cascoded higher voltage operation can be implemented. With this high voltage operation gate-oxide breakdown of the CG device limits the drain voltage swing of the CS device. This decreases the PAE of the topology [32]. Next to that all devices suffer from time dependent dielectric breakdown (TDDB) and hot carrier injection (HCI). These are two important issues and can't be disregarded. For the TDDB the maximum RMS gate voltage can't exceed certain values, which corresponds to a gate-oxide breakdown voltage of 1.21 V for a 40 *nm* CMOS process. HCI in devices occurs when the drain to source bias exposure is high over time. This bias can't be too high if devices need to be able to operate for long times [28].

4.1.3 General PA topology

Despite the fact that the cascode structure has a decreased PAE compared to the simple CS structure, and the gate-oxide voltage specifications need to be met to ensure long life spans the power gain, increased stability reversed isolation are superior to the common source device. For that matter the general PA topology, proposed in this work (Fig. 4.3), consists out of a cascade of 3 cascoded devices to achieve the design specifications. The general topology consists out of a power stage which is load-pull matched to the load in order to maximize the power transfer from the active devices to the load. Depending on the function of the desired PA in the 4-stage Doherty PA the device is biased in between the class-B, class-C region. Since this PA is biased in the class-B, class-C region the desired power gain can't be achieved by the output stage on it's own. Achieving the desired power gain means that two driving stages need to be added. These driver stages are biased in class-A to maximize the stage's gain. To further guarantee gain maximization the pre-amplification stages are matched conjugately.

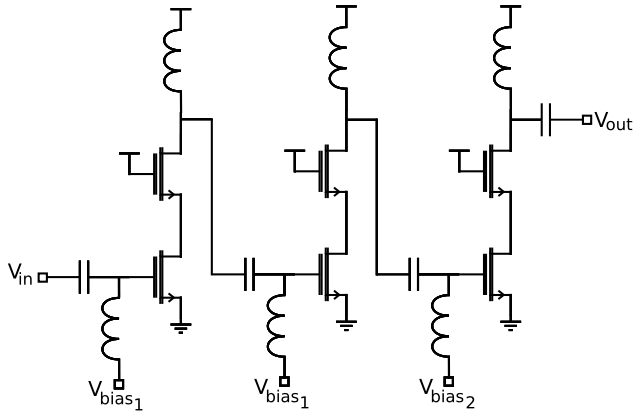


FIGURE 4.3: Cascode topology.

Power Added Efficiency

The Power added efficiency of the PA depends on the PAE of every stage, where every stages PAE is:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \eta_{drain}\left(1 - \frac{1}{G}\right) \tag{4.1}$$

If every stage is independent of one another the PAE of the entire PA is dependent on the stage that contributes the least amount of efficiency. However the gain of the different stages have an influence on the overall PAE given below [33, 34].

$$PAE_{tot} = \frac{1}{\frac{1}{PAE_1}\frac{1-\frac{1}{G_1}}{G_2G_3-\frac{1}{G_1}} + \frac{1}{PAE_2}\frac{1-\frac{1}{G_2}}{G_3-\frac{1}{G_1G_2}} + \frac{1}{PAE_3}\frac{1-\frac{1}{G_3}}{1-\frac{1}{G_1G_2G_3}}} \tag{4.2}$$

The complete derivation of the PAE can be found in Appendix C.
If for that matter the gain of the first and the second stage would both be 7 dB and the third stage has a gain of 5 dB the contribution of the first stage on the overall PAE would be in the range of 1%. The contribution in PAE of the second stage would be in the range of 30% of the overall PAE. The third stage would contribute in the range of 70% of the overall PAE. Therefore if the gain requirements need to be met and the overall PAE needs to be as high as possible it is desirable that the output stage has a sufficiently high gain and PAE. The PAE contribution of the subsequent stages can then be lower and the focus can lie more on gain. Since the power gain specifications as well as PAE need to be met the two driver stages will be operated in class-A to maximize gain, while the output stage will be operated in the region between class-B and class-C to maximize efficiency.
To increase the PAE one could say that the number of stages needs to be increased where for the second to last stage the focus lies more on the PAE to increase the overall PAE. However when three or more stages are employed it can occur that the PA becomes

unstable when a potential loop is present with a gain higher than 0 dB while the phase is -180° or less. So for three or more stage amplifiers, a phase shift of -180° is possible before the gain has dropped to 0 dB causing instability in the PA.

4.2 Simulations

The simulations made from the different PAs are discussed in this section. At the moment of writing two of the four PAs are not completely designed. Although the output power of the PAs presented in this section is sufficient, the PAs lack the desired gain to overcome the losses imposed by the power splitting network providing signals to the inputs of the PAs. Since the current PAs consist out of a two stage PA this is easily overcome by adding a third stage to increase the power gain. This remains to be implemented. The PAs discussed in this section are thus PAs that still need improvement to meet the desired specifications.

4.2.1 Carrier PA

As it is designed at this moment the carrier PA consist out of cascaded cascode stages to provide enough gain. The stages are input, output and interstage matched to 50 Ω to ease debugging purposes. Figure 4.4 shows the PAs schematic, the input and output matching network is made up out of the dc decoupling capacitor and shunt inductor. The inductor between the CG and CS devices resonates out the capacitor of the CS device to facilitate better matching between the CG and CS devices resulting in an increased gain.

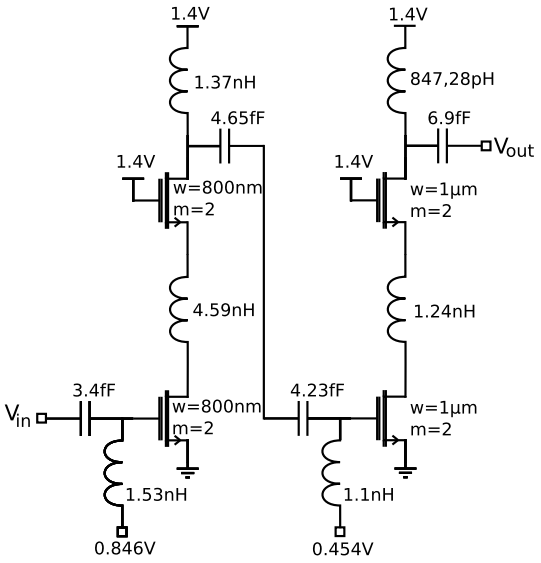


FIGURE 4.4: Schematic design of the carrier PA.

Gain, output power and power added efficiency

When the simulation results of the carrier, that are depicted in Fig. 4.5, are compared with the specifications it can be concluded that the output power specification of -10 dBm is met at maximum PAE.

The power added efficiency peaks at the highest point around 13.5%. Note that these simulations are conducted on a fixed load and that this PAE is thus the PAE where the PAs efficiency is peaking. In the 4-stage Doherty PA this peaking will occur 4 times in total for the carrier PA. Resulting in 4 peaks of a somewhat lower PAE since the load modulation can not guarantee the ideal load-line matching conditions.

The gain for the carrier ranges from 11.5 dB at -16 dBm output to 8 dB at -10 dBm output. Although the gain at the high output powers is slightly lower than desired[1] it is still a reasonable amount of gain considering that this gain needs to be delivered over a relatively large output power range. When a gain between 15 - 20 dB needs to be achieved a third driver stage needs to be added to the carrier PA. The input power seen in the figure shows that the input is correctly matched to the load of the input port and does not deviate from the desired input power.

[1] If a gain of 10 dB is assumed

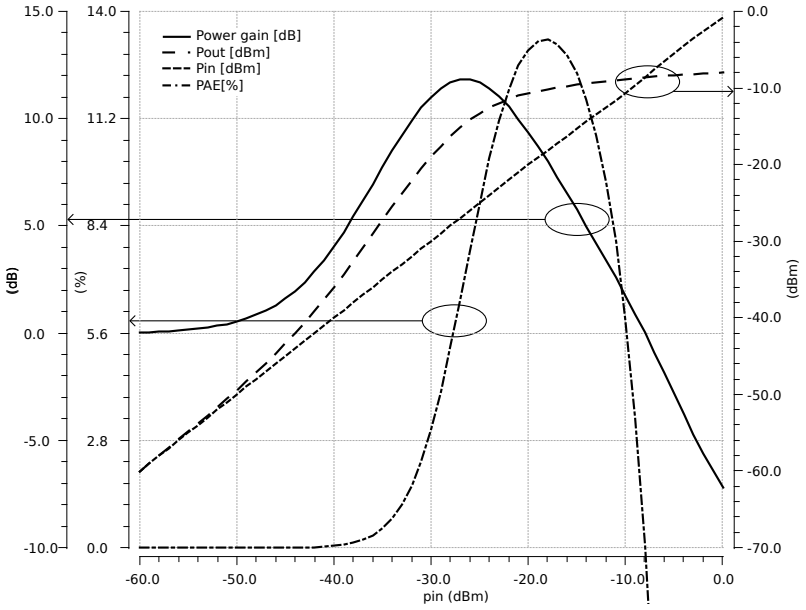


FIGURE 4.5: Carrier PA simulation results.

4.2.2 Peaking 1 PA

Like the carrier PA, the first peaking PA follows the general design of the PAs to provide enough gain. However a third pre-amplifier stage still needs to be added to satisfy the gain requirement. The stages are also input, output and interstage matched to 50 Ω for ease of debugging. Figure 4.6 shows the schematic representation of this PA.

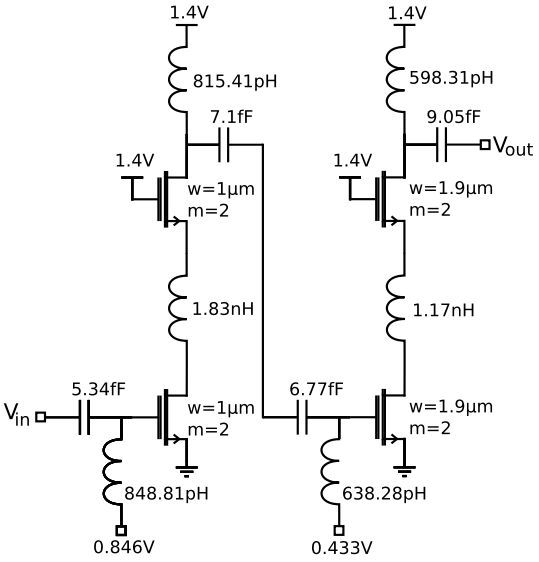


FIGURE 4.6: Schematic design of the peaking 1 PA.

Gain, output power and power added efficiency

The simulation results of the first peaking PA, depicted in Fig. 4.7 show that an output power of -7 dBm at maximum efficiency is met.
At this point the power added efficiency also peaks to a value of 13.3% when the PA is loaded with a fixed load. When a load modulation network is added this peaking would occur three times over the entire input range. Resulting, like the carrier PA, in 3 peaks of somewhat lower PAE since the load modulation cannot be guaranteed to be the same as the ideal load-line matching conditions.
The gain of the first peaking PA ranges from 11.5 dB at -11dBm output to 8 dB at -7 dBm output power. Just as the carrier PA, at high output powers the gain of the peaking PA is slightly lower than desired. However it is still a reasonable amount of gain at the high efficiency points[(2)]. When a gain between 15 - 20 dB needs to be achieved a third driver stage needs to be added to the carrier PA. The input power seen in the figure shows that the input is correctly matched to the load of the input port and does not deviate from the desired input power.

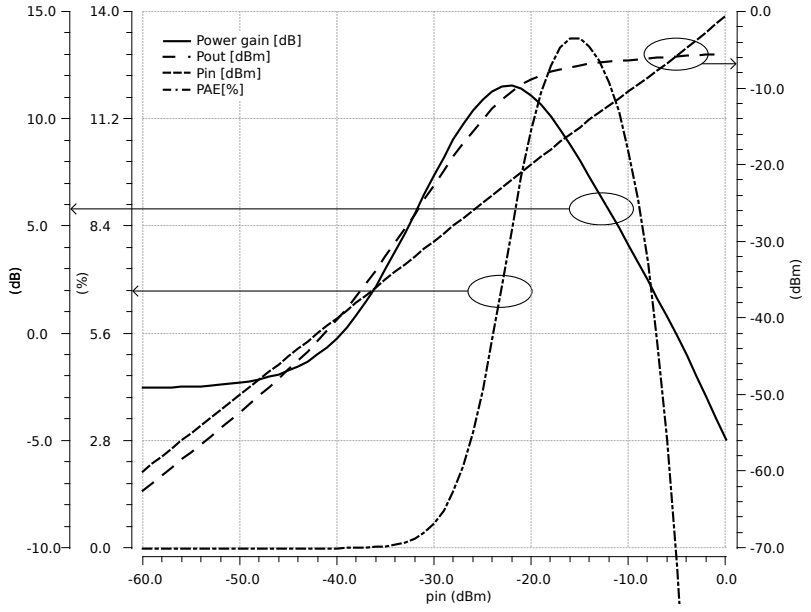


FIGURE 4.7: Peaking 1 PA simulation results.

4.3 What needs to be done

At the moment of writing the carrier and peaking 1 PA are partly designed. These PAs need to be further completed by adding a third stage to achieve the desired gain. Next to that simulations of gain, output power, PAE and stability need to be conducted

[2]If a gain of 10 dB is assumed

before a layout phase is started for these two PAs. To further complete the system the peaking 2 and peaking 3 PAs need to be designed.
Although the peaking 2 and peaking 3 PAs are necessary for the 4-stage Doherty PA, the design of these PAs has still to be conducted. Also stability is of importance, it can't be ignored. However it has not come so far to conduct stability simulations up to this moment. These simulations still need to be conducted.

Chapter 5

Conclusions and recommendations

This chapter reviews the graduation project and it draws conclusions from the system design and circuit design. Topics for future research are discussed together with the proposal for new research topics and an evaluation of the results.

5.1 Conclusions

In this thesis an exploration of an amplifier that is able of output powers ranging from -20 to 0 dBm with high efficiency is conducted. From the system analysis and design in chapter 3 it became clear that such a PA can be realized by designing a 4-stage Doherty PA. Such a PA needs to be capable to modulate the load presented at the unit PAs so that current and voltage swings are maximized throughout the output power range increasing the efficiency.
In the system design of this PA it became clear what the power contribution per PA needs to be in order to realize the output power range of the 4-stage Doherty PA. Also the loads presented to the PAs where examined with a load-line analysis so that maximal efficiency is maintained. During the analysis of the impedances, that a transmission line power combining network would impose, it became clear that the ideal loads follow at close proximity the ideal load-lines. However there is still room for improvement and a deeper investigation in this is desirable, especially since a closer approximation of the ideal loads would increase the efficiency of the entire system.

In the circuit design stage discussed in chapter 4 it became apparent that in order to achieve the desired gain, output power and efficiency four, multistage amplifiers need to

be created to realize the 4-stage Doherty PA. Each of these amplifiers consists out of a cascade of three cascoded stages. However at this point in time the carrier and peaking 1 PA are partially finished, in the sense that they deliver enough output power but not enough gain. This is because the losses of the power splitter where not yet taken into account and for these PAs a two stage cascode is designed. The gain of these amplifiers can be increased by adding a third pre-amplification stage at very low power added efficiency cost.

Due to time constraints the second and third peaking PAs as well as the power combining network have not been designed at this point, so a proof of concept cannot be delivered. However, although not at 60 GHz, several papers [9, 16, 21–23, 25, 35] validate this as a viable system design.

5.2 Future research

There remain a few uncertainties, especially with regard to the impact of the power combining network that modulates the load of the PAs. This network needs further research, the research to be done on this network is described in this section.

5.2.1 Effects of the load modulation on the matching network

The loads of the transmission lines, if calculated to present ideal load at full input $\frac{V_{in}}{V_{out}}$, have the following values:

$$Z_{01} = \sqrt{15}R_o \tag{5.1}$$

$$Z_{02} = \sqrt{\frac{5}{3}}R_o \tag{5.2}$$

$$Z_{03} = \sqrt{2}R_o \tag{5.3}$$

This means that if transmission lines are used and for instance an optimal load R_o of 50 Ω needs to be presented, the transmission lines have impedance values of:

$$Z_{01} \approx 194\Omega \tag{5.4}$$

$$Z_{02} \approx 65\Omega \tag{5.5}$$

$$Z_{03} \approx 71\Omega \tag{5.6}$$

Transmission line impedances of around 200 Ω are not feasible in CMOS [36]. For that reason a matching network between the output of the PA and the power combining network needs to be implemented.

The effects on the load modulation network in combination with the matching network needs to be thoroughly investigated in order to optimize the loads presented at the PA to maximize the voltage swings over the active device to increase the efficiency.

5.2.2 Improvements on load modulation

Since the load modulation network is a key element in the 4-stage Doherty PA it is wise to investigate this network further. Especially since a load presented by the load modulation network deviates from the ideal load-line, a drop in efficiency will result.
As discussed in Chapter 3: *Comparison between load-line and load impedances*, the load in this example is calculated to represent the desired load-line impedance at full input $\frac{V_{in}}{V_{max}}$ to maximize the efficiency at this point. It is worthwhile to investigate the likelihood at what back-off output powers the PA will operate. On these output powers the load modulation network can be optimized so that the optimal load-line load is presented in order to maximize the efficiency at this point.

Besides the best possible point where the load modulation network should peak, the type of modulation network is also of importance. For ease of calculation in this report the $\frac{\lambda}{4}$ transmission lines are used. However another load modulation network might be more suitable. Therefore further and thorough investigation need to be done in load modulation network such as distributed transformers, lumped component and TL load modulation networks to examine the best suitable network. In this research the disadvantages of the different networks need to be explored as well as the impact on the load modulation.

5.2.3 Near-field analysis

This work only covers the far-field Fraunhofer diffraction and not the near-field distribution. Already for a 3X3 array, the far-field distance is larger than the 2 *cm* operation range for the current sensor node. Because the beam shaping in the near-field is not examined, an analysis in this near-field is worthwhile in order to retrieve the beam shaping pattern.

5.2.4 Node input power

The input power that is required by the battery less sensor node is at least 5 dBm. This limits the operating distances of the system drastically. If the operating distance of 10 *m* has to be achieved at most -48 dBm an input power should be delivered. Then with a

1000 element array the 10 m distance could just about be met. With input power lower than this -48 dBm smaller array sizes would also be able to meet the 10 m distance.
To accomplish this the sensor node has to be improved greatly since legislation limits the total transmit power, antenna gain and EIRP of the base station. The operating distance can possibly be increased by adding a transformer at the end of the antenna of the sensor node. In [37] the authors use a transformer to increase the operating distance to 1 m. At this distance -10 dBm input power gets generated.
Another possibility to increase the operation distance is by adding a phased array at the sensor node. This phased array increases the node gain in a certain direction but has two problems, if the focus of the sensor node and base station are not in the same direction the received power will even drop. The other problem is the array size this increases the nodes size drastically whilst the small size is a big advantage of the node.
Increasing the amount of base stations can also increase the power received by the sensor node. The base stations therefore need to know exactly where the power of both stations is aimed. Also it can be possible that the combined powers of the base stations exceeds legal limits.
By adding a lens on the sensor node the power received by the antenna can be focused, so more power is received by the sensor node. This again goes at a cost of the size of the sensor node.

5.3 Evaluation

This project consisted out of a system analysis and a design exploration in the possibility to create a PA that is able to charge a battery-less sensor node. The initial intention of this project was to investigate in the system design, create a circuit design and create a layout. The system analysis and design turned out to be such a comprehensive phase that this project consisted for the better part out of this analysis and design. The fact that the output power regulation discussed in appendix **??** was missed meant that part of the project time was spent designing a system that, in hindsight, could not be deployed in most countries. The topology of this system is discussed in appendix D. This took up time that reduced the available time for the 4-stage Doherty PA.
Even though further research in the load modulation network is required, the 4-stage Doherty PA shows some promising results at system level. The 4-stage Doherty PA proves to be a good candidate for a wide output power range high efficiency PA. Also from the analysis done in this work it can be concluded that due to rules and regulations low output power and antenna arrays instead of high output power are necessary when designing PAs for phased array systems.

These results derived from the system design still have to be benchmarked with results from circuit level design and layout.

Appendix A

Load impedance derivation

In this appendix the full derivation of the load impedances is given.

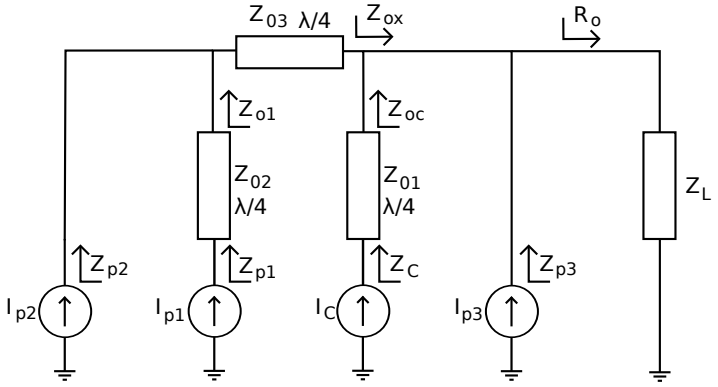


FIGURE A.1: 4-stage Doherty PA operational diagram.

Input impedance of a quarter wave transmission line

$$Z_{in} = Z_{TL}\frac{Z_L + jZ_{TL}\tan\beta l}{Z_{TL} + jZ_L\tan\beta l} \tag{A.1}$$

Where,

$$\beta = \frac{2\pi}{\lambda} \tag{A.2}$$

And,

$$l = \frac{\lambda}{4} \tag{A.3}$$

The input impedance of the quarter wave transmission line would then be [38]:

$$Z_{in} = \frac{Z_{TL}^2}{Z_L} \tag{A.4}$$

Impedance seen by the carrier PA

$$Z_c = \frac{Z_{01}^2}{Z_{oc}} \tag{A.5}$$

$$Z_{oc} = \left(1 + \frac{I_{p1} + I_{p2} + I_{p3}}{I_c}\right) Z_L \tag{A.6}$$

$$Z_c = \frac{Z_{01}^2}{\left(1 + \frac{I_{p1}+I_{p2}+I_{p3}}{I_c}\right) Z_L} \tag{A.7}$$

Impedance seen by the peaking 1 PA

$$Z_{p1} = \frac{Z_{02}^2}{Z_{o1}} \tag{A.8}$$

$$Z_{o1} = \frac{Z_{03}^2}{Z_{ox}} \left(1 + \frac{I_{p2}}{I_{p1}}\right) \tag{A.9}$$

$$Z_{ox} = \left(\frac{I_c + I_{p1} + I_{p2} + I_{p3}}{I_{p1} + I_{p2}}\right) Z_L \tag{A.10}$$

$$Z_{p1} = \frac{Z_{02}^2}{Z_{03}^2} \frac{I_c + I_{p1} + I_{p2} + I_{p3}}{(I_{p1} + I_{p2}) \left(1 + \frac{I_{p2}}{I_{p1}}\right)} Z_L \tag{A.11}$$

Impedance seen by the peaking 2 PA

$$Z_{p2} = \frac{Z_{03}^2}{Z_{ox}} \left(1 + \frac{I_{p1}}{I_{p2}}\right) \tag{A.12}$$

$$Z_{ox} = \left(\frac{I_c + I_{p1} + I_{p2} + I_{p3}}{I_{p1} + I_{p2}}\right) Z_L \tag{A.13}$$

$$Z_{p2} = \left(1 + \frac{I_{p1}}{I_{p2}}\right) \frac{(I_{p1} + I_{p2})}{(I_c + I_{p1} + I_{p2} + I_{p3})} \frac{Z_{03}^2}{Z_L} \tag{A.14}$$

Impedance seen by the peaking 3 PA

$$Z_{oc} = \left(1 + \frac{I_c + I_{p1} + I_{p2}}{I_{p3}}\right) Z_L \tag{A.15}$$

Impedance recalculated

When the transmission lines and load are rewritten to the optimal load resistance R_o.

$$\begin{aligned} Z_{01} &= X R_o & Z_{03} &= Z R_o \\ Z_{02} &= Y R_o & Z_L &= R_o \end{aligned} \tag{A.16}$$

The load impedances seen by the PAs are then rewritten to.

$$Z_c = X^2 \frac{Ro}{\left(1 + \frac{I_{p1}+I_{p2}+I_{p3}}{I_c}\right)} \tag{A.17}$$

$$Z_{p1} = \frac{Y^2}{Z^2} \frac{I_c + I_{p1} + I_{p2} + I_{p3}}{(I_{p1} + I_{p2})\left(1 + \frac{I_{p2}}{I_{p1}}\right)} R_o \tag{A.18}$$

$$Z_{p2} = Z^2 \left(1 + \frac{I_{p1}}{I_{p2}}\right) \frac{(I_{p1} + I_{p2})}{(I_c + I_{p1} + I_{p2} + I_{p3})} R_o \tag{A.19}$$

$$Z_{oc} = \left(1 + \frac{I_c + I_{p1} + I_{p2}}{I_{p3}}\right) R_o \tag{A.20}$$

Appendix B

Efficiency calculation

In this appendix the efficiency of the 4-stage Doherty PA is calculated. The efficiency calculation assumes equal device sizes and thus contributions. Further the assumption is made that only the load modulation has affect to the PA that is turned on last.
In reality the load modulation affects all PAs, their voltage swing and thus their efficiency. However this would increase the derivation complexity of the efficiency drastically and is for that matter not done.

B.1 Efficiency-I

From [39] it is known that:

$$\eta = \frac{P_{RF}}{P_{dc}} \frac{\frac{V_i}{V_{max}}}{p_x} \tag{B.1}$$

Here p_x are points: p_1, p_2, p_3 or 1

$$\begin{aligned} P_{RF} &= \frac{V_{dc}}{\sqrt{2}} \frac{I_{RF}}{\sqrt{2}} \frac{\frac{V_i}{V_{max}}}{p_x} \\ &= \frac{1}{2} I_{RF} V_{dc} \frac{\frac{V_i}{V_{max}}}{p_x} \end{aligned} \tag{B.2}$$

$$I_{RF} = \frac{I_{max}}{2\pi} \frac{\alpha - \sin\alpha}{1 - \cos\frac{\alpha}{2}} \tag{B.3}$$

$$P_{dc} = \begin{cases} I_{dc} V_{dc} \dfrac{\frac{V_i}{V_{max}}}{p_x} \\ I_{dc} V_{dc} \left(x \dfrac{\frac{V_i}{V_{max}}}{p_x} - y \right) \end{cases} \tag{B.4}$$

Here the dc current depends on the selected PA since the PA that is turned on last ranges from 0 to 1, controlled by $x\frac{\frac{V_i}{V_{max}}}{p_x} - y$, while other PAs are already active.

Assumption: Also the dc current of the PA that is turned on last reaches its maximum range i.e. from [0 - 1] I_{dc} between the point where it should be turned on and the point where it should saturate.

Assumption: This also should happen to the RF current. However this adds large discontinuities in the turning on region i.e. 0. Adding this causes large efficiency jumps. These are rather unrealistic since this is happens around the region where the PA, if biassed in class-B, does theoretically not consume any dc power or adds rf power. For that reason it is neglected. This assumption, although it is not discussed, is for that reason also made in [39].

$$I_{dc} = \frac{I_{max}}{2\pi}\frac{2\sin\frac{\alpha}{2} - \alpha\cos\frac{\alpha}{2}}{1-\cos\frac{\alpha}{2}} \tag{B.5}$$

For a PA biased in class-B $\alpha = \pi$:

$$I_{RF} = \frac{I_{max}}{2} \tag{B.6}$$

$$I_{dc} = \frac{I_{max}}{\pi} \tag{B.7}$$

Thus P_{RF} and P_{dc} are:

$$P_{RF} = \frac{1}{2} I_{RF} V_{dc} \frac{\frac{V_i}{V_{max}}}{p_x} \tag{B.8}$$

$$P_{dc} = \begin{cases} I_{dc}V_{dc}\dfrac{\frac{V_i}{V_{max}}}{p_x} \\ I_{dc}V_{dc}\left(x\dfrac{\frac{V_i}{V_{max}}}{p_x} - y\right) \end{cases} \tag{B.9}$$

Assumption: every PA contributes equally i.e. have the same size ratio 1:1:1:1.
Then $I_{max} = \frac{I_{max}}{4}$ and the DC and RF currents per unit PA are:

$$I_{RF} = \frac{1}{2}\frac{I_{max}}{4} \tag{B.10}$$

$$I_{dc} = \frac{1}{\pi}\frac{I_{max}}{4} \tag{B.11}$$

So per unit PA:

$$P_{RF} = \frac{1}{2}\frac{1}{2}\frac{I_{max}}{4} V_{dc} \frac{\frac{V_i}{V_{max}}}{p_x} \tag{B.12}$$

$$P_{dc} = \begin{cases} \frac{1}{\pi}\frac{I_{max}}{4}V_{dc}\frac{\frac{V_i}{V_{max}}}{p_x} \\ \frac{1}{\pi}\frac{I_{max}}{4}V_{dc}\left(x\frac{\frac{V_i}{V_{max}}}{p_x} - y\right) \end{cases} \tag{B.13}$$

$\boldsymbol{0} \leq \frac{V_i}{V_{max}} \leq \boldsymbol{p}_1$

When just the carrier PA is turned on:

$$\eta = \frac{\frac{1}{2}I_{RF}V_{dc}\frac{\frac{V_i}{V_{max}}}{p_1}\frac{V_i}{V_{max}}}{I_{dc}V_{dc}\frac{\frac{V_i}{V_{max}}}{p_1}} \frac{\frac{V_i}{V_{max}}}{p_1} \tag{B.14}$$

Assumption: at point p_1 the PA contributes with maximum current i.e. in the case of the carrier the maximum efficiency point lies at $\frac{V_i}{V_{max}} = p_1$ and maximum current delivered per PA is:

$$I_{RF} = \frac{1}{2}\frac{I_{max}}{4}$$

$$I_{dc} = \frac{1}{\pi}\frac{I_{max}}{4}$$

So the efficiency consists out of:

$$\eta = \frac{\frac{1}{2}\frac{1}{2}\frac{I_{max}}{4}}{\frac{1}{\pi}\frac{I_{max}}{4}}\frac{\frac{V_i}{V_{max}}}{p_1} \tag{B.15}$$

$$\eta = \frac{\pi}{4}\frac{\frac{V_i}{V_{max}}}{p_1} \tag{B.16}$$

$\boldsymbol{p}_1 < \frac{V_i}{V_{max}} \leq \boldsymbol{p}_2$

The carrier PA and the first peaking PA are turned on:

$$P_{RF} = \frac{1}{2}I_{RF}V_{dc}\frac{\frac{V_i}{V_{max}}}{p_2} \tag{B.17}$$

I_{RF} consists out of the RF currents of both the carrier as the peaking 1 PA.
P_{RF} is thus:

$$P_{RF} = \frac{1}{2}(I_{RF\_carrier} + I_{RF\_peak1})V_{dc}\frac{\frac{V_i}{V_{max}}}{p_2} \tag{B.18}$$

$$P_{dc} = I_{dc}V_{dc} \tag{B.19}$$

I_{dc} consists out of the dc currents of both the carrier as the peaking 1 PA.
P_{dc} is thus:

$$P_{dc} = (I_{dc\_carrier} + I_{dc\_peak1})V_{dc} \tag{B.20}$$

Assumption: at point p_2 the PAs contributes with maximum current. The maximum current delivered per PA is:

$$\begin{aligned} I_{RF\_carrier} &= \frac{1}{2}\frac{I_{max}}{4} & I_{dc\_carrier} &= \frac{1}{\pi}\frac{I_{max}}{4}\frac{\frac{V_i}{V_{max}}}{p_2} \\ I_{RF\_peak1} &= \frac{1}{2}\frac{I_{max}}{4} & I_{dc\_peak1} &= \frac{1}{\pi}\frac{I_{max}}{4}\left(2\frac{\frac{V_i}{V_{max}}}{p_2} - 1\right) \end{aligned} \tag{B.21}$$

So,

$$P_{RF} = \frac{1}{2}\frac{I_{max}}{4}V_{dc}\frac{\frac{V_i}{V_{max}}}{p_2} \tag{B.22}$$

$$P_{dc} = \frac{1}{\pi}\frac{I_{max}}{4}\left(3\frac{\frac{V_i}{V_{max}}}{p_2} - 1\right)V_{dc} \tag{B.23}$$

And the efficiency is thus:

$$\eta = \frac{\frac{1}{2}\frac{I_{max}}{4}V_{dc}\frac{\frac{V_i}{V_{max}}}{p_2}}{\frac{1}{\pi}\frac{I_{max}}{4}\left(3\frac{\frac{V_i}{V_{max}}}{p_2} - 1\right)V_{dc}}\frac{\frac{V_i}{V_{max}}}{p_2} \tag{B.24}$$

$$\eta = \frac{\pi}{2}\frac{\left(\frac{\frac{V_i}{V_{max}}}{p_2}\right)^2}{3\frac{\frac{V_i}{V_{max}}}{p_2} - 1} \tag{B.25}$$

$\boldsymbol{p}_2 < \frac{V_i}{V_{max}} \leq \boldsymbol{p}_3$

The carrier and first two peaking PAs are turned on:

$$P_{RF} = \frac{1}{2} I_{RF} V_{dc} \frac{\frac{V_i}{V_{max}}}{p_3} \tag{B.26}$$

I_{RF} consists out of the RF currents of the carrier, the peaking 1 and peaking 2 PA. P_{RF} is thus:

$$P_{RF} = \frac{1}{2}(I_{RF\_carrier} + I_{RF\_peak1} + I_{RF\_peak2}) V_{dc} \frac{\frac{V_i}{V_{max}}}{p_3} \tag{B.27}$$

$$P_{dc} = I_{dc} V_{dc} \tag{B.28}$$

I_{dc} consists out of the dc currents of the carrier, peaking 1 and peaking 2 PA. P_{dc} is thus:

$$P_{dc} = (I_{dc\_carrier} + I_{dc\_peak1} + I_{dc\_peak2}) V_{dc} \tag{B.29}$$

Assumption: at point p_3 the PAs contributes with maximum current. The maximum current delivered per PA is:

$$\begin{aligned} I_{RF\_carrier} &= \frac{1}{2}\frac{I_{max}}{4} & I_{dc\_carrier} &= \frac{1}{\pi}\frac{I_{max}}{4}\frac{\frac{V_i}{V_{max}}}{p_3} \\ I_{RF\_peak1} &= \frac{1}{2}\frac{I_{max}}{4} & I_{dc\_peak1} &= \frac{1}{\pi}\frac{I_{max}}{4}\frac{\frac{V_i}{V_{max}}}{p_3} \\ I_{RF\_peak2} &= \frac{1}{2}\frac{I_{max}}{4} & I_{dc\_peak2} &= \frac{1}{\pi}\frac{I_{max}}{4}\left(3\frac{\frac{V_i}{V_{max}}}{p_3} - 2\right) \end{aligned} \tag{B.30}$$

So,

$$P_{RF} = \frac{1}{2}\frac{3}{2}\frac{I_{max}}{4} V_{dc} \frac{\frac{V_i}{V_{max}}}{p_3} \tag{B.31}$$

$$P_{dc} = \frac{1}{\pi}\frac{I_{max}}{4}\left(5\frac{\frac{V_i}{V_{max}}}{p_3} - 2\right) V_{dc} \tag{B.32}$$

And the efficiency is thus:

$$\eta = \frac{\frac{3}{4}\frac{I_{max}}{4} V_{dc} \frac{\frac{V_i}{V_{max}}}{p_3}}{\frac{1}{\pi}\frac{I_{max}}{4}\left(5\frac{\frac{V_i}{V_{max}}}{p_3} - 2\right) V_{dc}} \frac{\frac{V_i}{V_{max}}}{p_3} \tag{B.33}$$

$$\eta = \frac{3\pi}{4} \frac{\left(\frac{\frac{V_i}{V_{max}}}{p_3}\right)^2}{5\frac{\frac{V_i}{V_{max}}}{p_2} - 2} \tag{B.34}$$

$\boldsymbol{p_3 < \frac{V_i}{V_{max}} \leq 1}$

All PAs are turned on:

$$P_{RF} = \frac{1}{2} I_{RF} V_{dc} \frac{V_i}{V_{max}} \tag{B.35}$$

I_{RF} consists out of the RF currents of the carrier, peaking 1, peaking 2 and peaking 3 PA.
P_{RF} is thus:

$$P_{RF} = \frac{1}{2}(I_{RF\_carrier} + I_{RF\_peak1} + I_{RF\_peak2} + I_{RF\_peak3}) V_{dc} \frac{V_i}{V_{max}} \tag{B.36}$$

$$P_{dc} = I_{dc} V_{dc} \tag{B.37}$$

I_{dc} consists out of the dc currents of the carrier, peaking 1, peaking 2 and peaking 3 PA.
P_{dc} is thus:

$$P_{dc} = (I_{dc\_carrier} + I_{dc\_peak1} + I_{dc\_peak2} + I_{dc\_peak3}) V_{dc} \tag{B.38}$$

Assumption: at point 1 the PAs contributes with maximum current. The maximum current delivered per PA is:

$$\begin{aligned}
I_{RF_carrier} &= \frac{1}{2}\frac{I_{max}}{4} & I_{dc_carrier} &= \frac{1}{\pi}\frac{I_{max}}{4}\frac{V_i}{V_{max}} \\
I_{RF_peak1} &= \frac{1}{2}\frac{I_{max}}{4} & I_{dc_peak1} &= \frac{1}{\pi}\frac{I_{max}}{4}\frac{V_i}{V_{max}} \\
I_{RF_peak2} &= \frac{1}{2}\frac{I_{max}}{4} & I_{dc_peak2} &= \frac{1}{\pi}\frac{I_{max}}{4}\frac{V_i}{V_{max}} \\
I_{RF_peak3} &= \frac{1}{2}\frac{I_{max}}{4} & I_{dc_peak3} &= \frac{1}{\pi}\frac{I_{max}}{4}\left(4\frac{V_i}{V_{max}} - 3\right)
\end{aligned} \tag{B.39}$$

So,

$$P_{RF} = \frac{I_{max}}{4} V_{dc} \frac{V_i}{V_{max}} \tag{B.40}$$

$$P_{dc} = \frac{1}{\pi}\frac{I_{max}}{4}\left(7\frac{V_i}{V_{max}} - 3\right) V_{dc} \tag{B.41}$$

And the efficiency is thus:

$$\eta = \frac{\frac{I_{max}}{4} V_{dc} V_i}{\frac{1}{\pi}\frac{I_{max}}{4}\left(7\frac{V_i}{V_{max}} - 3\right) V_{dc}} \frac{V_i}{V_{max}} \tag{B.42}$$

$$\eta = \pi \frac{\left(\frac{V_i}{V_{max}}\right)^2}{7\frac{V_i}{V_{max}} - 3} \tag{B.43}$$

This results in the conventionally obtained overall efficiency:

$$\eta = \begin{cases} \frac{\pi}{4}\frac{\frac{V_i}{V_{max}}}{p_1} & 0 \leq \frac{V_i}{V_{max}} \leq p_1 \\ \frac{\pi}{2}\frac{\left(\frac{\frac{V_i}{V_{max}}}{p_2}\right)^2}{3\frac{\frac{V_i}{V_{max}}}{p_2} - 1} & p_1 \leq \frac{V_i}{V_{max}} \leq p_2 \\ \frac{3\pi}{4}\frac{\left(\frac{\frac{V_i}{V_{max}}}{p_3}\right)^2}{5\frac{\frac{V_i}{V_{max}}}{p_3} - 2} & p_2 \leq \frac{V_i}{V_{max}} \leq p_3 \\ \pi\frac{\left(\frac{V_i}{V_{max}}\right)^2}{7\frac{V_i}{V_{max}} - 3} & p_3 \leq \frac{V_i}{V_{max}} \leq 1 \end{cases} \tag{B.44}$$

B.2 Efficiency-II

The different stages in the 4-stage Doherty PA are not biased in the same classes. The biasing depends on the moment when the stage needs to be turned on. The carrier PA is operated in class-B while the peaking PAs will be operated anywhere between class-B and class-C.
If the efficiency derivation of B.1 is considered as basis the effects on the theoretical efficiency will be as follows.

The RF-current through each PA stage can be formulated as.

$$I_x = I_{max\_PA_x} W_x \tag{B.45}$$

Here x represents the PA selected and W_x represents the factor for the RF-current that is set by the biasing. Then for each PA stage the factors are.

$$\begin{aligned} W_c &= \frac{1}{2\pi}\frac{\alpha_c - \sin(\alpha_c)}{1-\cos\left(\frac{\alpha_c}{2}\right)} & W_{p1} &= \frac{1}{2\pi}\frac{\alpha_{p1} - \sin(\alpha_{p1})}{1-\cos\left(\frac{\alpha_{p1}}{2}\right)} \\ W_{p2} &= \frac{1}{2\pi}\frac{\alpha_{p2} - \sin(\alpha_{p2})}{1-\cos\left(\frac{\alpha_{p2}}{2}\right)} & W_{p3} &= \frac{1}{2\pi}\frac{\alpha_{p3} - \sin(\alpha_{p3})}{1-\cos\left(\frac{\alpha_{p3}}{2}\right)} \end{aligned} \tag{B.46}$$

Where α_x represents the conduction angle of PA_x.

The dc-current through each PA stage can be formulated as.

$$I_x = I_{max\_PA_x} U_x \tag{B.47}$$

Here x represents the PA selected and U_x represents the factor for the dc-current that is set by the biasing. Then for each PA stage the factors are.

$$\begin{aligned} U_c &= \frac{1}{2\pi}\frac{2\sin\left(\frac{\alpha_c}{2}\right) - \alpha_c\cos\left(\frac{\alpha_c}{2}\right)}{1-\cos\left(\frac{\alpha_c}{2}\right)} & U_{p1} &= \frac{1}{2\pi}\frac{2\sin\left(\frac{\alpha_{p1}}{2}\right) - \alpha_{p1}\cos\left(\frac{\alpha_{p1}}{2}\right)}{1-\cos\left(\frac{\alpha_{p1}}{2}\right)} \\ U_{p2} &= \frac{1}{2\pi}\frac{2\sin\left(\frac{\alpha_{p2}}{2}\right) - \alpha_{p2}\cos\left(\frac{\alpha_{p2}}{2}\right)}{1-\cos\left(\frac{\alpha_{p2}}{2}\right)} & U_{p3} &= \frac{1}{2\pi}\frac{2\sin\left(\frac{\alpha_{p3}}{2}\right) - \alpha_{p3}\cos\left(\frac{\alpha_{p3}}{2}\right)}{1-\cos\left(\frac{\alpha_{p3}}{2}\right)} \end{aligned} \tag{B.48}$$

Where α_x again represents the conduction angle of PA_x

Assumption: The maximum $I_{max\_PA_x}$ currents of every PA are the same. i.e. the PAs have a size ratio 1:1:1:1.

Combining these factors leads to the following theoretical efficiency.

$$\eta = \begin{cases} \frac{1}{2}\frac{W_c}{U_c}\frac{\frac{V_i}{V_{max}}}{p_1} & 0 \le \frac{V_i}{V_{max}} \le p_1 \\ \frac{1}{2}\frac{(W_c + W_{p1})\left(\frac{\frac{V_i}{V_{max}}}{p_2}\right)^2}{U_c\frac{\frac{V_i}{V_{max}}}{p_2} + U_{p1}\left(2\frac{\frac{V_i}{V_{max}}}{p_2} - 1\right)} & p_1 \le \frac{V_i}{V_{max}} \le p_2 \\ \frac{1}{2}\frac{(W_c + W_{p1} + W_{p2})\left(\frac{\frac{V_i}{V_{max}}}{p_3}\right)^2}{U_c\frac{\frac{V_i}{V_{max}}}{p_3} + U_{p1}\frac{\frac{V_i}{V_{max}}}{p_3} + U_{p2}\left(3\frac{\frac{V_i}{V_{max}}}{p_3} - 2\right)} & p_2 \le \frac{V_i}{V_{max}} \le p_3 \\ \frac{1}{2}\frac{(W_c + W_{p1} + W_{p2} + W_{p2})\left(\frac{V_i}{V_{max}}\right)^2}{U_c\frac{V_i}{V_{max}} + U_{p1}\frac{V_i}{V_{max}} + U_{p2}\frac{V_i}{V_{max}} + U_{p3}\left(4\frac{V_i}{V_{max}} - 3\right)} & p_3 \le \frac{V_i}{V_{max}} \le 1 \end{cases} \tag{B.49}$$

Appendix C

Impact on PAE

In this appendix the PAE of the 2-stage PA is calculated to gain more insight in the contribution per stage to the power added efficiency [34].

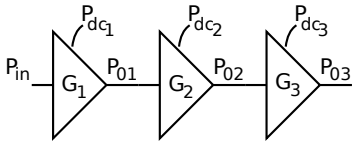


FIGURE C.1: 3-stage PA PAE contribution.

$$PAE_{tot} = \frac{P_{03} - P_{in}}{P_{dc1} + P_{dc2} + P_{dc3}} \tag{C.1}$$

$$\begin{aligned} \frac{1}{PAE_{tot}} &= \frac{P_{dc1}}{P_{01} - P_{in}} + \frac{P_{dc2}}{P_{02} - P_{in}} + \frac{P_{dc3}}{P_{03} - P_{in}} \\ &= \frac{P_{dc1}}{P_{01}G_2G_3 - \frac{P_{01}}{G_1}} + \frac{P_{dc2}}{P_{02}G_3 - \frac{P_{02}}{G_1G_2}} + \frac{P_{dc3}}{P_{03} - \frac{P_{03}}{G_1G_2G_3}} \\ &= \underbrace{\frac{P_{dc1}}{P_{01}\left(G_2G_3 - \frac{1}{G_1}\right)}}_{ⓐ} + \underbrace{\frac{P_{dc2}}{P_{02}\left(G3 - \frac{1}{G_1G_2}\right)}}_{ⓑ} + \underbrace{\frac{P_{dc3}}{P_{03}\left(1 - \frac{1}{G_1G_2G_3}\right)}}_{ⓒ} \end{aligned} \tag{C.2}$$

PAEs of the different stages when they are independent:

$$\frac{1}{PAE_1} = \frac{P_{dc1}}{P_{01}\left(1 - \frac{1}{G_1}\right)}, \quad \frac{1}{PAE_2} = \frac{P_{dc2}}{P_{02}\left(1 - \frac{1}{G_2}\right)}, \quad \frac{1}{PAE_3} = \frac{P_{dc3}}{P_{03}\left(1 - \frac{1}{G_3}\right)} \tag{C.3}$$

The factor of PAE contribution that a stage makes on the total system can be determined by comparing the independent PAEs of the stages with the individual dependent PAE:

$$\begin{aligned}
\text{ⓐ} \qquad \frac{P_{dc1}}{P_{01}\left(G_2G_3-\frac{1}{G_1}\right)}PAE_1 &= \frac{P_{dc1}}{P_{01}\left(G_2G_3-\frac{1}{G_1}\right)}\frac{P_{01}\left(1-\frac{1}{G_1}\right)}{P_{dc1}} \\
&= \frac{1-\frac{1}{G_1}}{G_2G_3-\frac{1}{G_1}} \\
&\approx \frac{1}{G_2G_3}
\end{aligned} \tag{C.4}$$

$$\begin{aligned}
\text{ⓑ} \qquad \frac{P_{dc2}}{P_{02}\left(G_3-\frac{1}{G_1G_2}\right)}PAE_2 &= \frac{P_{dc2}}{P_{02}\left(1-\frac{1}{G_1G_2}\right)}\frac{P_{02}\left(1-\frac{1}{G_2}\right)}{P_{dc2}} \\
&= \frac{1-\frac{1}{G_2}}{G_3-\frac{1}{G_1G_2}} \\
&\approx \frac{1}{G_3}
\end{aligned} \tag{C.5}$$

$$\begin{aligned}
\text{ⓒ} \qquad \frac{P_{dc3}}{P_{03}\left(1-\frac{1}{G_1G_2G_3}\right)}PAE_3 &= \frac{P_{dc3}}{P_{03}\left(1-\frac{1}{G_1G_2G_3}\right)}\frac{P_{03}\left(1-\frac{1}{G_3}\right)}{P_{dc3}} \\
&= \frac{1-\frac{1}{G_3}}{1-\frac{1}{G_1G_2G_3}} \\
&\approx \begin{cases} 1-\dfrac{1}{G_3} \\ 1 \end{cases}
\end{aligned} \tag{C.6}$$

The total PAE with contribution factor is then:

$$\begin{aligned}
PAE_{tot} &= \frac{1}{\frac{1}{PAE_1}\text{ⓐ}+\frac{1}{PAE_2}\text{ⓑ}+\frac{1}{PAE_3}\text{ⓒ}} \\
&= \frac{1}{\frac{1}{PAE_1}\frac{1-\frac{1}{G_1}}{G_2G_3-\frac{1}{G_1}}+\frac{1}{PAE_2}\frac{1-\frac{1}{G_2}}{G_3-\frac{1}{G_1G_2}}+\frac{1}{PAE_3}\frac{1-\frac{1}{G_3}}{1-\frac{1}{G_1G_2G_3}}} \\
&\approx \begin{cases} \dfrac{1}{\frac{1}{PAE_1G_1G_2}+\frac{1}{PAE_2G_3}+\frac{1-\frac{1}{G_3}}{PAE_3}} \\ \dfrac{1}{\frac{1}{PAE_1G_1G_2}+\frac{1}{PAE_2G_3}+\frac{1}{PAE_3}} \end{cases}
\end{aligned} \tag{C.7}$$

Appendix D

High output power PA topology

High output power high efficiency

When only deployment in the USA and Canada is desired the output power of the PA can be increased. With the high power PA it is necessary to make design considerations on the impact of the PA in combination with the array. For a first prototype it is not desirable that a 1000 element array is deployed, this simply is too costly and complex. Besides that a trade off between array size and spot size, as well as the total transmit power versus the element power and array complexity needs to be made. In this section the PA element output power and PA topology determination is discussed based on these trade offs.

Output power determination

As mentioned it is not desirable to create a 1000 element array. Design considerations need to be made to make a compromise in a fair spot size at 10 m and a reasonable array complexity. It is thereby convenient that the spot size of the array is small enough to still be able to scan a room with sufficient accuracy. On the other hand it is desirable that this is done with a small enough array while also keeping the PA complexity low. A suitable candidate is the 10x10 array, it has a spot size of approximately 2 m at 10 m distance and spot angle of 11.5°. This is sufficiently small enough to still scan a room with an array that has not a very high complexity.
If then the total EIRP of the array is maximally 40 dBm it can be calculated what output power per PA element is needed according to the array size. Figure D.1 depicts the results of this calculation and shows the transmit power, antenna gain, and element power. From the graph it can be noted that a 10x10 or 100 element array needs an

element power of 0 dBm, has an antenna gain of 20 dB and has a total output power of 20 dBm.

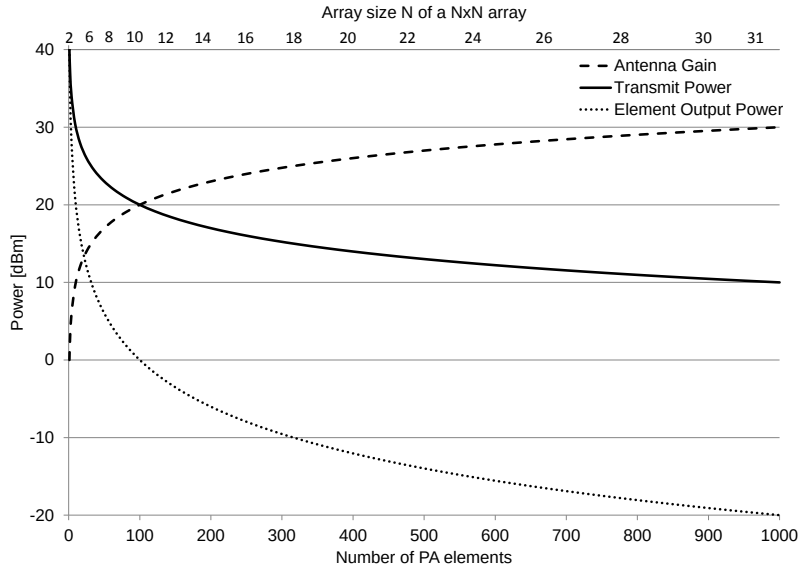


FIGURE D.1: Power per element based on the array size.

PA topology

The transmit power, element power determination done in D selects a transmit power of 20 dBm for an antenna array of 100 elements. With this antenna array the antenna gain is 20 dBi and PA element power is then set to 0 dBm. A suitable PA topology was selected for these specifications.

Since 0 dBm output power per element is needed a fairly low PA complexity is feasible. Therefore the differential CS topology is chosen, shown in Fig. D.2. The differential topology ensures a virtual ground between the active devices that eliminate large ground currents running through the substrate. The transformers in this topology ensure single ended to differential conversion as well as the matching between the stages and the biasing of the different stages.

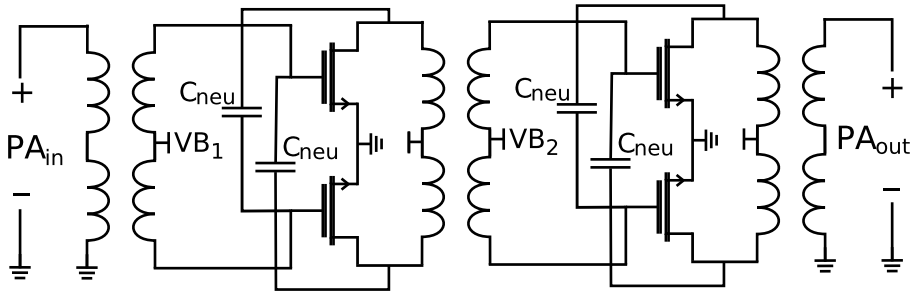


FIGURE D.2: Schematic representation of the PA topology [40].

Capacitor neutralization between the stages decreases the gate drain capacitor, increases the gain, ensure stability and provides isolation between the inputs and outputs[1] [40, 41]. Because the neutralization capacitor causes positive feedback a capacitor slightly smaller than the gate drain capacitor ensures that no oscillation can occur. Figure D.3 shows a simplified small signal equivalent of the differential pair with capacitor neutralization where the voltage gain of the circuit is [42].

$$\frac{V_{out}}{V_{in}}(j\omega) = \frac{g_m - j\omega(C_{gd} - C_{neu})}{j\omega(C_{gd} + C_{neu}) + 1/j\omega L} \tag{D.1}$$

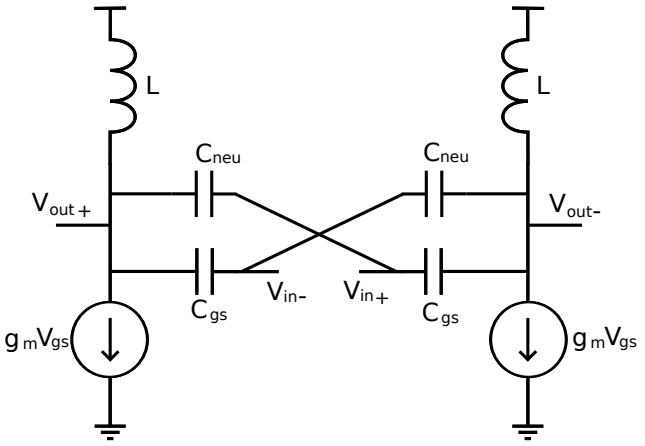


FIGURE D.3: Small signal equivalent circuit.

High output power conclusion

In this analysis only deployment in the USA and Canada is taken into consideration.If an output power of 0 dBm per element is selected with a 100 element array, so that 20 dBm transmit power, 20 dBi antenna gain and an EIRP of 40 dBm is achieved, the system is only deployable in the USA or Canada. During the project this was overlooked and a high output power topology was selected and partly designed.

When the system needs to be deployable in as many countries/continents as possible. The transmit power, EIRP, bandwidth and antenna gain need to be in the margins set by as many countries as possible. To do this the maximum transmit power needs to be lowered from 20 dBm to 10 dBm. In Tab. 3.1 an overview of these legislations is already given. The lowering of transmit power means a decrease in element power and also a decrease in EIRP. This decrease is undesired and if Fig. 3.6 is considered, results in a drastically shorter operating distance.

[1] reverse isolation

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