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MASTER

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Digitalization of the Gradient Amplifier Control Loop of an MRI Scanner

by R.J. van Wesenbeeck

Abstract

Within the framework of the Masters project at the Eindhoven University of Technology, Faculty of Electrical Engineering, in association with Philips Medical Systems, a feasibility study on the digitalization of the gradient amplifier control loop in an MRI scanner has been carried out. A description of the analog control loop and its components is given, and a design criterium is presented. The analog control loop is extended to a digitalized control loop. Because of the delay time introduced by the fact that the controller is a sampled system, the transients behavior deteriorates. Some general expressions for the final values of the current error and its integral are derived. These expressions show that the current error integral is non-zero in most of the cases, affecting the criterium. For the sampled pulse width modulator, algorithms for three sampling rates are given. Higher sampling rates result in less delay in the control loop. Feedforward seems to be a solution to many problems. It is shown that the criterium is automatically met in steady-state for proper choice of the feedforward filter, and also during the presence of transients it can be met if the feedforward filter results in a linear phase characteristic of the feedforward path. Furthermore, the range of the current error is reduced considerably, resulting in a gain of four bits for the ADC in the error path. In the last chapters of the thesis, a study is carried out on the digitalization of the pulse widths of the pulse width modulator. It seems that by choosing an appropriate rounding scheme for the switching times, the accuracy can be improved. High accuracy, however, can only be achieved for low sampling rates, because the quantization error on the pulse width is distributed over a longer time in that case. Digitalizing the pulse widths causes the same effects to occur as when a DA converter is placed in the control loop. Drifts and oscillations of the current error and its integral are the result. A remedy against this is the use of a noise shaper, based on a positive quantization error feedback. The best performance is achieved for the highest sampling rate of the PWM, four times per cycle.

List of Abbreviations

ADC		Analog to Digital (AD) Converter
DAC		Digital to Analog (DA) Converter
FFW		Feedforward Filter
G		Plant of R_c and L_c
GACL		Gradient Amplifier Control Loop
LP1 and LP2		Low-pass filter section after PWM
PW		Pulse Width
PWM		Pulse Width Modulator/Modulation
ZOH		Zero-Order Hold Circuit

B	[A/s]	Slope of ramp-shaped $I_{ref}(t)$
ΔPW	[s]	PW spacing after quantization
ΔT	[s]	T_s/N, N an integer
Δu^+	[V]	Spacing of u^+ after quantization
$e(t)$	[A]	Current Error
$e(\infty)$	[A]	Steady-state current value
$E(t)$	[As]	$\int_0^t e(\tau)d\tau$
$E(\infty)$	[As]	Steady-state value of $E(t)$
$e_c(t)$	[A]	Delay-corrected Current Error
$e_c(\infty)$	[A]	Steady-state value $e_c(t)$
$E_c(t)$	[As]	$\int_0^t e_c(\tau)d\tau$
$E_c(\infty)$	[As]	Steady-state value of $E_c(t)$
$e_{q,u}$	[V]	Quantization error of u^+
$e_{q,PW}$	[s]	Quantization Error of PW
$FFW(s)$		Transfer function of FFW
$G(s)$		Transfer function of G
$H_{cl}(s)$		Closed-loop transfer function of the GACL
$H_o(s)$		Open-loop transfer function of the GACL
$I_{ref}(t)$	[A]	Reference Current
$I(s)$		Interpolation Filter
L_c	[H]	Gradient Coil
$LP1(s)$ and $LP2(s)$		Transfer functions of LP1 and LP2
$PI_{out}(t)$	[V]	Output voltage of the PI controller
PW	[s]	Time that PWM output is V^+ (sign(PW)=1or0), $-V^+$ (sign(PW)=1)
PW_d	[s]	Digitalized PW
R_c	[Ω]	Gradient Coil Resistance
t_d	[s]	Propagation delay time of closed loop system for ramp input
$t_{d,i}$	[s]	Digitalized t_i
t_i	[s]	One of the switching times below

t^+_{off}	[s]	Time that output pos. PWM Half-bridge output goes from V^+ to 0V
t^-_{off}	[s]	Time that output neg. PWM Half-bridge output goes from V^+ to 0V
t^+_{on}	[s]	Time that output pos. PWM Half-bridge output goes from 0V to V^+
t^-_{on}	[s]	Time that output neg. PWM Half-bridge output goes from 0V to V^+
$t_{q,i}$	[s]	Quantization Error due to digitalized t_i
T	[s]	Extra open-loop delay time
$T_{s,PWM}$	[s]	PWM sampling time
T_z	[s]	Period of PWM triangular wave
u^+	[V]	PWM input signal
$u_d^+(k)$	[V]	Discretized version of u^+
$ZOH(s)$		Transfer function of ZOH

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1. Introduction

MRI systems belong to the advanced technical equipment in modern hospitals. These systems are used to make three-dimensional scans of the inside of humans. MRI (Magnetic Resonance Imaging) is based on magnetic nuclear resonance (NMR), a physical phenomenon based on the interaction of certain nuclei with a magnetic field. In the human body, hydrogen (H), sodium (Na), and phosphorus (P) nuclei are sensitive to NMR. These nuclei are mainly found in weak tissues, therefore, an important application of MRI is the localization of tumors.

The principle of NMR is, that some types nuclei align with a static magnetic field B_0 (which must be in the order of 1[T]). Aligned with B_0, they are susceptible to a resonance frequency ω_0, the Larmor frequency. The Larmor frequency is proportional to the magnetic field strength. This resonance frequency is typically in the RF range. To bring the nuclei into resonance, they must be triggered by an external RF pulse. This means, that an amount of RF energy is transferred to the nuclei. During the relaxation process following the pulse, the excited nuclei loose their energy reradiating RF signals. This relaxation signal is called the free induction decay. Its rate of decay depends on the kind of molecules in a tissue to which the phosphorus, sodium, and hydrogen nuclei are bounded, and its strength depends on the concentrations of these nuclei.

Three independent weak magnetic field gradients (T/m) superposed to B_0 are applied orthogonally, in the x-, y-, and z-directions. The z-gradient is used to select a certain tissue slice orthogonally to the z-axis. The technique of MRI scanning is based on the fact that the reradiated RF signal from a selected slice is related to the 2D-Fourier transform of the image of the slice. The free induction decay can be manipulated by applying time-constant and time-varying magnetic field gradients in the x- and y- direction. Sampling in time of the manipulated free induction decay corresponds to sampling the 2D-Fourier transform of the image of the selected slice.

The weak gradients in the magnetic field are built up by generating suited currents in the three orthogonal gradient coils. The complete system for generating the currents in these coils is called the gradient chain. Each coil has its own gradient amplifier power module, by which a voltage can be applied to the gradient coil. Each gradient amplifier consists of four parallelly connected Pulse Width Modulated voltage amplifiers. Connecting them in parallel results in less voltage harmonics over the gradient coil resulting from the switching behavior of the PWM's.

For good image quality, it is important that the places in the spatial frequency domain corresponding to the sampled RF signal are accurately reached by generating the prescribed current shapes in the gradient coils to generate the correct magnetic field gradients. For accurate positioning in the spatial frequency domain, the integrated current error in each gradient coil should not exceed 10[µAs]. However, generating these currents accurately is a problem because of the presence of disturbances and model parameter uncertainties. For this reason, the present gradient coils and their gradient amplifiers are embedded in analog gradient coil control loops.

Although the analog control loop gives reasonable performance, it could be advantageous to digitalize certain parts of the analog controller structure. Doing so, complex analog electronic circuits may be replaced by cheap and "simple" digital components, without deteriorating the system's performance. This could result in less components, a higher reliability, and lower service costs.

Other advantages of using computers, are the possibility to use modern control strategies, like advanced controller design, and the application of "Intelligent Control", making use of prior knowledge of the current shapes. Even more general, the digital components could make it advantageous to redesign the complete control structure for optimal performance and minimized costs.

By digitalizing the gradient amplifier control loop, however, also many problems may occur. The use of AD and DA converters will generate quantization errors, which will have their influence on e.g. the $10[\mu As]$ criterium of the integrated current error. Another problem might be the loss of phase margin because of the fact that the system must be sampled.

In this master thesis, the analog gradient amplifier control loop is analyzed to have a reference for the performance of the digitalized control loop. With respect to this reference, the advantages and disadvantages of replacing the analog gradient amplifier control loop by a digital configuration will become clear.

2. Process, Actuator, and Simplified Analog Control Loop

In this chapter, the process of the current through the gradient coil is defined first, and the kind of actuator, the PWM, is introduced to the reader. After this, the simplified model of analog gradient amplifier control loop (GACL) is given.

2.1 The Process to be Controlled

In fact, the process to be controlled is just generating a desired current in a coil that has a series resistance. The current must be generated by applying the correct voltage form following from the desired coil current form.
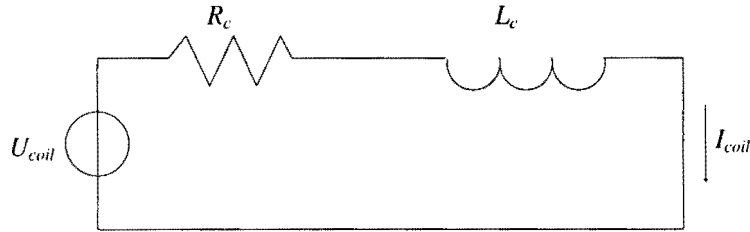
Figure 1: The process: Generating a desired current through a coil with a voltage source

For the model in Figure 1, the voltage-current relation is simply:

$$U_{coil}(t) = R_c I_{coil}(t) + L_c \frac{dI_{coil}(t)}{dt}$$

$$(1)$$

The numerical values of the coil and its series resistance are $L_c=185[\mu H]$, and $R_c=0.06[\Omega]$.

In the s-domain, (1) can be written as the transfer function $G(s)$:

$$G(s) = \frac{I_{coil}(s)}{U_{coil}(s)} = \frac{1/L_c}{s + R_c / L_c}$$

This process has a time constant of $\tau = L_c/R_c = 1/324[s] \approx 3[ms]$.

In Figure 2, the desired output current $I_{ref}(t)$ is given. This reference current form will be used throughout the document, because it represents the nominal current form of the gradient coil.
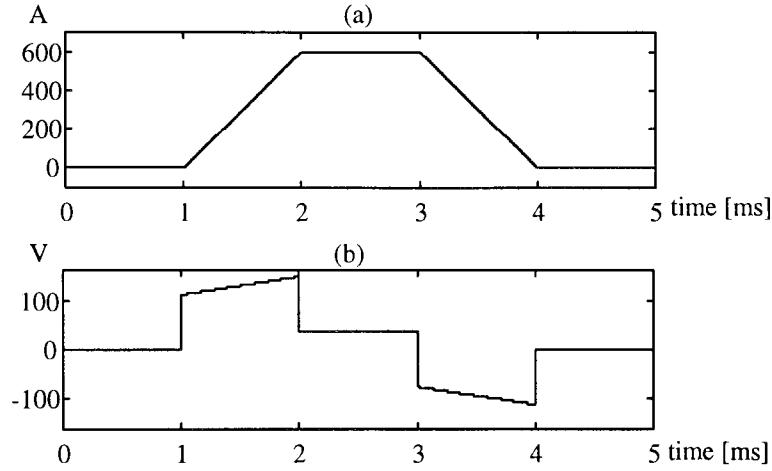
Figure 2: (a): Desired Coil Current $I_{ref}(t)$ (b): Corresponding voltage $U_{coil}(t)$

The trapezium shown in Figure 2(a) can be thought to be built up by a series of ramp functions with different slopes, that are switched on at the bending points of the trapezium:

$$I_{ref}(t) = B(\rho(t - 1ms) - \rho(t - 2ms) - \rho(t - 3ms) + \rho(t - 4ms))$$

(2)

In (2), t is in [ms], and $\rho(t) = \int_0^t u(\tau)d\tau$, with $u(t)$ the unit step function.

According to the specifications, the *error integral*

$$E(t) = \int_0^t e(t)dt$$

(3)

should not exceed 10[µAs], what is essential for the MRI-image quality:

$$|E(t)| \leq 10\mu As \qquad ,\forall t \geq 0$$

(4)

In Table 1, the specifications for $e(t)$ given at the specifications sheets [1] under the heading "Risetime" are given. The maximum range to which $e(t)$ must be limited at the trapezium top of $I_{coil}(t)$ are given for several time intervals at the flat top. The error is expressed as a fraction of the desired high level of $I_{coil}(t)$.

Table 1: Specifications for $e(t)$ at the flat top of the trapezium. $A_{max}=600A$

	Time Interval t [µs]	Error Interval e
1	0 (t < 100	-1% x A_{max} (e ≤ 1% x A_{max}
2	100 (t < 150	-0.5% x A_{max} (e (0.5% x A_{max}
3	150 (t < 500	-0.1% x A_{max} (e ≤ 0.1% x A_{max}
4	500 ≤ t	-170mA (e ≤ 170mA

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Unfortunately, just generating $I_{coil}(t)=I_{ref}(t)$ by applying the voltage following from (1) is not possible, because of voltage disturbances, components changes due to heating, etc. Therefore, the process must be embedded in a feedback loop with a controller, as will be discussed in paragraph 2.3.

2.2 The Pulse Width Modulator

The gradient amplifier, which is the voltage source used for generating $I_{coil}(t)$, is a Pulse Width Modulator (PWM) voltage amplifier. The voltages needed to generate the coil currents, are in the range of $-V^{+}=-350V$ to $V^{+}=350V$ DC. In our case the output voltage of the controller is in the range of -10 to 10V, so the voltage amplification is a factor 35.

The reason that the PWM is used, is that this is a compact and relatively cheap power amplifier. A disadvantage of the PWM is that it also generates higher order voltage harmonics because its output consists of voltage pulses. The type of PWM that is used as gradient amplifier is a full-bridge PWM, that is described in some detail in [2]. The next figure explains the principle:
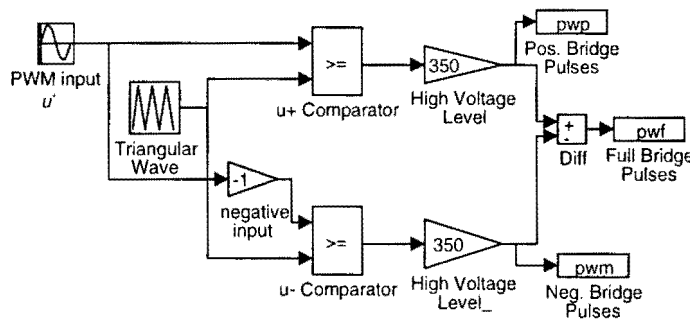
Figure 3: Functional blocks of the Full-bridge PWM

In Figure 4, the relevant signals are shown to explain how the PWM output pulse sequence is obtained in the model of Figure 3. The PWM input signal u^{+} is compared directly to the triangular wave in the positive half-bridge of the PWM. If the input is lower than the triangular wave, the output of the positive half-bridge will be 0V, and if it is higher, it will be V^{+}. The negative half-bridge does the same for the negative version of u^{+}. In the first period of the triangular wave in Figure 4, the vertical dashed lines illustrate the switching principle. The full-bridge pulse sequence is obtained by subtracting the negative half-bridge pulse sequence from the sequence of the positive half-bridge.
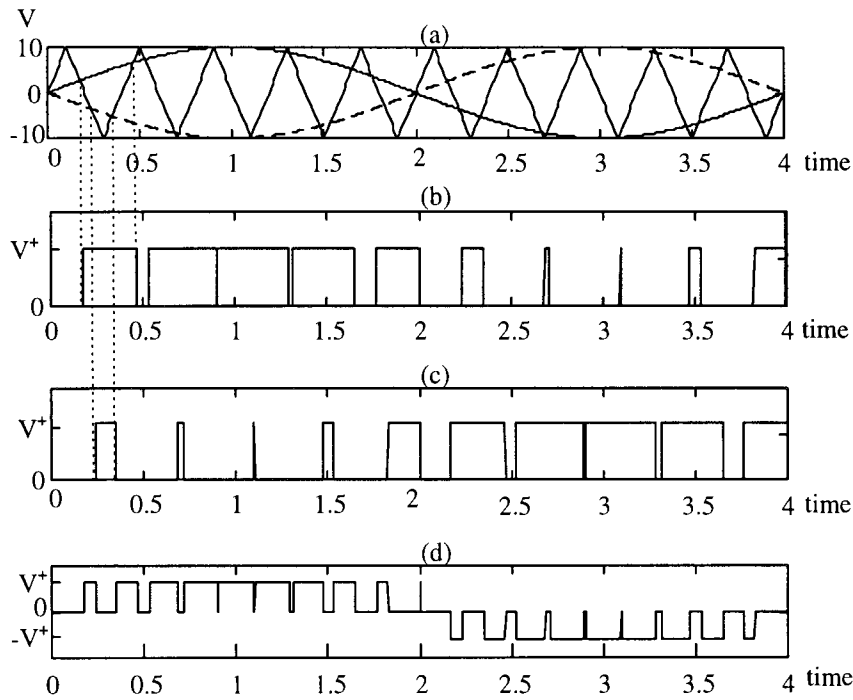
Figure 4: Full-bridge PWM signals (a): triangular wave, sinusoidal u* (full) and its negative
version (dashed); (b): Positive Half-bridge pulse sequence; (c): Negative Half-
bridge pulse sequence (d): Full-bridge pulse sequence

As is illustrated in Figure 4, the full-bridge pulse widths are proportional to the level of u^+.
The higher the input level, the wider the PW's, taking into account the sign of the input.

The output voltage of the PWM can not be applied to the gradient coil directly, since the
voltage harmonics will generate undesired current harmonics. Therefore, the PWM output is
low-pass filtered first, by two second-order low-pass sections LP1 and LP2:
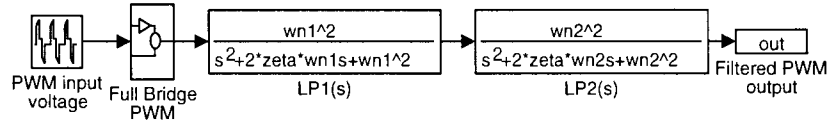
Figure 5: The PWM output voltage must be filtered because of the higher harmonics of the
pulses

The second-order low-pass filters can be expressed in the s-domain as follows:

$$\frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

(5)

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The filter parameters have the following values:

$$\omega_{n,1} = \frac{1}{\sqrt{L_1 C_1}} = 2\pi 12000$$

$$\omega_{n,2} = \frac{1}{\sqrt{L_2 C_2}} = 2\pi 24000$$

$\zeta = 0.3$

We can write for the poles of these filters:

$$p_{1,2} = -\zeta \omega_n \pm j\omega_n \sqrt{1 - \zeta^2}$$

The imaginary part is a consequence of the small damping factor $\zeta \leq 0.707$, and causes resonance at the frequency at (see [5], p. 217-219):

$$\omega_p = \omega_n \sqrt{1 - 2\zeta^2}$$

(6)

The resonance frequencies of LP1 and LP2 are $\omega_{p,1}$=10.9kHz, and $\omega_{p,2}$=21.7kHz, respectively. The bandwidth of a second-order low-pass filter is given by:

$$\omega_b = \omega_n \left[1 - 2\zeta^2 + \sqrt{2 - 4\zeta^2 (1 - \zeta^2)} \right]^{1/2}$$

(7)

Formula (7) shows that the -3dB bandwidths of the filters are $\omega_{b,1}$=17.4kHz, and $\omega_{b,2}$=34.9kHz. This means that the asymptotic attenuation is 0dB up to 17.4kHz, -40dB/decade between $\omega_{b,1}$ and $\omega_{b,2}$, and -80dB/decade beyond 34.9kHz.

The following figure gives the Bode plots of the two filters in series. At the resonance frequency of 12.5kHz, the amplification is about 6dB.
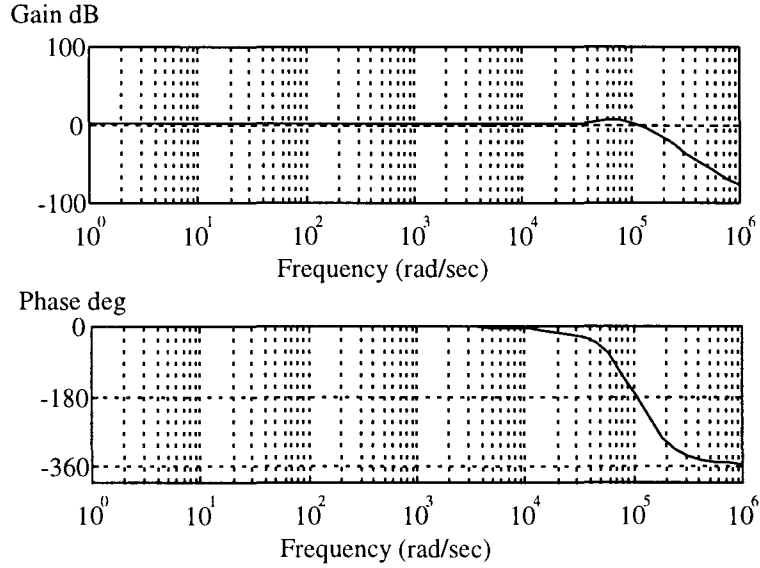
Figure 6: Bode plots of the low-pass filter combination of LP1 and LP2

2.3 The Simplified Analog Control Loop

The performance of the analog GACL will be used as a reference for the performance of the digitalized control loop. The analog control loop as discussed in this chapter, has been studied by a former graduate at MBS (see [2]). Its main characteristics are mentioned in this chapter. The analog control loop is a simplified version of the GACL, existing gradient amplifier control loop (see [1]). Figure 7 shows the elements of this simplified model:
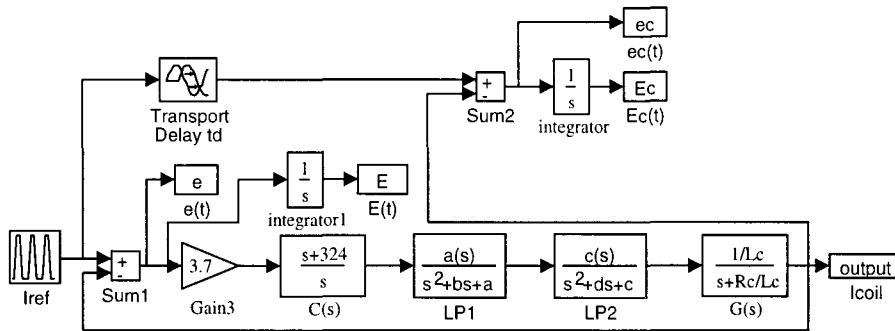
Figure 7: Model for closed-loop transfer function

The filters LP1 and LP2 are the second-order low-pass filters, that are necessary to filter out the higher harmonics of the Pulse Width Modulator (PWM). For simplicity, the filter coefficients are called a,b,c, and d here, instead of the expressions in ζ and ω_n as in the previous paragraph, so $a=(2\pi12000)^2$, $b=1.2\pi12000$, $c=(2\pi24000)^2$, and $d=1.2\pi24000$. The controller $C(s)$ is a simple PI controller, that compensates for the slowest time constant of the process, $L_c/R_c=1/324$[s], and reduces the steady-state current error.

The PWM itself is not modeled in detail in this simplified model, but its inherent voltage gain $PWM(s)=35$ is joined to the controller gain (3.7/35) in the block $Gain3$ in Figure 7. This is justified because in the present gradient chain, four PWM modules are connected in parallel, resulting in a current ripple caused by the voltage harmonics with a first harmonic at 100kHz (see [2] for the description of this so called Multi-Phase principle). Because the cut-off frequency of LP1 in series with LP2 is much lower, this ripple can be neglected in the simplified model.

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2.3.1 Current Error and Propagation Delay Time

First of all, let's define the current error as:

$$e(t) = I_{ref}(t) - I_{coil}(t)$$

In Figure 8, the output signal, which is the coil current $I_{coil}(t)$, the current error $e(t)$, the delay-corrected coil current error $e_c(t)$, and the integral of the delay corrected error $E_c(t)$ are plotted. The reason for the delay correction will become clear later on in this paragraph.
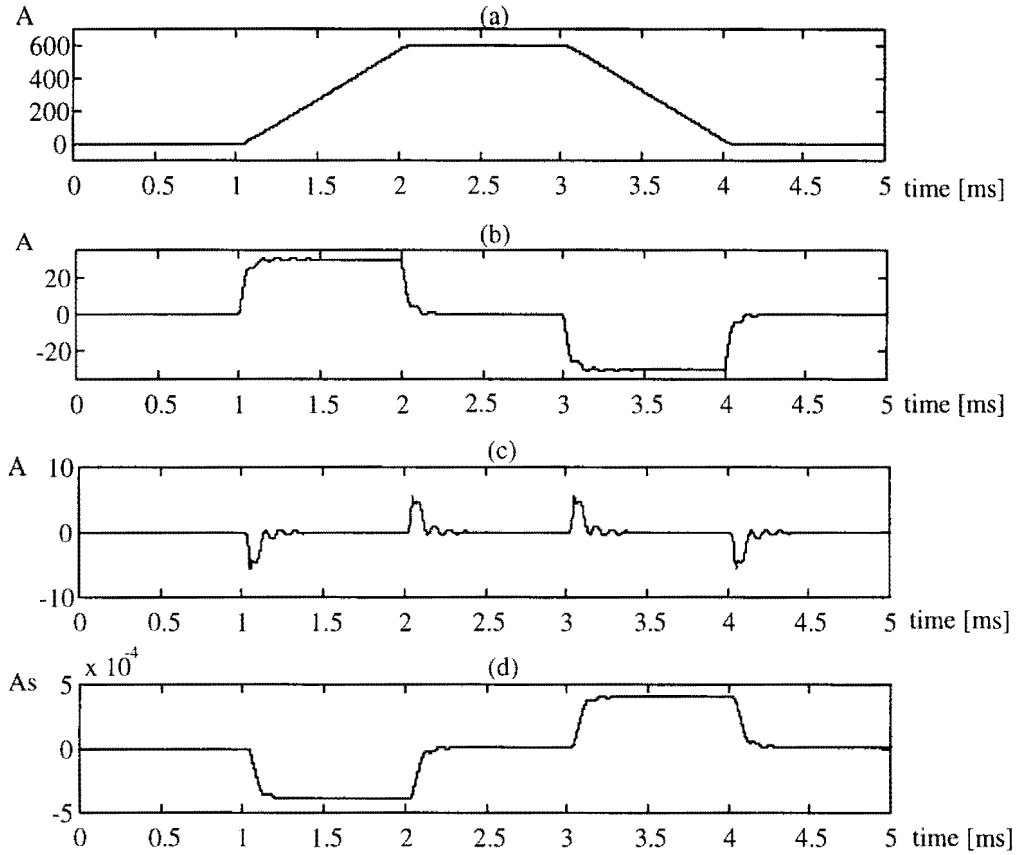
Figure 8: (a): $I_{coil}(t)$ (b): $e(t)$ (c): $e_c(t)$ (d): $E_c(t)$

The delay-corrected current error $e_c(t)$ is given by the delay-corrected input signal (delayed version of $I_{ref}(t)$) minus the output signal (the coil current $I_{coil}(t)$). $I_{ref}(t)$ is shifted over the propagation delay time of the control loop for a ramp function t_d, which is the same in steady-state for every ramp-shaped $I_{ref}(t)$. Its maximum value is 5.66[A]. As a consequence of the constant delay time, the final value of the current error, given by (9), reaches a constant value if a ramp is fed to the input of the control loop. This is shown in Figure 8 (b).

$$e(\infty) = \lim_{t \to \infty} e(t)$$

The following figure illustrates the relation between the constant steady-state delay time t_d for a (saturated) ramp input and the resulting $e(\infty)$:

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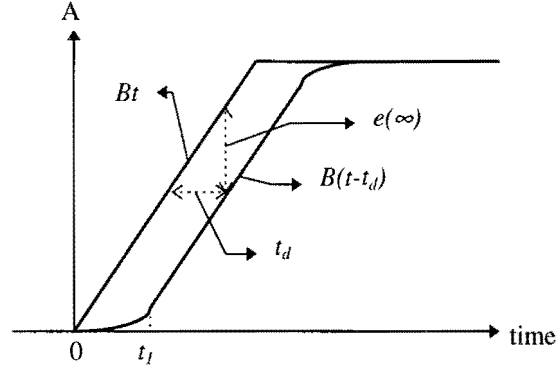
Figure 9: Explanation of the relation between the steady-state delay time t_d and the steady-state error for a ramp input Bt; t_l is the settling time

From Figure 9, it follows that:

$$e_c(t) = e(t) - e(\infty)$$

$$(10)$$

So, if $I_{ref}(t)$ consisting of a combination of ramp functions is shift over the propagation delay time t_d, we can put the current error to zero in steady-state, because of the subtraction of the constant steady-state error.

If the constant component $e(\infty)$ is subtracted from $e(t)$, the result is the inverse of the current transients. These transients are related to the poles of the closed-loop transfer function that will be given in (12). Because we deal with a stable system, the transients die out in time.

The delay time of the control loop for a ramp-shaped $I_{ref}(t)$ can be calculated by applying the final value theorem to $e(t)$. First, the open-loop transfer function is given, which looks like:

$$H_o(s) = \frac{K_p}{\tau R_c} \cdot \left(\frac{s\tau + 1}{s} \right) \cdot \frac{1}{\left(\dfrac{s^2}{a} + \dfrac{b}{a}s + 1 \right)} \cdot \frac{1}{\left(\dfrac{s^2}{c} + \dfrac{d}{c}s + 1 \right)} \cdot \frac{1}{\left(\dfrac{L_c}{R_c}s + 1 \right)}$$

$$(11)$$

The expression for the closed-loop transfer function can be calculated from $H_o(s)$ as follows:

$$H_{cl}(s) = \frac{H_o(s)}{1 + H_o(s)}$$

$$(12)$$

The factor K_p is the factor 3.7 before the controller in Figure 7. The time constant τ is equal to $\tau = L_c/R_c = 1/324$[s].

In (11) we can see that the (DC)-open-loop gain is given by:

$$K_v = \frac{K_p}{\tau R_c} = \frac{K_p}{L_c}$$

$$(13)$$

Numerically, this yields K_v=20,000. For a ramp-shaped $I_{ref}(t)$ with slope B, the final value theorem applied to the error signal $e(t)$ results in a steady-state error of:

$$e(\infty) = \lim_{t \to \infty} e(t) = \lim_{s \to 0} se(s) = \lim_{s \to 0} s \frac{B}{s^2} \left(1 - H_{cl}(s)\right) = \frac{B}{K_v} = Bt_d$$

(14)

The propagation delay time for a ramp input is found to be t_d=1/K_v=50[μAs]. The constant steady-state error is a result of the presence of just one integrator in the open-loop transfer function. For the analog gradient chain, the trapezium ramp B is 600[A/ms], and t_d=50[μs], therefore $e(\infty)$ is 30A.

If an input ramp function is applied, integrating $e(t)$ will result in a steady-state ramp for $E(t)$, because of the non-zero steady-state value $e(\infty)$. A better idea is to integrate $e_c(t)$, which will result in a constant steady-state value for $E(t)$. Therefore, criterium (4) will be applied to $E_c(t)$ instead of to $E(t)$.

In Figure 8, we can see that the negative level of $E_c(t)$ is -390[μAs], and the high level is at 400[μAs], which is about a factor 40 too large according to (4).

2.3.2   Bode Plots and Pole-Zero Maps

In the following figures, it is illustrated how the PI controller $C(s)$ in Figure 7 influences the open-loop Bode plots. First, the Bode plots for $H_o(s)$ are plotted in Figure 10. The pole-zero map of this transfer function is plotted in Figure 11.
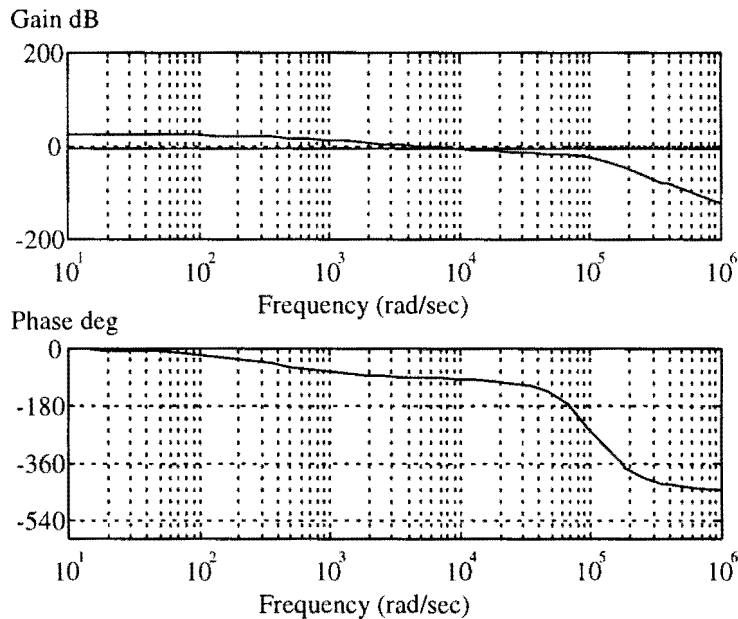
Figure 10: $H_o(s)$ without the controller

Figure 10 shows a rather low crossover frequency of 5424rad/s, and a considerable phase distortion for low frequencies. This is because the slow time constant of the coil-resistance plant (L_c/R_c=1/324[s]) is not compensated.

11
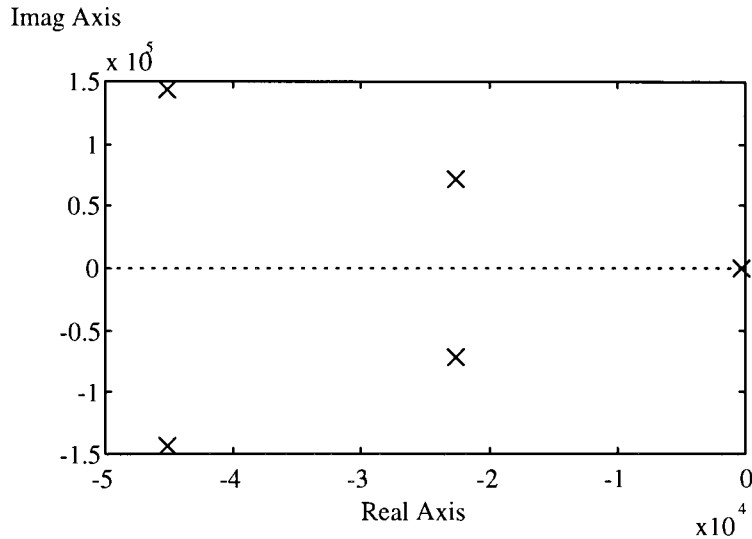
Figure 11: Pole-Zero map of $H_o(s)$ without the controller

In the pole zero map in Figure 11, the pole near zero belongs to the time constant R_c/L_c of the plant. The other pole pairs are those of the low-pass filter sections LP1 and LP2.

In the following two figures, the same plots are given as in Figure 10 and in Figure 11, but now for the case that also the PI controller is part of $H_o(s)$. Figure 12 shows the new open-loop Bode plots.
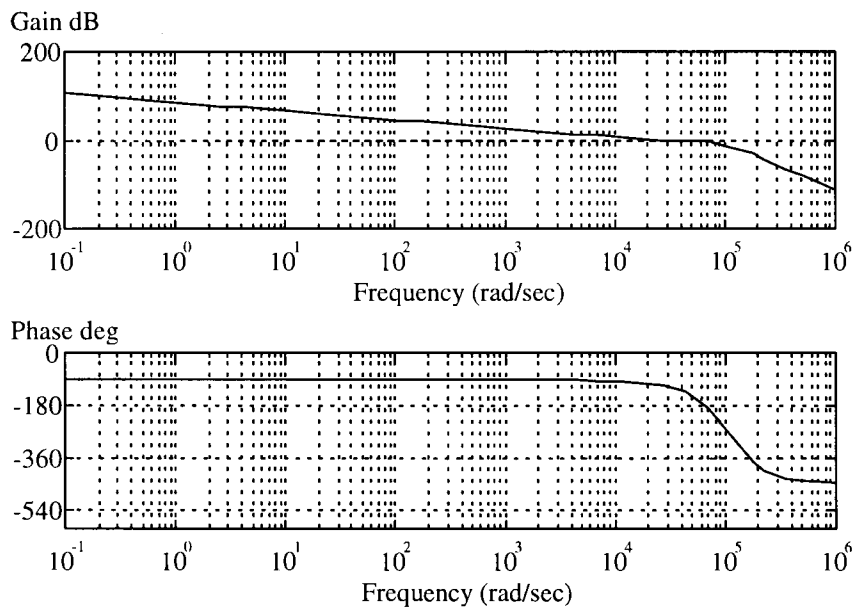
Figure 12: $H_o(s)$ with the PI controller; Gm=4.29dB (ω=6.809e4), Pm=74.2deg (ω=2.182e4)

The phase margin is 74.2(at ω=3.36kHz, which is an acceptable value.

In the next Root Locus diagram, we see the pole of the controller in s=0. The other pole and the zero near s=0, are a result of the time constant τ=1/324[s] that is both in the numerator of the controller and in the denominator of the plant. The figure shows that for values of K_p larger than about 6.2, the system will be unstable, because two branches of the root locus are going into the right half plane of the complex plane.

12
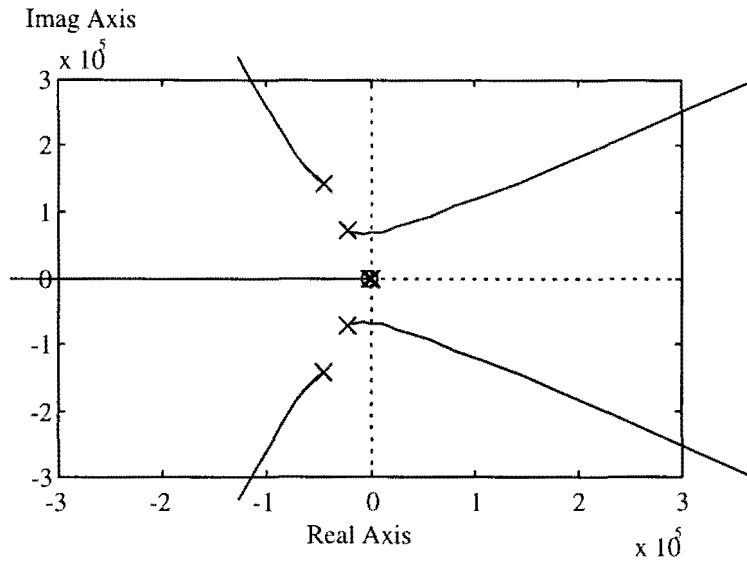
Figure 13: Root locus of $H_o(s)$ with the PI controller

In the last but one figure of this section, the pole-zero pattern of the poles of $H_{cl}(s)$ is given. The poles determine the exponential decay rates and the oscillation frequencies of the transients, governing $e_c(t)$ as plotted in Figure 8(b). The poles closest to the Imaginary Axis, called the dominant poles, cause badly damped transients.
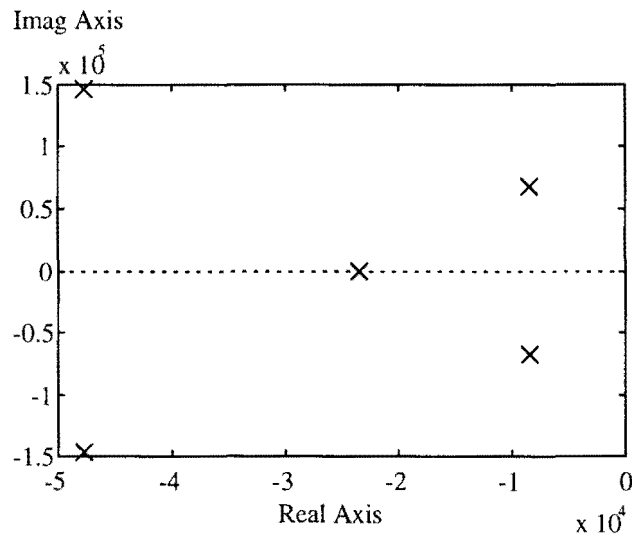
Figure 14: Pole-Zero map of $H_{cl}(s)$ including the PI controller

In the last figure of this section, the Bode plots for $H_{cl}(s)$ are given. The resonance peak at 10kHz is a result of the addition of the low-pass filters to $H_o(s)$. The system bandwidth (-3dB) is about 10kHz.

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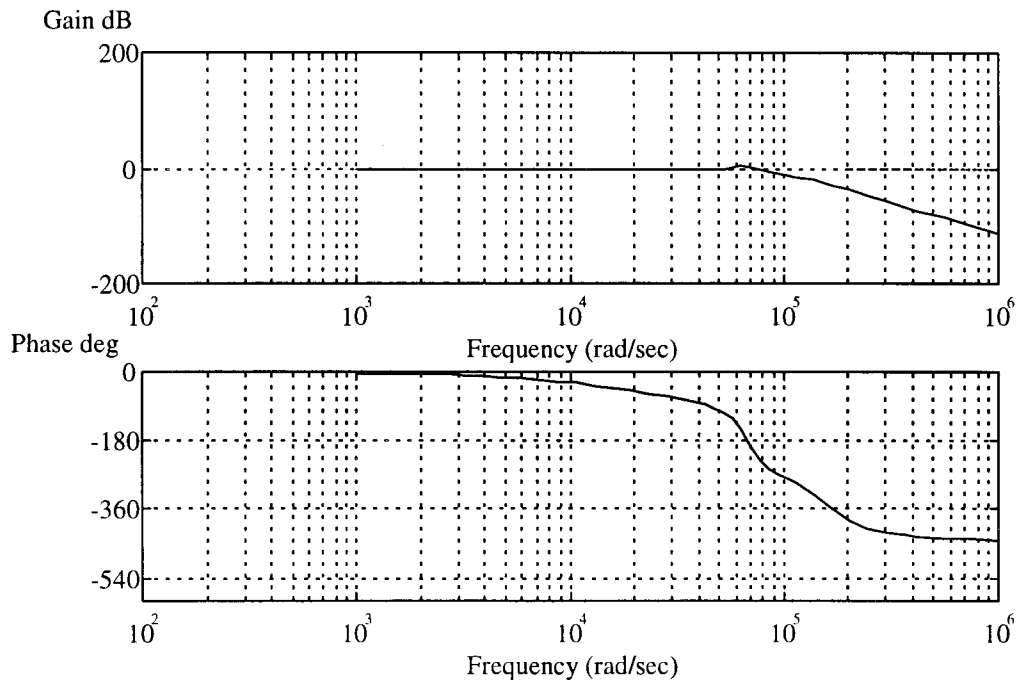
Figure 15: Bode plots of $H_{cl}(s)$ of the analog GACL

2.4 Performance of the Analog Control Loop

In this chapter, the analog control loop has been analyzed. Even after correction for the closed-loop propagation delay time, $E_c(t)$ doesn't meet the criterium, but it has a maximum of 400[μAs], a factor 40 too large.

3. The Digitalized Control Loop

In this chapter, the analog GACL of Figure 7 is digitalized straightforwardly, as shown in Figure 16. A time discrete controller $C(z)$ is designed based on the analog controller. Internally, binary representations of numbers are used by the digital controller. Therefore, analog signals must be sampled and digitalized first, using ADC's. In the digitalized GACL, the ADC is placed in the error path. Before the ADC, an anti-aliasing filter $B(s)$ is necessary to limit the signal band width. At the output of $C(z)$, a DAC in combination with a ZOH is needed to make the digital and time discrete output of the computer analog and time continuous.
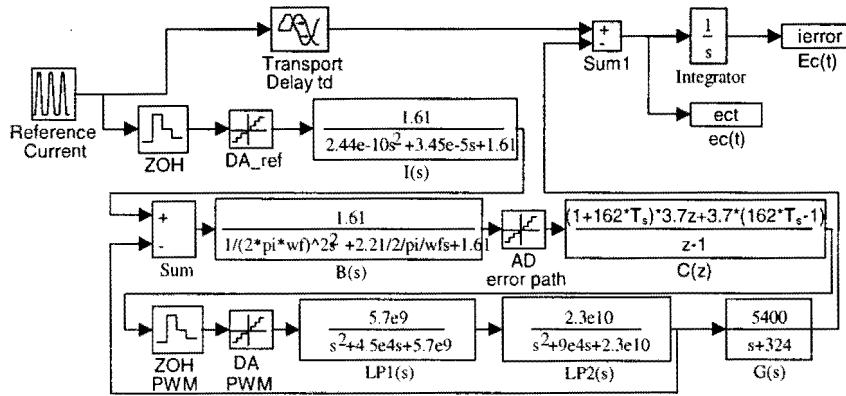
Figure 16: Model of the digitalized GACL

The model shown in Figure 16 is the same as the model used in the master report [2], except for the quantization error correction unit that has been omitted, because this unit didn't seem to be useful [2].

3.1 Components of the Digitalized System

3.1.1 The Digitalized PI Controller

If a digital controller has to be found if an analog controller is already available, the analog controller can be transformed to the discrete domain using a Tustin transformation:

$$s = \frac{2}{T_s} \frac{z-1}{z+1}$$

(15)

The transfer function of the transformed PI controller $C(s)$ of Figure 7 becomes in the z-domain:

$$C(z) = 3.7 \frac{(1+162T_s)z + 162T_s - 1}{z-1}$$

(16)

The sampling period is taken equal to the PWM cycle duration, thus $T_s = T_z = 40[\mu s]$.

3.1.2 The Analog to Digital Converter

The principal feature of this control scheme is that the ADC is not placed in the feedback path as usual, but in the error path instead, because of the reduced range of $e(t)$ (about 200A) compared to the range of $I_{coil}(t)$ (about 1200A). The number of bits that can be saved is

$$\log_2 \frac{1200}{200} \approx 2.6 \text{ bits for the ADC.}$$

3.1.3 Anti-Aliasing Filter

Before the AD conversion of the analog $e(t)$, this signal is bandwidth limited by a second-order Bessel filter $B(s)$ in Figure 16.

Bessel filters are filters with a linear phase characteristic ($\varphi=k\omega$, k is a constant) in a large frequency range, therefore not affecting signals too much. The general expression for a Bessel filter is given by (see [3]):

$$H(s) = \frac{\omega_n^2}{s^2 + \sqrt{3}\omega_n s + \omega_n^2}$$

(17)

or, equivalently:

$$H(s) = \frac{1.61}{\left(\dfrac{s}{\omega_b}\right)^2 + \dfrac{2.21}{\omega_b}s + 1.61}$$

(18)

The maximum bandwidth for $B(s)$ as in (18) depends on the sampling frequency $f_s=1/T_s$ of $C(z)$ and ZOH. According to the Nyquist criterium, signals with frequencies higher than $f_s/2$ must be damped enough by $B(s)$, so the cutoff frequency should be at least $\omega_b=f_s\pi$.

The cutoff frequency of $B(s)$ is chosen $\omega_b =15000\cdot2\pi$ (-3dB bandwidth). This bandwidth is not obeying the Nyquist sampling law, but a filter with a lower cut-off frequency will result in more oscillatory behavior of the closed-loop system. Besides, the frequency contents of the $I_{ref}(t)$ trapezium is concentrated between 200Hz and 10kHz, so no aliasing will take place, because frequencies above the Nyquist frequency of 12.5kHz are not present.

3.1.4 Interpolation Filter

As a consequence of placing the ADC in the error path, $I_{ref}(t)$ that is generated digitally, has to be DA converted first to calculate the analog $e(t)$. The DA conversion of $I_{ref}(t)$ is performed by a zero-order hold (ZOH) circuit, in combination with a DAC. The DA converted signal is filtered with an interpolation filter $I(s)$. For $I(s)$, a second-order Bessel filter is chosen with an appropriate cutoff frequency, depending on the sampling rate of the DA converter in the reference path.

3.1.5 Digital to Analog Converter and ZOH at Controller Output

Also a DAC is placed in the open-loop chain, representing the DA behavior of the PWM for the case that its pulse widths are digitalized (to be treated in chapter 8).

3.2 Simulation with Digitalized GACL

In this paragraph, a simulation is carried out with the model shown in Figure 16. The sample frequency is 25kHz, equal to the PWM basic frequency, and $B(s)$ has a cutoff frequency of 15kHz.

In Figure 16, the number of bits for the ADC and the DAC is 14, as in [2].

The delay of the loop after $I(s)$ remains $t_d=50[\mu s]$, as will be proven in chapter 4.

Figure 17 shows the signals $e_c(t)$ and $E_c(t)$ for the case that the trapezium-shaped $I_{ref}(t)$ is fed to the control loop. According to the simulation, the first high level of $E_c(t)$, which corresponds with the rising slope of the $I_{ref}(t)$, is at a level of about 650[μAs], which is a factor 65 too large. Furthermore, the peak of $e_c(t)$ is 13.99[A] now, instead of the 5.66[A] that was found in paragraph 2.3.1 for the analog GACL. In plot (d), $E_c(t)$ is shown for larger t. It shows that a drift in $E_c(t)$ occurs.
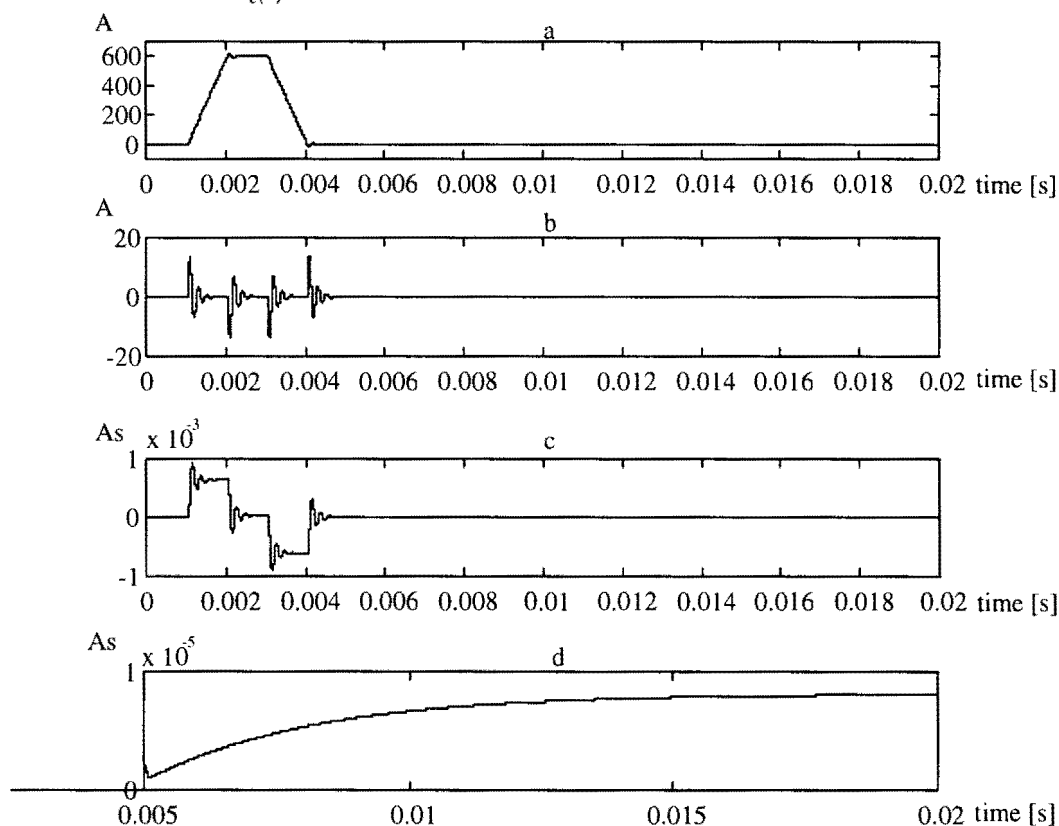
Figure 17: GACL with digital controller for model in Figure 16 with 14 bits ADC and DAC, and $T_s=T_z(a)$: $I_{coil}(t)$ (b): $e_c(t)$ (c): $E_c(t)$ (d): $E_c(t)$

3.3 Conclusions

Studying the simulation results in Figure 17 of the digitalized GACL in Figure 16 show three major differences with the results of the analog GACL in Figure 8. The transient signal $e_c(t)$ has deteriorated, the high level of $E_c(t)$ has increased, and a drift appears in $E_c(t)$ after $I_{ref}(t)$ has become zero. These effects seem to be typical for a loop with a digital controller, a ZOH, an ADC, and a DAC. In the remainder of this thesis, they will be analyzed in detail, and solutions to the problems are proposed.

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4. Open-loop Delay and Transients

If the analog GACL is digitalized, some extra delays are introduced to $H_o(s)$. For instance, the ADC needs a certain time to perform a conversion, the control algorithm will need some time to be executed, there is a time needed to calculated the PWM switching times, the PWM using sampling of the input implies a delay by itself, and the IGBT's of the full-bridge need a fixed time to turn on or off. In the first paragraph of this section, a time table is given summarizing all the recognized delay times so far.

Adding an extra delay time T to $H_o(s)$ will result in a reduced phase margin, as will be discussed in the second paragraph of this chapter. Less phase margin will result in worse transients behavior. For a too large extra delay time, the system will become unstable, because one complex pole pair are shifting into the right half of the complex plane. In the last paragraph of this section, the effect of the extra delay T on the transients is studied both analytically and by simulation.

4.1 Timing Table

Because the PWM must be able to give its maximum output, there should be no limitations on the individual switching times in the half PWM period that they belong to. All the preparations to calculate the next PWM switching moments must be scheduled before the beginning of each PWM cycle, if one PWM-input sample is used to calculate the switching moments for the period $(T_{s,PWM}=T_z)$. In the case that a different sample is used for each switching time, the preparations have to occur before their specific quarter the PWM cycle. In the timing table below, the order in which the events preceding the beginning of the PWM cycle must be executed is given:

Table 2: Timing Table for digital controller and PWM.

TIME EVENT	Conversion Time $\longrightarrow$	Alg. Calc. Time $\longrightarrow$	Switching Times Calc $\longrightarrow$
AD Conversion	▓▓▓		
Control Algorithm DSP		▓▓▓	
Calculation of the PWM switching times			▓▓▓
Time till beginning of PWM cycle: T_p	▓▓▓▓▓▓▓▓▓▓▓▓▓▓▓▓▓▓▓▓▓▓▓▓		

For the design of a digital controller, it is essential that the total delay between taking the sample and the beginning of the PWM cycle is always the same. Therefore, the maximum durations must be taken for the delay times in Table 2. As a result, the conversion must start at a fixed time before the beginning of the PWM cycle. This time will be called T_p, the preparation time. The next figure shows how this time is related to the (virtual) PWM triangular wave:
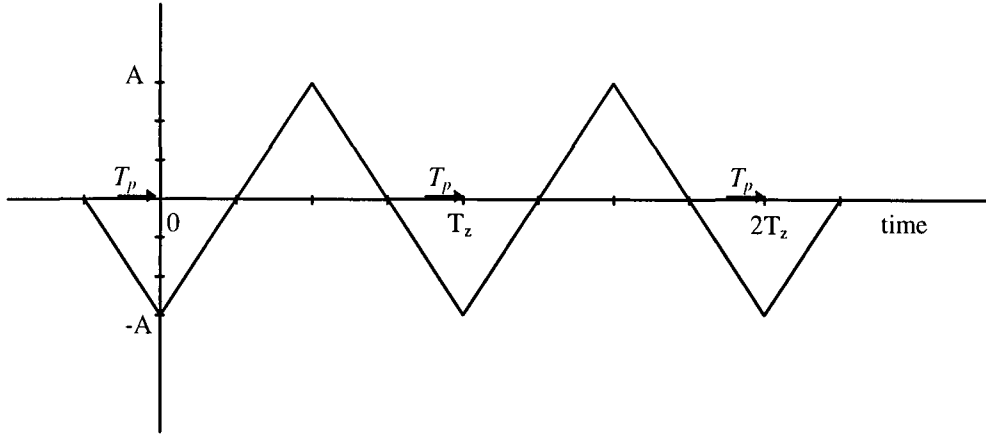
Figure 18: Preparation times between the sampling moments and the beginning of the PWM cycles, sampling once per PWM cycle

4.1.1 Choice of the AD-Conversion Sampling Frequency

The highest realizable sampling frequency of the ADC in the error path must be high enough, because, as a rule of thumb, the AD conversion time is the inverse of the highest sampling frequency of the ADC. A higher AD conversion rate is not a problem, because no high power signals are involved with the AD conversion, on the contrary to the high powers that are involved with the switching IGBT's of the PWM, which is in fact the ZOH at the output of $C(z)$. The PWM switching frequencies are limited to about 25kHz, because of power losses. A sampling frequency for AD conversion of e.g. 100kHz could be chosen. Choosing such a high frequency, which is much higher than needed for the closed-loop bandwidth of about 10kHz, gives us the possibility to do part of the low-pass filtering digitally, resulting in an analog low-pass (Bessel) filter with a less sharp cut-off characteristic, because the -3dB point has to lie at the Nyquist frequency of 50kHz now. Within the computer, the sampling frequency can be decreased to about 25kHz after the digital filtering (cut-off frequency of about 10kHz) has taken place. This combination of a digital low-pass filter and a sampling rate reduction is called a *decimator*.

4.2 Stability Requirements

What has to be studied first, is what the maximum value of the extra open-loop delay time T can be so that enough phase margin is kept. In each case, the preparation time T_p discussed in the former paragraph must fit within the maximum T. If a certain minimum phase margin is required, let's have a look at what the maximum T is allowed to be. Considering a general open-loop transfer function $H_o(s)$, we can proceed as follows. First, we have to calculate the phase margin of $H_o(s)$ without the delay term e^{-sT}. The delay term which modulus is unity doesn't change the frequency for which the magnitude plot of $H_o(s)$ crosses 0dB. Finding the phase margin for $H_o(s)$ now results in simply decreasing the phase margin of the case that no delay was present by $\omega_c T$, in which ω_c is the crossover frequency for $H_o(s)$. In formula, we can write now:

$$PM(H_o(j\omega))_T = PM(H_o(j\omega))_{T=0} - \omega_c T$$

(19)

Instability is reached for the value of T where $PM(H_o(j\omega))_{T=0}$ equals zero.

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4.3 Theoretical Calculation of the Transients

In this paragraph, the effect of an extra delay factor (e.g. due to digitalization) in $H_o(s)$ on the transients in $I_{coil}(t)$ will be studied. The roots of the characteristic equation of the control loop are calculated for different values of T. For the calculation of the system poles and the transients, a second-order Padé approximation is used for the delay factor:

$$e^{-sT} \cong \frac{1 - s\frac{T_s}{2} + s^2 \frac{T^2}{12}}{1 + s\frac{T_s}{2} + s^2 \frac{T^2}{12}}$$

$$(20)$$

Because we are dealing with a delay T present in the digital control structure as in 3.2, also an anti-aliasing Bessel filter with a cutoff frequency of 15kHz is placed in the loop:
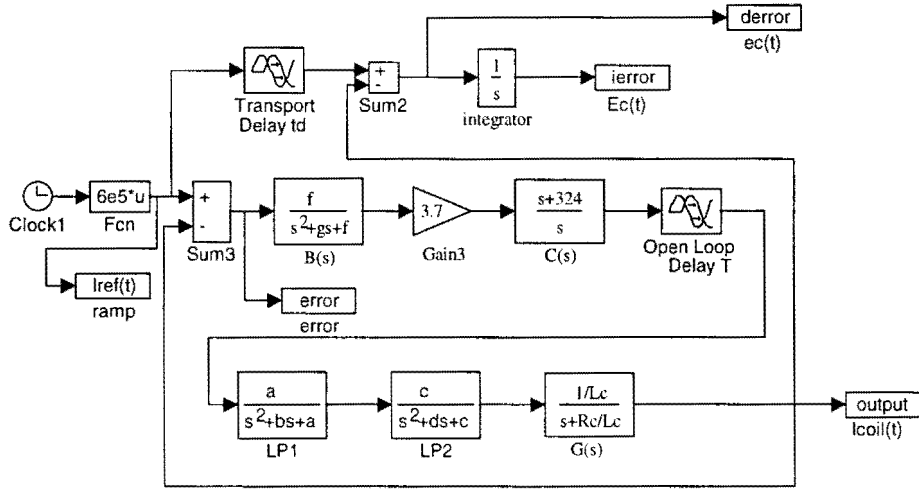
Figure 19: GACL with anti-aliasing Bessel filter and open-loop delay factor

The trapezium shaped $I_{ref}(t)$ consists of a number of time-shifted ramp functions, so the output transients can be studied by feeding a simple ramp-shaped $I_{ref}(t)$ to the control loop. The output is calculated by multiplying the Laplace transform of $I_{ref}(t)$ with $H_{cl}(s)$. Observing Figure 19 and using (20), $H_o(s)$ is found to be:

$$H_o(s) \cong acfK \frac{1 - s\frac{T}{2} + s^2 \frac{T^2}{12}}{s(s^2 + bs + a)(s^2 + ds + c)(s^2 + gs + f)(1 + s\frac{T}{2} + s^2 \frac{T^2}{12})}$$

$$(21)$$

$H_{cl}(s)$ is expressed in $H_o(s)$ as in (12).

The system poles are now calculated by equating the denominator of $H_{cl}(s)$ to zero. Because we have to find the roots of a 9th order polynomial, a computer is used to calculate the roots for different values of T. Knowing the complex conjugated and the real valued roots of the system characteristic equation, a partial fraction can be performed to find the corresponding time transient signals. If $I_{ref}(t)$ is a ramp function Bt which Laplace transform is B/s^2, $I_{coil}(t)$ can be found by partial fraction of $H_{cl}(s)$ multiplied by B/s^2. The transients are those fraction

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terms belonging to the poles of $H_{cl}(s)$. The fraction terms belonging to B/s^2 are the Laplace transform of the steady-state output of $H_{cl}(s)$, which is the ramp $I_{ref}(t)$ minus the steady state-error $e(\infty)$.

In the next plot the positions of the slowest complex pole in the complex plane are shown for values of T increasing from $T=0$ to $T=55[\mu s]$. The slowest complex pole belongs to the worst damped transient, and is called the dominant pole for that reason.
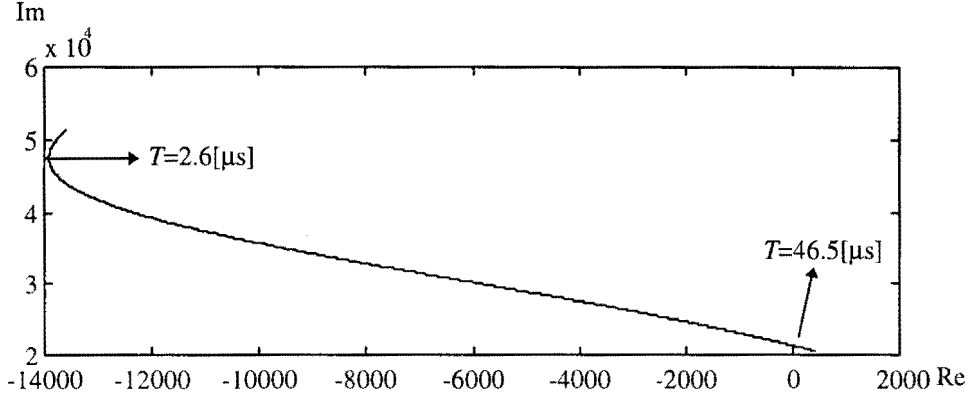
Figure 20: Slowest pole moving in the complex plane for $T=0$ to $T=50[\mu s]$

The verge of stability is reached for $T \approx 46.5[\mu s]$, for which an undamped oscillatory transient will be part of $I_{coil}(t)$. This is in accordance with (19), since for $H_o(s)$ of Figure 19, the phase margin for the case $T=0$ equals $56.76°$ at $\omega_c=3.4kHz$.

Calculating the roots of the system's characteristic equation resulted in only single complex pole pairs, and in single real poles. The corresponding transients are calculated now using partial fraction theory.

Unrepeated complex poles $a=\alpha+j\beta$ are present within the denominator of $H_{cl}(s)$ as:

$$(s-a)(s-\overline{a}) = (s-\alpha)^2 + \beta^2$$

The corresponding transient for this denominator factor in the time domain yields:

$$h_a(t) = e^{\alpha t}\left(\text{Im}(Q_a)\cos\beta t + \text{Re}(Q_a)\sin\beta t\right)$$

$$(22)$$

where $\text{Im}(Q_a)$ and $\text{Re}(Q_a)$ are the imaginary and the real parts of Q_a respectively:

$$Q_a = \frac{1}{\beta}\lim_{s \to a}\left((s-\alpha)^2 + \beta^2\right)H_{cl}(s)$$

Also unrepeated negative real poles may be present. An unrepeated real pole $s=a$ corresponds to the time signal:

$$h_a(t) = e^{at}$$

$$(23)$$

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An important conclusion is that every fraction is proportional to B, the slope of the input ramp. Thus also the transients will increase in amplitude if B increases, i.e. if the rise-time becomes shorter.

4.4 Simulations of the Transients for Different T

The formulas above are used to calculated the transients for different values of the extra delay time T in $H_o(s)$. The total transient signal and the transient corresponding to the dominant complex pole are shown in the next figure for four values of T: 0, 4[μs], 10[μs], and 20[μs]. The transient signals calculated with (22) and (23) seem to be almost equal to the results of a Simulink simulation with the model in Figure 19 using the same values of T. This justifies the use of the Padé approximation for the delay factor for the theoretical analysis.
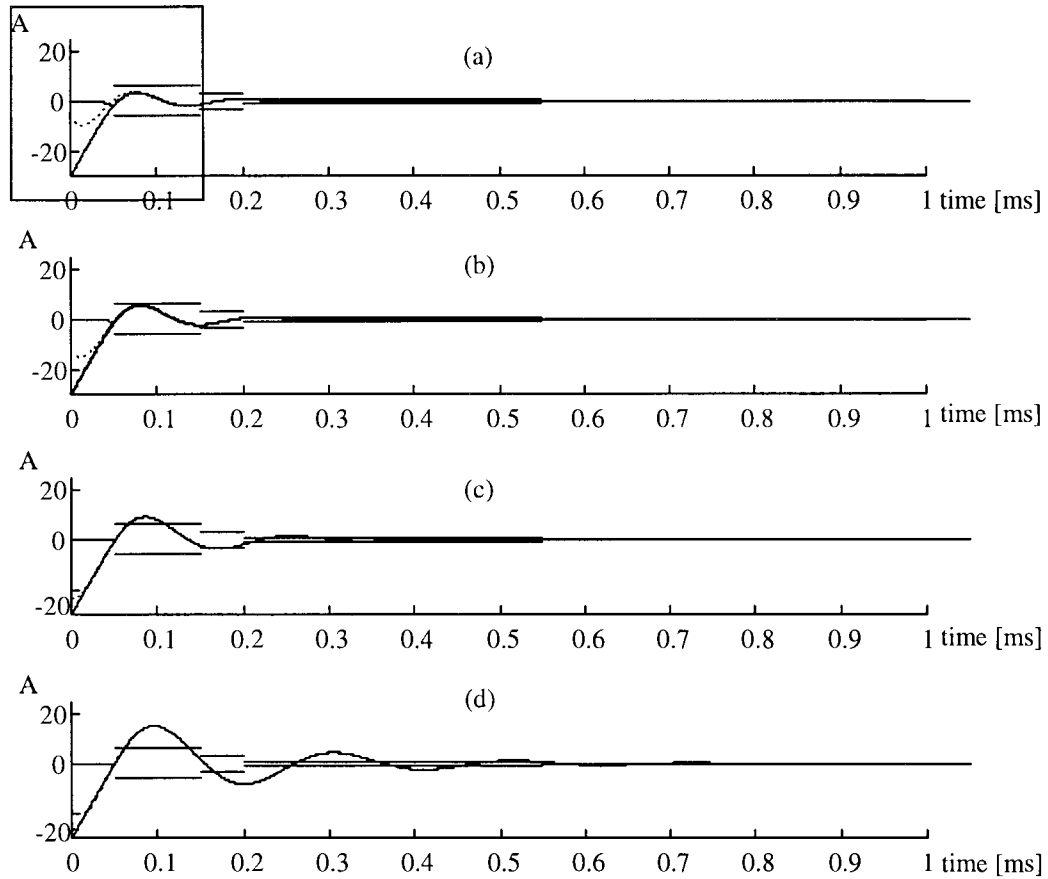
Figure 21: Transient signals for different delay times. Line types curves: full: transient calculated with Simulink; dashed-dotted: analytically calculated transient; dotted: transient corresponding to dominant complex pole. Delay times T: (a): $T=0$ (b): $T=4[μs]$ (c): $T=10[μs]$ (d): $T=20[μs]$

From Figure 21, it can be concluded that the dominating complex pole determines the behavior of the transient as expected. The result found with Simulink ($e_c(t)$ in Figure 19), is equal to the analytically calculated transient, except within the time interval $(0, t_d)$, with t_d=50[μs], the closed-loop delay time. In this interval, the Simulink values are equal to the negative output of the system, because the delay block for the reference signal in Figure 19 then gives a zero output. In the analytical calculation, $I_{ref}(t)=Bt$ is subtracted from $I_{coil}(t)$ beginning at $t=0$ (not at $t=t_d$), and the $e(\infty)$ is added to the output.

In Figure 21, also the specification bars from Table 1 are shown. Because the transients are the same for every ramp input (only the sign may be different), it doesn't matter that $I_{ref}(t)$ is chosen to be a continuous ramp function starting at $t=0$ instead of a trapezium as in Figure 2.

Because $I_{coil}(t)$ in Figure 19 follows $I_{ref}(t)$ delayed over t_d, also the intervals of t in Table 1 must be shifted forward in time over $t_d=50[\mu s]$. The corresponding specification bars are shown in Figure 21. For a delay time $T=0$, all the specifications are met, except for the third interval of t.

In the next figure, the maximum value of $e_c(t)$ is shown per time interval for as a function of T:
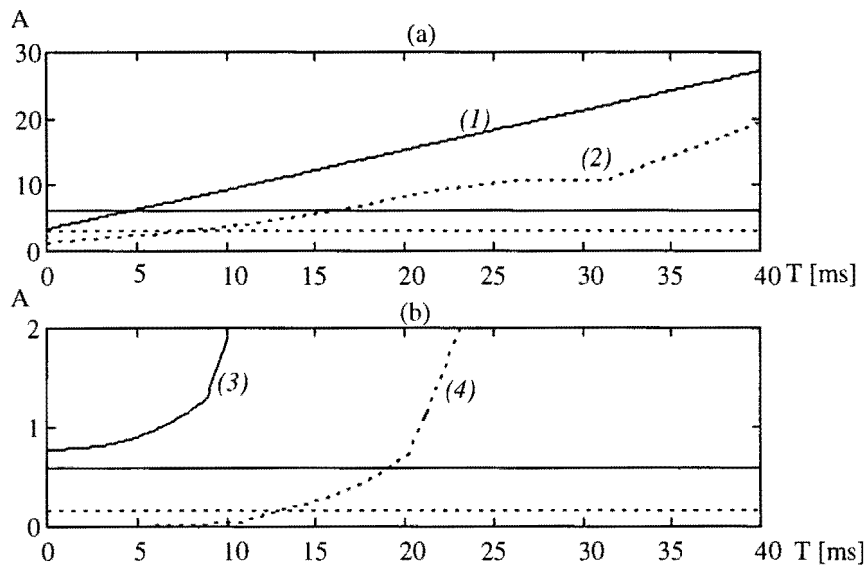
Figure 22: Maximum absolute $e_c(t)$ per specification interval and spec. borders: numbers indicated in brackets correspond to interval numbers in Table 1

Figure 22(b)(3) shows that the specifications are never met within the third time interval. For the other time intervals, there is an obvious relation between the increasing delay time T and the maximum value $e_c(t)$ in the interval. In Figure 22(a), $e_c(t)$ will violate the specs of the first time interval for all values of T larger than about 4[µs]. Using (19), this means that the phase margin should be at least 52°. Because the specs are violated for the smallest T within the first interval for $T=4[\mu s]$ (after the third interval), this is the critical delay time. As remarked earlier in this chapter, if the rise-time decreases, i.e. B increases, the overshoot will grow proportionally to B.

4.5 Conclusions

From the considerations in this chapter, it can be concluded that the open-loop delay factor should not be larger than about 4[µs] for the current control loop setup if good enough tracking of $I_{coil}(t)$ is required. This is not very much, since the PWM with an update frequency $1/T_{s,PWM}$ of 25kHz already introduces a larger amount of ZOH delay, see e.g. Figure 27. In the chapter 6, PWM schemes with higher $T_{s,PWM}$ will be derived, resulting in a reduced ZOH delay time of the PWM.

In chapter 7, a completely different approach is studied to reduce the transients in $I_{coil}(t)$ due to the tracking of $I_{ref}(t)$. Feedforward will be applied there to adapt $I_{ref}(t)$ for the filters it is fed to.

5. Analysis of Steady-state Errors and Delays

In this chapter, $H_o(s)$ of the GACL is extended with some extra elements to derive some general expressions for the final values $e(\infty)$ and $E_c(\infty)$ of $e(t)$ and $E_c(t)$, respectively. In paragraph 5.2 $H_o(s)$ is extended with a general delay factor T, and an arbitrary number (N) of second-order low-pass filters may be present. In paragraph 5.3, a zero-order hold circuit (ZOH) is also added to the generalized control loop model.

If an extra low-pass filter is needed in the loop based on Figure 7, an anti-aliasing filter for example, the formulas that are derived in this chapter can be used to calculate $e(\infty)$ and $E_c(\infty)$. Also the steady-state effects of a ZOH and some delays that are inherent to a discrete controller, can be studied with the formulas derived in this chapter.

It must be stressed, that the theory that will be discussed in this chapter, is only valid for the process and controller combination based on Figure 7, as given in Figure 23 or Figure 26. If another controller is used, or if a feedforward is used, the analysis must be redone for the new situation.

5.1 Second-order Low-pass Filter

The steady-state propagation delay $t_{d,filter}$ of a second-order filter for a ramp function Bt can be calculated by studying the steady-state error of the output signal of the filter when a ramp is applied to the filter input. For a general second-order filter of the form

$$H(s) = \frac{a}{s^2 + bs + a}$$

(24)

we can derive for the steady-state error when a ramp-shaped input is applied:

$$e(\infty) = \lim_{s \to 0} s \frac{B}{s^2} \left(1 - H(s)\right) = \frac{Bb}{a} = Bt_{d,filter}$$

(25)

So, the expression for the steady-state propagation delay time for a ramp input yields:

$$t_{d,filter} = \frac{b}{a}$$

(26)

5.2 Control Loop with N Second-order Low-pass Filters and a Delay

In the figure below, the analog GACL containing N second-order low-pass filters and a variable delay factor e^{-sT} is shown:
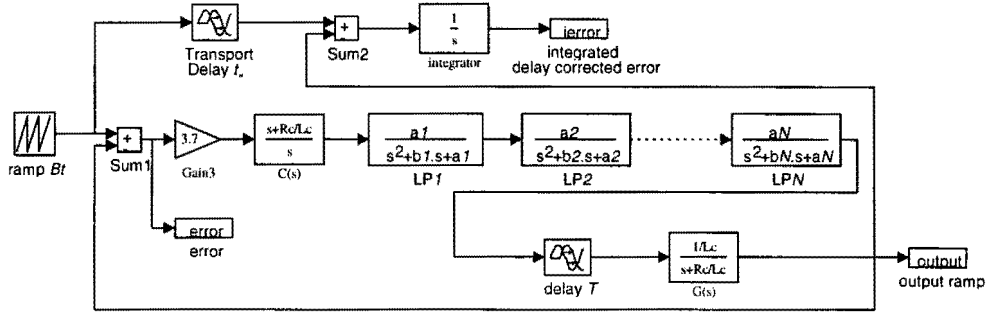
Figure 23: Analog GACL with N second-order low-pass filter sections and a variable delay factor

$H_o(s)$ having N second-order low-pass filters and a variable delay factor is given as:

$$H_o(s) = \frac{e^{-sT}}{t_d s} \prod_{i=1}^{N} \frac{a_i}{s^2 + b_i s + a_i}$$

(27)

The constant t_d equals $L_c/3.7$, where 3.7 is the controller proportional gain factor K_p. The steady-state delay t_d is the same as calculated in (14). This can be proven with the following derivation. The closed-loop function of (27) is found by evaluating (12):

$$H_{cl}(s) = \frac{e^{-sT} \prod_{i=1}^{N} a_i}{t_d s \prod_{i=1}^{N} (s^2 + b_i s + a_i) + e^{-sT} \prod_{i=1}^{N} a_i}$$

(28)

For an $I_{ref}(t)=Bt$, we can find the final value of $e(t)$ by working out the left part of (29). The exponentials in (28) are replaced by their Taylor approximations, after that, (29) is written as just one fraction, and only the relevant power-of-s terms in the numerator are taken into account:

$$e(\infty) = \lim_{t \to \infty} e(t) = \lim_{s \to 0} s \frac{B}{s^2} \left(1 - H_{cl}(s)\right) = Bt_d \quad ,$$

(29)

This steady-state error is proportional to $t_d=50[\mu s]$ and B, proving that t_d is still the steady-state closed-loop delay time for a ramp.

Also an expression can be found for the final value of $E_c(t)$. The final value theorem applied to $E_c(t)$ means that the Laplace transform of the output, $I_{ref}(s)H_{cl}(s)$, must be subtracted from

the input delayed over t_d (the exponential term in (30)), and the result has to be integrated (multiplication by 1/s):

$$E_c(\infty) = \lim_{t \to \infty} E_c(t) = \lim_{s \to 0} s \frac{1}{s} \cdot \frac{B}{s^2} \left(e^{-t_d s} - H_{cl}(s) \right)$$

(30)

Substituting (28) into (30) gives the following result after writing the exponential powers as Taylor series and only taking into account the relevant power of s terms:

$$E_c(\infty) = \lim_{s \to 0} \frac{B}{s^2} \left\{ t_d s^2 \left(T - \frac{t_d}{2} \right) + t_d s^2 \frac{\sum\limits_{j=1}^{N} b_j \prod\limits_{\substack{i=1 \\ i \neq j}}^{N} a_i}{\prod\limits_{i=1}^{N} a_i} \right\}$$

(31)

This expression can be simplified to:

$$E_c(\infty) = B t_d \left(T - \frac{t_d}{2} + \sum_{i=1}^{N} \frac{b_i}{a_i} \right)$$

(32)

We can see that $E_c(\infty)$ has a minimum, which can be found by equating the part in brackets to zero. The minimum value can be found then by inserting a delay equal to

$$T_{opt} = \frac{t_d}{2} - \sum_{i=1}^{N} \frac{b_i}{a_i}$$

(33)

into $H_o(s)$. Of course, this is only possible if

$$\frac{t_d}{2} > \sum_{i=1}^{N} \frac{b_i}{a_i} \quad ,$$

(34)

and enough phase margin is present.

Another conclusion is, that the influence of the second-order low-pass sections on the value of $E_c(\infty)$, is completely determined by their steady-state delay times for a ramp. What can also be concluded from (32), is, that replacing the second-order low-pass filters by a factor e^{-sT} having the same delay time as the filters that it replaces, doesn't change the final value $E_c(\infty)$. This will be shown in the following simulation.

5.2.1 Simulation: Substitution of LP1 and LP2 by an equivalent Delay

In the analog GACL, replacing the two second-order low-pass filter sections by a delay factor T_{eq} having the same steady-state delay time for a ramp as the filters, doesn't influence $E_c(\infty)$, according to (32):

$$E_c(\infty) = Bt_d\left(T_{eq} - \frac{t_d}{2}\right)$$

(35)

The delay introduced by these filters can be calculated using (26), and is found to be 11.8[µs]. The simulation model used for the plot of $E_c(t)$ in Figure 25 is given in Figure 24:
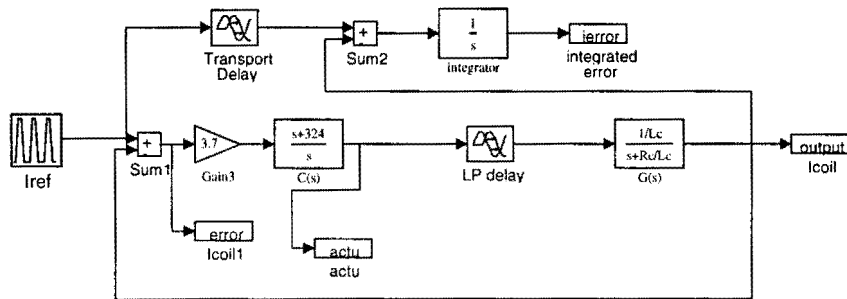
Figure 24: Simulation model used to study the effect of a general delay element

A trapezium as in Figure 2 is used for $I_{ref}(t)$. In Figure 25, also $E_c(t)$ is shown (the same as in Figure 8(c)) for the case that the low-pass filters are replaced by their equivalent delay. Comparing (a) and (b) in Figure 25 shows that replacing the low-pass filters by an equivalent delay factor, results in almost the same $E_c(t)$, approximating the same $E_c(\infty)=-396$[µAs] during the rising ramp of $I_{ref}(t)$. The only difference is a small transient signal due to the low-pass filters.
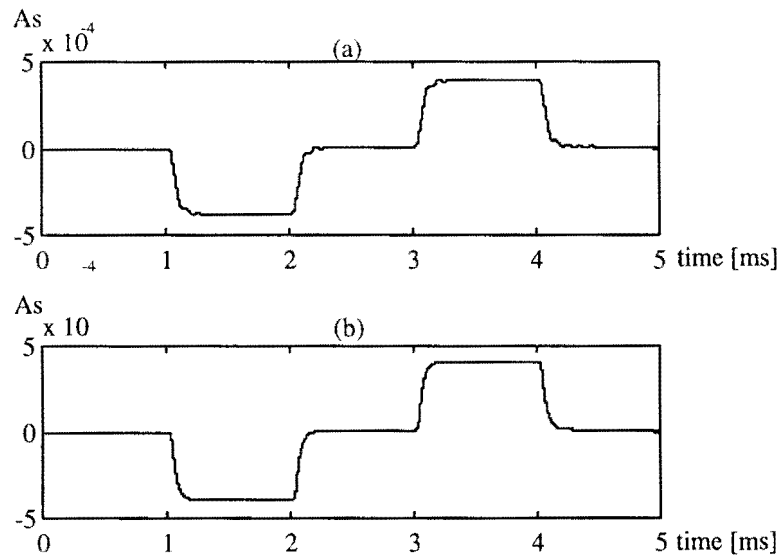
Figure 25: Delay-corrected error integral (a): LP1 and LP2 present in control loop, (b): LP1 and LP2 replaced by their equivalent delay of 11.8[µs]

5.3 Control Loop with N Second-order Low-pass Filters, a Delay, and a ZOH

At the output of the digital controller, a ZOH circuit has to be used to make the discrete time signal continuous. The PWM using samples to calculate the PWM switching times t_i (see paragraph 6.1) can be approximated by a ZOH circuit. If the sampling frequency $T_{s,PWM}$ is high enough in comparison with the system bandwidth, the digital $C(z)$ can be replaced by the analog $C(s)$, adding a ZOH at the controller output with the transfer function:

$$ZOH(s) = \frac{1 - e^{-sT_s}}{T_s s} \Big|_{s=j\omega} = e^{-j\frac{\omega T_s}{2}} \, \text{sin} \, c\!\left(\frac{\omega}{\omega_s}\right)$$

(36)

The next figure shows the generalized control loop extended with the ZOH:

Figure 26: The generalized control loop extended with a ZOH at the output of C(s)

The delay between the input and the output of a ZOH for the case that a ramp input is applied to the ZOH, is simply half the ZOH sampling period T_s, as shown in the figure below:

Figure 27: The delay for a ramp function introduced by the ZOH

Applying the final value theorem as in (29) and (30), tells us that the steady-state closed-loop propagation delay for a ramp input is still t_d (also shown in Figure 26), and that the final value of $E_c(t)$ yields:

$$E_c(\infty) = Bt_d\!\left(T + \frac{T_s}{2} - \frac{t_d}{2} + \sum_{i=1}^{N} \frac{b_i}{a_i}\right)$$

(37)

5.3.1 Calculation of $E_c(\infty)$ for Digitalized GACL

In Figure 17, $E_c(t)$ reaches a value of 650[μAs] during the rising ramp of $I_{ref}(t)$ between 1[ms] and 2[ms]. In Figure 16, $B(s)$, $ZOH(s)$, $LP1(s)$ and $LP2(s)$ are the delaying transfer functions. The steady-state delay time of $B(s)$ found by (26) equals 14.6[μs], for the ZOH we have $T_s=40$[μs], and for $LP1(s)$ and $LP2(s)$ we still have 11.8[μs]. Filling in these values in (37), we find $E_c(\infty)=642$[μAs], rather close to the value found in the simulation.

5.4 Conclusions

In this chapter, the expression in (37) for $E_c(\infty)$ is derived for the general structure in Figure 26. This formula shows that $E_c(\infty)$ can only be zero if the combination of t_d, T_s, T, and the sum of the delays of the low-pass sections is chosen such that (37) yields zero. This is a very stringent requirement.

A better method to make $E_c(\infty)$ equal to zero is the use of feedforward, to be dealt with in chapter 7.

6. PWM using One, Two, or Four Samples per Cycle

In this chapter, algorithms will be derived for calculating the PWM switching times from the samples of u^+. The calculation of the switching times can be done using one sample at the beginning of each PWM cycle, but it seems also to be possible to calculate the switching times using two or four samples per cycle. Using a higher sampling rate will result in better transients behavior, because of the reduced ZOH delay times.

If the sampling frequency is increased, also the bandwidth of the Bessel filter $B(s)$ (ω_f in (18)) can be increased, resulting in a simpler filter and in a smaller filter delay time, which results in an extra increase of phase margin, adding to the increased phase margin resulting from the smaller ZOH time for the PWM resulting from the higher update frequency.

6.1 One Sample per Cycle

In this paragraph, we will consider a PWM that samples u^+ at times kT_z where $k=0,1,2,...$, and T_z is the period time of one PWM cycle. , so $T_{s,PWM}=T_z$. Then, the switching moments for the power transistors can be calculated for the kth cycle, and scheduled forward in time.

First, we will calculate the ideal switching moments for the positive and the negative power half-bridges. These switching moments are called ideal, because they can realize continuous PW's.

We can find for the switching moments (see Figure 28):

$$t^+_{off} = F_{TA}(A + u^+) \qquad\qquad t^+_{on} = F_{TA}(3A - u^+)$$

$$t^-_{off} = F_{TA}(A - u^+) \qquad\qquad t^-_{on} = F_{TA}(3A + u^+)$$

$$(38)$$

In these formulas, A is the amplitude of the triangular PWM wave, $u^+=-u^-$ is the input signal for the PWM module, and the factor F_{AT} is defined as:

$$F_{AT} = \frac{T_z}{4A}$$

$$(39)$$

For the total PW of the full-bridge, we find:

$$PW = t^+_{off} - t^-_{off} + t^-_{on} - t^+_{on} = \frac{T_z u^+}{A}$$

$$(40)$$

The figure below explains these formulas:
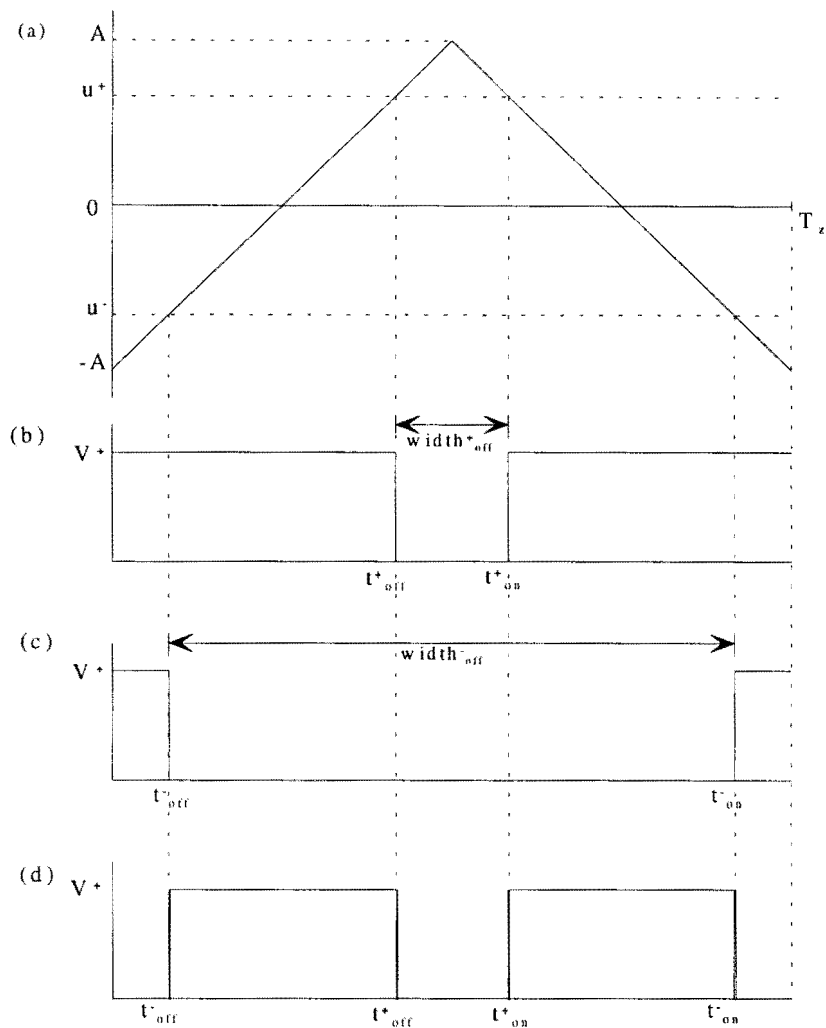
Figure 28: PWM with sampling and continuous PW's (a): switching times following from triangular wave form and control signal u$^+$ (b): positive half-bridge pulse form (c): negative half-bridge pulse form (d): full-bridge pulse form

6.1.1 Simulation: The Analog GACL with $T_{s,PWM}=T_z$

Having found now the moments that the pulses for the positive and the negative power transistor half-bridges must be low, we can program a PSI model for the PWM. At each sample time kT_z, the switching moments are calculated, and these are accurately scheduled forward in time relatively to the sampling moment using a special PSI function to schedule a discrete event forward in time.

In Simulink, the PWM could be implemented as shown in Figure 29. The calculation and scheduling forward-in-time of the switching times is now replaced by detecting the intersections of the output of the PWM-input ZOH with the triangular wave. Of course, the ZOH periods and the periods of the triangular wave must be equal and in phase. However, programming this model in Simulink is not a good idea, because Simulink can't detect the intersection points of the ZOH output with the triangular wave accurately (see [6]). For this reason, the simulations with the detailed PWM model will be done in PSI.
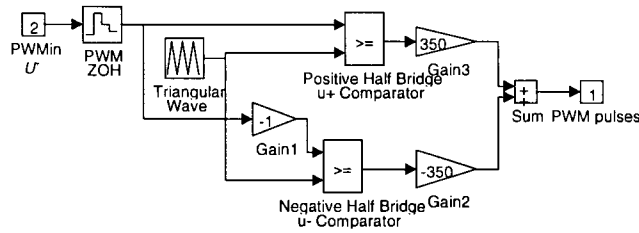
Figure 29: Implementation of the PWM in Simulink

In Figure 30, the model used for the simulations with the control loop containing the PWM with sampling is given. The model is in fact the loop of Figure 7, but the PWM is implemented now in detail, as given in Figure 3. For simulating the PWM with sampling, the input of the PWM must be preceded by a ZOH, as shown in Figure 30:
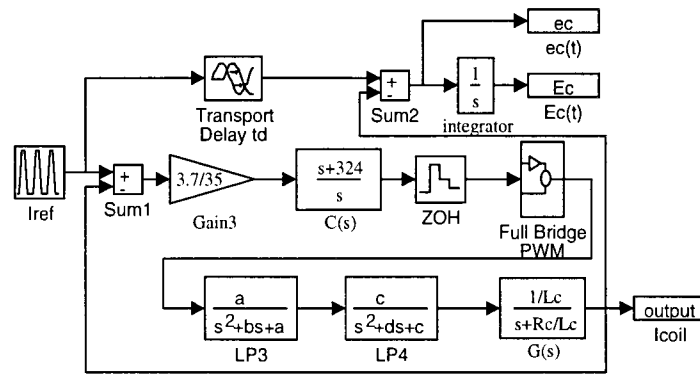
Figure 30: Simulation setup for experiments for PWM with sampling

In Figure 31 (next page), the simulation results for PWM with sampling and continuous PW's are plotted. It shows that $E_c(t)$ becomes positive during the rising ramp of the trapezium, is close to zero during the high level of 600A, and becomes negative during the falling ramp. When no PWM was used, as is the case in Figure 25, $E_c(t)$ showed an opposite behavior. Theoretically, using (37), we would expect a final value of 204[μAs] for the rising ramp with the slope of the first trapezium ramp, using the PWM period, i.e. T_s=40[μs] for the ZOH time, and the delay time of 11.8[μs] for the low-pass filter sections. For the simulation of Figure 31, the final value of $E_c(t)$ is not reached, because the ramp is changed already after 1[ms], when $E_c(t)$ has reached the value of 250[μAs].
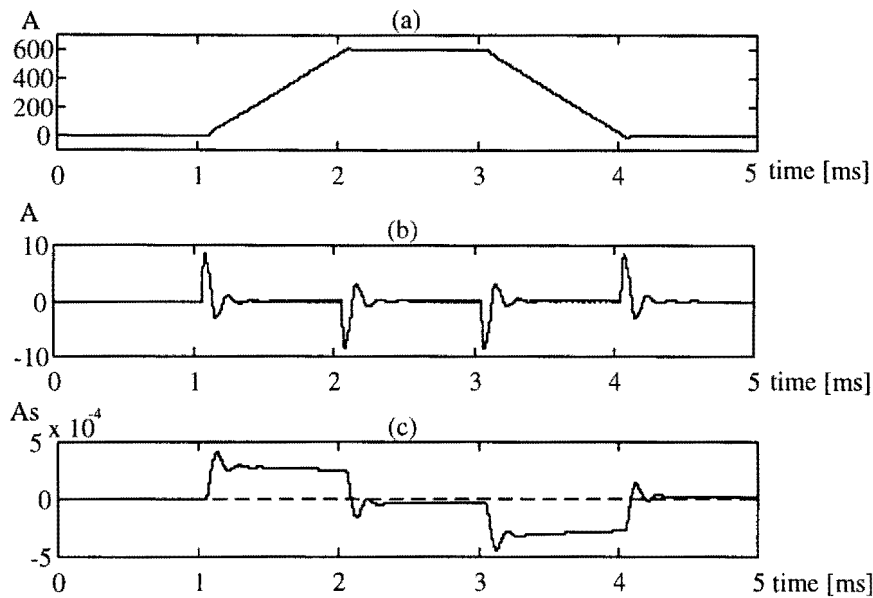
Figure 31: PWM with sampling, the PW is calculated at the sampling moments (a): $I_{coil}(t)$;
(b): $e_c(t)$; (c): $E_c(t)$, with high level of about 250[μAs], and a maximum peek at
405[μAs]

6.2 Two Samples per Cycle

In paragraph 6.1, the PWM algorithm was derived where a sample of u^+ was taken at the beginning of the PWM cycle. Both the on- and off-times for both the half-bridges were calculated from this sample.

Generally, the PWM forms two distinct voltage pulses for each half of its cycle, as can be seen in e.g. Figure 28. If there is enough time to perform the digital calculations, it is possible to calculate the PWM switching times for each half period pulse from different samples for each half period of the PWM. During each PWM cycle, two samples are taken: one at the beginning of the cycle, and one at half the cycle time. In this case, $T_{s,PWM}=T_s/2$.

The principle of calculating the PW for each half PWM period is shown in the figure below:
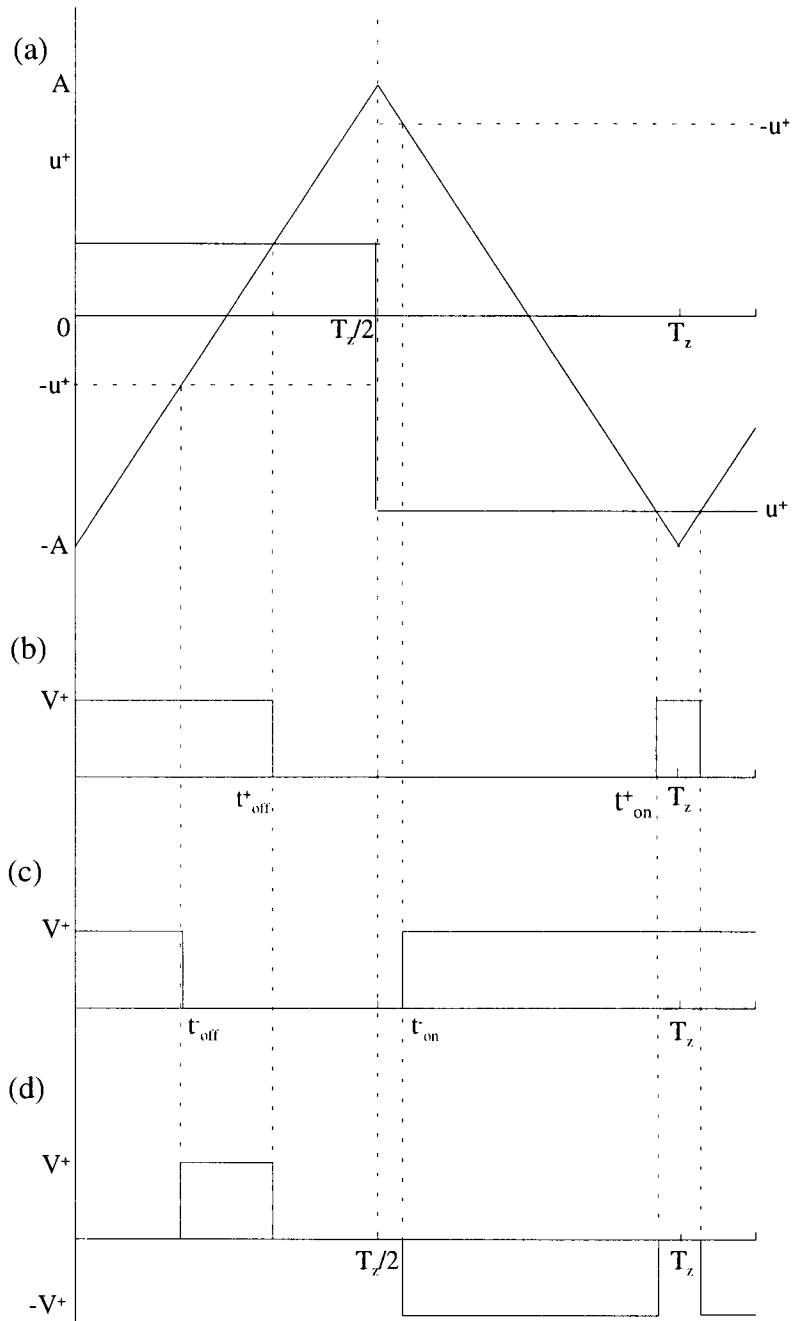
Figure 32: PWM with $T_{s,PWM}=T_z/2$ (a): switching times following from triangular wave form and control signal u^+ (b): positive half-bridge pulse form (c): negative half-bridge pulse form (d): full-bridge pulse form

For continuous PW's, the intersections of the control signal u^+ with the triangular wave determine the switching times.

The switching times can then be calculated as follows:

$$t_{off}^+ = F_{AT}\left(A + u^+(0)\right)$$

<div style="text-align:right">(41)</div>

$$t_{off}^- = F_{AT}\left(A - u^+(0)\right)$$

<div align="right">(41a)</div>

$$t_{on}^+ = F_{AT}\left(A - u^+\left(\frac{T_z}{2}\right)\right)$$

<div align="right">(41b)</div>

$$t_{on}^- = F_{AT}\left(A + u^+\left(\frac{T_z}{2}\right)\right)$$

<div align="right">(41c)</div>

The factor F_{AT} is defined as in (39).

The PW for the first half-cycle yields:

$$PW_1 = t_{off}^+ - t_{off}^- = \frac{T_z u^+(0)}{2A}$$

<div align="right">(42)</div>

For the second half-cycle, it yields:

$$PW_2 = t_{on}^+ - t_{on}^- = \frac{T_z u^+(T_z/2)}{2A}$$

<div align="right">(43)</div>

So, the general expression for the PW for one half-cycle is given by:

$$PW = \frac{T_z u^+}{2A} \quad ,$$

<div align="right">(44)</div>

where u^+ is the control signal at the sample time.

6.2.1 Simulation: The Analog GACL with $T_{s,PWM}=T_z/2$

The PWM algorithm with $T_{s,PWM}=T_z/2$ has been implemented in PSI. In the following plot, the results are shown when continuous PW's are used for both half-bridges. The same simulation using $T_{s,PWM}=T_z$ is also plotted for comparising the results.
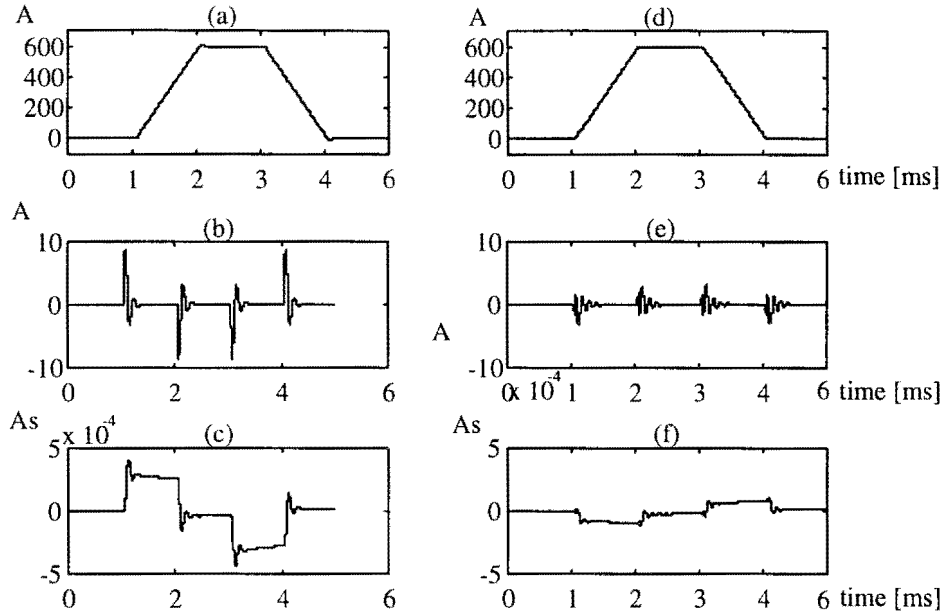
Figure 33: Continuous PW's; (a),(b),(c): $T_{s,PWM}=T_z$; (d),(e),(f): $T_{s,PWM}=T_z/2$ (a) and (d): $I_{coil}(t)$; (b) and (e): $e_c(t)$; (c) and (f): $E_c(t)$

In Figure 33(f), $E_c(t)$ reaches a lowest value of -98.8[μAs] during the rising ramp of the trapezium. According to (37) this value should be -96[μAs] in steady-state, so this is in good accordance with the simulation. Compared to the result for single sampling resulting in a highest value of $E_c(t)=405$[μAs], this is considerably better. Also the harmonics in $e_c(t)$ have diminished, because of the reduced open-loop delay time, and the resulting better phase margin.

6.3 Four Samples per Cycle

Observing the Full-bridge PWM scheme more scrutinizingly, it should also be possible to use a different sample of u^+ for each switching time, if the samples are taken at each $T_z/4$, thus $T_{s,PWM}=T_z/4$. Using $T_{s,PWM}=T_z/4$ reduces the open-loop delay introduced by the PWM, but faster digital equipment may be necessary. The next figure illustrates the idea of using $T_{s,PWM}=T_z/4$:

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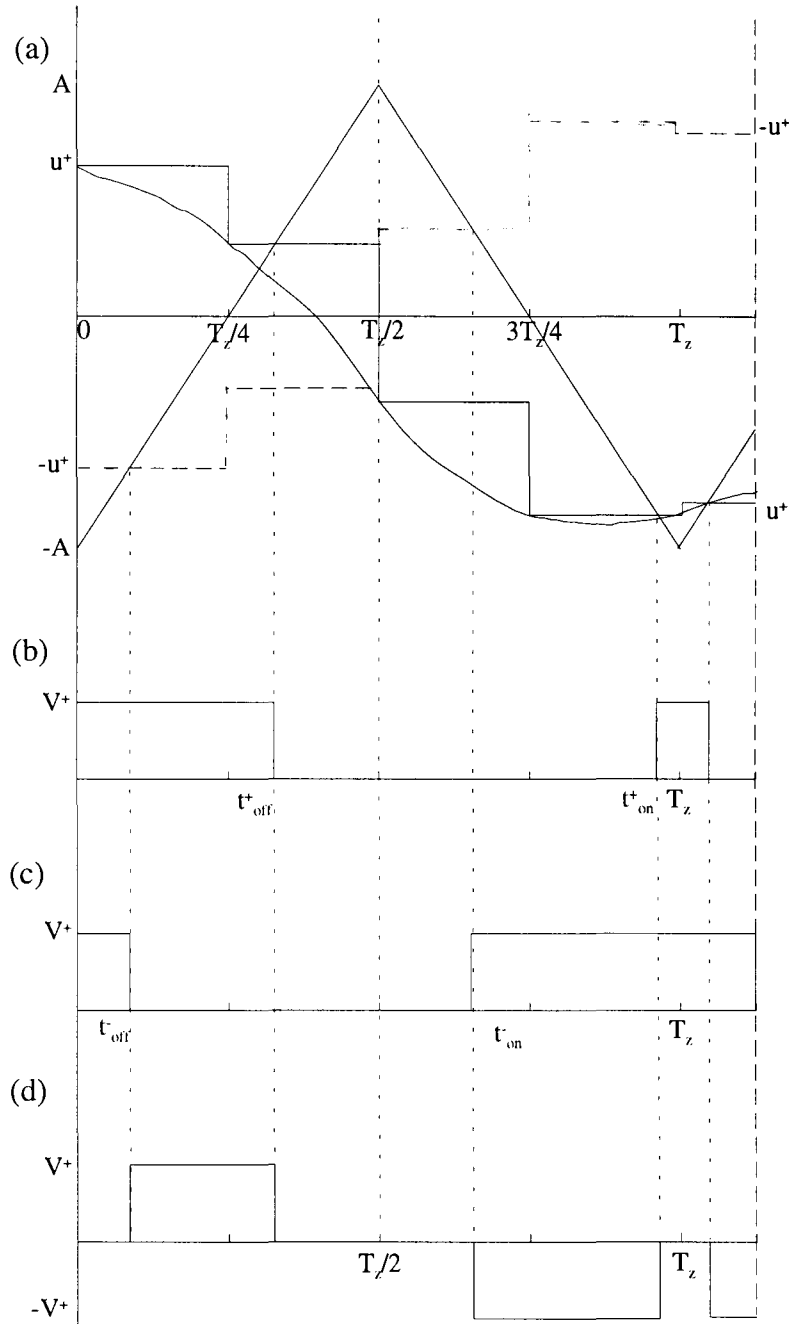
Figure 34: PWM using four input samples per cycle (a): analog switching times following from the triangular wave form and u^+ (b): positive half-bridge pulse shape (c): negative half-bridge pulse shape (d): full-bridge pulse shape

Depending on the sign of $u^+(t)$, we have to make a decision of what switching time must be calculated using Table 3. Special attention must be paid to the implementation in PSI of the algorithm in the case that u^+ is zero. The switching times can then best be calculated using the first and the third samples, those at $t=0$ and $t=\Delta T_z/2$, because a signal cannot be scheduled zero seconds forward in time.

Table 3: Depending on the sign of the sample u^+ taken on sample time t_s, one switching time is calculated

	$t_s=0$ $sign(u^+)=0$	$t_s=\Delta T/4$	$t_s=\Delta T/2$ $sign(u^+)=0$	$t_s=3\Delta T/4$
$sign(u^+)=$ 1	$t_{off}^- = F_{AT}(A - u^+)$	$t_{off}^+ = F_{AT}u^+$	$t_{on}^+ = F_{AT}(A - u^+)$	$t_{on}^- = F_{AT}u^+$
$sign(u^+)=-$ 1	$t_{off}^+ = F_{AT}(A + u^+)$	$t_{off}^- = -F_{AT}u^+$	$t_{on}^- = F_{AT}(A + u^+)$	$t_{on}^+ = -F_{AT}u^+$

The factor F_{AT} is defined again as $F_{AT} = \dfrac{T_z}{4A}$.

Although no complete PW is created in one quarter of the PWM cycle, we wish to find a sensitivity relation between u^+ and the PW similarly to (40) and (44). Using the results in Table 3, a change Δt_i in switching time t_i results in a change Δu^+ in u^+ as:

$$\left|\Delta u^+\right| = \left|\frac{\Delta t_i}{F_{AT}}\right| = \left|\frac{\Delta t_i 4A}{T_z}\right|$$

(45)

7. Improved Performance by Feedforward

Ideally, a feedforward voltage is added directly to L_c in series with R_c. In practice, however the feedforward voltage must be added before the PWM, because this is the amplifier that supplies the coil voltage, using two low-pass filters LP1 and LP2 to filter out the undesired harmonics caused by the PWM. One method to apply the feedforward voltage is feeding an $I_{ref}(t)$ that has been matched for $H_{cl}(s)$ to the reference path of the control loop, and the other method is feeding an appropriate signal to the input of the PWM. The next figure illustrates the two possibilities:
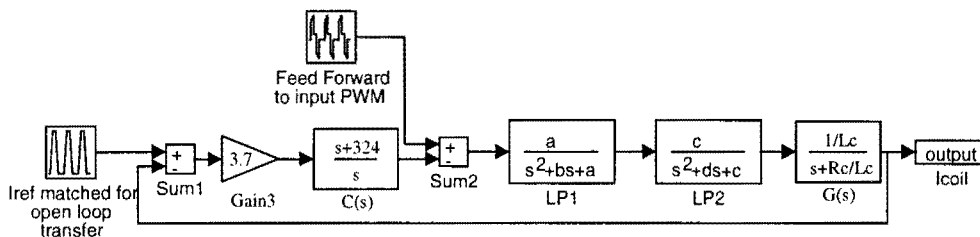
Figure 35: Two principally different ways of applying a feedforward

The most obvious place to apply the feedforward is right at the input of the PWM, because doing so, $C(s)$ isn't charged anymore with the tracking of $I_{ref}(t)$, but it can be designed for other purposes. Independently, the feedforward path can be used for getting a good tracking of $I_{ref}(t)$.

The other way of applying the feedforward, to the input of the control loop, will not be discussed in this chapter, because it is of less practical importance. It will result in a more oscillating $e(t)$, resulting in a larger error range, so that more bits must be chosen for the ADC.

The calculation of the feedforward that must be added to the input of the PWM can be done in two ways. One method is to multiply the complex Fourier coefficients of $I_{ref}(t)$ with the inverse of the transfer function of the filter consisting of the low-pass sections LP1 and LP2 of the PWM and the process. The advantage of taking the Fourier coefficients is that a very sharp cut-off frequency of the feedforward filter is obtained, because we can simply omit the higher harmonics of $I_{ref}(t)$ for calculating the feedforward.

The other method is to design a feedforward filter that matches $I_{ref}(t)$ for the transfer functions $LP1(s)$, $LP2(s)$, and $G(s)$. This way of calculating the feedforward is more flexible than the method using the Fourier components, because for calculating the Fourier components, the form of $I_{ref}(t)$ must be known exactly.

7.1 Feedforward using the Fourier Series Expansion of $I_{ref}(t)$

7.1.1 Fourier Series Expansion of $I_{ref}(t)$

The (periodical) trapezium shaped $I_{ref}(t)$ can be written as a Fourier series:
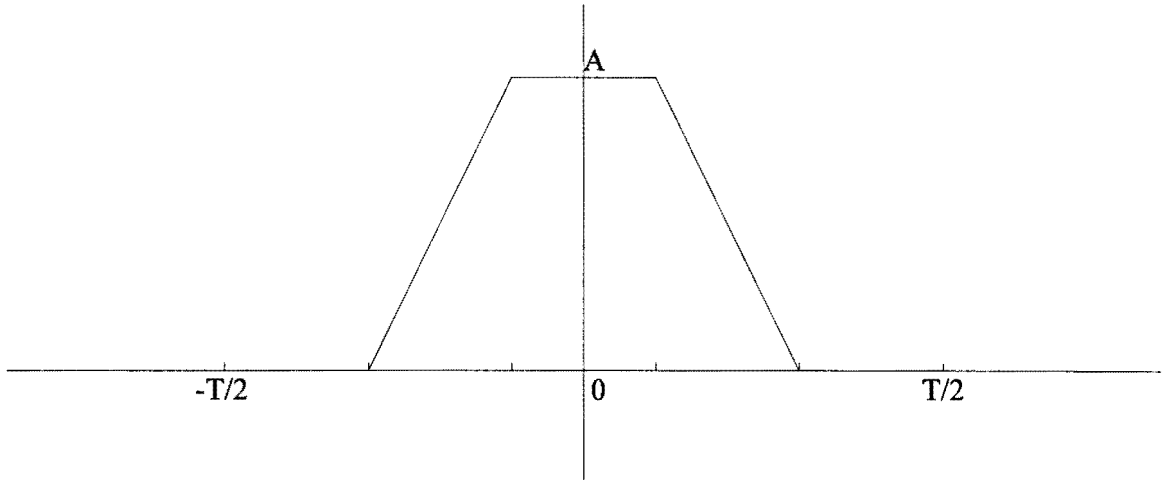
Figure 36: Trapezium shaped $I_{ref}(t)$

Calculation of the Fourier series $I_{ref}(t)$ yields:

$$I_{ref}(t) = \frac{4A}{5} + \sum_{i=1}^{\infty} a_i \cos(i\omega_0 t)$$

(46)

where

$$a_i = \frac{5A}{i^2\pi^2}\left(\cos\left(\frac{i\pi}{5}\right) - \cos\left(\frac{i3\pi}{5}\right)\right)$$

(47)

and $\omega_0 = 200*2*\pi$, because of the 5[ms] period of the trapezia.

7.1.2   Feedforward to the Fourier Components

First it will be shown how the feedforward can be calculated for the combination of $LP1(s)$, $LP2(s)$, and $ZOH(s)$ that is inherent for the sampled PWM.

In Figure 37, the Simulink model setup is shown that is used to apply the feedforward to the input of the PWM. In this model, the PWM is modeled by a ZOH with a ZOH time equal to $T_s = T_{s,PWM}$. Again, we want to calculate the feedforward by an operation on the coefficients and the phases of the Fourier series of $I_{ref}(t)$.
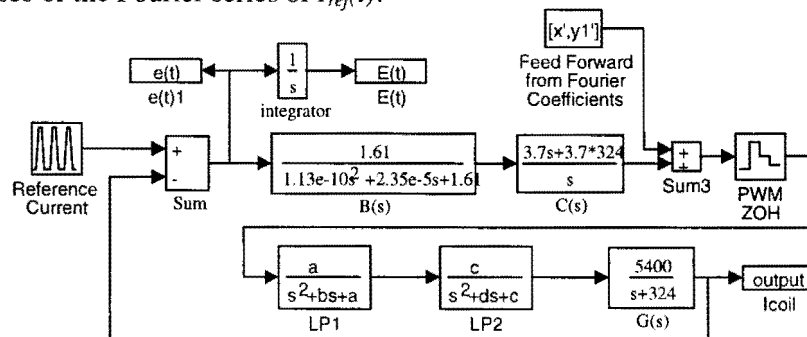
Figure 37: Feedforward fed to the input of the PWM

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The transfer function that must be inverted, is given by the chain $ZOH(s)-LP1(s)-LP2(s)-G(s)$. This transfer function yields:

$$H(s) = \frac{1 - e^{-sT_s}}{T_s s} \left(\frac{a}{s^2 + bs + a} \right) \left(\frac{c}{s^2 + ds + c} \right) \frac{5400}{s + 324}$$

(48)

In (48), T_s equals $T_{s,PWM}$.

This means, that the Fourier series of $I_{ref}(t)$ must be changed using:

$$H^{-1}(s) = \frac{1}{H(s)} = \frac{T_s s}{1 - e^{-T_s s}} \frac{\left(s^2 + bs + a\right)}{a} \frac{\left(s^2 + ds + c\right)}{c} \frac{s + 324}{5400}$$

(49)

We have to multiply the Fourier coefficients given in (47) with the magnitude of (49) for the corresponding frequency, and the phase of the corresponding cosine term in (46) must be shifted with the phase angle of (49) for that frequency.

In Figure 38(a), the feedforward is shown, constructed by performing the feedforward operation on the first 125 complex Fourier coefficients of the trapezium shaped $I_{ref}(t)$, that must be fed to the input of the ZOH in Figure 37. The ZOH delay time used here is $T_s=20[\mu s]$, corresponding to $T_{s,PWM}=T_z$.
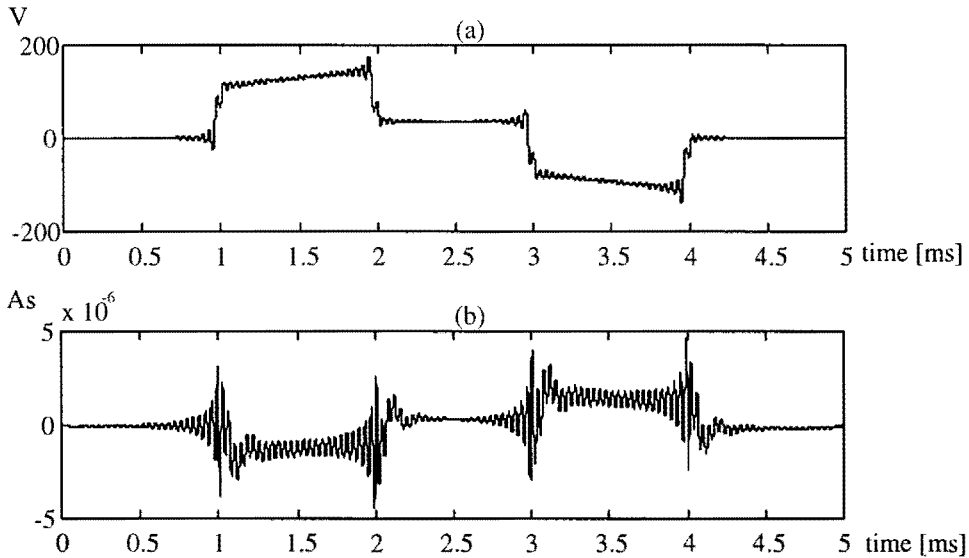
Figure 38: The desired feedforward voltage that must be fed to the input of the ZOH replacing the PWM

Figure 38(b) shows that the maximum absolute value of $E(t)$ now is about $8[\mu As]$, which is even smaller than prescribed by (4).

Note that because of the way that the feedforward was calculated, no delay will be present between $I_{ref}(t)$ and the $I_{coil}(t)$. Therefore, the $e(t)$ can be integrated immediately to $E(t)$.

Another conclusion drawn by studying Figure 37, is that if an ideal feedforward is added at the input of the PWM, it doesn't matter what filters are present in the error path before the

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place where the feedforward is added, as long as $e(t)$ error is zero. This doesn't mean that we don't need a controller, of course, because the controller is still needed to deal with disturbances and model uncertainties.

7.2   Feedforward Filter

In this chapter, the feedforward is not calculated using the Fourier coefficients of the trapezium shaped $I_{ref}(t)$, but a feedforward filter will be designed. Because $I_{ref}(t)$ is always a combination of ramp functions, the first step in calculating the feedforward is described in (50):

$$U_{ref}(t) = R_c I_{ref}(t) + L_c \frac{dI_{ref}(t)}{dt}$$

(50)

For a ramp shaped $I_{ref}(t)$ this voltage is easy to find.

In the next figure, the place of the feedforward filter FFW is shown:
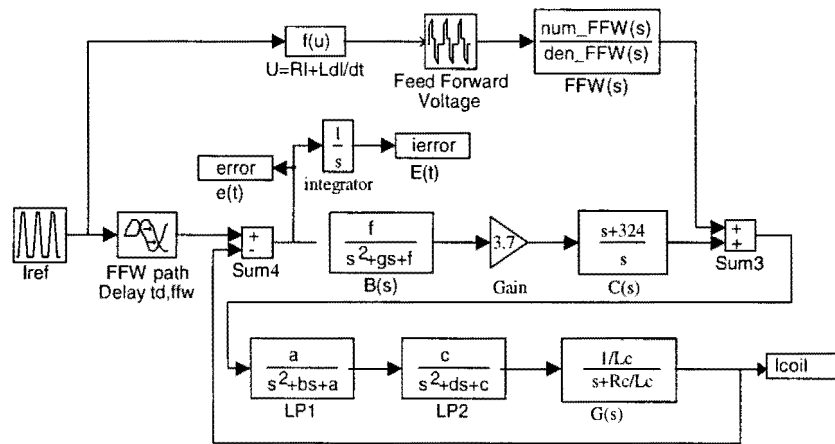
Figure 39: GACL configuration when a feedforward filter is used

Notice that $I_{ref}(t)$ is fed to the GACL delayed over $t_{d,ffw}$. This delay $(t_{d,ffw})$ is needed to compensate for the delay in the feedforward path, as will be explained later on.

For analyzing the GACL configuration with feedforward, the following model structure is used:
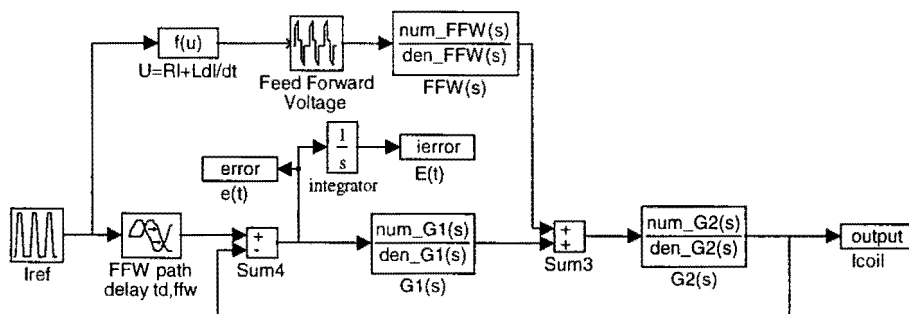
Figure 40: Simplified model of the GACL configuration with feedforward

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In Figure 40, two transfer functions must be taken into account to study $e(t)$ for this configuration, because $e(t)$ is the result of two independent contributions. One part which will be called $e_{ref}(t)$ results from the transfer of $I_{ref}(t)$ to $e(t)$ via the reference path (unconnected feedforward), and the other part, called $e_{ffw}(t)$, results from the transfer of $I_{ref}(t)$ to $e(t)$ via the feedforward path (unconnected reference path). Hence, in the Laplace domain, the total current error can be written as:

$$e(s) = e_{ref}(s) + e_{ffw}(s)$$

$$(51)$$

For calculating both contributions to $e(s)$, the series combination of $G_1(s)$ and $G_2(s)$ will be called $G_t(s) = G_1(s)G_2(s)$. The first transfer function is from $I_{ref}(t)$ via the reference path to $e(s)$, resulting in the contribution $e_{ref}(s)$:

$$e_{ref}(s) = I_{ref}(s)e^{-st_{d,ffw}} \frac{1}{1 + G_t(s)}$$

$$(52)$$

The other transfer function is from $I_{ref}(t)$ via the feedforward path to $e(s)$, and it contributes to:

$$e_{ffw}(s) = I_{ref}(s) \frac{s + R_c / L_c}{1 / L_c} FFW(s) \frac{-G_2(s)}{1 + G_t(s)}$$

$$(53)$$

In (53), the factor $\dfrac{s + R_c / L_c}{1 / L_c}$ represents the actions given by (50).

The delay $t_{d,ffw}$ that is placed in the reference path equals the steady-state delay for a ramp function of the feedforward path, shown in the figure below:
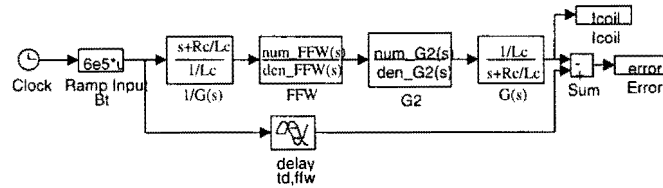
Figure 41: Feedforward path and equivalent steady-state delay time $t_{d,ffw}$ for a ramp input

This delay time can be calculated analytically using (25) if the filters mentioned above connected in series form a combination of second-order filters.

7.2.1 Feedforward following directly from the V/I Relation of G

First, let's take for the transfer of FFW $FFW(s)=1$. In that case, the ideal coil voltage is fed directly to the input of the PWM low-pass filters. The steady-state delay for a ramp-shaped $I_{ref}(t)$ $t_{d,ffw}$ is determined by the filters LP1 and LP2 only (if no PWM-ZOH is present), which yields

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$$t_{d,ffw} = \frac{b}{a} + \frac{d}{c}$$

(54)

which is found using (25).

Applying now the final value theorem to (51), will show that both $e(t)$ and its integral go to zero for $t \to \infty$:

$$e(\infty) = \lim_{t \to \infty} e(t) = \lim_{s \to 0} se(s) = 0$$

(55)

and

$$E(\infty) = \lim_{t \to \infty} E(t) = \lim_{t \to \infty} \int_0^t e(\tau)d\tau = \lim_{s \to 0} sE(s) = \lim_{s \to 0} e(s) = 0$$

(56)

This results show that $t_{d,ffw}$ given in (54) really is the delay time that must be placed in the reference path of the GACL if $FFW(s)=1$ is used.

In Figure 40, the simulation results confirm the theoretical results for the case that $FFW(s)=1$ and no PWM-ZOH is present:
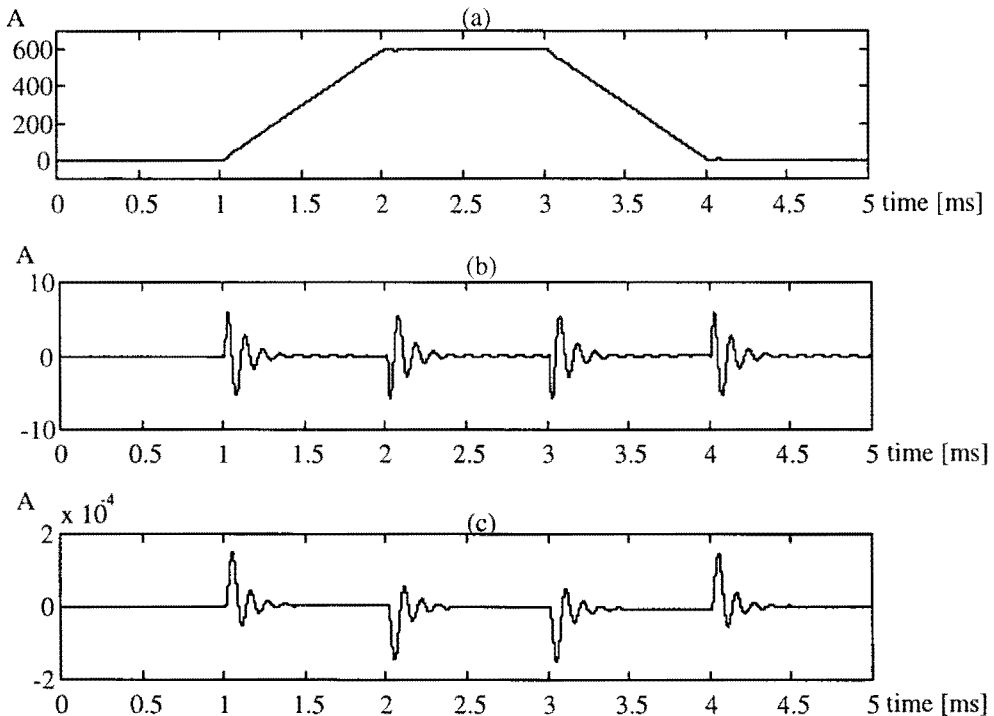
Figure 42: Signals when FFW(s)=1 is used (a): $I_{coil}(t)$ (b): e(t) (c): E(t)

Although for a ramp-shaped $I_{ref}(t)$, $E(t)$ goes to zero for increasing t, Figure 42 shows that there is still a rather large transient signal present. The absolute value of the overshoot peak is about 140[µAs], which is a factor 14 too large. A better feedforward filter is used in the next paragraph.

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7.2.2 Linear Phase Feedforward Path

One way to reduce this large transient peaks, is to make sure that the feedforward path has a linear phase transfer function.

Because the filters LP1 and LP2 are non-linear phase filters, FFW must contain the inverse transfer functions *LP1(s)* and *LP2(s)*, and furthermore two new second-order low-pass sections are added to make the filter physically realizable:

$$FFW(s) = \frac{p_1 p_2}{ac} \cdot \frac{s^2 + bs + a}{s^2 + q_1 s + p_1} \cdot \frac{s^2 + ds + c}{s^2 + q_2 s + p_2}$$

(57)

Applying the final value theorem as in (55) and (56), show again that both $e(\infty)$ and $E(\infty)$ are equal to zero, provided that for $t_{d,ffw}$ is taken:

$$t_{d,ffw} = \frac{q_1}{p_1} + \frac{q_2}{p_1}$$

(58)

For the new second-order low-pass sections Bessel filters are chosen, because of their linear phase characteristics. Their individual -3dB bandwidths are set to 25kHz, which is the Nyquist frequency of the PWM with $T_{s,PWM}=T_z/2$. This means, that the damping is -6dB at the Nyquist frequency. Doing so, the bandwidth of the feedforward path has changed from 21.6kHz, which is the bandwidth of the series of LP1 and LP2, to about 17.5kHz, the bandwidth of the series filter FFW, LP1 and LP2. This doesn't matter, as will be shown by simulation results, because the fundamental frequency of the reference current is 200Hz, so also for $I_{ref}(t)$, the bandwidth of 17.5kHz is high enough to let through the relevant voltage harmonics.

The plot below shows the simulation results for the new developed filter FFW. Again, no ZOH is present in $H_o(s)$. Using the linear phase $FFW(s)$, $|E(t)|$ is has a maximum of 16[μAs] caused by a transient effect.
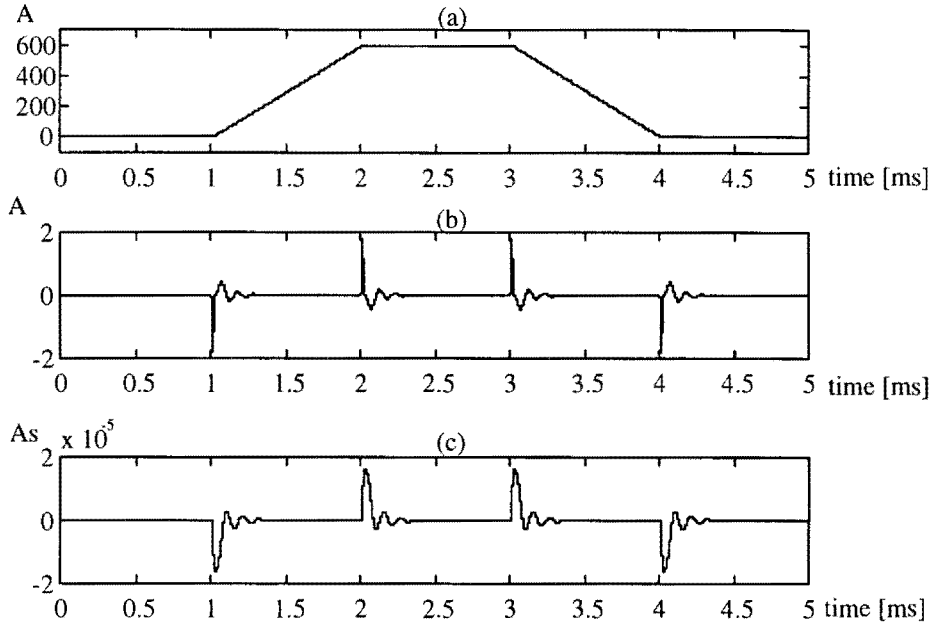
Figure 43: Linear Phase Feedforward (a): $I_{coil}(t)$ (b): $e(t)$ (c): $E(t)$

7.2.3 Feedforward and Extra Open-loop Delays

One reason that feedforward is used, is that the transient signals due to bad tracking of $I_{ref}(t)$ remain small even if there are extra delay factors in the GACL. The extra delays are represented by the delay factors T_1 and T_2 in the figure below:
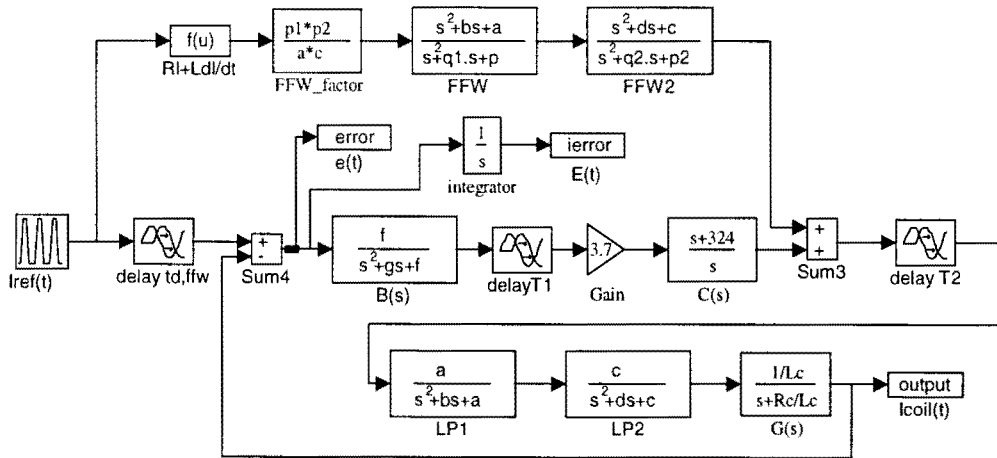
Figure 44: GACL with linear phase feedforward and extra delays T_1 and T_2 in G_1 and G_2

Applying the final value theorem as in (55) and (56), show again that both $e(\infty)$ and $E(\infty)$ are equal to zero, provided that for $t_{d,ffw}$ is taken:

$$t_{d,ffw} = \frac{q_1}{p_1} + \frac{q_2}{p_2} + T_2$$

(59)

As discussed in the chapter 4, the transient behavior of the control loop is influenced by an extra open-loop delay $T=T_1+T_2$. Since the feedforward is not influenced by T_2 (a delay has a linear phase transfer function), we can concentrate all the open-loop delay time in T_2, thus

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$T_1=0$, so $T=T_2$. The simulation results below show, that the transients are really reduced now even if there is some extra delay in the control loop. The input signal chosen to do this simulation is a ramp function with a slope equal to the trapezium ramps: 600[A/ms]. The resulting current transients have to meet the specifications for the settling behavior. The value of T_2 here is $T_2=30[\mu s]$. Even for this rather big delay time, the specifications for $e(t)$ are met, and $E(t)$ satisfies (4) most of the time, as shown in Figure 45:
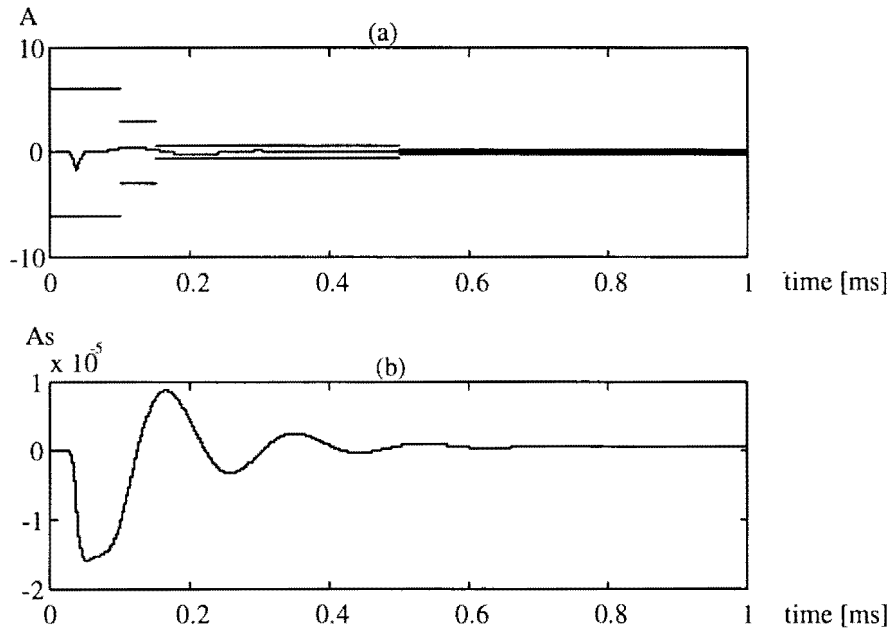
Figure 45: GACL with linear phase feedforward, $T_2=30[\mu s]$ (a): e(t) (b): E(t)

Although the error and its integral are within their specifications in Figure 45, the value of $T_2=30[\mu s]$ may be too large if there are disturbances. For good performance of the control loop, implying a sufficient amount of phase margin, the total delay time T should be minimized.

Looking at the small values of $e(t)$ in Figure 43 and Figure 45, another advantage of using feed-forward is the reduced range of $e(t)$. This means that a D/A converter with less bits can be placed in the error path.

7.3 Conclusions

In this chapter, two ways of calculating a feedforward have been discussed. The first method, using the Fourier series expansion of $I_{ref}(t)$, is of less practical importance than the other method, by which a feedforward filter was designed. A feedforward filter is more flexible, because complete knowledge of $I_{ref}(t)$ is not necessary to calculate the Fourier series expansion, requiring prior knowledge of the reference signal over a whole period.

The best performance of feedforward can be achieved by making sure that the feedforward path has a linear phase characteristic. This results in very good tracking of $I_{ref}(t)$ by the output, because the shape of $I_{ref}(t)$ is not affected much by the transfer function of the feedforward path.

Another advantage of using a feedforward filter that is a combination of second-order low-pass filters is that both $e(\infty)$ and $E(\infty)$ are zero. Using FFW with a linear phase characteristic,

the maximum value of $e(t)$ is about 2[A] for a rise time of 1[ms], as shown in Figure 1. In the analog gradient chain without the feedforward, the maximum $e(t)$ is at least 30[A] for the same risetime. The reduction of a factor 15 in the range of $e(t)$ results in a gain of about 4 bits for the ADC in the error path.

As a last advantage, the tracking of $I_{ref}(t)$ isn't a task of the controller anymore, so that the controller can be redesigned for optimal suppression of disturbances and for changing model parameters.

During the simulations, $I_{ref}(t)$ is delayed in the reference path over $t_{d,ffw}$. This makes $e(t)$ and $E(t)$ to go to zero in steady-state. In practice, however, small variations in $t_{d,ffw}$ will result in a non-zero steady-state value of $e(t)$, and therefore in drifts of $E(t)$. The practical realizability of this kind of feedforward is dependent on the accuracy of $t_{d,ffw}$, thus of how precisely the filter coefficients of LP1 and LP2 are known, assuming that the coefficients of FFW are known exactly. Furthermore, feedforward requires exact knowledge of e.g. R_c as a function of temperature, and of L_c as a function of I_{coil}.

8. Digitalizing the Analog Pulse Widths

8.1 Equivalent DA Converter

Generally, the relation between a certain quantization interval ε, the range of the signal to be converted $range(x(t))$, and the number of converter bits b required is given by:

$$b = \log_2 \left\lceil \frac{range(x(t))}{\varepsilon} \right\rceil$$

(60)

A consequence of using ADC's or DAC's, is the appearance of quantization errors e_q due to the loss of resolution when $x(t)$ is rounded to a b bits representation. The resulting quantization error e_q will be in the range:

$$-\frac{\varepsilon}{2} < e_q < \frac{\varepsilon}{2}$$

(61)

In the case that the PWM switching times t_i are calculated on a computer using the samples of u^+, t_i must be rounded to $t_{d,i}$, which must be a multiple of the clock cycle ΔT of the master clock with clock frequency f_{cl} steering the PWM. For making the calculations simple, one PWM cycle T_z is divided in N equal parts. The relation between ΔT, f_{cl}, T_z, and N then yields:

$$\Delta T = \frac{T_z}{N} = \frac{1}{f_{cl}}$$

(62)

In this case, the PW's of both the positive and the negative half-bridges must be multiples of ΔT.

If any analog switching time t_i is rounded to a corresponding $t_{d,i}$, a quantization error $t_{q,i}$ is made defined as:

$$t_{q,i} = t_i - t_{d,i}$$

(63)

The resulting loss of resolution of the switching times and thus of the PW's, is equivalent to DA converting u^+ and using continuous PW's.

Using (60), the equivalent DAC that corresponds with the N equal parts per half PWM period can be found by dividing the PWM input range of $2A$ through the resolution of Δu^+:

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$$b = \left\lceil \log_2 \frac{2A}{\Delta u^+} \right\rceil$$

$$(64)$$

8.2 Single Sampling per PWM Cycle

In first instance, each individual ideal switching time t_i following from the intersections of the control signal u^+ and its negative version (as derived in Chapter 1) with the triangular wave, is rounded to the nearest multiple of ΔT, called $t_{d,i}$, using the following rules:

To $t_{d,i} = k\Delta T$ (k again is an integer) if

$$k\Delta T \le t_i < (k + \frac{1}{2})\Delta T$$

$$(65a)$$

and to $t_{d,i} = (k + 1)\Delta T$ if

$$(k + \frac{1}{2})\Delta T \le t_i < (k + 1)\Delta T .$$

$$(65b)$$

In Figure 46, it is shown how the rounding is done. After digitalization, the full-bridge PW becomes:

$$PW_d = t^+_{d,off} - t^-_{d,off} + t^-_{d,on} - t^+_{d,on}$$

$$(66)$$

The difference between the ideal switching moment t^+_{off} and the largest multiple of ΔT less than or equal to t_i is called t_v.

As can be derived from Figure 46, the error $e_{q,PW}$ on PW can be expressed in terms of t_v as follows:

$$e_{q,PW} = -4t_v \qquad \text{if} \qquad 0 \le t_v < \frac{\Delta T}{2}$$

$$(67a)$$

and

$$e_{q,PW} = 4(\Delta T - t_v) \qquad \text{if} \qquad \frac{\Delta T}{2} \le t_v < \Delta T$$

$$(67b)$$

From these formulas, it can be seen that there is an unambiguous relation between t_v and $e_{q,PW}$, and $e_{q,PW}$ must be in the range:

$$-2\Delta T < e_{q,PW} < 2\Delta T$$

$$(68)$$
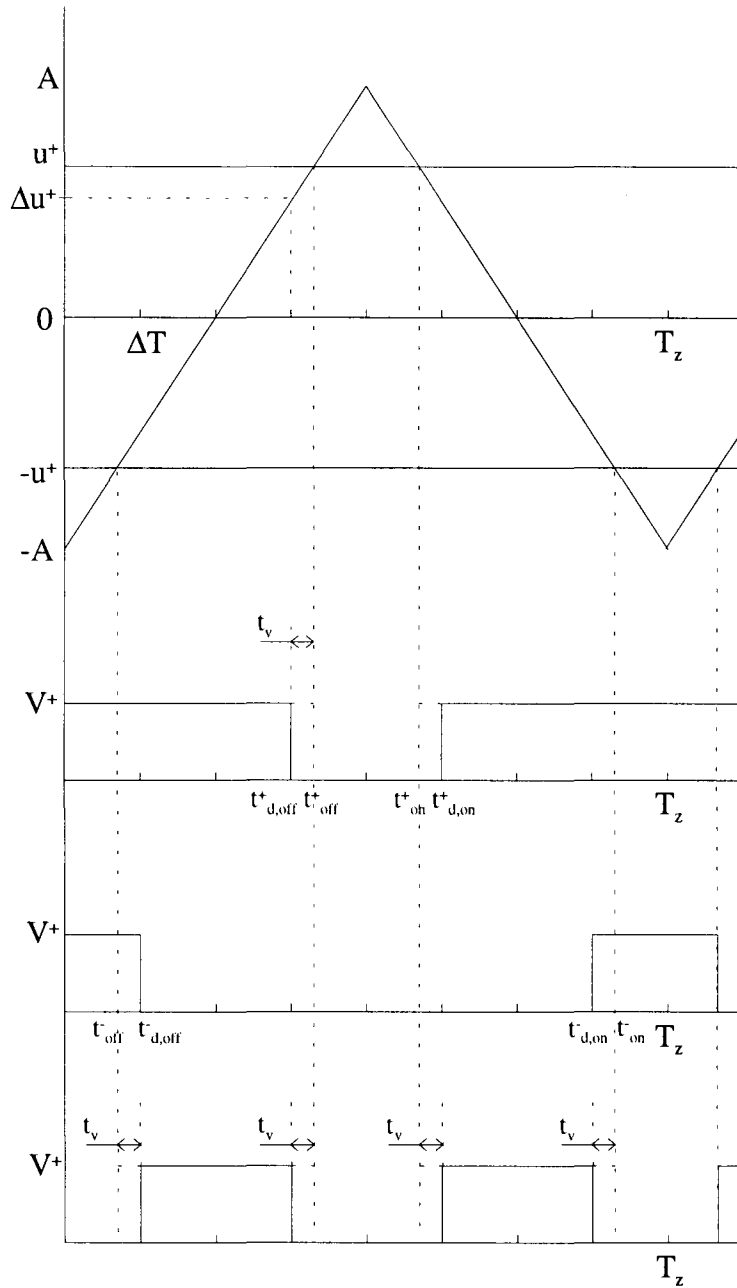
Figure 46: PWM with $T_{s,PWM}=T_z$ and digitalized PW's, same plots as in Figure 28.

Digitalizing the PW's has the same effect as digitalizing u^+. As can be found by transforming the range of (68) by (40), the quantization error $e_{q,u}$ of u^+, will be in the range:

$$-\frac{2A}{N} < e_{q,u} < \frac{2A}{N}$$

(69)

This shows that u^+ can thought to be quantized to an integer number of the amplitude steps:

$$\Delta u^+ = \frac{4A}{N}$$

(70)

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8.3 Rounding Scheme for Minimized PW Error Range

In this paragraph, a new rounding algorithm is derived for PWM $T_{s,PWM}=T_z$. The basic principle behind it is, that the total PW of the full-bridge pulse shape as shown in Figure 46, should not differ more than $\Delta T/2$ from the total analog PW for the full-bridge.

To find the optimal rounding scheme in the sense of a minimized $e_{q,PW}$ per PWM cycle, let's first have a look at the quantization errors $t_{q,i}$ that result from truncating or taking the ceiling of the switching times. Truncating means that the analog switching time t_i is rounded to the largest integer multiple of ΔT equal or less than t_i, and taking the ceiling means that the switching time is rounded to its ceiling multiple of ΔT, i.e. the smallest multiple of ΔT larger than t_i. Table 4 shows the $t_{q,i}$'s due to these actions. In this table, the time difference t_v, defined as the difference between t^+_{off} and the largest multiple of ΔT equal or less than t^+_{off}, is used. The time difference could also be defined for the other t_i's, as indicated in Figure 46.

Table 4: Quantization Errors $t_{q,i}$ caused by Truncation and Ceiling each t_i

	t^+_{off}	t^+_{on}	t^-_{off}	t^-_{on}
$t_{q,i}$ Truncation	$-t_v$	$\Delta T - t_v$	$\Delta T - t_v$	$-t_v$
$t_{q,i}$ Ceiling	$\Delta T - t_v$	$-t_v$	$-t_v$	$\Delta T - t_v$

The total PW error $e_{q,PW}$ follows by adding the distinct $t_{q,i}$'s. Table 4 shows, that a general expression of $e_{q,PW}$ is given by

$$e_{q,PW} = p\Delta T - 4t_v$$

(71)

where $p \in \{0,1,2,3,4\}$.

The strategy to come to an optimal switching time rounding scheme is now as follows. For each value of t_v, the error given in (71) must be within the range (compare to (61)):

$$-\frac{1}{2}\Delta T \le e_{q,PW} < \frac{1}{2}\Delta T$$

(72)

This implies, that we have to choose the parameter p in (71) properly for distinct intervals of t_v. This is easy, considering that for each interval, there will be a contribution of $-4t_v$ for $e_{q,PW}$. The next table shows the values of p for the distinct intervals of t_v.

Table 5: Choosing p for distinct intervals of t_v

Interval of t_v	p
$0 < t_v \le \dfrac{1}{8}\Delta T$	0
$\dfrac{1}{8}\Delta T < t_v \le \dfrac{3}{8}\Delta T$	1
$\dfrac{3}{8}\Delta T < t_v \le \dfrac{5}{8}\Delta T$	2
$\dfrac{5}{8}\Delta T < t_v \le \dfrac{7}{8}\Delta T$	3
$\dfrac{7}{8}\Delta T < t_v < \Delta T$	4

Now that we know what value of p must be chosen within the distinct intervals of t_v, we have to take a look at which combinations of truncating and taking the ceiling of the t_i's yield the desired value of p. This can be done easily by studying Table 4. In the next table, the possible combinations are shown.

Table 6: Rounding Combinations for a minimized range of $e_{q,PW}$ per PWM cycle for distinct values of p. The chosen combinations are shaded.

t_i	T/C	$t_{q,i}$	p=0	p=1			p=2						p=3			p=4
t^+_{off}	T	$-t_v$	X	X	X	X				X	X	X	X			
	C	$\Delta T - t_v$		X			X	X	X					X	X	X	X
t^+_{on}	T	$\Delta T - t_v$			X		X			X	X		X		X	X	X
	C	$-t_v$	X	X		X	X		X	X			X		X		
t^-_{off}	T	$\Delta T - t_v$			X			X		X		X	X	X		X	X
	C	$-t_v$	X	X	X		X	X		X		X			X		
t^-_{on}	T	$-t_v$	X	X	X	X		X	X		X					X	
	C	$\Delta T - t_v$				X			X		X	X	X	X	X		X

Studying Table 5 and Table 6, we see that it should be possible now to have a zero $e_{q,PW}$ for the values $t_v = 0$, $t_v = 1/4\Delta T$, $t_v = 1/2\Delta T$, and $t_v = 3/4\Delta T$. Filling in the new range of $e_{q,PW}$ which is ΔT now, according to (72), into (40), shows that the resolution of u^+ has also improved by a factor 4:

$$\Delta u^+ = \frac{A}{N}$$

(73)

This means, using (64), a 2-bit gain in resolution of u^+.

8.4 Double Sampling per Cycle

Now, the same analysis as in 8.3 will be performed for the digitalization of the t_i's when double sampling per PWM cycle is used. The digitalization variable t_v must now be determined for each half PWM cycle. For the first half period, it is defined as:

$$t_v = t_{off}^+ - \Delta T_z INT\left(\frac{t_{off}^+}{\Delta T_z}\right),$$

<div align="right">(74)</div>

where the $INT(x)$ function means that the integer value of x is taken, and for the second half period it is defined as:

$$t_v = \Delta T_z INT\left(\frac{t_{on}^+}{\Delta T_z} + 1\right) - t_{on}^+$$

<div align="right">(75)</div>

$$\text{with } k < \frac{t_{on}^+}{\Delta T_z} < k + 1$$

and $t_v=0$ if $\dfrac{t_{on}^+}{\Delta T_z} = k$, where k is an integer.

The errors $t_{q,i}$ caused by truncating and taking the ceiling for each t_i as a function of t_v are the same as in Table 4 for the case of double sampling per PWM cycle, because the definition of t_v is still the same.

First, let's study what is the range of $e_{q,PW}$ per half PWM cycle if "normal" rounding of the individual t_i's is used. The following table shows how is rounded in only two distinct intervals of t_v, and the resulting value of $e_{q,PW}$:

Table 7: $e_{q,PW}$ per half PWM cycle when normal rounding is used

Interval t_v	t_{off}^+	t_{off}^-	$e_{q,PW}$
$0 < t_v < \frac{1}{2}\Delta T$	T	C	$-2t_v$
$\frac{1}{2}\Delta T \le t_v < \Delta T$	C	T	$2\Delta T - 2t_v$
	t_{on}^+	t_{on}^-	
$0 < t_v < \frac{1}{2}\Delta T$	C	T	$-2t_v$
$\frac{1}{2}\Delta T \le t_v < \Delta T$	T	C	$2\Delta T - 2t_v$

Table 7 shows, that for each half PWM period, $e_{q,PW}$ is lying within the following range:

$$-\Delta T < e_{q,PW} \le \Delta T$$

<div align="right">(76)</div>

The corresponding quantization step $\Delta u^+=4A/N$ is the same as in (70).

Now, the same analysis has to be done as in chapter 8.3, to find the optimal rounding scheme minimizing the range of $e_{q,PW}$ per half PWM cycle.

Optimizing the rounding scheme, we have to look at $e_{q,PW}$ per half PWM cycle. This $e_{q,PW}$ per half PWM cycle is found by adding the individual $t_{q,i}$'s. Table 4 shows, that a general expression for it is given by:

$$e_{q,PW} = p\Delta T - 2t_v$$

$$(77)$$

where $p \in \{0,1,2\}$.

The strategy to come to an optimal rounding scheme to find the $t_{d,i}$'s is now as follows. For each value of t_v, $e_{q,PW}$ as given in (77) must be within the range:

$$-\frac{1}{2}\Delta T \le e_{q,PW} < \frac{1}{2}\Delta T$$

$$(78)$$

This implies, that we have to choose the parameter p in (78) properly for distinct intervals of t_v. This is easy, considering that for each interval, there will be a contribution of $-2t_v$ for $e_{q,PW}$. The next table shows the values of p for the distinct intervals of t_v:

Table 8: Choosing p for distinct intervals of t_v

Interval of t_v	p
$0 < t_v \le \frac{1}{4}\Delta T$	0
$\frac{1}{4}\Delta T < t_v \le \frac{3}{4}\Delta T$	1
$\frac{3}{4}\Delta T < t_v < \Delta T$	2

Now that we know what value of p must be used within the distinct intervals of t_v, we have to examine which combinations of truncating and taking the ceiling of the t_i's in each half period yield the desired value of p. This is be done by studying Table 4. In the next table, the possible combinations are shown.

Table 9: Optimal Rounding Combinations for distinct values of p (distinct p's per half period); The chosen combinations are shaded

Switching Time	T/C	$t_{q,i}$	p = 0	p = 1	p = 2
t^+_{off}	T	$-t_v$	X		X
	C	$\Delta T - t_v$		X	X
t^-_{off}	T	$\Delta T - t_v$		X	X
	C	$-t_v$	X	X	
t^+_{on}	T	$\Delta T - t_v$			X	X
	C	$-t_v$	X	X	
t^-_{on}	T	$-t_v$	X		X
	C	$\Delta T - t_v$		X	X

We could ask ourselves if it is possible now to optimize the rounding scheme of the t_i's for both the half PWM cycles and the whole PWM cycle. Comparing Table 9 with Table 6, we see that the tables don't show equal combinations of Truncating and Ceiling for $p=1$ and $p=2$. This means that minimizing the range of $e_{q,PW}$ can only be done per half PWM period OR per whole period.

Studying (44), we see that $e_{q,PW}$ per half-cycle corresponds with an error of u^+ of:

$$e_{q,u} = \frac{2A\Delta PW}{T_z}$$

$$(79)$$

From (79) we find that if the rounding mechanism is optimized for each half PWM cycle, the PW spacing ΔT corresponds to a control signal u^+ spacing of:

$$\Delta u^+ = \frac{2A}{N}$$

$$(80)$$

When normal rounding was used, the $e_{q,PW}$ interval in (76) resulted in a spacing of $\Delta u^+ = 4A/N$, so we see that the better rounding scheme results in a one bit gain for the PWM DAC, which can also be calculated using (64).

8.5 Four Samples per Cycle

In the case that each t_i is calculated with its own sample of u^+, digitalizing the switching times to $t_{d,i}$ results in independent quantization errors $t_{q,i}$. The individual values of $t_{q,i}$ are minimized when normal rounding is used to calculated the $t_{d,i}$'s from the t_i's, using (65a) and (-b), resulting a range of ΔT for $t_{q,i}$. Filling in $\Delta t_i = \Delta T$ in (45) yields a quantization spacing of u^+ of:

$$\Delta u^+ = \frac{4A}{N}$$

$$(81)$$

This is the same result as in paragraph 8.2, where the resolution of u^+ is given by (70).

8.6 Pulse Width Resolution and Minimum Quantization Error Interval

Using the same number of N, the resolution of u^+ is one bit less in the case of double sampling of u^+ per PWM cycle than in the case that the PW was calculated optimally for the whole PWM cycle using one sample of u^+. For the case that four samples of u^+ are used to calculate the $t_{d,i}$'s, it is even two bits less than in the case of sampling once and the optimal rounding scheme was used. The table below summarizes the resolutions for one, two, and four samples per PWM cycle, and for normal rounding and optimal rounding (minimized $e_{q,PW}$) that were derived in this chapter:

Table 10: Quantization Intervals Δu^+ for different numbers of samples per PWM cycle and for normal or optimal rounding schemes

	$T_{s,PWM}=T_z$	$T_{s,PWM}=T_z/2$	$T_{s,PWM}=T_z/4$
Δu^+ for normal rounding	$\dfrac{4A}{N}$	$\dfrac{4A}{N}$	$\dfrac{4A}{N}$
Δu^+ for optimal rounding	$\dfrac{A}{N}$	$\dfrac{2A}{N}$	$\dfrac{4A}{N}$

This could be expected, because the range of $e_{q,PW}$, which remains ΔT, is spread now over only half the PWM cycle, instead of over the whole PWM cycle. Generally, if we optimize the rounding scheme for a constant control voltage for N PWM cycles, the overall range of $e_{q,PW}$ will still be ΔT, but divided by T_z, the range of $e_{q,PW}$ will go to zero for $N\to\infty$, or, equivalently, Δu^+ will become infinitely high for constant u^+. For an u^+ that is not constant in time, however, the rounding scheme that was optimal over N PWM cycles for a constant level of u^+, is not optimal anymore.

An idea could be to optimize the rounding scheme over the number of (quarter) PWM cycles corresponding to the bandwidth of the control loop. This means, that we have to look first over how many (half) periods of the PWM the controller output signal remains approximately constant. However, if a *noise shaper* is used, to be discussed in chapter 10, the rounding scheme over several half periods will be affected by the noise shaper quantization error feedback.

9. Effects of the Digitalized Pulse Widths on the Current Error

In the former chapter, attention was paid to the quantization errors of the PW's, which are caused by the final time resolution of the switching times. These quantization errors were studied by taking the PWM apart. In this chapter, the PWM with digitalized PW's is placed in the control loop, at the place of the ZOH and the DAC after $C(z)$ in Figure 16.

In Figure 17(d), a drift of $E_c(t)$ is shown occurring in the digital GACL. As will be explained in this chapter, the drift is an effect due to the DAC after the digital controller.

In this chapter, $e(t)$ and $E(t)$ due to the error in the full-bridge PW's $e_{q,PW}$ will be studied in a deterministic way for the case that an initial current error $e(0)=e_0$ is present. The error behavior studied in this chapter will seem to be typical for the case that a DAC is in the controller loop.

The simulation model used in this chapter is the same as in Figure 30, so $B(s)$ and the ADC are not in the loop. The comparators of the PWM in Figure 29 now contain the rounding mechanism to obtain the digitalized PW's, so that the PWM in Figure 30 acts as a DAC.

In the figure below, $I_{ref}(t)$ consists of only one current trapezium, with the time running till 20[ms]. PWM with digitalized PW's (normal rounding, one sample of u^+ per PWM cycle) was used for this simulation. Notice that $E_c(t)$ drifts away after 4[ms], and that it stabilizes at $t{\approx}0{,}016$[s] at a final value of about -871[μAs]. The reason for this drift will be explained in this chapter.
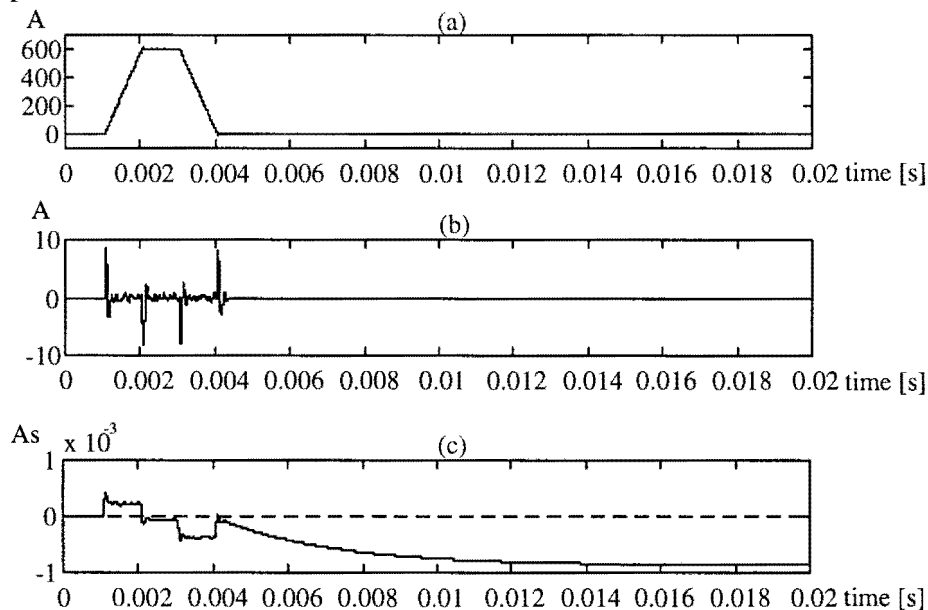
Figure 47: PWM with sampling and digitalized PW's, N=300; (a): $I_{coil}(t)$ (b): $e_c(t)$ (c): $E_c(t)$

9.1 Errors around Reachable Values of the Reference Current

This drifts of $e_c(t)$ and $E_c(t)$ in Figure 47 seem to be consequences of the digitalized PW's. If u^+ is within the band defined in (82) of half the quantization interval around 0V, the corresponding analog PWM pulses are rounded to a 0V PWM output pulse.

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$$-\frac{\Delta u^+}{2} < u^+ < \frac{\Delta u^+}{2}$$

$$(82)$$

This band of u^+ can be defined for every symmetric rounding scheme, for which u^+ is rounded to an integer multiple u_d^+ of Δu^+ according to the rules in (65a) and (-b), in which ΔT, t_i, and $t_{d,i}$ are replaced by Δu^+, u^+, and u_d^+, respectively.

In the loop in Figure 30, u^+ equals the output of $C(s)$, and therefore control over G is lost if u^+ is within the band of (82). In order to examine the resulting drift effects, we put $I_{ref}(t)=0$. Then, $e(t)$ is given by:

$$e(t) = -I_{coil}(t)$$

$$(83)$$

If there is no control over the plant for $t>0$, so the output of the PWM full-bridge remains 0V, the current $I_{coil}(t)$ can be calculated for the following R-L network, not taking into account the filters LP1 and LP2:
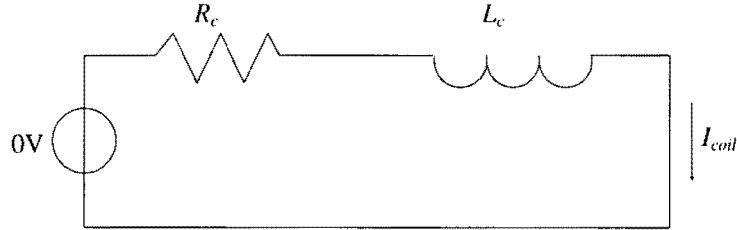
Figure 48: Gradient coil network when PWM output is 0V; LP1 and LP2 are not taken into account

Solving $I_{coil}(t)$ yields the following exponentially decaying current form:

$$I_{coil}(t) = I_0 e^{-\frac{R_c}{L_c}t}$$

$$(84)$$

where I_0 is the initial current at $t=0$.

In the time domain, the differential equation of the controller is given by:

$$PI_{out}(t) = K_p e(t) + \frac{K_p}{\tau}\int_0^t e(t)dt$$

$$(85)$$

Filling in (84) in (85), yields the following expression for $u^+(t)$ (remember that $PI_{out}(t) = u^+(t)$):

$$u^+(t) = K_p I_0 \left(\frac{L_c}{R_c \tau} - 1\right)e^{-\frac{R_c}{L_c}t} - \frac{K_p I_0 L_c}{R_c \tau}$$

$$(86)$$

For a zero output signal of the PWM, the absolute value of (86) must be within the band defined in (87):

$$K_p |I_0| \cdot \left| \left(\frac{L_c}{R_c \tau} - 1 \right) e^{-\frac{R_c}{L_c} t} - \frac{L_c}{R_c \tau} \right| < \frac{\Delta u^+}{2}$$

(87)

Because the time constant τ of $C(s)$ is chosen $\tau = L_c/R_c$, (87) is reduced to:

$$|I_0| < \frac{\Delta u^+}{2 K_p}$$

(88)

We can also easily integrate $e(t)$ to find $E(t)$:

$$E(t) = \int_0^t e(t) dt = \frac{I_0 L_c}{R_c} \left(e^{-\frac{R_c}{L_c} t} - 1 \right)$$

(89)

A value of special interest is:

$$E(\infty) = \frac{-I_0 L_c}{R_c}$$

(90)

Using the limit of I_0 given in (88), we find:

$$|E(\infty)| < \frac{\Delta u^+ L_c}{2 K_p R_c}$$

(91)

Now, we can generalize the preceding analysis for the case that $I_{ref}(t)$ is constant at a value corresponding to a realizable value of the PWM input $k\Delta u^+$:

$$I_{ref}(t) = \frac{k \cdot \Delta u^+ g_{PWM}}{R_c} = k\Delta I_{ref}$$

(92)

In (92), g_{PWM} is the voltage gain of the PWM ($g_{PWM}=35$), and k is an integer: $k=0,\pm1,\pm2,\ldots$. In order to maintain $I_{coil}(t)=I_{ref}(t)$ in (92) stationarily, the output of $C(s)$ has to be $k \cdot \Delta u^+$ stationarily. This means that the end value of the integrator in $C(s)$ has to reach this value, as $e(\infty)=0$.

Now, if we want to keep the PW at the width belonging to $k \cdot \Delta u^+$ at the input of the PWM for a certain value of $I_{coil}(t)$ given in (92) increased by an initial deviation ΔI_{coil0}, we find that ΔI_{coil0} must satisfy (88), replacing $I_0=\Delta I_{coil0}$. In this case, the expression for $I_{coil}(t)$ yields:

$$I_{coil}(t) = \frac{k \cdot \Delta u^+ g_{PWM}}{R_c} + \Delta I_{coil0} e^{-\frac{R_c}{L_c}t}$$

<div align="right">(93)</div>

The expression for the final value of $E(t)$ is the same as in (90), replacing I_0 by Δi_{coil0}.

9.1.1 Maximum Drifts in E(t) and Master Clock Frequency

In the table below, (91) is evaluated for the values Δu^+ for different numbers of samples per PWM cycle and for normal and optimal rounding as in Table 10:

Table 11: Maximum values for $|E(\infty)|$ for different numbers of PWM samples per cycle using different rounding schemes

	$T_{s,PWM}=T_z$	$T_{s,PWM}=T_z/2$	$T_{s,PWM}=T_z/4$
maximum $|E(\infty)|$, normal rounding	$\dfrac{2AL_c}{K_p R_c N}$	$\dfrac{2AL_c}{K_p R_c N}$	$\dfrac{2AL_c}{K_p R_c N}$
maximum $|E(\infty)|$, optimal rounding	$\dfrac{AL_c}{2K_p R_c N}$	$\dfrac{AL_c}{K_p R_c N}$	$\dfrac{2AL_c}{K_p R_c N}$

From the results of the table above, we can calculate how large N must to satisfy (4). Multiplying N by $1/T_z$=25kHz, the PWM frequency, we can find the required clock frequencies f_c as defined in (62):

Table 12: Minimal values of f_c (MHz) for obtaining $|E(\infty)|<10[\mu As]$ for different numbers of samples per PWM cycle (PWM frequency 25kHz) and different rounding schemes

	$T_{s,PWM}=T_z$	$T_{s,PWM}=T_z/2$	$T_{s,PWM}=T_z/4$
Normal Rounding, f_c	1458.35	1458.35	1458.35
Optimal Rounding, f_c	364.575	729.175	1458.35

Studying the table above, we see that 364.6MHz is the minimal f_c for which the criterium for $E(\infty)$ can be met. However, the next time that a current trapezium is generated, the drift might occur again, resulting in an accumulating $E(t)$, violating the criterium. Another disadvantage is that f_c=364.6MHz can only be used when sampling once per PWM cycle is used, and sampling once per cycle will result in less phase margin for the control loop than for sampling twice or four times per PWM cycle. Therefore, another solution must be found to take away the drift in $E(t)$. A solution to do this will be given in chapter 10.

9.1.2 Simulations showing the Drift in E(t)

Now, the analytical results derived in the first part of this paragraph will be illustrated by a PSI simulation with the model shown in Figure 30. In (85) K_p equals 3.7/35 instead of 3.7, because the detailed PWM has a voltage gain g_{PWM}=35. PWM with sampling once per cycle is used, with the non-optimal normal rounding scheme of paragraph 8.2, so that Δu^+ is given by (70).

For this simulation, we introduce the parameter l, that replaces the factor 2 resulting from substituting Δu^+ in (88):

$$I_0 = \frac{lA}{K_p N}$$

<div align="right">(94)</div>

For the simulation, the value for N is chosen to be 300, so one PWM cycle is divided in 300 equal parts. In this case, the upper border of the band defined in (82) is approximated if I_0 in (94) equals (l=-1.999):

$$I_0 = -\frac{1.999 A}{K_p N}$$

The simulation results are plotted in Figure 49. The plot (a) and (b) give the results when no digitalized PW's are used. They show that the controller actively controls the process to get rid of the initial current error $e(0)=-I_0$. In plot (c) and (d), digitalized PW's are used. In plot (c), also the negative version of the exponential signal of (84) is plotted, which equals the simulated $e(t)$, as expected. Notice that in plot (d) $E(t)$ reaches the value 1940[µAs], in accordance with (91).

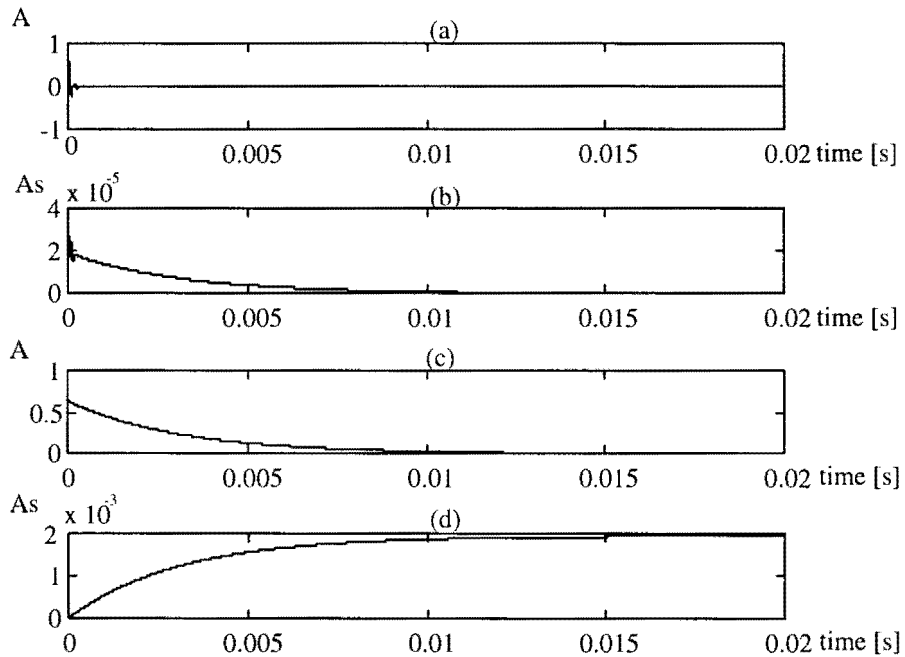*Figure 49: $k=0$, $N=300$, $l=-1.999$; (a): $e(t)$ for analog PW's; (b): $E(t)$ for analog PW's; (c): $e(t)$ for discrete PW's; (d): $E(t)$ for discrete PW's*

Now, in Figure 50, I_0 is chosen with $l=-2$ in (94), and again with $N=300$. In this case, plot (a) shows that the controller output changes the PWM output signal because the upper border in (82) is passed, and $e(t)$ is regulated to zero quickly.
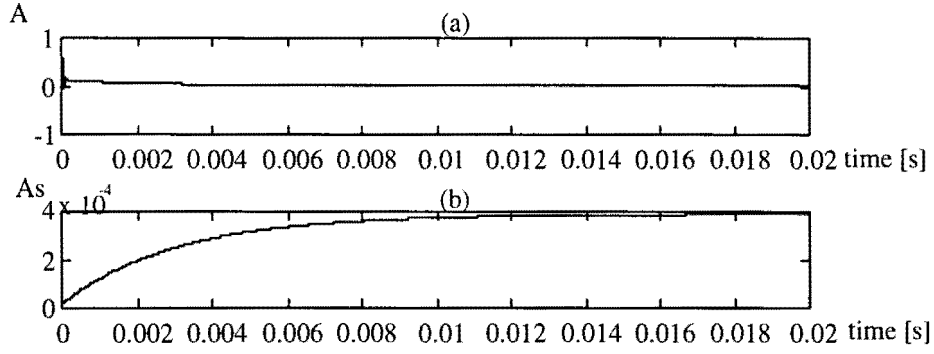
Figure 50: k=0, N=300, l=-2 (a): e(t), discrete PW's (b): E(t), discrete PW's

9.2   Errors around Unreachable Values of the Reference Current

If we want to reach a constant $I_{ref}(t)$ corresponding to a non-integer multiple of Δu^+ at the input of the PWM, say p, with $k<p<k+1$, where k is an integer, the output will not reach $I_{ref}(t)$ stationarily, but it will stay fluctuating around the desired $I_{ref}(t)=p\Delta I_{ref}$, where ΔI_{ref} is defined as in (92).

For the discussion below, let's assume that $I_{coil}(0)=I_{ref}(0)$, so that $e(0)=0$, so that the initial controller output is equal to the initial value of its integrator, which will be set to a voltage corresponding to $I_{ref}(t)$, thus $u^+(0)= PI_{out}(0) = p\Delta u^+$. This level of u^+ corresponds to an unrealizable output pulse of the PWM, so that PW will be digitalized to the closest realizable PW_d.
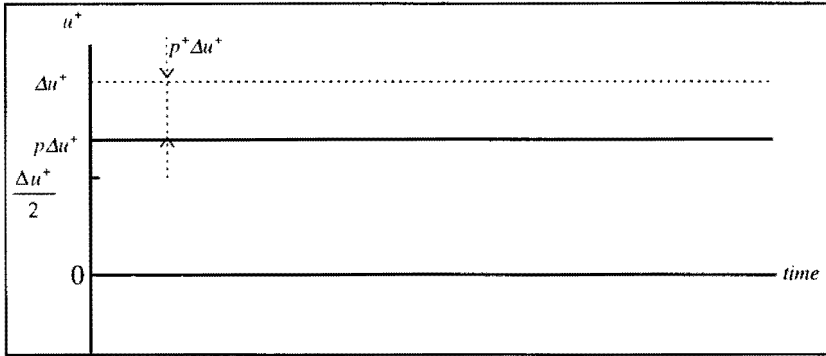
Figure 51: initial input of PWM corresponding to unreachable value of $I_{ref}(t)$

Assume that in Figure 51, $1/2 \le p < 1$, so that that $u^+=p\Delta u^+$ is rounded to a too high level $u_d^+ = \Delta u^+$, resulting in an exponentially increasing $I_{coil}(t)$. If we define $p^+=1-p$ (see Figure 51), we can write for the change in $I_{coil}(t)$:

$$\Delta I_{coil}(t) = p^+ \Delta I_{ref} \left(1 - e^{-\frac{R_c}{L_c}t} \right)$$

(95)

Now, $e(t)$ yields the negative version of (95). For $PI_{out}(t)$ we find the following expression:

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$$PI_{out}(t) = p\Delta u^+ + K_p e(t) + \frac{K_p}{\tau} \int_0^t e(t)dt$$

<div align="right">(96)</div>

Equating this formula for $PI_{out}(t)$ to $\dfrac{\Delta u^+}{2}$ and solving for t yields the crossing time t_1, and after this determining the next sampling time of the PWM greater than this crossing time, will give the moment that the PW changes to the level of $k=0$ (zero DC voltage). Solving this equation has to be done numerically, or can be estimated if the exponential power is approximated by a first- or second-order Taylor series. This will not be done explicitly, because as soon as we have to approximate the solutions numerically, it is better to run a Simulink simulation, what will be done in the next sub-paragraph.

9.2.1 Simulation showing the Fluctuations

For the simulation in Figure 52 the value of $p=0.8$ is taken, thus $I_{ref}(t)=0.8\Delta I_{ref}$. For the simulation, PWM with sampling once per PWM cycle and normal rounding is used.

The initial values of the integrators of the controller and the plant are taken as discussed above to prevent the occurrence of transients. So, $PI_{out}(0)$ is set to value corresponding to $I_{ref}(t)$, $PI_{out}(0)=0.8 \Delta u^+$. The outputs of the low-pass sections are given values corresponding to the PWM output PW, that follows from the value to which u^+ can be thought to be rounded for $p=0.8$, which is to Δu^+.

At $t=0$, $PI_{out}(0)$ is rounded to Δu^+, resulting in a too large PW. This will cause $I_{coil}(t)$ to grow, and therefore, $e(t)$ and $PI_{out}(t)$ will start to decrease. In Figure 52, it can be seen that $PI_{out}(t)$ dives under the level of $\Delta u^+/2$ at the crossing time t_1. The PW will be changed to a 0V PWM output at the next sample moment of the PWM, say $t_{s,1}$, and as a consequence, $e(t)$ starts to grow in the opposite direction, causing $PI_{out}(t)$ to grow in the opposite direction too. Then $e(t)$ will continue to grow in the new direction until at a next sample moment $PI_{out}(t)$ is above the $\Delta u^+/2$ level again, so that u^+ is rounded to Δu^+, and too large a PW is at the PWM output. This process will repeat itself, resulting in the oscillation of $I_{coil}(t)$ around the desired constant value of $I_{ref}(t)$, and thus $e(t)$ fluctuating around zero.

In plot (b), it seems that $E(t)$ is decreasing globally after all, meaning that still a transient effect is present.
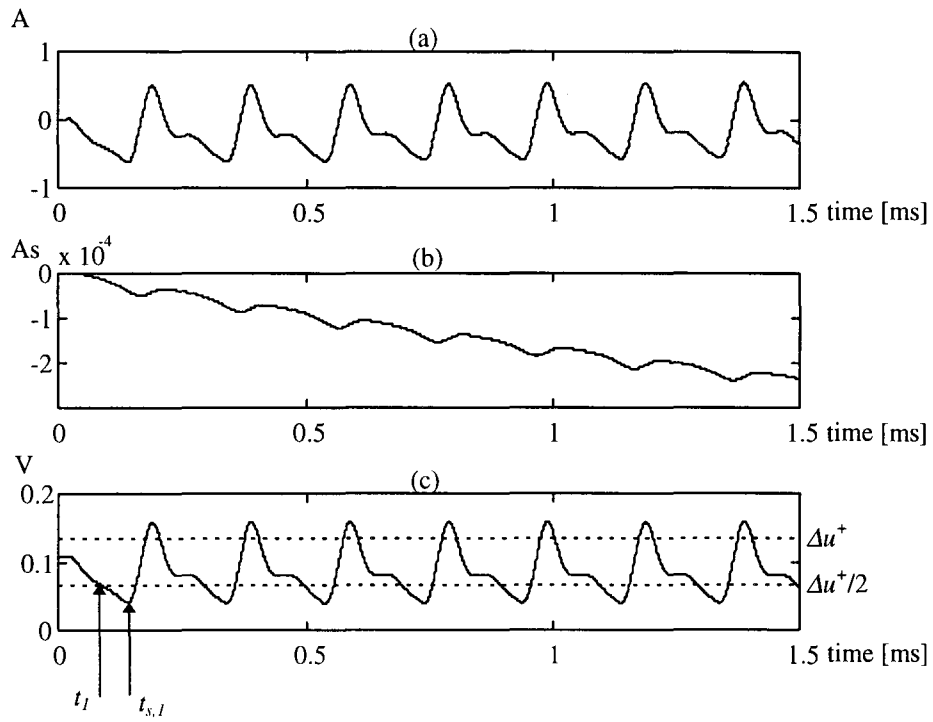
Figure 52: (a): e(t); (b): E(t); (c): u^+ (equal to Plout(t)); N=300, p=0.8

10. Implementation of a Noise Shaper to take away the Drift

At the end of paragraph 9.1, it was stated that even if the PW rounding scheme resulting in the smallest range of $e_{q,PW}$ is chosen, the drifts in $E(t)$ might accumulate, violating the criterium in (4). In this chapter, a solution to the drift problem is proposed, based on accumulating u^+ each sampling period with a delayed version of the quantization error.

10.1 The Function of the Noise Shaper

To prevent $e(t)$ and $E(t)$ from drifting away, a filter based on the structure in Figure 53 can be used, which is called *Noise Shaper* in digital audio techniques:
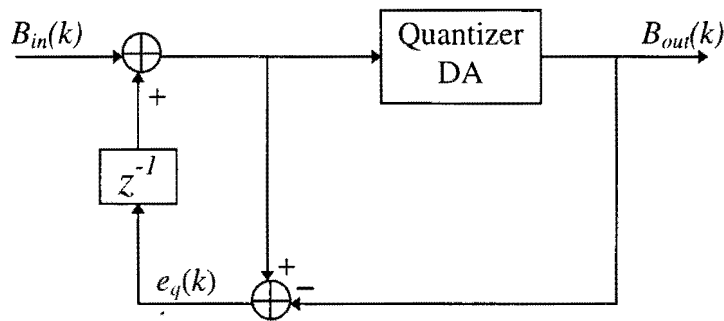
Figure 53: First-order Noise Shaper

In Figure 53, the quantization error $e_q(k)$ is added to the input $B_{in}(k)$ of the filter, delayed over the sample time T_s (represented by the block z^{-1}).

In the GACL with the digitalized PW's, the noise shaper is used to filter the quantization errors $e_{q,PW}(k)$ resulting from digitalizing $PW(k)$. The implementation of the noise shaper for the filtering of $e_{q,PW}(k)$ is given in Figure 54:
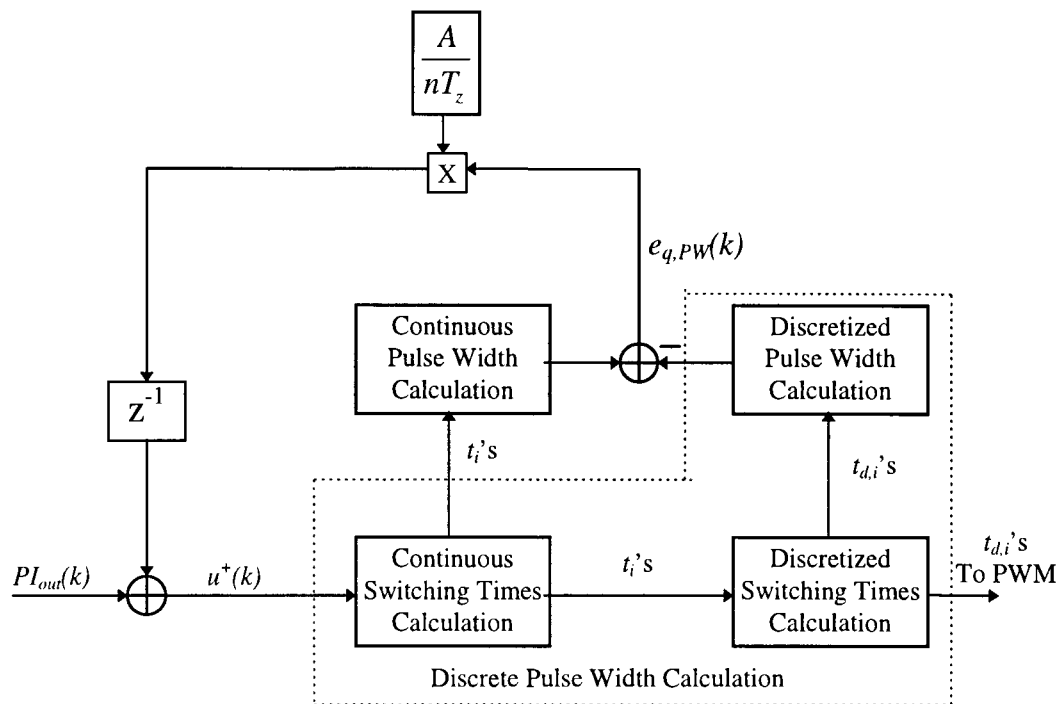
Figure 54: Implementation of the first-order noise shaper to the PWM input

In Figure 54, the factor z^{-1} represents the delay over one period of the PWM sampling time $T_{s,PWM}$ over which $e_{q,PW}(k)$ is fed back to the input of the discrete PW calculation block. Before adding $e_{q,PW}(k-1)$ to $PI_{out}(k)$, it is multiplied by a factor $A/(nT_z)$, where n is the number of samples per PWM cycle.

In the case that a constant value of the signal $PI_{out}(k)$ in Figure 54 is such that the corresponding PWM output is rounded to 0V by the quantizer, $e_{q,PW}(k)$ will increase $PI_{out}(k)$ until $u^+(k)$ becomes so large that the corresponding PWM output isn't 0V anymore. In the closed-loop system of the gradient coil, control can be retaken then, and as a result the drift signals $e(t)$ and $E(t)$ will grow in the opposite direction.

10.2 Theory on Noise Shapers

In [4], §10.3, a general treatment of noise shapers can be found. In that treatment, $e_q(k)$ is considered as white noise. For the GACL, if $PI_{out}(k)$ is varying relatively fast over adjacent periods, $e_{q,PW}(k)$ might be considered as white noise.

In the discussion of chapter 9, however, $e_{q,PW}(k)$ can not be considered as white noise, because the errors are completely deterministic there. On the other hand, if $u^+(k)$ is changing over many quantization steps per $T_s = T_{s,PWM}$, the theory on the noise behavior of the noise shaper is quite useful.

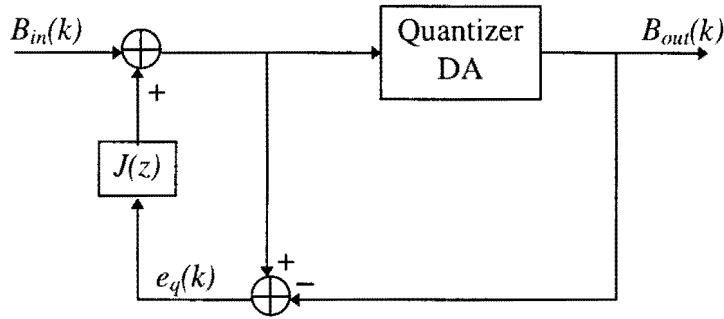The general noise shaper is represented as:

Figure 55: General form of a noise shaper

For the general noise shaper, the following formula can be found:

$$e_q(z)J(z) + B_{in}(z) - B_{out}(z) = e_q(z)$$

(97)

The quantizer is only implicitly within this expression. We can write equation (97) as

$$\frac{B_{out}(z)}{B_{in}(z)} = 1 - \frac{e_q(z)}{B_{in}(z)}(1 - J(z))$$

(98)

In expression (98), it is found that the signal transfer function is equal to 1, while the second part of the equation

$$e_q(z)(1 - J(z))$$

(99)

determines the error at the moment the output word length is reduced.

The term $(1-J(z))$ is usually called the noise transfer function and determines the coloring of the output noise. Because the signal gain equals 1, this error can be related to the input signal as well. In case the word length of a system is reduced to N bits, then a value

$$\frac{e_q}{B_{in}} = \frac{1}{2^N - 1} \approx 2^{-N}$$

(100)

is obtained. The value of $e_q(k)$ is thus equal to the LSB value of the N-bits output word. The noise shaping operation reduces the error even more, as will be shown. From equation (98) it is seen that the spectral density of the error signal at the output of the system is determined by the filter operation $(1-J(z))$.

For the case of the first-order noise shaper, we can write for equation (97) using $J(z)=z^{-1}$:

$$B_{out}(z) = B_{in}(z) - e_q(z)(1 - z^{-1})$$

(101)

The first-order filter operation reduces the power of $e_q(z)$ for low frequencies ($z \approx 1$). The total power of $e_q(k)$ is obtained by integrating $e_q(z)$ over the signal bandwidth f_b. Supposing that $e_q(k)$ is white noise in the band ($f=0$ to $f=f_s/2$), the result becomes:

$$e_{tot}^2 = \int_0^{\theta_1} e_q^2 \left|1 - z^{-1}\right|^2 d\theta$$

In this equation, $\theta_1 = \dfrac{2\pi f_b}{f_s}$, with f_s the output sampling frequency.

Inserting $z = e^{j\theta}$ we obtain

$$\left|\frac{B_{out}}{e_q}\right|^2 = \left|1 - z^{-1}\right|^2 = 2(1 - \cos\theta)$$

and

$$e_{tot}^2 = 2(\theta_1 - \sin\theta_1)e_q^2$$

Without the noise-shaping the total uniformly distributed noise over the band $\theta=0$ to $\theta=\theta_1$ is equal to:

$$e_{uniform}^2 = e_q^2 \int_0^{\theta_1} d\theta = e_q^2 \theta_1$$

Figure 56 shows the difference with or without the noise shaper. If $e_q^2=1$, the noise power is equal to the surface under the quadratic amplitude curve of the filter.
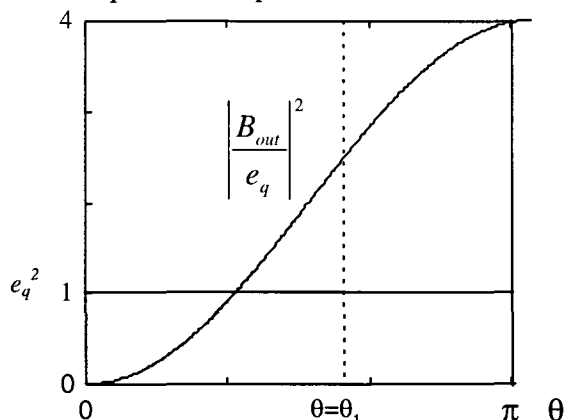

Figure 56: The quadratic amplitude transfer function of the noise shaper and the constant power of $e_q(z)$

In comparing the results of equations (104) and (105), the improvement with respect to noise and dynamic range of the system is obtained. Using F_1 as the dynamic range improvement factor we get:

$$F_1 = \frac{e_{tot}}{e_{uniform}} = \sqrt{2\left(1 - \frac{\sin\theta_1}{\theta_1}\right)}$$

Using a second-order Taylor approximation for $\sin\theta_1$, it can be calculated that the "Break Even Point" of (106) is at $\theta=\theta_1\approx0.61\pi$. Therefore, the noise reduction only exists when high enough oversampling is applied. This means, that for bigger values of θ_1, the total power of $e_q(k)$ is even larger than for the uniform case!

In the table below, the improvement factors F_1 are given for different numbers of samples per PWM cycle. The system bandwidth $f_b=10\text{kHz}$ is used for θ_1.

Table 13: F_1 for different PWM sample frequencies

	$T_s=T_z$	$T_s=T_z/2$	$T_s=T_z/4$
F_1	1.24	0.70	0.36

Table 13 shows that the largest reduction of the power of the quantization error is reached if four samples per PWM cycle are used.

Higher order noise shapers show even worse improvement factors for high bandwidths. Therefore, we will take a first-order noise shaper only.

10.2.1 Simulation: Normal Rounding Scheme, Single Sample per PWM Cycle, N=30 and N=300

In this sub-paragraph, two simulations are performed using of the noise shaper in the GACL. Single sampling per PWM cycle is used. The PWM cycle will be divided in 30 equal parts for the first simulation, and in 300 equal parts for the second simulation. The switching times are digitalized using the normal rounding scheme, as was done for the simulations in sub-paragraph 9.1.2. $I_{ref}(t)$ consists of only three current trapezia, and after these, it remains zero.

In Figure 57, the results are shown for the number $N=30$ when the noise shaper is used. Now, the maximum value of $E_c(t)$ is $-573[\mu\text{As}]$, and the end value is fluctuating around zero with a maximum amplitude of about $60[\mu\text{As}]$. If no noise shaper was used, the value of $E_c(t)$ could drift to a maximum of $4860[\mu\text{As}]$, according to Table 11. This means a reduction with a factor 81 of the drift in $E_c(t)$.

Comparing the behavior of $e_c(t)$ for the case that the noise shaper is used to the case that it wasn't, it can be seen that its amplitudes have increased, resulting in an increased quantization noise power. This could have been predicted by the fact that $F_1=1.24$ for $T_s=T_z$ as in Table 13.
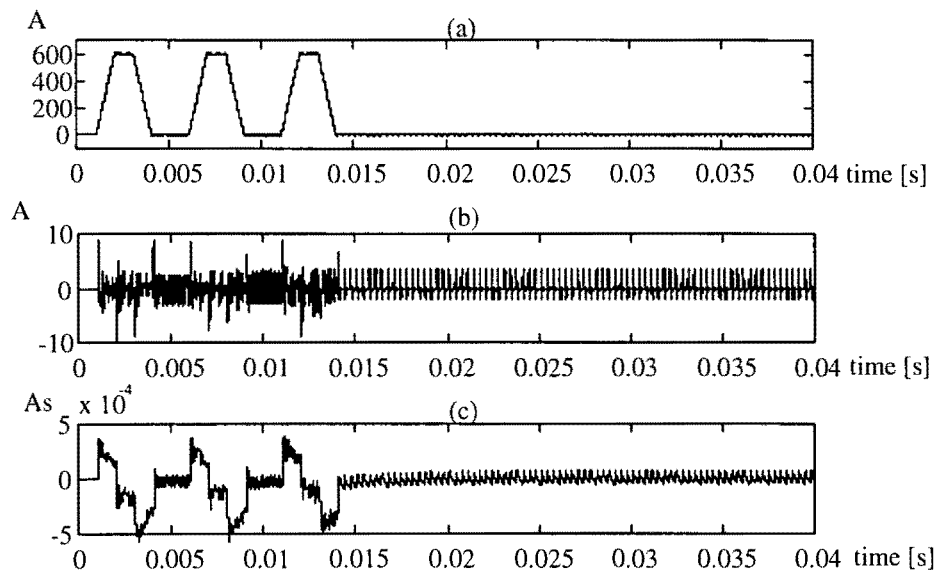
Figure 57: N=30, noise shaper is used. (a): $I_{coil}(t)$; (b): $e_c(t)$; (c): $E_c(t)$

For comparising the behavior with the results from chapter 8.3, the simulations are also carried out for the case that the PWM cycle is divided into 300 equal parts. Using the noise shaper, the error integral will fluctuate with an average amplitude of 60[μAs], which also means a reduction of a factor 81 compared to the largest value of 4860[μAs] that can occur due to drift when no noise shaper is used.
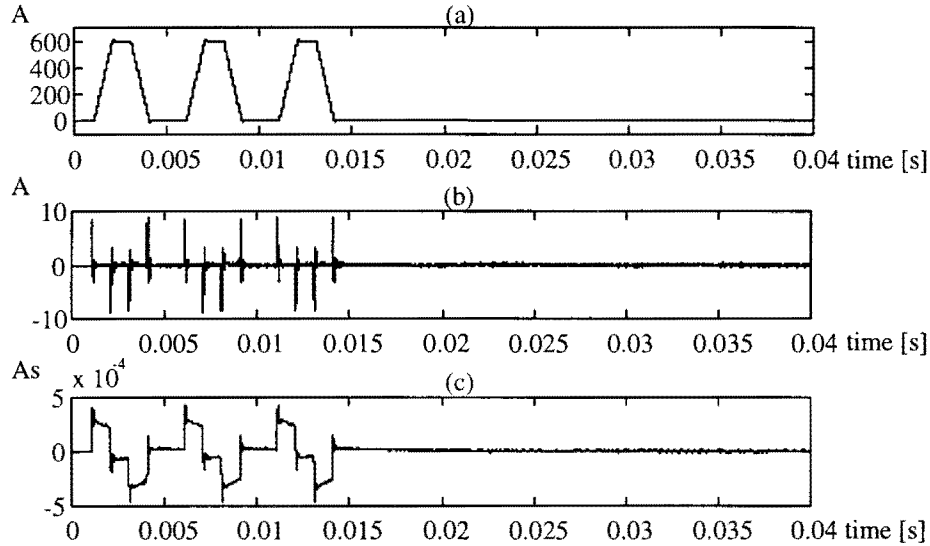

Figure 58: N=300, noise shaper is used. (a): $I_{coil}(t)$ (b): $e_c(t)$ (c): $E_c(t)$

10.3 Different Sampling Rates and Rounding Schemes

In this paragraph, simulations are carried out to study the oscillations in $e(t)$ and $E(t)$ resulting from the noise shaper. In order to keep it simple, the PWM using discrete PW's is replaced by a ZOH in series with a quantizer. The quantization interval of the quantizer corresponds to Δu^+ as given in Table 10. If the oscillation in $E(t)$ caused by the noise shaper must be limited to satisfy (4), N, the number of clock cycles of the master clock per PWM cycle, must be chosen large enough.

The first table gives the simulation results for the minimum values for N required to meet the criterium in the case that one sample per PWM cycle is used. For comparison with the case that no noise shaper would be used, the maximum values of the drift in $E(t)$ according Table 11 are also given. The better performance obtained by using the noise shaper is expressed by the improvement factor F_2, defined by division by 10[μAs] (the amplitude of $E(t)$ if the noise shaper is used) of the values following from Table 11.

Table 14: Minimal N and improvement factors F_2 for the case of $T_s=T_z$

	Minimal N	$E(\infty)$ [μAs]	F_2
Normal Rounding	750	778	78
Optimal Rounding	200	729	73

Table 14 shows that for $Ts=T_z$, using the optimal rounding scheme, N can be reduced from 750 to 200, while F_2 remains the same, approximately.

In the next table, the results are shown for sampling twice per PWM cycle.

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Table 15: Minimal N and F_2 for the case of $T_s=T_z/2$

	Minimal N	$E(\infty)$ [μAs]	F_2
Normal Rounding	350	1667	167
Optimal Rounding	200	1458	146

As shown in Table 15, also in the case of double sampling, N can be lowered considerably if the optimal rounding scheme is used, while F_2 doesn't change relatively much.

For the last table, sampling four times per PWM cycle is used. The normal rounding scheme is also the optimal rounding scheme for this case, as was discussed in paragraph 8.5.

Table 16: Minimal N and F_2 for the case of $T_s=T_z/4$

	Minimal N	$E(\infty)$ [μAs]	F_2
Normal Rounding	150	3889	389

According to the three tables above, using the noise shaper always results in an improvement factor F_2 much larger than unity. Minimal N in combination with the highest F_2 can be reached in the case of $T_s=T_z/4$. $N=150$ corresponds to a master clock frequency for the digital circuit driving the PWM of only 3.75MHz if $T_z=40[\mu s]$.

10.4 Conclusions

Positive feedback of the quantization errors seems to be an effective method to prevent the gradient current error from drifting. For every PWM sampling frequency T_s and every rounding scheme, a great reduction of the drifts in $E(t)$ can be achieved. According to the simulations, the greatest improvement in the behavior of $E(t)$ was obtained for the highest PWM sampling frequency with $T_s=T_z/4$. Another advantage of choosing the highest sampling frequency is the lower variance of $e(t)$ caused by quantization effects. This results in lower amplitudes of $e(t)$.

11. Conclusions and Recommendations

11.1 Conclusions

Studying the analog gradient amplifier control loop learns that this structure is not suited to meet the criterium of a maximum integrated current error of 10[μAs]. Extra delay times inherent to a sampled system result in less phase margin, and therefore in more oscillatory behavior. General expressions for the final value showed that $E(\infty)$ is heavily dependent on delays and second-order filters in the open-loop of the present analog control loop.

A great reduction of the current error and its integral can be obtained by designing an appropriate feedforward filter. If the transfer of the feedforward path is a combination of second-order low-pass filters, the final values of the current error and its integral are zero. The best overall performance is obtained by making the feedforward path linear phase. The linear phase characteristic reduces the current transients considerably, so that the 10[μAs] criterium can be met all of the time in the simulations. The reduced range $e(t)$ results in a gain of about four bits for the AD converter in the error path.
In practice, however, the performance of feedforward using filters is dependent on the accuracy of the estimate of the delay time of the feedforward path over which the reference signal must be delayed in the reference path. This problem, however, also exists for the original analog control structure, where the delay corrected error was calculated.

Digitalizing the pulse widths is inherent to calculating the PWM switching times digitally. Dependent on the number of samples used per PWM cycle (one, two, or four samples), the switching times can be rounded such, that the range of the pulse width error is minimized for the specific sampling rate. A high resolution can be realized at a relatively low sampling rate (one sample per PWM cycle), but even then, accumulating drifts may occur in the integrated current error, violating the criterium. A noise shaper can take away this drift, but the drift is replaced by an oscillation. The amplitude of this oscillation, however, can meet the criterium if the resolution of the digitalized pulses is high enough. If each switching time is calculated using a different sample (sampling four times per PWM cycle), the criterium is met using a master clock frequency of 3.75Mhz (PWM cycle divided in 150 equal parts), corresponding to a relatively low pulse width resolution.

11.2 Recommendations

Applying feedforward releases the controller of tracking the reference current. It could be redesigned to suppress disturbances and model uncertainties. Modern control methods as LQG or H_∞ could be used to control the integrated current error directly.

Using higher sampling rates for updating the PWM switching times, e.g. four samples per cycle, results in a Nyquist frequency higher than those of the lowest PWM voltage pulse harmonics. As a consequence, the current ripple resulting from the lowest PWM voltage harmonics is in the control bandwidth now, so that higher cutoff frequencies could be chosen for LP1 and LP2, and the controller has to be redesigned to reduce the ripple. For the same reason, it must be studied if it is still necessary to connect four PWM modules in parallel to apply the multiple-phase principle.

Attention must also be paid to digital filtering techniques. Possibly in combination with a modern controller, the oscillations caused by the noise shaper could be suppressed, or the oscillations could be shifted to higher frequencies.

In principle, a feedforward could also be applied in the analog GACL. This would require extra analog filters in the feedforward path. Using a computer, this filtering can be performed digitally, resulting in a cheaper realization of these filters. In combination with a newly designed controller and some extra "tricks" like e.g. using a noise shaper, the system performance can be improved, and costs might be reduced, giving a good foundation to digitalize the GACL.

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