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A miniaturized 5.2 Watt battery charger

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A Miniaturized 5.2 Watt Battery Charger.

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Abstract

In the present report a complete theoretical analysis and practical design of a miniaturized 20cc, 5.2 Watt battery charger will be given. A standard flyback topology is chosen, theoretically analyzed and implemented. The need to reduce the number of components resulted in an integrated flyback solution, the VIPer20 of SGS-Thomson. A novel frequency reduction technique is introduced to prevent the battery charger to operate in burst mode at low output loads and high input voltages, followed by a practical implementation. The electrical losses in the converter are identified, calculated and successfully verified by measurement. The feedback loop is theoretically analyzed using the state space averaging method, which results in a dynamic small signal (AC) and steady state (DC) model of the converter operating in current and voltage regulation mode. From these models the Bode plots are calculated and successfully verified by a closed loop gain measurement. The electrical volume of the prototype battery charger is 25cc due to the chosen transformer. When using flying leads 20cc is possible.

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1. Introduction

1.1 Formulation of the Problem

To obtain more freedom in the mechanical construction and casing design of power supplies used for charging battery packs of cellular phones, one needs to reduce the electrical volume by using smaller and/or less components. Here a contradiction occurs, since the customer is nowadays interested in features like fast charging, which more or less implies that high charging currents should be used, and low standby losses. This does not automatically result in smaller and/or less components. By decreasing the casing dimensions, we also decrease the overall convection area. As a result the internal losses of the power supply should be kept as low as possible in order to maintain the temperature of the power supply at an acceptable level. The price of the power supply should also be considered from a cost-saving point of view. The bill of material should be kept as low as possible.

1.2 Description of Assignment

The assignment of my graduation project was to develop a small battery charger, which can be used to charge NiCd, NiMH and Li-Ion batteries. The output specifications are a regulated continuous output current of $800mA \pm 10\%$ at an output voltage of $6.5V \pm 10\%$ for NiCd and NiMH and $4.1V \pm 1\%$ for Li-Ion. While operating in current regulation an output voltage down to $3V$ must be guaranteed. Below $3V$ current foldback should occur. The power supply is not allowed to operate in burst mode at the minimum output current of $50mA$. The input voltage is universal mains, which is an input voltage of $85V$ up to $265V$. The power supply should meet the EMI and safety regulations. These specifications must be achieved in a volume of $\pm 20cc$. For a better understanding of the battery charger output voltage and current, we will give a full explanation below.

The battery charger output voltage and current are given in Fig. (1.1). This graph depicts the complete charge cycle of an entirely discharged battery pack. The ideal situation is represented by the dashed lines, the drawn curve is normally measured.
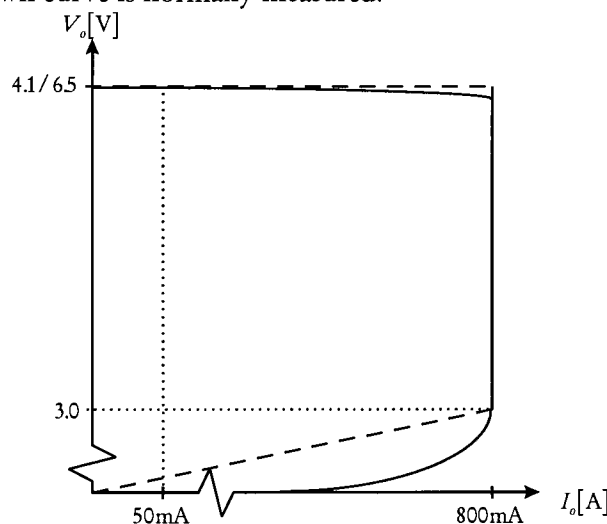
Fig. (1.1) Ideal and normally measured output voltage and current of the battery charger

When the charger is connected to the cellular phone it will first operate in voltage regulation mode. A series resistance in the cellular phone with the impedance of the battery pack will limit the pre-charge current to $50mA$. During pre-charge the voltage of the battery pack will rise up till $3V$ and at that point the charging control of the cellular phone is activated. The series resistance is short circuited by a MOSFet internally in the cellular phone, causing the battery charger to operate in

current regulation mode. In this stage the battery pack is charged at the maximum current of 800mA. We are now at the vertical line in the graph. The battery voltage will increase to the nominal battery pack voltage. At this point we are in the "knee" of the $V_o - I_o$ curve, and the charger will change from current to voltage regulation mode. The charge control circuit in the cellular phone will identify a completely charged battery pack at the horizontal part of the $V_o - I_o$ curve and will shut down.

1.3 Report Description

A first step in the development of the power supply is choosing the right topology. Since lots of combinations are possible with the topologies which are nowadays available, we reduced the possibilities to the ones which were actual at EPM in the period I started my graduation project. After a short comparison, given in Chapter 2, between different topologies, we have chosen one topology to be studied. In Chapter 3 a complete theoretical analysis and design will be given. A power supply is, like a lot of electronics, a controlled system and it uses a feedback loop to increase system performance. The improper closing of such a loop may result in overshoot, instabilities or even worse system performance as without a closed feedback loop. In Chapter 4 a equivalent Steady-State (DC) model and a Dynamic (AC) Small Signal Model of the converter including its current and voltage feedback system will be derived. By using these models we can predict the behavior of the converter and this will be verified by measurements. Minimizing the volume was one of the main targets of this project. This implies less convection area and therefore the electrical losses must be kept below an acceptable level. A detailed analyses and calculation of the electrical losses is given in Chapter 5 followed by a verification by measuring the efficiency of the converter. Meeting the EMI level can be a problem due to the switching behavior of the converter. Chapter 6 is devoted to the EMI behavior of the converter, EMI measurement setup and EMI levels. Since the measurements already done do not cover all the specifications of the battery charger, we describe several general measurements in Chapter 7. A summary of the conclusions in this report and recommendations are given in Chapter 8, followed by some additional derivations and explanations in the Appendices

In this Chapter we have set out the object of this project. In the next Chapter we will decide which topology is the best choice for this application.

2. Topology and Converter Choice

2.1 Topology Choice

The first and rather important decision in this project is choosing the right topology, which roughly fixes the electrical structure and the setup of the power supply. In order to choose the best converter topology for this application, we have made a comparison of several topologies which were actual at EPM in the period I started my graduation project. See Table (2.1) for a short overview.

	Resonant LLC converter	Resonant LLC converter with input voltage pre-conditioner	Conventional fly-back converter	Bi-directional fly-back converter
transformer	E16	E13	E13	E13
input filter	CLC filter	CLC-filter	CLC-filter	CLC filter
output filter	low pass filter	low pass filter	low pass filter	low pass filter
switches	primary two MOS-Fets, secondary two diodes	primary two MOS-Fets, secondary two diodes	primary a MOS-Fet, secondary a diode	primary and secondary a MOS-Fet
switching frequency	75-105kHz	35-45kHz	100kHz	100kHz
primary peak current	$\dfrac{\pi P_o/\eta}{V_{DC_{min}}\cos(\vartheta_{f_{min}})}=338\text{mA}$	$\dfrac{\pi P_o/\eta}{V_{DC_{min}}\cos(\vartheta_{f_{min}})}=338\text{mA}$	$\sqrt{\dfrac{2P_o}{\eta L_p f_s}}=430\text{mA}$	$\sqrt{\dfrac{2P_o}{\eta L_p f_s}}=430\text{mA}$
primary maximum voltage	V_{DC}	V_{DC}	$V_{DC}+NV_o$	$V_{DC}+Nv_o$
complexity control system	half bridge driver, VCO, voltage reference	half bridge driver, VCO, voltage reference	PWM, voltage reference	two control loops, consisting of two accurate voltage sensing circuits, primary a PWM circuit
EMI	+ +	+ +	0	+
efficiency	65-70%	70-75%	60-65%	65-70%
volume	-	-	0	+
result	Universal input increases the transformer size and therefore is this topology not useful	Input voltage control increases the total size and therefore is this topology not useful	Although not original, due to the small amount of components is this topology useful	control circuits are not yet integrated and therefore too complicated to build discrete

Table (2.1) A comparison between different topologies

The final choice is more or less based on the number and the size of the components, especially the transformer, necessary to build the converter. Table (2.1) shows that the conventional fly-back converter is the best choice when considering size and the number of components. When considering EMI, a LLC based converter is more applicable, but the universal mains aim increases the size of the transformer. This can be overcome by using an input voltage pre-conditioner and therefore by increasing the number of components. The bi-directional flyback converter is interesting because of the low switching losses. A problem using this topology is the complexity of the primary and secondary control circuits, which are not yet integrated at the present moment. Because of the fact that the topology as such is rather interesting for miniaturisation aims, we have included a small description of a possible implementation of a bi-directional flyback converter in Appendix D. Every topology has it's own merits and demerits, but since miniaturisation is the most important aim in this project we therefore have chosen for the conventional flyback converter. A next step in the decrease of the number of components is integration and therefore we will now investigate several integrated flyback solutions.

2.2 VIPer20 Integrated Flyback Solution

At the beginning of this project we have made a short inventory of the integrated control circuits which include a high voltage MOSFet and are easy available. We came up with the next three integrated circuits,

- TEA1401T from Philips,
- TOP221 from Power Integrations,
- VIPer20 from SGS-Thomson.

In order to make a choice between one of the listed i.c.'s, we made a comparison using the following considerations,

- flexibility of the integrated circuit in, for example, adjustable switching frequency, control loop gain and phase correction,
- voltage or current mode control,
- package layout,
- price,
- knowledge of the integrated circuit already at EPM.

See Table (2.2)for a summary of the results.

	TEA1401T	*TOP221*	*VIPer20*
flexibility	+ +	-	+ +
voltage/current mode control	current	voltage	current
package layout	SO20	DIL-8/TO220	PowerSO-10
price	Fl 2.10	Fl 1.20	Fl1.20
knowledge at EPM	+	+	-

Table (2.2) Results of the comparison of the three integrated flyback solutions

The VIPer20 is chosen since it is flexible, has a current mode control strategy, the package layout can easily use the printed circuit board as a heat spreader, it is not as expensive as the TEA1401T and EPM's knowledge concerning the VIPer20 can be extended, since it has never been used in one of EPM's power supplies.

The Viper20 is a combination of a current mode controller, protection circuit, start-up power supply and a high voltage MOSFet in one integrated circuit, as shown in Fig. (2.1). This integrated combination is ideal in our case, since we are aiming at a minimal electrical volume.
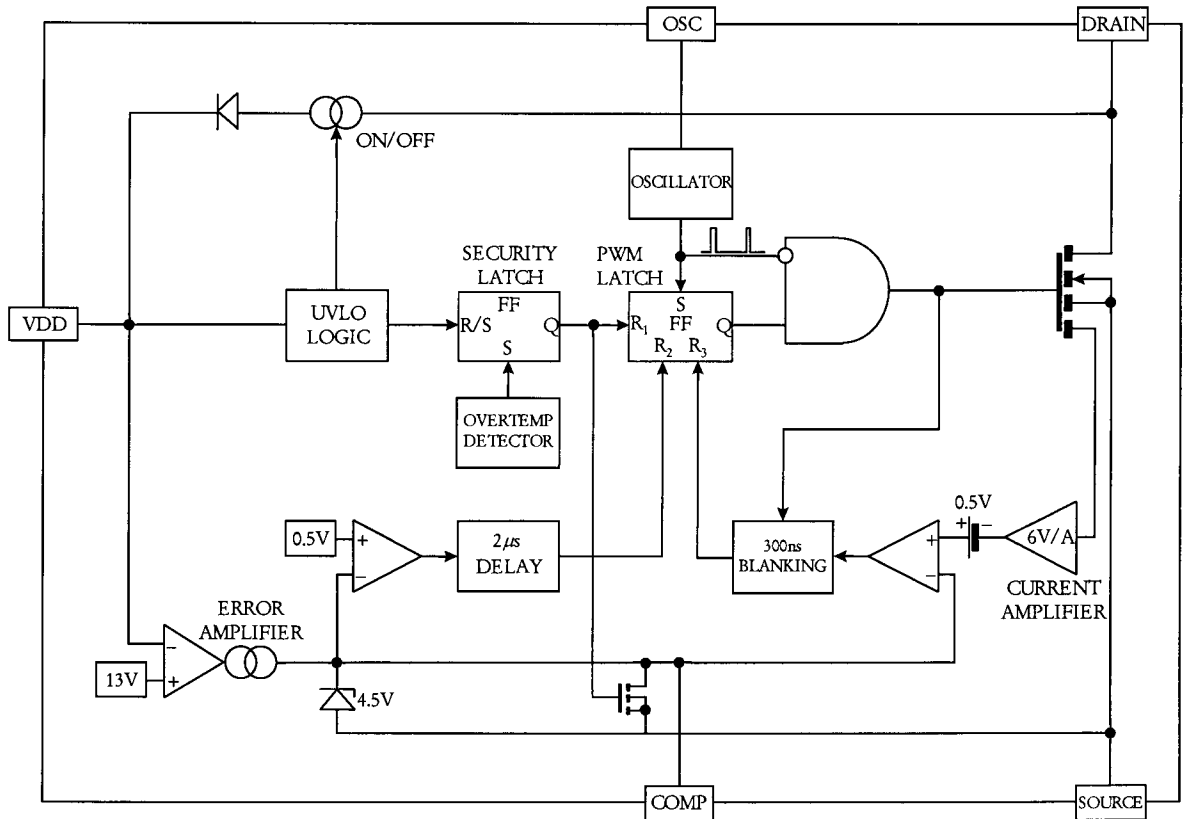
Fig. (2.1) Block diagram of the VIPer20

First we will shortly explain the operation of the VIPer20. The MOSFet is switched off during startup and at this time the high voltage current source is charging a capacitor which is connected to the V_{DD} pin. As a consequence the voltage at the V_{DD} will increase until the voltage reaches 11V . At this point, the internal high voltage current source is switched off and the control logic is activated causing the converter to start switching. The level of V_{DD} is decisive for the operation mode of the converter. If $V_{DD} \leq 8V \lor V_{DD} \geq 13V$ then the converter is shut down. If $8V < V_{DD} \leq 12.5V$ then the converter is operating in secondary sensing mode and uses the information of the comp pin. If $12.5V < V_{DD} < 13V$ then the converter is operating in primary sensing mode and uses an internal voltage reference to control the V_{DD} voltage, which is directly coupled to the output voltage.

The most important features of the VIPer20 are listed below,
I.   adjustable switching frequency up to 200kHz,
II.   current mode control,
III. under voltage lock-out with hysteresis,
IV. integrated start-up supply,
V.   over temperature protection,
VI. PowerSO-10 casing.

Ad I. The switching frequency will be determined externally by a capacitor and resistor combination and because of that it is possible to adjust the switching frequency, which will be shown in the present report. The fact that the switching frequency is not internally determined creates more design possibilities.

Ad II. The internal controller is a current mode controller, which has the advantage of complete rejection of the 100Hz input ripple at the output. This means that no 100Hz ripple will be

present in the output and therefore the cut off frequency of the control loop can be beneath 100Hz, which results in an easy to stabilise control system.

Ad III. The under voltage lockout will be used to create a foldback function at the output. Since the output voltage and the supply voltage are directly coupled, it is possible to switch the converter of whenever the output voltage drops below a stated level.

Ad IV. The integrated start up supply, which is switched off during normal operation, reduces the losses which are normally produced in the start up resistors.

Ad V. No external circuit is needed to protect the VIPer20 for over temperature

Ad VI. The PowerSO-10 casing has the advantage to conduct the heat to the printed circuit board and will therefore be used as a heat spreader. The mechanical layout of the PowerSO-10 casing is depicted in Fig. (2.2).
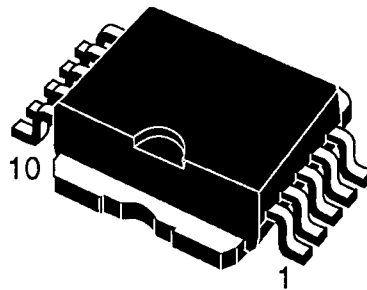
Fig. (2.2) PowerSO-10 casing of the VIPer20

The VIPer20 is an interesting circuit to make a power supply with, however it does have some serious disadvantages. First of all the heat spreader connected to the PowerSO-10 casing is electrical connected to the drain of the internal MOSFet. Since the drain voltage contains very high (600V) and very steep flanks, is this a disadvantage from an EMI point of view. Another disadvantage is the fact that the VIPer20 can handle up to 20W mono input and 10W universal mains, which is approximately twice the power we need. The area of the internal MOSFet could have been smaller, resulting in a smaller C_{DS}. This would have been interesting from an efficiency point of view, since the switching losses are proportional to $\frac{1}{2}C_{DS}V_{DS}^2$. The last disadvantage, which can be directly concluded from the data-sheets is the minimum on time of the MOSFet, which is $0.3\mu s$. This minimum will cause the power supply to operate in burst mode at low output power. A way to overcome this problem will be shown in the present report.

In this chapter we have made two decisions, i.e. the use of a conventional flyback topology and the use of the VIPer20. In the next chapter we will design a flyback converter when using the VIPer20.

3. Design of the Flyback Converter

3.1 Design of the Input Circuit

The input circuit used in this power supply is depicted in. Fig. (3.1).
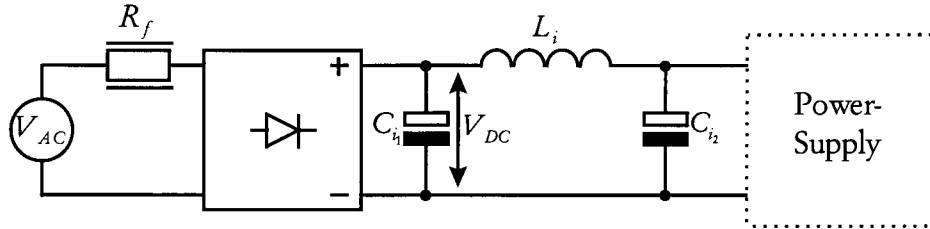
Fig. (3.1) The input filter section.

The input filter has two functions, namely preventing the input voltage to drop below a stated level of 70V, it's energy buffer function, and EMI suppression, it's filter function. For calculating the minimum capacitance, which should be available to guarantee the minimum input voltage level, we invoked the principle of conservation of energy. The minimum amount of energy, which should be stored in the capacitors and the inductor during the on time of the diode bridge, is equal to the energy which is transferred to the output divided by the efficiency of the remaining circuit, minus the energy taken directly from the mains, whenever the diode bridge is conducting, thus

$$E_C = \frac{E_o}{\eta} - E_{mains} .$$

Since the load, and therefore the output power is constant, we can calculate the charging and discharging times of the capacitors by applying some basic trigonometrics to the graph depicted in Fig. (3.2).
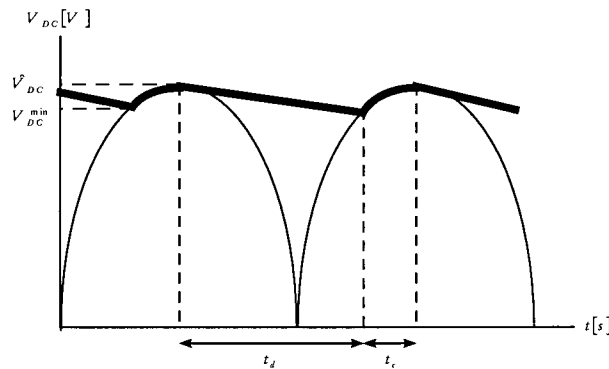
Fig. (3.2) Rectified voltage after the diode bridge.

Solving for the charging and discharging times respectively, we obtain

$$t_c = \frac{\cos^{-1}\left(\frac{V_{DC}^{min}}{\hat{V}_{DC}}\right)}{4\pi f_L} = \frac{\cos^{-1}\left(\frac{70V}{\sqrt{2} \cdot 85V}\right)}{4 \cdot \pi \cdot 50Hz} = 1.51ms,$$

$$t_d = \frac{1}{2f_L} - t_c = 8.49ms.$$

As a consequence, we have for the stored energy in the capacitor

$$E_C = \frac{2t_d f_L P_{out}}{\eta 2 f_L} = \frac{2 \cdot 8.49 \text{ms} \cdot 50 \text{Hz} \cdot 5.2 \text{W}}{0.75 \cdot 2 \cdot 50 \text{Hz}} = 58.86 \text{mJ} .$$

This energy, if we neglect the energy which is stored in the inductor, is equal to

$$E_C = \tfrac{1}{2}(C_{i1} + C_{i2})V^2 = \tfrac{1}{2}(C_{i1} + C_{i2})(V_{DC}^2 - V_{DC_{min}}^2),$$

which results in an input capacitance of

$$C_{i1} + C_{i2} = \frac{2E_C}{V_{DC}^2 - V_{DC_{min}}^2} = \frac{2 \cdot 58.86 \text{mJ}}{(\sqrt{2} \cdot 85 \text{V})^2 - 70 \text{V}^2} = 12.33 \mu\text{F} .$$

The other function of the input circuit is to suppress the disturbances which are produced by the triangular formed current shapes at switching frequency. One way to attenuate these disturbances, is to create a low pass filter, which is already present in the form of C_{i_1} and L_i . Taking the maximum current of the inductor in consideration and choosing components in regular series we find $C_{i_1} = 4.7 \mu\text{F}$ and $L_i = 820 \mu\text{H}$, resulting in a cut off frequency of 2564Hz, which is the lowest cut off frequency possible in this situation to have maximum attenuation at the switching frequency. The remaining capacitor, C_{i_2} , can be calculated and results in $7.6 \mu\text{F}$. This is a rather big capacitor and it is impossible to fit this casing size on our printed circuit board. The maximum input capacitance we can create, considering the printed circuit board space, is equal to $3.3 \mu\text{F} + 4.7 \mu\text{F} = 8 \mu\text{F}$, resulting in $V_{DC} = 28.22 \text{V}$ at $V_{AC} = 85 \text{V}$. This causes the converter to operate shortly in continuous mode at $V_{AC} = 85 \text{V}$, as shown in Fig. (3.3). The minimum input voltage to guarantee discontinuous mode is in our case $V_{AC} = 98.69 \text{V}$ in stead of $V_{AC} = 85 \text{V}$.
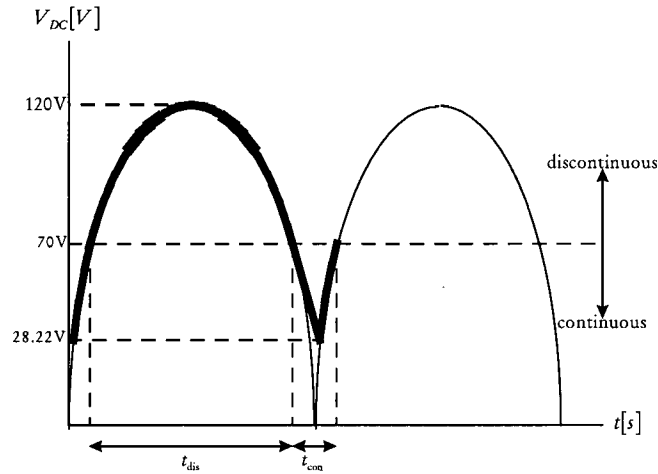
Fig. (3.3) The actual rectified input voltage

Resistor R_f is added to limit the inrush current to approximately 20A and can be calculated using Ohm's law

$$R_f = \frac{\hat{V}_{AC}^{max}}{I_{in}^{max}} = \frac{\sqrt{2} \cdot 265 \text{V}}{20 \text{A}} = 18.74 \Omega .$$

Choosing this resistor in regular series, we find $R_f = 18 \Omega$.

3.2 Transformer Design

The principle we use for dimensioning the flyback transformer is based on comparing the magnetic energy stored in the air gap of the flyback transformer during the on time of the MOSFet to the energy transferred to the output during the off time of the MOSFet [12]. The magnetic energy stored in the air gap of the primary inductance is equal to

$$E_m = \frac{1}{2} L_p I_p^2 .$$

The power, drawn from the output in discontinuous mode, is equal to

$$P_o = E_m f_s \eta = \frac{L_p I_p^2 f_s \eta}{2} . \tag{3.1}$$

In Eq. (3.1) η represents the efficiency of the transformer and the secondary circuit, f_s is the switching frequency and I_p the primary current. The primary peak current is calculated using the basic inductor equation $V = L \frac{di}{dt}$, which reads in our case

$$\hat{I}_p = \frac{1}{L_p} \int_0^{\delta_p T} V_{DC} dt = \frac{V_{DC} \delta_p T}{L_p} . \tag{3.2}$$

Solving for L_p by substitution of Eq. (3.2) in Eq. (3.1) results in

$$L_p = \frac{V_{DC}^2 \delta_p^2 \eta}{2 P_o f} . \tag{3.3}$$

The number of primary turns and the ratio between the primary and the secondary number of turns can be calculated invoking Maxwell's second law

$$V_{DC} = \oint E ds = N_P \frac{d}{dt} \iint_{A_e} B dA .$$

Since A_e is constant and B starts at zero, due to using half the B-H curve, this equation reduces to

$$V_{DC} \delta_p T = N_P B A_e .$$

Solving for the number of primary windings, N_p, we obtain

$$N_p = \frac{V_{DC} \delta_p T}{B A_e} .$$

For calculating the minimum number of primary windings we evaluate

$$N_{P_{min}} = \frac{V_{DC_{min}} \delta_{p_{max}}}{f_s B_{max} A_e} , \tag{3.4}$$

in which $\delta_{p_{max}}$ is the start up duty cycle of the VIPer20 and from the data-sheets we have $\delta_{p_{max}} = 0.13$.

From the ratio between the primary and secondary peak currents we have

$$\frac{\hat{I}_p}{\hat{I}_s} = N = \frac{\dfrac{V_{DC} \delta_p}{L_p}}{\dfrac{V_o \delta_s}{L_s}} = \frac{V_{DC} \delta_p}{V_o \delta_s N^2} ,$$

and with $\delta_p + \delta_s = 1$ at the minimum input voltage, this results in

$$N = \frac{V_{DC} \delta_p}{V_o (1 - \delta_p)} . \tag{3.5}$$

The losses in the VIPer20 are mainly switching losses and not conduction losses, in perticular at high input voltages. The losses in the secondary diode are mainly conduction losses and therefore it is recommendable to choose N as small as possible. Table (3.1) lists several different N values including the primary and secondary peak currents, which are calculated using Eqs. (3.2), (3.3) and (3.5).

N	δ_p	$L_p[\mu H]$	$\hat{I}_p[mA]$	$\hat{I}_s[mA]$
4	0.271	221	687	2747
5	0.317	303	586	2928
6	0.358	386	519	3116
7	0.393	458	476	3333
8	0.426	548	435	3484

Table (3.1) Possible transformer transfer ratios including the resulting L_p, $\hat{I}_p$ and $\hat{I}_s$

The maximum rated I_{ds} of the VIPer20 is 500mA resulting in $N = 7$.

From Eq. (3.5) we have $\delta_p = 0.39$ and $\delta_s = 0.61$. Now we are able to calculate the primary inductance, L_p, by using Eq. (3.3)

$$L_p = \frac{(70V)^2 \cdot 0.39^2 \cdot 0.8}{2 \cdot 5.2W \cdot 125 \cdot 10^3 Hz} = 458.64 \mu H.$$

The design of the transformer is based on a E13/6/6 transformer of which we use the physical dimensions in the next calculations. The parameters used in the calculations below are the effective area, $A_e = 20.2mm^2$ and the nominal winding width, $l_b = 6.5mm$. The minimum number of primary windings can be calculated using Eq. (3.4)

$$N_{P_{min}} = \frac{375V \cdot 0.13}{125kHz \cdot 375mT \cdot 20.2 \cdot 10^{-6} m^2} = 51.46.$$

Thin wire causes an increase of the copper losses in the transformer. On the other hand, thick wire expands the number of winding layers and results therefore in an increase of the proximity losses. Because of that, we aim at completely filled layers. From this we obtain $N_p = 60$, which results in, when using 0.16mm wire and a filling constant of 1.3, two filled layers of 30 windings. The number of secondary windings, N_s, can be calculated using

$$N_S = \frac{N_P}{N} = 8.57 \rightarrow 9.$$

Since $N_s = 9$ we can use 0.4mm triso wire to obtain one filled layer. Two benefits of triso wire are the galvanic isolation between the primary and secondary side of the transformer and the good coupling between the primary and the secondary layer. The bias winding, necessary for the power supply of VIPer20 is chosen with due observance of the next consideration. One requirement of the converter when operating in current mode is that the output voltage must be defined from 6.5V down to 3V. Since the output voltage V_o and the bias voltage V_b are directly coupled by the ratio of N_s and N_b we have

$$\frac{V_o^{min}}{V_b^{min}} = \frac{N_s}{N_b},$$

$$N_b = N_s \frac{V_b^{min}}{V_o^{min}} = 9 \cdot \frac{8.5V}{3V} = 25.5 \rightarrow 26.$$

Due to peak rectification in the bias circuit, we have chosen, after some experiments, $N_b = 20$. To more or less create a filled layer we have chosen 0.28mm² wire, which is rather thick in this case, but we use the bias winding as a shield between primary and secondary side.

The airgap in the core can be calculated by invoking Maxwell's first law

$$\oint Hdl = i_{circ}.$$

Since $\mu_{r_{3C85}} \gg 1$ we can make a approximation

$$\oint H dl = N_p I_p = \int_{l_F} \frac{B}{\mu_0 \mu_{r_{3C85}}} dl + \int_{l_g} \frac{B}{\mu_0} dl \approx \frac{B l_g}{\mu_0}.$$

Solving for the magnetic field, we obtain

$$B = \frac{N_p I_p \mu_0}{l_g}.$$

Using the relations $\phi = B N_p A_e$, $\phi = L_p I_p$ and after solving for l_g, we find

$$l_g = \frac{N_p^2 \mu_0 A_e}{L_p}.$$

Substitution of the known values results in

$$l_g = \frac{60^2 \cdot 4 \cdot \pi \cdot 10^{-7} \, \mathrm{Hm^{-1}} \cdot 20.2 \cdot 10^{-6} \, \mathrm{m^2}}{458.64 \, \mu \mathrm{H}} = 0.199 \mathrm{mm}.$$

The windings of the transformer are constructed as depicted in Fig. (3.4).

(a)   (b)
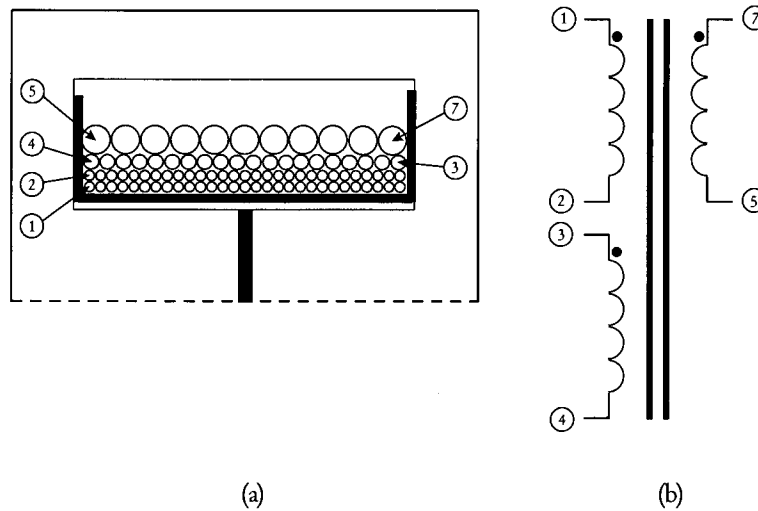
Fig. (3.4) (a) Layout of the transformer (b) Electrical connections

This layout [*Afstudeerverslag Patrick en Dion*] is chosen because of the EMI friendly behavior, since the voltage difference between the secondary and primary windings is minimal, due to the bias winding. Important is that the two grounds, points ③ and ⑦, are at the same side of the bobbin. Most ideal, but rather impractical for this transformer, is to choose $N_b = N_s$. The capacitance between primary and secondary , the so called crosstalk capacitance, is low, whenever this condition is met. The EMI behavior of this converter benefits from this effect, as will be shown in Chapter 6.

3.3 Design of the Output Filter

Normally the output filter is designed by taking the lifetime or maximum ripple current of the capacitor in consideration. This results usually in a rather big capacitor casing and since miniaturization is the aim, this is a disadvantage. If we had chosen for the traditional solution we needed a $470 \mu \mathrm{F}/25\mathrm{V}$ capacitor. Size $10.2 \mathrm{mm}\varnothing \mathrm{x}$ $13.5\mathrm{mm}$. A way to avoid this is using Ceramic Multilayer Capacitors because of the low Equivalent Series Resistance. A second step in miniaturization is building a higher order low-pass filter with smaller components in stead of a first order filter with a rather big capacitor. We used a π-section as depicted in Fig. (3.5).
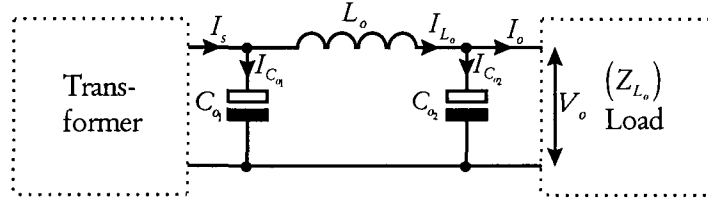
Fig. (3.5) Output filter.

Total size 4.3mm∅x14mm and two 1206 SMD capacitors, which can be placed on the bottom side of the printed circuit board under the inductor.

The voltage ripple superimposed on the DC output voltage must be less then $\pm 1\%$. Calculating this ripple can not be done straightforward using the complex calculation method as in basic network theory, since the secondary current is triangular shaped. As explained in Appendix A we can decompose this triangular shaped signal into it's harmonics, calculate the voltage ripple at the output for all the harmonics and after summation we find the total voltage ripple at the output.

In this system we can distinguish the next transfer functions

$$H_1(f) = \frac{I_s(f)}{I_{C_{o1}}(f)} = \frac{Z_{L_o}\left(Z_{C_{o2}} + Z_{L_o}\right) + Z_{C_{o2}} Z_{L_o}}{\left(Z_{C_{o1}} + Z_{L_o}\right)\left(Z_{C_2} + Z_{L_o}\right) + Z_{C_{o2}} Z_{L_o}},$$

$$H_2(f) = \frac{I_s(f)}{I_{L_o}(f)} = \frac{Z_{C_{o1}}\left(Z_{C_{o2}} + Z_{L_o}\right)}{\left(Z_{C_{o1}} + Z_{L_o}\right)\left(Z_{C_{o2}} + Z_{L_o}\right) + Z_{C_{o2}} Z_{L_o}},$$

$$H_3(f) = \frac{I_s(f)}{I_{C_{o2}}(f)} = \frac{Z_{C_{o1}} Z_{L_o}}{\left(Z_{C_{o1}} + Z_{L_o}\right)\left(Z_{C_{o2}} + Z_{L_o}\right) + Z_{C_{o2}} Z_{L_o}},$$

$$H_4(f) = \frac{I_s(f)}{I_o(f)} = \frac{Z_{C_{o1}} Z_{C_{o2}}}{\left(Z_{C_{o1}} + Z_{L_o}\right)\left(Z_{C_{o2}} + Z_{L_o}\right) + Z_{C_{o2}} Z_{L_o}},$$

$$H_5(f) = \frac{I_s(f)}{V_o(f)} = H_4(f) Z_{L_o}.$$

Solving $I_{C_{o1}}(t)$ by substitution and transforming the result back to time domain yields

$$I_{C_{o1}}(t) = a_0^s \left|H_1(f)\right| + \sum_{n=1}^m \left|H_1(f)\right| a_n^s \cos\left(\frac{2\pi nt}{T} + \arg(H_1(f))\right) + \left|H_1(f)\right| b_n^s \sin\left(\frac{2\pi nt}{T} + \arg(H_1(f))\right).$$

Using the same procedure we can calculate the remaining wave forms, $I_{L_o}(t)$, $I_{C_{o2}}(t)$, $I_o(t)$ and $V_o(t)$. We used the Ceramic Multilayer Capacitors of $22\mu F$ with an ESR of $200m\Omega$. By trial and error we found $L_o = 22\mu H$ with an ESR of 1Ω in order to obtain a output voltage ripple of less then $\pm 1\%$. We calculated the output voltage and current ripple with a resistive load of

$$R_L = \frac{(V_o^2)}{P_o} = \frac{(6.5V)^2}{5.2W} = 8.125\Omega.$$ The calculated output voltage and current are depicted in

Fig. (3.6).

(a)   (b)
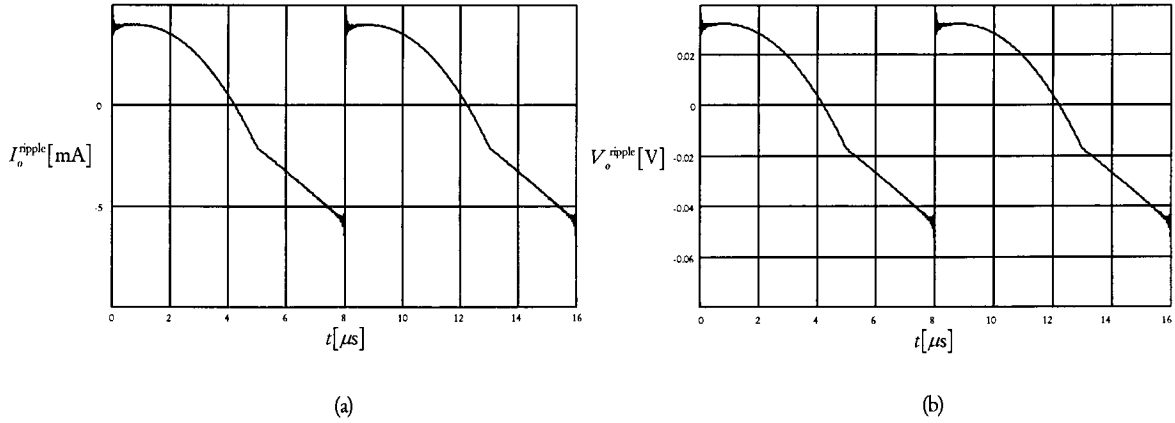
Fig. (3.6) (a) Output ripple current (b) Output ripple voltage (n = 150).

3.4 Design of the Voltage Regulation Circuitry

For the voltage regulation circuit we have made use of a programmable shunt regulator diode, which has the advantages to create a precision reference voltage, in order to guarantee the ±1% output voltage. The schematic used for the voltage regulation is depicted in Fig. (3.7).
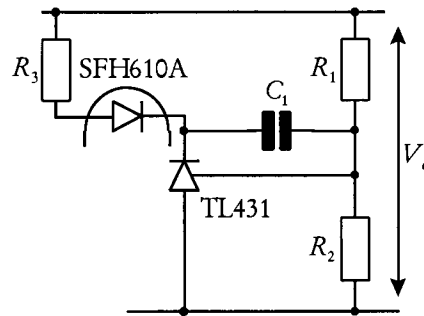
Fig. (3.7) Circuit of the voltage regulation circuitry.

This circuit is built around a typical application of the TL431, a precision voltage reference. The reference pin of the TL431 is internally fixed at precisely 2.5V. The voltage divider, consistent out of resistor R_1 and R_2 should fulfill this condition, when $V_o = 6.5V$. From this we have

$$V_r = V_o \frac{R_2}{R_1 + R_2},$$

$$R_1 = R_2 \left(\frac{V_0}{V_r} - 1 \right),$$

in which we choose $R_2 = 10k\Omega$, which results in $R_1 = 16k\Omega$. The current in these resistors is

$$I = \frac{V_o}{R_1 + R_2} = \frac{6.5V}{16k\Omega + 10k\Omega} = 250\mu A,$$

which is much more then the reference input current of $4\mu A$. In other words, the reference input current will hardly influence the voltage divider. Capacitor C_1 will be explained in Chapter 4.

Since the tolerance in the output voltage is limited to ±1%, we calculate the tolerance in the output voltage given the tolerances of the components used in Fig. (3.7). From the same figure we have

$$V_o = V_r \frac{R_1 + R_2}{R_2}.$$

We expect the tolerance to increase linear from it's minimum to it's maximum and therefore we can write for the absolute tolerance in the output voltage

$$\left|\frac{\Delta V_o}{V_o}\right| = \left|\frac{1}{V_o}\right|\left(\left|\frac{\partial V_o}{\partial V_r}\right||\Delta V_r| + \left|\frac{\partial V_o}{\partial R_1}\right||\Delta R_1| + \left|\frac{\partial V_o}{\partial R_2}\right||\Delta R_2|\right) = \left|\frac{1}{V_o}\right|\left(\frac{R_1 + R_2}{R_2}|\Delta V_r| + \frac{V_r}{R_2}|\Delta R_1| + \frac{V_r R_1}{R_2^2}|\Delta R_2|\right)$$

$$= \left|\frac{1}{6.5V}\right|\left(2.5V|\Delta V_r| + 2.5\cdot10^{-4}\,\text{A}|\Delta R_1| + 4\cdot10^{-4}\,\text{A}|\Delta R_2|\right).$$

Substituting $\Delta V_r = 10\text{mV}$, $\Delta R_1 = 800\Omega$ and $\Delta R_2 = 500\Omega$ results in $\dfrac{\Delta V_o}{V_o} = 6.54\%$, which is not

surprisingly since we are using 5% resistors. Using 1% resistors we have $\dfrac{\Delta V_o}{V_o} = 1.62\%$ and using

0.1% resistors we have $\dfrac{\Delta V_o}{V_o} = 0.51\%$ which is within the specifications. We will use the resistors

which are available at EPM causing, due to 5% tolerance, an error in the output voltage of at most ±6.54%, which is equal to ±425mV.

3.5 Design of the Current Regulation Circuitry

Since we are aiming at minimum losses in the converter, it is appreciable to reduce the losses in the resistors. Especially the current sense resistor is normally dissipating a lot. See Fig. (3.8 a) for a conventional setup.
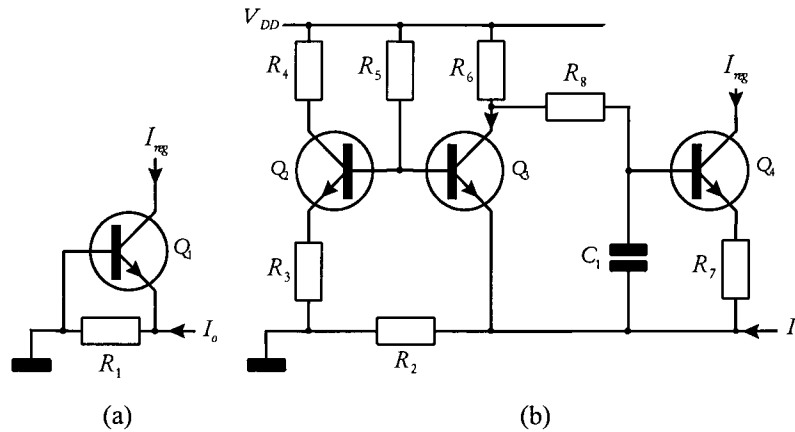
Fig. (3.8) (a) Conventional current measuring circuit (b) Current measuring circuit with minimalised losses.

From this figure we have for the current sense resistor losses $P_L = I_O R_1$. When using a BC848C transistor for Q_1, the bases-emitter-voltage needs to be approximately 650mV to turn the transistor in a on state. The current regulation must be activated at $I_o = 800\text{mA}$. Using this we can calculate the value of R_1, and obtain $R_1 = 812\text{m}\Omega$. The resulting losses in the resistor are $I_O^2 R_1 = 520\text{mW}$. Reducing these losses can be accomplished by having a closer look at the $V_{be} - I_c$ curve of a transistor, of which an example is given in Fig. (3.9).
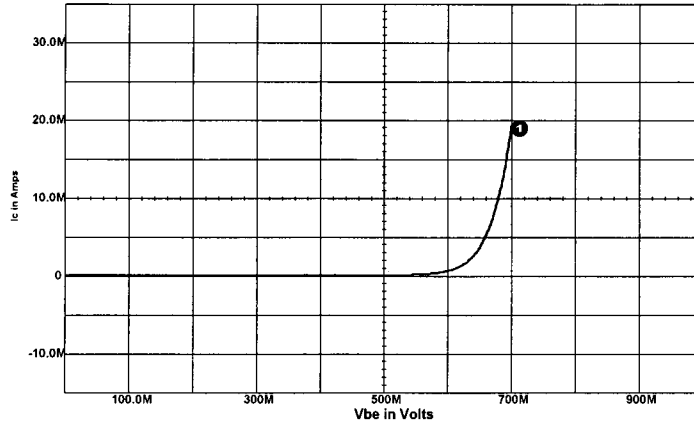
Fig. (3.9) V_{be} versus I_C curve of the BC848C transistor.

Up till 550mV, the collector current hardly changes due to a change in the base-emitter voltage. A voltage drop of 550mV across the current sense resistor R_1 does not contribute to an increase in the collector current, but does generate losses in the resistor. A way to avoid this is creating an offset voltage of 550mV in series with the base-emitter. The current sense resistor now only adds a small voltage to increase the collector current. This means that the resistor value of the current sense resistor can be chosen smaller, and as a consequence the losses reduce.

This offset voltage idea can be used the other way around as depicted in Fig. (3.8.b). Transistor Q_2 is operating in saturation, in order to create a constant current source. This to create a defined voltage across R_3 and $V_{be_{Q_3}}$, which is just enough to turn a BC848C in an on state. The current sense resistor now decreases the $V_{be_{Q_3}}$ to turn Q_3 in a nearly off state. From this circuit we have

$$I_{e_{Q_2}} R_3 + V_{be_{Q_3}} = \left(I_O + I_{e_{Q_3}} \right) R_2 + V_{be_{Q_2}} . \tag{3.6}$$

Solving Eq. (3.6) for $V_{be_{Q_3}}$ yields

$$V_{be_{Q_3}} = I_{e_{Q_2}} R_3 + V_{be_{Q_2}} - \left(I_O + I_{e_{Q_3}} \right) R_2 .$$

Transistor Q_3 is in the on state when $I_O < 800\text{mA}$ and in an off state when $I_O \geq 800\text{mA}$. We can choose an operating point at $I_o = 800\text{mA}$, at which the emitter voltages are chosen equal resulting in $V_{e_{Q_2}} = V_{e_{Q_3}} = I_o R_2 = 800\text{mA} \cdot 0.1\Omega = 80\text{mV}$ (Q_2 and Q_3 have the same V_e voltage at this point). Since the bases of the transistors are connected, we have, with neglecting $I_{e_{Q_3}}$,

$$\frac{I_{e_{Q_2}}}{I_{e_{Q_3}} + I_O} \approx \frac{I_{e_{Q_2}}}{I_O} = \frac{R_2}{R_3} . \tag{3.7}$$

Applying Kirchhoff's current law to Q_2, results in after neglecting the base current,

$$\frac{V_{DD} - V_{e_{Q_2}} - V_{ce(sat)}}{R_4} = \frac{V_{e_{Q_2}}}{R_3} = I_O \frac{R_2}{R_3} . \tag{3.8}$$

Since Q_2 is operating in saturation we have

$$V_{b_{Q_2}} = 500\text{mV} + I_o R_2 = V_{DD} - \frac{I_{e_{Q_2}}}{\beta_{SAT}} R_5 . \tag{3.9}$$

Solving Eq. (3.6), Eq. (3.8) and (3.9) after taking $R_2 = 0.1\Omega$, $R_3 = 120\Omega$ and $\beta_{SAT} = 8.33$, results in $R_4 = 3.48\text{k}\Omega$ and $R_5 = 24\text{k}\Omega$. Low-pass filter R_8 / C_1 is added for gain correction at higher frequencies and will explained in Chapter 4.

Transistor Q_4 is added because the signal I_{reg} is inverted. In this configuration Q_3 is forced to operate in saturation mode if $I_O < 800\text{mA}$, since Q_4 is off. We limit the $I_{e_{Q_3}}$ to 2mA by choosing R_6

$$R_6 = \frac{V_{DD} - V_{be4}}{I_{c3}} = \frac{2.5\text{V} - 0.5\text{V}}{2\text{mA}} = 1\text{k}\Omega.$$

We used ICAPS/4 to run a simulation of the current control circuit at three ambient temperatures, $T_{amb} = 27°\text{C}$, $T_{amb} = -5°\text{C}$ and $T_{amb} = 85°\text{C}$, to verify the proper working of the circuit. The results are depicted in .Fig. (3.10)

(a)   (b)
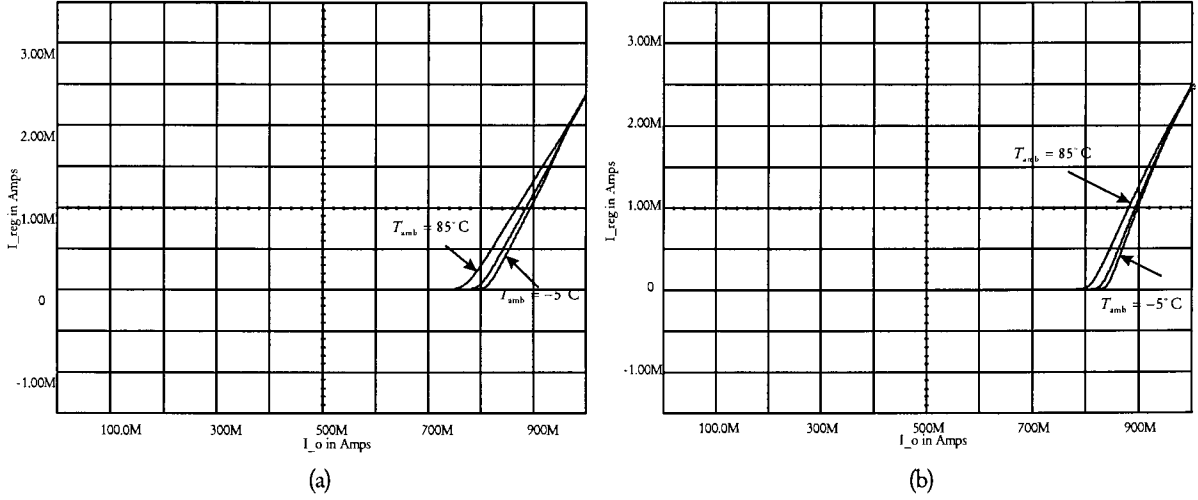
Fig. (3.10) Simulation results of the current control circuit, (a) $V_o = 3V$ (b) $V_o = 6.5V$

3.6 Design of the Frequency Control Circuitry

One disadvantage of the VIPer20 is the minimum on time, which is limited to $0.3\mu s$. This limit results in a restriction for the switching frequency and the primary duty cycle

$$\delta_p \frac{1}{f_s} \geq 0.3\mu s \rightarrow f_s \leq 3.33 \cdot 10^6 \delta_p \text{Hz}. \tag{3.10}$$

Consider the next two situations

$$\delta_p^{\max} = \sqrt{\frac{2L_p P_o^{\max} f_s}{\left(V_{DC}^{\min}\right)^2 \eta}} = \sqrt{\frac{2 \cdot 458.64\mu H \cdot 5.2W \cdot 125kHz}{\left(70V\right)^2 \cdot 0.8}} = 0.39 \rightarrow \delta_p \frac{1}{f_s} = 3.12\mu s,$$

$$\delta_p^{\min} = \sqrt{\frac{2L_p P_o^{\min} f_s}{\left(V_{DC}^{\max}\right)^2 \eta}} = \sqrt{\frac{2 \cdot 458.64\mu H \cdot 325mW \cdot 125kHz}{\left(375V\right)^2 \cdot 0.8}} = 0.02 \rightarrow \delta_p \frac{1}{f_s} = 0.16\mu s.$$

The power supply will operate in burst mode at minimum load and maximum input voltage. A way to avoid this problem is to make the switching frequency a function of the input voltage and the output load, resulting in a mechanism which reduces the switching frequency whenever the primary on time becomes too small. The maximum switching frequency is

$$f_s^{\max} = \frac{\left(V_{DC}^{\min}\right)^2 \left(\delta_p^{\max}\right)^2 \eta}{2P_o^{\max} L_p} = \frac{\left(70V\right)^2 \cdot 0.39^2 \cdot 0.8}{2 \cdot 5.2W \cdot 458.64\mu H} = 125kHz.$$

The minimum primary duty cycle can be calculated using Eq. (3.10)

$$L_p = \frac{\left(V_{DC}^{max}\right)^2 \delta_p \eta}{2P_o^{min}\left(3.33 \cdot 10^6 \delta_p\right)} = 458.64\,\mu H = \frac{(375V)^2 \cdot \delta_p \cdot 0.8}{2 \cdot 235mW \cdot \left(3.33 \cdot 10^6 \cdot \delta_p\right)} \rightarrow \delta_p = 0.088,$$

which results in a minimum switching frequency of $f_s = 3.33 \cdot 10^6 \delta_p = 29.38\text{kHz}$.

The internal oscillator of the VIPer20 and the external components are depicted in Fig. (3.11).
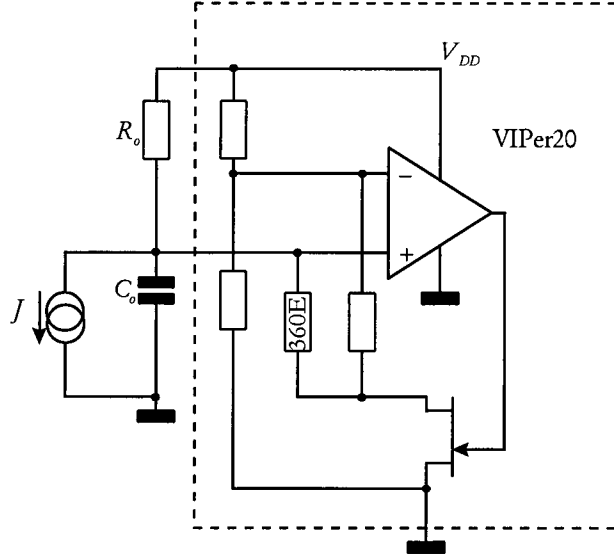
Fig. (3.11) The oscillator of the VIPer20 and external components

This oscillator is based on charging and discharging capacitor C_o between it's two threshold voltages, oscillator valley (V_{osc}^{valley}) and oscillator peak voltage (V_{osc}^{peak}). From the data sheets we have $V_{osc}^{valley} = 3.7V$ and $V_{osc}^{peak} = 7.1V$. The current source J is not standard, but an extension of the oscillator to control the frequency externally. In the calculations below R_D is the 360Ω resistor. We will first derive the oscillator frequency as function of the current J. During charging of the capacitor C_o the system is governed by the next first order differential equation

$$\frac{V_{DD} - V_{C_o}}{R_o} + J + C_o \frac{d\left(-V_{C_o}\right)}{dt} = 0,$$

(3.11)

$$R_o C_o \frac{dV_{C_o}}{dt} + V_{C_o} = R_o J + V_{DD}.$$

Solving Eq. (3.11) for the capacitor voltage V_{C_o} and after substitution of the boundary conditions

$V_{C_o}\big|_{t=t_0} = 3.7V$ and $V_{C_o}\big|_{t=t_1} = 7.1V$ in the general solution, we find for the capacitor voltage

$$V_{C_o}^{(1)}(t) = \left(3.7 - V_{DD} - R_o J\right)e^{-\frac{t}{R_o C_o}} + V_{DD} + R_o J,$$

and for the time $t = t_1$

$$t_1(V_{DD}, J) = R_o C_o \ln\left(\frac{3.7 - V_{DD} - R_o J}{7.1 - V_{DD} - R_o J}\right).$$

During discharging of capacitor C_o the system is governed by the next first order differential equation

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$$\frac{V_{DD} - V_{C_o}}{R_o} + J + \frac{V_{C_o}}{R_D} + C_o \frac{d(-V_{C_o})}{dt},$$

$$\frac{R_D R_o C_o}{R_D + R_o} \frac{dV_{C_o}}{dt} + V_{C_o} = \frac{R_D}{R_D + R_o} V_{DD} + \frac{R_D R_o}{R_D + R_o} J. \tag{3.12}$$

Solving Eq. (3.12) for the capacitor voltage V_{C_o} and after substitution of the boundary conditions $V_{C_o}\big|_{t=t_1} = 7.1\text{V}$ and $V_{C_o}\big|_{t=t_2} = 3.7\text{V}$ in the general solution, we find for the capacitor voltage

$$V_{C_o}^{(2)}(t) = \left(7.1 - \frac{R_D}{R_D + R_o} V_{DD} - \frac{R_D R_o}{R_D + R_o} J\right) e^{-\frac{R_D + R_o}{R_D R_o C_o} t} + \frac{R_D}{R_D + R_o} V_{DD} + \frac{R_D R_o}{R_D + R_o} J,$$

and for the time $t = t_2$

$$t_2(V_{DD}, J) = \frac{R_D R_o C_o}{R_D + R_o} \ln\left(\frac{7.1 - \dfrac{R_D}{R_D + R_o} V_{DD} - \dfrac{R_D R_o}{R_D + R_o} J}{3.7 - \dfrac{R_D}{R_D + R_o} V_{DD} - \dfrac{R_D R_o}{R_D + R_o} J}\right).$$

By definition is the switching frequency equal to

$$f_s(V_{DD}, J) = \frac{1}{t_1(V_{DD}, J) + t_2(V_{DD}, J)}.$$

A plot of the switching frequency as function of the current J and $V_{DD} = 13\text{V}$, $R_o = 3.1\text{k}\Omega$, $C_o = 4.7\text{nF}$ is given in Fig. (3.12).
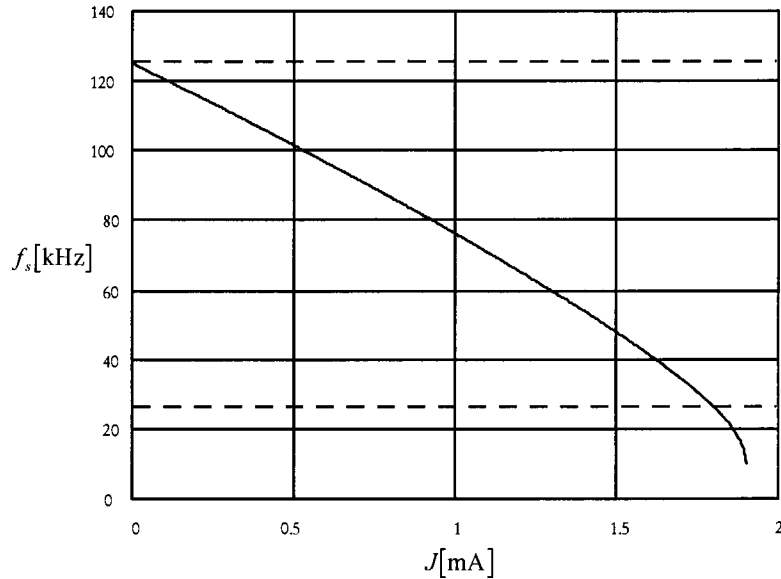
Fig. (3.12) The switching frequency versus the control current J at $V_{DD} = 13\text{V}$.

The dotted lines are presenting the minimum and maximum switching frequency.

The voltage V_{amp} is joined with the duty cycle δ_p as $0.5\text{V} \le V_{amp} \le 2.5\text{V} \rightarrow 0.05 \le \delta_p \le 0.39$.
Because of this the current source J will be implemented as a voltage controlled current source which joins the voltage V_{amp} and the current J as $0.5\text{V} \le V_{comp} \le 2.5\text{V} \rightarrow 1.6\text{mA} \ge J \ge 0\text{mA}$.
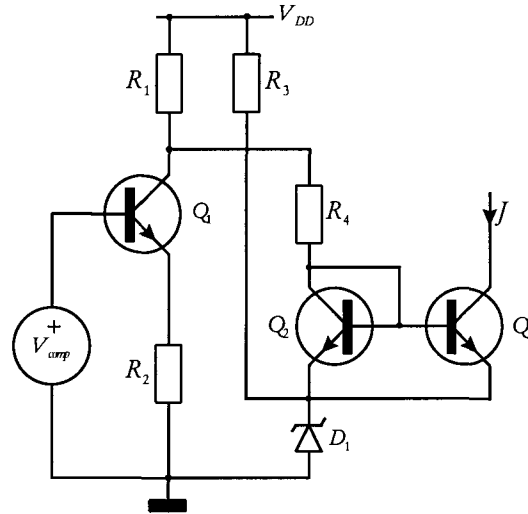
Fig. (3.13) Voltage controlled current source used in frequency control

The voltage regulator diode, D_1, is added to prevent Q_1 from saturating. At $J = 0\text{mA}$ the collector voltage of Q_1 could become approximately 700mV, which causes Q_1 to saturate. The diode is chosen 3V because of the oscillator valley voltage of 3.1V. Otherwise Q_3 would saturate. Because of the diode , the minimum collector voltage of Q_1 is 3V, which is more than the maximum base voltage of 2.5V. We will now derive a relationship between the current J and the input voltage V_{amp}. The output current is equal to

$$J = \frac{V_{C_{Q_1}} - V_{C_{Q_2}}}{R_4} = \frac{V_{C_{Q_1}} - \left(V_{D_1} + V_{be_{Q_2}}\right)}{R_4} = \frac{V_{DD} - I_{c_{Q_1}}R_1 - JR_1 - \left(V_{D_1} + V_{be_{Q_2}}\right)}{R_4}.$$

If we neglect the base current of transistor Q_1 and therefore assume $I_{c_{Q_1}} = I_{e_{Q_1}}$ we find

$$J = -V_{amp}\frac{R_1}{R_1 R_2 + R_2 R_4} + \frac{V_{DD}}{R_1 + R_4} + \frac{V_{be_{Q_1}}R_1}{R_1 R_2 + R_2 R_4} - \frac{V_{D_1} + V_{be_{Q_2}}}{R_1 + R_4}, \tag{3.13}$$

and

$$\left|\frac{\Delta J}{\Delta V_{amp}}\right| = \frac{R_1}{R_1 R_2 + R_2 R_4}, \tag{3.14}$$

and as a consequence

$$R_4 = \frac{\left(V_{be_{Q_1}} - V_{amp} + V_{DD} - V_{D_1} - V_{be_{Q_2}}\right)\left(1 - \left|\frac{\Delta J}{\Delta V_{amp}}\right|R_2\right)}{J},$$

From Eqs. (3.13) and (3.14) we find by substitution of $V_{DD} = 13\text{V}$, $V_{be_{Q_1}} = V_{be_{Q_2}} = 700\text{mV}$ and $V_{D_1} = 3\text{V}$ for the resistors $R_1 = 4.8\text{k}\Omega$, $R_2 = 1\text{k}\Omega$ and $R_4 = 1.2\text{k}\Omega$.

We might seem to have a problem with this solution for the current source, since it is very dependend of the supply voltage V_{DD}. However, V_{DD} is directly coupled to V_o and therefore constant whenever the converter is operating in voltage mode. Is the converter operating in current mode, then V_o will decrease and as a consequence V_{DD} will also decrease. Because of this, the current source will sink less current from the oscillator causing the switching frequency to increase. This is not a problem for the minimum primary on time $T_{on} = 0.3\mu s$. The minimum load in current mode is $P_o = V_o^{\min}I_o = 3\text{V} \cdot 800\text{mA} = 2.4\text{W}$. In this situation $V_{DD} = 8.5\text{V}$ resulting the

current source to sink 0.95mA. The switching frequency versus the shunted current is shown in Fig. (3.12) and is at 0.95mA equal to 75kHz. The minimum duty cycle will be reached at maximum input voltage and is equal to

$$\delta_p^{\min} = \sqrt{\frac{2L_p P_o^{\min} f_s}{\left(V_{DC}^{\max}\right)^2 \eta}} = \sqrt{\frac{2 \cdot 458.64\mu\text{H} \cdot 2.4\text{W} \cdot 75\text{kHz}}{\left(375\text{V}\right)^2 \cdot 0.8}} = 0.038 \rightarrow \delta_p \frac{1}{f_s} = 0.51\mu s \,.$$

Even in a situation when the current source is not working at all we have

$$\delta_p^{\min} = \sqrt{\frac{2L_p P_o^{\min} f_s^{\max}}{\left(V_{DC}^{\max}\right)^2 \eta}} = \sqrt{\frac{2 \cdot 458.64\mu\text{H} \cdot 2.4\text{W} \cdot 125\text{kHz}}{\left(375\text{V}\right)^2 \cdot 0.8}} = 0.049 \rightarrow \delta_p \frac{1}{f_s} = 0.40\mu s \,,$$

which is more than the minimum on time.

We used ICAPS/4 to simulate the current source at three ambient temperatures, $T_{amb} = 27°\text{C}$, $T_{amb} = -5°\text{C}$ and $T_{amb} = 85°\text{C}$, to verify the proper working of the circuit. A graph of the voltage V_{comp} versus the current J is given in Fig. (3.14).
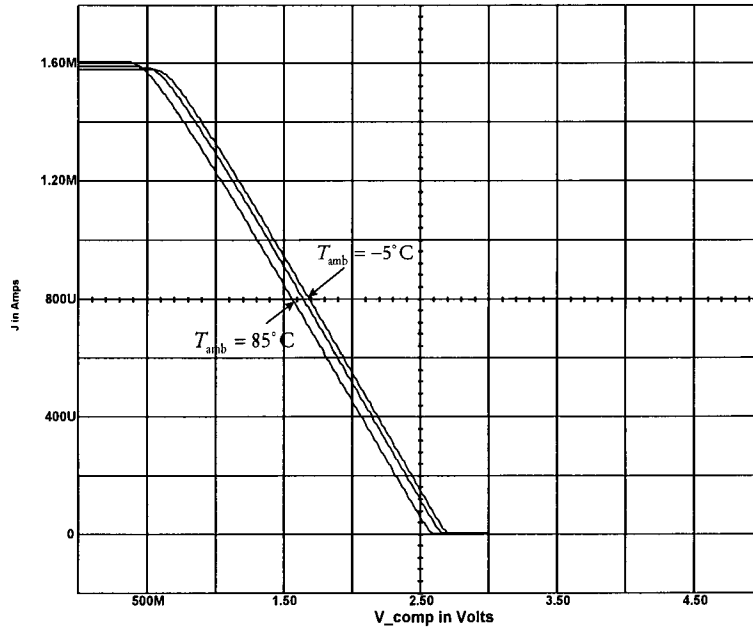
Fig. (3.14) Results of the simulations of the voltage controlled current source.

3.7 Design of the Bias Voltage Regulation

As pointed out in the paragraph of the transformer design, we have chosen $\dfrac{N_b}{N_s} = 2.22$, to guarantee a minimum output voltage of 3V. This results in a guaranteed bias voltage of minimal 8.5V. However the maximum bias voltage is in the ideal case $V_b^{\max} = 2.22 \cdot 6.5\text{V} = 14.43\text{V}$, but with peak rectification 18V. The VIPer20 will work in primary sense mode if $12.5\text{V} \le V_{DD} \le 13\text{V}$ and will shut down if $V_D \ge 13V$. A solution is to reduce the voltage with a linear regulator as depicted in Fig. (3.15).
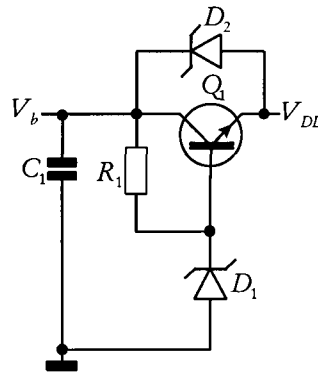
Fig. (3.15) Linear regulation circuit used in the bias circuit.

As pointed out V_{DD} must be below 12.5V for secondary sensing. If we choose the voltage regulator diode voltage 13V then $V_{DD} = V_{D_1} - V_{be_{Q_1}} = 13V - 0.7V = 12.3V$. The resistor is added to limit the current in the voltage regulator diode and is equal to

$$R_1 = \frac{V_b^{max} - V_{D_1}}{I_{D_1}} = \frac{18V - 13V}{1mA} = 5k\Omega.$$

We have chosen the current rather low to decrease the losses in the resistor. No problem occurs if $V_b \leq V_{D_1}$, because the transistor will work as an ordinary diode and $V_{DD} = V_b - 0.7V$. Diode D_2 is added to charge the capacitor during the startup using the high voltage current source of the VIPer20.

A disadvantage of this method is that we disable the overvoltage protection of the VIPer20. One way to overcome this problem is using voltage regulator diode D_2 as depicted in Fig. (3.15). If the collector voltage of the transistor increases beyond 20V then a fault has appeared and the power supply should be shut down. For example if the opto coupler is not functioning. Choosing $D_2 = 7V$ will force the power supply to shut down if the collector voltage is 20V, because the VIPer20 will shut down if $V_{DD} \geq 13V$.

3.8 Printed Circuit Board Design

The printed circuit board is designed by taking safety rules in consideration. We have kept 6mm creep distance between the "hot" and "cold" side of the battery charger and 3mm creep distance between the fused and the net side of the battery charger. From an EMI point of view we have kept the electrical loops as small as possible. The final printed circuit board is depicted in Fig. (3.16).

Primary power path at switching frequency

Secondary power path at switching frequency

(a)   *(b)*

Fig. (3.16) The (a) bottom and (b) the top side of the printed circuit board

We used a bi-layer printed circuit board to decrease the capacitive coupling with the environment. This was necessary since the drain is electrically connected with the PowerSO-10 casing.
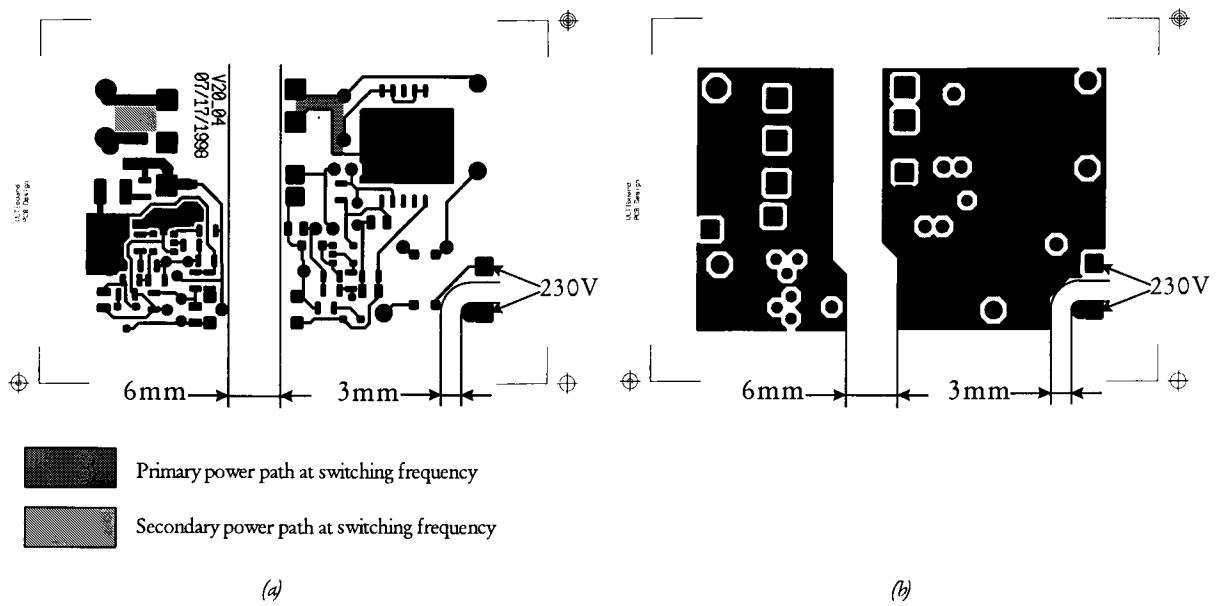
4. Control Loop Calculations and Measurements

In order to predict the behaviour of the converter in voltage and current mode regulation, we have computed the Bode plots of the open loop transfer function, which are needed to determine stability. To do so, we need a small signal (AC) model of the converter in each working mode (voltage or current regulation). These models will be derived using the State-Space Averaging Method and simple network analysis. We will first give some theoretical background information concerning the used stability margins. Then the needed transfer functions will be calculated and analysed. Afterwards we will measure the transfer functions with a gain/phase analyser to verify the calculated transfer functions.

4.1 Stability Margins

Most power supplies behave roughly similar to that of the system which is depicted in Fig. (4.1.a).
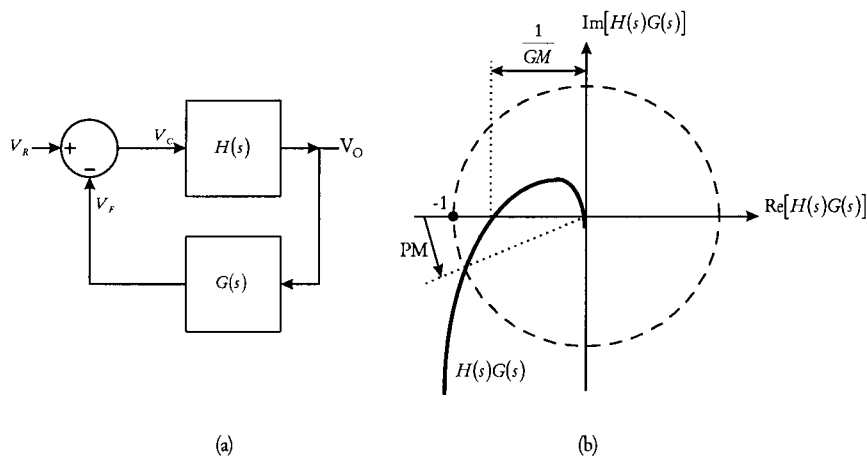
Fig. (4.1) (a) A typical controlled system (b) Nyquist plot for defining gain margin (GM) and phase margin (PM).

The closed loop transfer function of this system is

$$\frac{V_O(s)}{V_R(s)} = \frac{H(s)}{1 + G(s)H(s)}.$$ (4.1)

The open loop transfer function can be measured by injecting a test signal into the closed loop of a system as depicted in Fig. (4.1.a). We can use the closed loop to predict the stability of the system. For systems which can be described by Eq. (4.1) this can be done by making use of the argument principle [8]. From Eq. (4.1) we find that the closed loop roots are solutions of $1 + G(s)H(s) = 0$. Therefore we are interested in the Nyquist plot of $H(s)G(s)$ near -1 on the real axis, since the plot is not allowed to encircle this point in a clockwise or counterclockwise direction for a stable system. This as a direct result of the argument principle and the fact that poles and zeros are not allowed in the right half plane. Clockwise encircling indicates a zero in the right half plane and counterclockwise encircling indicates a pole in the right half plane. From this we can define a phase margin and a gain margin as depicted in Fig. (4.1.b). These definitions can also be used in Bode plots of $H(s)G(s)$ and are stated as,

> GAIN MARGIN (GM) is the factor by which the gain is less than the neutral stability value,
> PHASE MARGIN (PM) is the amount by which the phase of $H(s)G(s)$ exceeds -180° when $|H(s)G(s)| = 1$.

This results in simple restrictions to the Bode plots of $H(s)G(s)$ in order to guarantee system stability.

4.2 The State-Space Averaging Method applied to a Flyback Converter with CLC output Filter

The use of the State-Space Averaging Method as will be presented here is taken from [*Barzegar, F, et al*].

4.2.1 Equivalent Steady-State (DC) Model and Dynamic (AC) Small Signal Model

The equivalent circuit models for the power path of a flyback converter in discontinuous mode are presented in Fig. (4.2).

(a)

(c)

(b)

(d)
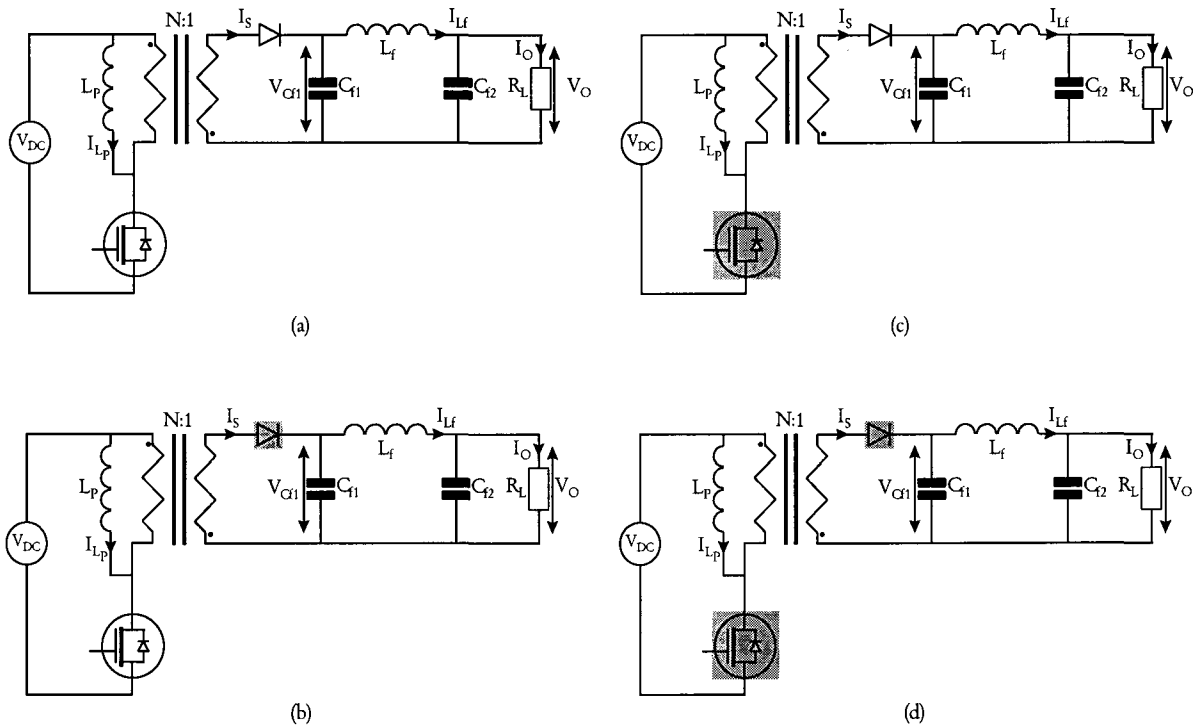
Fig. (4.2) The equivalent circuit models for the power path of a flyback converter in discontinuous mode.

Fig. (4.2.a) shows the complete circuit of the flyback converter as used. In the remaining figures striped components denote components in "off" state, representing the situations in the stages $0 < t \leq \delta_1 T$, $\delta_1 T < t \leq \delta_2 T$ and $\delta_2 T < t \leq T$ respectively. Several simplifications are made in this model to make a pencil and paper calculation possible. The first simplification is the absence of ESR in the output capacitors and the inductor. This is allowed, since we are using Ceramic Multilayer Capacitors, which have an ESR of only $200\text{m}\Omega$. The series resistance of the inductor is not this low, but for simplicity neglected. The second simplification is the absence of parasitic components like the resistance and inductance of the printed circuit board traces. In this system the state-space vector $\mathbf{x}(t)$, which contains the state variables of the system, and the source vector $\mathbf{u}(t)$ are defined according to

$$\mathbf{x}(t) = \begin{pmatrix} I_{L_p}(t) \\ I_{L_f}(t) \\ V_{C_{f1}}(t) \\ V_o(t) \end{pmatrix}, \qquad \mathbf{u}(t) = V_{DC}.$$

The next step in the state-space averaging method is to define the system equations in three stages, since the converter is working in discontinuous mode. For stage one, $0 < t \le \delta_1 T$, the next set of equations is governing the state variables

$$L_p \frac{dI_p}{dt} = V_{DC},$$

$$L_f \frac{dI_{L_f}}{dt} = V_{C_{f1}} - V_o,$$

$$C_{f1} \frac{dV_{C_{f1}}}{dt} = I_{L_f},$$

$$C_{f2} \frac{dV_0}{dt} = I_{L_f} - \frac{V_o}{R_L},$$

or written in matrix form ,

$$\dot{\mathbf{x}}(t) = \mathbf{A}_1 \mathbf{x}(t) + \mathbf{B}_1 \mathbf{u}(t) = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_f} & -\frac{1}{L_f} \\ 0 & \frac{1}{C_{f1}} & 0 & 0 \\ 0 & \frac{1}{C_{f2}} & 0 & -\frac{1}{C_{f2}R_L} \end{pmatrix} \mathbf{x}(t) + \begin{pmatrix} \frac{1}{L_p} \\ 0 \\ 0 \\ 0 \end{pmatrix} \mathbf{u}(t). \tag{4.2}$$

For the second stage , $\delta_1 T < t \le \delta_2 T$, the next set of equations is governing the state variables,

$$L_p \frac{dI_p}{dt} = -NV_{DC},$$

$$L_f \frac{dI_{L_f}}{dt} = V_{C_{f1}} - V_o,$$

$$C_{f1} \frac{dV_{C_{f1}}}{dt} = NI_p - I_{L_f},$$

$$C_{f2} \frac{dV_0}{dt} = I_{L_f} - \frac{V_o}{R_L},$$

or written in matrix form ,

$$\dot{x}(t) = A_1 x(t) + B_1 u(t) = \begin{pmatrix} 0 & 0 & -\dfrac{N}{L_p} & 0 \\ 0 & 0 & \dfrac{1}{L_f} & -\dfrac{1}{L_f} \\ \dfrac{N}{C_{f1}} & -\dfrac{1}{C_{f1}} & 0 & 0 \\ 0 & \dfrac{1}{C_{f2}} & 0 & -\dfrac{1}{C_{f2}R_L} \end{pmatrix} x(t) + \begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \end{pmatrix} u(t). \tag{4.3}$$

For the last stage, $\delta_2 T < t \le T$, the next set of equations is governing the state variables,

$$L_p \frac{dI_p}{dt} = 0,$$

$$L_f \frac{dI_{L_f}}{dt} = V_{C_{f1}} - V_o,$$

$$C_{f1} \frac{dV_{C_{f1}}}{dt} = I_{L_f},$$

$$C_{f2} \frac{dV_0}{dt} = I_{L_f} - \frac{V_o}{R_L},$$

or written in matrix form ,

$$\dot{x}(t) = A_1 x(t) + B_1 u(t) = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \dfrac{1}{L_f} & -\dfrac{1}{L_f} \\ 0 & \dfrac{1}{C_{f1}} & 0 & 0 \\ 0 & \dfrac{1}{C_{f2}} & 0 & -\dfrac{1}{C_{f2}R_L} \end{pmatrix} x(t) + \begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \end{pmatrix} u(t). \tag{4.4}$$

Since the derivatives are taken along linear ramp slopes, we can replace the derivatives by differences without creating any computational rounding errors. Applying this to Eq. (4.2) to Eq. (4.4) yields

$$\frac{x(\delta_1 T) - x(0)}{\delta_1 T} = A_1 x(t) + B_1 u(t),$$

$$\frac{x(\delta_2 T) - x(\delta_1 T)}{\delta_2 T} = A_2 x(t) + B_2 u(t),$$

$$\frac{x(T) - x(\delta_2 T)}{(1 - \delta_1 - \delta_2)T} = A_3 x(t) + B_3 u(t).$$

Elimination of the $x(\delta_1 T)$ and $x(\delta_2 T)$ terms by substitution results in

$$\dot{x}(t) = Ax(t) + Bu(t) = \left(\delta_1 A_1 + \delta_2 A_2 + (1 - \delta_1 - \delta_2)A_3\right)x(t) + \left(\delta_1 B_1 + \delta_2 B_2 + (1 - \delta_1 - \delta_2)B_3\right)u(t).$$

$$\tag{4.5}$$

Rewriting this result in matrix form and using the relation $\delta_2 = (\delta_1 V_{DC})/(NV_O)$, which can be derived for a flyback converter in discontinuous mode, we obtain

$$\dot{x}(t) = \begin{pmatrix} 0 & 0 & -\dfrac{V_{DC}\delta_1}{L_p V_o} & 0 \\[2ex] 0 & 0 & \dfrac{1}{L_f} & -\dfrac{1}{L_f} \\[2ex] \dfrac{V_{DC}\delta_1}{C_{f1}V_o} & \dfrac{NV_o - V_i\delta_1}{C_{f1}NV_o} & -\dfrac{V_{DC}\delta_1}{C_{f1}NV_o} & 0 & 0 \\[2ex] 0 & \dfrac{1}{C_{f2}} & 0 & -\dfrac{1}{C_{f2}R_L} \end{pmatrix} x(t) + \begin{pmatrix} \dfrac{\delta_1}{L_p} \\[2ex] 0 \\[1ex] 0 \\[1ex] 0 \end{pmatrix} u(t).$$

We are now able to create disturbances in the input variables V_{DC}, δ_1 and x,

$$\begin{aligned} V_{DC} &= \bar{v}_{DC} + \tilde{v}_{DC}, \\ x &= \bar{x} + \tilde{x}, \\ \delta_1 &= \bar{\delta}_1 + \tilde{\delta}_1, \end{aligned} \tag{4.6}$$

in order to derive a steady-state (DC) model and a dynamic (AC) model. Substitution of Eq. (4.6) in Eq. (4.5) results in

$$\dot{\bar{x}} + \dot{\tilde{x}} = \left(A_2\left(\bar{\delta}_1 + \tilde{\delta}_1\right)\frac{\bar{v}_{DC}}{NV_0} + A_3\left(1 - \bar{\delta}_1\frac{\bar{v}_{DC}}{NV_0} - \tilde{\delta}_1\frac{\bar{v}_{DC}}{NV_0}\right)\right)(\bar{x} + \tilde{x}) + B_1\left(\bar{\delta}_1 + \tilde{\delta}_1\right)\left(\bar{v}_{DC} + \tilde{v}_{DC}\right).$$

$$\tag{4.7}$$

We are now able to separate Eq. (4.7) in a steady state (DC) model and a dynamic (AC) small signal model. We will first obtain the DC model. If the system is in steady state then the derivative of the state vector x is zero. As a consequence and after neglecting the AC terms, (4.7) reduces to

$$\dot{\bar{x}} = \bar{0} = \left(A_2\bar{\delta}_1\frac{\bar{v}_{DC}}{NV_o} + A_3\left(1 - \bar{\delta}_1\frac{\bar{v}_{DC}}{NV_o}\right)\right)\bar{x} + B_1\bar{\delta}_1\bar{v}_{DC}.$$

Solving for the state vector x we obtain the DC model

$$\bar{x} = -\left(A_2\bar{\delta}_1\frac{\bar{v}_{DC}}{NV_o} + A_3\left(1 - \bar{\delta}_1\frac{\bar{v}_{DC}}{NV_o}\right)\right)^{-1} B_1\bar{\delta}_1\bar{v}_{DC}.$$

Substitution of the known component values, $V_{DC} = 375\text{V}$ and $\dfrac{P_o}{I_o^2} = R_L = 8.125\Omega$ results in

$$\bar{x} = \begin{pmatrix} 0.192\text{A} \\ 0.8\text{A} \\ 6.5\text{V} \\ 6.5\text{V} \end{pmatrix},$$

which was to be expected.

The AC model is obtained using a similar approach. If we neglect second order terms in (4.7) and drop the DC terms, then (4.7) can be written as

$$\tilde{x} = \left(A_2\bar{x}\frac{V_{DC}}{NV_o} - A_3\bar{x}\frac{V_{DC}}{NV_o} + B_1\bar{V}_{DC}\right)\tilde{\delta}_1 + \left(A_2\delta_1\frac{V_{DC}}{NV_o} + A_3 - A_3\bar{\delta}\frac{V_{DC}}{NV_o}\right)\tilde{x} + B_1\bar{\delta}_1\tilde{V}_{DC}.$$

$$\tag{4.8}$$

For our own ease we drop the tilde. As an intermediate step towards the derivation of the AC model we apply a Laplace transformation with respect to time. The Laplace transform domain

quantities are indicated by a diacritical hat. For example, the Laplace transform domain

counterpart of x is defined as $\hat{x} = \int_{t=0}^{\infty} \exp(-st)x\,dt$.

As a consequence of the Laplace transformation and the vanishing initial conditions we have $\partial t \rightarrow s$. Subjecting Eq. (4.8) to the Laplace transformation results in

$$s\hat{x} = \left(\mathbf{A}_2 \bar{x} \frac{\bar{v}_{DC}}{NV_o} - \mathbf{A}_3 \bar{x} \frac{\bar{v}_{DC}}{NV_o} + \mathbf{B}_1 \bar{v}_{DC} \right)\hat{\delta}_1 + \left(\mathbf{A}_2 \bar{\delta}_1 \frac{\bar{v}_{DC}}{NV_o} + \mathbf{A}_3 - \mathbf{A}_3 \bar{\delta} \frac{\bar{v}_{DC}}{NV_o} \right)\hat{x} + \mathbf{B}_1 \bar{\delta}_1 \hat{v}_{DC}.$$

$$(4.9)$$

Solving Eq. (4.9) for the state space vector $\hat{x}$ yields

$$\hat{x} = \left(s\mathbf{I} - \mathbf{A}_2 \bar{\delta}_1 \frac{\bar{v}_{DC}}{NV_o} - \mathbf{A}_3 + \mathbf{A}_3 \bar{\delta}_1 \frac{\bar{v}_{DC}}{NV_o} \right)^{-1} \left(\mathbf{A}_2 \bar{x} \frac{\bar{v}_{DC}}{NV_o} - \mathbf{A}_3 \bar{x} \frac{\bar{v}_{DC}}{NV_o} + \mathbf{B}_1 \bar{v}_{DC} \right)\hat{\delta}_1 +$$

$$(4.10)$$

$$\left(s\mathbf{I} - \mathbf{A}_2 \bar{\delta}_1 \frac{\bar{v}_{DC}}{NV_o} - \mathbf{A}_3 + \mathbf{A}_3 \bar{\delta}_1 \frac{\bar{v}_{DC}}{NV_o} \right)^{-1} \mathbf{B}_1 \bar{\delta}_1 \hat{v}_{DC}$$

in which $\mathbf{I}$ is the unit matrix. Eq. (4.10) is the AC model in the Laplace s-domain. We are now able to study the behaviour of the power path of the flyback converter in discontinuous mode up till frequencies of one tenth of the switching frequency.

4.2.2 Dynamic (AC) Small Signal Model of the Voltage Regulation Feedback Loop.

The voltage feedback circuitry including it's small signal equivalent is depicted in Fig. (4.3).

(a)   (b)
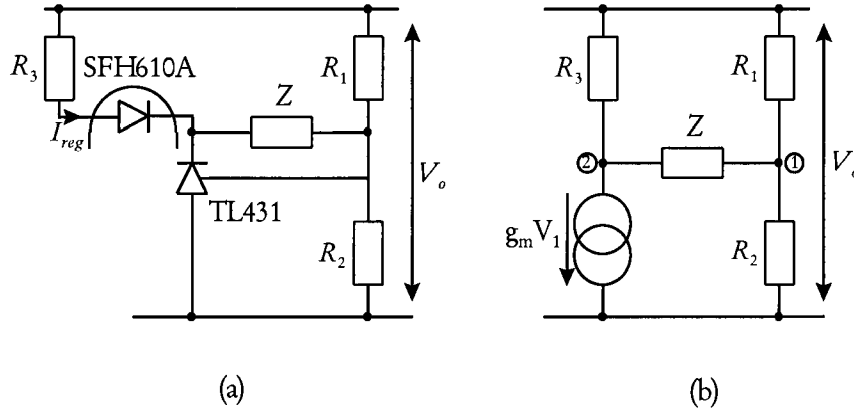
Fig. (4.3) Voltage feedback circuitry and it's small signal equivalent.

We will now apply Kirchhoff's current law on the marked nodes ① and ② to obtain the transfer

function $\dfrac{i_{reg}(s)}{v_o(s)}$. Solving for the opto-coupler led current as a consequence of the voltage V_o results

in

$$I_{reg} = \frac{g_m Z R_2 + g_m R_1 R_2 + R_1}{Z(R_1 + R_2) + g_m R_1 R_2 R_3 + R_1 R_2 + R_1 R_3 + R_2 R_3} V_o,$$

in which $g_m = 1.1 \mathrm{AV}^{-1}$, according the data sheets of the TL431.

Substituting a capacitor for the complex impedance Z leads to a led current

$$I_{reg}(s) = \frac{sC\left(g_m R_1 R_2 + R_1\right) + R_2 g_m}{sC\left(g_m R_1 R_2 R_3 + R_1 R_2 + R_1 R_3 + R_2 R_3\right) + R_1 + R_2} V_o. \tag{4.11}$$

Because of the absence of any DC-component in this transfer function we have for the AC-model

$$\frac{\tilde{i}_{reg}(s)}{\tilde{v}_o(s)} = \frac{sC\left(g_m R_1 R_2 + R_1\right) + R_2 g_m}{sC\left(g_m R_1 R_2 R_3 + R_1 R_2 + R_1 R_3 + R_2 R_3\right) + R_1 + R_2},$$

with resulting pole and zero,

$$n = -\frac{R_2 g_m}{C\left(g_m R_1 R_2 + R_1\right)},$$

$$p = -\frac{R_1 + R_2}{C\left(R_1 R_2 R_3 + R_1 R_2 + R_1 R_3 + R_2 R_3\right)},$$

and DC-gain

$$K_{DC} = \frac{R_2 g_m}{R_1 + R_2}.$$

For the component choice we have to take the parallel RC network attached to the comp pin in consideration. See Appendix C for the circuit diagram (components 3301 and 2302). The transfer function is

$$\frac{V_{comp}}{I_{reg}} = \frac{R_c}{sR_c C_c + 1},$$

with resulting pole

$$p = -\frac{1}{R_c C_c}.$$

Obtaining an overall low pass characteristic results in

$$\frac{R_2 g_m}{C\left(g_m R_1 R_2 + R_1\right)} = \frac{1}{R_c C_c},$$

$$R_c = \frac{g_m R_1 R_2 + R_1}{R_2 g_m} = 16\text{k}\Omega, \quad \text{if } C_c = C.$$

The overall system pole is chosen as low as possible, because the switching frequency of this converter can decrease to 29.38kHz. $C = 100\text{nF}$ results in a cut-off frequency of 2.56Hz.

4.2.3 Dynamic (AC) Small Signal Model of the Current Regulation Feedback Loop.

The circuit used for current regulation feedback is depicted in Fig. (4.4).

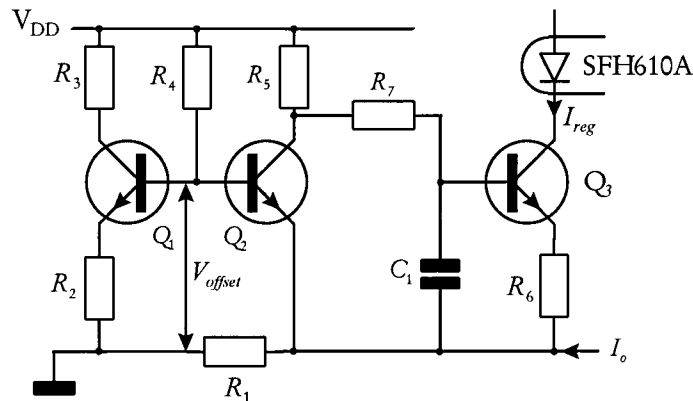*Fig. (4.4) Current control circuitry*

We will derive I_{reg} as function of I_o. For this circuit we can derive the next set of equations

$$I_{reg} = I_{c_{Q_3}} = S_{Q_3} V_{be_{Q_3}},$$

$$V_{be_{Q_3}} = V_{c_{Q_2}} \frac{1}{1 + sR_7 C_1},$$

$$V_{c_{Q_2}} = V_{DD} - I_{C_{Q_2}} R_5,$$

$$I_{C_{Q_2}} = S_{Q_2} V_{be_{Q_2}},$$

$$V_{be_{Q_2}} = V_{offset} - I_o R_1.$$

Substitution of these equations results in

$$I_{reg}(s) = \frac{S_{Q_3} V_{DD} - V_{offset} S_{Q_2} S_{Q_3} R_5}{1 + sR_7 C_1} + I_o \frac{S_{Q_2} S_{Q_3} R_5 R_1}{1 + sR_7 C_1}. \tag{4.12}$$

Creating disturbances in $I_o = \tilde{i}_o + \tilde{i}_o$ and drop the DC-terms in Eq. (4.12) results in the AC-model of the current control circuitry

$$\tilde{i}_{reg}(s) = \tilde{i}_o \frac{S_{Q_2} S_{Q_3} R_5 R_1}{1 + sR_7 C_1}, \tag{4.13}$$

with pole

$$p = -\frac{1}{R_7 C_1}.$$

Choosing $R_7 = 100\text{k}\Omega$ and $C_1 = 100\text{nF}$ results in a cut-off frequency of 15.92Hz.

4.3 Simulations

4.3.1 Simulations of the Voltage Regulation Feedback Loop.

We will now calculate the Bode and phase plots of the transfer function, derived in Section (4.2), using the mathematical package Mathcad. Since we are using a DC power supply we have no disturbances in the input voltage resulting in $\hat{v}_{DC} = 0\text{V}$. Therefore the state space vector of Eq. (4.10) changes to

$$\hat{x} = \left(sI - A_2 \bar{\delta}_1 \frac{\bar{v}_{DC}}{NV_o} - A_3 + A_3 \bar{\delta}_1 \frac{\bar{v}_{DC}}{NV_o} \right)^{-1} \left(A_2 \bar{x} \frac{\bar{v}_{DC}}{NV_o} - A_3 \bar{x} \frac{\bar{v}_{DC}}{NV_o} + B_1 \bar{v}_{DC} \right) \hat{\delta}, \tag{4.14}$$

creating a relationship between disturbances in the output voltage, the last element of the state vector, and disturbances in the primary duty cycle, $G_0(s) = \hat{x}(s)/\hat{\delta}(s)$. Rewriting (4.11) results in the transfer function $G_1(s) = \hat{i}_{reg}(s)/\hat{v}_o(s)$.For the voltage at the comp pin of the VIPer20, we can write

$$\hat{v}_{comp}(s) = \hat{i}_{reg}(s) \cdot CTR \cdot \frac{R_c}{sR_c C_c + 1},$$

resulting in the transfer function

$$G_2(s) = \frac{\hat{v}_{comp}(s)}{\hat{i}_{reg}(s)} = CTR \cdot \frac{R_c}{sR_c C_c + 1},$$

in which CTR is the current transfer ratio of the opto coupler and R_c with C_c are the components of the impedance at the comp pin. See Appendix C for the complete schematic in which R_c and C_c have component number 3301 and 3202 respectively. From the data sheets we have $G_3(s) = \tilde{v}_{comp}(s)/\tilde{i}_p(s) = 1/6$. The last step is finding a relationship between the primary peak current, $\hat{i}_p$, and the primary duty cycle, $\hat{\delta}$. For the primary peak current we have

$$\hat{I}_p = \frac{1}{L_p} \int_0^{\delta_p T} V_{DC} \mathrm{d}t = \frac{V_{DC}\delta_p T}{L_p},$$

which is equal to, and after rearranging,

$$G_4(s) = \frac{\tilde{\delta}_p(s)}{\hat{i}_p(s)} = \frac{L_p}{V_{DC}T}.$$

The open loop transfer function is now defined as $H^v_{open}(s) = G_0(s)G_1(s)G_2(s)G_3(s)G_4(s)$. The gain and phase of $H^v_{open}(s)$ are given in Fig. (4.5).

Fig. (4.5) Gain and phase plots of the theoretical open loop voltage regulation transfer function for $R_L = 10\Omega$ and $V_{DC} = 350V$.

From these plots we read a phase margin of $90°$ and a gain margin of more then 50dB, resulting in a stable system.

4.3.2 Simulations of the Current Regulation Feedback Loop.

We can use the same procedure as described in the last paragraph to calculate the gain and phase plots of the open loop transfer function when the converter is operating in current mode. In this mode we have the same power path which means that Eq. (4.14) is still valid. The relationship $G_5(s) = \hat{i}_{reg}(s)/\hat{i}_o(s)$ is given by Eq. (4.13). The open loop transfer function can now be defined as

$H^c_{open}(s) = \frac{G_0(s)}{R_{LOAD}} G_2(s)G_3(s)G_4(s)G_5(s)$. Division by R_{LOAD} is necessary since we are considering

the output current which is equal to the output voltage divided by the resistive load. The gain and phase of $H^c_{open}(s)$ are given in Fig. (4.6).
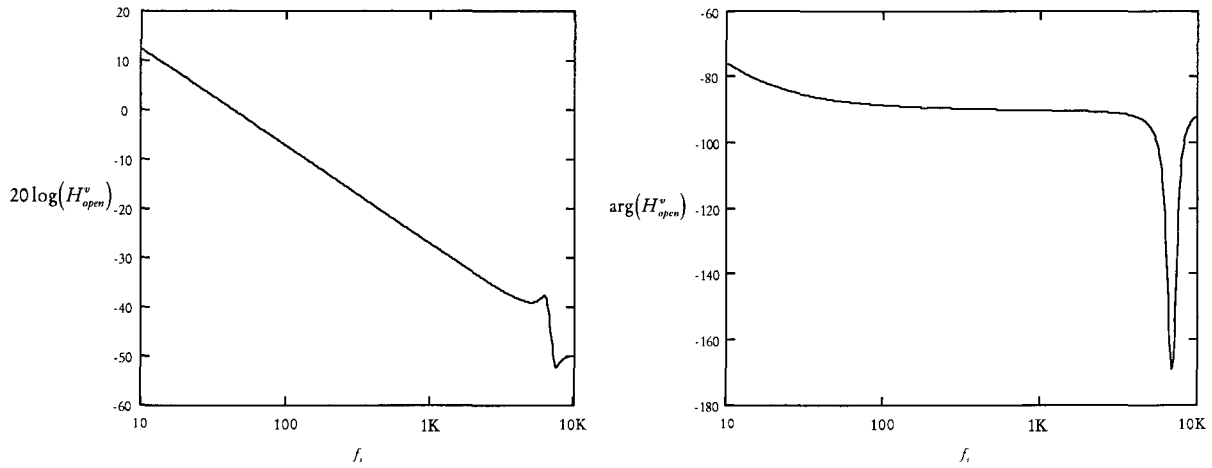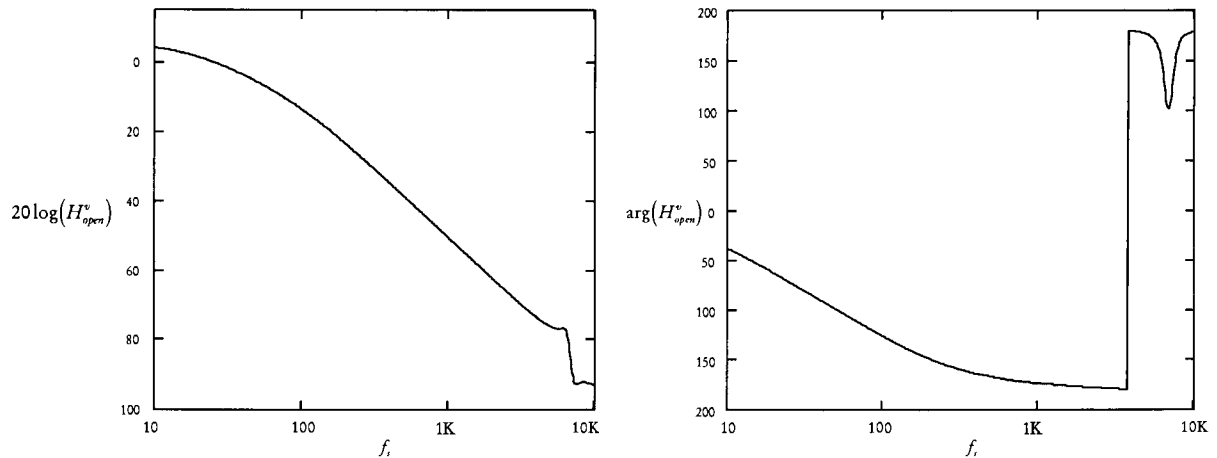
Fig. (4.6) Gain and phase plots of the theoretical open loop current regulation transfer function for
$R_L = 6\Omega$ *and* $V_{DC} = 350\text{V}$.

From these plots we read a phase margin of $110°$ and a gain margin of more then 70dB, resulting in a stable system.

4.4 Measurements

4.4.1 Loop Gain and Phase Measurement by Injection of a Test Signal into the Closed Loop

In practice it is extremely inconvenient to determine the loop properties by opening the feedback loop, since it is difficult to maintain the system at a proper operating point. One way to tackle this problem is to measure the loop properties in the closed loop, which are the same in a closed or opened system [2]. The measuring setup is depicted in Fig. (4.7).
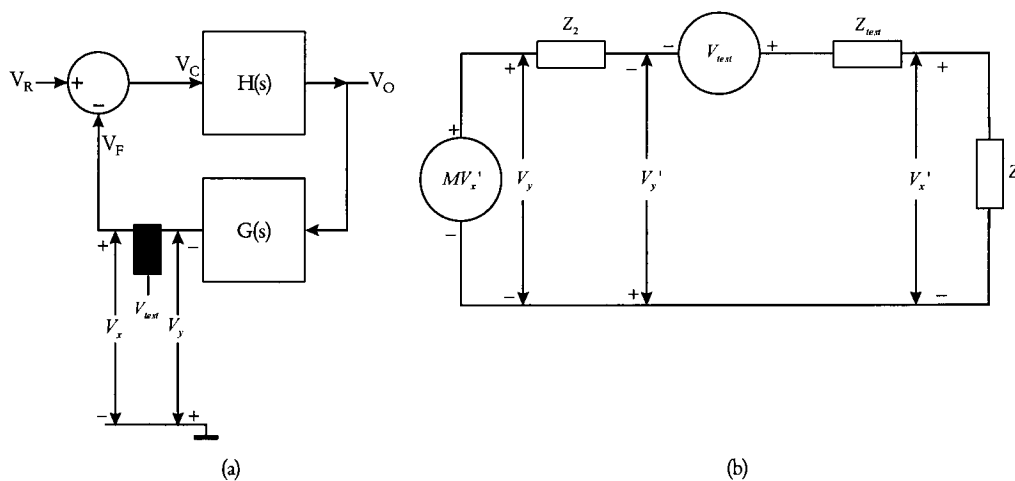
Fig. (4.7) Gain and phase measurement setup

A test signal, V_{test}, is injected in the control loop and measured directly after and ahead the injection point. The control loop gain and phase can be calculated using

$$\text{Gain} = 20\log\left(\left|\frac{V_x}{V_y}\right|\right),$$

$$\text{Phase} = \arg\left(\frac{V_x}{V_y}\right).$$

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In this figure Z_1 is the impedance looking "forward" from the injection point and Z_2 is the impedance looking "backwards" from the injection point. These impedances will create an error in our measurement as will explained below. In the most ideal case $Z_1 = \infty$ or very high and $Z_2 = 0\Omega$. The gain of the system can be expressed by

$$\frac{V_y}{V_x'} = K_{ideal} = M\frac{Z_1}{Z_1 + Z_2 + Z_{test}} \rightarrow K_{ideal} = M\frac{Z_1}{Z_1 + Z_{test}},$$

in which K_{ideal} is the ideal measured open loop gain. By approximation we have $K_{ideal} \approx M$ if $Z_1 \gg Z_{test}$, which is almost always the case. If $Z_2 \neq 0\Omega$, we can write for the gain of the system

$$\frac{V_y'}{V_x'} = K = M + \frac{Z_2}{Z_1} = \left(1 + \frac{Z_2 + Z_{test}}{Z_1}\right)K_{ideal} + \frac{Z_2}{Z_1},$$

resulting in

$$K_{ideal} = K\frac{Z_1}{Z_1 + Z_2 + Z_{test}} - \frac{Z_2}{Z_1 + Z_2 + Z_{test}},$$

and by approximation $K \approx K_{ideal}$ if $Z_1 \gg Z_2$. When measuring the gain using this setup, we have to compensate with this factor.

4.4.2 Gain Phase Measurement of the Voltage Regulation Feedback Loop.

The setup for measuring the properties of the voltage regulation feedback loop is given in Fig. (4.8). The injected voltage level, V_{test}, is 500mV$_{pp}$ and the resistive output load $R_L = 10\Omega$, forcing the battery charger to operate in voltage regulation mode.
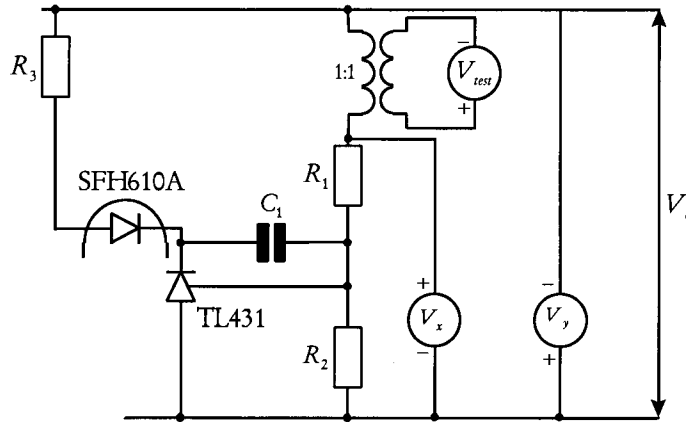
Fig. (4.8) Setup for the voltage regulation feedback loop measurement

In this situation we have

$$K_{ideal} = K\frac{Z_1}{Z_1 + Z_2 + Z_{test}} - \frac{Z_2}{Z_1 + Z_2 + Z_{test}} = K\frac{16k\Omega}{16k\Omega + 470\Omega + 50\Omega} - \frac{470\Omega}{16k\Omega + 470\Omega + 50\Omega}$$

$$= 0.969K - 0.028 \approx 0.969K,$$

resulting in a measured curve which is 0.3dB too high. Since the inputs of the gain-phase analyser are not floating, we have to change the polarity of probe V_y, resulting in a $180°$ phase shift. The results of the measurements are depicted in Fig. (4.9).

(a)   (b)
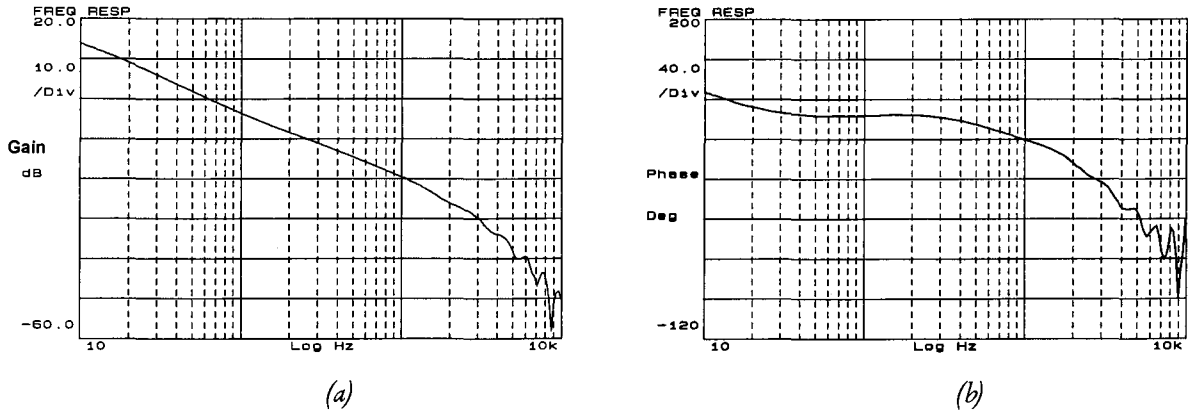
Fig. (4.9) Measured (a) gain and (b) phase plots in voltage regulation mode

The measured gain and phase at 10Hz are a bit too high (1.5dB and 25° respectively). From this we can conclude that the calculated pole at 2.56Hz is higher (approximately 5Hz). The sharp resonance at 7.23kHz, caused by the output CLC filter, is not present. The neglected series resistance of the output inductor decreases the quality factor, resulting in a damping of the resonance.

4.4.3 Gain Phase Measurement of the Current Regulation Feedback Loop.

The measurement setup is given in Fig. (4.10)
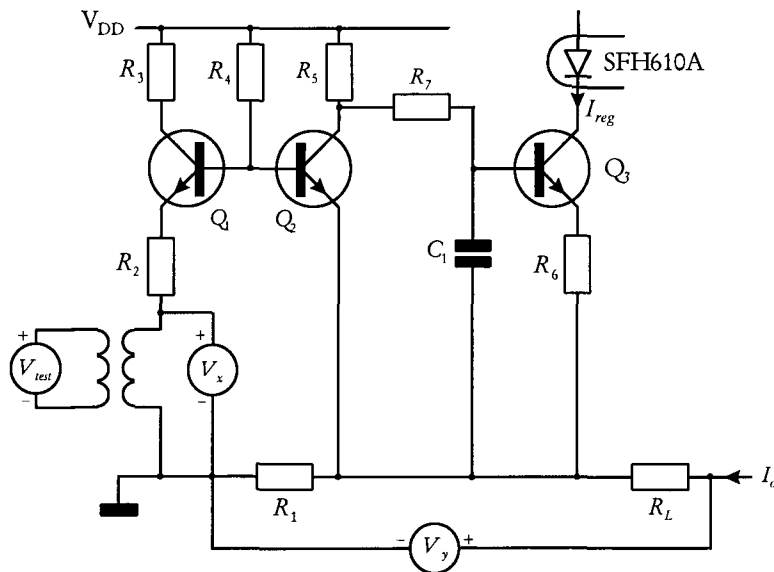
Fig. (4.10) Setup for the current regulation feedback loop measurement

Resistor R_2 is changed to 68Ω, in order to compensate for the source impedance $Z_{test} = 50\Omega$. Voltage V_y is normally measured across resistor R_1, which is in our case very impractical since $R_1 = 0.1\Omega$. The AC-voltage across R_1 is small resulting in inaccurate measurements. Increasing V_y can be accomplished by taking the resistive load R_L in consideration as depicted in Fig. (4.10).

In this situation we have

$$K_{ideal} = K\frac{Z_1}{Z_1 + Z_2 + Z_{test}} - \frac{Z_2}{Z_1 + Z_2 + Z_{test}} = K\frac{68\Omega}{68\Omega + (0.1\Omega + 6\Omega) + 50\Omega} - \frac{0.1\Omega + 6\Omega}{68\Omega + (0.1\Omega + 6\Omega) + 50\Omega}$$

$$= 0.55K - 0.049 \approx 0.55K,$$

resulting in a measured curve which is 5.2dB too low. The DC-error introduced by measuring across $R_1 + R_L$ is

$$\frac{R_L}{R_1} = \frac{6\Omega}{0.1\Omega} = 60 \rightarrow 35.6\text{dB},$$

resulting in a measured curve of 35.6dB to high. Both these errors result in a measured curve of 30.4dB to high. The results of the measurements are depicted in Fig. (4.11).
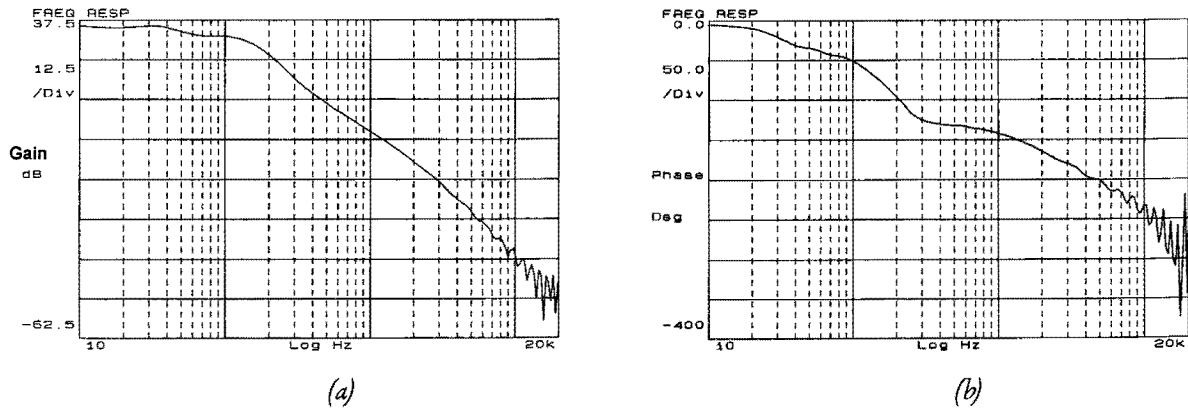
Fig. (4.11) Measured (a) gain and (b) phase plots in current regulation mode

The measured gain at 10Hz is in accordance with the calculated value. The measured phase at the same frequency is 25° too high. This means that the calculated pole at 16.92Hz is actually placed at a higher frequency. The resonance of the output CLC filter is not clear in the picture since the measured voltage are too low for the gain-phase analyser.

5. Electrical Losses in the Converter

In this chapter we will analyze and verify by measurement the electrical losses in the converter at $V_{AC} = 110V$ and $V_{AC} = 230V$, both at $P_o = 5.2W$. The following loss mechanisms can be identified in the converter,

- losses in the transformer. We will identify DC, skin, proximity effects,
- losses in the VIPer20. We will identify switching, R_{DS} and supply losses,
- losses in the input circuit ,
- losses in the output circuit,
- losses in the current sense resistor,
- losses in additional electronics.

The losses are calculated with the simulation program ICAPS/4 or MathCad.

5.1 Losses in the Transformer

Since skin depth is a function of the frequency, we will decompose the primary and secondary currents into their harmonic components by using a Fourier transform as explained in Appendix A. After that we are able to calculate the losses of each frequency component and summation results in the total losses.

5.1.1 DC Losses

The first part of the transformer losses are the DC losses and are calculated using

$P_{DC} = I_p^2 R_{DC_p} + I_s^2 R_{DC_s}$, in which the subscript p is used to denote the primary winding and the subscript s is used to denote the secondary winding. We neglect the DC losses in the bias winding, since the bias current is very low. The resistance of the copper wire is equal to

$$R_{DC_p} = \frac{\rho_{CU} N_p l_k}{\pi \left(\frac{d_p}{2}\right)^2} ,$$

$$R_{DC_s} = \frac{\rho_{CU} N_s l_k}{\pi \left(\frac{d_s}{2}\right)^2} ,$$

in which l_k is the winding length of one turn. Using the amplitudes calculated in Appendix A we find

$$P_{DC_p} = \sum_{n=1}^{m} \left(a_n^p \frac{\hat{I}_p}{\sqrt{2}}\right)^2 R_{DC_p} + \left(a_p^0 \frac{\hat{I}_p}{\sqrt{2}}\right)^2 R_{DC_p} ,$$

$$P_{DC_s} = \sum_{n=1}^{m} \left(a_n^s \frac{\hat{I}_s}{\sqrt{2}}\right)^2 R_{DC_s} + \left(a_s^0 \frac{\hat{I}_s}{\sqrt{2}}\right)^2 R_{DC,P} , .$$

$$P_{DC} = P_{DC_p} + P_{DC_s} .$$

If the input voltage increases, then the primary RMS current decreases. The secondary RMS current is independent of the input voltage. Calculating the DC losses for $V_{AC} = 110V$ and $V_{AC} = 230V$ results in $P_{DC}|_{110V} = 99.55\text{mW}$ and $P_{DC}|_{230V} = 72.63\text{mW}$ respectively.

5.1.2 Skin Effect Losses

The skin depth is given by

$$\delta^n_{skin} = \sqrt{\frac{\rho_{CU}}{\mu_r \mu_0 \pi n f_s}} \, .$$ (5.1)

The skin depth is a function of the frequency, so the harmonics have different penetration depths in copper, which are decreasing resulting in a increasing resistance. The idea is to calculate the skin depths for the different harmonics and compute the representative resistance. Each harmonic component has it's own losses and after summation we have the total skin losses. As will be clear, some harmonics are not causing any skin effect, since the skin depth is larger or equal to the radius of the wire. We also neglect the skin losses in the bias winding, since the bias current is very low. First we calculate the area in which the primary and the secondary current flows,

$$A^n_p = \pi \left(\frac{d_p}{2}\right)^2 - \pi \left(\frac{d_p}{2} - \delta^n_{skin}\right)^2,$$

$$A^n_s = \pi \left(\frac{d_s}{2}\right)^2 - \pi \left(\frac{d_s}{2} - \delta^n_{skin}\right)^2.$$ (5.2)

From this we find that the first five harmonics of the primary current do not cause any skin effect. In general we have for the resistance of a wire $R = \frac{\rho l}{A}$, in which A is the cross area of the wire, ρ is the conductivity of the used material and l is the length of the wire. Making use of this and Eqs. (5.1) and (5.2) we have,

$$R^n_{skin_p} = \frac{\rho_{CU} N_p l_k}{\pi \left(\frac{d_p}{2}\right)^2 - \pi \left(\frac{d_p}{2} - \sqrt{\frac{\rho_{CU}}{\mu_r \mu_0 \pi n f_s}}\right)^2},$$

$$R^n_{skin_s} = \frac{\rho_{CU} N_s l_k}{\pi \left(\frac{d_s}{2}\right)^2 - \pi \left(\frac{d_s}{2} - \sqrt{\frac{\rho_{CU}}{\mu_r \mu_0 \pi n f_s}}\right)^2}.$$ (5.3)

The dissipated power is equal to $P = I^2 R$. Calculating this for the n harmonics, summating the results for primary and secondary side, we have

$$P_{skin_p} = \left(a^p_0 \frac{\hat{I}_p}{\sqrt{2}}\right)^2 R_{DC_p} + \sum_{n=1}^{5}\left(\sqrt{(a^n_p)^2 + (b^n_p)^2}\frac{\hat{I}_p}{\sqrt{2}}\right)^2 R_{DC_p} + \sum_{n=6}^{m}\left(\sqrt{(a^n_p)^2 + (b^n_p)^2}\frac{\hat{I}_p}{\sqrt{2}}\right)^2 R^n_{skin_p},$$

$$P_{skin_s} = \left(a^s_0 \frac{\hat{I}_p}{\sqrt{2}}\right)^2 R_{DC_s} + \sum_{n=1}^{m}\left(\sqrt{(a^n_s)^2 + (b^n_s)^2}\frac{\hat{I}_s}{\sqrt{2}}\right)^2 R^n_{skin_s},$$

$$P_{skin} = P_{skin_p} + P_{skin_s} - P_{DC}.$$

Since the amplitude of the harmonics is dependent of the input voltage, we will calculate the skin losses for both the input voltages. Substitution of the calculated values we have

$P_{skin}|_{110V} = 7.79\text{mW}$ and $P_{skin}|_{230V} = 8.73\text{mW}$.

5.1.3 Proximity Losses

Up to this point a single isolated conductor is considered. When another conductor is brought into close proximity to the first, proximity losses are created. This will be explained by the use of Fig. (5.1).
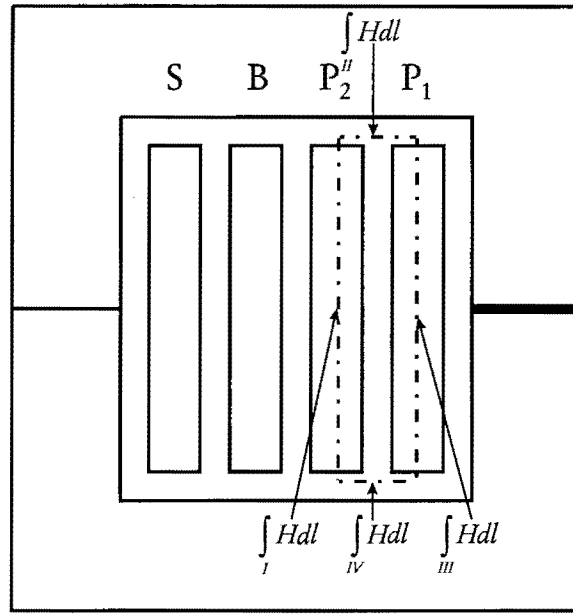
Fig. (5.1) Proximity Losses.

As indicated in this figure, we depict the windings as a solid sheet. Since we approximate the layers with solid sheets, we have to redefine the resistance of the wire due to skin effect

$$R^n_{skin_p} = \frac{\rho_{cu} l_k}{\frac{N_p}{2} d_p \delta^n_{skin}},$$

$$R^n_{skin_s} = \frac{\rho_{cu} l_k}{N_s d_s \delta^n_{skin}},$$

$$R^n_{skin_b} = \frac{\rho_{cu} l_k}{N_b d_b \delta^n_{skin}}.$$

For the explanation of the proximity effect we use Ampere's law, $\oint H dl = I$. We can separate this integral in four parts as indicated in the figure $\int\limits_{I} H dl + \int\limits_{II} H dl + \int\limits_{III} H dl + \int\limits_{IV} H dl = I_{encl}$. In the middle of the first and the second primary sheet, the H field is zero. The contributions of integral *I* and *III* to the contour integral are zero. The contributions of integral *II* and *IV* are zero since the H field is perpendicular to the integration path. Summation results in

$$\int\limits_{I} H dl + \int\limits_{II} H dl + \int\limits_{III} H dl + \int\limits_{IV} H dl = I_{encl} = 0A.$$

If we have, in the region enclosed by the integration path, a current of 1A in P_1, then, as a consequence, we have $-1A$ in P_2. The net current in P_2 is still 1A and as a logic result we have outside the integration region in P_2 a current of 2A, to compensate for the negative current. This process continues up to the outer windings and results in increasing currents.

The proximity losses are calculated in two steps. In the on time, the primary winding is the source and during the off time the secondary winding is the source. We neglect the bias winding as a source, but calculate the losses in it.

The calculations used for the proximity losses are given below. To make a paper and pencil calculation possible, we approximate the winding layers by solid sheets and assume currents to fall

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off abruptly. If $\delta_{skin} > \dfrac{d}{2}$, we have one of the two possibilities as depicted in Fig. (5.2). From these current distributions we can calculate the average current in the sheet which are respectively

$$\bar{I}_{(a)} = \frac{2I(d - \delta_{skin}) + I\delta_{skin}}{d},$$

$$\bar{I}_{(b)} = \frac{2(d - \delta_{skin})}{d}.$$
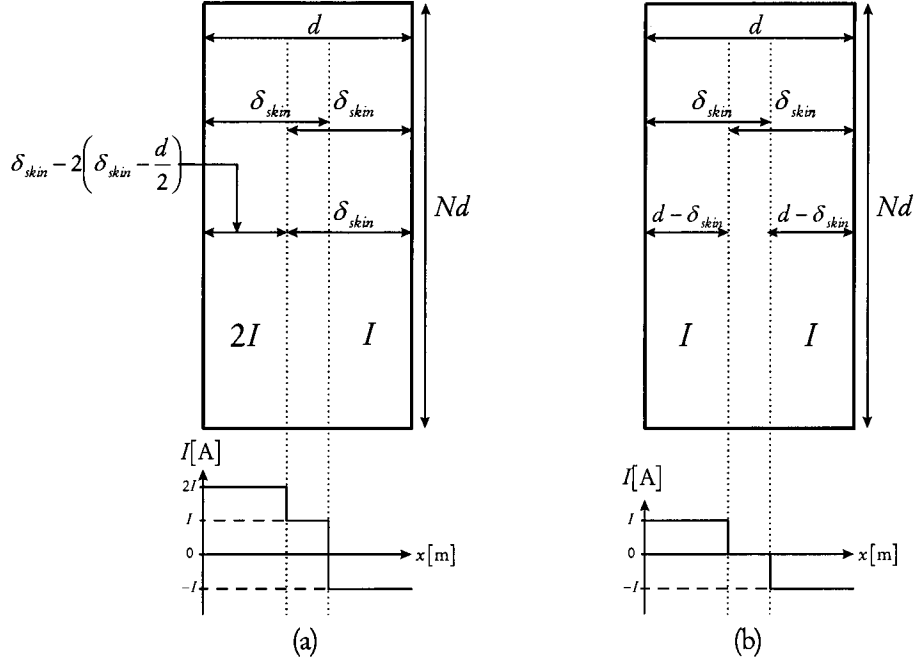
Fig. (5.2) Occurring current distributions in the winding sheets when $\delta_{skin} > \dfrac{d}{2}$ with (a) unequal currents and (b) equal currents.

The proximity losses in the first primary layer

$$P^{on}_{prox\,p1} = \left(a_p^0 \frac{\hat{I}_p}{\sqrt{2}} \right)^2 R_{DC_p} + \left(\sqrt{\left(a_p^1\right)^2 + \left(b_p^1\right)^2} \; \frac{\hat{I}_p}{\sqrt{2}} \right)^2 R_{DC_p} + \sum_{n=2}^{m} \left(\sqrt{\left(a_p^n\right)^2 + \left(b_p^n\right)^2} \; \frac{\hat{I}_p}{\sqrt{2}} \right)^2 R^n_{skin_p} \; .$$

The proximity losses in the second primary layer

$$P^{on}_{prox\,p2} = \left(a_p^0 \frac{\hat{I}_p}{\sqrt{2}} \right)^2 + \left(\sqrt{\left(a_p^1\right)^2 + \left(b_p^1\right)^2} \; \frac{\hat{I}_p}{\sqrt{2}} \right)^2 R_{DC_p} + \left(\sqrt{\left(a_p^2\right)^2 + \left(b_p^2\right)^2} \; \frac{1.18\hat{I}_p}{\sqrt{2}} \right)^2 R_{DC_p}$$

$$+ \left(\sqrt{\left(a_p^3\right)^2 + \left(b_p^3\right)^2} \; \frac{1.33\hat{I}_p}{\sqrt{2}} \right)^2 R_{DC_p} + \left(\sqrt{\left(a_p^4\right)^2 + \left(b_p^4\right)^2} \; \frac{1.42\hat{I}_p}{\sqrt{2}} \right)^2 R_{DC_p}$$

$$+ \left(\sqrt{\left(a_p^5\right)^2 + \left(b_p^5\right)^2} \; \frac{1.48\hat{I}_p}{\sqrt{2}} \right)^2 R_{DC_p} + \sum_{n=6}^{m} \left(\sqrt{\left(a_p^n\right)^2 + \left(b_p^n\right)^2} \; \frac{2\hat{I}_p}{\sqrt{2}} \right)^2 R^n_{skin_p}$$

$$+ \sum_{n=6}^{m} \left(\sqrt{\left(a_p^n\right)^2 + \left(b_p^n\right)^2} \; \frac{\hat{I}_p}{\sqrt{2}} \right)^2 R^n_{skin_p}$$

The proximity losses in the bias winding

$$P^{on}_{prox_b} = \left(\sqrt{\left(a_p^1\right)^2 + \left(b_p^1\right)^2} \; \frac{1.34\hat{I}_p}{\sqrt{2}} \right)^2 R_{DC_b} + 2\sum_{n=2}^{m} \left(\sqrt{\left(a_p^n\right)^2 + \left(b_p^n\right)^2} \; \frac{2\hat{I}_p}{\sqrt{2}} \right)^2 R^n_{skin_b}$$

The proximity losses in the secondary winding

$$P^{on}_{prox_s} = 2\sum_{n=1}^{m} \left(\sqrt{\left(a_p^n\right)^2 + \left(b_p^n\right)^2} \; \frac{2\hat{I}_p}{\sqrt{2}} \right)^2 R^n_{skin_s}$$

The proximity losses in the first primary layer

$$P^{off}_{prox_{P_1}} = \left(\sqrt{\left(a_s^2\right)^2 + \left(b_s^2\right)^2} \; \frac{0.36\hat{I}_s}{\sqrt{2}} \right)^2 R_{DC_p} + \left(\sqrt{\left(a_s^3\right)^2 + \left(b_s^3\right)^2} \; \frac{0.66\hat{I}_s}{\sqrt{2}} \right)^2 R_{DC_p}$$

$$+ \left(\sqrt{\left(a_s^4\right)^2 + \left(b_s^4\right)^2} \; \frac{0.84\hat{I}_s}{\sqrt{2}} \right)^2 R_{DC_p} + \left(\sqrt{\left(a_s^5\right)^2 + \left(b_s^5\right)^2} \; \frac{0.95\hat{I}_s}{\sqrt{2}} \right)^2 R_{DC_p}$$

$$+ 2\sum_{n=6}^{m} \left(\sqrt{\left(a_s^n\right)^2 + \left(b_s^n\right)^2} \; \frac{\hat{I}_s}{\sqrt{2}} \right)^2 R^n_{skin_p}$$

The proximity losses in the second primary layer are equal to the proximity losses in the first primary layer. The proximity losses in the bias winding

$$P^{off}_{prox_b} = \left(\sqrt{\left(a_s^1\right)^2 + \left(b_s^1\right)^2} \; \frac{0.67\hat{I}_s}{\sqrt{2}} \right)^2 R_{DC_b} + 2\sum_{n=2}^{m} \left(\sqrt{\left(a_s^n\right)^2 + \left(b_s^n\right)^2} \; \frac{\hat{I}_s}{\sqrt{2}} \right)^2 R^n_{skin_b}$$

The proximity losses in the secondary winding

$$P^{off}_{prox_s} = \left(a_p^0 \; \frac{\hat{I}_s}{\sqrt{2}} \right)^2 R_{DC_s} + \sum_{n=1}^{m} \left(\sqrt{\left(a_s^n\right)^2 + \left(b_s^n\right)^2} \; \frac{\hat{I}_s}{\sqrt{2}} \right)^2 R^n_{skin_s}$$

The calculated proximity losses are $P_{prox}\big|_{110V} = 64.17 \mathrm{mW}$ and $P_{prox}\big|_{230V} = 14.41 \mathrm{mW}$.

5.1.4 Core Losses

The core losses are calculated using Steinmetz formula [1],

$$P_{core}(\tau) = C_m f^x B^y \left(c_2 \tau^2 - c_1 \tau + c \right).$$

The constants for the material 3C85 in the frequency range of 100kHz up to 200kHz are $C_m = 1.5$, $x = 1.5$, $y = 2.6$, $c_2 = 0.91 \cdot 10^4$, $c_1 = 1.88 \cdot 10^2$ and $c = 1.97$. This formula is a function of the temperature τ as depicted in Fig. (5.3).
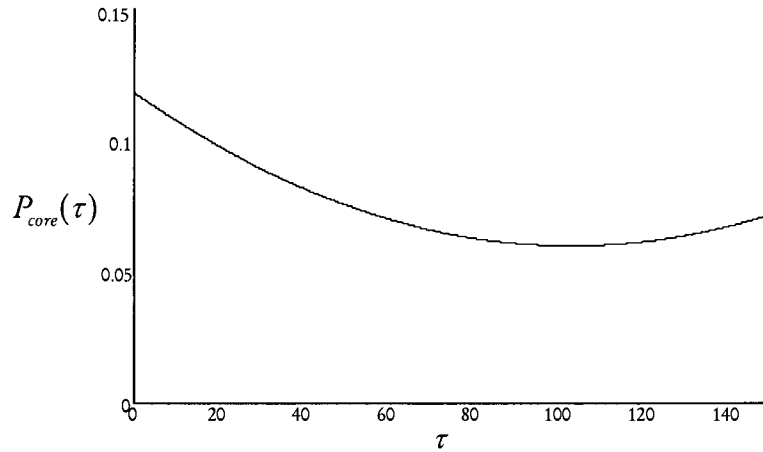
Fig. (5.3) Core losses as function of the temperature of 3C85 ferrite at $V_{AC} = 230V$ and $P_o = 5.2W$.

The graph shows that the losses have a minimum at $90°C < \tau < 115°C$, which will be the working temperature of the transformer. The problem is that this formula is only valid for sinusoidal shaped signals. In our case of triangular shaped signals, the frequency is multiplied with a correction number K to compensate for this difference. This correction number K is well described in [1]. The core losses are not only dependent of B_{pp} but also of $\dfrac{dB_{pp}}{dt}$. As a consequence K will be dependent of the primary duty cycle δ_p and we will calculate P_{core} for high and low input voltage. For low input voltage, $V_{AC} = 110V$, and maximum output power, $P_o = 5.2W$, we have $K = 1.25$ and $B_{AV} = 100mT$. This results in $P_{core}(100°C) = 58.18mW$. For high input voltage, $V_{AC} = 230V$, and maximum output power, $P_o = 5.2W$, we have $K = 3$ and $B_{AV} = 72.5mT$. This results in $P_{core}(100°C) = 60.51mW$. We could not choose maximum input voltage and minimum output power as a more extreme situation since we decrease the switching frequency as the duty cycle becomes less than 0.1.

5.2 Losses in the VIPer20

The losses in the VIPer20 can be separated in 3 parts, the switching and conduction losses of the internal MOSFet and the power supply losses for the control logic and gate drive of the VIPer20. The switching losses can be calculated by having a closer look at the drain-source voltage ringing. This ringing is a result of oscillations produced by the primary and leakage inductance in combination with the drain-source capacitance and parasitic capacitance in the primary circuitry. A drain-source voltage graph is depicted in Fig. (5.4). We measured the frequency of the high and low frequency ringing with the oscilloscope, resulting in $f_r^h = 6.1MHz$ and $f_r^l = 900kHz$ respectively.
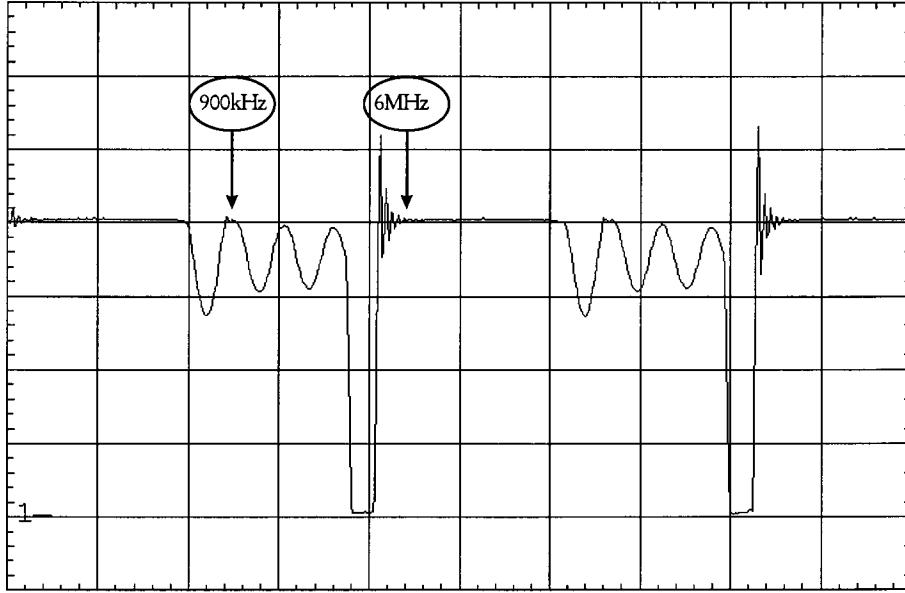
Fig. (5.4) Drain-source voltage ringing

For the low frequency ringing we have

$$f_r^l = \frac{1}{2\pi\sqrt{(L_p + L_\sigma)C_p}},$$
(5.4)

and for the high frequency ringing we have

$$f_r^b = \frac{1}{2\pi\sqrt{L_\sigma C_p}}$$
(5.5)

From Eqs. (5.4), (5.5) and the primary inductance $L_p = 458.64\mu H$, we can calculate C_p and L_σ , Which results in $C_p = 66.70\text{pF}$ and $L_\sigma = 10.21\mu H$. The energy of C_p is dissipated during turning the MOSFet in an on state. This energy is equal to $\frac{1}{2}C_p(V_{DC} + NV_o)^2$, and is different for high and low input voltages. This results in

$$V_{DC} = \sqrt{2} \cdot 110\text{V} = 155.56\text{V} \rightarrow \frac{1}{2}C_p(V_{DC} + NV_o)^2 = \frac{1}{2} \cdot 66.70\text{pF}(155.56\text{V} + 7 \cdot 6.5\text{V})^2 = 1.35\mu J,$$

$$V_{DC} = \sqrt{2} \cdot 230\text{V} = 325.27\text{V} \rightarrow \frac{1}{2}C_p(V_{DC} + NV_o)^2 = \frac{1}{2} \cdot 66.70\text{pF}(325.27\text{V} + 7 \cdot 6.5\text{V})^2 = 4.58\mu J.$$

Multiplying by the switching frequency results in the switching losses 168.75mW and 572.50mW respectively.

The conduction losses are calculated using

$$P_{R_{DS}} = R_{DS}I_{p_{RMS}}^2 = R_{DS}\left(\hat{I}_p\sqrt{\frac{\delta_p}{3}}\right)^2.$$
(5.6)

Substitution of $R_{DS} = 16\Omega, \hat{I}_p = 420\text{mA}$, $\delta_p\big|_{110V} = 0.375$ and $\delta_p\big|_{230V} = 0.1$ results in

$P_{R_{DS}}\big|_{110V} = 352.8\text{mW}$ and $P_{R_{DS}}\big|_{230V} = 94.08\text{mW}$.

The power supply losses are calculated from the data sheets by using the maximum input current and the working voltage at the V_{DD} pin. This results in $P_{PS} = 13\text{mA} \cdot 12\text{V} = 156\text{mW}$. The results are recapitulated in Table (5.1).

	$V_{AC} = 110\text{V}$	$V_{AC} = 230\text{V}$
Switching	168.75mW	572.50mW
Conduction	352.8mW	94.08mW
Power Supply	156mW	156mW
Total	**677.55mW**	**822.58mW**

Table (5.1) Losses in the VIPer20.

5.3 Losses in the Input Circuit.

We calculated the losses in the input circuitry by making use of the simulation program ICAPS/4. The simulated circuit is depicted in Fig. (5.5).
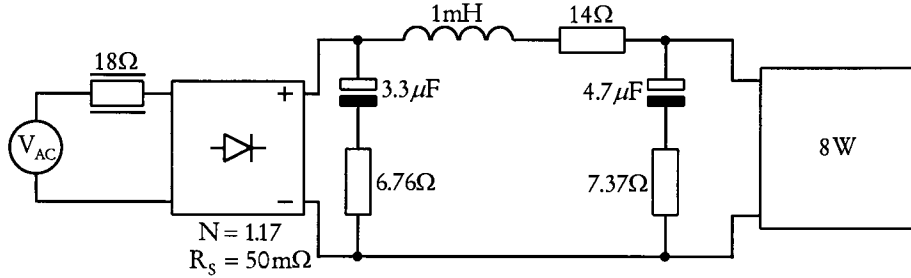

Fig. (5.5) Model for calculating the input section losses.

The resistors in series with the capacitors and inductor represent the equivalent series resistance of these components. Before we could make simulations of the input section, we had to make a correct diode model for the diodes used in the diode bridge. From the V_F versus I_D curve taken from the data sheets, we calculated the emission coefficient, N , and the series resistance, R_s . This resulted in N= 1.17 and R_s = 50mΩ. We simulated at V_{AC} is 110V and 230V . The results are given in Table (5.2).

	$V_{AC} = 110\text{V}$	$V_{AC} = 230\text{V}$
Resistor 18Ω	237mW	89.7mW
Diode Bridge	102mW	46.8mW
Inductor 1mH	97.5mW	30.3mW
Capacitor 3.3μF	11.5mW	5.1mW
Capacitor 4.7μF	25.6mW	11.1mW
Total	**473.6mW**	**183mW**

Table (5.2) Calculated losses in the input section.

5.4 Losses in the Output Circuit

The losses in the output circuit mainly consists of the secondary diode and the inductor losses. The inductor losses are equal to $P_{22\mu H} = I_{s_{RMS}}^2 R_{22\mu H} = (0.8\,\text{A})^2 \cdot 0.19\Omega = 121.6\text{mW}$. The losses of the secondary diode are equal to

$$P_D = \frac{1}{T}\int_0^T U_D I_D dt = \frac{1}{T}\left(\int_0^{\delta_1 T} U_R I_R dt + \int_0^{\delta_2 T} U_F I_F dt \right), \tag{5.7}$$

in which the subscript R represents the Reverse and the subscript F the Forward. From the data sheets we have $I_R|_{100^\circ C} = 0.6\text{mA}$ and $U_F|_{100^\circ C} = 650\text{mV}$. The reverse voltage, U_R , is equal to the

input voltage divided by the transformer transfer ratio N, which, in our case, is 7. For the forward current we have

$$I_F = \hat{I}_s \sqrt{\frac{\delta_s}{3}} = \hat{I}_p N \sqrt{\frac{\delta_s}{3}} = 420\text{mA} \cdot 7 \sqrt{\frac{0.625}{3}} = 1.34\text{A}.$$

Since the primary duty cycle and the reverse voltage are dependent of the input voltage, we have to calculate the losses for $V_{AC} = 110\text{V}$ and $V_{AC} = 230\text{V}$. The primary duty cycle at 110V is 30% at full load and 10% at 230V at full load. The switching period T is 8ms. Substitution in Eq. (5.7) results in $P_D|_{110\text{V}} = 670.98\text{mW}$ and $P_D|_{230\text{V}} = 676.43\text{mW}$.

5.5 Losses in the Current Sense Resistor

Although the losses in the current sense resistor are reduced, it still contributes to the total losses. The losses are equal to $P_C = I_s^2 R_C = (0.8\text{A})^2 \cdot 100\text{m}\Omega = 64\text{mW}$.

5.6 Losses in the Additional Electronics

A rough estimation of the losses in additional electronics will be made. First the losses in the voltage references including their bias resistors. Primary we have voltage regulator diode D_{6302}. Since the supply voltage is approximately 12V we have a bias current of 5mA (R_{3303}). This results in a total loss of 60mW. Secondary we have Q_{8202} (TL431). The supply voltage is 6.5V, which results in a bias current of 8.51mA and a total loss of 55mW. We also have primary the bias resistors of Q_{7300}, R_{3302} and R_{3305}. The current here is by approximation the supply voltage divided by the resistors, in other words, we neglect the collector emitter voltage. The total losses are 30mW. The total losses in the additional electronics, with some neglected losses included, can be estimated at 175mW.

5.7 Total Losses in the Converter

We will enumerate the losses in Table (5.3).

	$V_{AC} = 110\text{V}$	$V_{AC} = 230\text{V}$
Transformer	229.69mW	156.28mW
VIPer20	677.55mW	822.58mW
Input Circuit	473.6mW	183mW
Output Circuit	670.98mW	676.43mW
Current Sense Resistor	64mW	64mW
Additional Electronics	175mW	175mW
Total	2290.82mW	2077.29mW

Table (5.3) Total losses in the converter.

From this we can calculate the efficiency of the converter at $P_o = 5.2\text{W}$ which is $\eta|_{110\text{V}} = 0.65$ and $\eta|_{230\text{V}} = 0.71$.

5.8 Efficiency Measurements

The efficiency of the converter is measured with an electronic source (Hewlett Packard 6812A) and an electronic load (Hewlett Packard 6050A) at both the input voltages. The results are depicted in Fig. (5.6) below.
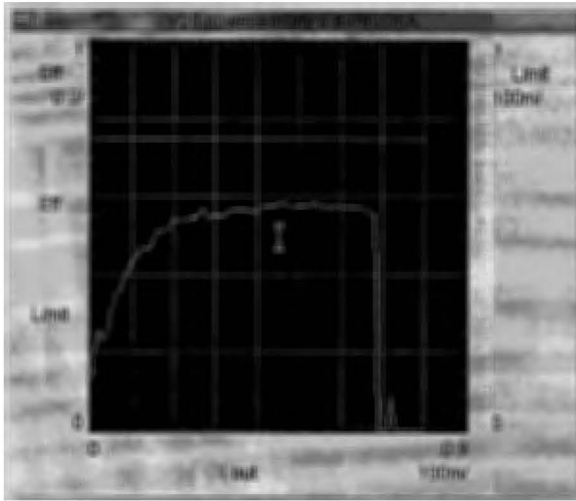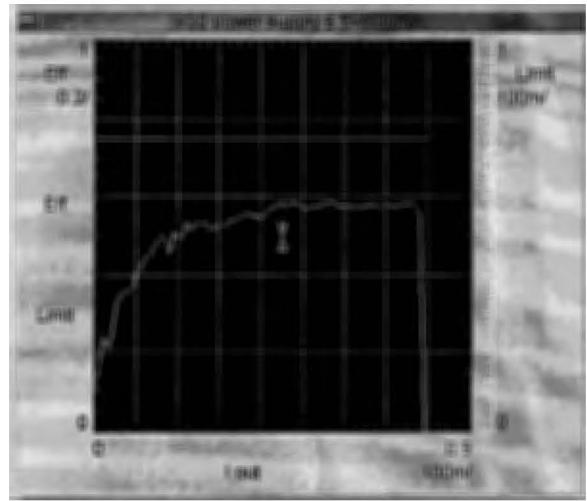
(a)   (b)

Fig. (5.6) (a) Efficiency of the converter at $V_{AC} = 110V$ (b) Efficiency of the converter at $V_{AC} = 230V$

The efficiency is 0.55 at 110V and 0.57 at 230V. It is rather difficult to include all the losses in the converter, but the gap between the measured and the calculated efficiency is to big. Therefore we measured the input current and voltage at $I_o = 781mA$ and $V_o = 6.29V$, resulting in $P_o = 4.93W$, in order to obtain the efficiency of the converter. The results are depicted in Table (5.4).

$V_{AC}[V]$	$I_{AC}[mA]$	$P_{AC}[W]$	$\eta[\%]$
110	68	7.5	66
230	33	7.5	66

Table (5.4) Results of the efficiency measurements

These values do agree with the calculated values.

6. Electro Magnetic Interference

One of the disadvantages of switched mode power supplies are the small rise and fall times of the switching signals and therefor higher harmonics are involved. While designing a switched mode power supply, one should try to minimize the cause of the disturbances if possible. In this chapter several aspects will be presented. Measurements be done at the final power supply and will be explained.

6.1 Measurement Setup

The two types of conducted noise, common mode and differential mode noise, are measured at EPM by use of a line impedance stabilization network conform the CISPR-16 standard [*CISPR-16, IEC 1987, 1993*]. The setup is depicted in Fig. (6.1).
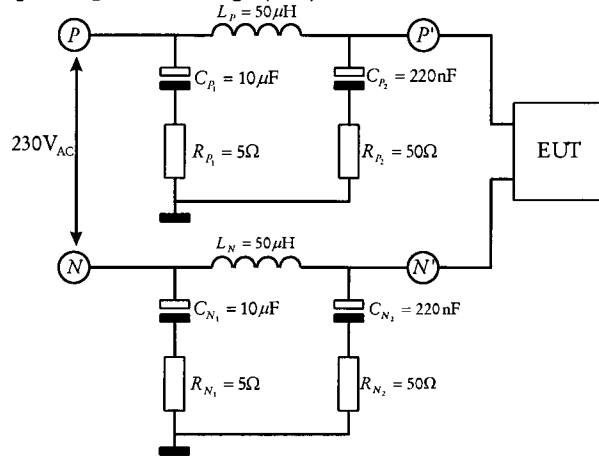

Fig. (6.1) An $50\Omega / 50\mu H + 5\Omega$ *artificial mains V-network conform the CISPR-16 standard*

The conducted noise will be presented as a voltage across R_{P_2} or R_{N_2} ,depending on which line the dBμV meter is connected. If the dBμV meter is connected, then the 50Ω is the internal impedance of the dBμV meter, otherwise a 50Ω resistor is connected. One aim is to create a constant impedance to ground for both the dBμV meter and the EUT, whatever the impedance of the mains is, over the working frequency range. For the impedance to ground when looking in the EUT-p connector with the mains short-circuited to ground, we have

$$Z_i^1 = \frac{-\omega^2 C_{P_2} L_P R_{P_2} + j\omega L_P}{-\omega^2 C_{P_2} L_P + j\omega C_{P_2} R_{P_2} + 1} \xrightarrow{\omega \gg 1} R_{P_2} = 50\Omega .$$

The actual values are lower resulting in $Z_i^1 = 36.14\Omega$ at 150kHz and $Z_i^1 = 50\Omega$ at 30MHz.
For the impedance to ground when looking across R_{P_2} we have

$$Z_i^2 = \frac{-\omega^2 C_{P_2} L_P R_{P_2} + R_{P_2}}{-\omega^2 C_{P_2} L_P + j\omega C_{P_2} R_{P_2} + 1} \xrightarrow{\omega \gg 1} R_{P_2} = 50\Omega .$$

The actual values are lower resulting in $Z_i^2 = 32.29\Omega$ at 150kHz and $Z_i^2 = 50\Omega$ at 30MHz.
For the impedance to ground when looking in the EUT-p connector with the mains open, we have

$$Z_i^3 = \frac{-j\omega^3 R_{P_2} C_{P_1} C_{P_2} L_P - \omega^2 \left(R_{P_1} R_{P_2} C_{P_1} C_{P_2} + C_{P_1} L_P \right) + j\omega \left(R_{P_1} C_{P_1} + R_{P_2} C_{P_2} \right) + 1}{-j\omega^3 C_{P_1} C_{P_2} L_P - \omega^2 \left(R_{P_2} C_{P_1} C_{P_2} + R_{P_2} C_{P_1} C_{P_2} \right) + j\omega \left(C_{P_1} + C_{P_2} \right)} \xrightarrow{\omega \gg 1} R_{P_2} = 50\Omega ,$$

and for the impedance to ground when looking across R_{P_2} we have

$$Z_i^4 = \frac{-j\omega^3 R_{P_2} C_{P_1} C_{P_2} L_P - \omega^2 R_{P_1} R_{P_2} C_{P_1} C_{P_2} + j\omega \left(R_{P_2} C_{P_1} + R_{P_2} C_{P_2} \right)}{-j\omega^3 C_{P_1} C_{P_2} L_P - \omega^2 \left(R_{P_2} C_{P_1} C_{P_2} + R_{P_2} C_{P_1} C_{P_2} \right) + j\omega \left(C_{P_1} + C_{P_2} \right)} \xrightarrow{\omega \gg 1} R_{P_2} = 50\Omega .$$

Since the measured signal is in the range of $-20\text{dB}\mu V = 0.1\mu V$ to $100\text{dB}\mu V = 0.1V$, special care must be taken to reduce influences not caused by the switched mode power supply. The hf disturbances which are already on the mains are attenuated by the input inductor and the capacitor to ground. The $50\mu H$ inductor combined with the $10\mu F$ capacitor to ground are preventing disturbances of the switched mode power supply to be injected in the mains.

The voltages measured with this LISN are limited for Class B equipment to the levels stated in Table (6.1).

Frequency [MHz]	*Quasi Peak* [dBμV]	*Average* [dBμV]
0.15-0.5	66-56	56-46
0.5-5	56	46
5-30	60	50

Table (6.1) Limits of conducted noise

6.2 Sources of EMI disturbances

Several effects are causing EMI disturbances. Differential mode currents are mainly produced by the current through ESR of the input capacitor. The switching character of the current through this capacitor is causing voltage spikes across the ESR and can be measured by the $\text{dB}\mu V$ meter.

The main part of the common mode current is produced due to the voltage difference across the cross talk capacitor between the primary and secondary side. A change in the construction of the transformer, which results in a reduce of the voltage across the capacitance, reduces these disturbances as shown in Fig. (6.2).

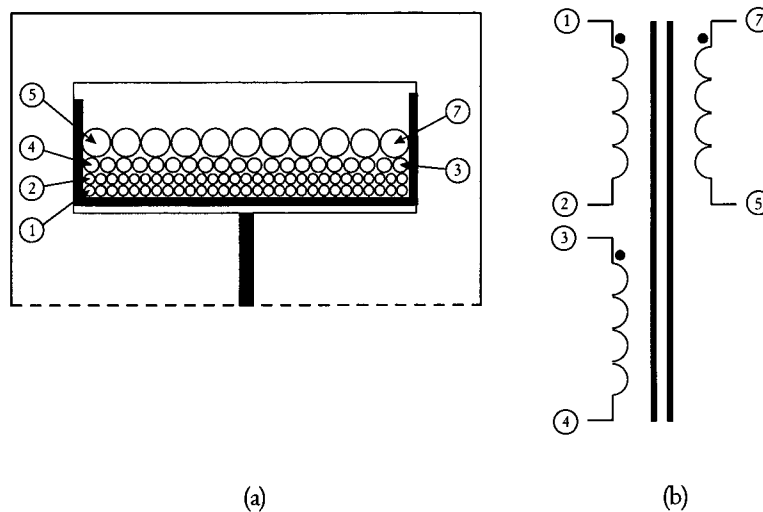(a)   (b)

Fig. (6.2) (a) Layout of the transformer (b) electrical connections

Using this construction we use the bias winding as a shield between primary and secondary side. Important is that the two grounds, points ③ and ⑦, are at the same side of the bobbin. For the capacitance between the secondary and bias winding we have

$$i_{C_{bs}} = C_{bs} \frac{dV_{bs}}{dt}.$$

This current, $i_{C_{bs}}$, will be decrease if the voltage difference between the bias and secondary windings is low. A Y-capacitor will create a short circuit for the remaining common mode current.

Concerning the printer circuit board layout we have tried to reduce capacitive coupling with the environment in order to reduce common mode currents. This is done by reducing the copper area of planes and wires. Magnetic coupling is reduced by reducing loop areas, especially the loops input capacitor, VIPer20, transformer and transformer, secondary diode, secondary capacitor and the loop diode bridge, input capacitor. See Fig. (3.16) for the final printed circuit board layout.

6.3 Measurements

The vector sum of the common and differential mode currents is measured using the LISN as described before. The converter was operating at maximum load. The results are given in Fig. (6.3).

(a)   (b)
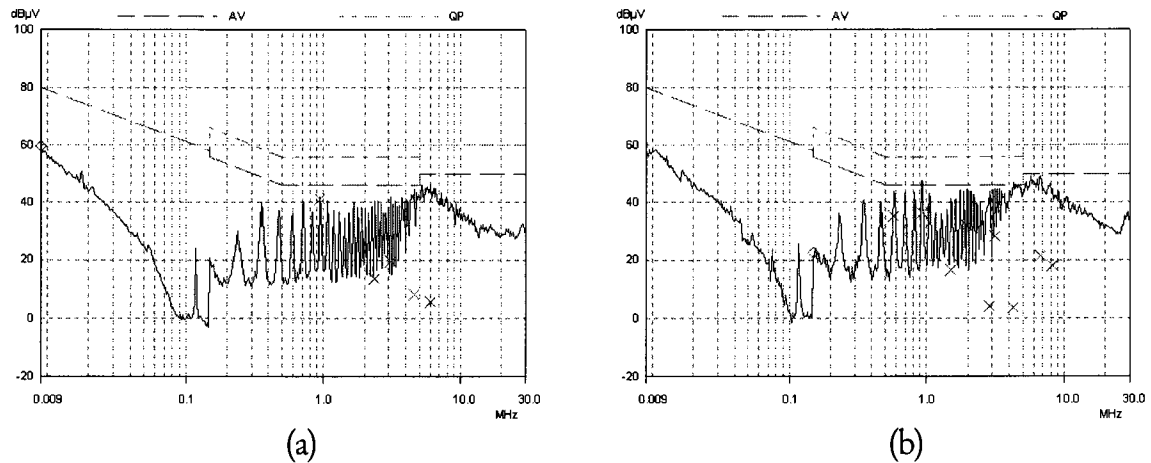
Fig. (6.3) EMI measurements (a) at $V_{DC} = 110V$ *and (b) at* $V_{DC} = 230V$

The switching frequency at 125kHz is clearly present in the spectrum. The rise in amplitude around 1MHz and 6MHz is a result of the ringing of L_p , L_σ and C_p, as shown in Fig. (6.4).
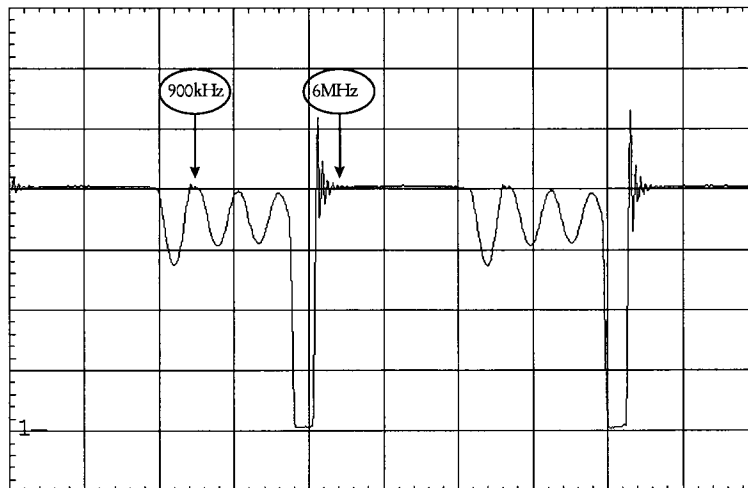
Fig. (6.4) A typical drain-source voltage showing the low and high frequency ringing

From Fig. (6.3) we can conclude that the expected EMI problems failed to occur. The battery charger met the EMI specifications at both the input voltages

7. Measurements

In this Chapter some general measurement are done to check the working of the power supply and if the targets as stated in the introduction are met.

7.1 Load Curve

We measured V_o versus I_o at $V_{AC} = 110\text{V}$ and $V_{AC} = 230\text{V}$ as listed in Table (7.1) and depicted in Fig. (7.1).

$V_{AC} = 110\text{V}$		$V_{AC} = 230\text{V}$	
$I_o[\text{mA}]$	$V_o[\text{V}]$	$I_o[\text{mA}]$	$V_o[\text{V}]$
50	6.574	50	6.576
276	6.574	390	6.575
362	6.573	499	6.574
480	6.573	680	6.574
563	6.573	740	6.573
715	6.572	767	6.573
797	6.570	800	6.565
802	6.499	801	6.505
803	6.405	807	6.279
812	6.008	813	6.009
817	5.518	819	5.510
820	5.015	821	4.984
821	4.560	823	4.498
823	4.075	827	3.993
827	3.569	833	3.523
829	2.919	841	2.874

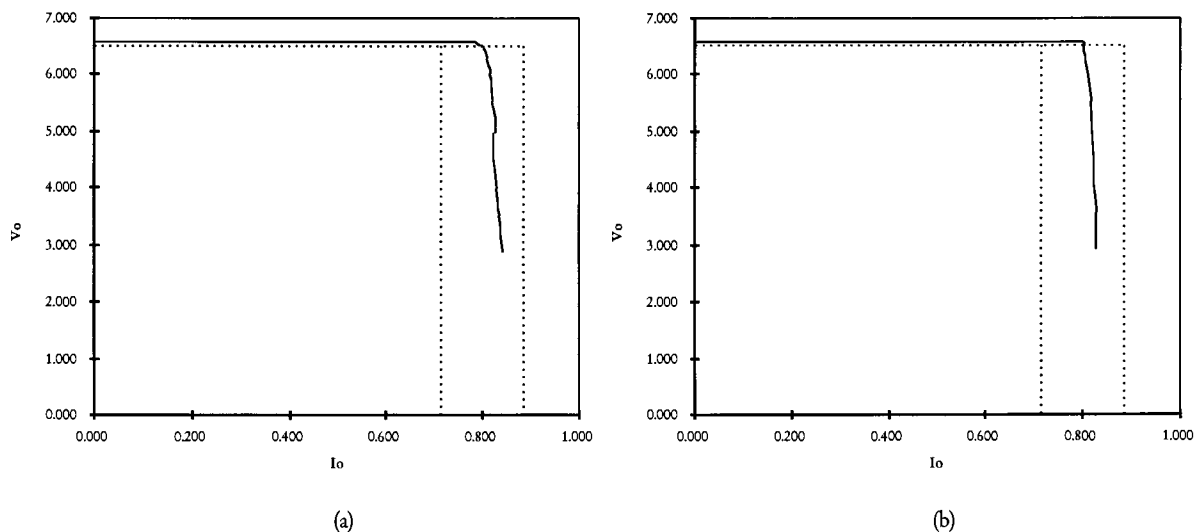*Table (7.1) Measured output current and voltage.*

Fig. (7.1) V_o versus I_o at $V_{AC} = 110\text{V}$ and $V_{AC} = 230\text{V}$.

From Table (7.1) we have that the maximum voltage error is 74mV which is below the expected level of 425mV . The output current is within it's limits of ±10% as denoted by the dotted lines in Table (7.1).

7.2 Switching Frequency

The minimum and maximum switching frequency are both measured. For the minimum switching frequency we have $I_o = 51\text{mA}$ and $V_o = 6.51\text{V}$ resulting in $P_o = 332\text{mW}$. Using a oscilloscope we measured $\delta_p = 0.9\%$ and $f_s = 29\text{kHz}$. The theoretical calculated value in this working condition can be calculated using

$$f_s^{\min} = \frac{V_{DC}^2 \delta_p^2 \eta}{2 P_o L_p} = \frac{(375\text{V})^2 \cdot 0.009^2 \cdot 0.8}{2 \cdot 332\text{mW} \cdot 458.64\,\mu\text{H}} = 30.02\text{kHz}.$$

From this we have that the actual switching frequency is 3.40% to low. For the maximum frequency it doesn't really matter which input voltage we apply since the frequency will not influence the switching frequency at maximum load. The output conditions are $I_o = 780\text{mA}$ and $V_o = 6.33\text{V}$ resulting in $P_o = 4.96\text{W}$. Again using an oscilloscope we measured $\delta_p = 7\%$ and $f_s = 113\text{kHz}$. The theoretical calculated value in this working condition can be calculated using

$$f_s^{\max} = \frac{V_{DC}^2 \delta_p^2 \eta}{2 P_o L_p} = \frac{(375\text{V})^2 \cdot 0.07^2 \cdot 0.8}{2 \cdot 4.96\text{mW} \cdot 458.64\,\mu\text{H}} = 121.16\text{kHz}.$$

From this we have that the actual switching frequency is 6.73% to low.

7.3 Stand-by Power

We measured the input current and voltage at no output load in order to obtain the stand-by power. The results are depicted in Table (7.2).

$V_{AC}[\text{V}]$	$I_{AC}[\text{mA}]$	$P_{STB}[\text{mW}]$
110	7	770
230	3	700

Table (7.2) Results of the stand-by power measurements

7.4 Load Regulation

$V_{AC}[\text{V}]$	$I_o[\text{mA}]$	$V_o[\text{V}]$	$P_o[\text{W}]$
258	802	6.41	5.14
231	800	6.39	5.11
200	799	6.38	5.10
171	797	6.38	5.08
140	794	6.34	5.03
110	792	6.32	5.01
85	791	6.31	4.99

Table (7.3) Output power as function of the input voltage

Using some linear regression we have $P_o = 4.917 + 8.739 \cdot 10^{-4} V_{AC}$, which is valid for $85\text{V} \le V_{AC} \le 258\text{V}$. From Table (7.3) we have a load regulation of 1.6% .
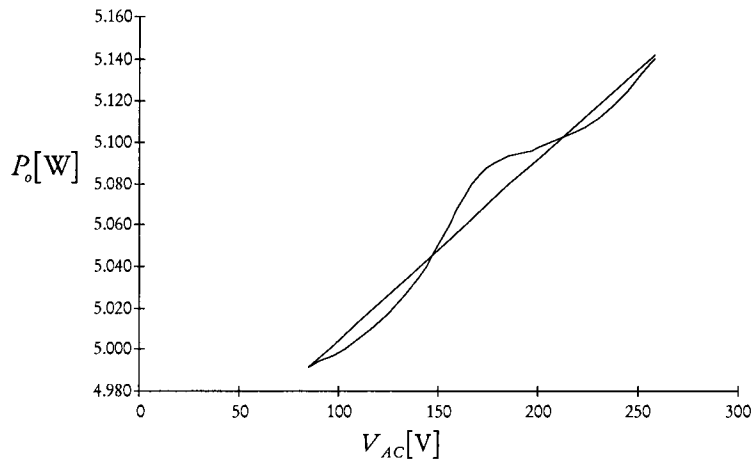
Fig. (7.2) Measured and calculated load regulation

7.5 Temperature Dependent Measurements

The following V_o versus I_o measurements are done at different ambient temperatures form $-5°C$ up to $85°C$ without casing at $V_{AC} = 110V$ and $V_{AC} = 230V$. The results are depicted in Fig. (7.3).

(a)   (b)
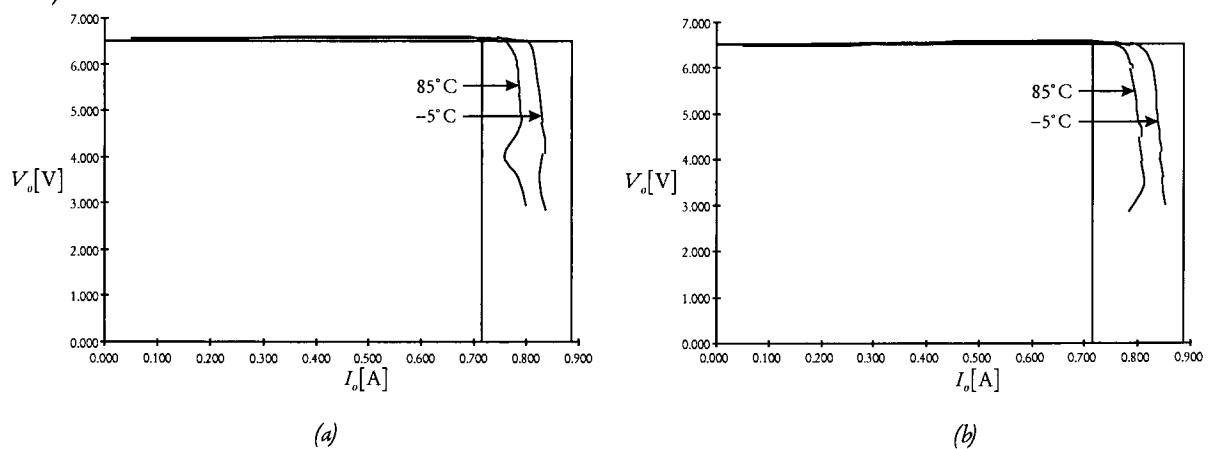
Fig. (7.3) Measured V_o versus I_o curves at (a) 110V and (b). 230V

The vertical lines denote the allowed tolerance in the current regulation and as will be clear, the curves are within the allowed area. An output voltage of $3V$ is guaranteed as shown in Fig. (7.3).

We also measured the temperature of the transformer when the converter is in a 30cc casing. For the results see Table (7.4)

$V_o[V]$	$I_o[mA]$	$T_{amb}[°C]$	$T_{transformer}[°C]$
6.51	796	45	93
6.57	799	50	98
6.54	795	55	103
6.57	700	55	98

Table (7.4) Measured transformer temperature as function of the ambient temperature at maximum output power and $V_{AC} = 230V$.

7.6 Output Ripple and Noise

The maximum output voltage and current ripple are measured using a artificial battery as load.

Output voltage ripple and noise $[\mathrm{mV_{pk\text{-}pk}}]$	Output current ripple and noise $[\mathrm{mA_{pk\text{-}pk}}]$
< 65	< 10

Table (7.5) Maximum output voltage and current ripple

7.7 Short Circuit Output Current

The output current while short circuited is measured at $V_{AC} = 110\mathrm{V}$ and $V_{AC} = 230\mathrm{V}$. The results are depicted in Table (7.6).

$V_{AC}[\mathrm{V}]$	$I_o[\mathrm{mA}]$
110	196
230	394

Table (7.6) Measured short circuit output currents at $V_{AC} = 110\mathrm{V}$ and $V_{AC} = 230\mathrm{V}$

7.8 Electrical Volume

Since the transformer bobbin is hand made, it is 1.5mm bigger in height as necessary. We therefore calculated the electrical volume for the actual and a precisely fitting bobbin. See Table (7.7) for numerical results.

	length [mm]	depth [mm]	height [mm]	volume [cm³]
Actual bobbin	47.65	30.10	18.80	26.96
Perfect bobbin	47.65	30.10	17.30	24.81

Table (7.7) Electrical volume with different transformer bobbins

8. Conclusions and Recommendations

Regarding the VIPer20 several remarks can be made about the advantages and disadvantages. The adjustable frequency up to 200kHz is one of the advantages and is used to prevent the battery charger to operate in burst mode at high input voltages and low output loads. The switching frequency is measured at minimal output load and maximum input voltage. The measured switching frequency is 3.4% too low. At maximum output load we measured a switchinf frequency of 6.7% to low.

Another advantage of the VIPer20 is the undervoltage lockout, which is used to create the current foldback function. Measurements show that 3V output voltage is guaranteed in current regulation. Below 3V the current decreases to the short circuit current

Calculations and measurements show conformity in the high switching losses of the VIPer20. These losses are caused by the big drain-source capacitance of the MOSFet, since it can handle twice the needed output power. Considering this, a smaller MOSFet is appreciable.

The expected EMI problems caused by the electrical coupling between the drain and casing did not occur. The bi-layer printed circuit board with a earth plane at the top side, reduced the capacitive coupling with the environment effectively. The results of the EMI measurements were conform the EMI regulations.

Regarding the battery charger in general, several remarks can be made. Replacing the traditional output capacitor by a CLC-filter, build up with ceramic multilayer capacitors, results in a reduction of the electrical volume, while retaining a low output voltage ripple. The measured voltage ripple is in accordance with the specifications.

The calculated electrical efficiency of the battery charger is in accordance with the measured efficiency. The VIPer20 dissipates the most, especially at high input voltages due to the high switching losses. At low input voltages, the inrush current limiting resistor dissipates a lot, due to the increase of the RMS input current. The secondary diode dissipates a lot at all input voltages. At this point the bi-directional flyback converter holds the promise of yielding outstanding results.

The open loop gain and phase measurements in voltage and current regulation mode are in confirmation with the calculations. From this we can conclude that the calculated dynamic small signal (AC) models are representative for battery charger in both the operating modes.

We did not manage to remain within the 20cc electrical volume. Because of the handmade transformer bobbin we have an electrical volume of 27cc, which can be reduced to 25cc, if the transformer bobbin is machine-made. Nevertheless, the target of 20cc electrical volume is possible when using flying leads. This can be investigated in successive projects.

Despite of some interesting features of the VIPer20 it is not the best solution to be used in battery chargers. The nowadays increasing demand of very low standby losses ($\leq 100mW$) can not be answered when using a VIPer20. The high drain-source capacitance is inevitable when using a VIPer20. The idea, as represented, of switching frequency reduction is interesting, also for reducing the switching losses. A possible implementation as a feature in VIPer20 alike integrated flyback solutions should be considered.

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Appendix A Fourier Transform of a Triangular Shaped Signal

The primary and secondary currents are triangular shaped with death times in between and therefore we can not apply basic network theory. To avoid this problem, we use a Fourier transform with respect to time to decompose the signal in it's harmonic contents. The primary and secondary currents are depicted in Fig. (A.1).
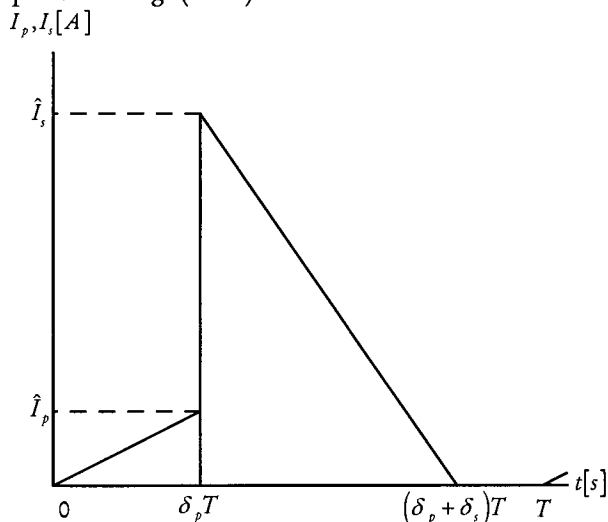

$I_p, I_s [A]$

Fig. (A.1) The ideal primary and secondary current.

The functions of the primary and secondary currents in time domain can be written as

$$I_p(t) = \begin{cases} \hat{I}_p \dfrac{t}{\delta_p T} & \text{if } 0 \le t \le \delta_p T \\ 0 & \text{if } \delta_p T < t < T \end{cases},$$

$$I_s(t) = \begin{cases} \hat{I}_p \left(1 - \dfrac{t}{\delta_s T}\right) & \text{if } \delta_p T \le t \le (\delta_p + \delta_s) T \\ 0 & \text{if } 0 < t < \delta_p T \wedge (\delta_p + \delta_s) T < t < T \end{cases}.$$

The primary current can be written using it's Fourier coefficients

$$I_p(t) = a_0^p + \sum_{n=1}^{m} a_n^p \cos\left(\frac{2\pi n t}{T}\right) + b_n^p \sin\left(\frac{2\pi n t}{T}\right),$$

$$a_0^p = \frac{1}{T} \int_0^{\delta_p T} \hat{I}_p \frac{\tau}{\delta_p T} d\tau,$$

$$a_n^p = \frac{2}{T} \int_0^{\delta_p T} \hat{I}_p \frac{\tau}{\delta_p T} \cos\left(\frac{2\pi n \tau}{T}\right) d\tau,$$

$$b_n^p = \frac{2}{T} \int_0^{\delta_p T} \hat{I}_p \frac{\tau}{\delta_p T} \sin\left(\frac{2\pi n \tau}{T}\right) d\tau,$$

and similar we can write for the secondary current

$$I_s(t) = a_0^s + \sum_{n=1}^{m} a_n^s \cos\left(\frac{2\pi n t}{T}\right) + b_n^s \sin\left(\frac{2\pi n t}{T}\right),$$

$$a_0^s = \frac{1}{T} \int_0^{\delta_s T} \hat{I}_s\left(1 - \frac{\tau}{\delta_s T}\right) d\tau,$$

$$a_n^s = \frac{2}{T} \int_0^{\delta_s T} \hat{I}_s\left(1 - \frac{\tau}{\delta_s T}\right) \cos\left(\frac{2\pi n \tau}{T}\right) d\tau,$$

$$b_n^s = \frac{2}{T} \int_0^{\delta_s T} \hat{I}_s\left(1 - \frac{\tau}{\delta_s T}\right) \sin\left(\frac{2\pi n \tau}{T}\right) d\tau.$$

Evaluating the integrals results in

$$a_0^p = \frac{1}{2} \hat{I}_p \delta_p,$$

$$a_n^p = \hat{I}_p \frac{\cos(2n\pi\delta_p) + 2n\pi\delta_p \sin(2n\pi\delta_p) - 1}{2n^2\pi^2\delta_p},$$

$$b_n^p = \hat{I}_p \frac{\sin(2n\pi\delta_p) - 2n\pi\delta_p \cos(2n\pi\delta_p)}{2n^2\pi^2\delta_p},$$

and for the secondary current

$$a_0^s = \frac{1}{2} \hat{I}_s \delta_s,$$

$$a_n^s = \hat{I}_s \frac{1 - \cos(2n\pi\delta_s)}{2n^2\pi^2\delta_s},$$

$$b_n^s = \hat{I}_s \frac{2n\pi\delta_s - \sin(2n\pi\delta_s)}{2n^2\pi^2\delta_s}.$$

As a check we printed the composed currents I_p and I_s in Fig. (A.2). Since we are using the signals separately, the shift in time of the secondary current is not causing any problems.
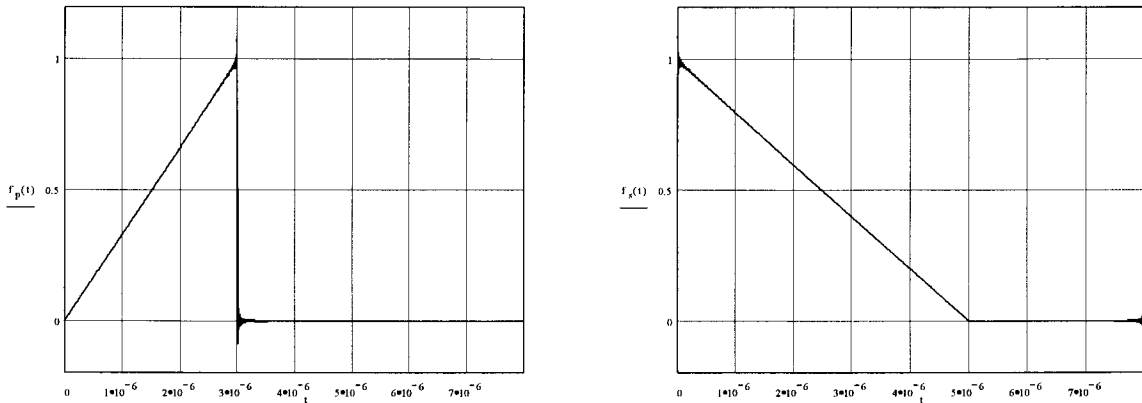

Fig. (.A.2) The primary and secondary current after inverse Fourier transform (n = 500).

Appendix B Circuit Diagram

Appendix C Bidirectional Flyback Converter

In this chapter a novel type of flyback converter, the bidirectional flyback converter, will be presented.

1 Working of Operation

The bi-directional flyback converter, as depicted in Fig. (C.1), shows similarities with the conventional flyback converter. The only difference is that we are using energy, which is present at the secondary side, to discharge the drain-source capacitor of the primary MOSFet in order to obtain zero voltage switching. The same is applied to the secondary MOSFet by using energy of the primary side. We will now explain one complete switching cycle of the converter in stationary state, which is seperated in 4 stages. Some typical wave forms are depicted in Fig. (C.2).
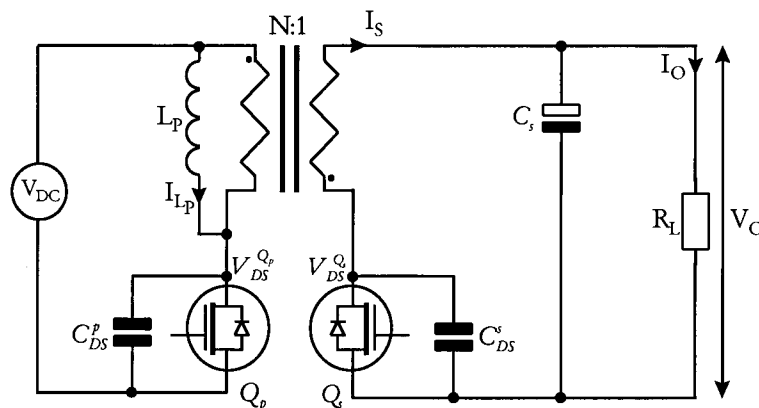

Fig (C.1) Schematic circuit of the bi-directional flyback converter

Stage 1 $\left[0 \leq t < \delta_1 T\right]$:

In this interval the primary MOSFet is "on" and the secondary MOSFet is "off", resulting in an linear increasing primary current I_p, since the primary inductance is connected to a constant voltage source, V_{DC}. Electrical energy is converted to magnetic energy and stored in the airgap of the transformer. This interval is similar to the first interval of a conventional flyback converter. At $t = \delta_1 T$ the primary MOSFet is switched "off".

Stage 2 $\left[\delta_1 T \leq t < \delta_2 T\right]$:

Since the magnetic flux in the transformer core can not decrease abruptly, I_s is initiated. This current is able to flow because of drain source capacitor in the secondary MOSFet. We can make use of this current since it discharges the capacitor, C_{DS}^Q, resulting in a decreasing drain source voltage of the secondary MOSFet. By just waiting long enough, the body diode will start conducting and we are more or less able to switch at zero voltage, resulting in less switching losses in the secondary MOSFet. The secondary MOSFet will be "on" at $t = \delta_2 T$. This interval is not present using a conventional flyback converter.

Stage 3 $\left[\delta_2 T \leq t < \delta_3 T\right]$:

The first part of this interval has similarities with a conventional flyback converter. During the first part of this interval the remaining part of the energy is transferred to the output load and the secondary capacitor, resulting in a decreasing secondary current. At a certain point in time the secondary current reverses sign and becomes negative resulting in a flow of energy from the

capacitor to the transformer. When to switch the secondary MOSFet "off" depends on the control strategy and will be discussed below. The secondary MOSFet will be "off" at $t = \delta_3 T$.

Stage 4 $[\delta_3 T \le t < T]$:

Since there is magnetic energy in the airgap of the transformer, a negative primary current will flow using the drain source capacitor off the primary MOSFet. This results in a decreasing drain source voltage, since $C_{DS}^{Q_p}$ is discharged. At a certain point the body diode of the primary MOSFet will start to conduct and again we can switch the MOSFet "on" at more or less zero voltage. This interval is also not present in a conventional flyback converter.
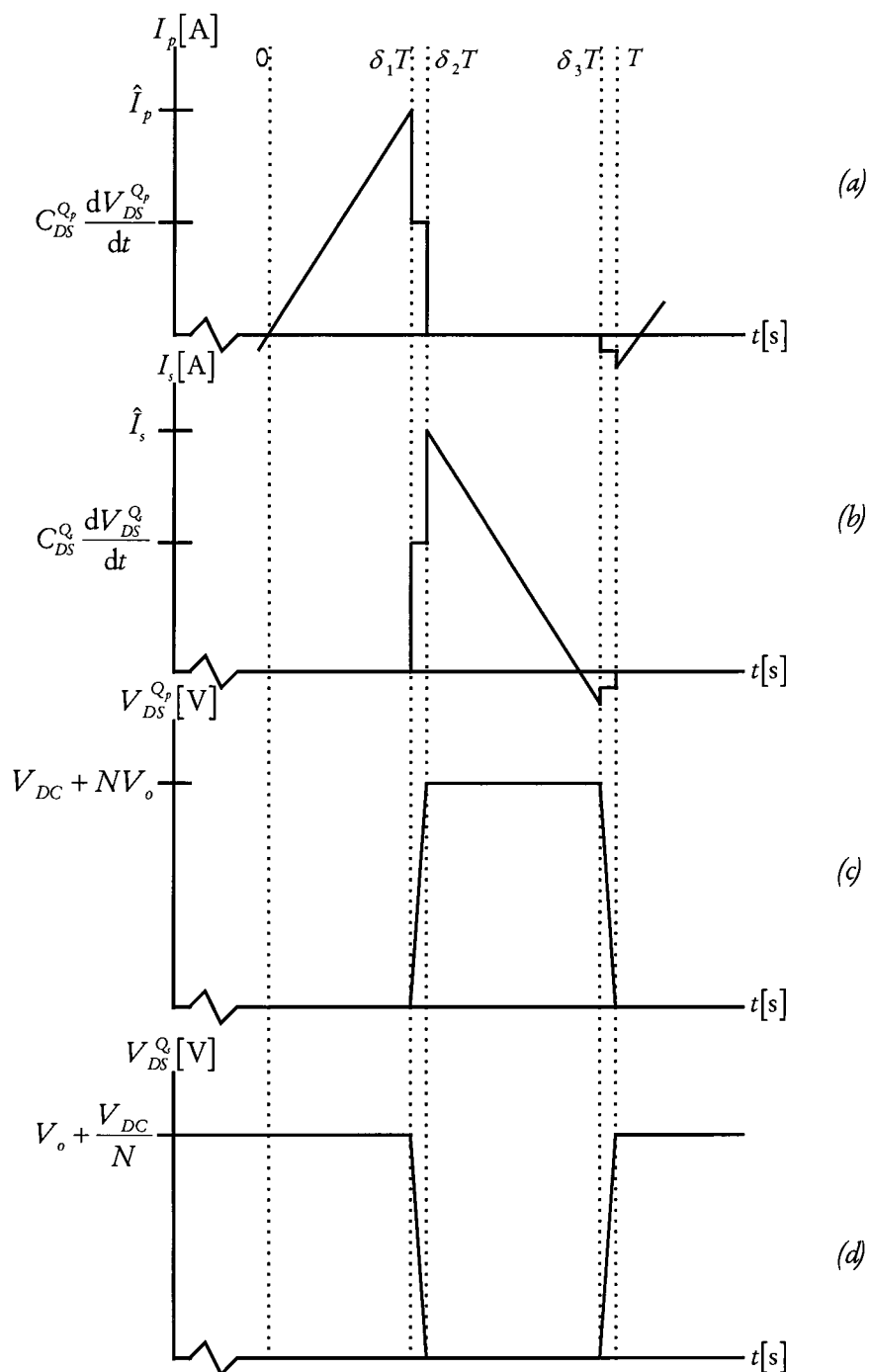

Fig. (C.2) Typical currents and voltages of a bi-directional flyback converter

2 Control Strategy

We will consider a possible control strategy, resulting in a variable switching frequency. If we use variable switching frequency then the secondary on time is constant and the primary on time is controlled by the reflected energy and the input voltage. The control strategy is to give the secondary a constant "on" time. In illustration of this see Fig. (C.3), which shows three different situations. Using this type of control the secondary side acts like a partly reflecting energy mirror. The more energy is transferred to the secondary side, the more energy will be reflected beck to the primary side. This reflected energy is measured at the primary side by measuring the drain source voltage of the primary MOSFet. If this drain source voltage is to high then there should be more energy reflected and therefore the primary "on" time will be increased. Since this converter is working at the boundary of continuous and discontinuous mode the change in primary "on" time causes a change in the switching frequency. Since the power supplies are used as battery chargers a voltage and current regulation circuit needs to be implemented. One way to achieve this is to make the secondary "on" time a function of the output power $P_o = V_o I_o$, which is not constant during one charging cycle of a battery as explained in the introduction of this report. Where normally the information of the current and voltage control circuits control an optocoupler current, we now use this information to control the secondary "on" time. As will be clear the switching frequency is now a function of the output power and therefore not constant.
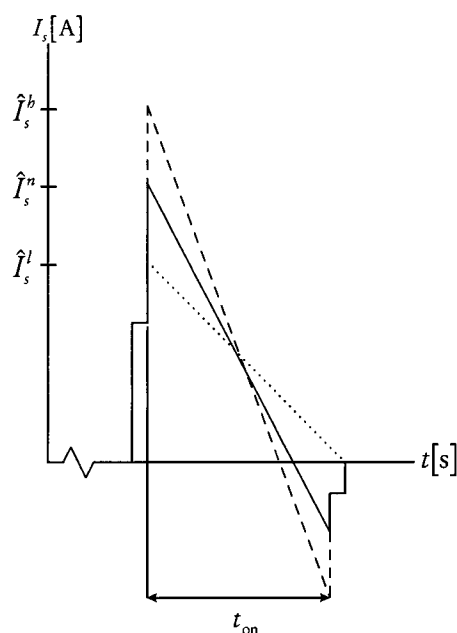

Fig. (C.3) Secondary current with variable frequency control. The dashed curve represents a situation when to much energy is transferred back to the primary side, the dotted curve represents a situation when there is no energy transferred to the primary side and the solid curve represents a situation when there is exactly enough energy is transferred to the primary side.