Single switch regulating ballast topologies

a circuit capable of dimming a fluorescent lamp while maintaining low input current distortion

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SUMMARY

This report describes the results of my graduation project at Philips Lighting Eindhoven via the Eindhoven University of Technology. The report describes the investigation of potential single switch regulating ballast topologies for lighting applications. Many prior art electronic ballasts that perform both power factor correction and inverter functionality include two or more power switches (in the form of transistors). Because the cost of transistors is relatively high, reducing the number of transistors may have a significant effect on the cost of the ballast.

The investigated ballasts fulfil the IEC 1000-3-2 class C requirements concerning line current harmonic distortion. The ultimate goal of this report is to demonstrate that (dimmable) single switch ballasts have the potential to be small and cost effective and can compete with the present ballasts, like the up-converter/half-bridge topologies.

In the literature six interesting single switch ballasts were found. Through analysis of a series- and a parallel resonant soft-switching ballast topology it has been proved that these type of circuits are not very attractive as a ballast. Both ballasts strongly depend on their load (lamp resistance), are not suitable for light dimming, and may suffer from high voltage stress on the power switch (> 3x peak mains voltage).

Analysis, simulation, design rules and experimental results are given of a small and cost effective ballast. The ballast drives a TL-5 49W lamp from the mains (230V~), is capable of high power factor (0.99), low THD (12%) and high efficiency (87%). The voltage stress on the power switch (V_{dss}=800V) is twice the peak mains voltage under nominal operation. The operating frequency of the ballast is 50kHz. The lamp current is sinusoidal and the lamp power can be controlled through PWM (1%). Drawbacks of the circuit build are the (excessive) power dissipation in the power switch (3 - 4W), due to hard switching, and the voltage increase across the switch when the lamp is dimmed to a (very) low level. Nevertheless, the circuit offers good performance and proves to be small and cost effective.

Referring to the single switch ballasts found in literature; single switch ballasts require more magnetic components (in the form of inductors) than the present ballasts but less silicon is used. Compared to up-converter/half-bridge topologies a high-voltage IC and a switch (half-bridge) is exchanged with a high-voltage/high-current switch. Also a switch (half-bridge) is exchanged with an inductor.

Further investigation of the single switch ballast and/or other single switch ballasts is recommended since not all possibilities have been exploited.

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APPENDICES

1. INTRODUCTION

In the literature some interesting papers about single switch converters for lighting applications were found. Single switch converters have an opportunity to be small and cost effective. Many prior art electronic ballasts that perform both power factor correction and inverter functionality include two or more power switches. Because the cost of transistors is relatively high, reducing the number of transistors may have a significant effect on the cost of the ballast.

In the past different class-E converters (single switch) have been investigated at Dev. L.E. Ehv. Most of these converters had the disadvantage of high voltage across the power semiconductor switch, 3 - 4 times $\hat{u}_{mains}$. High voltage semiconductor switches are relatively expensive. The new presented converters show a lower voltage stress on the power switch, 1.5 - 2.5 times $\hat{u}_{mains}$. This led to the assignment of my graduation project via the Eindhoven University of Technology at Philips Lighting.

The assignment holds a study of literature and an investigation of the single switch regulating ballast topologies. The investigated ballasts should fulfil the IEC 1000-3-2 class C requirements concerning line current harmonic distortion. One potential topology is selected for tight investigation and experimental results. The ultimate goal of this project is to demonstrate that (dimmable) single switch ballasts have the potential to be small and cost effective and that they can compete with the present ballasts, like the up-converter/half-bridge topologies.

2. INTRODUCTION TO ELECTRONIC BALLASTS

Fluorescent lamps cannot be connected directly to the mains. As they have a negative impedance they need a so-called ballast to limit the current. The ballast should produce high voltage on the cold lamp, create some degree of ionization and then limit the current of the hot lamp.

Magnetic ballasts present high size and weight, flickering, poor regulation and low power factor. Electronic ballasts overcome these problems and increase the efficiency. Moreover, when the lamp is driven with high frequency currents higher light output for the same electrical input is obtained. Intelligent electronic ballasts, featuring movement detection and daylight control (dimming of the fluorescent lamp), offer an efficiency improvement of 70%. The main drawback of electronic ballasts is their higher initial cost with respect to magnetic ballasts although the energy saving achieved with electronic ballasts makes them more economic in the long run.

International regulatory standards such as IEC 1000-3-2 impose restrictions on the harmonic components of the line current and the circuit power factor of lighting equipment. The current drawn from the mains has to meet the requirements given in table 2-1.

Table 2-1: Maximum permissible harmonics of supply current ref. IEC 1000-3-2 class C

Harmonic order n	Maximum permissible harmonic in %
2	2
3	30*pf
5	10
7	7
9	5
11	3
13	2

Typical electronic ballasts consist of a pre-conditioner (power factor controller) to achieve a high power factor and a dc-ac converter for the high frequency supply to the lamp, figure 2-1. The pre-conditioner is usually an up-converter operating in discontinuous current mode and the dc-ac inverter is usually based on a half-bridge topology.

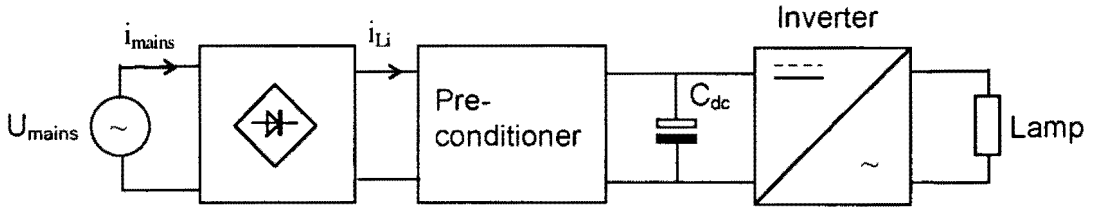


Figure 2-1: Typical two stage electronic ballast

The up-converter is controlled in a way that the current drawn from the mains looks like that of Figure 2-2.

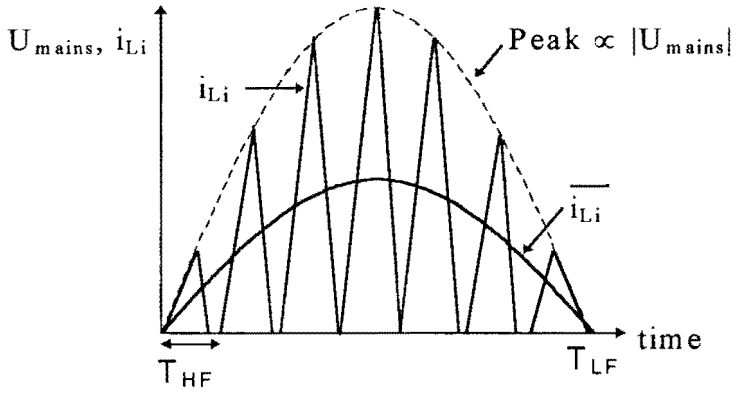


Figure 2-2: Mains voltage and current of a pre-conditioner

The up-converter operates at a frequency much higher than the mains frequency. Current is drawn from the mains in a way that the average value of each high current pulse is proportional to the mains voltage. A sinusoidal mains current with a high power factor can be obtained by means of a low pass LC-filter. The up-converter as pre-conditioner is fully described in [3].

Disadvantages of two-stage ballasts are the extra circuitry needed for power factor correction and the reduced reliability due to extra components. Therefore other methods for power factor correction have been developed, like power feedback, where the power factor correction is integrated with the high frequency inverter [1,2].

Many prior art electronic ballasts that perform both power factor correction and inverter functionality include two or more power switches. Because the cost of transistors is relatively high, reducing the number of transistors may have a significant effect on the cost of the ballast. As another effort to reduce the cost of the ballast and miniaturisation, new ballasts have been developed based on a single switch, figure 2-3.

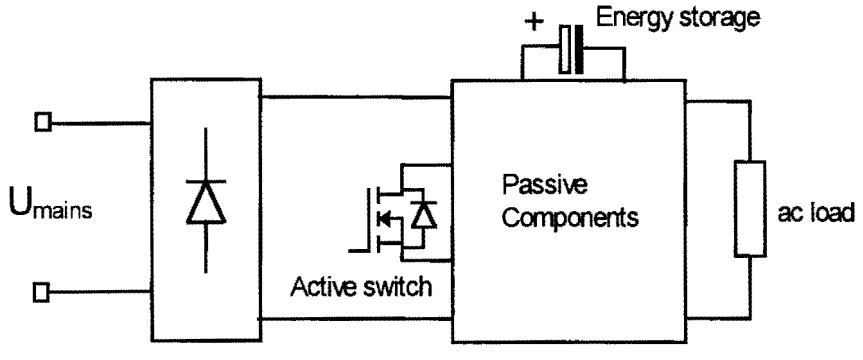


Figure 2-3: Structure of single switch unity power factor ballasts

A high input power factor requires the input side to emulate a resistor and the use of input current shaping means. The ballast must provide internal low frequency storage to prevent the lamp from being turned off each time the mains voltage reaches zero and to deliver a constant power to the lamp.

2.1 REFERENCES

[1] Chen, W. and F.C. Lee, T. Yamauchi; AN IMPROVED 'CHARGE PUMP' ELECTRONIC BALLAST WITH LOW THD AND LOW CREST FACTOR., Proc. In: Applied Power Electronics Conference, Vol. 2 (1996), p. 622-627.

[2] Heuvel, A. W. van den; ANALYSIS OF DOUBLE POWER FEEDBACK CIRCUITS BASED ON THE CHARGE PUMP MODEL., Report DLEE 4003/97.

[3] Rozenboom, J., Duarte, J.L, Smidt, P.J.M; MINI-VERMOGENSELEKTRONICA-VERMOGENSELEKTRONICA ONDER 2KW., Faculty of Electrical Engineering, Eindhoven University of Technology, 1995, p. 36-44 (DC-DC).

3. INVESTIGATION OF A SERIES- AND A PARALLEL RESONANT SOFT-SWITCHING TOPOLOGY

3.1 INTRODUCTION

Appendix A shows the bibliography, resulting from a study of literature, concerning single switch / stage ballasts. The ballasts found in literature are classified to potential ballast topologies. Table 3-1 gives an overview.

Table 3-1 Potential single switch ballast topologies		
	Topology	Ref. app. A
1	Series resonant soft-switching converter with LC tank circuit	[7], [24], [17]
2	Soft-switching class-E converter, fixed duty cycle control	[27]
3	Buck-boost automatic current shaper combined with class-E conv.	[15]
4	Flyback converter combined with push-pull converter	[18]
5	Electronic ballast employing coupled inductors for energy storage and voltage clamp with parallel resonant load	[3], [5], [6] [28]
6	Electronic ballast employing coupled inductors for energy storage and voltage clamp with series resonant load	[4]

The topologies mentioned in table 3-1 are shown in figure 3-1 up to figure 3-6.

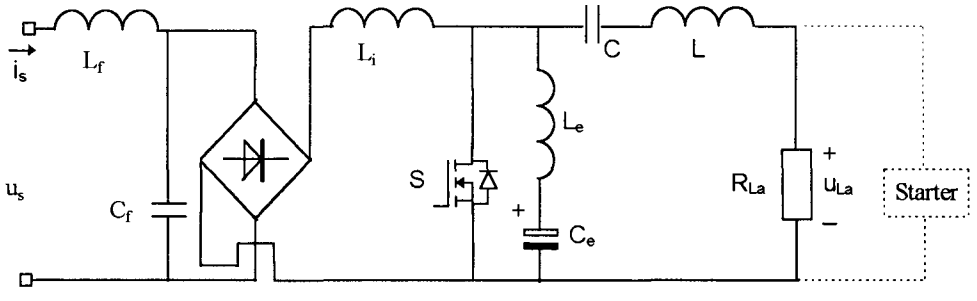


Figure 3-1 Series resonant soft-switching converter with LC tank circuit

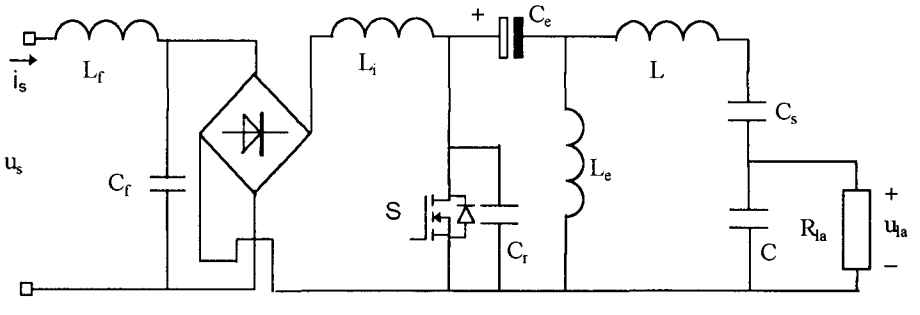


Figure 3-2 Soft-switching class-E converter, fixed duty cycle control

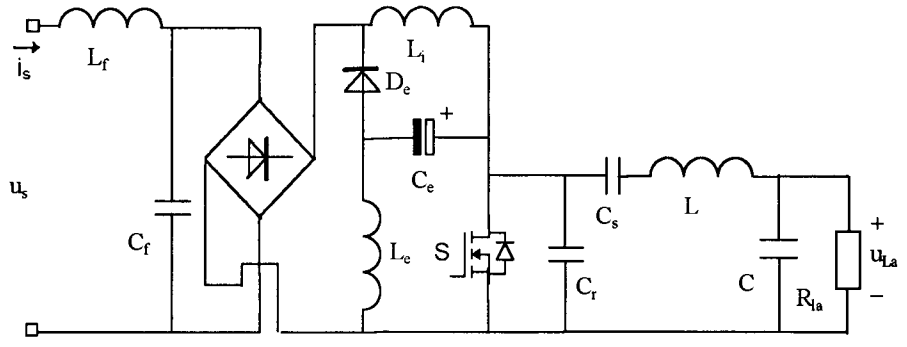


Figure 3-3 Buck-boost automatic current shaper combined with class-E converter

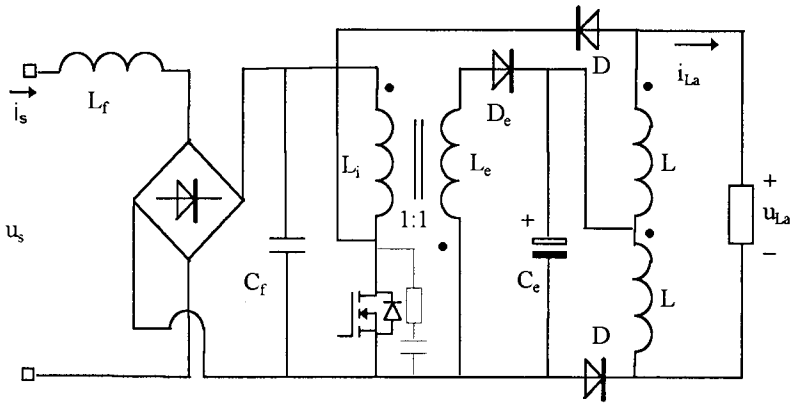


Figure 3-4 Flyback converter combined with push-pull converter

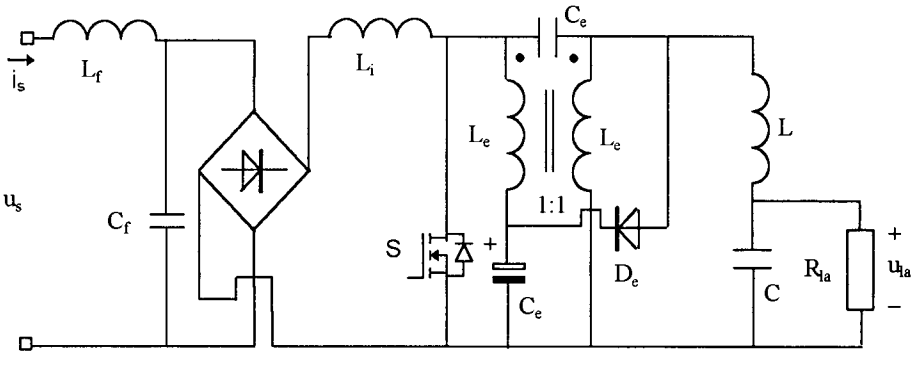


Figure 3-5 Electronic ballast employing coupled inductors for energy storage and voltage clamp with parallel resonant load

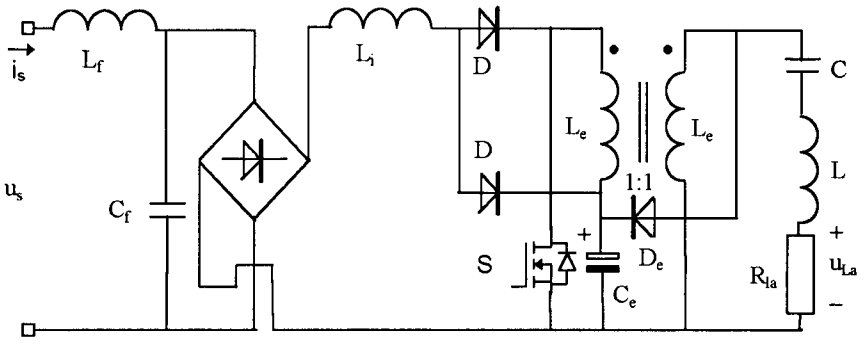


Figure 3-6 Electronic ballast employing coupled inductors for energy storage and voltage clamp with series resonant load

Figure 3-1 up to figure 3-6 show some important similarities. For example, each topology has an input EMI filter (L_f,C_f) and an energy storage circuit (C_e, L_e, D_e). The energy storage circuit prevents the lamp from being turned off each time the mains voltage reaches zero. Each topology consists of an input inductor (L_i) operating in discontinuous current mode for high frequency energy transfer and high power factor. The switch of each topology can be controlled with a low cost driver circuit; no level shifters are needed. Furthermore, the output circuit consisting of (L, C, C_s, R_{la}) is often a series resonant circuit or a parallel resonant circuit or a combination of both.

Referring to the reference's of the topology concerned; Topology 1, 2, and 3 have the advantage of providing soft switching to the power switch but they also show the highest voltage stress on the power switch and are not suitable for light dimming. Using topology 1 it may not be possible or rather difficult to maintain a low lamp current crest factor, also additional circuitry is needed to start the lamp.

The magnetics of topology 4 are rather large (two EE 42 cores). The lamp voltage is square wave, which leads to higher harmonics in the lamp current, resulting in unacceptable EMI[1]. Furthermore a very large high voltage capacitor is needed to create the voltage source for the push-pull configuration (C_e=220uF/250V, u_s=127V).

Topology 5 and 6 show the best performance. The maximum voltage stress on the power switch, at full load, is less than twice the mains voltage peak and the lamp current is sinusoidal. Both topologies are suitable for light dimming. A significant difference between topology 5 and topology 6 is that topology 5 has a parallel resonant output circuit and topology 6 a series resonant output circuit.

[1] Because the lamp is installed in the open, the amount of radiated EMI depends on the amount of harmonics contained in the lamp current. A sinewave is an ideal waveform for the lamp current in that it both has a low crest factor and acceptable EMI.

3.2 SERIES RESONANT SOFT-SWITCHING TOPOLOGY

As a result of the topologies presented in paragraph 3.1 a series resonant soft-switching topology is investigated. Figure 3-7 shows the series resonant soft-switching topology, appendix A [7].

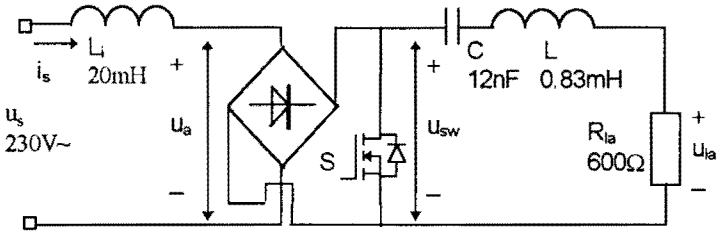


Figure 3-7 Series resonant soft-switching converter

Inductor L_i may operate in continuous or discontinuous current mode, depending on its inductance. The basic operation of the circuit, however, does not depend on the input current mode.

High frequency operation:

Two operating modes occur during a switching period, depending on the switch status. Figure 3-8 shows the two modes.

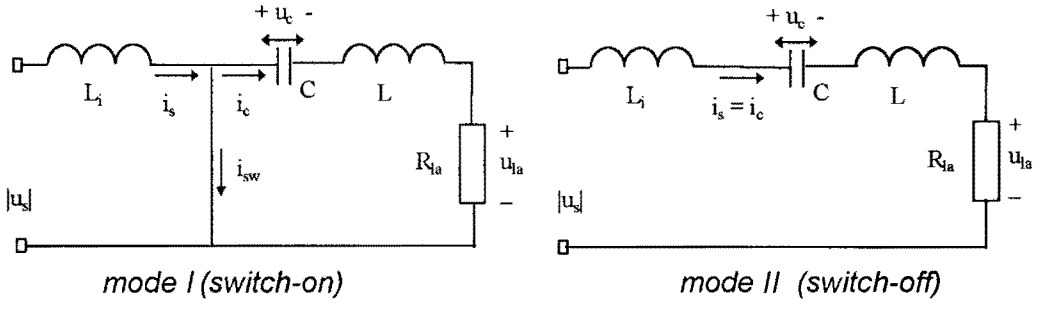
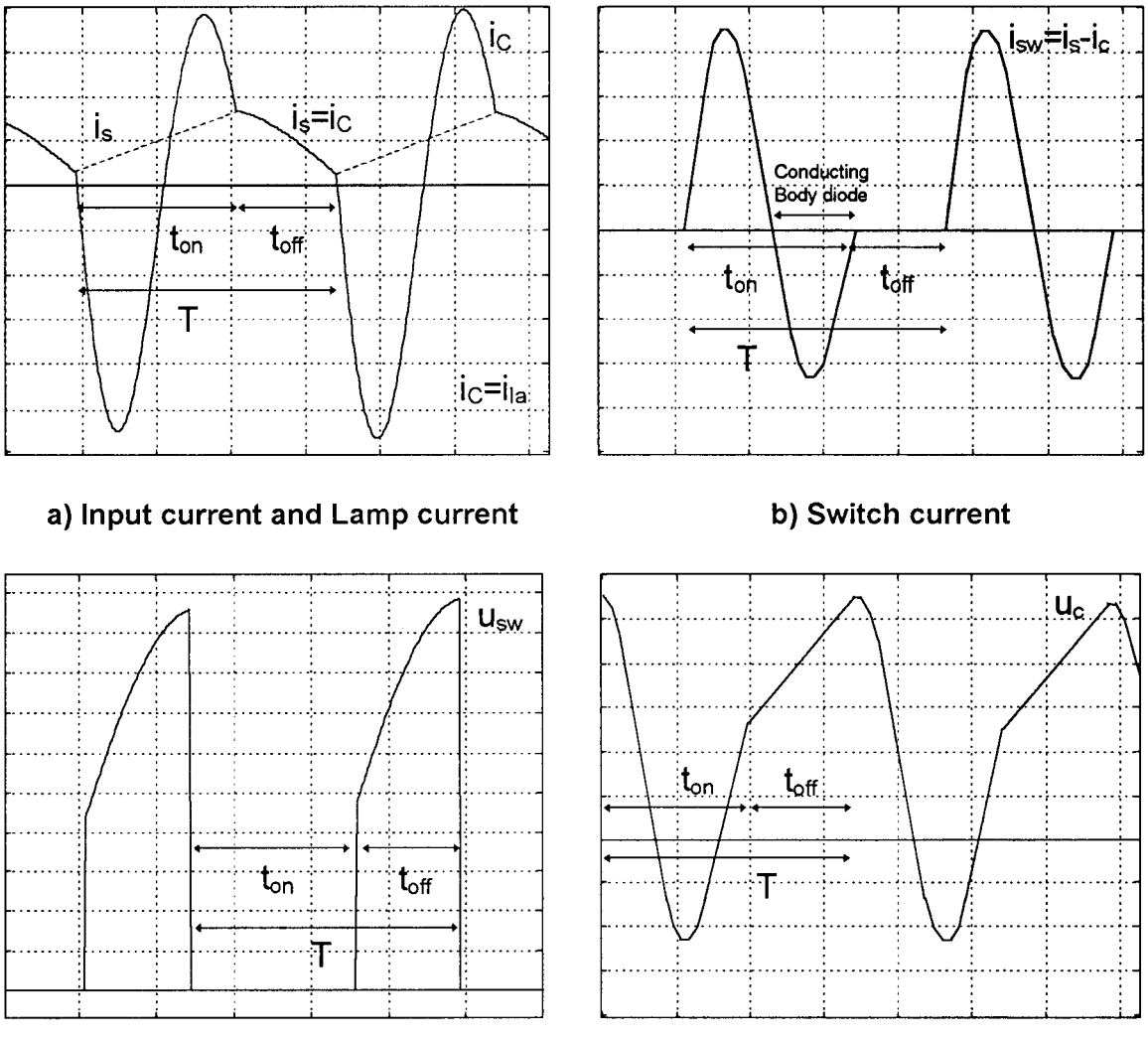


Figure 3-8 Switched circuits of the series resonant soft-switching converter

When the switch is turned on mode I is applied. Current i_s increases linearly under the action of supply voltage $|u_s|$, which is entirely applied to inductor L_i. Turning the switch on also causes an oscillation of the resonant path (L,C) whose current and capacitor voltage behave as sinusoidal waveforms, figure 3-9ad. The switch current i_{sw} is initially positive but, due to the resonance, reverses at a certain time. A soft current transfer from the switch into the body diode occurs, followed by a current reversal, figure 3-9b. During conduction of the body diode the switch can be gated off at zero voltage.

When the body diode ends conduction, mode II is applied. Current i_s flows into the resonant path, whose oscillation frequency is determined by the series of L_i, L and C. With L_i » L the oscillation frequency of the circuit drops, accordingly the behaviour of current i_s and capacitor voltage u_c becomes nearly linear in function of time, figure 3-9ad.



a) Input current and Lamp current

b) Switch current

c) Switch voltage

d) Capacitor voltage

Figure 3-9 High frequency waveforms

Since the resonance frequency of a series resonance circuit is independent of the lamp resistance, the on-time of the switch is given by $t_{on} \approx T_o = 2\pi.\sqrt{(LC)}$. The off-time of the switch is determined by the constant switching frequency and the fixed on-time of the switch.

A derivation of the high frequency currents and voltages, as well as the maximum switch voltage can be found in appendix B. The currents and voltages of the circuit in function of time are derived using state-space analysis and laplace transforms.

Low frequency operation:

For analysis of the low frequency operation only the positive half of the mains voltage is considered. The low frequency operation is shown in figure 3-10. The waveforms are obtained with; $u_s=325.\sin(2\pi 1000.t)$ and $f_{switch}=28.5kHz$; $d=0.34$.

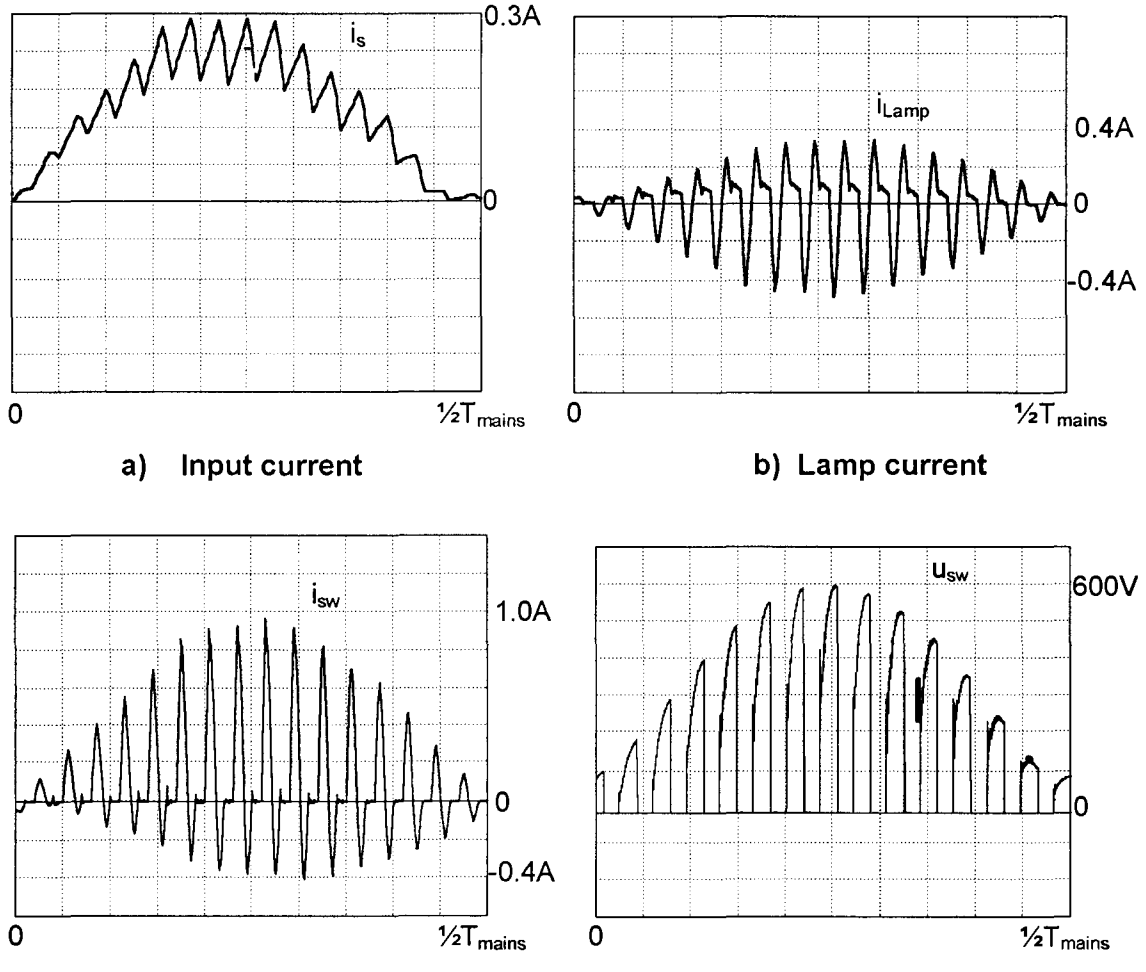


Figure 3-10 Low frequency waveforms

We may write:

$$u_s = L_i . \frac{di_s}{dt} + u_a \qquad (3\text{-}1)$$

Since the average voltage drop across L_i along a switching period is small and the mains voltage is also considered to be constant during a switching period, u_s is nearly equal to $\overline{u}_a$. If $\overline{u}_{sw}$ is the average value of the voltage across the switch during t_{off} and *d* is the duty cycle defined by $d=t_{on}/T$, we have;

$$u_s \approx \overline{u}_a = \overline{u}_{sw} . (1-d) \qquad (3\text{-}2)$$

or

$$\overline{u}_{sw} = \frac{|u_s|}{1-d} \qquad (3\text{-}3)$$

Thus, by keeping constant the duty-cycle, a sinusoidal envelope of voltage u_{sw} results, figure 3-10d. At any time, voltage u_a on the ac side of the bridge rectifier has the same amplitude as switch voltage u_{sw} and the same polarity as input current i_s. Current i_s becomes sinusoidal, its phase being determined by the actual value of inductor L_i, figure 3-10a. In practice, the filter impedance at the line frequency is small, and i_s is nearly in phase to the mains voltage u_s.

Figure 3-10b shows that the lamp current extinguishes at any zeroing of the mains voltage. This causes lamp flickering and also affects the lamp lifetime. Arc extintion can be avoided with the circuit shown in figure 3-1. Inductor L_e in series with capacitor C_e avoids zeroing of the voltage feeding the high frequency section. The basic operation of this circuit is quite similar to the circuit described here.

Dimming operation with the series resonant circuit is not possible due to the fact that $R_{la}<2\sqrt{(L/C)}$; in order to obtain resonant switching, the lamp current must exceed the input current in every high frequency switching period.

Another disadvantage is that the switch voltage equals the lamp voltage during ignition of the lamp. For example, the ignition voltage of a TL5/49W lamp can be as high as $1100V_{top}$.

3.3 PARALLEL RESONANT SOFT-SWITCHING TOPOLOGY

As a result of the topologies presented in paragraph 3.1 and the topology presented in paragraph 3.2 a parallel resonant soft-switching topology is investigated. Figure 3-11 shows the circuit.

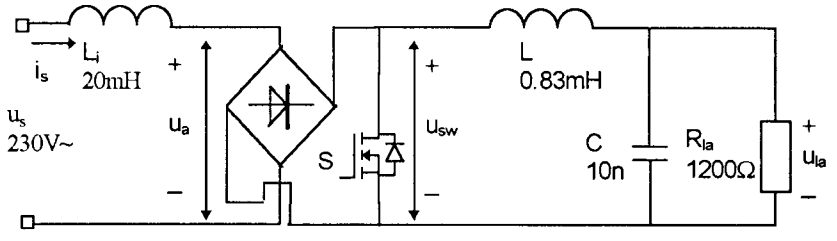


Figure 3-11 Parallel resonant soft-switching converter

Inductor L_i may operate in continuous or discontinuous current mode, depending on its inductance. The basic operation of the circuit is the same as described in paragraph 3.2 and is therefore not extensively explained here. Again two operating modes occur during a switching period, depending on the switch status. The parallel resonant topology differs from the series resonant topology in that the lamp voltage equals the capacitor voltage. Ignition of the lamp should be possible without additional circuitry and high voltage across the switch. The voltage stress on the power switch, during normal operation, is about the same as for the series resonant circuit.

High frequency operation:

A derivation of the high frequency currents and voltages, as well as the maximum switch voltage can be found in appendix C. The currents and voltages as function of time are derived using state-space analysis and laplace transforms. The major high frequency waveforms of the converter are very similar to those described in paragraph 3.2. The shape of the waveforms can be found in figure 3-12.

Low frequency operation:

For analysis of the low frequency operation only the positive half of the mains voltage is considered. The low frequency operation is shown in figure 3-12. The waveforms are obtained with; $u_s=325.\sin(2\pi 1000.t)$ and $f_{switch}=28.5kHz$; $d=0.43$.

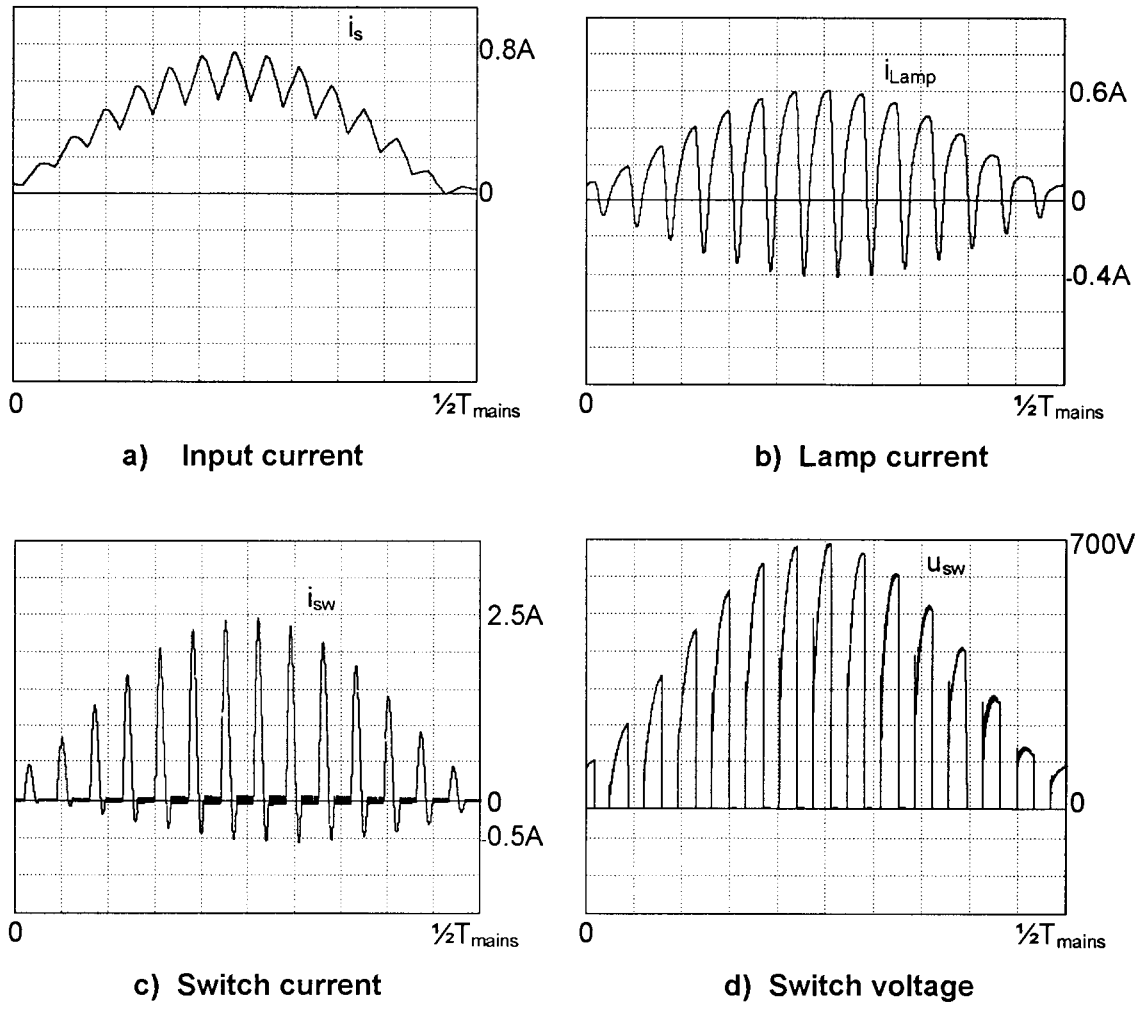


Figure 3-12 Low frequency waveforms

In order to obtain soft-switching, the lamp resistance of the parallel resonant converter should be bigger than a critical value $R_{la}>½\sqrt{(L/C)}$ and the lamp voltage should exceed the mains voltage peak. (For the series resonant converter the lamp resistance should be less than a critical value $R_{la}<2\sqrt{(L/C)}$). Dimming of the lamp is not possible because of the fixed on-time of the switch ($t_{on} \approx 2\pi.\sqrt{(LC)}$).

The parallel resonant soft-switching topology has the same major disadvantages as the series resonant soft-switching topology. The circuit suffers from lamp flickering and sets bounds to the lamp resistance in order to obtain soft-switching.

4. INVESTIGATION ELECTRONIC BALLAST

The most promising topology (5) is used for tight investigation. The ballast shown in figure 3-5 is analysed, designed, built and tested.

4.1 INTRODUCTION

Figure 4-1 shows the original circuit of the ballast to be examined.

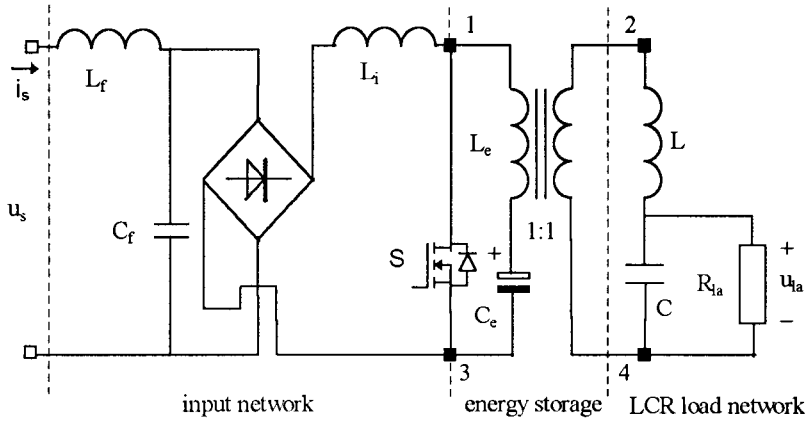


Figure 4-1 Ballast with unclamped energy storage circuit

If in the application the lamp does not need the isolation from the circuit common terminal direct coupling may be satisfactory. Using direct coupling point 1 is connected to 2 and point 3 is connected to 4. Direct coupling has the advantage that some current can flow directly from the input circuit into the resonant circuit without flowing through any energy storage circuit, this may result in a high efficiency. Using direct coupling a DC blocking capacitor has to be added in series with the lamp to prevent direct current from flowing through the lamps.

The ballast, shown in figure 4-1, uses an unclamped energy storage circuit to prevent the lamp from being turned off at zero crossings of the mains voltage. When it is desired to reduce the ripple in the lamp current and to clamp the switch voltage (in case the lamps are removed), a clamping winding is needed. Without clamping winding the energy delivered to the lamp will fluctuate considerably. Figure 4-2 shows a direct coupled clamped energy storage circuit.

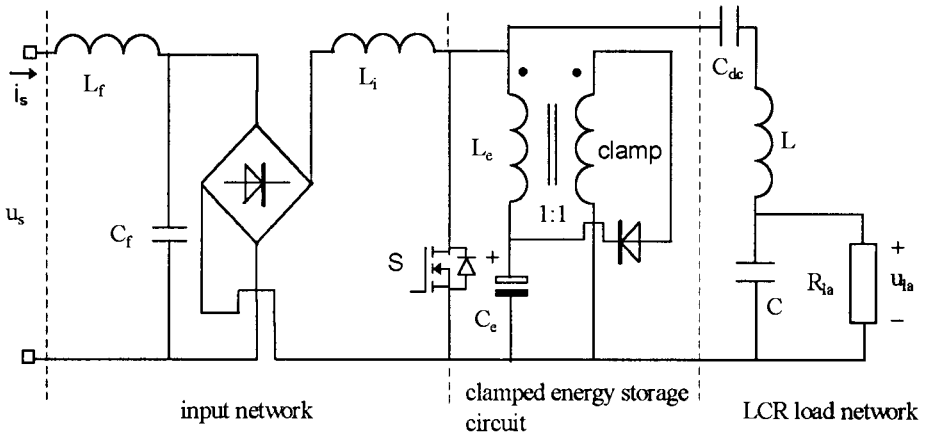


Figure 4-2 Ballast with direct coupled clamped energy storage circuit with tightly coupled windings

When the voltages across the clamp winding and winding L_e equals the voltage across capacitor C_e, the clamping diode becomes forward biased. Charge is transferred through clamping diode and winding into storage capacitor C_e. The presence of the clamping winding constraints the voltage across the primary winding from exceeding the voltage across storage capacitor C_e.

The clamp inductor needs tightly coupled windings, otherwise if there is any leakage present between the two windings, the energy is transported to the drain-source capacitance of the switch resulting in a high voltage spike across the switch. Voltage spikes require either a more expensive higher voltage switch or an expensive snubber circuit. Figure 4-3 shows a direct coupled clamped energy storage circuit where the clamp inductor needs loosely coupled windings.

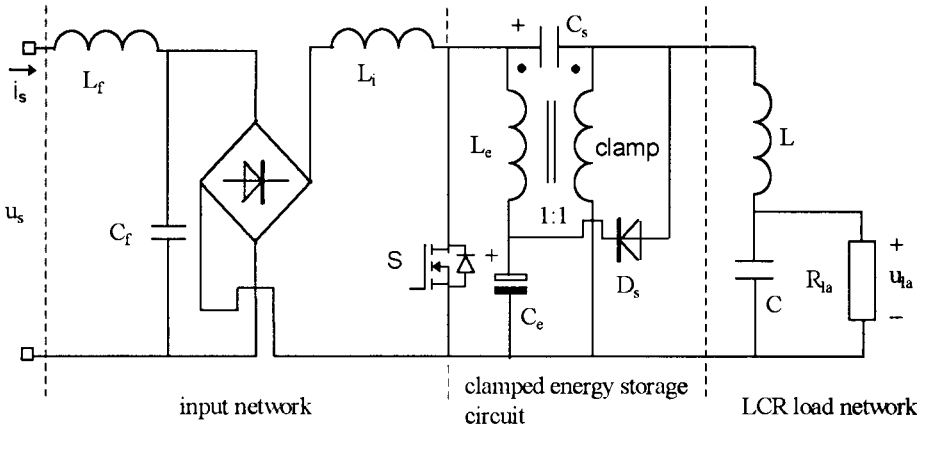


Figure 4-3 Ballast with direct coupled clamped energy storage circuit with loosely coupled windings

The voltage across winding L_e is clamped across C_s and the voltage across the clamp winding is clamped across C_e. If there is any leakage present between the two windings the energy is recycled into capacitors C_e and C_s. Applying this configuration capacitor C_s also prevents direct current from flowing through the lamps. The ballast shown in figure 4-3 is used for further investigation.

4.2 STATE-SPACE DESCRIPTION OF THE BALLAST

The ballast shown in figure 4-3 is converted to the circuit of figure 4-4.

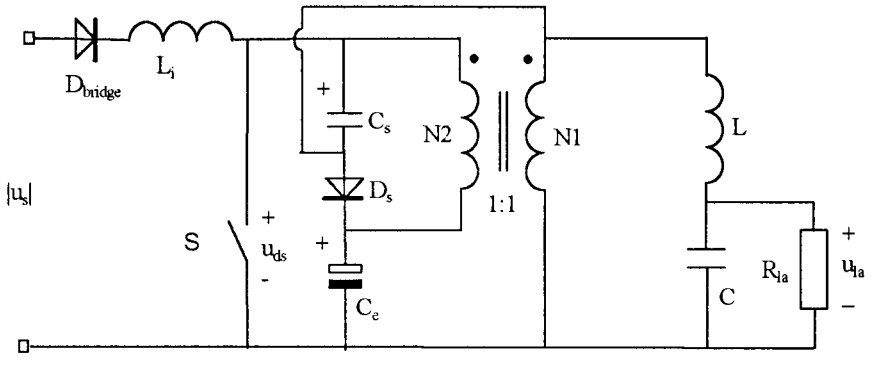


Figure 4-4 Equivalent circuit of the ballast

The input network is replaced by a new power source $|u_s|$ and a rectifier diode D_{bridge}. The low pass filter (L_f,C_f) does not determine the operation of the ballast and is therefore left out. The lamp is characterized by a (negative) resistor. The MOSFET is modelled as an ideal switch.

If bridge rectifying diode D_{bridge} and clamp diode D_s are also considered as an ideal switch, the circuit contains three switches. Using three switches eight combinations are possible. Not all combinations are applicable, table 4-1 shows the possible combinations.

Table 4-1: States of the electronic ballast

State	S	D_{bridge}	D_s
I	on	on	off
II	off	on	on
III	off	off	off
IV	off	on	off

The linear switched circuit model, called state I is drawn in figure 4-5.

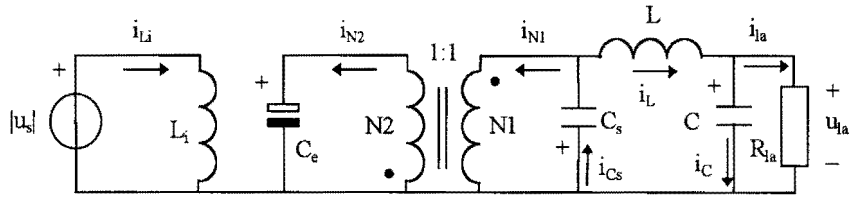


Figure 4-5 Linear switched circuit model, called State I

When the switch is on, diode D_s blocks and energy is stored in inductor L_i and in the magnetising inductor of the coupled inductors. Due to transformer action of the coupled inductors, the voltage across capacitor C_s is the same as the voltage across capacitor C_e. During this stage a constant negative voltage is applied to the LCR output circuit.

The linear switched circuit model, called state II is drawn in figure 4-6.

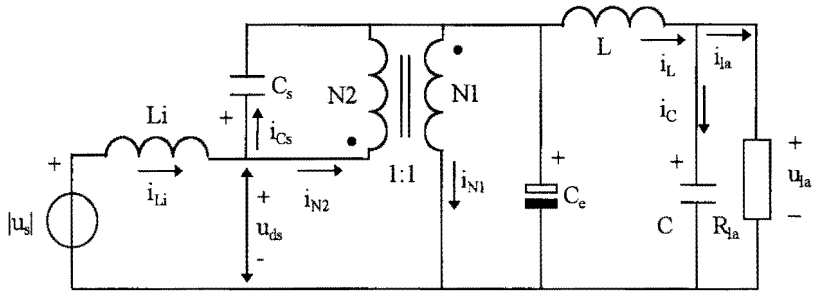
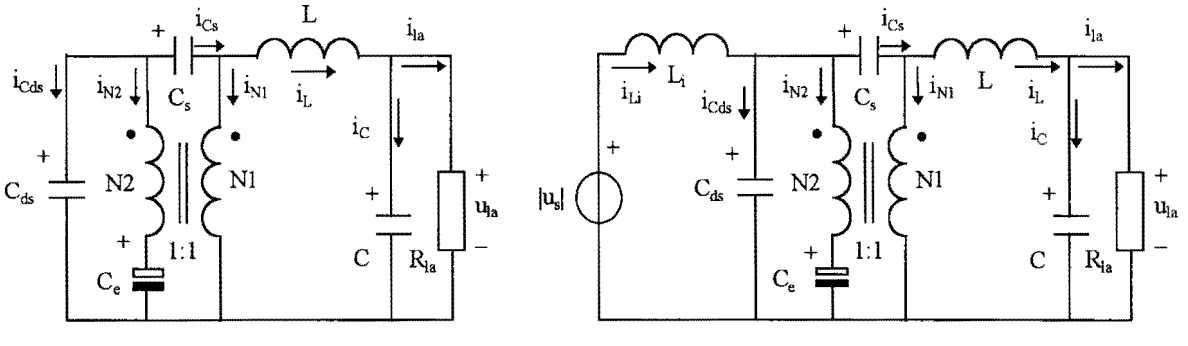


Figure 4-6 Linear switched circuit model, called State II

When the switch is switched off, diode D_s starts to conduct and inductive energy from the input inductor and coupled inductors is transferred to the LCR network and to capacitor C_e. During state II, the voltage across the switch is clamped to $U_{Cs}+U_{Ce}$ and a constant positive voltage is applied to the LCR output circuit.

The linear switched circuit models, called state III and IV are shown in figure 4-7.



State III **State IV**

Figure 4-7 Linear switched circuit models, called State III and IV

When clamp diode D_s stops conducting all switches are off, state III, and a free oscillation of the voltage across the switch occurs. The drain-source capacitance C_{ds}, the output inductor L and the output capacitor C approximately determine the oscillation frequency, the lamp resistance R_{la} determines the damping of the oscillation.

At the moment clamp diode D_s stops conducting the voltage across the switch is at its maximum and starts decreasing. When the drain-source voltage approaches the instantaneous mains voltage state IV must be considered. During state IV the bridge diode D_{bridge} is conducting again, while the clamp diode blocks.

The drain-source voltage can not become negative due to the body diode of the switch. The maximum drain-source voltage is determined by state II when the clamp diode is conducting, $U_{ds,max}=U_{Ce}+U_{Cs}$. The voltage oscillation across the drain-source terminals continues until switch S is switched on again.

For nominal operation (duty-cycle 50%) the clamp diode keeps conducting when switch S is switched off, therefore only state I and II have to be considered.

4.3 CIRCUIT ANALYSIS, NOMINAL OPERATION

The nominal operation of the ballast can be explained by two linear switched circuit models, state I and state II.

Input circuit:

If the amplitude of the mains voltage is given by $\hat{u}_s$ and the ballast is designed in a way that $U_{Cs}\approx U_{Ce}\approx\hat{u}_s\approx$constant, the input behaviour (waveform of the input current before filtering) can be described by the circuit shown in figure 4-8.

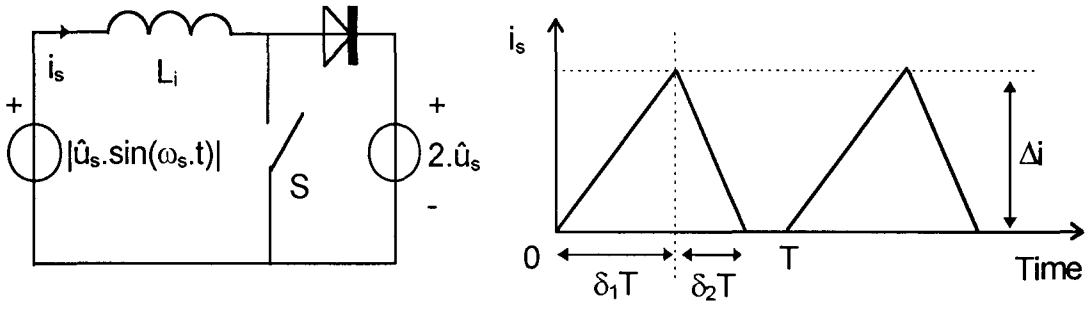


Figure 4-8 Model for describing the input current

The mains frequency is given as ω_s. The switching frequency of the converter (f=1/T) is chosen much higher than the mains frequency. The mains voltage can be considered constant (U_s) during every high frequency switching period T and the envelope of all voltage steps during a mains frequency period approximates a half sinewave, as given by figure 4-9a.

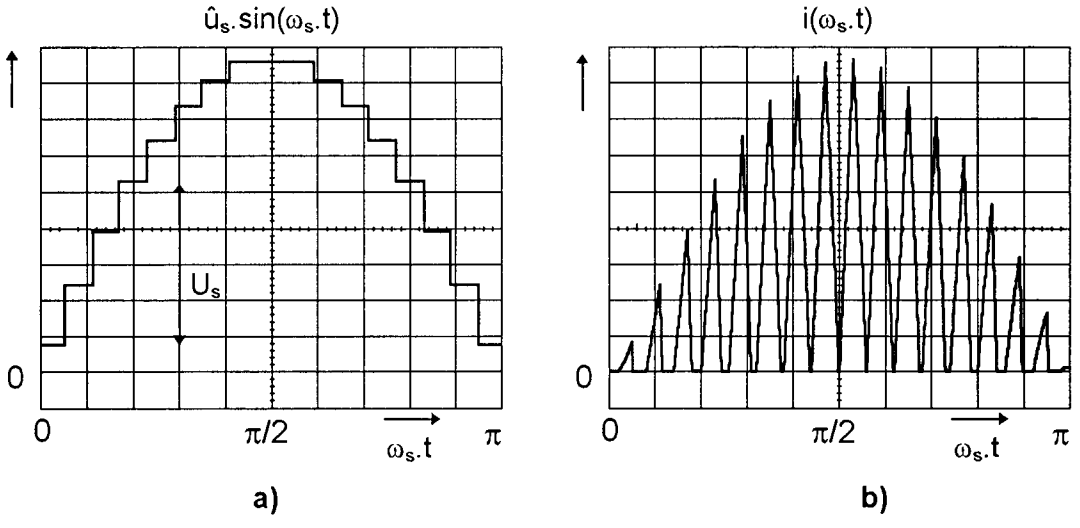


Figure 4-9 A half sine wave with discrete voltage steps and the current pulses within a half sine wave of the supply

The duty cycle is assumed to be constant during a mains frequency period. The time t=0 starts at a half period of duration $\omega_s.t=\pi$. Due to the high frequency input filter, the ac line current should be given by the instantaneous mean value of the input inductor current. During one high frequency cycle the average input current is:

$$\bar{i}_s = \frac{\delta_1 + \delta_2}{2} . \frac{\delta_1 . T}{L} . U_s \qquad (4\text{-}1)$$

Since $\delta_1.T$ is fixed and $\delta_2.T$ is a function of the mains voltage, $\delta_2.T$ has to be eliminated. With

$$\Delta i = \frac{\delta_1 . T}{L} . U_s = \frac{2.\hat{u}_s - U_s}{L} . \delta_2 . T \qquad (4\text{-}2)$$

we obtain

$$\delta_2 = \frac{\delta_1 . U_s}{2.\hat{u}_s - U_s} \qquad (4\text{-}3)$$

If we combine equation 4-1 and 4-3 we get;

$$\bar{i}_s = \frac{\delta_1^{\,2} . T}{2. L} . \left[\frac{2.\hat{u}_s}{2.\hat{u}_s - U_s} \right] . U_s \qquad (4\text{-}4)$$

Now $\bar{i}_s$ is no longer an average value but depends on $\omega_s.t$;

$$i_s(\omega_s.t) = \frac{\delta_1^2.T}{2-\sin(\omega_s.t)}.\frac{\hat{u}_s}{L}\sin(\omega_s.t) \qquad (4\text{-}5)$$

If $\frac{\delta_1^2.T}{2-\sin(\omega_s.t)}$ is constant, the source current has a sinusoidal shape. If δ_1 and T are constant during a mains frequency period, meaning a low cost control circuit for the power switch, the mains current is nearly sinusoidal as illustrated by figure 4-10.

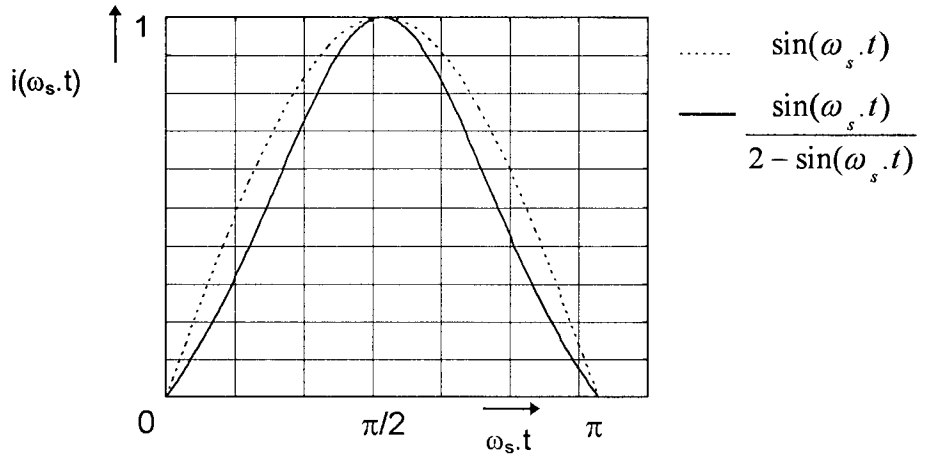


Figure 4-10 Mains current with δ_1 and T constant

Tabel 4-1 shows the harmonics of the mains current as a percentage of the first harmonic if δ_1 and T are constant. Also the maximum permissible values according to the IEC 1000-3-2 class C standard are given.

Table 4-1: Harmonics of the mains current if δ_1 and T are constant

Harmonic order n	Harmonic in %	Maximum permissible harmonic in %
2	0	2
3	13	30
5	0.1	10
7	0.3	7
9	0.1	5
11	0.1	3
13	0.4	2

Tabel 4-1 shows that the mains current meets the requirements if the power switch is operated at constant frequency and fixed duty cycle. A low pass filter at the input (L_f,C_f) can be used to filter the higher harmonics.

The input power over one low frequency period is calculated with;

$$P_s = \frac{1}{\pi}\int_0^{\pi} i_s(\omega_s t).\hat{u}_s.\sin(\omega_s t).d\omega_s t \qquad (4\text{-}6)$$

With equation (4-5) we obtain;

$$P_s = \frac{8.\delta_1^2.T}{9L}.U_s^2 \qquad (4\text{-}7)$$

where U_s is the rms input voltage, $U_s = \hat{u}_s/\sqrt{2}$. For nominal operation $\delta_1 = 0.5$, thus

$$P_s = \frac{2T}{9L}.U_s^2 \qquad (4\text{-}8)$$

Power conversion stage:
Figure 4-5 and 4-6 show a "voltage source" configuration across the coupled inductors if the ballast is designed in a way that $U_{Cs} \approx U_{Ce} \approx \hat{u}_s \approx$ constant. The coupled inductors have been described by two different models. The first "theoretical" model is shown in figure 4-12 and uses the mutual inductance M.

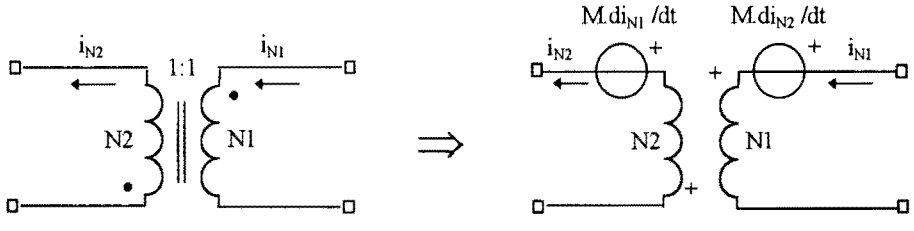


Figure 4-12 Coupled inductor model with mutual inductance M

The second "practical" model is shown in figure 4-13. This model shows the magnetising inductor L_m, which is used for energy storage and uses the coupling coefficient k to describe the leakage inductance's L_{s1} and L_{s2}.

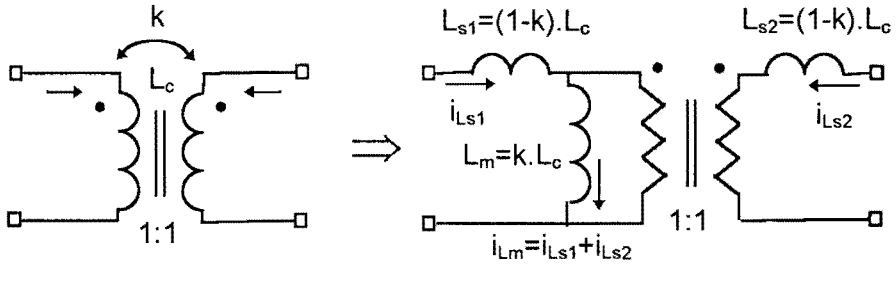


Figure 4-13 Coupled inductor model with coupling coefficient k and leakage inductance's L_{s1} and L_{s2}.

Appendix D shows the states I up to IV, using the first model. Appendix E shows states I up to IV, using the second model. Also a state space description of the circuit is given with the according matrices A and B for each state. Eventually the first and second model yield the same results.

Assuming the voltages across capacitors C_e and C_s equal $\hat{u}_s$ and using the coupled inductor model shown in figure 4-13 we obtain;

$$i_{Lm} = i_{Lm}(0) + \Delta i_{Lm} \qquad (4\text{-}9)$$

$$i_{Ls1} = i_{Ls1}(0) + \Delta i_{Ls1} = i_{Ls1}(0) + \tfrac{1}{2}.\Delta i_{Lm} \qquad (4\text{-}10a)$$

$$i_{Ls2} = i_{Ls2}(0) + \Delta i_{Ls2} = i_{Ls2}(0) + \tfrac{1}{2}.\Delta i_{Lm} \qquad (4\text{-}10b)$$

with

$$\Delta i_{Lm} = \frac{\hat{u}_s.T}{(1+k).L_c}.$$

The magnetising current i_{Lm} models the energy stored in the airgap. Figure 4-14 shows the current through the magnetizing inductor L_m.

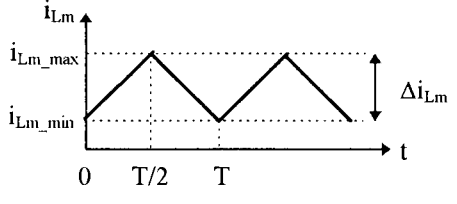


Figure 4-14 Current through the magnetizing inductor L_m.

The power transferred after one high switching cycle is;

$$P_{Lm} = \frac{\Delta E}{\Delta t} = \frac{\frac{1}{2}L_m.(i_{Lm\_max}{}^2 - i_{Lm\_min}{}^2)}{T} \qquad (4\text{-}12)$$

Using the fundamental of the voltage across the LCR output circuit (appendix F) and with the condition $i_{Lm\_min} = -i_L(0)$, which will be explained later, we get:

$$P_{Lm} = \frac{k.\hat{u}_s{}^2}{2(k+1)^2.L_c.f} + \frac{k.\hat{u}_s}{(k+1)}.\hat{i}_L.\sin(\varphi) \qquad (4\text{-}13)$$

Where;

L_c =inductance of the coupled inductors (1:1)

f =switching frequency

$\hat{i}_L$ =peak of the inductor current flowing through the output inductor (LCR-circuit)

φ =angle between the voltage across the LCR-circuit (u_{LCR}) and the current flowing to the output inductor (i_L)

Voltage across the power switch:

Figure 4-6 (state II) shows that the voltage across the switch is clamped to $U_{Cs}+U_{ce}$ If the ballast is designed in a way that $U_{Cs}\approx U_{Ce}\approx\hat{u}_s\approx$constant, the voltage across the switch is square wave and alternates between zero and twice the peak of the mains voltage.

Current through the power switch:

The (steady-state) switch current is evaluated for duty cycle 50%. The instantaneous current through the switch is the sum of the current through the input inductor L_i, the current through the output inductor L and the current through the magnetising inductor L_m;

$$i_{sw}(t) = i_{Li}(t) + i_L(t) + i_{Lm}(t) \qquad (4\text{-}14)$$

Figure 4-15 shows the waveforms of the currents determining the current flowing through the switch over 4 switching cycles.

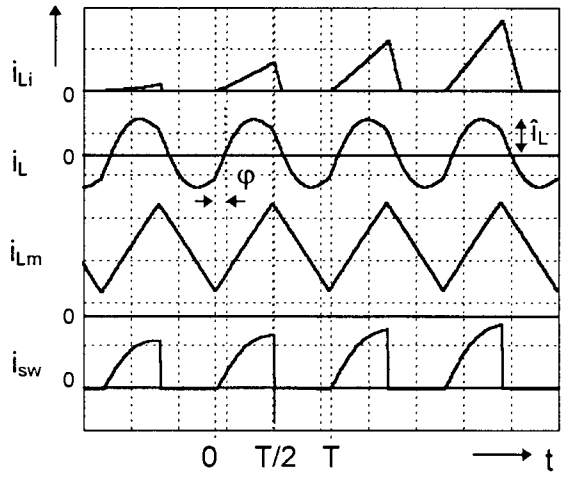


Figure 4-15 Waveforms determining the current flowing through the switch

Time t=0 starts at a high frequency period of duration T. Figure 4-15 shows that the high frequency current through the switch depends on the instantaneous value of the mains voltage (U_s) because current i_{Li} does.

The input current can be calculated with;

$$i_{Li}(t) = \frac{U_s}{L_i}.t \qquad (0< t <½T) \qquad (4\text{-}15)$$

The current through the output inductor L can be calculated with;

$$i_L(t) = \hat{i}_L.\sin(\tfrac{2\pi}{T}t - \varphi) \qquad (0< t <½T) \qquad (4\text{-}16)$$

and the current through the magnetising inductor L_m;

$$i_{Lm}(t) = \frac{2.\hat{u}_s}{(k+1)L_c}.t + i_{Lm}(0) \qquad (0< t <½T) \qquad (4\text{-}17)$$

Considering one high frequency cycle, the average current through the switch is;

$$\bar{i}_{sw} = \bar{i}_{Li} + \bar{i}_L + \bar{i}_{Lm} \qquad (4\text{-}18)$$

$$\bar{i}_{sw} = \frac{1}{2}.\left[\frac{1}{2}.\frac{U_s}{L_i}.\frac{T}{2} + \frac{2.\hat{i}_L\cos(\varphi)}{\pi} + \frac{1}{2}.\frac{2.\hat{u}_s}{(k+1).L_c}.\frac{T}{2} + i_{Lm}(0)\right]$$

With the condition that i_{sw}=0 at t=0 we find that $i_{Lm}(0)$= - $i_L(0)$, thus

$$\bar{i}_{sw} = \frac{U_s.T}{8L_i} + \frac{\hat{i}_L\cos(\varphi)}{\pi} + \frac{\hat{u}_s.T}{4(k+1)L_c} + \frac{\hat{i}_L.\sin(\varphi)}{2} \qquad (4\text{-}19)$$

Now $\bar{i}_{sw}$ is no longer an average value but depends on $\omega_s t'$, where $0<\omega_s t'<\pi$ and ω_s is the low frequency;

$$i_{sw}(\omega_s t') = \frac{\hat{u}_s.T.\sin(\omega_s t')}{8L_i} + \frac{\hat{i}_L\cos(\varphi)}{\pi} + \frac{\hat{u}_s.T}{4(k+1)L_c} + \frac{\hat{i}_L.\sin(\varphi)}{2} \qquad (4\text{-}20)$$

The rms value of the current through the switch can be calculated with

$$I_{sw} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_{sw}(\omega_s.t')^2.d\omega_s.t'} \quad . \qquad (4\text{-}21)$$

Using equation 4-21 we obtain $I_{sw} = \bar{i}_{sw}$ where U_s is no longer the instantaneous value of the mains voltage, but the rms value of the mains voltage $U_s=\hat{u}_s/\sqrt{2}$.

Output circuit:

If the ballast is designed in a way that $U_{Cs} \approx U_{Ce} \approx \hat{u}_s \approx$ constant then the output circuit can be described by the waveforms shown in figure 4-16.

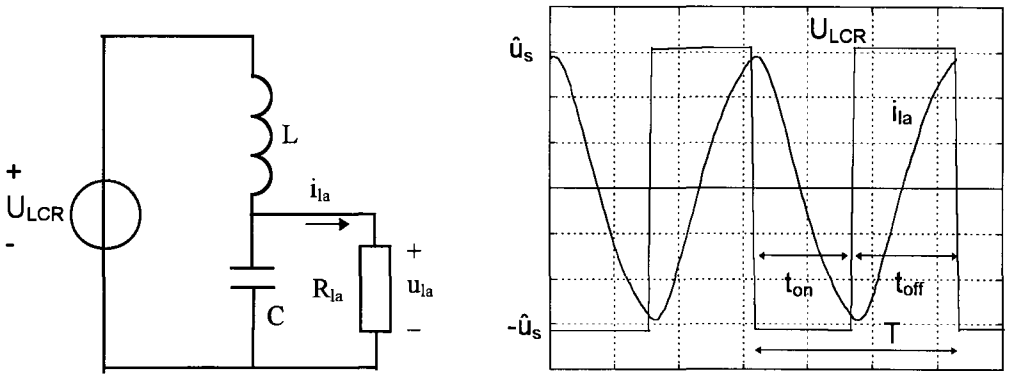


Figure 4-16 Output network with corresponding waveforms; $U_{sw}=U_{LCR}+\hat{u}_s$

Figure 4-5 shows that during state I a negative voltage is applied to the LCR network (U_{Cs}) and figure 4-6 shows that during state II a positive voltage is applied to the LCR network (U_{Ce}). Thus the voltage across the LCR network is square wave with amplitude equal to the peak of the mains voltage.

The voltage across the LCR network is filtered by the output L,C combination (low pass filter) and a nearly sinusoidal lamp current is obtained. Analysis of the output circuit, using the fundamental of the square wave, can be found in appendix F. The output power can be calculated with;

$$P_o = \frac{16.|H|^2}{\pi^2 R}.U_s^{\,2}, \text{ where } |H|^2 = \frac{1}{\left(\frac{\omega}{\omega_o}\right)^2.\frac{1}{Q^2}+\left(1-\left(\frac{\omega}{\omega_o}\right)^2\right)^2}, Q = R\sqrt{\frac{C}{L}}, \omega_o = \frac{1}{\sqrt{LC}} \qquad (4\text{-}22)$$

The voltage across the LCR-load network is square wave. The fourier series of this voltage for 50% duty-cycle operation is;

$$u_{LCR} = \sum_{n=1}^{\infty} \frac{-2\sqrt{2}.U_s}{n\pi}.[1-(-1)^n].\sin(\frac{2\pi n}{T}t) \qquad (4\text{-}23)$$

where T is the high frequency switching period and U_s the effective input voltage.
If the switching frequency equals the resonance frequency of the LC-combination ($\omega=\omega_o$) and only the first harmonic of voltage u_{LCR} is used then the output power can be calculated with;

$$P_o = \left[\frac{4U_s}{\pi}\right]^2.\frac{C}{L}.R_{la} \qquad (4\text{-}24)$$

4.4 CIRCUIT ANALYSIS, DIMMING OPERATION

The power to the lamp can be controlled by changing the duty cycle of the switch (PWM) and/or by changing the switching frequency (FC). While dimming, the lamp resistance is not constant. The lamp resistance versus the lamp voltage is measured, the results are shown in figure 4-17.

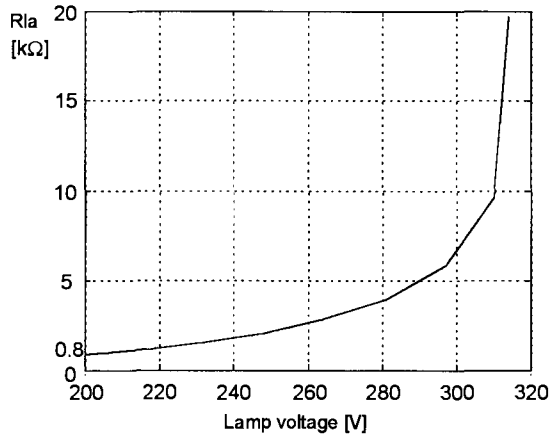


Figure 4-17 Lamp resistance versus lamp voltage

Referring to single switch ballasts the in- and output power is controlled by the same switch. In order to maintain high efficiency these two powers should have the same control characteristics.

FC dimming:

Figure 4-18 shows the FC-dimming characteristic of a TL5/49W lamp with L=3.5mH and C=2.7nF. The input power P_s is calculated with equation 4-7. The lamp resistance as function of the lamp voltage is taken from figure 4-17.

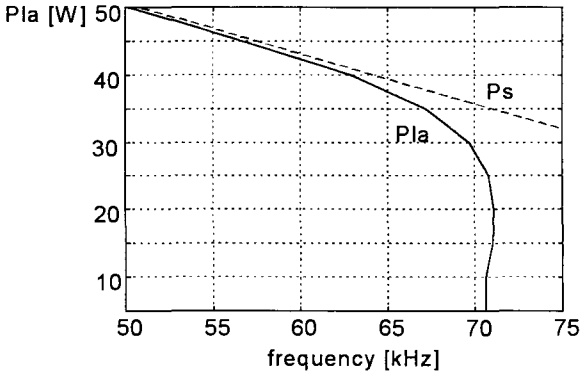
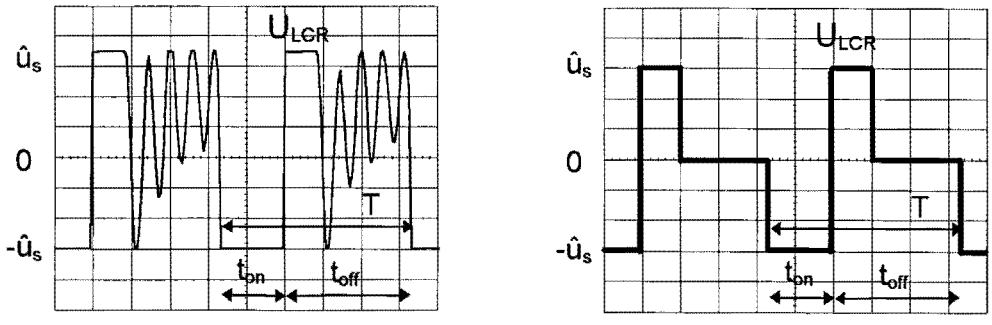


Figure 4-18 Lamp power versus frequency

Figure 4-18 shows that dimming of the lamp using frequency control is limited to approximately 30W (60% of nominal lamp power). For switching frequencies higher than 70 kHz, the in- and output power diverge.

PWM dimming:

If the duty-cycle of the switch is less than 50%, the voltage across the LCR-circuit is no longer a square wave but looks more like the waveform shown in figure 4-19a.



a) Simulated b) Simplified

Figure 4-19 Voltage across the LCR-circuit with duty-cycle≈30%

Using PWM the amplitude of the fundamental voltage across the LCR network is controlled. For dimming operation, the four linear switched circuit models described in paragraph 4.2 should be considered. Analysis of the waveforms, however, is rather comprehensive due to nonlinearity of the circuit. To simplify the analysis, the voltage across the LCR-network is approximated by the waveform of figure 4-19b. Fourier analysis of this waveform is given in appendix G.

Figure 4-20 shows the PWM-dimming characteristic of a TL5/49W lamp with L=3.5mH and C=2.7nF. The input power P_s is again calculated with equation 4-7 and the lamp resistance as function of the lamp voltage is again obtained from figure 4-17.

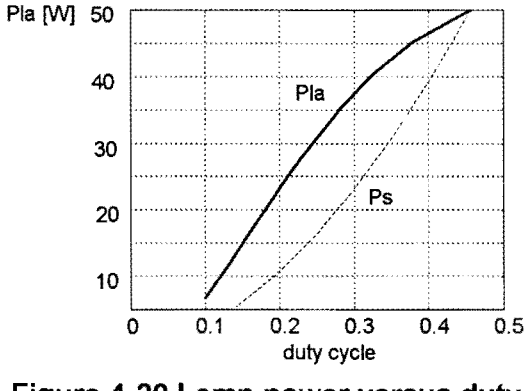


Figure 4-20 Lamp power versus duty cycle

Figure 4-20 shows that while dimming the lamp, the (calculated) lamp power P_{la} exceeds the input power P_s. In practice, of course, this could never happen, the lamp power will always be lower than the input power. More reliable and accurate results can be obtained with simulations (chapter 5). Measurements, confirm that with PWM dimming the output power follows the input power, unlike frequency dimming. Dimming of the lamp using PWM is possible to at least 1% percent of nominal lamp power.

5. SIMULATION AND EXPERIMENTAL RESULTS

5.1 CIRCUIT DESIGN

The circuit used for simulations and experiments is shown in figure 5-1.

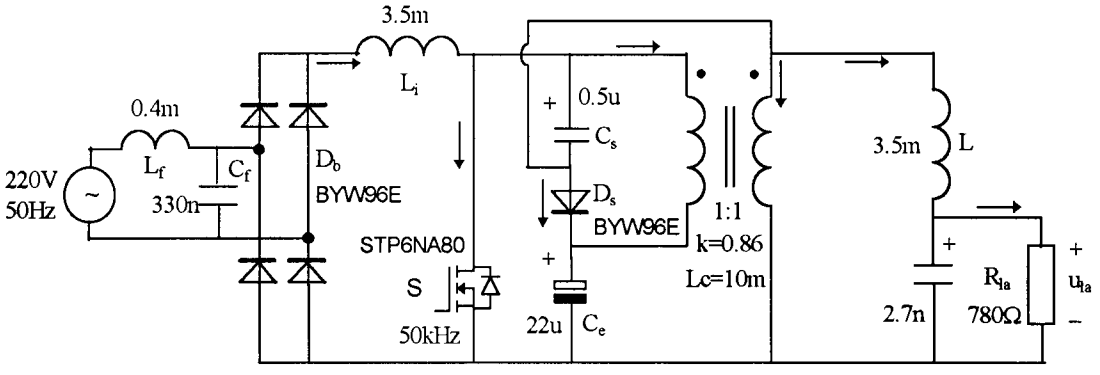


Figure 5-1 Ballast used for simulations and experimental results

The ballast is designed for a TL5-49W fluorescent lamp. The nominal lamp voltage is 195V and the equivalent lamp resistance is 780Ω. The ignition voltage of the lamp can be as high as $1100V_{top}$. In order to compare the ballast with the existing ballasts an operating frequency of 50kHz is chosen.

input inductor (L_i):

The input power $P_s=P_o/\eta$, where η is the efficiency. L_i can be calculated with equation 4-8. With P_o=49W, η=0.85, T=20μS and U_s=220V we obtain **L_i=3.73mH**.

output inductor (L) and output capacitor (C):

Ratio C/L can be calculated with equation 4-24. With P_o=49W, R_{la}=780Ω and U_s=220V we obtain C/L=8E-7. With $T=2\pi\sqrt{(LC)}$=20μS we obtain **C=2.85nF** and **L=3.37mH**. The open circuit voltage will be sufficient to strike the lamp because the resonance frequency of the LC-combination equals the switching frequency and $Q\rightarrow\infty$. The ignition voltage of the lamp also determines the voltage rating of the output capacitor.

Coupled inductors (L_c):

With equation 4-13 the inductance of the coupled inductors (1:1) can be calculated. If we assume the energy storage circuit must provide the nominal lamp power when the mains voltage is zero we have $P_{Lm}=P_o$=49W. With equation F-13 we can calculate $\hat{i}_L$=0.45A and with equation F-6 we can calculate $\varphi=55°$. Then with $\hat{u}_s$=311V, k=0.86, f=50kHz we obtain **L_c=11.7mH**. In practice, the inductance of the coupled inductors may be less, since a part of the energy is recycled by the clamp circuit. However, extra losses will be introduced due to the extra circulating currents and the current through the power switch will be increased which leads to extra power dissipation.

Capacitor *(C_e):*

Capacitor C_e must be large enough to supply the nominal lamp power and must have a low voltage ripple in order to obtain a low lamp current crest factor. The voltage rating of capacitor C_e is at least the mains voltage peak. An elco **C_e=22μF/450V** is chosen which results in a lamp current crest factor cf=1.47.

Capacitor (C_s):

In order to prevent high resonant currents capacitor C_s must not resonate with the leakage inductance of the coupled inductors. Therefore $L_{s1}.C_s=(1-k).L_c.C_s>>L.C$. The voltage rating of C_s is the same as for C_e. A film capacitor **C_s=0.5μF/450V** is chosen.

Input filter (C_f, L_f):

An input filter is necessary to prevent electromagnetic interference with other users of the system. For the application a LC-filter is used to filter the high frequency current pulses through the input inductor. An inductor **L_f=0.4mH** and capacitor **C_f=330nF** is chosen with cut-off frequency $f_{3\text{-}dB}\approx$10kHz. The input filter, however, is not optimised.

Bridge rectifying diodes (D_b):

The maximum current flowing through a bridge diode equals the maximum current flowing through inductor L_i. With equation 4-2 and L_i=3.73mH, δ_1=0.5, T=20μS and $\hat{u}_s$=311V we obtain $i_{Li,max}=i_f$=0.83A. Each bridge diode must be capable of blocking the mains voltage peak and switch at 50kHz. Four BYW96E (avalance, fast, soft-recovery) diodes are chosen with **V_f=1kV** and **$I_{f(av)}$=3A**, also considering the inrush current.

Clamp diode (D_s):

The maximum voltage across the clamp diode is $U_{Ce,max}+U_{Cs,max}$. The maximum current through the clamp diode is approximately the maximum switch current and can be calculated with equation 4-14, $I_{f,max}$=1.9A. For the application a BYW96E (avalance, fast, soft-recovery) is chosen with **V_f=1kV** and **$I_{f(av)}$=3A**.

Power switch:

The maximum voltage across the switch is $U_{Ce,max}+U_{Cs,max}$ and is approximately $2.\hat{u}_s$=622V for nominal operation. The maximum current through the switch can be calculated with equation 4-14, $I_{sw,max}$=1.9A. For the application a switch is chosen with **V_{BR}=800V** and **I_{max}=6A** (STP6NA80).

5.2 IN- AND OUTPUT POWER

Figure 5-2 shows the measured (_meas) and simulated (_sim) in- and output power (P_s and P_{la}) as function of the duty cycle. For simulation all components were assumed to be ideal, therefore $P_{s\_sim}=P_{la\_sim}$.

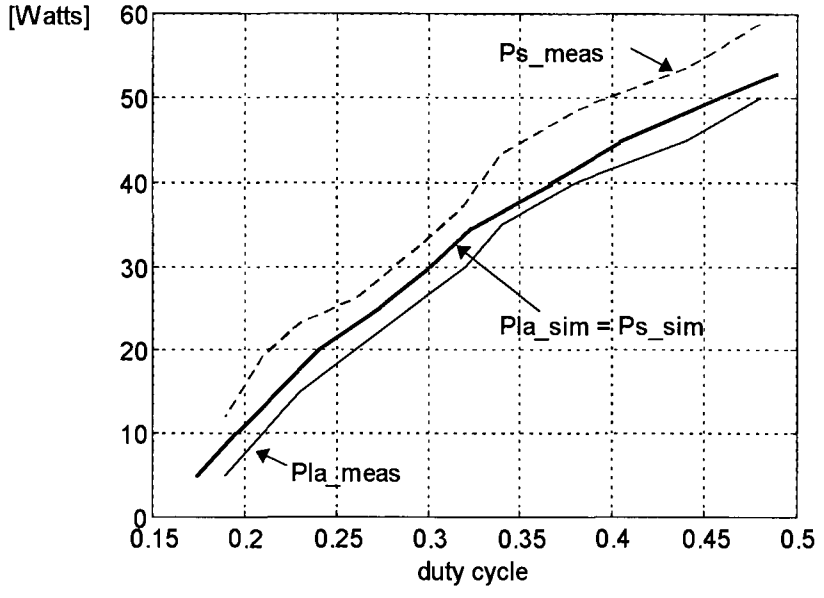


Figure 5-2 Measured and simulated in- and output power versus duty cycle.

Figure 5-2 shows that the total losses ($=P_{s\_meas}-P_{la\_meas}$) are approximately constant over the total dimming range. This results in a decreasing efficiency while dimming the lamp. At nominal lamp power the efficiency of the ballast is approximately 86%, that is 8W total losses. Tabel 5-1 shows the measured temperature of each component and the estimated loss.

Table 5-1 Losses in the ballast at nominal lamp power. P_{total}=8W; T_{amb}=20°C

Component (figure 5-1)	Temperature [°C]	Estimated loss [W]	Percentage of total losses [%]
L_f	<45	0.25	3.125
L_i	<45	1	12.5
L_c	<60	1.5	18.75
L	<45	1	12.5
S	<75	3	37.5
D_b	<60	0.5	6.25
D_s	<60	0.5	6.25
C_f, C_s, C_e, C	<35	0.25	3.125

Table 5-1 shows that almost 40% of the total loss is dissipated in the power switch.

Comparing figure 4-20 with figure 5-2 we can conclude that the circuit can be perfectly designed for nominal operation since the calculated and measured in- and output power match. For dimming operation there's a mismatch between the calculated and measured values. The simulated values are very close to the measured values, so dimming operation can perfectly be described by simulations.

In practice, a mismatch between the in- and output power results in an increase or decrease of the tank capacitor (C_e) voltage. Figure 5-3 shows the measured voltage across capacitor C_e in function of the duty cycle.

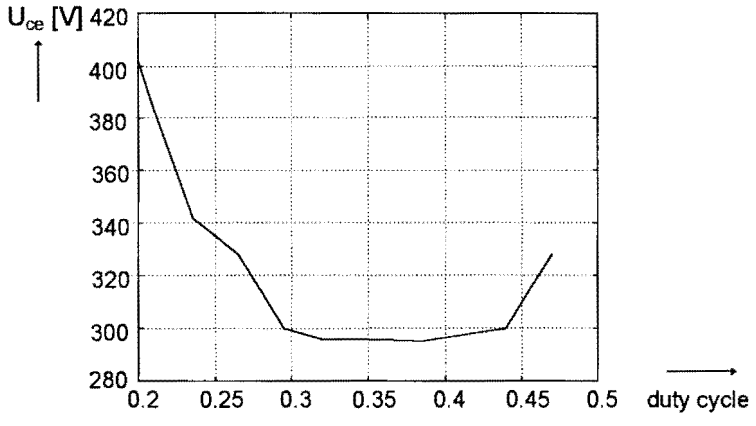


Figure 5-3 Capacitor voltage Uce versus duty cycle

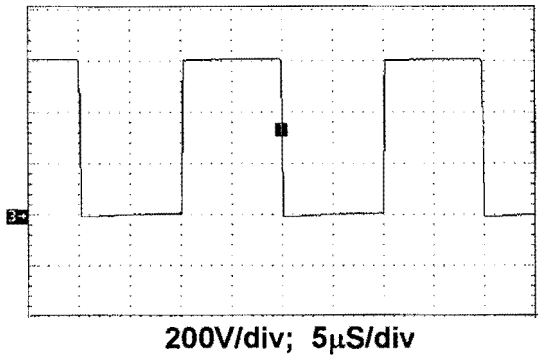
Since the voltage across the switch is approximately twice the voltage across capacitor C_e, the breakdown voltage of the switch should be higher than 800V if the lamp is dimmed more than 20% of nominal lamp power (d<0.2).

5.3 WAVEFORMS, NOMINAL OPERATION

The simulated waveforms match with the measured waveforms, therefore only the measured waveforms will be discussed.

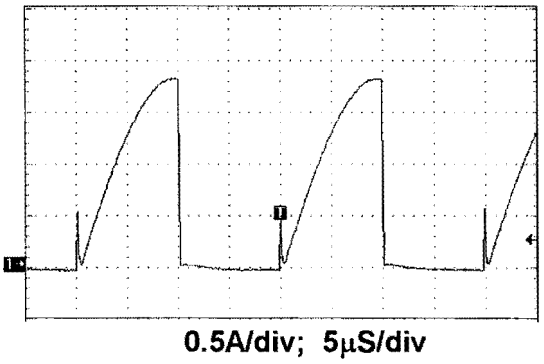
Switch:

Figure 5-4 shows the high frequency voltage across the switch and figure 5-5 shows the high frequency current through the switch.



200V/div; 5μS/div

Figure 5-4 HF Drain-source voltage



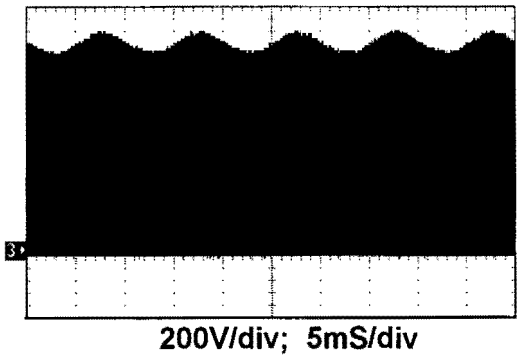
0.5A/div; 5μS/div

Figure 5-5 HF Drain-source current

Figure 5-4 shows that the drain to source voltage is perfectly square wave with maximum amplitude twice the peak of the mains voltage. The current spike, figure 5-5, at switch-on is a result of the discharge of the drain-source capacitance. The spike introduces EMI and should therefore be avoided. The amplitude of the spike can be controlled by connecting a resistance in series with the gate of the MOSFET.

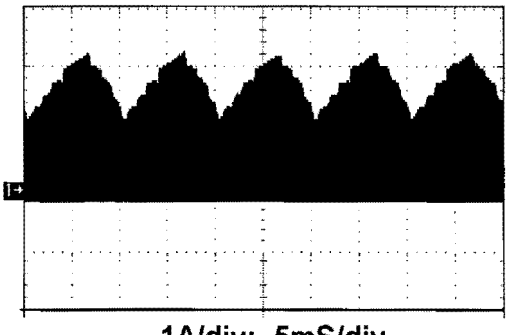
It is shown that the ballast uses hard-switching, the MOSFET is switched on while the drain-source voltage is maximal and is switched off when the current through the switch is maximal. Compared to soft-switching this usually results in more power dissipation in the switch. To minimize the power dissipation, the switch should be switched off fast.

Figure 5-6 shows the low frequency drain to source voltage. The voltage ripple is approximately 50V. Figure 5-7 shows the low frequency drain to source current.



200V/div; 5mS/div

Figure 5-6 LF Drain-source voltage

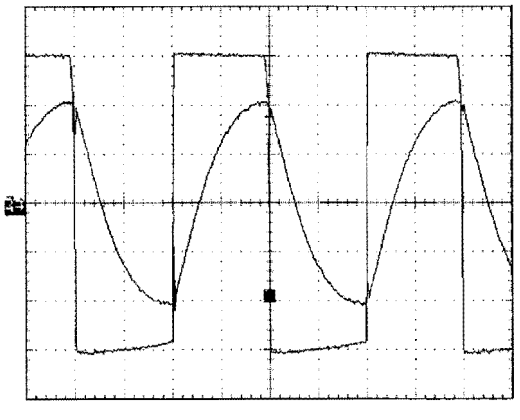


1A/div; 5mS/div

Figure 5-7 LF Drain-source current

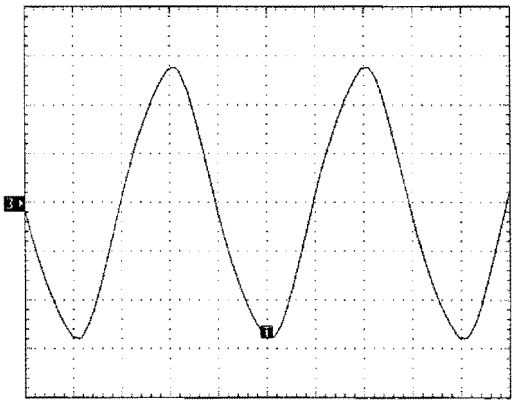
Output circuit:

Figure 5-8 shows the high frequency current through the output inductor (L) and the voltage across the LCR circuit. Figure 5-9 shows the high frequency lamp voltage.



100V/div; 0.2A/div; 5μS/div

Figure 5-8 HF Output inductor current

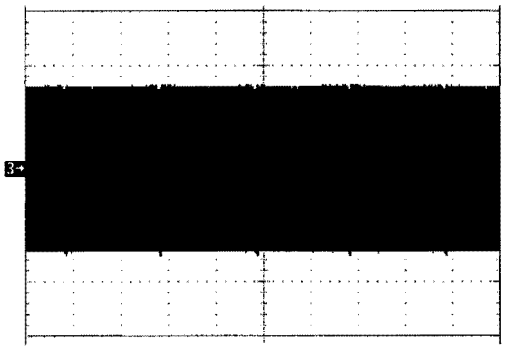


100V/div; 5μS/div

Figure 5-9 HF Lamp voltage

Figure 5-8 shows the inductive behaviour of the LCR output circuit. The output behaviour is important for the ballast converting efficiency. Proper choice of the switching frequency minimises the circulating current in the LCR network and minimises the current stress in the power switch. It is best to operate the LCR circuit at the boundary of inductive and capacitive load, equation F-4. However, for 220V mains voltage this can only be realized with a lamp voltage higher than $280V_{rms}$. For 115V mains voltage (USA) the lamp voltage should be higher than $146V_{rms}$.

Figure 5-9 shows that the lamp voltage is nearly sinusoidal which results in a low crest factor. Figure 5-10 shows the low frequency lamp voltage and figure 5-11 shows the frequency spectrum of the lamp current. It is shown that the lamp current only contains odd harmonics. The measured lamp current crest factor is 1.5.



200V/div; 5mS/div

Figure 5-10 LF Lamp voltage

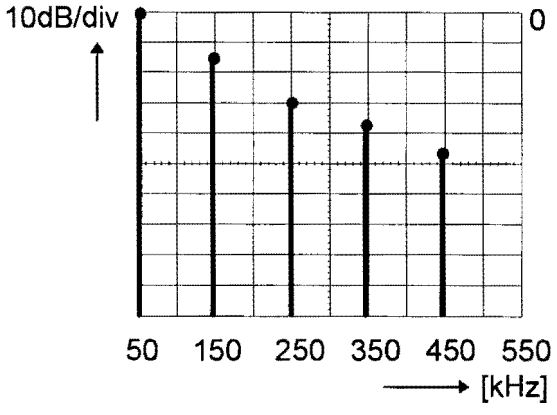
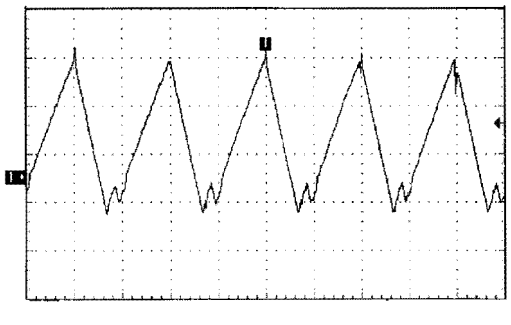


Figure 5-11 Frequency spectrum of the lamp current

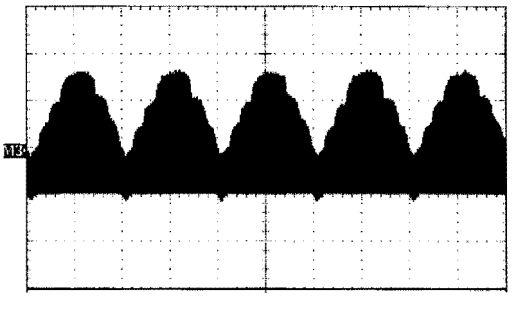
Input circuit:

Figure 5-12 shows the high frequency current through the input inductor (L_i) and figure 5-13 shows the low frequency, not filtered, current.



0.2A/div; 10μS/div

Figure 5-12 HF input inductor current

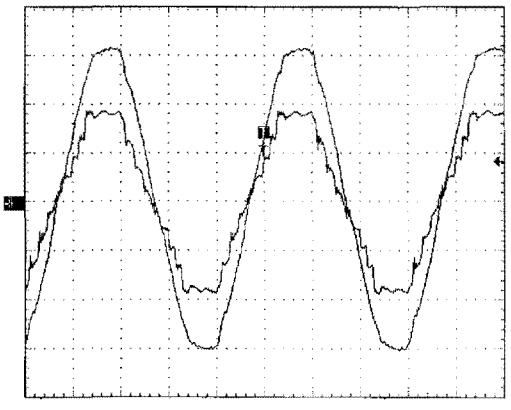


0.5A/div; 5mS/div

Figure 5-13 LF input inductor current

Figure 5-12 shows that the input inductor operates in discontinuous current mode and has a triangle shaped waveform.

Figure 5-14 shows the low frequency mains voltage and the filtered (L_f, C_f) input current. The mains current is nearly sinusoidal and in phase with the mains voltage. This results in high power factor pf=0.99 and low total harmonic distortion THD=12%.

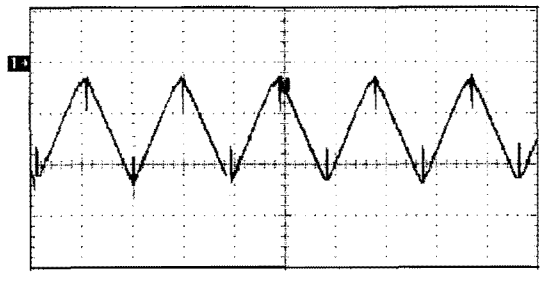


100V/div; 0.2A/div; 5mS/div

Figure 5-14 Mains voltage and mains current

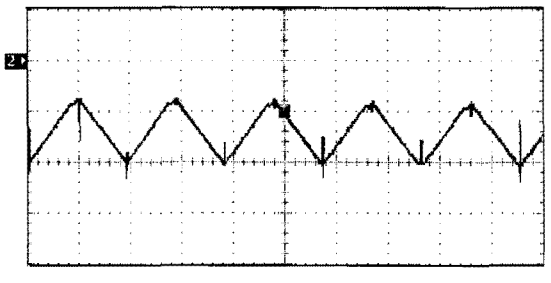
Power conversion stage:

Figure 5-15 and figure 5-16 show the high frequency current through the primary and secundary winding of the coupled inductors.



0.2A/div; 10µS/div

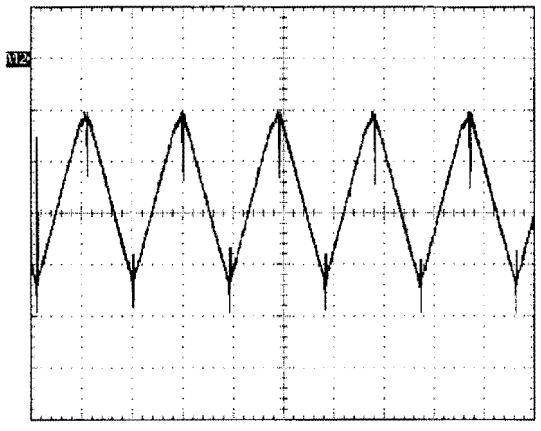
Figure 5-15 HF Prim. inductor current



0.2A/div; 10µS/div

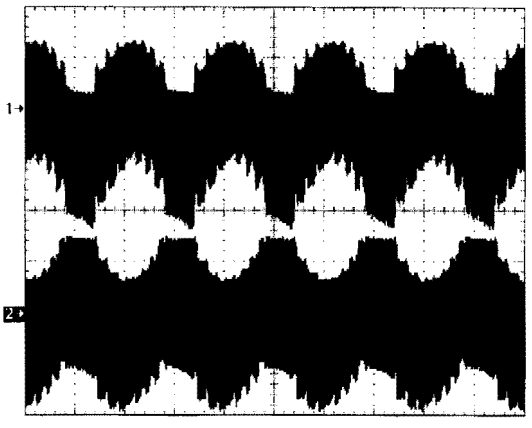
Figure 5-16 HF Sec. inductor current

The voltages across the coupled inductors alternate between an approximately constant positive and negative level during the on and off time of the switch. Therefore the inductor currents are triangle shaped. The sum of both currents, figure 5-17, has also a triangle shape.



0.2A/div; 10µS/div

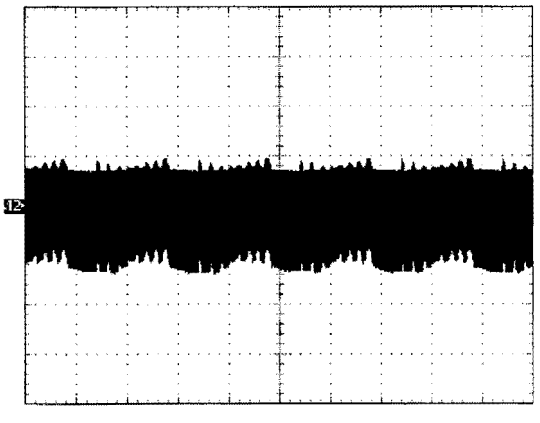
Figure 5-17 HF Prim. + Sec. current



0.2A/div; 5mS/div

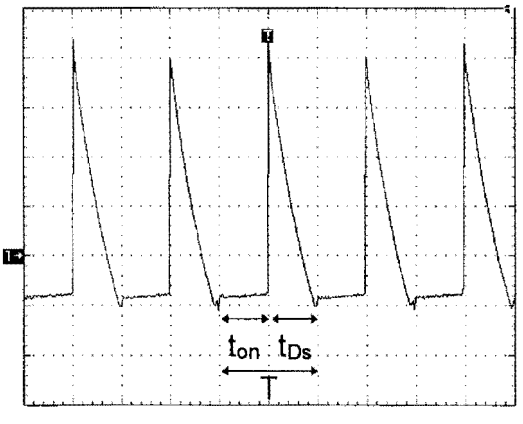
Figure 5-18 LF Prim. & Sec. current

The currents through the primary and secundary winding are measured with a dc current probe. Both currents show a dc-offset. The dc offset varies with the mains frequency, figure 5-18. However, if both currents are added, figure 5-19, the dc offset can be considered constant.



0.5A/div; 5mS/div

Figure 5-19 LF Prim. + Sec. current



0.5A/div; 10µS/div

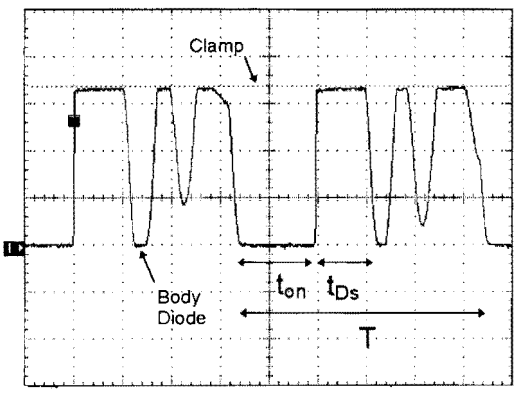
Figure 5-20 Clamp diode current

Figure 5-20 shows the current through the clamp diode. The clamp diode starts to conduct after time t_{on} when the switch is off and energy is supplied to the lamp and stored in the tank capacitor C_e. The conduction time of the diode t_{Ds} is approximately 50% for nominal operation.

5.4 WAVEFORMS, DIMMING OPERATION

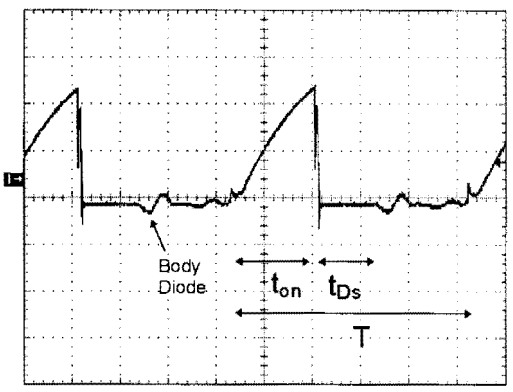
The major waveforms for dimming operation will be discussed with duty-cycle 25%. Waveforms which do not differ, besides the amplitude, from normal operation are not shown. The simulated waveforms match with the measured waveforms, therefore only the measured waveforms are shown.

Figure 5-21 shows the high frequency voltage across the switch and figure 5-22 shows the high frequency current through the switch.



200V/div; 4µS/div

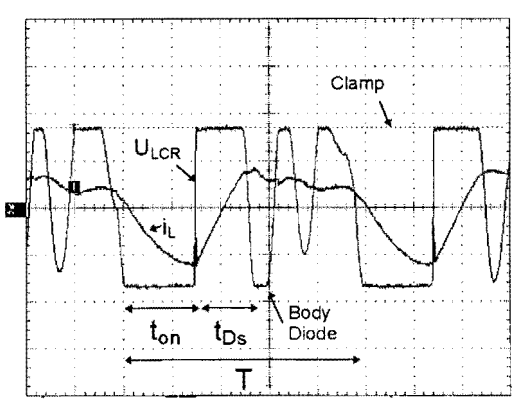
Figure 5-21 HF Drain-source voltage



0.5A/div; 4µS/div

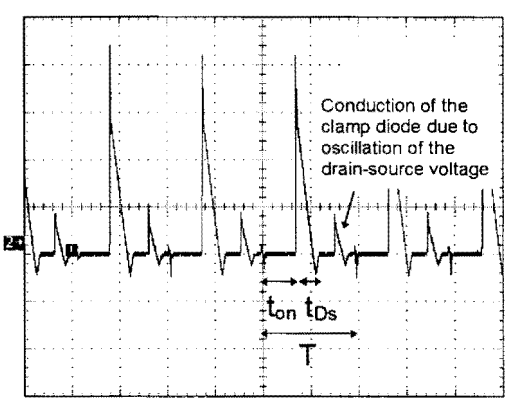
Figure 5-22 HF Drain-source current

Figure 5-21 shows that the drain-source voltage is well defined during time t_{on}, when the switch is on, and during time t_{Ds}, when the clamp diode (D_s) is conducting. The clamp diode stops conducting when the (discontinuous) input current is zero and the current through the primary + secundairy winding (magnetising inductor) equals the current through the output inductor (L). After time $t_{on}+t_{Ds}$ free oscillations occur. The voltage across the switch is limited by the clamp circuit and the body diode of the switch. Figure 5-23 shows the high frequency current through the output inductor (L). Figure 5-24 shows the current through the clamp diode, the diode conducts several times during the off time of the switch.



200V/div; 0.4A/div; 4µS/div

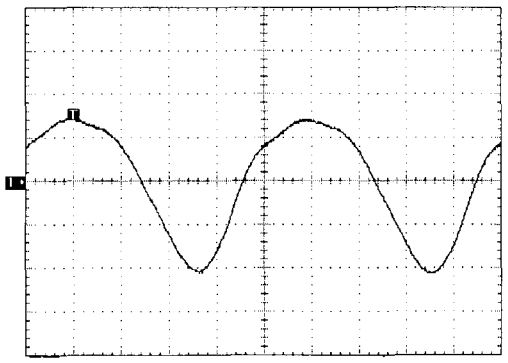
Figure 5-23 HF Output inductor current



0.4A/div; 10µS/div

Figure 5-24 HF Clamp diode current

Figure 5-25 shows the high frequency lamp voltage and figure 5-26 shows the frequency spectrum of the current through the lamp.



200V/div; 4μS/div
Figure 5-25 HF-Lamp voltage

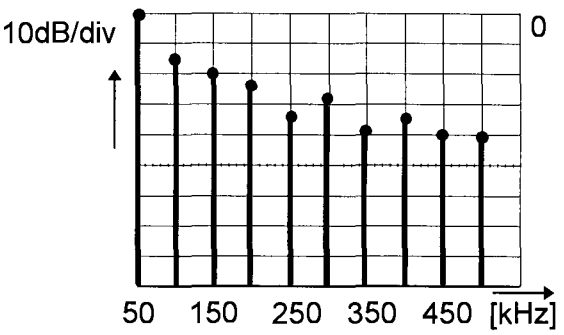
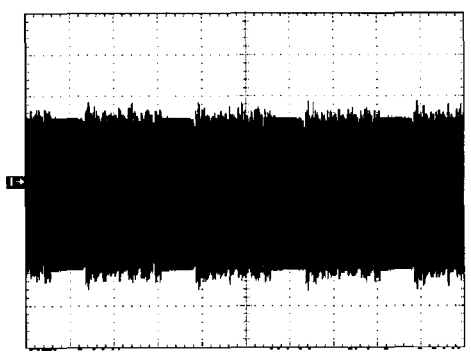
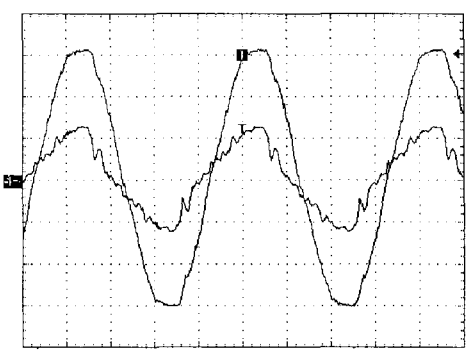


Figure 5-26 Frequency spectrum of the current through the lamp

For nominal operation the lamp voltage was sinusoidal and contained only odd harmonics. When dimming the lamp (PWM) even harmonics also occur in the lamp voltage. Figure 5-27 shows the low frequency lamp voltage. The measured lamp current crest factor is 1.8.



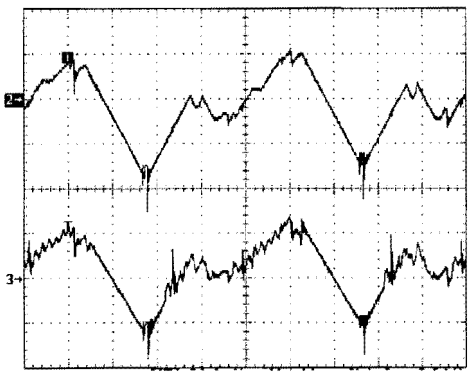
200V/div; 4mS/div
Figure 5-27 LF-Lamp voltage



100V/div; 0.1A/div 5μS/div
Figure 5-28 Mains voltage and current

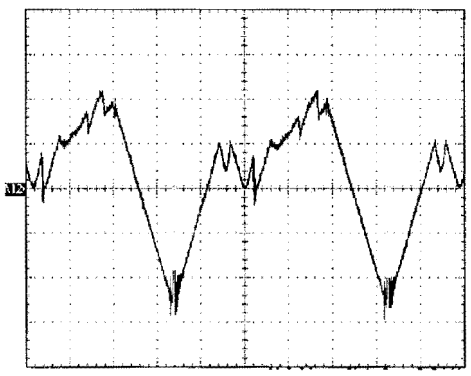
When dimming the lamp high power factor is maintained and the mains current remains nearly sinusoidal, figure 5-28.

Figure 5-29 shows the high frequency current through the primary and secundary winding of the coupled inductors and figure 5-30 shows the sum of both currents.



0.04A/div; 4μS/div

Figure 5-29 Prim. & Sec. current



0.04A/div; 4μS/div

Figure 5-30 Prim. + Sec. current

It is shown that the currents are linear during switch-on and during the conduction of the clamp diode D_s. Else the currents are very non linear.

5.5 SWITCH TYPE AND DRIVER CIRCUIT

The driver circuit is drawn in figure 5-31. A low voltage IC, SG3524, is used for the generation of the PWM signal. The output of the PWM generator is buffered by six inverters connected in parallel.

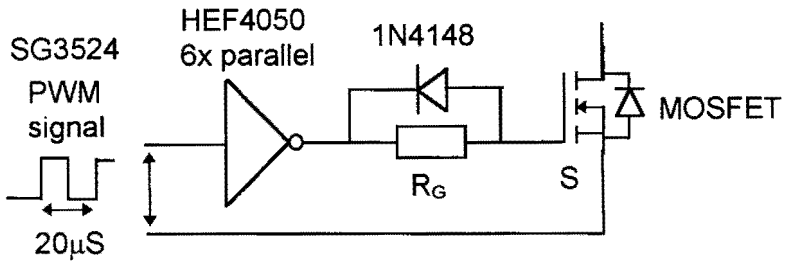


Figure 5-31 Driver circuit

The driver circuit provides fast turn-off ($t_{on}\approx$100ns) and slower turn-on ($t_{off}\approx$200ns). A slower turn-on time is required to prevent high current peaks caused by the discharge of the drain-source capacitance.

As a rule of thumb, the power dissipation in the MOSFET should not exceed 1.5W. Different types of MOSFETs were tested in the application because the power loss in the MOSFET first available (BUK456/800A) exceeded 1.5W. Table 5-2 shows the result of the calculated and measured values.

Table 5-2: Calculated and measured power dissipation in the MOSFET					
	Calculated			Measured	
Type MOSFET	P_{switch} [W]	P_{on} [W]	P_{tot} [W]	T_h [°C]	P_{tot} [W]
BUK456/800A	0.5	1.8	2.3	65-70	3.0
BUK456/1000B	0.5	3.0	3.5	85-90	5.5
STP4NA80	0.9	1.4	2.3	75-80	4.9
STP4NB80	-	-	-	75-80	4.9
STP6NA80	1.3	1	2.3	60-65	3.9
STH8NA80FI	1.5	0.9	2.4	60-65	3.9
STH9NA80FI	-	0.6	-	55-60	3.6

The power dissipation in the MOSFET is calculated with

$$P_{tot} = P_{switch} + P_{on} = \tfrac{1}{2}.C_{ds}.U_{DS}^{2}.f + i_{ds}^{2}.R_{ds(on)} \qquad (5\text{-}1)$$

where i_{ds}=0.77A, $U_{ds,max}$=650V, f=50kHz and $R_{ds(on)}$ at 25°C. The measured power dissipation is determined by temperature measurements. The temperature of the MOSFETs + heatsink (T_h) is measured after 5 minutes with an infrared temperature probe (Fluke 80T-IR). Then the power loss is calculated with;

$$P_{tot} \approx \frac{T_h - T_a}{Rth_{j-mb} + Rth_{mb-h} + Rth_{h-a}} \qquad (5\text{-}2)$$

where T_a=20°C, $Rth_{j\text{-}mb}$=1°C/W; $Rth_{mb\text{-}h}$=0.5°C/W, $Rth_{h\text{-}a}$=15°C/W.

Table 5-2 shows that non of the MOSFETs meet the requirement of P_{max}=1.5W. The measured power loss in the MOSFET is even higher than the estimated power loss. The difference between the calculated and measured value are for the greater part caused by the switching loss. Furthermore, the temperature dependency of the on-resistance is not taken into account.

Suggestions for lowering the power dissipation in the switch are;

1) lowering the switching frequency, disadvantage larger magnetic components,
2) changing the winding ratio of the coupled inductors, $u_{ds}=u_{ce}.[N_1+N_2]/N_1$; e.g. if $N_1=2.N_2$ then u_{ds} is $1.5*u_{mains}$,
3) intelligent switching, e.g. by using the voltage oscillations across the switch,
4) minimising the current through the switch, e.g. by operating the output circuit at the boundary of inductive and capacitive load or by increasing the value of the coupled inductors (equation 4-20),
5) finding a MOSFET with low on-resistance and low drain-source capacitance.

5.6 MAGNETIC DESIGN

Important data for designing an inductor are; current, inductance, core size, core material, flux density, and wire size. The inductor must be optimized for size and power losses. Given the inductance and the maximum current through the inductor, the airgap, number of turns and the core size can be determined using the following equations;

$$N_{min} = \frac{L.I_{max}}{B_{max}.A_{min}} \qquad \text{[turns]} \qquad (5\text{-}3)$$

$$x_{gap} = \frac{\mu_o.N_{min}.I_{max}}{B_{max}} \qquad \text{[m]} \qquad (5\text{-}4)$$

where;

N_{min} = minimum number of turns
B_{max} = maximum flux density (0.3 Vs/m^2)
A_{min} = minimum area of core cross-section
I_{max} = maximum current through choke
x_{gap} = size of the airgap
μ_o = permeability of air, $4.\pi.10^{-7}$ H/m
L = inductance of the inductor

A more accurate magnetic design is performed using a computer program called "CONV". Figure 5-32 shows an example of the program output.

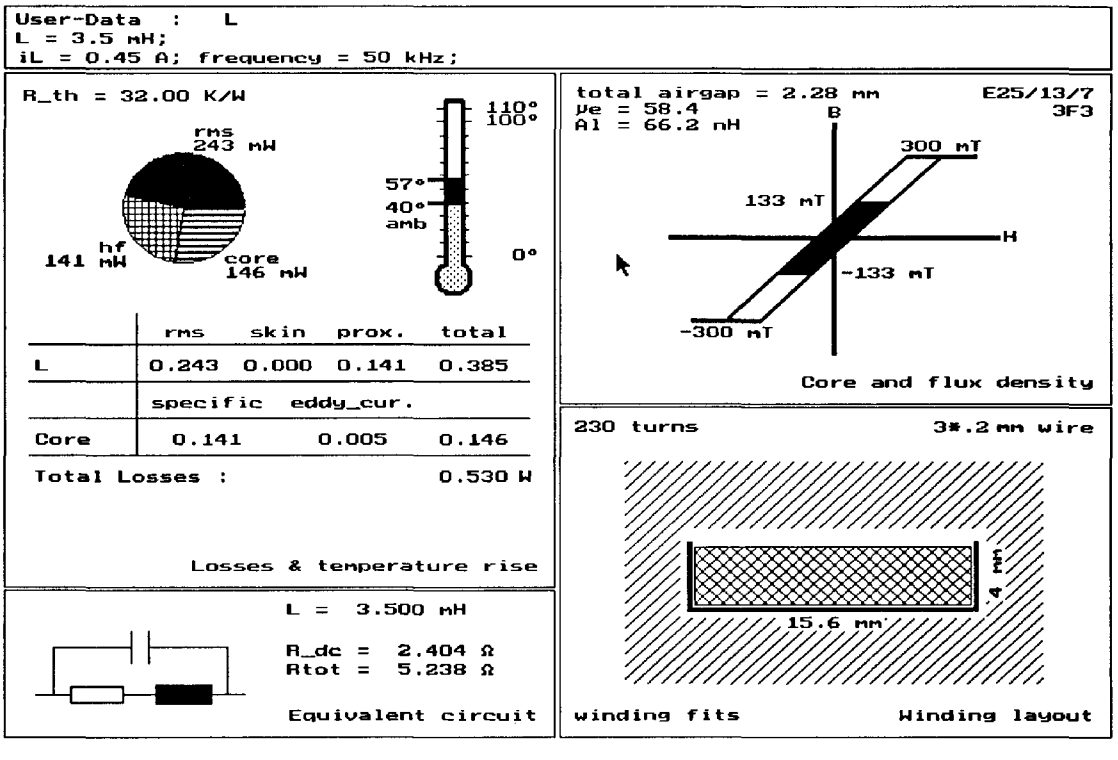


Figure 5-32 Example of "CONV" output.

The inductors are designed with 50% duty cycle of the switch, that is nominal operation. Figure 5-33 shows the simulated input current with the required design data.

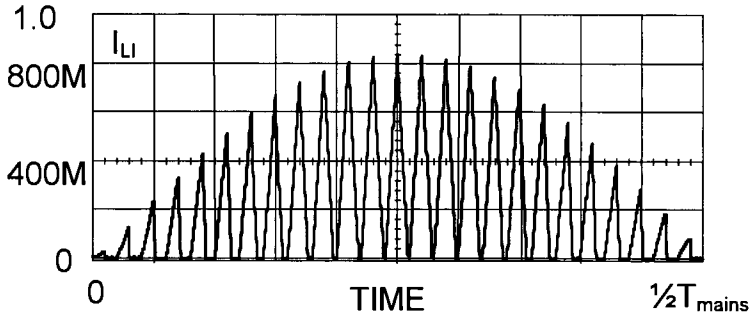


Figure 5-33 Input current L_i=3.5mH
max=0.833A; min=0A; avg=0.21A; rms=0.31A; ULi_max=650V

The input inductor is designed on a E25/13/7 core. Figure 5-34 shows the simulated output current with the required design data.

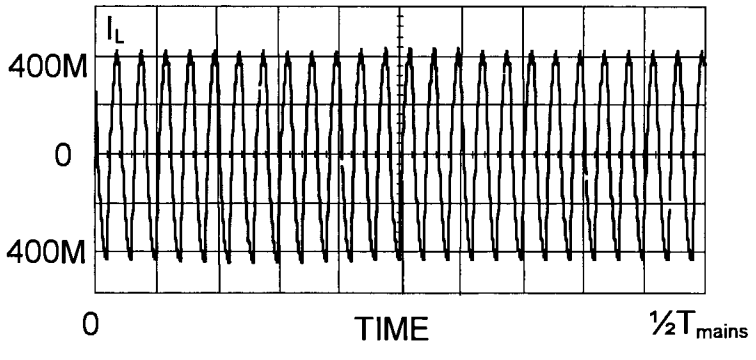


Figure 5-34 Output current L=3.55mH
max=0.43A; min=0.45A; avg=0.4A; rms=0.3A; UL_max=630V

The output inductor is also designed on a E25/13/7 core. Figure 5-35 shows the simulated current through the magnetising inductor with the required design data.

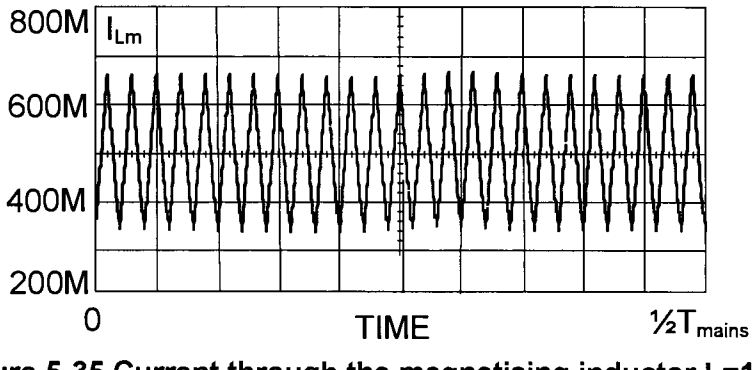


Figure 5-35 Current through the magnetising inductor L=10mH
max=0.68A; min=0.35A; avg=0.51A; rms=0.52A; ULm_max=400V

The output inductor is designed on a U20/16/7 core.

6. CONCLUSIONS

In the literature six interesting single switch ballasts were found. The ballasts show some important similarities.

- Each topology has an input EMI filter and an input inductor operating in discontinuous current mode for high frequency energy transfer and high power factor.
- All ballasts fulfil the IEC 1000-3-2 class C requirements concerning line current harmonic distortion.
- Each topology consists of an energy storage circuit which prevents the lamp from being turned off each zero crossing of the mains voltage.
- The switch of each topology can be controlled with a low cost driver circuit; no level shifters are needed.
- The output circuit is often a series resonant circuit, a parallel resonant circuit or a combination of both.

Through analysis of a series- and a parallel resonant soft-switching ballast topology it has been proved that these type of circuits are not very attractive as a ballast. The operation of the circuit strongly depends on the load (lamp resistance) and light dimming is not possible.

Tight investigation of a single switch ballast has proved that such a ballast has the opportunity to be small and cost effective and can compete with present ballasts. The voltage stress on the power switch is relatively low compared to other single switch ballasts, that is 1.5 up to 2.5 times the mains voltage peak.

Referring to the single switch ballasts found in literature; single switch ballasts require more magnetic components (in the form of inductors) than the present ballasts but less silicon is used. Compared to up-converter/half-bridge topologies a high-voltage IC and a switch (half-bridge) is exchanged with a high-voltage/high-current switch. Also a switch (half-bridge) is exchanged with an inductor.

7. RECOMMENDATIONS + FOLLOW UP

A major drawback of the investigated ballast is the power loss in the semiconductor switch (3 - 4W). Future work has to be done to minimize the power dissipation in the switch.

Yet, no attention has been paid to filament (pre-)heating and lamp power control. Further investigation of the ballast and/or other single switch ballasts (mentioned in this report) is recommended since not all possibilities have been exploited.

Patents;

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[2] Konopka, J.G. and P.W. Shackle; HIGH-POWER FACTOR CIRCUIT FOR ENERGIZING GAS DISCHARGE LAMPS., Applicant: Motorola Lighting Inc., 16 Feb. 1993, Washington D.C.: Patent Cooperation Treaty (PCT), Patent Number 5374875.

[3] Konopka, J.G. and P.W. Shackle; SINGLE TRANSISTOR BALLAST FOR GAS DISCHARGE LAMPS., Applicant: Motorola Lighting Inc., 29 Oct. 1993, Washington D.C.: Patent Cooperation Treaty (PCT), PCT/US94/10437, Patent Number 5399944.

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Articles;

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Figure B-1 shows the circuit to be evaluated.

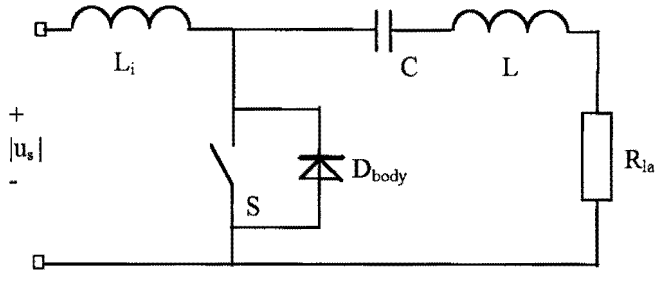

Figure B-1 Series resonant soft-switching topology

Two operating modes occur during a switching period, depending on the switch status. During a switching period the rectified mains voltage $|u_s|$ is assumed to be constant with amplitude U_s. Figure B-2 shows the switched circuit when the switch and/or body diode is conducting.

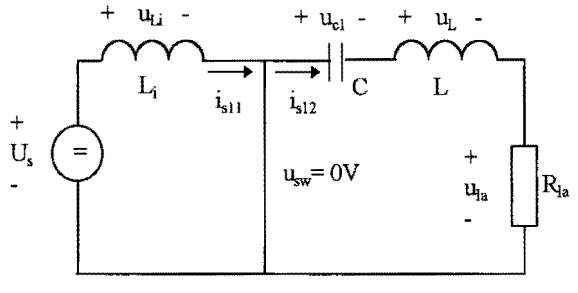

Figure B-2 Mode I: switch on and/or conducting body diode

We define the state vector x and calculate the matrices A_{s1}, B_{s1} as:

$$x_{s1} = \begin{bmatrix} i_{s11} \\ i_{s12} \\ u_{c1} \end{bmatrix}, \quad A_{s1} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & -R/L & -1/L \\ 0 & -1/C & 0 \end{bmatrix}, \quad B_{s1} = \begin{bmatrix} 1/Li \\ 0 \\ 0 \end{bmatrix} \qquad \text{(B-1)}$$

The control vector $u = U_s$. The signals defined by the state vector x are also the signals to be observed, therefore the output vector y is not needed. Signals $i_{s11}(t)$, $i_{s12}(t)$ and $u_{c1}(t)$ are obtained using Laplace.

We find:

$$i_{s11}(t) = \frac{U_s}{L_i}.t + i_{s11}(0) \qquad \text{(B-2)}$$

$$i_{s12}(t) = e^{-\alpha_1 t}\left[\frac{\frac{1}{2}.R_{la}.i_{s12}(0) - u_{c1}(0)}{\omega_1.L}.\sin(\omega_1.t) + i_{s12}(0).\cos(\omega_1.t)\right] \qquad \text{(B-3)}$$

$$u_{c1}(t) = e^{-\alpha_1 t}\left[\left(\frac{R_{la}.u_{c1}(0)}{2.\omega_1.L} + \frac{i_{s12}(0)}{\omega_1.C}\right).\sin(\omega_1.t) + u_{c1}(0).\cos(\omega_1.t)\right] \qquad \text{(B-4)}$$

with $i_{s11}(0) = i_{s12}(0)$ and we have;

$$\alpha_1 = \frac{R_{la}}{2L}, \qquad \omega_1 = \sqrt{\frac{1}{LC} - \frac{R_{la}^2}{4L^2}}, \qquad R_{cr} = 2\sqrt{\frac{L}{C}} \qquad R_{la} < R_{cr}. \qquad \text{(B-5)}$$

The constant α_1 is the damping time constant and ω_1 is the damped oscillation frequency [rad/sec] of the resonant circuit in mode I.

Figure B-3 shows the switched circuit when the switch and body diode are blocking.

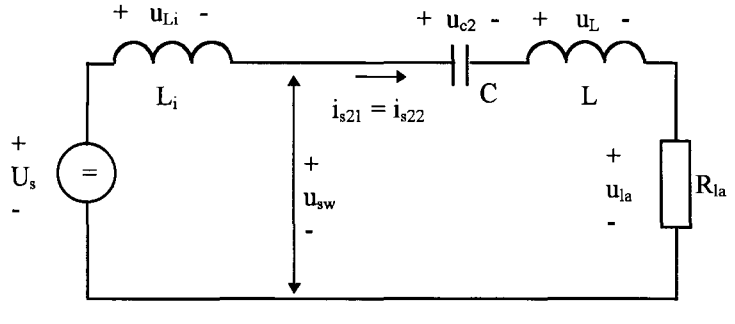

Figure B-3 Mode II: switch off and blocking body diode

The matrices A_{s2}, B_{s2} are:

$$A_{s2} = \begin{bmatrix} -R_{la}/L_T & 0 & -1/L_T \\ -R_{la}/L_T & 0 & -1/L_T \\ 1/C & 0 & 0 \end{bmatrix}, \quad B_{s2} = \begin{bmatrix} 1/L_T \\ 1/L_T \\ 0 \end{bmatrix} \quad \text{with } L_T = Li + L \qquad \text{(B-6)}$$

Signals $i_{s21}(t)=i_{s22}(t)$ and $u_{c2}(t)$ are obtained using Laplace.

$i_{s21}(t)= i_{s22}(t)$: (B-7)

$$i_{s22}(t) = e^{-\alpha_2.t}\left[\frac{\left(U_s - u_{c2}(0) - \frac{1}{2}R_{la}.i_{s22}(0)\right)}{\omega_2.L_T}.\sin(\omega_2.t) + i_{s22}(0).\cos(\omega_2.t)\right] \quad \text{(B-8)}$$

$$u_{c2}(t) = e^{-\alpha_2.t}\left[\left(u_{c2}(0) - U_s\right).\cos(\omega_2.t) + \left(\frac{i_{s22}(0)}{\omega.C} + \frac{\left(u_{c2}(0) - U_s\right).R_{la}}{2\omega.L_T}\right).\sin(\omega_2.t)\right] + U_s \quad \text{(B-9)}$$

with $\alpha_2 = \frac{R_{la}}{2L_T}$, $\omega_2 = \sqrt{\frac{1}{L_T C} - \frac{R_{la}^2}{4L_T^2}}$, $R_{cr} = 2\sqrt{\frac{L_T}{C}}$, $R_{la} < R_{cr}$, $L_T = L_i + L$ (B-10)

The constant α_2 is the damping time constant and ω_2 is the damped oscillation frequency [rad/sec] of the resonant circuit in mode II.

Voltage across the switch:
During mode II, the voltage across the switch can be calculated with;

$$u_{sw}(t) = U_s - u_{Li}(t) = U_s - L_i.\frac{di_{s22}(t)}{dt} \quad \text{(B-11)}$$

If we substitute equation (B-8) into (B-11), the expression for $u_{sw}(t)$ is obtained.

Maximum voltage across the switch:
During mode II, the switch voltage is given by:

$$u_{sw}(t) = u_{c2}(t) + L\frac{di_{s22}(t)}{dt} + i_{s22}(t).R_{la} \quad \text{(B-12)}$$

The capacitor voltage $u_c(t)$ and the currents during a switching cycle are drawn in figure B-4. During mode I (t_{on}), voltage $u_{c1}(t)$ and current $i_{s12}(t)$ have a damped oscillation, whose duration approaches $T_o \approx t_{on}$. When the switch is turned on, current $i_{s11}(t)$ increases linearly under the action of supply voltage U_s, which is entirely applied to inductor L_i. When the body diode ends conduction, mode II applies. The current $i_{s21}(t)=i_{s22}(t)$ flows into the resonant path, whose oscillation frequency becomes determined by the series of L_i and L. With L_i » L the oscillation frequency of the circuit drops, accordingly the behaviour of the current and the capacitor voltage becomes nearly linear, figure B-4.

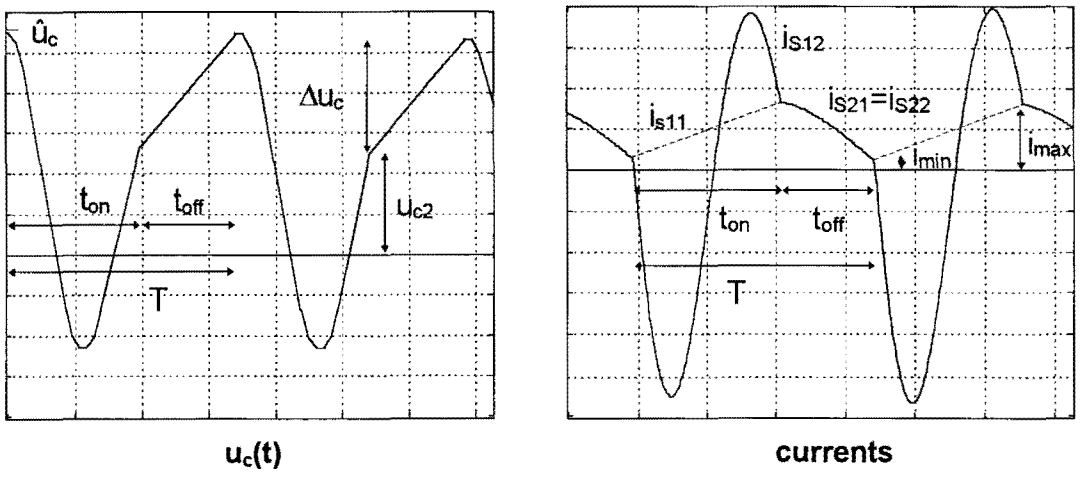

Figure B-4 Capacitor voltage $u_c(t)$ and currents during a switching cycle

The capacitor voltage u_{c2} after time t_{on} can be calculated as:

$$u_{c2} = \hat{u}_c . e^{-\frac{R_{la}}{2.L} . t_{on}} \qquad \text{(B-13)}$$

With $\hat{u}_c = u_{c2} + \Delta u_c$ we have;

$$\hat{u}_c = \frac{1}{1 - e^{-\frac{R_{la}}{2.L} . t_{on}}} . \Delta u_c \qquad \text{(B-14)}$$

If we assume the current $i_{s22}(t)$ to be linear during t_{off}, see figure B-5;

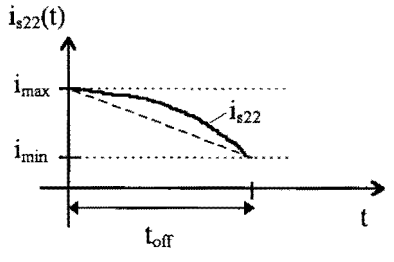

Figure B-5 Linearization of current $i_{s22}(t)$ during t_{off}

Then we can calculate Δu_c as;

$$\Delta u_c = \frac{1}{C}\int_{t_{off}} i_{s22}(t).dt = \frac{\frac{1}{2}.(i_{max}+i_{min})}{C}.t_{off} \qquad \text{(B-15)}$$

Thus during t_{off}, voltage u_c rises linearly. If we substitute equation (B-15) into (B-14) we obtain;

$$\hat{u}_c = \left[1-e^{-\frac{R_{la}}{2.L}.t_{on}}\right]^{-1}.\frac{\frac{1}{2}.(i_{max}+i_{min})}{C}.t_{off} \qquad \text{(B-14)}$$

The voltage drop across inductor L is very small compared to voltage across the capacitor C (u_{c2}) and may be neglected. The switch voltage is at its maximum at the end of the switching period. From equation (B-12) we obtain;

$$\hat{u}_{sw} \approx \hat{u}_c + i_{min}.R_{la} \qquad \text{(B-15)}$$

$$\hat{u}_{sw} = \left[1-e^{-\frac{R_{la}}{2.L}.t_{on}}\right]^{-1}.\frac{\frac{1}{2}.(i_{max}+i_{min})}{C}.t_{off} + i_{min}.R_{la} \qquad \text{(B-16)}$$

Figure C-1 shows the circuit to be evaluated.

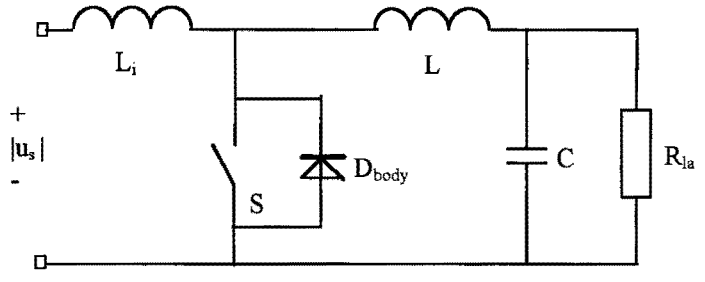

Figure C-1 Parallel resonant soft-switching topology

Two operating modes occur during a switching period, depending on the switch status. During a switching period the rectified mains voltage $|u_s|$ is assumed to be constant with amplitude U_s. Figure C-2 shows the switched circuit when the switch is on and/or the body diode are conducting.

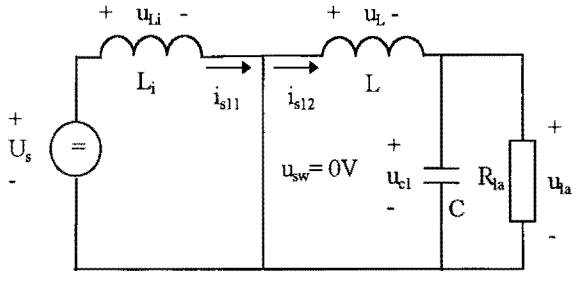

Figure C-2 Mode I: switch on and/or conducting body diode

We define the state vector x and calculate the matrices A_{s1}, B_{s1} as:

$$x_{s1} = \begin{bmatrix} i_{s11} \\ i_{s12} \\ u_{c1} \end{bmatrix}, \quad A_{s1} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & -1/L \\ 0 & 1/C & -1/R_{la}C \end{bmatrix}, \quad B_{s1} = \begin{bmatrix} 1/Li \\ 0 \\ 0 \end{bmatrix} \qquad \text{(C-1)}$$

The control vector $u = U_s$. The signals defined by the state vector x are also the signals to be observed, therefore the output vector y is not needed. Signals $i_{s11}(t)$, $i_{s12}(t)$ and $u_{c1}(t)$ are obtained using Laplace.

We find:

$$i_{s11}(t) = \frac{U_s}{L_i}.t + i_{s11}(0) \qquad \text{(C-2)}$$

$$i_{s12}(t) = e^{-\alpha_1.t}\left[\frac{i_{s12}(0)}{2\omega_1 R_{la} C} - \frac{u_{c1}(0)}{\omega_1.L}.\sin(\omega_1.t) + i_{s12}(0).\cos(\omega_1.t)\right] \qquad \text{(C-3)}$$

$$u_{c1}(t) = e^{-\alpha_1.t}\left[\left(\frac{i_{s12}(0)}{\omega_1.C} - \frac{u_{c1}(0)}{2.\omega_1.R_{la}.C} + \right).\sin(\omega_1.t) + u_{c1}(0).\cos(\omega_1.t)\right] \qquad \text{(C-4)}$$

with $i_{s11}(0) = i_{s12}(0)$ and

$$\alpha_1 = \frac{1}{2R_{la}C}, \quad \omega_1 = \sqrt{\frac{1}{LC} - \frac{1}{4R_{la}{}^2C^2}}, \quad R_{cr} = \tfrac{1}{2}\sqrt{\frac{L}{C}}, \quad R_{la} > R_{cr} \qquad \text{(C-5)}$$

The constant α_1 is the damping time constant and ω_1 is the damped oscillation frequency of the resonant circuit [rad/sec] during mode I.

Figure C-3 shows the switched circuit when the switch and body diode are blocking.

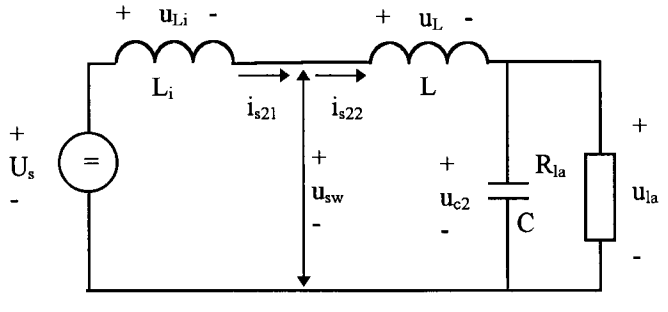

Figure C-3 Mode II: switch and body diode are blocking

The matrices A_{s2}, B_{s2} are:

$$A_{s2} = \begin{bmatrix} 0 & 0 & -1/L_T \\ 0 & 0 & -1/L_T \\ 0 & 1/C & -1/R_{la}C \end{bmatrix}, \quad B_{s2} = \begin{bmatrix} 1/L_T \\ 1/L_T \\ 0 \end{bmatrix} \text{ with } L_T = L_i + L \qquad \text{(C-6)}$$

Signals $i_{s21}(t)=i_{s22}(t)$ and $u_{c2}(t)$ are obtained using Laplace. We find:

$i_{s21}(t)= i_{s22}(t)$: (C-7)

$$i_{s22}(t) = e^{-\alpha_2.t}\left[\left(\frac{(U_s - u_{c2}(0))}{\omega_2.L_T} + \frac{\left(i_{s22}(0) - U_s/R_{la}\right)}{2.\omega_2.R_{la}.C}\right).\sin(\omega_2.t) + \left(i_{s22}(0) - \frac{U_s}{R_{la}}\right).\cos(\omega_2.t)\right] \quad \text{(C-8)}$$

$$u_{c2}(t) = e^{-\alpha_2.t}\left[\left(u_{c2}(0) - U_s\right).\cos(\omega_2.t) + \left(\frac{2.R_{la}.i_{s22}(0) - u_{c2}(0) - U_s}{2.\omega.R_{la}.C}\right).\sin(\omega_2.t)\right] + U_s$$

with $\alpha_2 = \frac{1}{2R_{la}C}$, $\omega_2 = \sqrt{\frac{1}{L_T C} - \frac{1}{4R_{la}^2 C^2}}$, $R_{cr} = \frac{1}{2}\sqrt{\frac{L_{la}}{C}}$, $R_{la} > R_{cr}$ (C-9)

The constant α_2 is the damping time constant and ω_2 is the damped oscillation frequency of the resonant circuit [rad/sec] during mode II.

Voltage across the switch:
During mode II, the voltage across the switch can be calculated as;

$$u_{sw}(t) = U_s - u_{Li}(t) = U_s - L_i.\frac{di_{s22}(t)}{dt} \quad \text{(C-10)}$$

If we substitute equation (C-8) into (C-11), the expression for $u_{sw}(t)$ is obtained.

Maximum voltage across the switch:
During mode II, the switch voltage is given by:

$$u_{sw}(t) = L\frac{di_{s22}(t)}{dt} + u_{c2}(t) \quad \text{(C-11)}$$

Capacitor voltage $u_c(t)$ and the currents during a switching cycle are drawn in figure C-4. During mode I (t_{on}), voltage $u_{c1}(t)$ and current $i_{s12}(t)$ have a damped oscillation, whose duration approaches $T_o \approx t_{on}$. When the switch is turned on, current $i_{s11}(t)$ increases linearly under the action of supply voltage U_s, which is entirely applied to inductor L_i.

When the body diode ends conduction, mode II applies. The current $i_{s21}(t)=i_{s22}(t)$ flows into the resonant path, whose oscillation frequency becomes determined by the series of L_i and L. With L_i » L the oscillation frequency of the circuit drops, accordingly the behaviour of the current and the capacitor voltage becomes nearly linear, figure C-4.

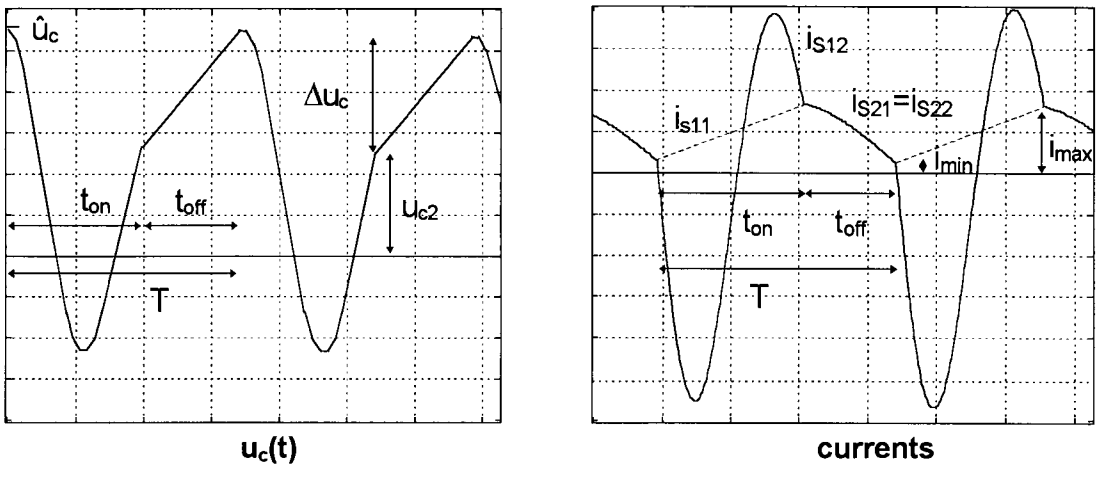

Figure C-4 Capacitor voltage $u_c(t)$ and currents during a switching cycle

The capacitor voltage u_{c2} after time t_{on} can be calculated as:

$$u_{c2} = \hat{u}_c . e^{-\frac{1}{2R_{la}C} \cdot t_{on}} \qquad \text{(C-12)}$$

With $\hat{u}_c = u_{c2} + \Delta u_c$ we have;

$$\hat{u}_c = \frac{1}{1 - e^{-\frac{1}{2.R_{la}C} \cdot t_{on}}} . \Delta u_c \qquad \text{(C-13)}$$

If we assume the current $i_C(t)$ to be linear during t_{off} , see figure C-5;

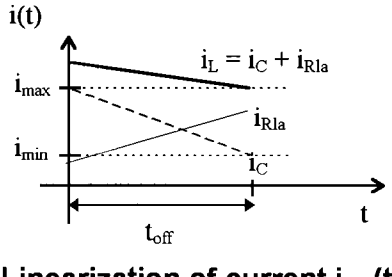

Figure C-5 Linearization of current $i_{s23}(t)$ during t_{off}

Then we can calculate Δu_c as;

$$\Delta u_c = \frac{1}{C}\int_{t_{off}} i_C(t).dt = \frac{\frac{1}{2}.(i_{\max}+i_{\min})}{C}.t_{off} \qquad \text{(C-14)}$$

Thus during t_{off}, voltage u_c rises linearly. If we substitute equation (C-14) into (C-13) we obtain;

$$\hat{u}_c = \left[1-e^{-\frac{1}{2.R_{la}C}.t_{on}}\right]^{-1}.\frac{\frac{1}{2}.(i_{\max}+i_{\min})}{C}.t_{off} \qquad \text{(C-15)}$$

The voltage drop across inductor L is very small compared to voltage across the capacitor C (u_{c2}) and may be neglected. The switch voltage is at its maximum at the end of the switching period. From Eq. (C-11) we obtain;

$$\hat{u}_{sw} \approx \hat{u}_c = \left[1-e^{-\frac{1}{2.R_{la}C}.t_{on}}\right]^{-1}.\frac{\frac{1}{2}.(i_{\max}+i_{\min})}{C}.t_{off} \qquad \text{(C-16)}$$

State 1:

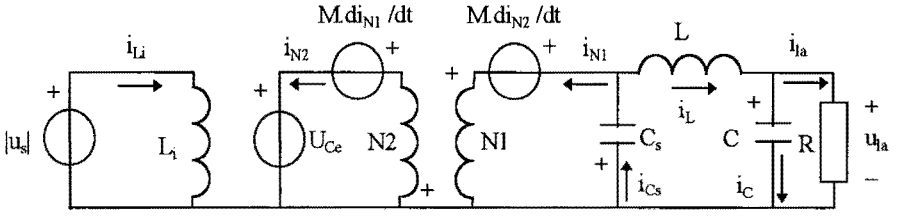

Figure D-1 Linear switched circuit model for State I

Condition: $u_{ds}=0$

State vector:

$$x = \begin{bmatrix} i_{Li} & i_L & i_{N2} & i_{N1} & u_{Cs} & u_C \end{bmatrix}^T$$

Control vector:

$u = [\, u_s \; U_{ce} \,]^T$.

Matrices A_{s1}, B_{s1}:

$$A_{s1} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L} & \frac{-1}{L} \\ 0 & 0 & 0 & 0 & \frac{-M}{M^2-N2N1} & 0 \\ 0 & 0 & 0 & 0 & \frac{M^2}{N1(M^2-N2N1)} - \frac{1}{N1} & 0 \\ 0 & \frac{1}{C_s} & 0 & \frac{1}{C_s} & 0 & 0 \\ 0 & \frac{1}{C} & 0 & 0 & 0 & \frac{-1}{R.C} \end{bmatrix},$$

$$B_{s1} = \begin{bmatrix} \frac{1}{Li} & 0 \\ 0 & 0 \\ 0 & \frac{N1}{M^2-N2N1} \\ 0 & \frac{-M}{M^2-N2N1} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}.$$

State II:

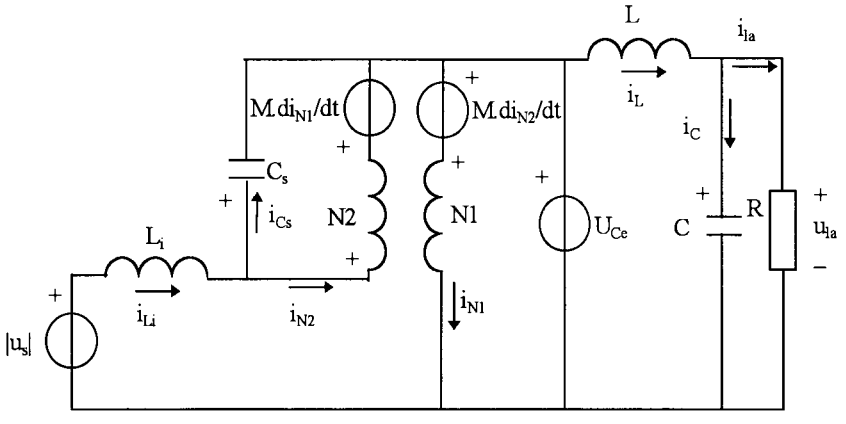

Figure D-2 Linear switched circuit model for State II

Condition: $u_{ds} = u_{cs} + u_{ce}$

State vector:

$$x = \left[i_{Li} \quad i_L \quad i_{N2} \quad i_{N1} \quad u_{Cs} \quad u_C \right]^T$$

Control vector:

$u = [\, u_s \; U_{ce} \,]^T$.

Matrices A_{s2}, B_{s2}:

$$A_{s2} = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{-1}{Li} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L} \\ 0 & 0 & 0 & 0 & \frac{-M^2}{N2(M^2-N1N2)} + \frac{1}{N2} & 0 \\ 0 & 0 & 0 & 0 & \frac{M}{M^2-N1N2} & 0 \\ \frac{1}{C_s} & 0 & \frac{-1}{C_s} & 0 & 0 & 0 \\ 0 & \frac{1}{C} & 0 & 0 & 0 & \frac{-1}{R.C} \end{bmatrix},$$

$$B_{s2} = \begin{bmatrix} \frac{1}{Li} & \frac{-1}{Li} \\ 0 & \frac{1}{L} \\ 0 & \frac{M}{M^2-N2N1} \\ 0 & \frac{-N2}{M^2-N2N1} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}.$$

State III:

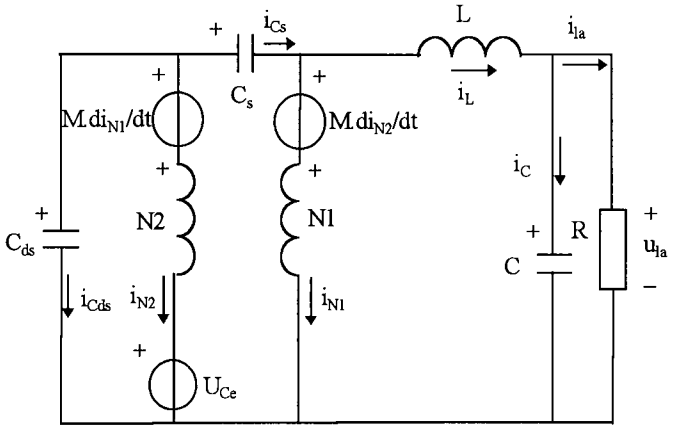

Figure D-3 Linear switched circuit model for State III

State vector:

$$x = \left[i_{Li} \quad i_L \quad i_{N2} \quad i_{N1} \quad u_{cs} \quad u_c \quad u_{ds} \right]^T$$

Control vector:

u =[u_s U_{ce}]^T.

Matrices A_{s3}, B_{s3}:

$$A_{s3} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L} & \frac{-1}{L} & \frac{1}{L} \\ 0 & 0 & 0 & 0 & \frac{-M}{M^2-N2N1} & 0 & \frac{M-N1}{M^2-N2N1} \\ 0 & 0 & 0 & 0 & \frac{M^2}{N1(M^2-N2N1)} - \frac{1}{N1} & 0 & \frac{-M(M-N1)}{N1(M^2-N2N1)} + \frac{1}{N1} \\ 0 & \frac{1}{C_s} & 0 & \frac{1}{C_s} & 0 & 0 & 0 \\ 0 & \frac{1}{C} & 0 & 0 & 0 & \frac{-1}{R.C} & 0 \\ 0 & \frac{-1}{C_{ds}} & \frac{-1}{C_{ds}} & \frac{-1}{C_{ds}} & 0 & 0 & 0 \end{bmatrix},$$

$$B_{s3} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & \frac{N1}{M^2-N2N1} \\ 0 & \frac{-M}{M^2-N2N1} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}.$$

State IV:

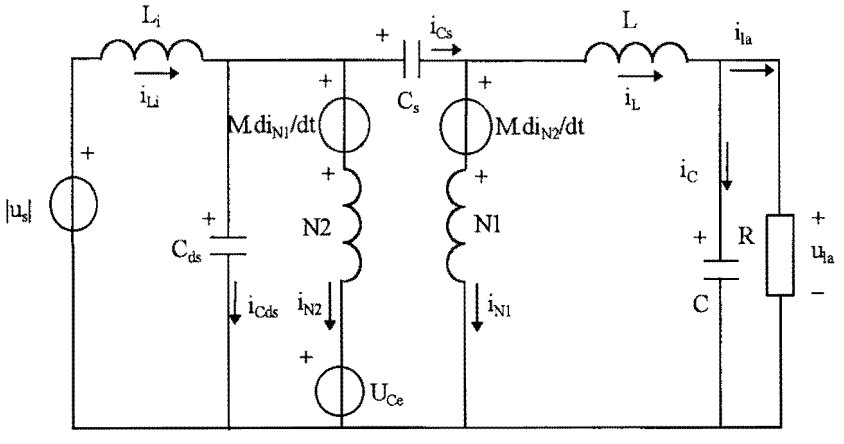

Figure D-4 Linear switched circuit model for State VI

State vector:

$$x = \left[i_{Li} \quad i_L \quad i_{N2} \quad i_{N1} \quad u_{cs} \quad u_c \quad u_{ds} \right]^T$$

Control vector:

$u = [\, u_s \; U_{ce} \,]^T$.

Matrices A_{s4}, B_{s4}:

$$A_{s4} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{Li} \\ 0 & 0 & 0 & 0 & \frac{-1}{L} & \frac{-1}{L} & \frac{1}{L} \\ 0 & 0 & 0 & 0 & \frac{-M}{M^2-N2N1} & 0 & \frac{M-N1}{M^2-N2N1} \\ 0 & 0 & 0 & 0 & \frac{M^2}{N1(M^2-N2N1)} - \frac{1}{N1} & 0 & \frac{-M(M-N1)}{N1(M^2-N2N1)} + \frac{1}{N1} \\ 0 & \frac{1}{C_s} & 0 & \frac{1}{C_s} & 0 & 0 & 0 \\ 0 & \frac{1}{C} & 0 & 0 & 0 & \frac{-1}{R.C} & 0 \\ \frac{1}{C_{ds}} & \frac{-1}{C_{ds}} & \frac{-1}{C_{ds}} & \frac{-1}{C_{ds}} & 0 & 0 & 0 \end{bmatrix},$$

$$B_{s4} = \begin{bmatrix} \frac{1}{Li} & 0 \\ 0 & 0 \\ 0 & \frac{N1}{M^2-N2N1} \\ 0 & \frac{-M}{M^2-N2N1} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}.$$

State 1:

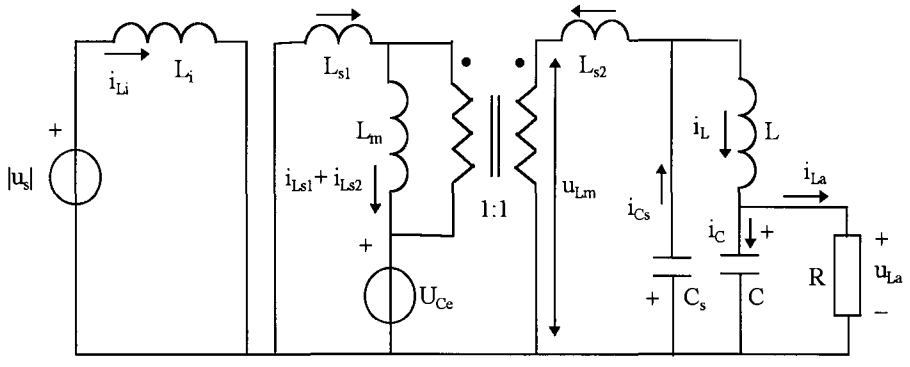

Figure E-1 Linear switched circuit model for State I

Condition: $u_{ds}=0$

State vector:

$$x = \begin{bmatrix} i_{Li} & i_{Ls1} & i_{Ls2} & i_L & u_{Cs} & u_C \end{bmatrix}^T,$$

Control vector:

$$u = \begin{bmatrix} |u_s| & U_{Ce} \end{bmatrix}^T$$

Matrices A_{s1}, B_{s1}:

$$A_{s1} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{k}{p} & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{p} & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L} & \frac{-1}{L} \\ 0 & 0 & \frac{1}{C_s} & \frac{1}{C_s} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C} & 0 & \frac{-1}{R.C} \end{bmatrix}, \qquad B_{s1} = \begin{bmatrix} \frac{1}{Li} & 0 \\ 0 & \frac{-1}{p} \\ 0 & \frac{k}{p} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}.$$

$$p = \frac{(1-k^2)}{k} * L_m$$

k =coupling coefficient

L_c =inductance of coupled inductors (1:1)

L_m =magnetising inductance (L_m=k.L_c)

L_{s1}=primary leakage inductance (L_{s1}=(1-k).L_c)

L_{s2}=secundary leakage inductance (L_{s2}= L_{s1})

State II:

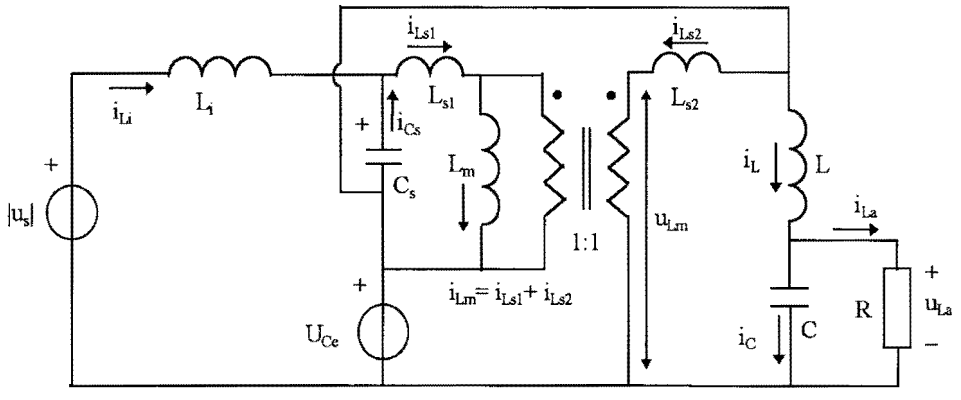

Figure E-2 Linear switched circuit model for State II

Condition: $u_{ds}= u_{cs}+ u_{ce}$

State vector:

$$x = \left[i_{Li} \quad i_{Ls1} \quad i_{Ls2} \quad i_L \quad u_{Cs} \quad u_C \right]^T,$$

Control vector:

$$u = \left[|u_s| \quad U_{Ce} \right]^T$$

Matrices A_{s2}, B_{s2}:

$$A_{s2} = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{-1}{Li} & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{p} & 0 \\ 0 & 0 & 0 & 0 & \frac{-k}{p} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L} \\ \frac{1}{C_s} & \frac{-1}{C_s} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C} & 0 & \frac{-1}{R.C} \end{bmatrix},$$

$$B_{s2} = \begin{bmatrix} \frac{1}{Li} & \frac{-1}{Li} \\ 0 & \frac{-k}{p} \\ 0 & \frac{1}{p} \\ 0 & \frac{1}{L} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}.$$

$$p = \frac{(1-k^2)}{k} * L_m$$

k =coupling coefficient

L_c =inductance of coupled inductors (1:1)

L_m =magnetising inductance (L_m=k.L_c)

L_{s1}=primary leakage inductance (L_{s1}=(1-k).L_c)

L_{s2}=secundary leakage inductance (L_{s2}= L_{s1})

State III:

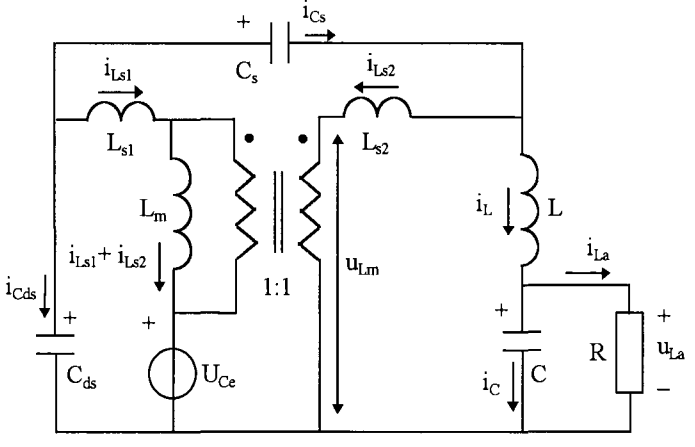

Figure E-3 Linear switched circuit model for State III

State vector:

$$x = \left[i_{Li} \quad i_{Ls1} \quad i_{Ls2} \quad i_L \quad u_{cs} \quad u_c \quad u_{ds} \right]^T$$

Control vector:

$u = [\, u_s \; U_{ce} \,]^T$.

Matrices A_{s3}, B_{s3}:

$$A_{s3} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{k}{p} & 0 & \frac{1-k}{p} \\ 0 & 0 & 0 & 0 & \frac{-1}{p} & 0 & \frac{1-k}{p} \\ 0 & 0 & 0 & 0 & \frac{-1}{L} & \frac{-1}{L} & \frac{1}{L} \\ 0 & 0 & \frac{1}{C_s} & \frac{1}{C_s} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C} & 0 & \frac{-1}{R.C} & 0 \\ 0 & \frac{-1}{C_{ds}} & \frac{-1}{C_{ds}} & \frac{-1}{C_{ds}} & 0 & 0 & 0 \end{bmatrix}, \qquad B_{s3} = \begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{p} \\ 0 & \frac{k}{p} \\ 0 & \frac{1}{L} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}.$$

$$p = \frac{(1-k^2)}{k} * L_m$$

k =coupling coefficient

L_c =inductance of coupled inductors (1:1)

L_m =magnetising inductance (L_m=k.L_c)

L_{s1}=primary leakage inductance (L_{s1}=(1-k).L_c)

L_{s2}=secundary leakage inductance (L_{s2}= L_{s1})

State IV:

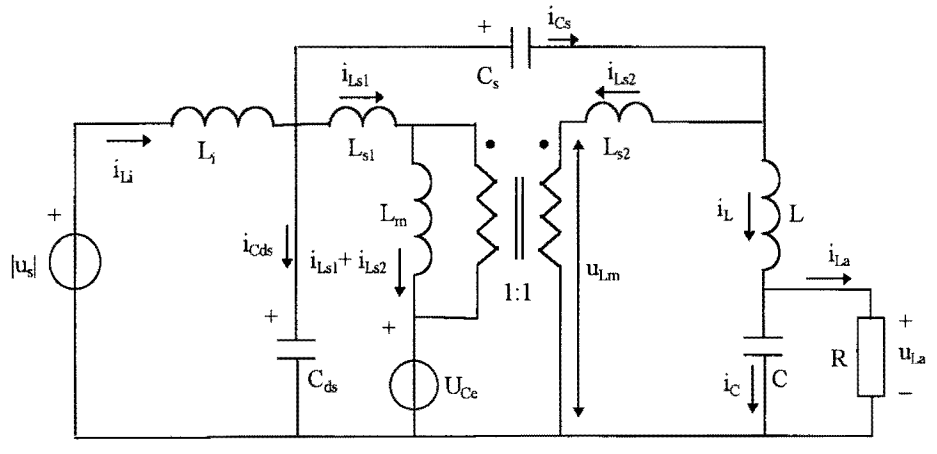

Figure E-4 Linear switched circuit model for State IV

State vector:

$$x = \left[i_{Li} \quad i_{Ls1} \quad i_{Ls2} \quad i_L \quad u_{cs} \quad u_c \quad u_{ds} \right]^T$$

Control vector:

u =[u_s U_{ce}]^T.

Matrices A_{s4}, B_{s4}:

$$A_{s4} = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{-1}{Li} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{k}{p} & 0 & \frac{1-k}{p} \\ 0 & 0 & 0 & 0 & \frac{-1}{p} & 0 & \frac{1-k}{p} \\ 0 & 0 & 0 & 0 & \frac{-1}{L} & \frac{-1}{L} & \frac{1}{L} \\ 0 & 0 & \frac{1}{C_s} & \frac{1}{C_s} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C_p} & 0 & \frac{-1}{R.C_p} & 0 \\ \frac{1}{C_{ds}} & \frac{-1}{C_{ds}} & \frac{-1}{C_{ds}} & \frac{-1}{C_{ds}} & 0 & 0 & 0 \end{bmatrix}, \qquad B_{s4} = \begin{bmatrix} \frac{1}{Li} & 0 \\ 0 & \frac{-1}{p} \\ 0 & \frac{k}{p} \\ 0 & \frac{1}{L} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}.$$

$$p = \frac{(1-k^2)}{k} * L_m$$

k =coupling coefficient

L_c =inductance of coupled inductors (1:1)

L_m =magnetising inductance (L_m=k.L_c)

L_{s1}=primary leakage inductance (L_{s1}=(1-k).L_c)

L_{s2}=secundary leakage inductance (L_{s2}= L_{s1})

Circuit to be analysed:

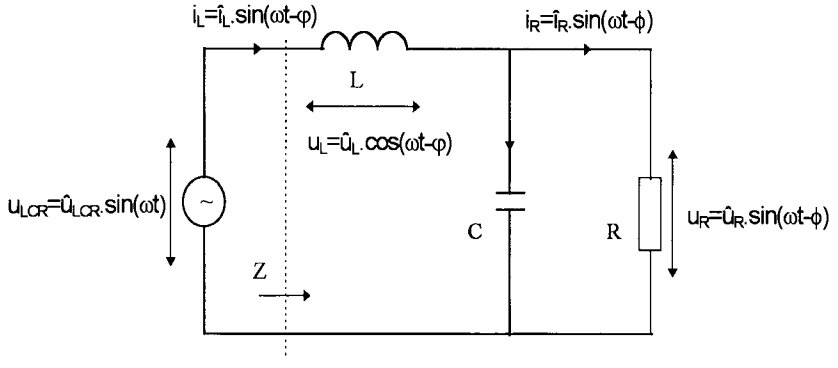

Figure F-1 Output circuit with LCR load network

Normalized parameters:

$$Z_o = \omega_o L = \frac{1}{\omega_o C} = \sqrt{\frac{L}{C}}$$ characteristic impedance (F-1)

$$Q = \omega_o RC = \frac{R}{\omega_o L} = \frac{R}{Z_o} = R\sqrt{\frac{C}{L}}$$ loaded quality factor at frequency ω_0 (F-2)

$$\omega_o = \frac{1}{\sqrt{LC}}$$ undamped natural frequency (F-3)

$$\omega_r = \sqrt{\omega_o^{\,2} - \frac{1}{(CR)^2}}$$ boundary between cap. and ind. loads (F-4)

$$\omega_r = \omega_o \cdot \sqrt{\left(1 - \tfrac{1}{Q^2}\right)}$$ for Q≥1 (F-5)

Typical Amplitude vs Frequency characteristic:

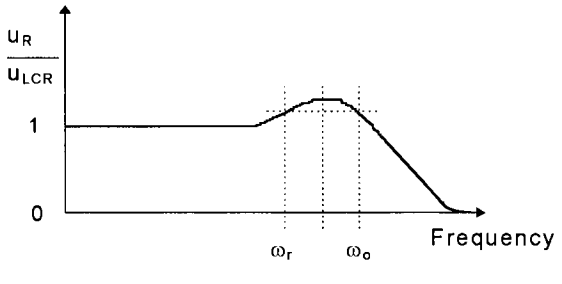

Figure F-2 Typical amplitude versus frequency characteristic

For Q≤1, ω_r does not exist and the resonant circuit represents an inductive load at any operating frequency. For Q>1, ω_r/ω_o increases with Q. For $\omega>\omega_r$, the impedance remains inductive and current i_L lags the voltage u_{LCR}. For $\omega<\omega_r$, the impedance remains capacitive and current i_L lags the voltage u_{LCR}.

Impedance $Z = |z|.e^{j\varphi}$:

$$|z| = Z_o \cdot \sqrt{\frac{Q^2\left(1-\left(\frac{\omega}{\omega_o}\right)^2\right)^2 + \left(\frac{\omega}{\omega_o}\right)^2}{1+\left(Q.\frac{\omega}{\omega_o}\right)^2}}, \qquad \varphi = \arctan\left\{Q.\frac{\omega}{\omega_o}.\left[\left(\frac{\omega}{\omega_o}\right)^2 + \frac{1}{Q^2} - 1\right]\right\} \quad \text{(F-6)}$$

Transfer function $H = |H|.e^{j\phi}$:

$$|H| = \frac{1}{\sqrt{\left(\frac{\omega}{\omega_o}\right)^2.\frac{1}{Q^2} + \left(1-\left(\frac{\omega}{\omega_o}\right)^2\right)^2}} = \frac{R}{Z_o}\frac{1}{\sqrt{\left(\frac{\omega}{\omega_o}\right)^2 + Q^2\left(1-\left(\frac{\omega}{\omega_o}\right)^2\right)^2}} \quad \text{(F-7)}$$

$$\phi = \arctan\left\{\left(\frac{\omega}{\omega_o}\right).\frac{1}{Q}.\frac{1}{1-\left(\frac{\omega}{\omega_o}\right)^2}\right\}$$

Current through inductor L:

$$i_L = \hat{i}_L.\sin(\omega.t-\varphi) \qquad \text{with} \qquad \hat{i}_L = \frac{\hat{u}_{LCR}}{|Z|} \quad \text{(F-8)}$$

Voltage across inductor L:

$$u_L = \hat{u}_L.\cos(\omega.t-\varphi) \qquad \text{with} \qquad \hat{u}_L = \omega.L.\hat{i}_L \quad \text{(F-9)}$$

Current through resistor R:

$$i_R = \hat{i}_R.\sin(\omega.t-\phi) \qquad \text{with} \qquad \hat{i}_R = \frac{\hat{u}_{LCR}.|H|}{R} \quad \text{(F-10)}$$

Voltage across resistor R:

$$u_R = \hat{u}_R.\sin(\omega.t-\phi) \qquad \text{with} \qquad \hat{u}_R = \hat{i}_R.R \quad \text{(F-11)}$$

Output power P_o:

$$P_o = \tfrac{1}{2}\hat{i}_R^{\,2}.R \qquad \text{(F-12)}$$

When $\omega=\omega_o$, we have:
Amplitude of current through inductor L:

$$\hat{i}_L = \frac{\hat{u}_{LCR}}{Z_o}.\sqrt{Q^2+1} \quad \text{and with } Q^2>>1 \text{ we have } \hat{i}_L = \frac{\hat{u}_{LCR}}{Z_o^{\,2}}.R \qquad \text{(F-13)}$$

Thus, $\hat{i}_L$ is directly proportional to R.

Amplitude of voltage across inductor L:

$$\hat{u}_L = \hat{u}_i.\sqrt{Q^2+1} \qquad \text{(F-14)}$$

Amplitude of current through resistor R:

$$\hat{i}_R = \frac{\hat{u}_{LCR}}{Z_o} \qquad \text{(F-15)}$$

Thus, $\hat{i}_R$ is independent of R. This is perfect for driving a negative load resistance such as a fluorescent lamp.

Amplitude of voltage across the capacitor C:

$$\hat{u}_R = Q.\hat{u}_{LCR} \qquad \text{(F-16)}$$

Thus, when the lamp is off, Q is high and therefore the peak output voltage is high; striking the lamp.

Ouput power P_o:

$$P_o = \tfrac{1}{2}.\hat{u}_{LCR}^{\,2}.\frac{R}{Z_o^{\,2}} \qquad \text{(F-17)}$$

Waveform:

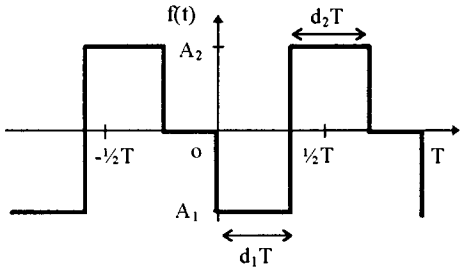

Figure G-1 Waveform for fourier analysis

Definitions:

$$f(t)=\frac{a_o}{2}+\sum_{n=1}^{\infty}\left[a_n.\cos\left(\frac{2\pi.n.t}{T}\right)+b_n.\sin\left(\frac{2\pi.n.t}{T}\right)\right]=\frac{a_o}{2}+\sum_{n=1}^{\infty}A_n.\cos\left(\frac{2\pi.n.t}{T}+\varphi_n\right) \quad \text{(G-1)}$$

$$a_n=\frac{2}{T}\int_{-T_2}^{T_2}f(t).\cos\left(\frac{2\pi.n.t}{T}\right).dt \qquad b_n=\frac{2}{T}\int_{-T_2}^{T_2}f(t).\sin\left(\frac{2\pi.n.t}{T}\right).dt \quad \text{(G-2)}$$

$$A_n^{\,2}=a_n^{\,2}+b_n^{\,2} \qquad \varphi_n=-\arctan\left(\frac{b_n}{a_n}\right) \quad \text{(G-3)}$$

dc-component:

$$a_o=-2A_1.d_1+2A_2.d_2 \quad \text{(G-4)}$$

coefficient a_n:

$$a_n=\frac{2}{T}\int_{0}^{d_1.T}-A_1.\cos\left(\frac{2\pi.n.t}{T}\right).dt+\frac{2}{T}\int_{d_1.T}^{(d_1+d_2).T}A_2.\cos\left(\frac{2\pi.n.t}{T}\right).dt$$

$$a_n=\frac{-A_1}{n\pi}.\sin(2\pi.n.d_1)-\frac{A_2}{n\pi}.\left[-\sin(2\pi.n.(d_1+d_2))+\sin(2\pi.n.d_1)\right] \quad \text{(G-5)}$$

coefficient b_n:

$$b_n=\frac{2}{T}\int_{0}^{d_1.T}-A_1.\sin\left(\frac{2\pi.n.t}{T}\right).dt+\frac{2}{T}\int_{d_1.T}^{(d_1+d_2).T}A_2.\sin\left(\frac{2\pi.n.t}{T}\right).dt$$

$$b_n=\frac{A_1}{n\pi}.\left[\cos(2\pi.n.d_1)-1\right]-\frac{A_2}{n\pi}.\left[\cos(2\pi.n.(d_1+d_2))-\cos(2\pi.n.d_1)\right] \quad \text{(G-6)}$$