MASTER

Fully balanced LNA 58 - 64 GHz with 3.8 dB NF, 10 dB Gt and constant group delay in CMOS nm

Janssen, E.J.G.

Award date:
2008

Fully Balanced LNA 58 - 64 GHz with 3.8 dB NF, 10 dB G_t and constant group delay in CMOS 65 nm

Master Thesis

Erwin Janssen

Mixed-signal Microelectronics,
Eindhoven University of Technology

Contents

Acknowledgment

The author would like to thank Reza Mahmoudi of Eindhoven University for his helpful support and suggestions during the project and the co-workers of NXP Semiconductors for enabling the tape-out and for their helpful support during the layout phase, especially Edwin van der Heijden, Anton de Graauw and Dennis Jeurissen. The author would like to thank Philips research for enabling the tape-out of the transformer and Pooyan Sakian of Eindhoven University for his help during the noise figure measurement.

Chapter 1

Introduction

The increasing demand for higher data rate in RF communication links requires the use of more bandwidth. Around 60 GHz, 6 GHz of unlicensed bandwidth is available which enables data rates of several gigabits per second. To implement such systems, modern CMOS technology is interesting because of its promise to use digital signal processing combined with RF front end electronics. This enables the integration of a full system on chip. In this report the design, simulation and layout of a 60 GHz differential LNA using 65 nm CMOS is discussed. Because the f_t of the used CMOS device is approximately twice the operating frequency, many problems arise.

One of those difficulties is the existence of many parasitic effects. To model these, an EM-simulator has been used in combination with RC-extraction techniques performed on the layout. During the design one of the goals is to minimize the effect of these parasitics.

In order to achieve the required 6 GHz bandwidth (≈ 10 %), feedback is applied. At these high frequencies the use of coupled structures such as transformers to apply this feedback become interesting because of their low noise contribution, low DC-voltage drop and because their dimensions are not such a big issue anymore. Therefore a search was done for designs that make use of transformers for feedback purposes. Several designs have been compared in order to decide which topology to choose. In order to accurately model the behavior of a transformer on chip, an EM simulator was used. To verify the behavior predicted by the EM-simulator a transformer was designed, simulated, taped out and measured.

Another problem is the low supply voltage of 1.2 Volt. Because of this, it is not possible to stack many transistors. This results in solutions that make use of as little stacked devices as possible.

1.1 LNA

The LNA is the first system block after the signal source, the antenna. It's main task is to retrieve and amplify the signal from the source with the least possible deterioration. Main design criteria are noise figure, gain, and linearity (IP_3).

1.1.1 Noise

In all electronic systems there are random fluctuations in the current and voltage caused by the random movement of electrons. This phenomenon is called noise. The noise adds to the

signal causing a deterioration of the signal quality. If the signal strength is weak compared to this noise it is hard to retrieve the information carried by the signal. So to have a reliable communication link, a certain ratio is required between the signal and noise power. This is called the signal to noise ratio, SNR. It sets a lower bound to the minimum signal power level possible at the input source of the receiver while still having a reliable communication.

The noise factor F, is defined as the ratio between the SNR at the output and the input of an electronic system.

$$F_{LNA} = \frac{SNR_{out}}{SNR_{in}} = \frac{P_{in}N_{out}}{G_a P_{in} N_{in}} = \frac{N_{out}}{G_a N_{in}} = \frac{G_a(N_{in} + N_{LNA})}{G_a N_{in}} = 1 + \frac{N_{LNA}}{N_{in}}$$

P_{in}	=	Input Signal Power
N_{in}	=	Input Noise Power
N_{out}	=	Output Noise Power
N_{LNA}	=	Noise Power added in LNA
G_a	=	Available Gain

To obtain a sensitive receiver the noise factor should be kept as small as possible, so N_{LNA} should be kept low. The LNA is the first system block of the receiver after the antenna and maybe some filtering. Due to this the noise factor of the LNA, F_{LNA}, adds directly to the noise factor of the total system.

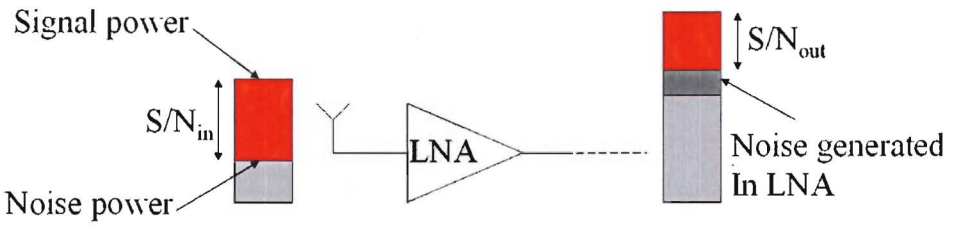


Figure 1.1: The LNA is the first system block in a receiver and its noise adds directly to the noise figure.

This can be verified by Friis' formula.

$$F_{total} = F_{LNA} + \frac{F_2 - 1}{G_{a,LNA}} + \frac{F_3 - 1}{G_{a,2} G_{a,LNA}} + \ldots$$

As can be seen by this formula, the contribution of the noise factor of the second system block, F_2, will be divided by the available gain of the LNA, $G_{a,LNA}$. So for a LNA it is desirable to have a low noise factor and a high gain. Often the noise figure is given instead of the noise factor. It is defined as follows:

$$NF = 10 \log_{10} \frac{SNR_{out}}{SNR_{in}} = 10 \log_{10} F$$

1.1.2 Gain

Because the noise factor of the subsequent stages can be divided by the available gain (G_a) of the LNA, it is preferable to have high G_a. The definition of available gain is as follows:

$$G_a = \frac{\text{Power available from the network}}{\text{Power available from the source}} = \frac{1-|\Gamma_s|^2}{|1-s_{11}\Gamma_s|^2}|s_{21}|^2\frac{1}{1-|\Gamma_{out}|^2}$$

$$\begin{aligned} \Gamma_s &= \text{Source reflection Coefficient} \\ \Gamma_{out} &= \text{Output reflection Coefficient} \\ s_{xx} &= \text{Scattering Parameters} \end{aligned}$$

"Power available" is defined as the maximum power that can be delivered to the next stage, so the power transfer when Z_{out} of the first stage, source or network, is equal to Z_{in}^* of the next stage, so network or load. This gain is independent of source or load impedance, and it's eventual mismatch. Maximizing G_a means maximizing the s_{21}-parameter as can be seen by the formula. This is the forward transmission coefficient with the output properly terminated, so $Z_{out} = Z_{load}^*$.

This might lead to the wrong reasoning the source and load mismatch does not affect the overall noise factor. These mismatches do affect the noise factor because a mismatch leads to less power in both signal and noise, but the noise generated in the next stage still has the same power. This will eventually result in a lower SNR, so a higher F. Therefore it is important to have $Z_{in} = Z_{src}^*$ and $Z_{out} = Z_{load}^*$.

On the other hand, the noise factor is also dependent of Z_{src}. In designing an LNA it is therefore interesting to have $Z_{src} = Z_{src,opt,NF} = Z_{in}^*$. If this cannot be accomplished a tradeoff will result, to minimize the overall noise factor.

1.1.3 IP3

Apart from the lower bound of the signal strength there is also an upper bound. This is given by the linearity of the system. If the signal strength increases the non-linear behavior of the active devices become more dominant. This gives rise to intermodulation products.

$$V_{out}(t) = \alpha V_{in}(t) + \beta V_{in}^2(t) + \gamma V_{in}^3(t) + \ldots$$

Where the third order intermodulation product has the same (extrapolated) strength as the output signal, IP_3 is defined. This is shown in figure 1.2.

The IP_3 can be referred to the input or the output power. It then is defined respectively as IIP_3 and OIP_3. The 1 dB_c point indicated in the figure shows where the gain has dropped by 1 dB. This point is approximately 10 dB lower than the IIP_3 point (input referred).

When cascading different subsystems the first subsystem (LNA) is not dominant in the total IIP_3 of the system. The total IIP_3 is defined as follows (this formula is not valid or all cascaded systems but it gives a nice indication):

$$\frac{1}{IIP_{3,total}} = \frac{1}{IIP_{3,1}} + \frac{G_{a,1}}{IIP_{3,2}} + \frac{G_{a,1}G_{a,2}}{IIP_{3,3}} + \ldots$$

In the region between the noise floor and where the third order intermodulation product is equal to the noise floor, the system can handle the signal in a reliable fashion. This range is called the spurious free dynamic range, $SFDR$. It is defined as follows:

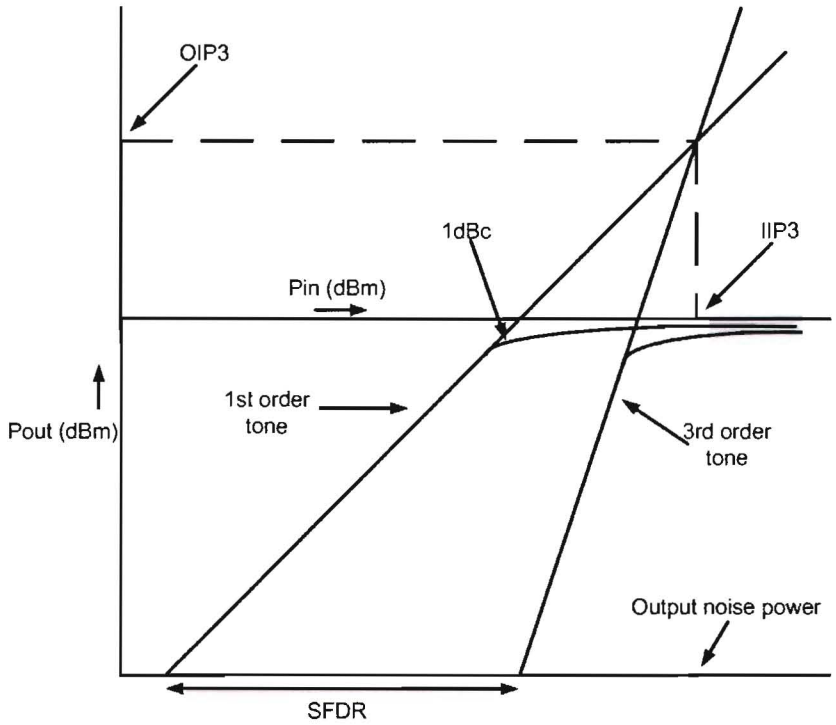


Figure 1.2: IIP_3, $OIP3$, $1dB_c$, noise floor and spurious free dynamic range.

$$SFDR(dB) = \frac{2}{3}\Big(OIP_3(dBm) - \text{Output noise power}(dBm)\Big)$$

Concluding the previous sections the main objectives of the LNA are a low noise figure, high gain and high IP_3. To find an optimum, the spacing between the noise figure and gain has to be maximized. Afterwards the IP_3 will determined at this optimum. Then an optimal IP_3 will be located in the range for optimal noise figure - gain spacing.

1.2 Specifications

The topology of this LNA has to be differential to improve local oscillator leakage resistance and linearity (see appendix section A.2). Another reason to choose for the differential topology is it's immunity to the impact of the bond-wire gain reduction. Furthermore the differential amplifier can be directly connected to a differential antenna. To implement the LNA the TSMC 65 nm CMOS technology has to be used. Main specifications for this design are gain (s_{21}) of at least 15 dB, noise figure of 5 dB at maximum and IIP_3 of at least 0 dBm.

The frequency range the LNA has to cover is 58 to 64 GHz. This is 9.8 % of the center frequency at 61 GHz. A certain gain flatness over this frequency band has to be accomplished. Design goal is 0.5 dB over the entire bandwidth. To achieve this, feedback can be used. Different feedback topologies have to be investigated considering alternatives such as inductive or transmission line feedback coupling.

To remove common mode signals there has to be a common mode rejection. To include this a CMRR design goal of at least 10 dB has to be met. A summary of all design specifications is given below:

Gain (s_{21})	> 15 dB
Noise figure	< 5 dB
IIP_3	> 0 dBm
Gain flatness in 6 GHz Bandwidth	< 0.5 dB
CMRR	> 10 dB

Chapter 2

Topologies

In a literature search different topologies were investigated for the LNA. Starting point for this search is the use of feedback. Applying feedback is possible over some different active topologies such as common gate and common source. To make a decision how to implement the active part, first a comparison will be given for these two topologies. After this comparison several topologies will be investigated for the 60 GHz LNA. Eventually a decision will be made between the different topologies. During the analysis the following variables will be used to model the behavior of the MOST:

R_g = Gate resistance
R_{ds} = Drain source resistance
C_{gs} = Capacitance between gate and source
C_{gd} = Capacitance between gate and drain
g_m = Transconductance

2.1 Common source

With the common source topology the source is connected to AC ground and the gate is connected to the signal source. The schematic is shown in figure 2.1 and the small signal model is given in figure 2.2.

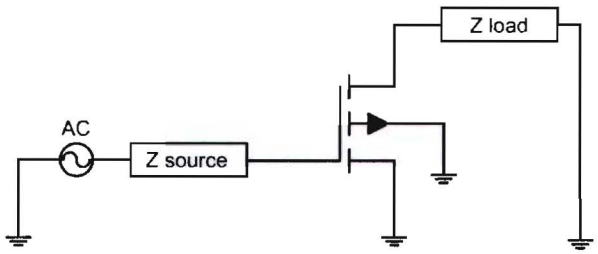


Figure 2.1: Common source

$$V_s = V_b = 0V$$

For this topology the ABCD-parameters, input impedance and noise figure will be determined to make a good comparison. The ABCD-parameters of the common source topology

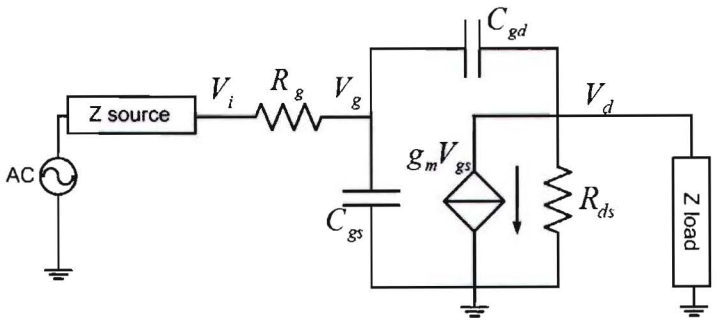


Figure 2.2: Small signal equivalent circuit common source topology

are given below:

$$\mathbf{ABCD} = \begin{bmatrix} \frac{sR_gC_{gd}(sC_{gs}+g_m)+\frac{R_g}{R_{ds}}(sC_{gd}+sC_{gs})+\frac{1}{R_{ds}}+sC_{gd}}{sC_{gd}-g_m} & \frac{1+sR_g(C_{gs}+C_{gd})}{sC_{gd}-g_m} \\ \frac{s^2C_{gd}C_{gs}+sC_{gd}(g_m+\frac{1}{R_{ds}})+\frac{sC_{gs}}{R_{ds}}}{sC_{gd}-g_m} & \frac{s(C_{gs}+C_{gd})}{sC_{gd}-g_m} \end{bmatrix}$$

In general R_g is very small. This results in an A-parameter (unloaded voltage gain) as follows:

$$A \approx \frac{\frac{1}{R_{ds}} + sC_{gd}}{sC_{gd} - g_m}$$

Because $g_m > \frac{1}{R_{ds}}$, the common source topology has both voltage, and current gain bigger than one possible (up to a certain frequency). Using the ABCD-parameters the noise performance of the common source can be investigated. To calculate the noise factor, the noise generated in the transistor channel and the noise due to the gate resistance have been taken into account, see figure 2.3.

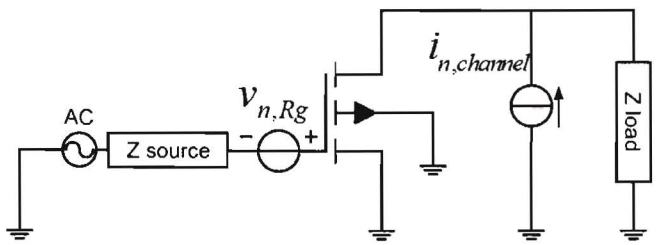


Figure 2.3: Channel noise in MOST and noise due to R_g

$$\overline{i^2_{n,channel}} = 4kT\gamma g_m$$

$$\overline{v^2_{n,R_g}} = 4kTR_g$$

$$\begin{aligned} k &= \text{Boltzmann constant} \approx 1.38 \cdot 10^{-23} \\ T &= \text{Absolute temperature} = 300K \\ \gamma &= \text{Technology dependent constant} \end{aligned}$$

To calculate the noise factor, the output noise has to be referred to the input. To do this, the output noise current will be multiplied by B and D to get an input noise voltage and current source respectively, as shown in figure 2.4.

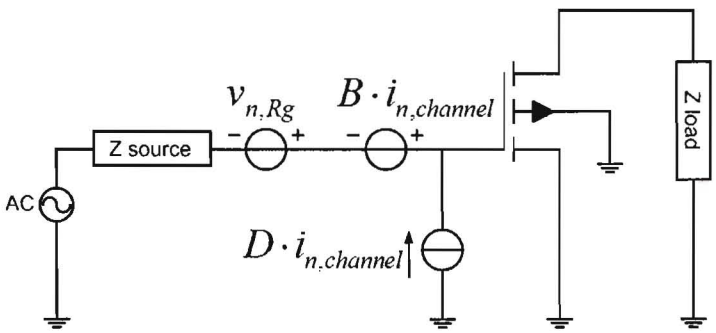


Figure 2.4: Noise sources referred to the input

$$v_{n,in} = B\sqrt{4kT\gamma g_m}$$

$$i_{n,in} = D\sqrt{4kT\gamma g_m}$$

The current source can be modeled as a voltage source. To do this the current source has to be multiplied by Z_{src}, the source impedance. Because of the correlation between the input current and voltage source they have to be added before squaring. Because of the small value of R_g, B can be approximated by the following formula:

$$B \approx \frac{1}{sC_{gd} - g_m}$$

$$\overline{v_{n,in}^2} = 4kTR_g + |B + Z_{src}D|^2 4kT\gamma g_m$$

$$\overline{v_{n,in}^2} \approx 4kTR_g + \left|\frac{1 + Z_{src}(sC_{gs} + sC_{gd})}{sC_{gd} - g_m}\right|^2 4kT\gamma g_m$$

$$F_{CS} \approx \frac{4kTR_{src} + 4kTR_g + \left|\frac{1+Z_{src}(sC_{gs}+sC_{gd})}{sC_{gd}-g_m}\right|^2 4kT\gamma g_m}{4kTR_{src}}$$

$$F_{CS} \approx 1 + \frac{R_g}{R_{src}} + \frac{\gamma g_m}{R_{src}}\left|\frac{1 + Z_{src}(sC_{gs} + sC_{gd})}{sC_{gd} - g_m}\right|^2$$

The equation of the noise factor consists a (double) zero and a pole, with the position of the pole as follows:

$$\omega_{pole} = \frac{g_m}{C_{gd}} > \frac{g_m}{C_{gs} + C_{gd}} = \omega_t$$

The position of the pole is beyond the ω_t of the device so this effect can be ignored. To minimize the contribution of the input referred current sources, Z_{src} is chosen to have a certain inductance. This inductance can be chosen to resonate with the capacitive effects present in the transistor and thereby lower the noise factor. The noise factor then looks as follows:

$$F_{CS} \approx 1 + \frac{R_g}{R_{src}} + \frac{\gamma g_m}{R_{src}} \left| \frac{1 + (R_{src} + sL_{src})(sC_{gs} + sC_{gd})}{g_m} \right|^2$$

To determine the optimal value for L_{src}, the derivative is taken and made equal to zero:

$$\frac{\partial F_{CS}}{\partial L_{src}} = 0$$

$$\rightarrow L_{src,opt,NF} = \frac{1}{\omega^2(C_{gs} + C_{gd})}$$

The noise factor then becomes:

$$F_{CS} \approx 1 + \frac{R_g}{R_{src}} + \frac{\gamma g_m}{R_{src}} \left| \frac{R_{src}(sC_{gs} + sC_{gd})}{g_m} \right|^2$$

$$F_{CS} \approx 1 + \frac{R_g}{R_{src}} + \frac{\gamma}{g_m} R_{src} \omega^2 (C_{gs} + C_{gd})^2$$

$$\rightarrow \omega_t = \frac{g_m}{C_{gs} + C_{gd}}$$

$$F_{CS} \approx 1 + \frac{R_g}{R_{src}} + \frac{\gamma \omega^2}{\omega_t^2} g_m R_{src}$$

As can be seen from this formula, maximizing ω_t lowers the noise factor. Therefore g_m must be maximized, at the cost of power consumption. Because $\omega/\omega_t \approx 1/2$ for 60 GHz in CMOS 65 nm (at optimal biasing), F_{CS} is approximately equal to:

$$F_{CS} \approx 1 + \frac{R_g}{R_{src}} + \frac{\gamma}{4} g_m R_{src}$$

To determine the optimal source resistance, again the derivative is taken (this time to R_{src}) and made equal to zero:

$$\frac{\partial F_{CS}}{\partial R_{src}} \approx \frac{\gamma g_m}{4} - \frac{R_g}{R_{src}^2} = 0$$

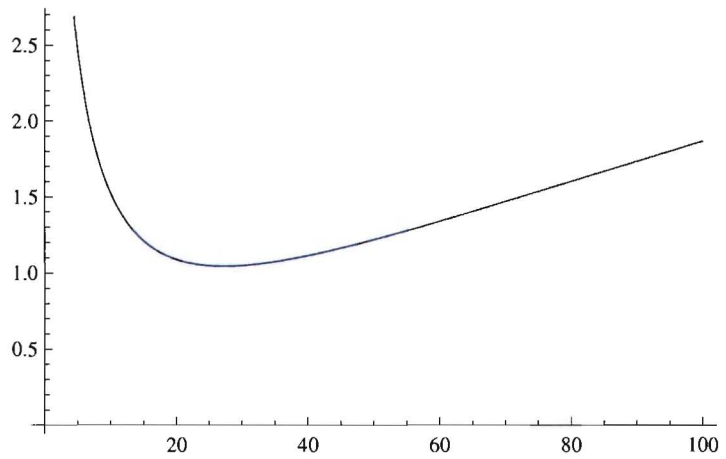


Figure 2.5: Calculated noise figure ($10\log F_{CS}$) as function of R_{src} with $L_{src} = L_{src,opt,NF}$ and $W_{MOST} = 30\mu$m.

$$\rightarrow R_{src,opt,NF} \approx 2\sqrt{\frac{R_g}{\gamma g_m}}$$

If R_g is small, $R_{src,opt,NF}$ also becomes small. The resulting F_{min} is equal to:

$$F_{CS,min} \approx 1 + \frac{R_g}{2\sqrt{\frac{R_g}{\gamma g_m}}} + \frac{\gamma g_m}{2}\sqrt{\frac{R_g}{\gamma g_m}}$$

$$\rightarrow F_{CS,min} \approx 1 + \sqrt{\gamma g_m R_g}$$

As can be seen the minimum noise factor becomes small for small R_g. Last feature to determine is the input impedance. This can be done by using the ABCD-parameters. To also take into account the effect of Z_{load}, the ABCD-parameters of the total system have to be calculated:

$$\mathbf{ABCD}_{Total} = \mathbf{ABCD}_{MOST} \cdot \mathbf{ABCD}_{Z_{load}}$$

$$\mathbf{ABCD}_{Z_{load}} = \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_{load}} & 1 \end{bmatrix}$$

$$Z_{in} = \left.\frac{V_o}{Vi}\right|_{I_o=0} = \frac{A_{Total}}{C_{Total}} = \frac{A_{MOST}A_{Z_{load}} + B_{MOST}C_{Z_{load}}}{C_{MOST}A_{Z_{load}} + D_{MOST}C_{Z_{load}}}$$

$$Z_{in} = \frac{A_{MOST} + \frac{B_{MOST}}{Z_{load}}}{C_{MOST} + \frac{D_{MOST}}{Z_{load}}}$$

$$\rightarrow Z_{in} = R_g + \frac{sC_{gd}(R_{ds}||Z_{load}) + 1}{s^2C_{gd}C_{gs}(R_{ds}||Z_{load}) + sC_{gd}(g_m(R_{ds}||Z_{load}) + 1) + sC_{gs}}$$

As can be seen by the formula the effect of C_{gd} on the input impedance is being multiplied by $g_m(R_{ds}||Z_{load})$. This is the Miller effect. This Miller effect also causes a path from the drain to the source, so from output to input. When the common source topology is used in a LNA, this signal path should be blocked to prevent instability. To further investigate the behavior due to this Miller capacitance, $g_m(R_{ds}||Z_{load})C_{gd}$ is now further called C_M.

$$Z_{in} = R_g + \frac{s\frac{C_m}{g_m} + 1}{s\frac{C_m}{g_m} \cdot sC_{gs} + sC_m + sC_{gd} + sC_{gs}}$$

If the effect of the Miller capacitance is big, the input impedance converges to:

$$Z_{in} = R_g + \frac{1}{sC_{gs} + g_m} =$$

$$\rightarrow R_{in} = R_g + \frac{g_m}{\omega^2C_{gs}^2 + g_m^2}$$

$$\rightarrow X_{in} = -\frac{\omega C_{gs}}{\omega^2C_{gs}^2 + g_m^2}$$

On the other hand, if the effect of the Miller capacitance is small, the input impedance converges to:

$$Z_{in} = R_g + \frac{1}{s(C_{gd} + C_{gs})}$$

$$\rightarrow R_{in} = R_g$$

$$\rightarrow X_{in} = -\frac{1}{\omega(C_{gd} + C_{gs})}$$

So the input impedance will be some where between these extremes, depending on Z_{load}. Under input matching conditions R_{in} has to be equal to R_{src}. Also X_{in} then has to be equal to $-X_{src}$. This means an inductance equal to (for high Miller effect):

$$L_{src,match} = \frac{\omega C_{gs}}{g_m^2 + \omega^2C_{gs}^2} \neq L_{src,opt,NF}$$

or (for small Miller effect):

$$L_{src,match} = \frac{1}{\omega^2(C_{gs} + C_{gd})} = L_{src,opt,NF}$$

Depending on Z_{load}. As can be seen the situation with little Miller effect has the same inductance for both power match and minimum noise factor.

2.2 Common gate

With the common gate topology the gate of the MOST is connected to AC ground and the source terminal is connected to the signal source. The schematic is drawn in figure 2.6. The equivalent small signal model is shown in figure 2.7. To be able to do easy calculations on the common gate topology the ABCD-parameters are calculated. R_g is neglected in the matrix shown because in general it has small influence on the behavior of the parameters but formulas become quite big.

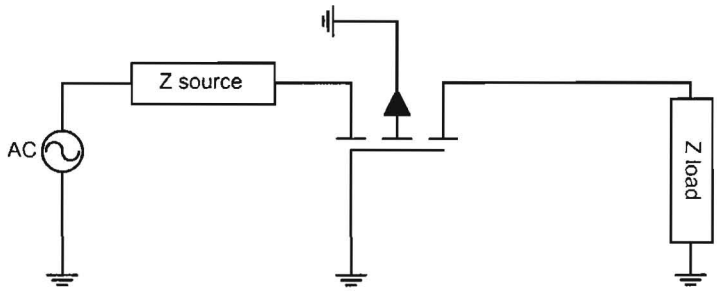


Figure 2.6: Common gate

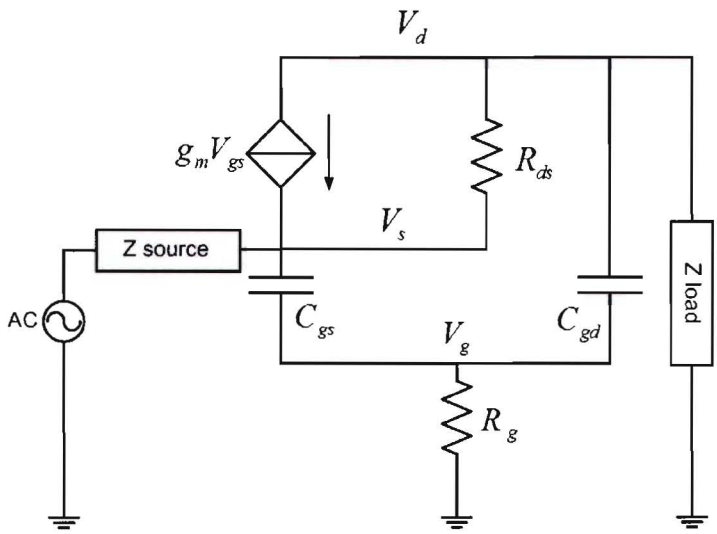


Figure 2.7: Small signal equivalent circuit common gate topology.

$$\mathbf{ABCD} \approx \begin{bmatrix} \frac{sR_{ds}C_{gd}+1}{g_m R_{ds}+1} & \frac{R_{ds}}{g_m R_{ds}+1} \\ \frac{s^2 R_{ds}C_{gs}C_{gd}+sC_{gd}(g_m R_{ds}+1)+sC_{gs}}{g_m R_{ds}+1} & \frac{sR_{ds}C_{gs}+g_m R_{ds}+1}{g_m R_{ds}+1} \end{bmatrix}$$

The value of D is defined as $\frac{I_i}{I_o}\Big|_{V_o=0}$. Because this value is always ≥ 1, the current gain of the common gate topology is ≤ 1. This means there is no current gain but only voltage gain possible in the common gate topology.

To calculate the noise factor, the noise generated in the transistor channel has to be taken into account as well as the noise generated in R_g.

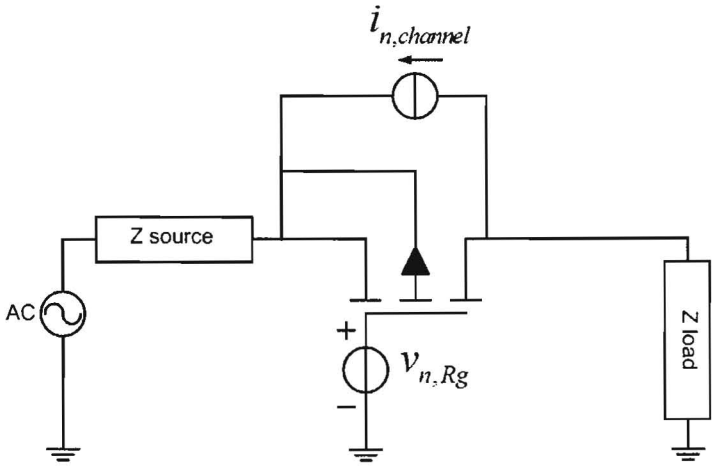


Figure 2.8: Noise source present in the transistor channel.

$$\overline{i^2_{n,channel}} = 4kT\gamma g_m$$

The channel noise has to be referred to the input. To do this, it is moved to the output and input. To get the output source to the input it has to be multiplied by B and D to get a voltage and current source respectively, see figure 2.9.

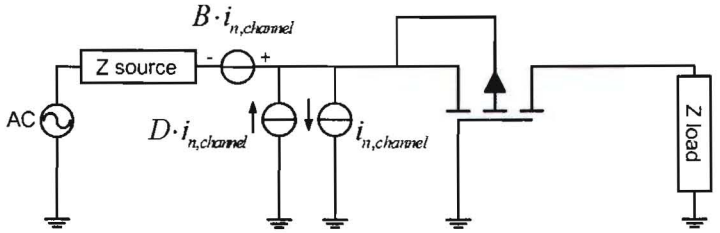


Figure 2.9: Referring the channel noise to the input.

$$\overline{v^2_{n,in,channel}} = \left|B + (D-1)Z_{src}\right|^2 4kT\gamma g_m$$

$$\overline{v^2_{n,in,channel}} = \left|\frac{R_{ds}}{g_m R_{ds}+1} + \left(\frac{sR_{ds}C_{gs} + g_m R_{ds} + 1}{g_m R_{ds}+1} - 1\right)Z_{src}\right|^2 4kT\gamma g_m$$

$$\overline{v^2_{n,in,channel}} = \left|\frac{R_{ds} + sR_{ds}Z_{src}C_{gs}}{g_m R_{ds}+1}\right|^2 4kT\gamma g_m$$

Also the noise generated by R_g has to be referred to the input. Therefore the noise voltage source can be shifted to the in and output. Then the noise source at the output can be brought

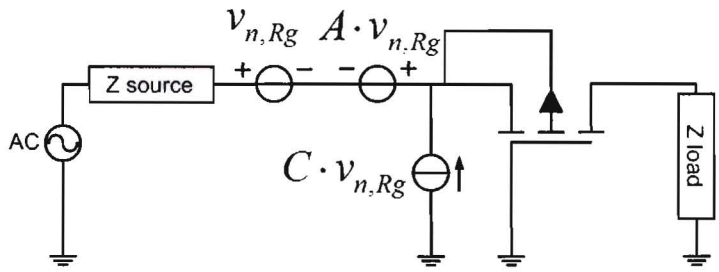


Figure 2.10: Referring the noise due to R_g to the input.

back to the input by multiplying it with A and C. The resulting input referred noise due to R_g is shown in figure 2.10.

By doing this the following formula for the noise contribution due to the gate resistance results:

$$\overline{v_{n,in,R_g}^2} = \left|1 - A - C \cdot Z_{src}\right|^2 4kTR_g$$

$$\overline{v_{n,in,R_g}^2} \approx 4kTR_g \left| \frac{g_m R_{ds} - sR_{ds}C_{gd}(sC_{gs}Z_{src} + g_m Z_{src} + 1) - Z_{src}s(C_{gs} + C_{gd})}{g_m R_{ds} + 1} \right|^2$$

The resulting noise factor is equal to the following expression:

$$F_{CG} \approx$$

$$\frac{4kTR_{src} + 4kTR_g \left| \frac{g_m R_{ds} - sR_{ds}C_{gd}(sC_{gs}Z_{src} + g_m Z_{src} + 1) - Z_{src}s(C_{gs} + C_{gd})}{g_m R_{ds} + 1} \right|^2 + 4kT\gamma g_m \left| \frac{R_{ds} + sR_{ds}Z_{src}C_{gs}}{g_m R_{ds} + 1} \right|^2}{4kTR_{src}}$$

$$F_{CG} \approx$$

$$1 + \frac{R_g}{R_{src}} \left| \frac{g_m R_{ds} - sR_{ds}C_{gd}(sC_{gs}Z_{src} + g_m Z_{src} + 1) - Z_{src}s(C_{gs} + C_{gd})}{g_m R_{ds} + 1} \right|^2 + \frac{\gamma g_m}{R_{src}} \left| \frac{R_{ds} + sR_{ds}Z_{src}C_{gs}}{g_m R_{ds} + 1} \right|^2$$

An approximation is made by neglecting R_{ds}:

$$\lim_{R_{ds} \to \infty} F_{CG} \approx$$

$$1 + \frac{R_g}{R_{src}} \left| \frac{g_m - sC_{gd}(sC_{gs}Z_{src} + g_m Z_{src} + 1)}{g_m} \right|^2 + \frac{\gamma g_m}{R_{src}} \left| \frac{1 + sZ_{src}C_{gs}}{g_m} \right|^2$$

If a source impedance is formed with a resistive and an inductive part, again the inductance can be chosen to resonate with the capacitive effects present in the transistor. Thereby it is possible to lower the noise factor. To find the optimal value of L_{src}, the derivative of the noise factor is taken and made equal to zero:

$$\frac{\partial F_{CG}}{\partial L_{src}} = 0$$

$$L_{src,opt,NF} \approx \frac{R_g C_{gd}(\omega^2 C_{gd} C_{gs} - g_m^2) + C_{gs}\gamma g_m}{\omega^2 R_g C_{gd}^2(\omega^2 C_{gs}^2 + g_m^2) + \omega^2 C_{gs}^2 \gamma g_m}$$

If R_g is very small, the optimal source inductance converges to:

$$L_{src,opt,NF} \approx \frac{1}{\omega^2 C_{gs}}$$

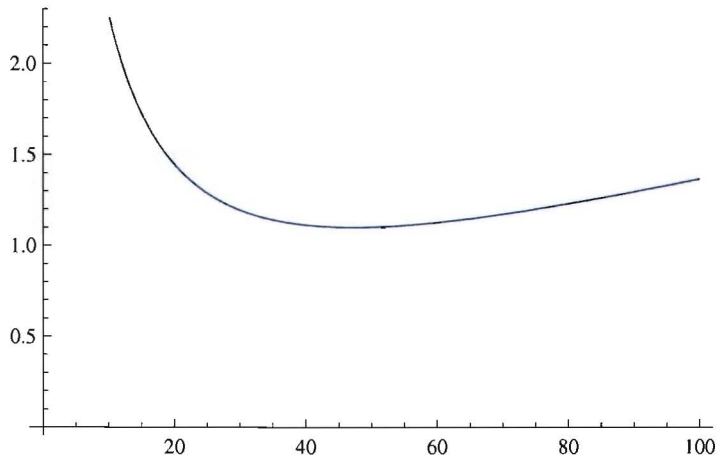


Figure 2.11: Calculated noise figure ($10\log F_{CG}$) as function of R_{src} with $L_{src} = L_{src,opt,NF}$ and $W_{MOST} = 30\mu$m.

To find the optimal value for R_{src}, also the derivative is taken and made equal to zero:

$$\frac{\partial F_{CG}}{\partial R_{src}} = 0$$

$$R_{src,opt,NF} \approx g_m \omega (C_{gd} + C_{gs}) \frac{\sqrt{\omega^2 R_g^2 C_{gd}^2 + R_g \gamma g_m}}{\omega^2 R_g C_{gd}^2(\omega^2 C_{gs}^2 + g_m^2) + \omega^2 C_{gs}^2 \gamma g_m}$$

If R_g is again small, the optimal source resistance also becomes small. The resulting F_{min} is approximately equal to:

$$F_{CG,min} \approx 1 + 2\omega\sqrt{R_g} \frac{(\omega\sqrt{R_g})^2 C_{gd}^2 + \omega\sqrt{R_g} C_{gd}\sqrt{\omega^2 R_g C_{gd}^2 + \gamma g_m} + \gamma g_m}{\omega_t \sqrt{\omega^2 R_g C_{gd}^2 + \gamma g_m}}$$

$$F_{CG,min} \approx 1 + \omega R_g C_{gd} + 2\frac{\omega\sqrt{R_g}}{\omega_t} \cdot \frac{\omega^2 R_g C_{gd}^2 + \gamma g_m}{\sqrt{\omega^2 R_g C_{gd}^2 + \gamma g_m}}$$

$$F_{CG,min} \approx 1 + \omega R_g C_{gd} + 2\frac{\omega}{\omega_t} \cdot \sqrt{\omega^2 R_g^2 C_{gd}^2 + R_g \gamma g_m}$$

As can be seen from this formula, also for the common gate topology maximizing ω_t lowers the noise factor. Therefore g_m must be maximized, at the cost of power consumption. Because $\omega/\omega_t \approx 1/2$ for 60 GHz in CMOS 65 nm, $F_{CG,min}$ is approximately equal to:

$$F_{CG,min} \approx 1 + \omega R_g C_{gd} + \sqrt{\omega^2 R_g^2 C_{gd}^2 + R_g \gamma g_m}$$

If realistic values are filled in, the expression converges to:

$$\rightarrow F_{CG,min} \approx 1 + \sqrt{R_g \gamma g_m}$$

As can be seen the F_{min} becomes small for small R_g. Next feature is the input impedance. This is calculated in the following formula using the same approach as in the previous section:

$$Z_{in} = \frac{s^2 R_g C_{gd} C_{gs} + s C_{gd} g_m R_g + s C_{gd} + \frac{R_g s(C_{gs}+C_{gd})+1}{R_{ds}||Z_{load}}}{s^2 C_{gs} C_{gd} + s C_{gd} g_m + \frac{sC_{gd}}{R_{ds}} + \frac{sC_{gs}}{R_{ds}||Z_{load}} + \frac{s^2 R_g C_{gd} C_{gs} + s C_{gd} g_m R_g + g_m}{Z_{load}} + \frac{R_g s(C_{gs}+C_{gd})+1}{R_{ds} Z_{load}}}$$

If Z_{load} is assumed small, the input impedance reduces to:

$$Z_{in} \approx \frac{1 + s R_g (C_{gd} + C_{gs})}{s^2 R_g C_{gd} C_{gs} + s C_{gd} g_m R_g + \frac{R_g}{R_{ds}} s(C_{gd} + C_{gs}) + s C_{gs} + g_m + \frac{1}{R_{ds}}}$$

$$Z_{in} \approx \frac{1 + j g_m R_g \frac{\omega}{\omega_t}}{-\omega^2 R_g C_{gd} C_{gs} + j\omega(C_{gd} g_m R_g + \frac{g_m R_g}{\omega_t R_{ds}} + C_{gs}) + g_m + \frac{1}{R_{ds}}}$$

Because R_g is usually small and $g_m R_g \frac{\omega}{\omega_t} \approx \frac{1}{2} g_m R_g < 1$, Z_{in} can be approximated by:

$$Z_{in} \approx \frac{1}{g_m + \frac{1}{R_{ds}} + j\omega C_{gs}}$$

$$Z_{in} \approx \frac{g_m + \frac{1}{R_{ds}} - j\omega C_{gs}}{(g_m + \frac{1}{R_{ds}})^2 + \omega^2 C_{gs}^2}$$

$$\rightarrow R_{in} \approx \frac{g_m + \frac{1}{R_{ds}}}{(g_m + \frac{1}{R_{ds}})^2 + \omega^2 C_{gs}^2} \approx \frac{g_m}{g_m^2 + \omega^2 C_{gs}^2}$$

$$\rightarrow X_{in} \approx \frac{-\omega C_{gs}}{(g_m + \frac{1}{R_{ds}})^2 + \omega^2 C_{gs}^2} \approx \frac{-\omega C_{gs}}{g_m^2 + \omega^2 C_{gs}^2}$$

If Z_{load} is assumed big, the input impedance neglecting R_g becomes:

$$Z_{in} \approx \frac{R_{ds} + \frac{1}{sC_{gd}}}{g_m R_{ds} + 1 + s R_{ds} C_{gs} + \frac{C_{gs}}{C_{gd}}}$$

This input impedance converges to the same situation with small Z_{load} if R_{ds} is big, which is usually the case. Therefore the input impedance of the common gate topology has little

dependence on Z_{load}. This input impedance is an important feature of the common gate topology. It gives the designer the freedom to choose an input impedance by setting the biasing of the transistor. By doing this, matching between the LNA and the antenna can be provided.

Under input matching conditions R_{in} has to be equal to R_{src}. Also X_{in} then has to be equal to $-X_{src}$. This means an inductance equal to:

$$L_{src,match} = \frac{\omega C_{gs}}{g_m^2 + \omega^2 C_{gs}^2} \neq L_{src,NF}$$

As can be seen there is a tradeoff between the optimal inductance concerning noise performance and input match.

2.3 Discussion CS - CG

In the following table the common source topology is compared with the common gate topology concerning gain and noise performance based on the previous sections:

Topology	Voltage gain	Current gain	Noise performance	Input impedance
CS	+	+	+	depends on Miller effect
CG	+	-	+	+

As can be seen from this table, both common source and common gate topology have nice properties. The common source stage has both high current and voltage gain. It thereby makes sure the noise generated in the following stage can not flow directly to the input. So in a total system, the noise performance will be better. The noise performance of the topologies themselves are approximately the same for both stages. F_{min} for both topologies are approximately equal and is given below:

$$F_{CS,min} \approx F_{CG,min} \approx 1 + \sqrt{R_g \gamma g_m}$$

If the Miller effect is big in the common source topology, it's input impedance is approximately equal to the input impedance of the common gate. If the Miller effect on the other hand is small, the input impedance becomes mainly capacitive, which is less attractive for matching. Also the Miller effect present in the common source topology creates a path from output to input, causing a possibility for instability. It should therefore be blocked somehow. A choice was made to look at both a common source and common gate topology using feedback to see the effect of the feedback elements on the performance, and make a decision then.

2.4 G_m-boosted common gate

The first topology discussed as a candidate for the 60 GHz LNA is the g_m-boosted common gate LNA. For the active part this topology makes use of a common gate stage. As seen in the previous part this topology has as an advantage that there is an easy way of providing a wideband input match. After applying this, the biasing of the transistor is set to a certain value resulting in a certain noise figure. When using g_m-boosting, a lower noise figure can be

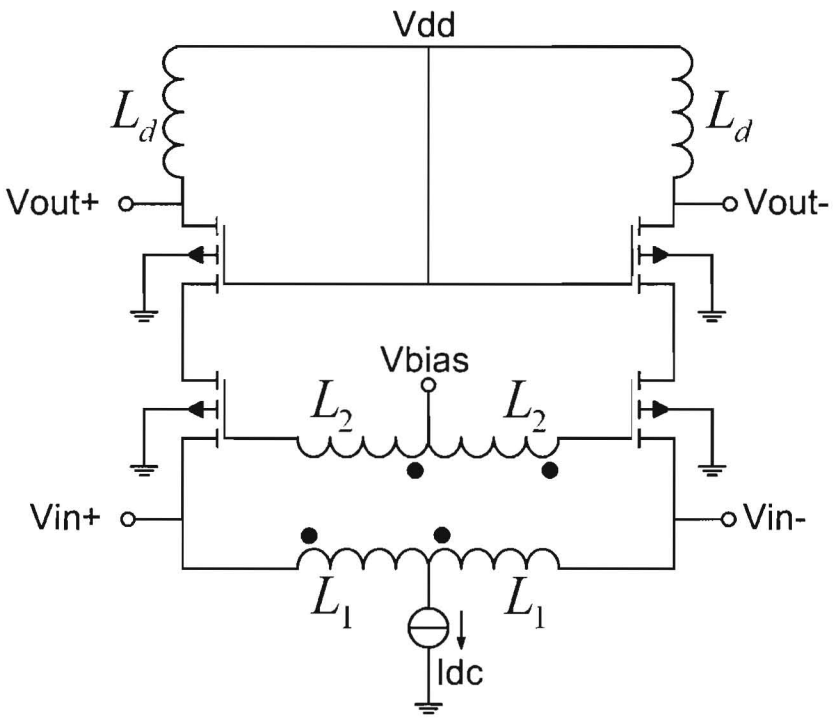


Figure 2.12: G_m-boosted common gate LNA. The left combination of L_1 and L_2 forms a transformer as well as the right combination.

achieved with the common gate stage while still maintaining the input match criterion [1]. The schematic of the g_m-boosted CG LNA is shown in figure 2.12.

As can be seen in the schematic the input stage is followed by another common gate stage, so a cascode. This is done to increase the output impedance and isolate the output from the input. Because the common gate topology only gives voltage gain, the output impedance must be high to have enough gain. The biasing of the transistors is done at the inductors. Inductors are interesting because they have no DC voltage drop and add little noise.

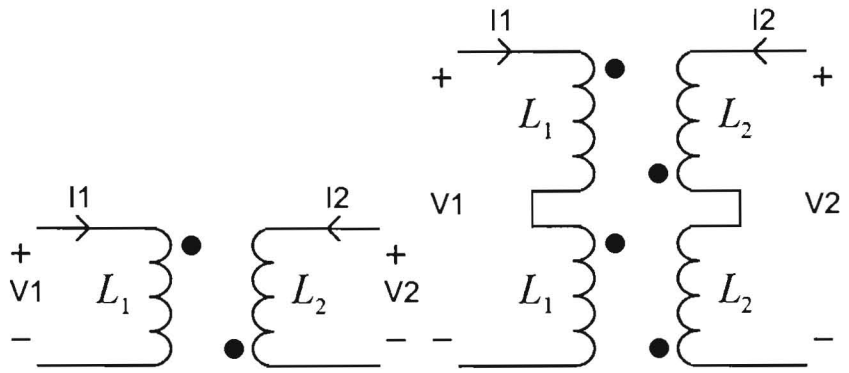
To be able to use the half circuit concept, the transformer needs to be cut in two parts. To see what effect this has on the inductance and the coupling, the Z-parameters are used. In figures 2.13(a) and 2.13(b) a single and a cascoded transformer are shown.

The Z-parameters of the single transformer look as follows:

$$\mathbf{Z}_{single} = \begin{bmatrix} sL_1 & sM \\ sM & sL_2 \end{bmatrix}$$

With M being the mutual inductance defined as $k\sqrt{L_1 L_2}$ (k = the coupling factor). To obtain the Z-parameters for the cascoded transformers, the Z-matrix of the single transformer must be multiplied by two (because of the series connection and the fact that both transformers are identical):

$$\mathbf{Z}_{casc} = \begin{bmatrix} s \cdot 2L_1 & s \cdot 2M \\ s \cdot 2M & s \cdot 2L_2 \end{bmatrix} = \begin{bmatrix} sL_{1,casc} & sM_{casc} \\ sM_{casc} & sL_{2,casc} \end{bmatrix}$$



(a) Single transformer. (b) Two transformers cascoded.

Figure 2.13: Single and cascoded transformer

This means all inductances double. For the coupling factor this means:

$$M_{casc} = 2M_{single} = 2k\sqrt{L_1 L_2} = k\sqrt{2L_1 \cdot 2L_2} = k\sqrt{L_{1,casc} L_{2,casc}}$$

So the coupling factor stays the same, and the inductances halve when using the half circuit concept.

2.4.1 Input impedance

To calculate the input impedance the small signal circuit shown in figure 2.14 is used (R_g has been neglected because of it's little influence).

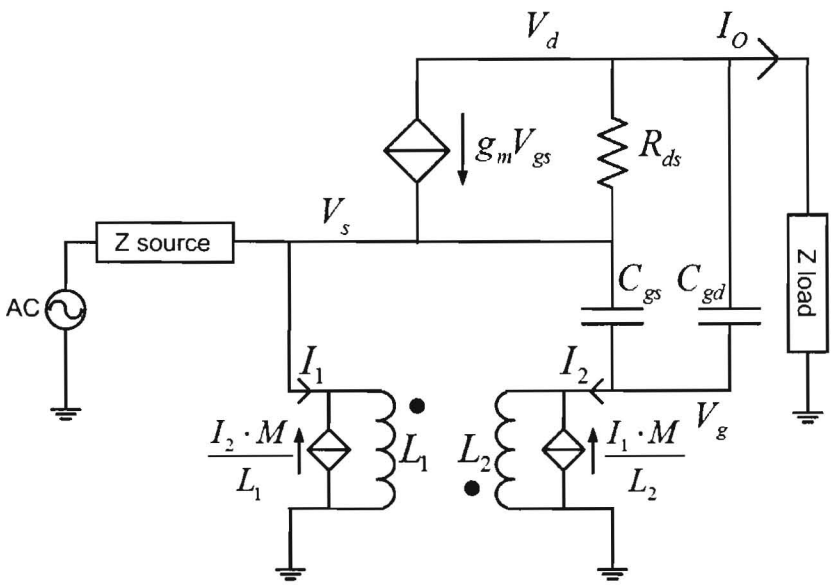


Figure 2.14: Small signal equivalent circuit of the g_m-boosted common gate LNA

An ideal cascode is assumed, so $Z_{load} = 0$. The Y-parameters of the network look as follows:

$$\mathbf{Y} = \begin{bmatrix} sC_{gs} + g_m + \frac{1}{R_{ds}} + \frac{1}{s(1-k^2)L_1} & -sC_{gs} - g_m - \frac{k}{s(1-k^2)\sqrt{L_1 L_2}} & -\frac{1}{R_{ds}} \\ -sC_{gs} - \frac{k}{s(1-k^2)\sqrt{L_1 L_2}} & s(C_{gs} + C_{gd}) + \frac{1}{s(1-k^2)L_2} & -sC_{gd} \\ -g_m - \frac{1}{Rds} & g_m - sC_{gd} & \frac{1}{Z_{load}} + sC_{gd} + \frac{1}{R_{ds}} \end{bmatrix}$$

$$\mathbf{Y} \cdot \begin{bmatrix} V_s \\ V_g \\ V_d \end{bmatrix} = \begin{bmatrix} I_{in} \\ 0 \\ 0 \end{bmatrix}$$

If C_{gd} and R_{ds} are neglected because of their little effect on Z_{in} the input impedance looks as follows, with $n = \sqrt{\frac{L_2}{L_1}}$:

$$Z_{in} \approx \frac{s^2(1-k^2)L_2 C_{gs} + 1}{sC_{gs}(n^2 - 2kn + 1) + g_m(1 - kn) + \frac{1}{sL_1}}$$

Because the $(1 - k^2)$ term in the numerator becomes small when $k \to -1$, the input impedance can be approximated by the following formula for high coupling:

$$Z_{in} \approx \frac{1}{sC_{gs}(1+n)^2 + g_m(1+n) + \frac{1}{sL_1}}$$

If L_1, C_{gs} and n are chosen in such a way that they become resonant at the operating frequency (which is the same frequency for minimum noise, see appendix), the input impedance at resonance reduces to:

$$Z_{in} \approx \frac{1}{g_m(1+n)}$$

So for the differential situation the input impedance is:

$$Z_{in_{diff}} = 2 \cdot Z_{in_{SE}} \approx \frac{2}{g_m(1+n)}$$

As can be seen from this formula, the real part of the input impedance of the g_m-boosted CG LNA is approximately lowered by a factor of $\frac{1}{1+n}$ in comparison of the conventional CG stage. This is due to the amplification between the source and gate.

2.4.2 Noise factor

In the appendix the noise factor is calculated. The resulting noise factor looks as follows:

$$F_{g_m-boosted} \approx 1 + \frac{2R_g}{(1+n)^2 R_{src}} \left| 1 + \frac{Z_{src}}{2sL_1} \right|^2 + \frac{2\gamma}{g_m(1+n)^2 R_{src}}$$

As can be seen the noise factor can be lowered by increasing g_m, n and R_{src}, and lowering R_g. If X_{src} is chosen capacitive, the noise due to R_g can be made very small and neglected, resulting in:

$$F_{g_m-boosted} \approx 1 + \frac{2\gamma}{g_m(1+n)^2 R_{src}}$$

If now a power match is created between the antenna and the LNA, $\frac{g_m(1+n)}{2} R_{src} = 1$ (for high coupling), the noise figure for the g_m-boosted CG LNA looks as follows:

$$F_{g_m-boosted} \approx 1 + \frac{\gamma}{1+n}$$

As can be seen from this formula, for high transformer coupling the noise factor is lowered by $(1+n)$. This quantity can be identified as the voltage gain between the source and gate due to the transformer. This formula suggests the noise figure can be made arbitrarily low by increasing n. This is not true because there are also other noise sources present in the LNA such as the induced gate noise [1]. Also the presence of the cascode transistor will deteriorate the noise figure. The noise figure will therefore be higher in reality and n will have a certain optimum. Simulations will be used to determine the exact value of the noise factor and optimal n, using more realistic models for the used components taking various non-idealities into account.

2.4.3 Loop gain

For the lowering of the noise factor, a negative coupling is needed. To avoid instability it is needed to avoid positive feedback. Therefore the loop gain $A\beta$ of the g_m-boosted CG LNA has to be calculated. To determine the open loop gain, the loop has to be broken somewhere. In figure 2.15 it is shown where the loop is opened. The transistor model is replaced by a combination of a nullator and a norator.

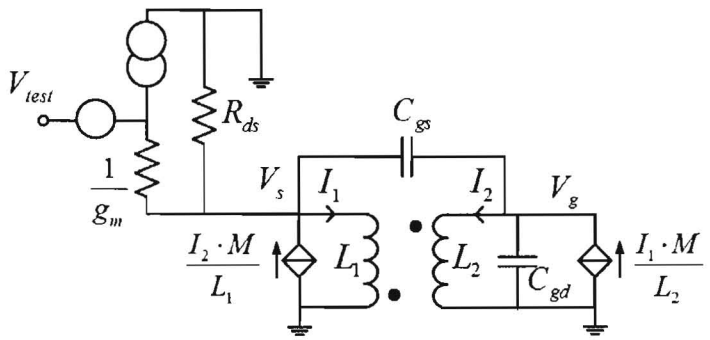


Figure 2.15: Opening the loop to calculate the open loop gain

The resulting loop gain with C_{gd} and R_{ds} ignored looks as follows:

$$A\beta = \frac{g_m(s^2(1-k^2)L_2C_{gs} + kn)}{g_m(s^2(1-k^2)L_2C_{gs} + 1) + sC_{gs}(n^2 - 2kn + 1) + \frac{1}{sL_1}}$$

At the operating frequency L_1, C_{gs}, n and k are again chosen to resonate, so the loop gain looks as follows:

$$A\beta = \frac{(kn - \omega^2(1-k^2)L_2C_{gs})}{(1-\omega^2(1-k^2)L_2C_{gs})}$$

With $|k| \rightarrow 1$, the expression converges to kn. This means the loop gain is negative when the coupling is negative. This holds as long as the denominator does not become negative as well. So to have negative feedback the following equations must hold:

$$k < 0$$

And

$$\omega^2(1-k^2)L_2C_{gs} < 1$$

This is in agreement with the constraint for lowering the noise figure, namely a negative coupling.

2.4.4 Voltage gain

The output signal of the g_m-boosted CG LNA has been shorted to ground so far, because of the use of a cascode and to ease calculations. To determine the voltage gain there has to be some kind of load, which will be modeled by Z_{load}. To model the behavior of the cascode, C_{gd} and R_{ds} are disconnected from the drain and connected to ground. The voltage gain is given by the following formula (assuming an ideal cascode):

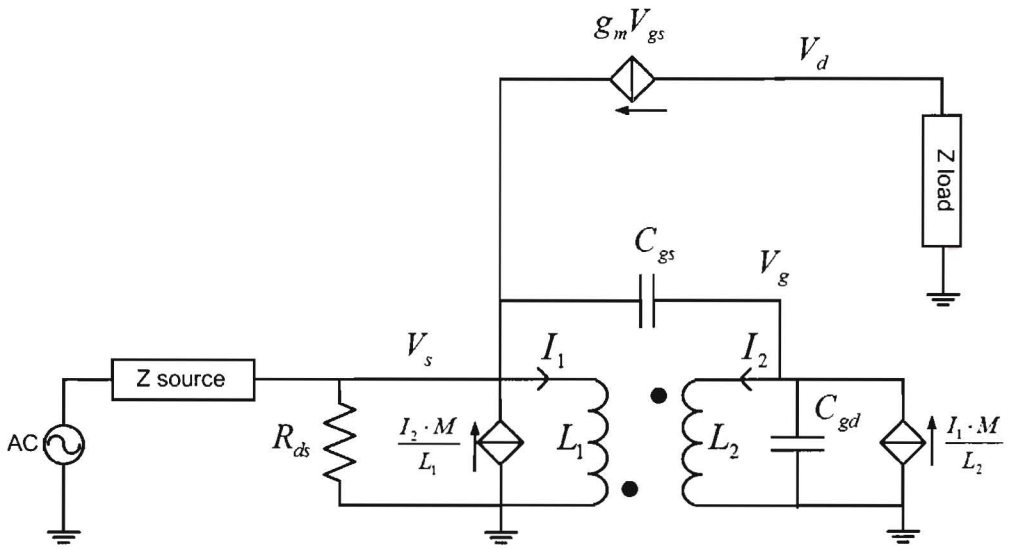


Figure 2.16: Small signal equivalent circuit to determine the voltage gain

$$\frac{V_{out}}{V_{in}} = \frac{g_m Z_{load}(s^2(1-k^2)L_2C_{gd} + 1 - kn)}{s^2(1-k^2)L_2(C_{gd}+C_{gs}) + 1}$$

As can be seen from this formula, if $k \rightarrow -1$, the transfer gain increases. So also for high gain, $k \rightarrow -1$ is preferred. The resulting voltage gain is then:

$$\frac{V_{out}}{V_{in}} = g_m(1+n)Z_{load}$$

To maximize the voltage gain, the denominator can to be made equal to zero, so:

$$\omega^2(1-k^2)L_2(C_{gd}+C_{gs}) = 1$$

The resulting value of L_1 should then be:

$$L_1 = \frac{L_2}{n^2} = \frac{1}{\omega^2 n^2(1-k^2)(C_{gd}+C_{gs})}$$

This formula is not in accordance with the optimal value of L_1 for noise performance and input impedance. So there has to be made some kind of compromise.

The transfer function also consists a double zero resulting in a notch in the transfer at:

$$\omega_{zero} = \frac{1-kn}{(1-k^2)L_2C_{gd}}$$

Operation around this frequency should be prevented.

2.5 Voltage-voltage transformer feedback LNA

The second topology discussed as a candidate for the implementation of the 60 GHz LNA is the voltage-voltage transformer feedback LNA (see figure 2.17). This topology uses a CS MOST as an active part. Big advantage of a common source MOST is the combination of both high voltage gain and current gain. Disadvantage is the signal path from output to input through C_{gd}, the Miller capacitance. This increases the possibility of instability. Measures have to be taken against this reverse signal path. By using the voltage-voltage transformer feedback LNA topology this is possible without the use of the conventional cascode. This increases voltage headroom for the MOST and lowers the noise factor of the total LNA. In most calculations R_g is neglected because of its little influence on most parameters. Only for the noise performance and the input impedance it has been taken into account.

2.5.1 Output isolation

Because the active part of the voltage voltage feedback topology is a common source MOST, there has to be some kind of output isolation to minimize the signal path from output to input. The output signal at the drain (V_{out}) is connected via C_{gd} to V_g, as is shown in figure 2.18. Because of the transformer being connected between the drain and source of the transistor the signal at the drain is being copied to the source. The signal at the source is the inverse of the signal at the drain because of the negative coupling. The signal at the source is connected to the gate through C_{gs}. Because of the opposite effects of the signals through C_{gs} and C_{gd} the output signal can be canceled at V_g [3]. The transfer function $\frac{V_g}{V_{out}}$ of the circuit is calculated using the half circuit concept and looks as follows:

$$\frac{V_g}{V_{out}} =$$

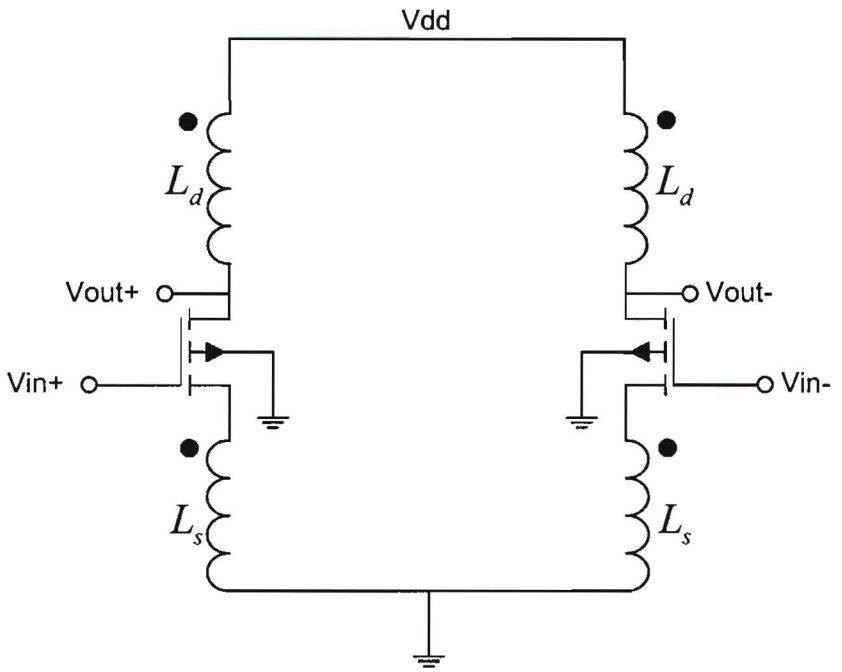


Figure 2.17: Voltage voltage transformer feedback LNA. The left combination of L_s and L_d forms a transformer as well as the right combination

$$\frac{s^2(1-k^2)L_sC_{gs}R_{ds} + s(1-k^2)L_s(g_mR_{ds}+1+\frac{C_{gs}}{C_{gd}}) + R_{ds}(1+\frac{kC_{gs}}{nC_{gd}})}{s^2(1-k^2)L_sC_{gs}R_{ds} + s(1-k^2)L_s(g_mR_{ds}+1+\frac{C_{gs}}{C_{gd}}) + R_{ds}(1+\frac{C_{gs}}{C_{gd}})}$$

To see the low frequency behavior the limit for $s \rightarrow 0$ is taken:

$$\lim_{s\to 0} \frac{V_g}{V_{out}} = \frac{R_{ds}(1+\frac{kC_{gs}}{nC_{gd}})}{R_{ds}(1+\frac{C_{gs}}{C_{gd}})} = \frac{nC_{gd}+kC_{gs}}{nC_{gd}+nC_{gs}}$$

$$\frac{V_g}{V_{out}} = 0 \quad \text{if} \quad nC_{gd} + kC_{gs} = 0$$

$$\rightarrow \frac{n}{k} = -\frac{C_{gs}}{C_{gd}}$$

To see the output isolation versus frequency, values for a 30 μm MOSFET are taken in combination with a transformer with $n = 2$, $k = -0.667$ and $L_s = 30pH$. The values for the transformer are chosen such that $-\frac{n}{k} = \frac{C_{gs}}{C_{gd}}$. For technologies such as CMOS 65nm this ratio is approximately equal to 3. The magnitude of V_g versus V_{out} is shown in figure 2.19.

Figure 2.19 shows good output isolation for frequencies below 1-10 GHz. For frequencies from 10-200 GHz the output isolations becomes worse. Above 200 GHz there is no isolation anymore under the given circumstances, but because the used MOST model is not valid anymore for these high frequencies, these results cannot be trusted.

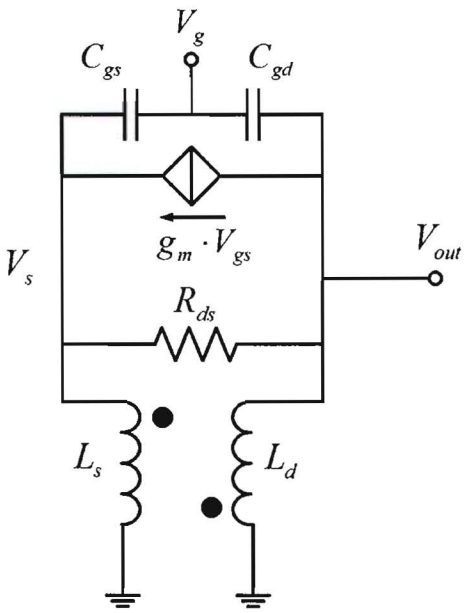


Figure 2.18: Lumped element model of the V-V transformer feedback topology (single ended).

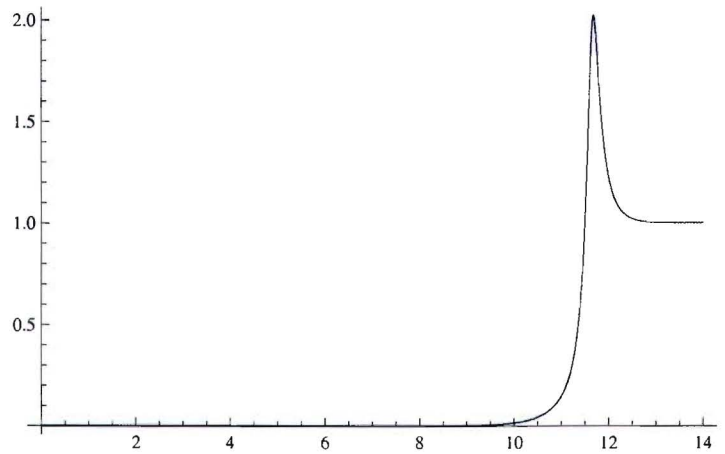


Figure 2.19: Magnitude response $\frac{V_g}{V_{out}}$ with $\frac{n}{k} \approx -\frac{C_{gs}}{C_{gd}} = -3$. The horizontal axis shows the frequency on a logarithmic scale.

2.5.2 Voltage gain

To calculate the voltage gain, also the half circuit concept is used, because it is equal to the voltage gain of the differential implementation. To determine the voltage gain, the limit is taken for $R_{ds} \to \infty$. Simulations show small deviation due to this, but calculations become much easier.

$$\lim_{R_{ds}\to\infty} \frac{V_{out}}{V_{in}} = \frac{s^3(1-k^2)L_dC_{gs}C_{gd} + s^2(1-k^2)g_mL_dC_{gd} + sn^2C_{gd} + knsC_{gs} - g_mn(n-k)}{s^3(1-k^2)L_dC_{gd}C_{gs} + s^2(1-k^2)g_mL_dC_{gd} + sn^2C_{gd} + sC_{gs} + g_m(1-kn) + \frac{1}{sL_s}}$$

If $-\frac{n}{k}$ is chosen to be $\frac{C_{gs}}{C_{gd}}$ to provide output isolation, the $sn^2C_{gd} + knsC_{gs}$ term in the numerator cancels:

$$\lim_{R_{ds}\to\infty} \left.\frac{V_{out}}{V_{in}}\right|_{-\frac{n}{k}=\frac{C_{gs}}{C_{gd}}} =$$

$$\frac{s^3(1-k^2)L_dC_{gs}C_{gd} + s^2(1-k^2)g_mL_dC_{gd} - g_mn(n-k)}{s^3(1-k^2)L_dC_{gd}C_{gs} + s^2(1-k^2)L_dC_{gd}g_m + sn^2C_{gd} + sC_{gs} + g_m(1-kn) + \frac{1}{sL_s}}$$

For high coupling, the higher order terms disappear:

$$\lim_{k\to-1}\lim_{R_{ds}\to\infty} \left.\frac{V_{out}}{V_{in}}\right|_{-\frac{n}{k}=\frac{C_{gs}}{C_{gd}}} = \frac{-g_mn(1+n)}{sn^2C_{gd} + sC_{gs} + g_m(1+n) + \frac{1}{sL_s}}$$

If we choose the value of L_s to resonate with C_{gs} and C_{gd}, the gain is maximal. To do so, the value of L_s should be:

$$L_s = \frac{1}{\omega^2(n^2C_{gd} + C_{gs})}$$

The voltage gain at resonance then reduces to:

$$\lim_{k\to-1}\lim_{R_{ds}\to\infty} \left.\frac{V_{out}}{V_{in}}\right|_{-\frac{n}{k}=\frac{C_{gs}}{C_{gd}}} = \frac{-g_mn(1+n)}{g_m(1+n)} = -n$$

So to have high gain, n should be high. Combining this with the criterion for output isolation, n and k should both be high. In practical situations the highest possible coupling on chip is approximately 0.7 - 0.8. This results in a transformer windings ratio of 2.1 - 2.4. These are also practical values for implementation on chip.

2.5.3 Input impedance

Also for the calculation of the input impedance, the half circuit concept is used. Afterwards, to get the input impedance of the differential structure the impedance has to be multiplied with 2. To determine the input impedance the schematic of figure 2.18 is used, R_{ds} has been neglected because it has little effect on the input impedance but it makes calculations more complex:

$$\mathbf{Y} = \begin{bmatrix} \frac{1}{R_g} & -\frac{1}{R_g} & 0 & 0 \\ 0 & s(C_{gs}+C_{gd}) & -sC_{gs} & -sC_{gd} \\ 0 & -(sC_{gs}+g_m) & \frac{1}{R_{ds}} + g_m + sC_{gs} + \frac{1}{s(1-k^2)L_s} & -\frac{1}{R_{ds}} + \frac{-k}{s(1-k^2)\sqrt{L_dL_s}} \\ 0 & -(sC_{gs}-g_m) & -\frac{1}{R_{ds}} - g_m - \frac{k}{s(1-k^2)\sqrt{L_dL_s}} & \frac{1}{R_{ds}} + sC_{gd} + \frac{1}{s(1-k^2)L_d} \end{bmatrix}$$

$$\mathbf{Y} \cdot \begin{bmatrix} V_i \\ V_g \\ V_s \\ V_{out} \end{bmatrix} = \begin{bmatrix} I_{in} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$\lim_{R_{ds}\to\infty} Z_{in} =$$

$$R_g + \frac{s^3(1-k^2)L_dC_{gd}C_{gs} + s^2(1-k^2)L_dC_{gd}g_m + s(n^2C_{gd}+C_{gs}) + g_m(1-kn) + \frac{1}{sL_s}}{sC_{gd}(n^2-2kn+1)(sC_{gs}+g_m) + \frac{C_{gd}+C_{gs}}{L_s}}$$

For high coupling, the high order terms in the denominator disappear:

$$\lim_{k\to-1}\lim_{R_{ds}\to\infty} Z_{in} = R_g + \frac{s(n^2C_{gd}+C_{gs}) + g_m(1+n) + \frac{1}{sL_s}}{sC_{gd}(1+n)^2(sC_{gs}+g_m) + \frac{C_{gd}+C_{gs}}{L_s}}$$

When L_s is chosen to have the value for maximal voltage gain, the input impedance at resonance reduces to:

$$\rightarrow L_s = \frac{1}{\omega^2(n^2C_{gd}+C_{gs})}$$

$$\lim_{k\to-1}\lim_{R_{ds}\to\infty} Z_{in} = R_g + \frac{g_m(1+n)}{\omega^2(nC_{gd}-C_{gs})^2 + j\omega C_{gd}g_m(1+n)^2}$$

If the output isolation ($-n/k = C_{gs}/C_{gd}$) is applied, the following equation for the input impedance is valid:

$$\lim_{k\to-1}\lim_{R_{ds}\to\infty} Z_{in} = R_g + \frac{1}{j\omega C_{gd}(1+n)}$$

For the differential situation the input impedance has to be multiplied by two:

$$\lim_{k\to-1}\lim_{R_{ds}\to\infty} Z_{in} = 2R_g + \frac{2}{j\omega C_{gd}(1+n)}$$

$$\lim_{k\to-1}\lim_{R_{ds}\to\infty} R_{in} = 2R_g$$

$$\lim_{k\to-1}\lim_{R_{ds}\to\infty} X_{in} = -\frac{2}{\omega C_{gd}(1+n)}$$

As can directly be seen from these formulas, the input resistance is equal to $2R_g$ for $n = \frac{C_{gs}}{C_{gd}}$ when the coupling is assumed ideal. Simulations show that for a coupling smaller then one, the input impedance can even become negative for $-\frac{n}{k} > \frac{C_{gs}}{C_{gd}}$. This should be prevented, because a negative input impedance can result in instability. As can be seen the input impedance of the V-V transformer feedback LNA converges to the input impedance of the common source topology with little Miller effect, because under the given circumstances $nC_{gd} = C_{gs}$.

2.5.4 Noise factor

In the appendix the noise factor is calculated. The resulting noise factor looks as follows (with $Z_{src} = R_{src} + sL_{src}$):

$$F_{diff} \approx 1+2\frac{R_g}{R_{src}}+2\frac{\gamma g_m}{R_{src}}\left|\left(\frac{s(C_{gs}+C_{gd})}{g_m^2(1+n)}-\frac{1}{g_m}\right)+\frac{R_{src}+sL_{src}}{2}\cdot\left(\frac{s^2(C_{gs}+C_{gd})^2}{g_m^2(1+n)}-\frac{s(C_{gs}+C_{gd})}{g_m}\right)\right|^2$$

If L_{src} is chosen to have the following inductance, the noise factor is minimized:

$$L_{src,opt,NF} = \frac{2}{\omega^2(C_{gs}+C_{gd})}$$

This source inductance is approximately equal to the inductance needed for input power matching. The optimal value for R_{src} is given in the following equation:

$$R_{src,opt,NF} \approx 4\sqrt{\frac{R_g}{\gamma g_m}} \neq R_{src,match} = 2R_g$$

If R_g becomes very small, $R_{src,opt,NF} \to 0$. The resulting noise factor with $Z_{src,opt,NF}$ is as follows:

$$F_{min} \approx \frac{2\sqrt{\frac{R_g\gamma}{g_m}}\omega(C_{gd}+C_{gs})\cdot\sqrt{\omega^2(C_{gd}+C_{gs})^2+g_m^2(1+n)^2}+g_m(1+n)}{g_m(1+n)}$$

If the dependence of the various transistor parameters are seen proportional of transistor width W, the resulting dependence of the noise factor as a function of transistor width can be observed:

$$F_{min} \propto \frac{\sqrt{\frac{1/W}{W}}W\cdot\sqrt{W^2+W^2}+W}{W} = \frac{W+W}{W} = 1$$

So the minimum noise factor is independent of the chosen transistor width. A further approximation of the minimum noise factor can be given in the form:

$$F_{min} \approx \frac{2\sqrt{\frac{R_g\gamma}{g_m}}\omega(C_{gd}+C_{gs})\cdot\sqrt{\omega^2+\omega_t^2(1+n)^2}+\omega_t(1+n)}{\omega_t(1+n)}$$

Because $\omega_t^2(1+n)^2 > \omega^2$, F_{min} is approximately equal to:

$$F_{min} \approx 1+2\sqrt{\frac{R_g\gamma}{g_m}}\cdot\omega(C_{gd}+C_{gs}) = 1+2\frac{\omega}{\omega_t}\cdot\sqrt{R_g\gamma g_m}$$

The resulting minimal noise factor at 60 GHz is approximately:

$$F_{min} \approx 1+\sqrt{R_g\gamma g_m}$$

As can be seen this F_{min} also converges to the behavior seen in the common source topology with little Miller effect. If R_g becomes very small again, the noise factor converges to unity. When a power match is created, the noise factor looks as follows:

$$F_{match} \approx 2 + \frac{\gamma R_g}{g_m}\omega^2(C_{gd}+C_{gs})^2\Big(1+\frac{\omega^2(C_{gd}+C_{gs})^2}{g_m^2(1+n)^2}\Big)$$

$$F_{match} \approx 2 + \frac{\gamma\omega^2 g_m R_g}{\omega_t^2}\Big(1+\frac{\omega^2}{\omega_t^2(1+n)^2}\Big)$$

$$F_{match} \approx 2 + \frac{\gamma g_m R_g}{4}\Big(1+\frac{1}{4(1+n)^2}\Big)$$

$$F_{match} \approx 2$$

So when a power match is applied, the noise factor is dominated by R_g and is equal to 2 at minimum, resulting a noise figure of at least 3dB.

2.6 Discussion g_m-boosted CG - V-V transformer feedback LNA

To make a decision which topology to choose, they will be compared using the calculations and simulations. A choice will be made based on noise and gain performance and the input impedance.

2.6.1 Noise performance

To compare the noise performance, the calculated noise factors are shown in the following equations. For the g_m-boosted CG LNA:

$$F_{g_m-boosted} \approx 1 + \frac{2R_g}{(1+n)^2 R_{src}}\Big|1+\frac{Z_{src}}{2sL_1}\Big|^2 + \frac{2\gamma}{g_m(1+n)^2R_{src}}$$

As already discussed the F_{min} of this topology is not equal to unity due to various other noise sources. When power matched and neglecting the noise due to R_g:

$$F_{g_m-boosted,matched} \approx 1 + \frac{\gamma}{1+n}$$

And for the V-V transformer feedback LNA:

$$F_{V-V\ feedback} \approx 1+2\frac{R_g}{R_{src}}+2\frac{\gamma g_m}{R_{src}}\Big|\Big(\frac{s(C_{gs}+C_{gd})}{g_m^2(1+n)}-\frac{1}{g_m}\Big)+\frac{R_{src}+sL_{src}}{2}\cdot\Big(\frac{s^2(C_{gs}+C_{gd})^2}{g_m^2(1+n)}-\frac{s(C_{gs}+C_{gd})}{g_m}\Big)\Big|^2$$

The $F_{V-V\ feedback,min}$ is equal to:

$$F_{V-V\ feedback,min} \approx 1 + \sqrt{R_g\gamma g_m}$$

The NF of this topology converges to the noise performance of the CS. If Z_{src} is chosen to achieve power match, the noise figure will be approximately 3 dB. This results in a compromise

between noise figure and power match, so gain. As can be seen the deterioration of the noise figure is dominated by R_g in the V-V FB LNA and by the channel noise for the g_m-boosted CG LNA when both are power matched.

When realistic values are used, there is only little difference between the NF of the two topologies. Only the V-V transformer feedback LNA makes use of a CS active part, so the noise generated in the next stage will have less influence on the overal noise figure due to the higher current gain with respect to the CG topology. Also the fact the g_m-boosted CG makes use of a cascode deteriorates the NF. So expected are better results for the V-V feedback topology, especially when a compromise between gain and noise performance is performed.

2.6.2 Gain

To compare the gain of both LNA topologies, the calculated voltage gain for both LNA's are given below (both for high coupling):

$$|A_{V,g_m-boosted}| = g_m(1+n)|Z_{load}|$$

$$|A_{V,V-V\,feedback}| = n$$

In general, $g_m Z_{load} > 1$, so:

$$g_m(1+n)|Z_{load}| > n$$

So based on calculations the g_m-boosted CG LNA gives best performance concerning voltage gain. On the other hand, the g_m-boosted CG LNA has smaller current gain compared to the V-V transformer feedback LNA. This is because of the use of a CG stage in the g_m-boosting CG LNA, and a CS stage in the V-V transformer feedback LNA. To achieve high (voltage) gain a cascode is used in the g_m-boosted CG topology resulting in a high output impedance, leading to a smaller difference in power gain compared to the difference in voltage gain.

2.6.3 Input impedance

To compare the input impedance, they are given for both topologies below (both for high coupling):

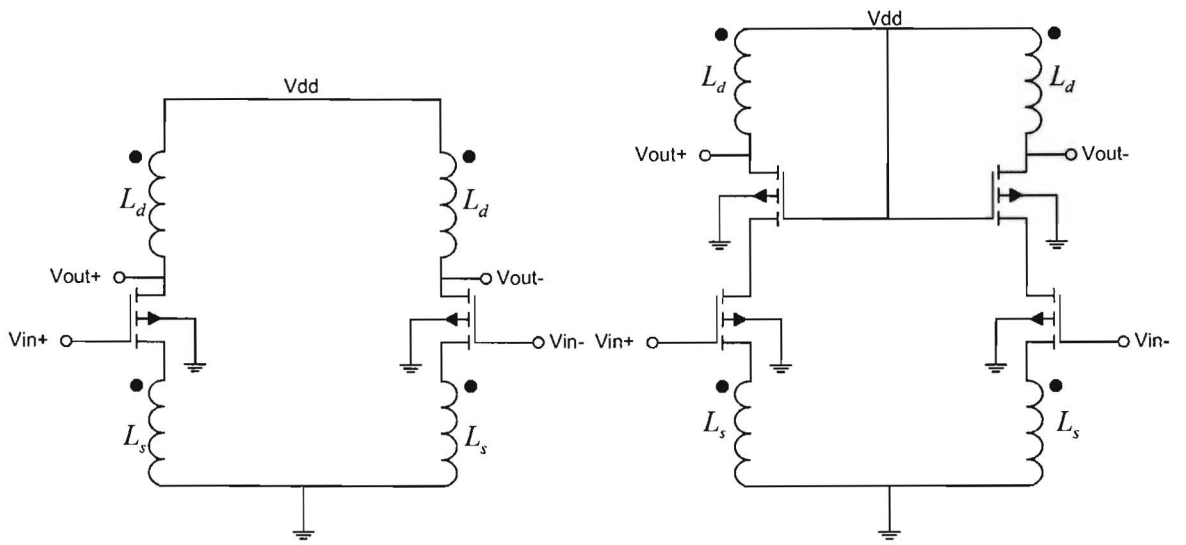
$$Z_{in,g_m-boosted} \approx \frac{2}{g_m(1+n)}$$

$$Z_{in,V-V\ feedback} = 2R_g + \frac{2}{j\omega C_{gd}(1+n)}$$

As can be seen the g_m-boosted CG LNA has a purely resistive input impedance, which is approximately equal to the Z_{in} of the CG topology divided by (1+n) (due to the feedback). The V-V transformer feedback LNA mainly has a capacitive input impedance. This can be tuned out with an inductor, but because of the high Q of this input impedance it must be designed to have low loss. As can be seen the input impedance of this topology converges to the Z_{in} of the CS topology with little Miller effect. Concerning the input impedance the g_m-boosted CG LNA has better properties compared to the V-V transformer feedback topology.

2.6.4 Simulations

Because the calculations are not as accurate as the models used in Cadence, simulations were performed for the different topologies. The voltage voltage transformer feedback topology was simulated in two different forms. These are shown in figures 2.20(a) and 2.20(b).



(a) V-V feedback LNA without cascode.

(b) V-V feedback LNA with cascode.

Figure 2.20: Both voltage-voltage transformer feedback topologies that were investigated during the simulations.

The right figure shows the voltage voltage transformer feedback LNA by using a cascode as active device. This way there is output isolation available due to the common gate after the common source stage, so the restriction on the ratio of n and k is not that strong. This assures a higher output impedance enabling higher gain. Because of the use of an extra active stage the noise performance is expected to be worse. Simulations were performed for each circuit in a short period and gave the following results:

	G_m-boosting	V-V feedback without cascode	V-V feedback with cascode
Gain	7.5 dB	6 dB	10 dB
NF	7 dB	3 dB	6.5 dB

These might not be the absolute maximum because there was only little time to do the simulations, but there is a certain trend visible. As expected the gain of the V-V transformer feedback topology with cascode is high compared to the other two topologies. The gain of the V-V transformer feedback LNA without cascode is worst, but it has a very low noise figure, also as expected. The g_m-boosted CG has the worst noise performance, but higher gain than the V-V transformer feedback LNA without cascode.

2.6.5 Decision

Based on the previous section decided was to continue with the V-V transformer feedback LNA without cascode. Biggest disadvantage of this topology is the high Q input impedance.

This will result in a difficult implementation of the matching network, which must be high Q as well to reduce losses. Decided is to make the design with an inductor to tune out the imaginary part of the input impedance and de-embed the network from this position. To achieve more gain two stages can be cascaded.

Chapter 3

MOST modeling CMOS 65 nm TSMC

The technology used to implement the 60 GHz LNA is the CMOS 65 nm process of TSMC. The transistor used was the standard V_t RF transistor. The parameters free to choose are the gate length L and width W and the folding factor. For a fixed $\frac{W}{L}$, different folding factors result in different f_t, f_{max} and noise performance. To model the behavior of the MOST transistor the model of figure 3.1 is used. It takes g_m, R_{ds}, and the capacitances C_{gs} and C_{gd} into account.

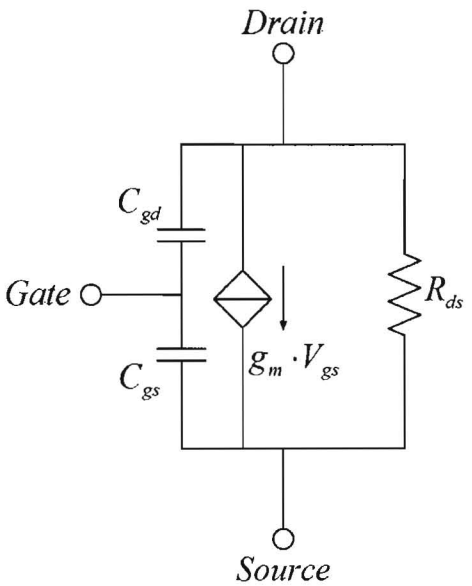


Figure 3.1: MOST model

To get high gain, f_t should be high. The definition of f_t is the frequency at which the current gain of the active device drops to unity, given in the following formula:

$$\frac{I_{out}}{I_{in}} = \frac{(g_m - sC_{gd})V_{gs}}{s(C_{gs} + C_{gd})V_{gs}}$$

$$\rightarrow f_t = \frac{(g_m - sC_{gd})}{2\pi(C_{gs} + C_{gd})} \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

To get maximal f_t, g_m should be high and $(C_{gs} + C_{gd})$ should be low. In the following equations g_m and $(C_{gs} + C_{gd})$ are written as functions of W and L. C_{ox} is the capacitance per unit area of gate oxide in F/m^2, μ_0 is the surface mobility of the channel in m^2/Vs and LD is the lateral diffusion component in m [4].

$$g_m = \mu_0 C_{ox} \frac{W}{L}(V_{gs} - V_t)$$

$$C_{gs} = C_{ox}(LD + \frac{2}{3}L_{eff})W_{eff} \approx C_{ox}\frac{2}{3}LW$$

Simulations show C_{gd} is approximately 0.4 times C_{gs}.

$$C_{gs} + C_{gd} \approx 1.4 C_{ox}\frac{2}{3}LW \approx C_{ox}LW$$

$$\rightarrow f_t \approx \frac{\mu_0 C_{ox}\frac{W}{L}(V_{gs} - V_t)}{2\pi C_{ox}LW} = \frac{\mu_0(V_{gs} - V_t)}{2\pi L^2}$$

This last formula is not valid anymore for sub-micron processes such as 65 nm because of "short channel" effects. Because of these effects g_m is smaller in reality. But the trend of the increasing f_t with decreasing L is still valid. So to get optimal performance, L should be as small as possible, in this technology this is 65 nm.

Next parameter to determine in the transistor is the fingerwidth. A long fingerwidth gives high gate resistance, because the material used for the gate is polysilicon which has a resistivity of 15 Ω /square. A small fingerwidth gives high parasitic capacitances between gate, source and drain, so degrades f_t. Simulations showed a fingerwidth of 1 μm gives best results concerning G_{max} and noise performance at 60 GHz.

To determine the optimal bias current I_d, a sweep was done in the simulator simulating G_{max} and NF_{min} as a function of V_{gs}. This plot is shown in figure 3.3 (W = 40 μm). The schematic used to measure the performance at 60 GHz of a single MOST is shown in figure 3.2. The used inductances and capacitances all have high values to produce an AC open and short respectively (only valid in simulation of course).

As can be seen in figure 3.3 the optimal bias voltage V_{gs} is 0.75 Volt (with V_{ds} = 1.2 Volt). The optimum is independent of the MOST width. With this gate voltage there is a DC drain current flowing through the MOST of approximately 8.5 mA. The used MOST width is 40 μm, so the optimal current density J_{opt} is as follows:

$$J_{opt} = \left.\frac{I_d}{W}\right|_{V_{gs}=0.75} = \frac{8.5mA}{40\mu m} \approx 0.21 mA/\mu m$$

To get values for the different model elements, simulations were done at this optimal bias point, so V_{gs} is 0.75 V, fingerwidth is 1 μm and gate length is 65 nm. The formulas used to determine the different model parameters are listed below.

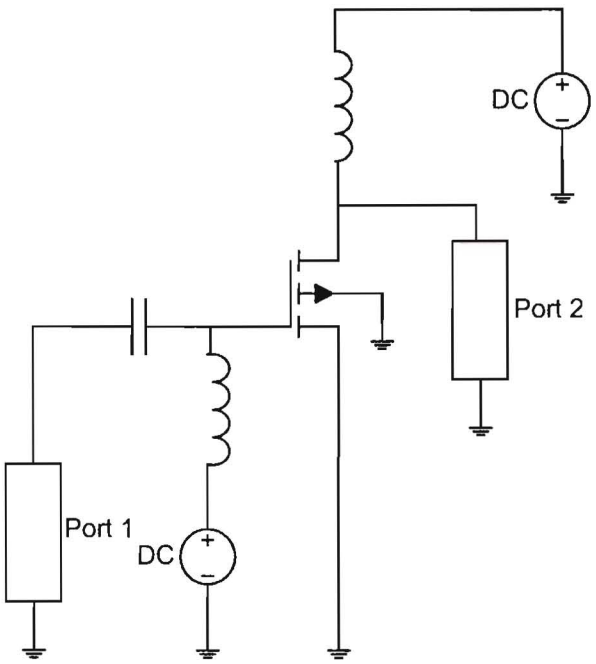


Figure 3.2: MOST modeling schematic

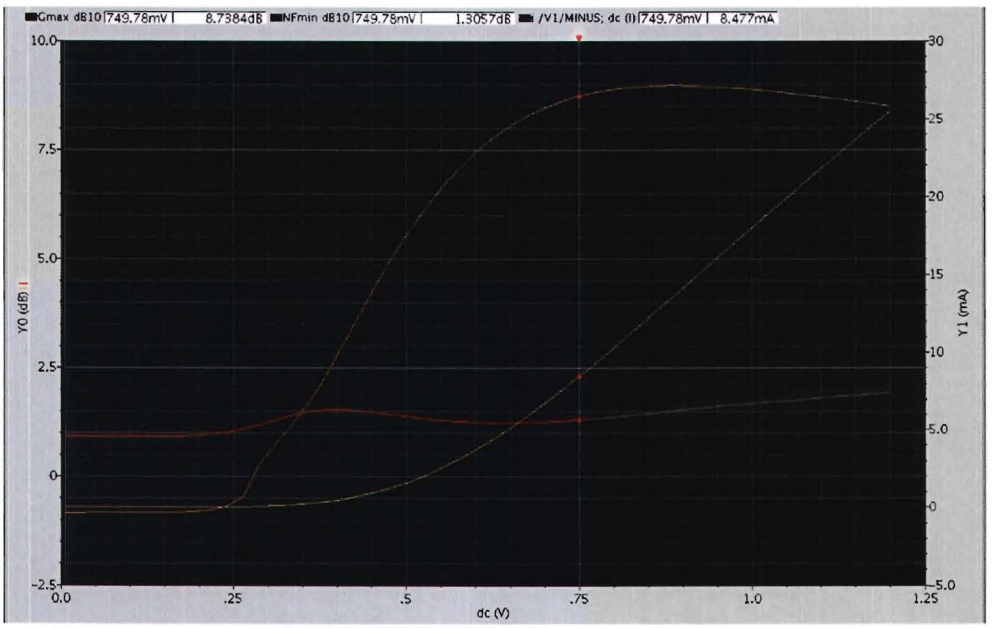


Figure 3.3: G_{max}, NF_{min} and I_d versus V_{gs}

$$C_{gs} = \frac{Im[Y_{11}] + Im[Y_{12}]}{\omega}$$

$$C_{gd} = \frac{-Im[Y_{12}]}{\omega}$$

$$g_m = Re[Y_{21}]$$

$$R_{ds} = \frac{1}{Re[Y_{22}] + Re[Y_{12}]}$$

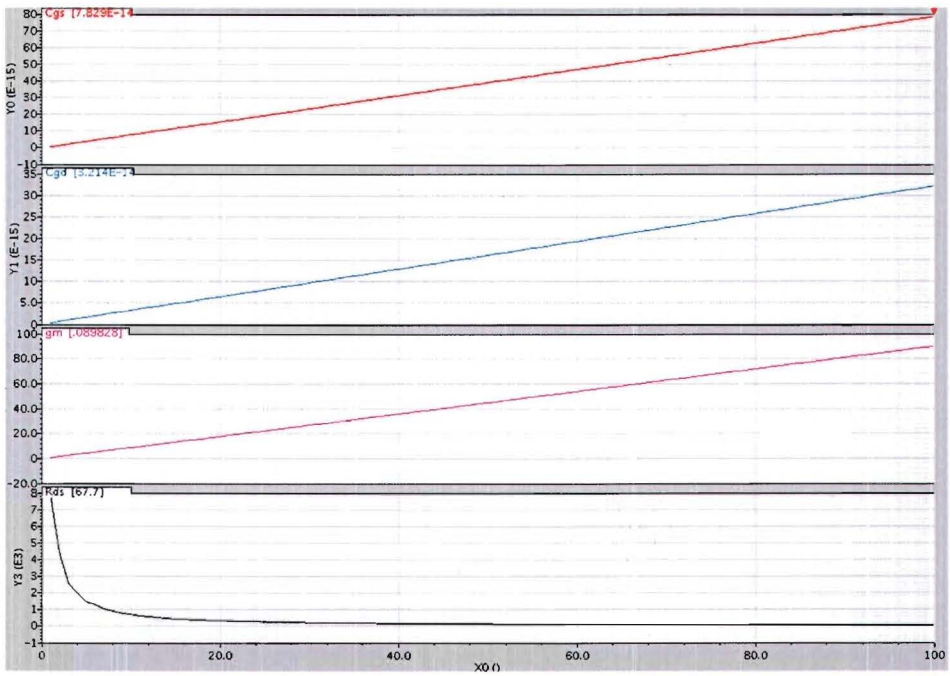


Figure 3.4: Simulation of different model parameters as a function of W at $V_{gs} = 0.75$ Volt and $V_{ds} = 1.2$ Volt.

As can be seen from figure 3.4 C_{gs}, C_{gd} and g_m are proportional to the transistor width. R_{ds} is proportional to the inverse of W. The values of the parameters behave approximately as follows:

$$\begin{aligned} C_{gs} &\approx 0.78 \text{ fF}/\mu m \\ C_{gd} &\approx 0.32 \text{ fF}/\mu m \\ g_m &\approx 0.90 \ mA/\mu m \\ R_{ds} &\approx 7000 \ \Omega\mu m \end{aligned}$$

These parameter values can be used to determine the value of f_t:

$$f_t \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})} = \frac{0.90 \cdot 10^{-3} \cdot W}{2\pi(0.78 \cdot 10^{-15} + 0.32 \cdot 10^{-15}) \cdot W} \approx 130 \text{ GHz}$$

The parameter values can also be used for simulations in ADS. Therefore a simple model was build using C_{gs}, C_{gd}, R_{ds} and a voltage controlled current source for g_m. Also a noise current source is included to model the channel noise. In figure 3.5 this simple equivalent small signal model is shown.

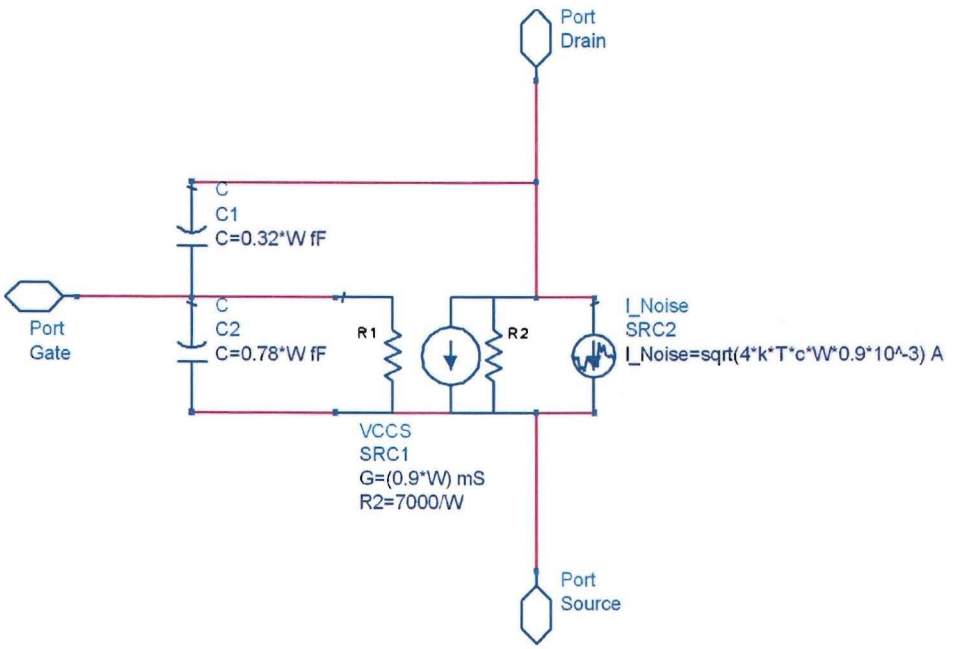


Figure 3.5: MOST model used in simulations in ADS with W being the MOST width (R_1 is made very high so it is negligible)

Chapter 4

Transformers

Every topology of interest for the implementation of the 60 GHz LNA makes use of a transformer for feedback purposes. Therefore a study was done on the behavior and modeling of the transformer, and its physical limitations in the CMOS 65 nm technology. First calculations are performed, and after that electromagnetic simulations are done to see the impact of the various parasitics. Also a single transformer has been taped-out to measure the transformer parameters and verify with the calculations and simulations.

4.1 Simple transformer model

To model the behavior of a transformer the following model can be used. The coupling between the two inductors is modeled using controlled current sources [2].

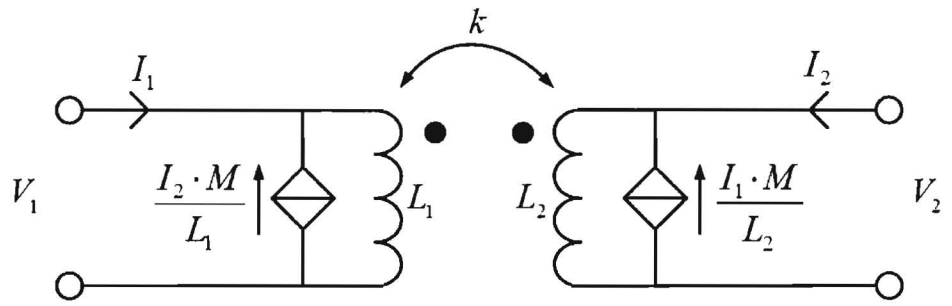


Figure 4.1: Transformer circuit

The current flowing through L_1 induces a current in L_2 and vice versa. The amount of coupling is given by k, the coupling factor. M is the mutual inductance, and is given by the following formula:

$$M = k\sqrt{L_1 L_2}$$

$$-1 \leq k \leq 1$$

Due to the coupling the voltages V_1 and V_2 are both functions of I_1 and I_2. Using the formulas for V_1 and V_2 it is possible to obtain equations for I_1 and I_2. These are the nodal equations of the circuit.

$$\begin{aligned} V_1 &= I_1 sL_1 + I_2 sM \\ V_2 &= I_2 sL_2 + I_1 sM \\ \rightarrow I_1 &= \frac{V_1}{s(1-k^2)L_1} - \frac{kV_2}{s(1-k^2)\sqrt{L_1 L_2}} \\ \rightarrow I_2 &= \frac{V_2}{s(1-k^2)L_2} - \frac{kV_1}{s(1-k^2)\sqrt{L_1 L_2}} \end{aligned}$$

To calculate the coupling factor, the H-parameters can be used [3]:

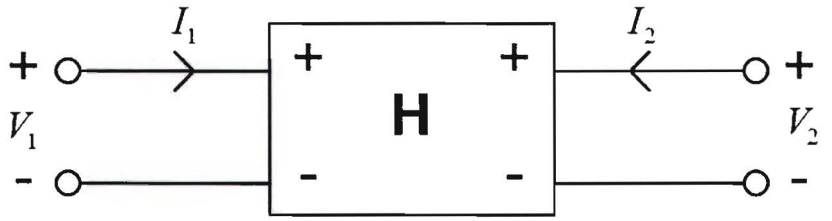


Figure 4.2: Definition of voltages and currents using the H-parameters

$$\mathbf{H} = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} V_1 \\ I_2 \end{bmatrix}$$

$$H_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0} = -k\sqrt{\frac{L_1}{L_2}}$$

So if the ratio between L_1 and L_2 are known, the coupling can be calculated using the following formula:

$$k = -H_{21}\sqrt{\frac{L_2}{L_1}}$$

4.2 Multi-turn inductor

A n turn inductor is a series connection of n inductors each having an inductance L. Because all these series inductances have mutual coupling with each other the model of figure 4.3 can be used to calculate the inductance seen at the terminals. The inductance seen at the terminals then can be calculated:

$$V = Is(nL) + \frac{IM}{L}s(nL)$$

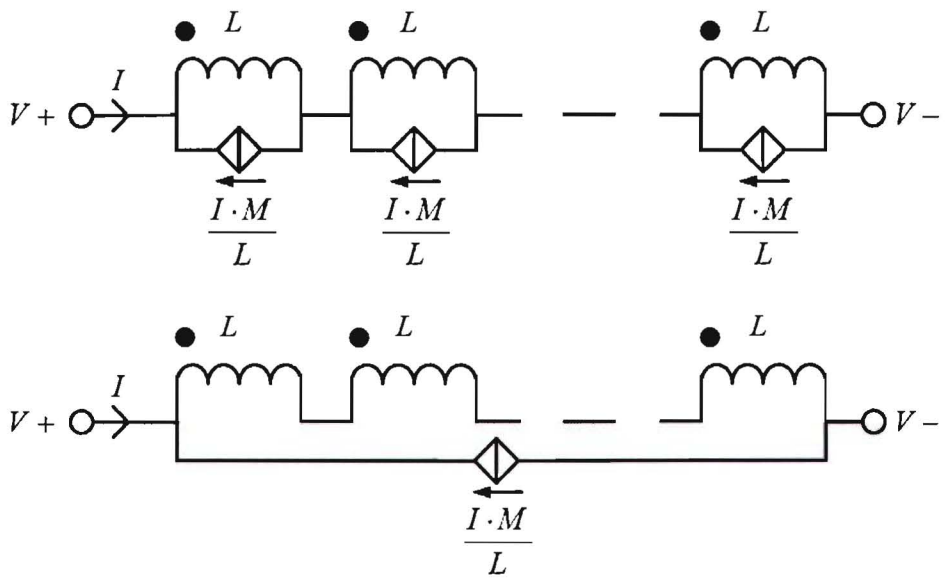


Figure 4.3: N turn inductor model

Because each turn "sees" $n-1$ turns each having a mutual coupling equal to $M = k\sqrt{LL} = kL$, the total mutual inductance is equal to:

$$M = kL(n-1)$$

$$\rightarrow Z = \frac{V}{I} = s(nL)(1 + k(n-1))$$

$$\lim_{k \to 1} s(nL)(1 + k(n-1)) = sn^2L$$

So the inductance of an inductor having n turns with $k = 1$ is equal to n^2L. Because in reality the coupling is always a bit less it will be lower.

This means that if a transformer has a turns ratio of n between the two inductors, the ratio between the two inductances will be n^2. So if L_1 has x turns and L_2 has xn turns, the inductance ratio is as follows:

$$\frac{L_2}{L_1} = \frac{(xn)^2L}{x^2L} = n^2$$

$$\rightarrow n = \sqrt{\frac{L_2}{L_1}}$$

4.3 Q-factor

Every metal line has a certain resistance, so the impedance of the inductors of the transformer also has a real part. This results in losses and generates noise. Therefore it is desirable to

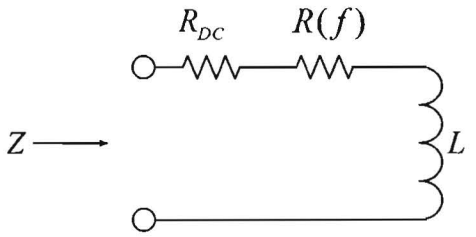


Figure 4.4: Q-factor

have low resistance in the inductors for most applications, such as the an LNA. To model this effect, the Q-factor of an R-L section is defined as follows (Z is the impedance seen looking into the inductor):

$$Q = \frac{\text{Energy stored}}{\text{Energy dissipated}} = \frac{Im[Z]}{Re[Z]} = \frac{\omega L}{R_{DC} + R(f)}$$

The resistance seen looking into the inductor consists of a DC-resistance R_{DC} and a frequency dependant part $R(f)$ due to the skin effect. At increasing frequencies the current flow through a conductor is concentrated at the surface. The current density J in an infinitely thick conductor decreases exponentially with depth δ from the surface, with J_S being the surface current:

$$J = J_S\, e^{-\delta/d}$$

The depth at which the current density has dropped to e^{-1} is defined as the skin depth:

$$d = \sqrt{\frac{2\rho}{\omega\mu}}$$

With ρ being the resistivity of the material and μ being the absolute magnetic permeability if the material.

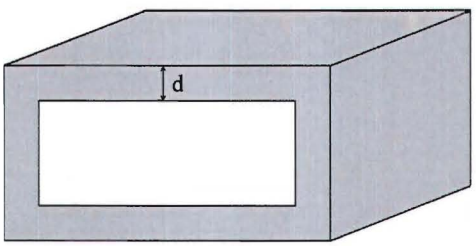


Figure 4.5: d denotes the skin depth

The skin effect is made visible in figure 4.5 of a modeled line. The current is concentrated in the gray area. This results in a smaller effective area for the current to flow through, causing a higher effective resistance. For copper the resulting skin depth at 60 GHz is equal to approximately 0.27 μm. For aluminum this value is equal to 0.33 μm at 60 GHz due to its higher resistivity. The thickness of the conductors is about 1 μm. Because of these small skin depths, they have to be taken into account during simulations.

The skin effect is also present in a via connecting the metal layers. A via consists of an array of metal connections. This way the different metal layers are connected to each other. If a high frequency current is driven through this structure, the current will be concentrated in the outer via's. This is shown in figure 4.6.

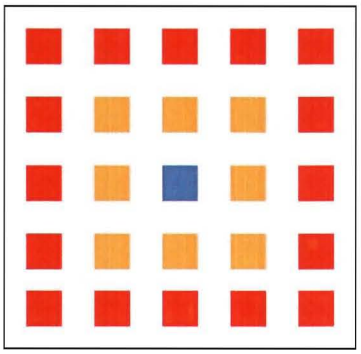


Figure 4.6: The HF behavior of a cluster of via's. The current is concentrated in the outer (red) via's.

Because there is less current flowing through the inner via's, the resistance seen at high frequencies increases, as expected due to the skin effect.

4.4 Positive and negative coupling

To determine how to connect a transformer to obtain positive or negative coupling, figure 4.7 is shown. As can be seen, if the outer inductor is exited, a current flow from the positive potential to the negative will result.

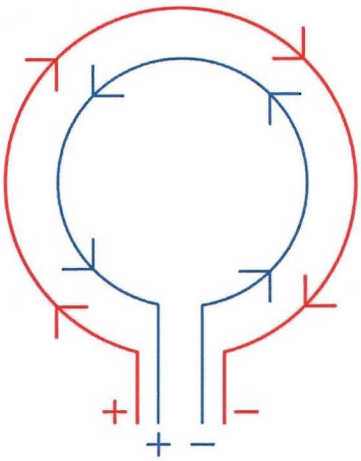


Figure 4.7: Action = reaction

This will result in a current flow in the inner inductor as well, but it will be in the opposite direction. The voltage induced will be as show in the figure. If both inductors are connected

to ground at the same side, a transformer with positive coupling results. On the other hand, if the outer inductor is connected to ground on one side, and the inner inductor is connected to ground on the other side, negative coupling results.

4.5 Transformer model using parasitics

To have a more accurate model for the transformer, some parasitics need to be taken into account. The main parasitics present in the transformer are the capacitances and resistances as seen in figure 4.8.

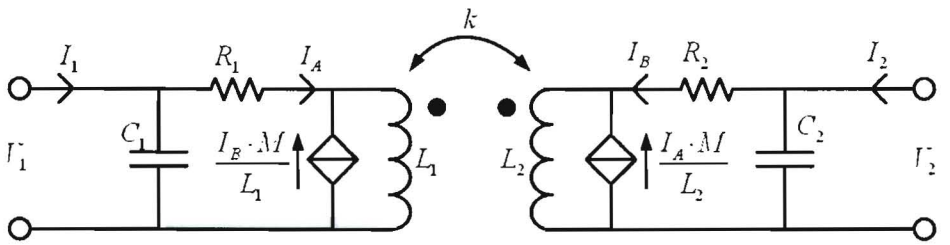


Figure 4.8: Transformer circuit with some parasitics

The transfer function $\frac{V_2}{V_1}$ is given in the formula below.

$$\frac{V_2}{V_1} = \frac{sI_1k\sqrt{L_1L_2} + I_2(sC_1((sL_1 + R_1)(sL_2 + R_2) - s^2k^2L_1L_2) + sL_2 + R_2)}{sI_2k\sqrt{L_1L_2} + I_1(sC_2((sL_1 + R_1)(sL_2 + R_2) - s^2k^2L_1L_2) + sL_1 + R_1)}$$

$$\left.\frac{V_2}{V_1}\right|_{I_2=0} = \frac{sk\sqrt{L_1L_2}}{sC_2((sL_1 + R_1)(sL_2 + R_2) - s^2k^2L_1L_2) + sL_1 + R_1}$$

The input impedance looks as follows:

$$Z_{in}|_{I_2=0} = \left.\frac{V_1}{I_1}\right|_{I_2=0} =$$

$$\frac{sC_2((sL_1 + R_1)(sL_2 + R_2) - s^2k^2L_1L_2) + sL_1 + R_1}{sC_1(sC_2((sL_1 + R_1)(sL_2 + R_2) - s^2k^2L_1L_2) + sL_1 + R_1) + sC_2(sL_2 + R_2) + 1}$$

To see where the resonance frequency occurs for high coupling, the resistances can be ignored.

$$\lim_{k\to 1}\lim_{R_1\to 0}\lim_{R_2\to 0} Z_{in}|_{I_2=0} = \frac{sL_s}{1 + s^2(L_1C_1 + L_2C_2)}$$

$$\rightarrow \omega_{res} = \frac{1}{\sqrt{L_1C_1 + L_2C_2}}$$

$$\rightarrow f_{res} = \frac{1}{2\pi\sqrt{L_1C_1 + L_2C_2}}$$

For an inductor on chip the parasitics scale approximately with the inductance value. Because of this, the biggest inductor has the highest value of both L and C. This results in approximately the following resonance frequency for $n > 1$:

$$\rightarrow f_{res} \approx \frac{1}{2\pi\sqrt{LC}}$$

With L and C of the biggest inductor. This means the unloaded resonance frequency of both inductors with high mutual coupling are the same, and it is dictated by the biggest inductor.

Another main effect is the existence of an interwinding capacitor C_m, as shown in figure 4.9. The transfer function of this transformer looks as follows (with the resistances neglected and $L_2 = n^2 L_1$):

$$\left.\frac{V_2}{V_1}\right|_{I_2=0} = \frac{s^2(1-k^2)L_2C_m + kn}{s^2(1-k^2)L_2(C_2+C_m)+1}$$

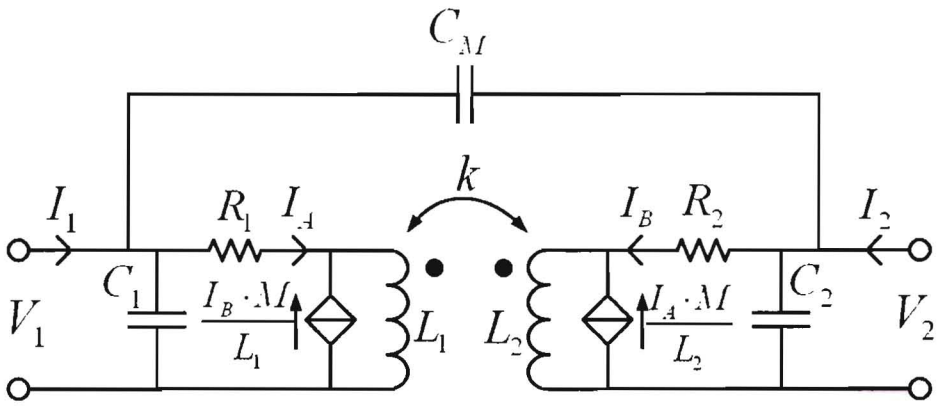


Figure 4.9: Transformer circuit with parasitics including C_m

As can be seen the transfer function has an extra double zero due to this capacitor. This zero results in a notch only for positive coupling and is situated at the following frequency:

$$f_{notch} = \frac{1}{2\pi}\sqrt{\frac{kn}{(1-k^2)L_2C_m}}$$

There occurs a resonance resulting in maximum voltage gain at the following frequency:

$$f = \frac{1}{2\pi\sqrt{(1-k^2)L_2(C_2+C_m)}}$$

The transfer function is given in figure 4.10 for a transformer with the following values: $L_1 = 25$ pH, $L_2 = 100$ pH, $R_1 = 0.9\ \Omega$, $R_2 = 3.7\ \Omega$, $C_1 = 2.5$ fF, $C_2 = 10$ fF and $C_m = 10$ fF. In the transfer function the notch is seen for positive coupling. Also the resonance is visible.

The input impedance looks as follows (with resistances neglected):

$$Z_{in}|_{I_2=0} = \left.\frac{V_1}{I_1}\right|_{I_2=0} =$$

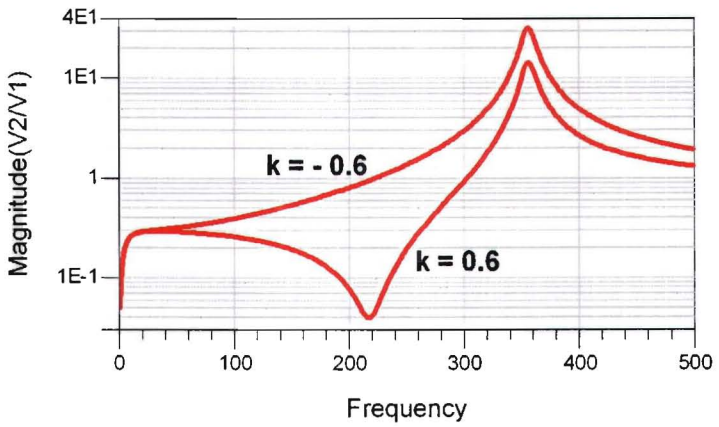


Figure 4.10: Transfer function of a transformer with positive and negative coupling

$$\frac{s^3L_1(1-k^2)L_2(C_2+C_m)+sL_1}{s^2L_1C_1(s^2(1-k^2)L_2(C_2+C_m)+1)+s^2L_2C_2(s^2(1-k^2)L_1C_m+1)+s^2(n^2-2kn+1)L_1C_m+1}$$

To see the effect of positive or negative coupling, the limit is taken for $k \to 1$ and $k \to -1$:

$$\lim_{k\to 1} Z_{in}|_{I_2=0} = \frac{sL_1}{s^2L_1C_1+s^2L_2C_2+s^2(1-n)^2L_1C_m+1}$$
$$= \frac{1}{s(C_1+n^2C_2+(1-n)^2C_m)+\frac{1}{sL_1}}$$

$$\lim_{k\to -1} Z_{in}|_{I_2=0} = \frac{sL_1}{s^2L_1C_1+s^2L_2C_2+s^2(1+n)^2L_1C_m+1}$$
$$= \frac{1}{s(C_1+n^2C_2+(1+n)^2C_m)+\frac{1}{sL_1}}$$

The effective amount of capacitance seen in the transformer responsible for the resonance frequency is seen to be bigger in the case of negative coupling:

$$C_1+n^2C_2+(1+n)^2C_m > C_1+n^2C_2+(1-n)^2C_m$$
$$(1+n)^2C_m > (1-n)^2C_m$$

Because of the voltage gain between the two nodes of the transformer the effective capacitance seen due to C_m increases for high n. This means a transformer with negative coupling will have a lower resonance frequency (concerning input impedance) in comparison with a transformer with positive coupling.

If n is chosen to be equal to one in combination with high positive coupling, this effect disappears because in that case there is no AC voltage over C_m present, the input impedance then reduces again to:

$$\lim_{k\to 1} Z_{in}|_{I_2=0,n=1} = \frac{1}{s(C_1+n^2C_2)+\frac{1}{sL_1}} = \frac{sL_1}{1+s^2(L_1C_1+L_2C_2)}$$

The inductance seen at the input of the given transformer, is shown in figure 4.11 for both positive and negative coupling. It can clearly be seen that in the case of negative coupling the resonance frequency is lower compared to the situation with positive coupling.

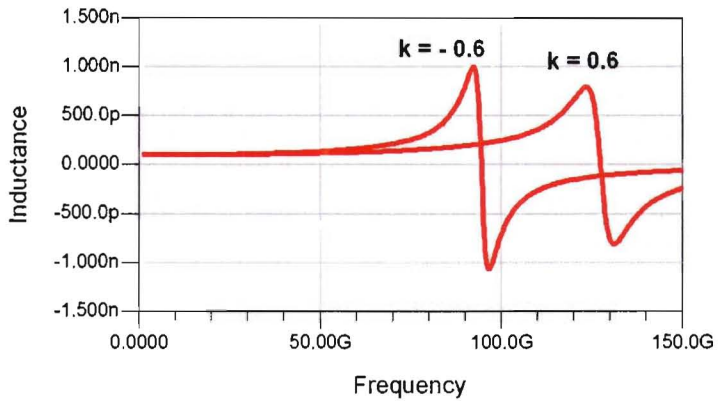


Figure 4.11: Inductance seen at the input of a transformer with positive and negative coupling

4.6 Starting point for the design of a transformer

To implement a transformer at the given frequency (60 GHz), an investigation has to be done to find out what the possibilities and restrictions are. Main design goals for a transformer are the primary and secondary inductances, the Q-factors of both inductors, the resonance frequencies and the mutual coupling. First the behavior of the inductance, Q-factor and resonance frequency will be investigated. The inductance and capacitance are linked in the following way assuming a lossless situation (L in H/m and C in F/m, v_p = phase velocity [5]):

$$v_p = \frac{1}{\sqrt{\epsilon_0 \epsilon_r \cdot \mu_0 \mu_r}} = \frac{1}{\sqrt{LC}}$$

This means that an increase in capacitance leads to a decrease of inductance, so it is desirable to keep the capacitance low. It is known from the stack information that the effective ϵ_r of the dielectrics of the complete stack used is approximately equal to 4.1. The value of μ_r is approximately equal to unity. To determine the exact values of L and C, simulations were performed using the top copper layer with various line widths with a length of 10 μm. After these simulations the inductance and capacitance (left axis) as well as the resistivity (right axis) at 60 GHz are determined, as shown in figure 4.12.

$$v_p = \frac{1}{\sqrt{LC}} = 142.7 \cdot 10^6 m/s$$

$$\rightarrow \epsilon_{r,eff} \approx 4.4$$

So the simulator gets a higher value than based on simple calculations. An explanation of this is the silicon substrate underneath the dielectrics and the fact the losses are not included in the calculation. The silicon substrate has an ϵ_r of approximately 11.9. The inductor and capacitor values can be approximated by a certain fitting. The inductance shows a behavior proportional to $1/W$ and the capacitance shows a behavior proportional to W. If L increases both capacitance and inductance increase proportional to L. The fitting looks as follows and is only valid for the used stack (width and length in μm):

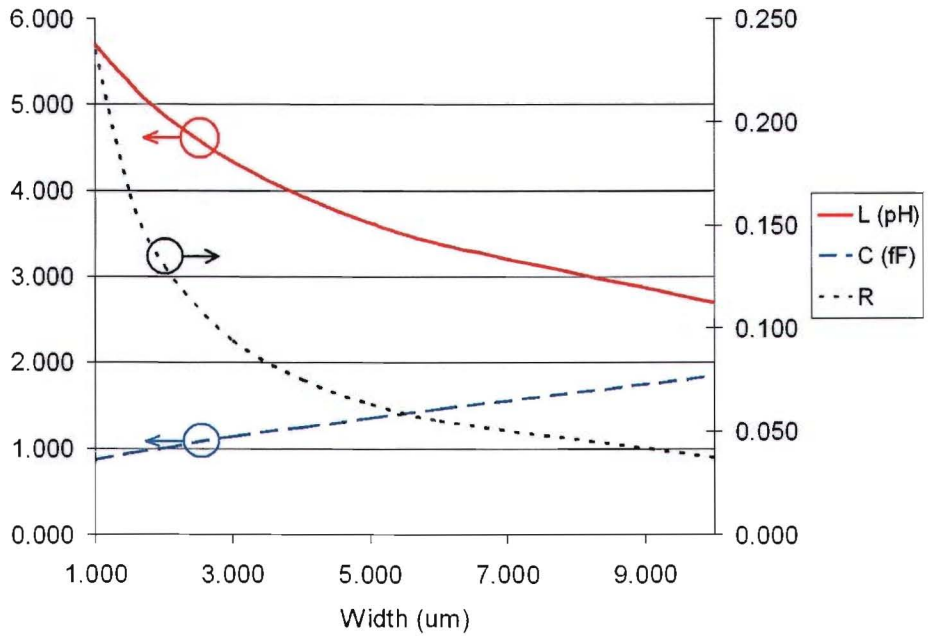


Figure 4.12: Simulated parameters with metal line length 10 μm

$$L \text{ (in pH)} \approx Length \cdot \frac{4.57}{Width + 7}$$

$$C \text{ (in fF)} \approx (0.0755 + 0.011 \cdot Width) \cdot Length$$

Using these formulas, the resonance frequency can be determined for a given length and resulting inductor value. If an inductor value of 70 pH is chosen, the resulting resonance frequency and Q-factor ($\frac{\omega L}{R}$) look as shown in figure 4.13. As can clearly be seen from this picture, the choice of metal width is a trade off between the resonance frequency and the Q-factor. A wide line width results in a high Q-factor, and a small metal width results in a high resonance frequency.

A choice was made based on these observations to use a metal width of 3-4 μm. The values used so far are used to get an indication of the values of the inductance, resistance and capacitance corresponding to a certain length and resulting diameter. The inductor value obtained when using a different shape will differ from these simulations because of for example coupling effects. As an example an inductor with a perimeter of 90 um is simulated. The simulated inductor value is 49 pH. When calculated using the values in the graph the value is 39 pH, a difference of 26 %.

Next feature to investigate is the coupling factor. Ideally this can vary between 0 and 1, or for negative coupling between 0 and -1. The transformer needed for the implementation of the LNA should have negative coupling. If the wanted coupling is low, the two inductors

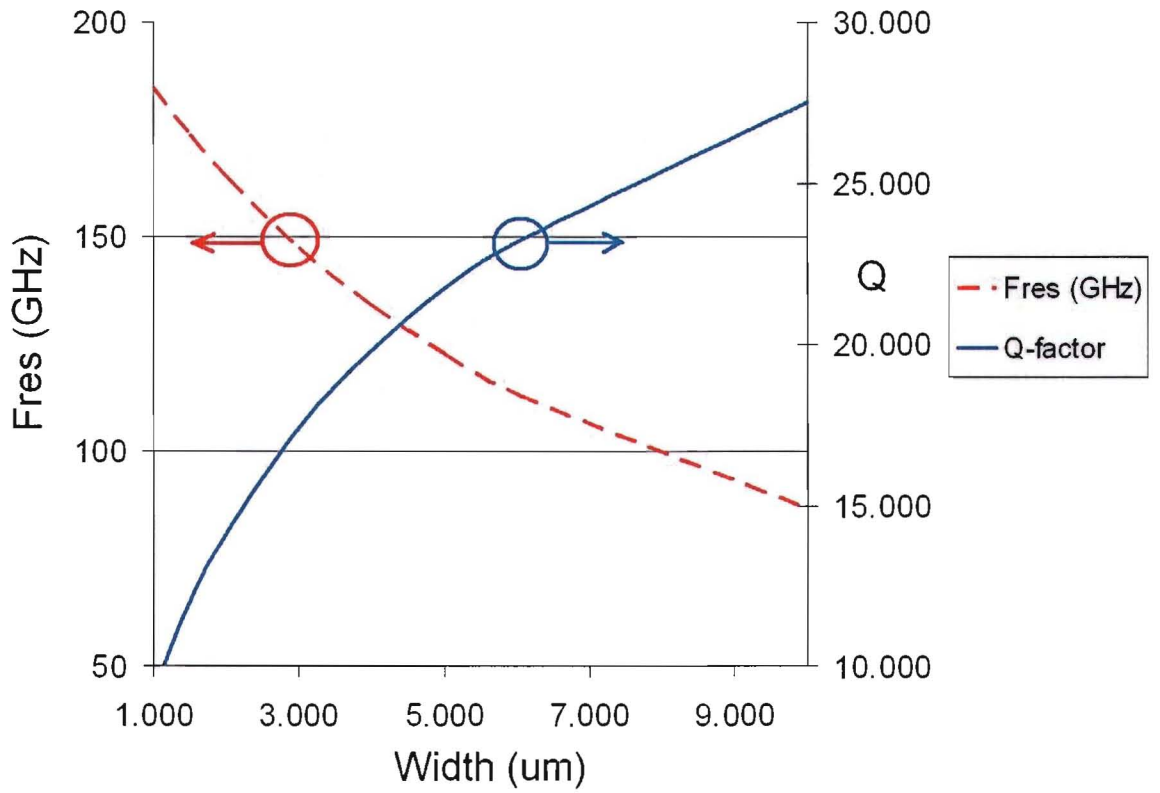


Figure 4.13: Resonance frequency and Q-factor of an inductor of 70 pH as a function of metal width.

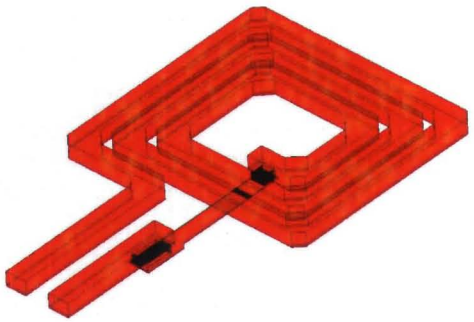
should be placed far apart. If on the other hand the coupling should be high, the inductors should be placed as close as possible. An interesting way of providing high coupling is to use two metal layers exactly underneath each other. This way there is very little distance so there will be high coupling, but there will be a large interwinding capacitance C_m, see figure 4.9.

An investigation was done to determine the coupling between the different metal layers. Two identical structures were used and placed exactly on top of each other. These simulations gave coupling factors of approximately 0.8, so the coupling possible using the given stack varies from 0 to 0.8 or from 0 to -0.8 for negative coupling.

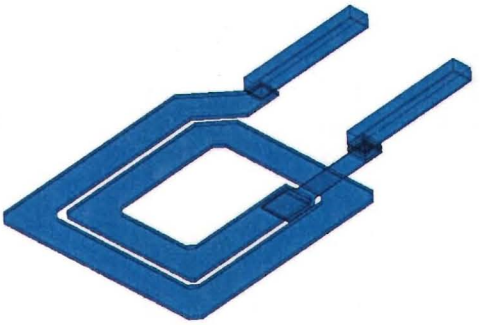
4.7 Single transformer tape-out

4.7.1 Simulation

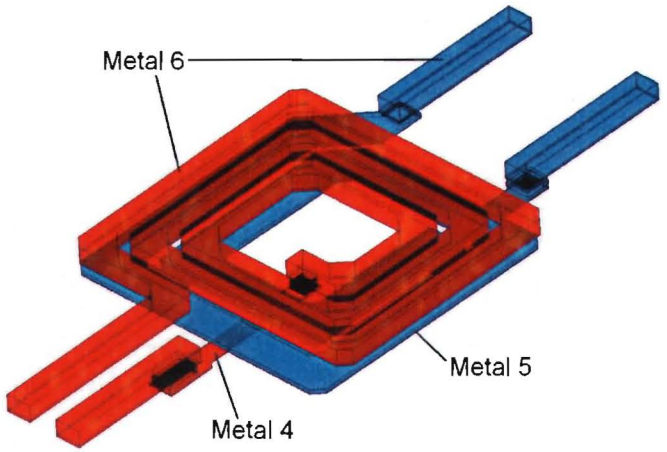
To verify the behavior of a transformer on chip with simulation results in Momentum, a transformer was designed and taped out. Using the design plan discussed in the previous section, a transformer was designed and taped out. The structure is shown in figures 4.14(a), 4.14(b) and 4.14(c).



(a) Primary inductor transformer



(b) Secondary inductor transformer

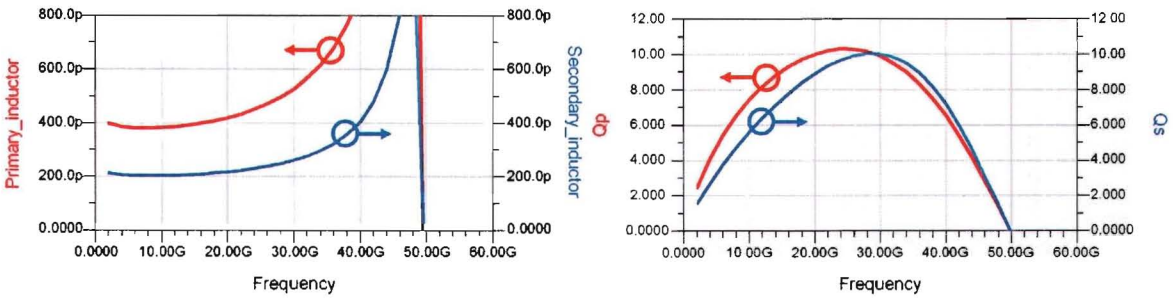


(c) Complete transformer structure

Figure 4.14: Transformer taped out for verification EM simulation vs. reality. To have $n \approx 1.5$ the primary inductor has three turns and the secondary has two turns. To have high coupling the two inductors are placed exactly on top of each other.

The simulation results for inductance and Q-factor (defined as $Im[Z]/Re[Z]$) are shown in figures 4.15(a) and 4.15(b). The simulated coupling factor at 20 GHz is approximately 0.7. The coupling factor is determined at this frequency because the resonance frequency is approximately at 50 GHz.

To model the behavior of the transformer it is possible to build a lumped element model. This model is shown in figure 4.17. Because of the negative coupling there is no notch present in the transfer function of the transformer. Therefore the capacitance between the windings can be modeled using a bigger capacitance at the positions of C_1 and C_2, and C_m can be omitted. The values for L_1 and L_2 used in the lumped element model are chosen approximately equal to the low frequency value seen in the simulation, so $L_1 \approx 385pH$ and $L_2 \approx 200pH$. To extract values for the resistance the quality factor is used. Then the value of the capacitances are fit using the resonance frequency. Capacitance will be added on both sides proportional to the inductor value because these parasitics scale approximately proportional to the inductor size. Last step is to include the coupling factor. This can be extracted from the simulation data using the H-parameters as already explained in section 4.1. This results in a coupling factor of 0.7. If C_m has to be extracted, the transformer can



(a) Simulated inductance.

(b) Simulated Quality factor.

Figure 4.15: Simulation results transformer.

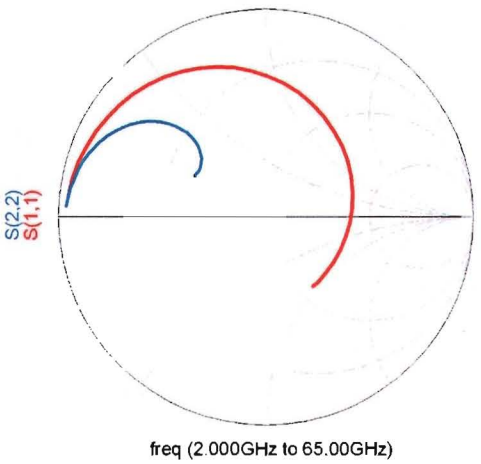


Figure 4.16: Smith chart of simulated s_{11} (primary inductor) and s_{22} (secondary inductor) with Z_0 of 100 Ω because of differential measurement.

be connected in such a way it has positive coupling. From the position of the notch the value of C_m can be extracted.

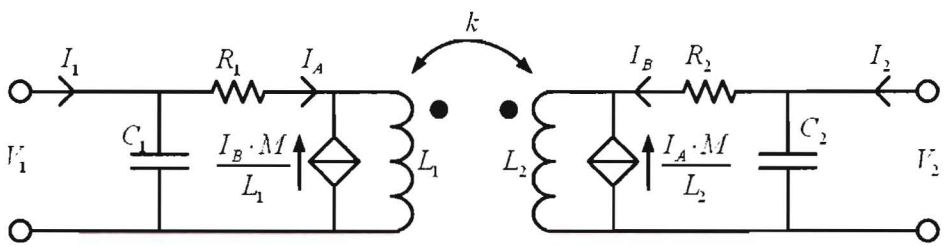


Figure 4.17: Transformer circuit with some parasitics

4.7.2 Layout

The layout of the transformer is shown in figure 4.18. As can be seen the transformer is in the center. The metal dots next to the transformer are there to fulfill the metal density rules of the TSMC process. The transformer is connected to the GSGSG (G = ground, S = signal) bondpads on the top and bottom by using coplanar waveguides. These waveguides have a characteristic impedance of 50 Ω, because the measurement setup is also at 50 Ω (100 Ω differential).

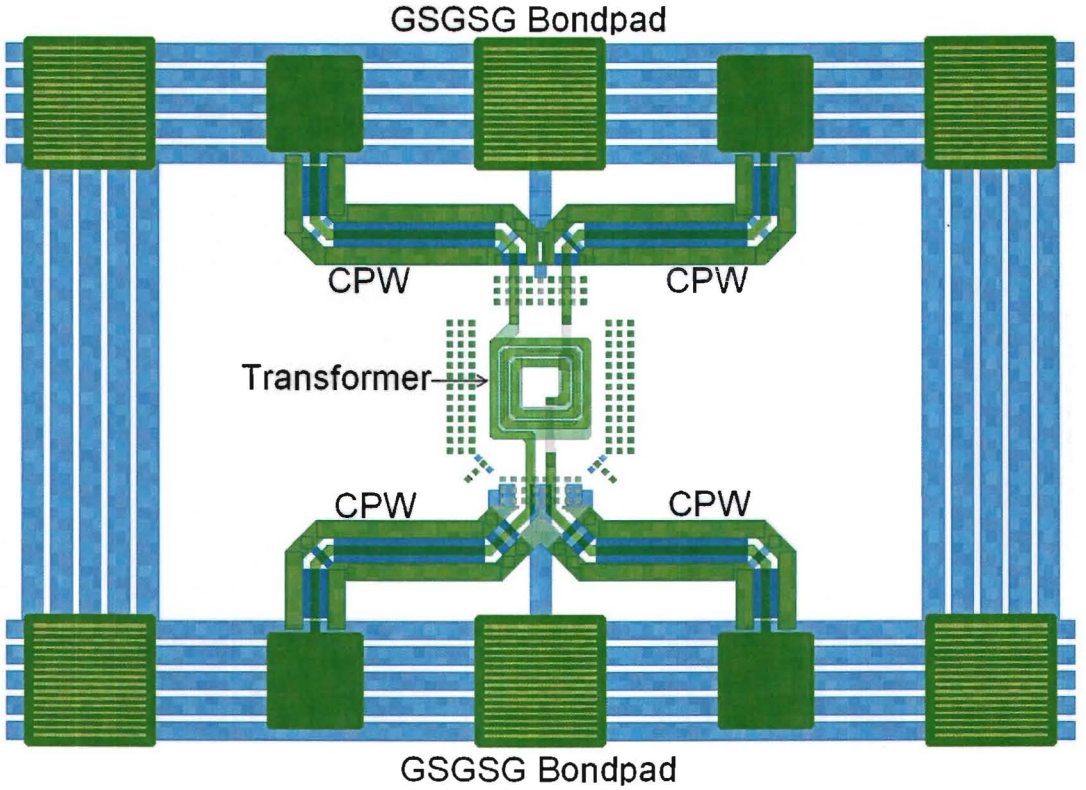


Figure 4.18: Layout of the transformer.

The waveguides and bondpads will have a big influence on the measurement, and can not be simulated in ADS Momentum along because of memory reasons. So to be able to measure the transformer solely, also de-embedding structures have been included. These de-embedding structures consist of the bondpads with the coplanar waveguides (CPW's) but without the transformer. Three structures were prepared, one with the CPW's left open, one with the CPW's shorted, and one with a line connecting the top CPW's with the bottom CPW's. This way the structure without the transformer can be modeled and subtracted from the measurement of the transformer with the CPW's and the bondpad. This will result in the behavior of the transformer solely. Because of area reasons only the open and short structures were taped out, resulting in less reliability for the de-embedding above 20-30 GHz because of the missing line structure. In figure 4.19 a microphotograph of the chip several months after the tape-out is shown. As can be seen there are a lot more metal dots added. This has been done automatically to fulfill the TSMC metal densities.

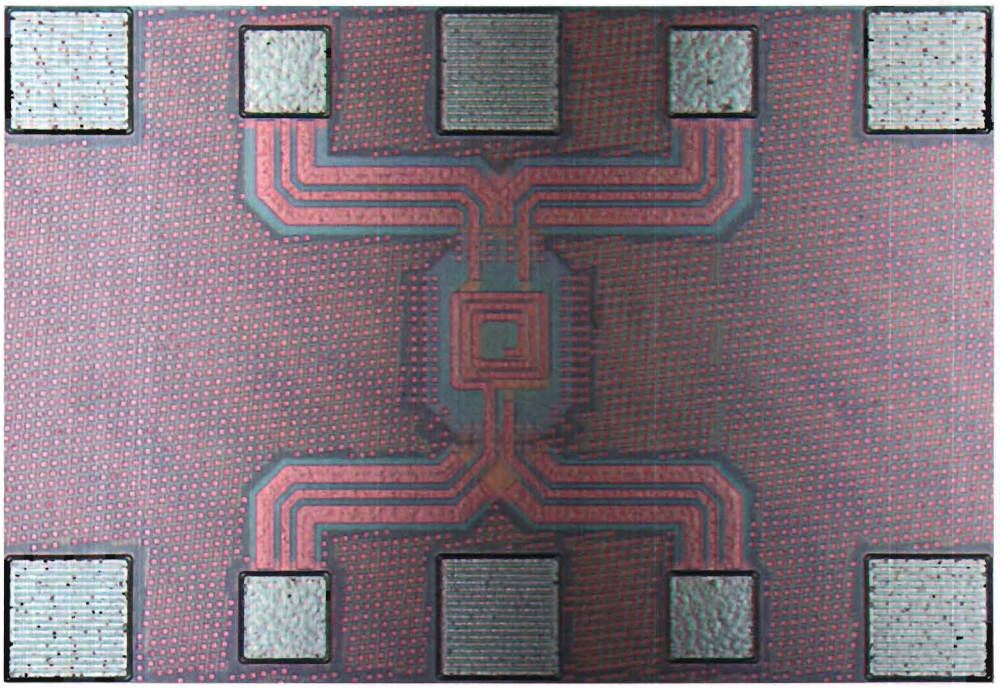


Figure 4.19: Chip microphotograph of transformer.

4.7.3 Measurement

The transformer was taped out in August 2007 and was measured several months later. In figures 4.20 and 4.21 the measurement setup is shown.

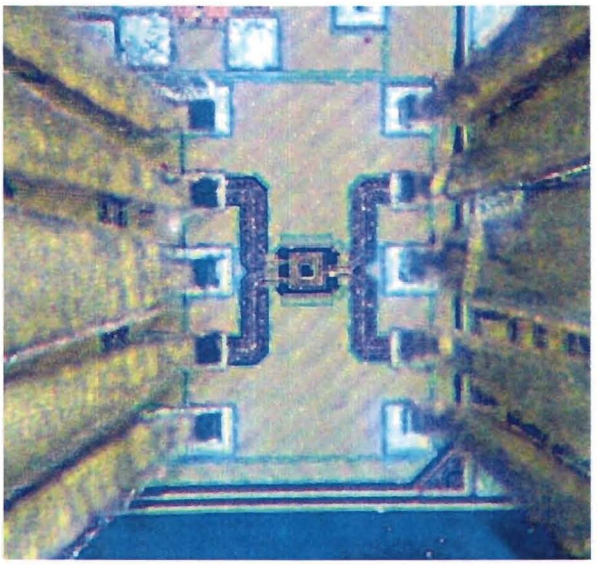


Figure 4.20: Chip microphotograph of transformer during measurements.

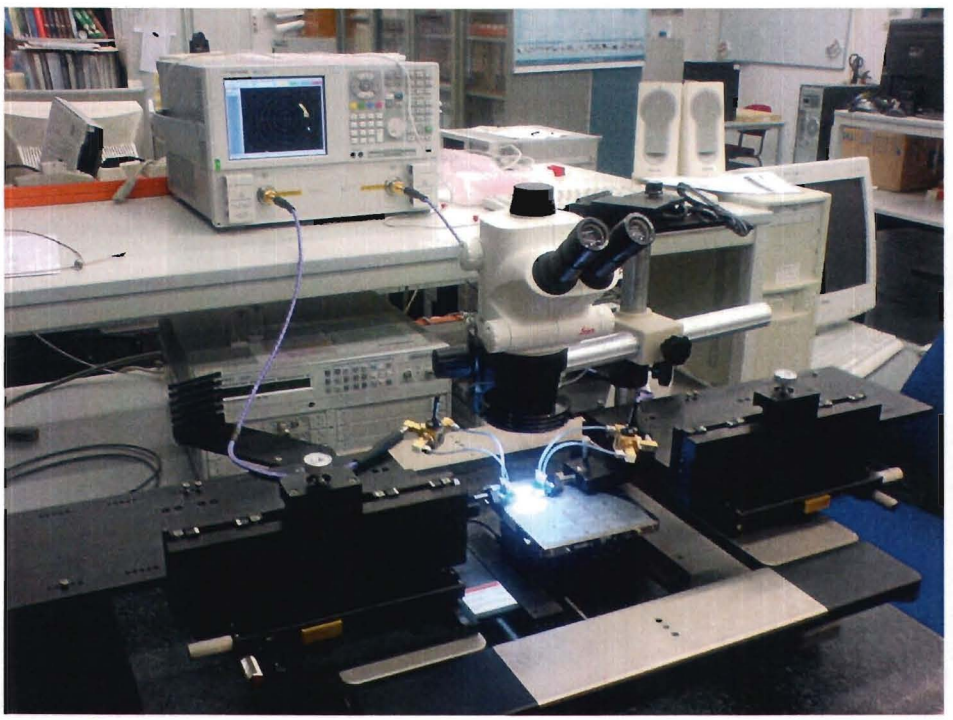


Figure 4.21: Measurement setup.

Several measurements were performed on the transformer. The transformer was measured from 10 - 40 GHz. The measurements above this frequency range were very difficult (if not impossible) due to the missing de-embedding structure. The measurement results are shown in figures 4.22 and 4.23.

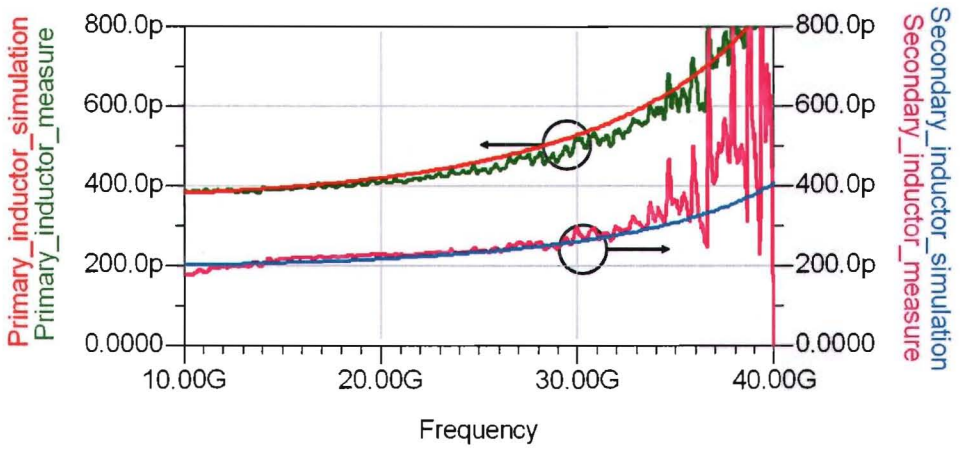


Figure 4.22: Inductance measurement versus simulation 10-40 GHz. The results are quite similar, the biggest deviation is observed for the high frequency behavior of the secondary inductance.

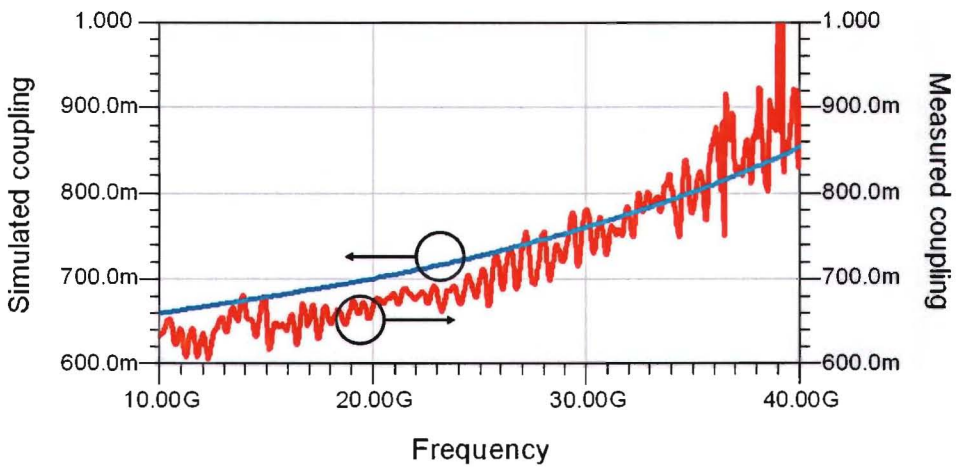


Figure 4.23: Coupling measurement versus simulation 10-40 GHz.

The Q-factors were very difficult to measure and didn't give accurate results. The measured values for inductance and coupling show very small deviations from the simulated values. In the following table the measured values are compared with the simulated values, for low frequencies:

Parameter	Simulation	Measurement
L_p	$\approx$ 385 pH	$\approx$ 385 pH
L_s	$\approx$ 200 pH	$\approx$ 200 pH
Coupling (at 20 GHz)	$\approx$ 0.7	$\approx$ 0.67

As can be seen the values for the primary and secondary inductances are quite accurate. The coupling seems to be a bit less in reality, but the difference is very small. Conclusion is the simulation in Momentum comes quite close concerning inductance but it gives slight more coupling than seen in reality.

4.8 Transformer implemented LNA

Next a transformer for the LNA will be designed. This transformer has to be implemented in a slight different stack, resulting in slight different behavior. To model this behavior again the same procedure is followed as in the previous section.

4.8.1 Stack information

In the documentation from TSMC, information of how the chip is being build up is given. With this it is possible to generate a substrate file in which ADS Momentum can perform it's simulations. To implement the inductors it is best to choose the metal layers that have the most distance from the substrate. This is to prevent mutual coupling between the inductor and the conductive silicon. This coupling results in losses and gives a low Q-factor of the passive device, which is unwanted. The used stack consists of seven copper layers and one aluminum layer above them. The two top copper layers have a higher thickness (lower resistance) compared to the lower layers.

4.8.2 Design goals and how to get there

Simulations show it is best to have a high Q-factor in the drain inductor in comparison to the source inductor for both gain and noise performance. So during the design, the Q-factor of the drain inductor is most important. To obtain the exact values of the drain and source inductor, simulations using Cadence are performed.

To fulfill the output isolation requirement ($\frac{n}{k} = -\frac{C_{gs}}{C_{gd}}$) the coupling between the aluminum and the two top metal layers has to be determined. A simulation was performed for this. This simulated coupling is equal to approximately -0.72. The ratio between C_{gs} and C_{gd} is approximately equal to 2.3, resulting in a turns ratio of 1.7. With these values, simulations in Cadence were performed to find the optimal source (and resulting drain) inductor value. This resulted in the following design specifications:

L_d	$\approx$ 90 pH
L_s	$\approx$ 30 pH
Coupling	$\approx$ -0.75

To achieve these goals, several choices have to be made. As already stated in the previous sections a line width of 3 - 4 μm gives the best results concerning Q-factor and resonance frequency. The remaining unknown variables are the diameter of the inductors, the number

of windings for each inductor, the metal layers to use for the inductors and the structure. Of course also the design rules and current density rules have to be taken into account.

Some of these questions can be answered after studying the stack info. To implement the transformer, the three top metal layers have been chosen to be used because then the highest quality factors can be obtained (thickest metal layers with the most distance from the substrate). To design the source inductor, the top metal (aluminum) is chosen. For the drain inductor the two metal layers underneath are chosen. This way the drain inductor consists of two metal layers which results in a high Q-factor. The source inductor will have a slight lower Q-factor.

Simulations show that multiple turns will result in low resonance frequencies because of high capacitance in the inductor itself. Therefore it is most interesting to use as little turns as possible for the inductors used in the transformer. To end up with a turns ratio of 1.7, the drain inductor is given two turns and the source inductor is given one turn. Of course this will result in a turns ratio of 2, which is too high.

Therefore the overlapping connections are made with a certain length. These will have an inductance ratio of one, so also a turns ratio of one. The resulting total turns ratio of the complete structure will therefore have a turns ratio smaller than two but bigger than one. If the dimensions are chosen correctly, this will result in a turns ratio of 1.7.

Last question to be asked before designing the transformer is the diameter of the inductors. This diameter sets the inductance value of both inductors. Simulations show best results for a source inductance of approximately 30 pH, which is already a very small inductance. Simulations will be performed to achieve this inductance. This will give an indication of the diameter of the source and drain inductor.

4.8.3 Design source inductor

The source inductor has to be implemented in the aluminum layer and has to have an inductor value of approximately 30 pH. Simulations were performed for this and gave an outer diameter of 33 μm. The resulting structure is shown in figure 4.24. To have maximum coupling, the inductor has exactly the same shape as the drain inductor (see next section), but only one turn. This results in two turns that are shorted at the position were the drain inductor connects the two turns. As can be seen from the figure the connections connecting the two inductors have a certain length resulting in a turns ratio of approximately 1.7 with respect to the drain inductor.

Reason to choose for an octagonal shape is because this gives a higher Q-factor compared to a square design. In fact, an circle is ideal, but not allowed by the TSMC design rules. As can be seen from this figure the source inductor also has a center tap connection for connecting the ground. Through this center tap and also through the inductor itself, the DC-bias current has to flow. Because the relatively low electro-migration of the used metal (aluminum), this sets an upper bound to the maximum DC-current. Resulting maximum DC-current through this inductor is 21 mA. So in the eventual design, a maximum of 21 mA can flow through each stage. To get the most accurate simulation results, also the connections to metal 7 in the center tap and to the transistors are drawn.

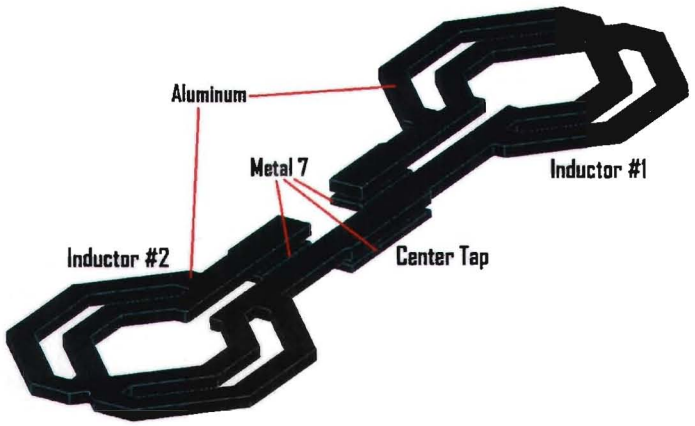


Figure 4.24: Source inductor

4.8.4 Design drain inductor

The drain inductor has to be implemented in the two top metal layers underneath the aluminum and has to have an inductor value of approximately 90 pH. It also has to consist of 1.7 turns with respect to L_s. Therefore L_d is chosen to be a two turn inductor. The voltage-voltage transformer feedback LNA has a differential structure with DC bias current through L_d. This means it has to be implemented in a differential fashion with center-tap. Also the maximum current density has to be taken into account during the design, but because of the high electro-migration possible in copper, this is not a problem in the drain inductor.

During the design of the transformer, it also has to be taken into account how the structure will be implemented in the layout. The structure has to obey the design rules of the TSMC 65nm technology. The output of the LNA is situated at the drain inductor. Therefore connections will be made for connecting the inductor to a differential coplanar waveguide. After several simulations to obtain the right inductor value, the structure shown in figure 4.25 for L_d is found.

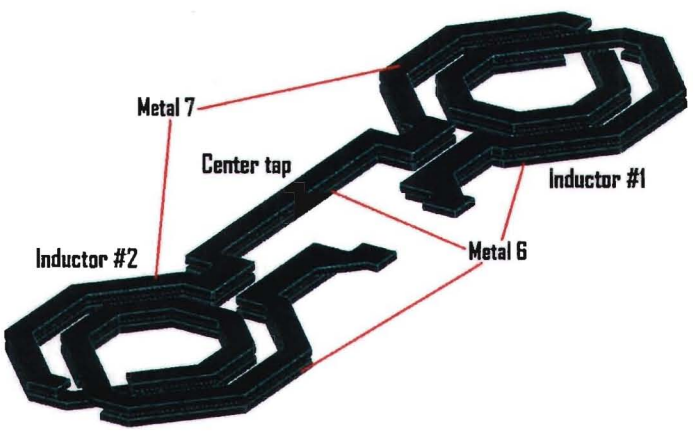


Figure 4.25: Drain inductor

As can be seen from figure 4.25 there are two inductors due to the differential structure. The center tap at the left will be used for connection to Vdd. At the right the connection to the differential coplanar waveguide can be seen.

4.8.5 Transformer layout and simulations

To implement the complete transformer, the drain and source inductor are joined together in an inverting fashion. The resulting structure is shown in figure 4.26.

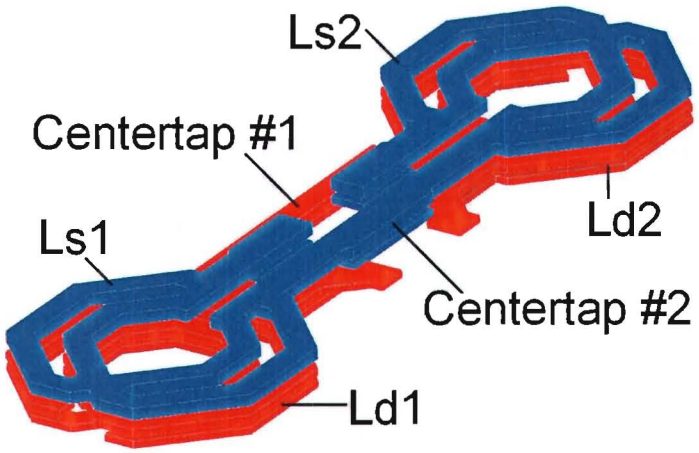
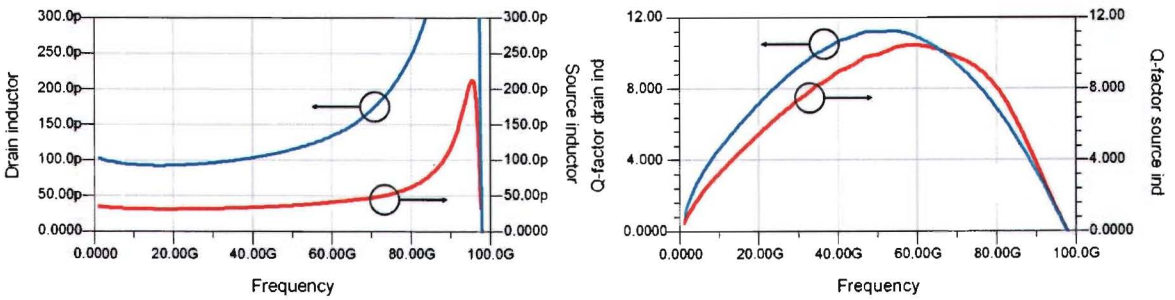


Figure 4.26: Transformer with on top blue L_s and below red L_d

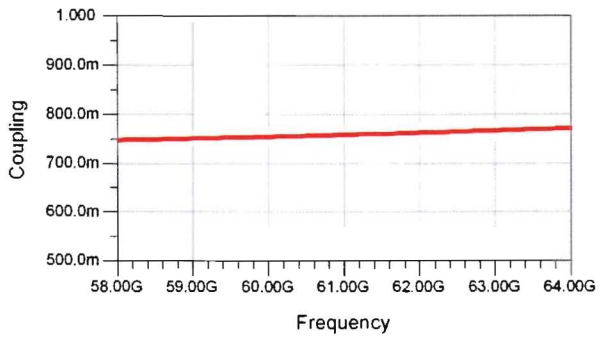
With this structure again simulations are performed to get the values for the inductance, the losses resulting in a certain Q-factor, and the coupling. The simulation results are shown in figures 4.27(a), 4.27(b) and 4.27(c).

As can be seen, the inductor values and the resulting n are approximately right. The Q factors are both > 10 and $Q_d > Q_s$. The resonance frequency is quite low due to the inverting coupling and is approximately 98 GHz. The coupling is about -0.75. The ratio between n and k is approximately 2.3. To be able to do s-parameter simulations in Cadence using this transformer model, a s-parameter dataset is generated in Momentum and imported in Cadence. Therefore a very wideband simulation was done from 8 MHz to 300 GHz. This is done to include frequency dependent behavior to determine for example the stability. For DC-resistance a low frequency simulation is needed (8 MHz).



(a) Inductances.

(b) Q-factors.



(c) Coupling factor in the band of interest.

Figure 4.27: Simulation results transformer to be implemented in the LNA.

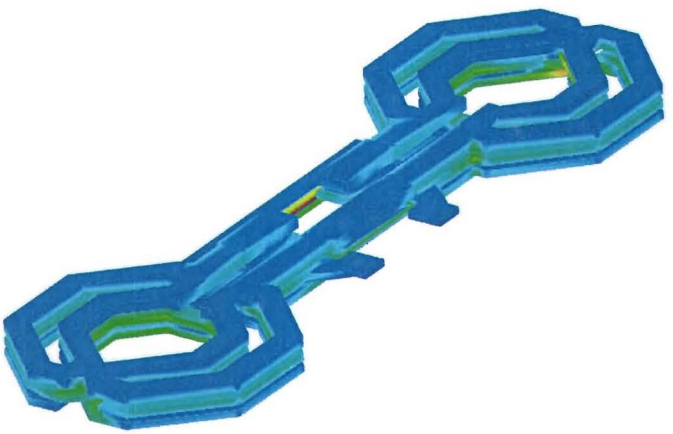


Figure 4.28: Current density plot of the transformer

Chapter 5

Design V-V feedback LNA

After the first hand calculations, a start was made with the eventual design using the PSP transistor model, and momentum simulations for various passive devices. The circuit level simulations were performed in Cadence. Design goal used during the design is maximizing the space between the NF and s_{21} parameter. A maximum performance curve was identified as a function of transistor width. Next the IIP_3 performance as a function of transistor width is determined. Then a choice was made looking at the possibility of the design in reality, taking realistic component values into consideration.

5.1 Single stage design

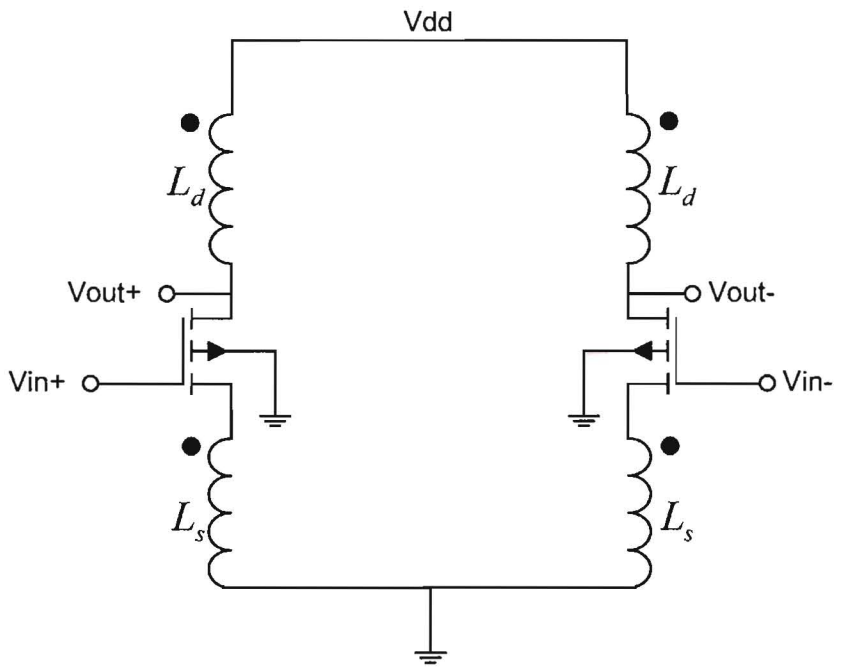


Figure 5.1: Schematic of the voltage-voltage transformer feedback LNA

5.1.1 Starting point based on calculations

From calculations the initial values for the different components have been determined. A summary of these component values are:

For maximal gain:

$$L_s = \frac{1}{\omega^2(n^2 C_{gd} + C_{gs})}$$

To provide impedance matching, the imaginary part of the input impedance has to be tuned out. This can be done using the following value for a gate inductor L_g which is equal for both noise performance and power match:

$$L_g = -\frac{Im[Z_{in}]}{\omega} \approx \frac{1}{\omega^2 C_{gd}(1+n)}$$

This gives the following curves for the inductances versus the transistor width (both single ended values):

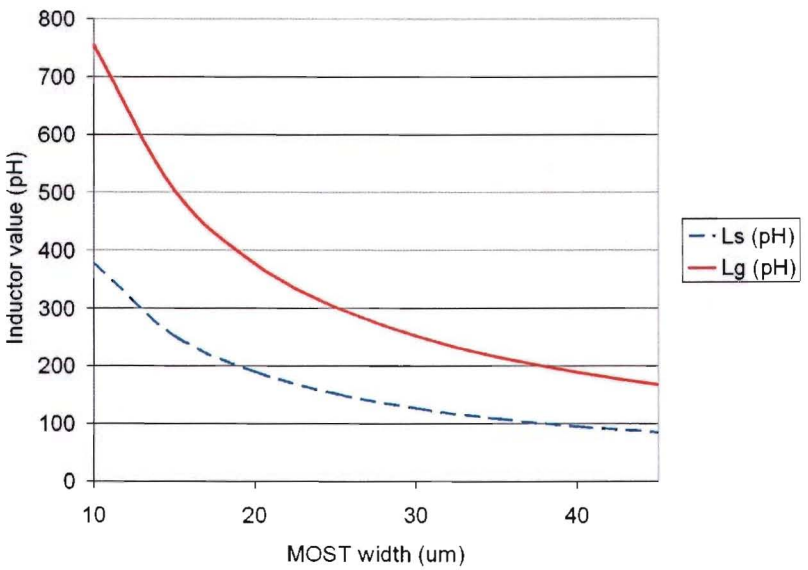


Figure 5.2: Inductances to be used in the schematic based on calculations. As can be seen $L_g > L_s$.

To provide output isolation the following statement should hold:

$$\frac{n}{k} = -\frac{C_{gs}}{C_{gd}}$$

To have high gain, n should be high, so also k should be high. As seen during calculations, the input impedance might become negative if the ratio of n and k becomes larger than C_{gs}/C_{gd}. This should be prevented. This means all component values are known by

calculation. Of course these values will differ from the values to be used in Cadence because the models used are much simpler than the models Cadence uses.

During the design the stability of the LNA should be investigated for both differential and common mode signals. Because the LNA has an $s_{21} > 1$, it is possible to create a loop gain > 1, which can result in instability. If the LNA becomes instable, which can occur for a very wide band of frequencies, it behaves as an oscillator. This of course is an unwanted situation. To check the circuit, the following formulas were used [5]:

$$K = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |\Delta|^2}{2|s_{12}s_{21}|}$$

$$\Delta = s_{11}s_{22} - s_{12}s_{21}$$

If $K > 1$ and $|\Delta| < 1$, the system is unconditionally stable.

5.1.2 Noise figure and s_{21}

Using these figures as a starting point, simulations were performed. During these simulations, lower values for L_s and L_g were found to be optimal. Explanation for this are the extra parasitics (capacitors) in the components. After several simulations the exact component values including parasitics were determined to have maximal performance, using a transformer with n = 1.7 and k = -0.7 - -0.8. The biasing of the transistors was chosen as stated in the section about the MOST modeling. These component values gave the performance shown in figure 5.3 concerning gain and noise figure (NF) versus transistor width.

As can be seen, the performance changes only little varying the transistor width (as expected), but a big MOST gives slight better results. On the other hand, a large transistor consumes more power than a small transistor for the same bias current density through the transistor channel. Conclusion is that concerning noise figure and gain every transistor width can be chosen, if feasibility of the inductances is not taken into account.

5.1.3 IIP_3 and 1 dB_c

Next, simulations were performed for IIP_3 and 1 dB_c. These are shown in figures 5.4(a) and 5.4(b).

As can be seen in these figures, maximum IIP_3 is achieved using a transistor of approximately 25 μm. The 1 dB_c increases with transistor width. This can be explained from the fact that the big transistor uses lower impedance levels to operate optimal, so it can generate higher output current levels, while maintaining the same voltage levels. From figure 5.4(b) it can very well be seen that a higher 1 dB_c takes a higher power consumption. Conclusion is that for higher linearity, a wide transistor has to be chosen, at the cost of power consumption. For optimal IP_3 performance a transistor width of 25 μm gives best results.

5.1.4 In and output impedances

As already stated, the imaginary part of the input impedance can be tuned out with an inductor. The frequency for which this input match becomes resonant, is approximately equal to the center frequency of the pass-band of the LNA. The real part of the input impedance is low

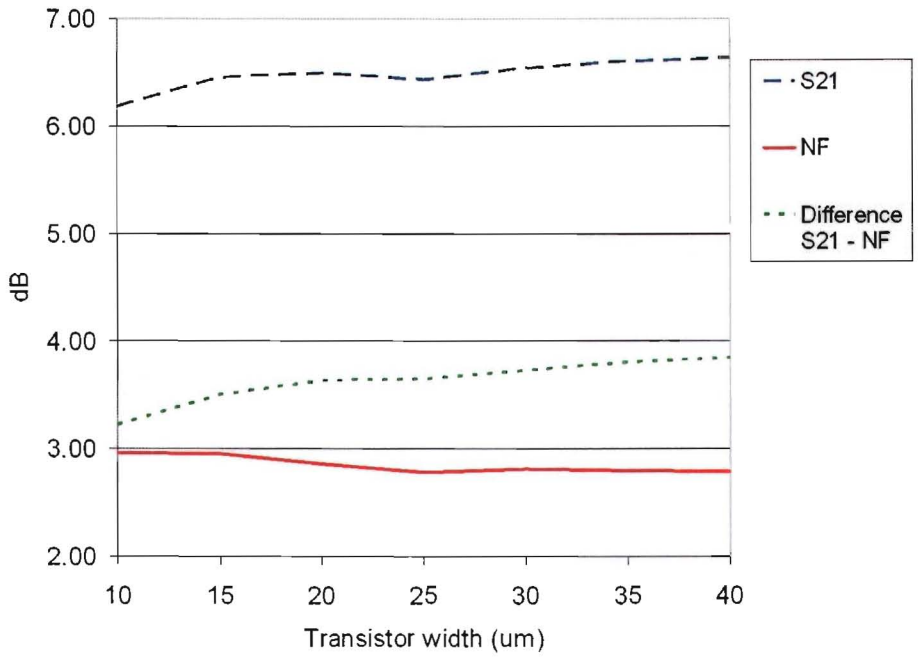
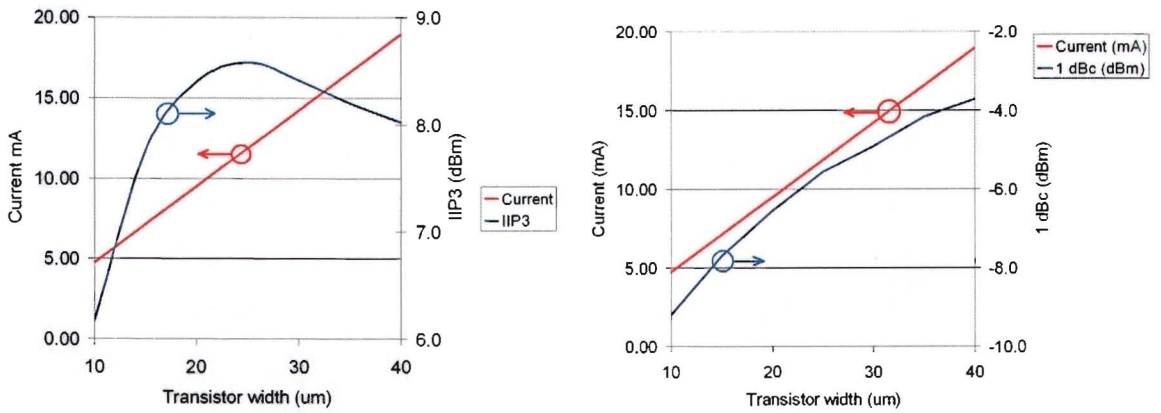


Figure 5.3: Simulation results of s_{21} and noise figure versus MOST width



(a) IIP_3 (b) 1 dB_c

Figure 5.4: Simulation results of IIP_3, 1 dB_c and DC current consumption versus MOST width.

in comparison to the imaginary part, as already calculated, when output isolation is applied. To get maximum gain, the source resistance must be chosen approximately equal to the input resistance. For noise considerations on the other hand, simulations (and calculations) show a higher optimal source impedance level. Therefore a tradeoff has to be applied for this (see figure 5.5).

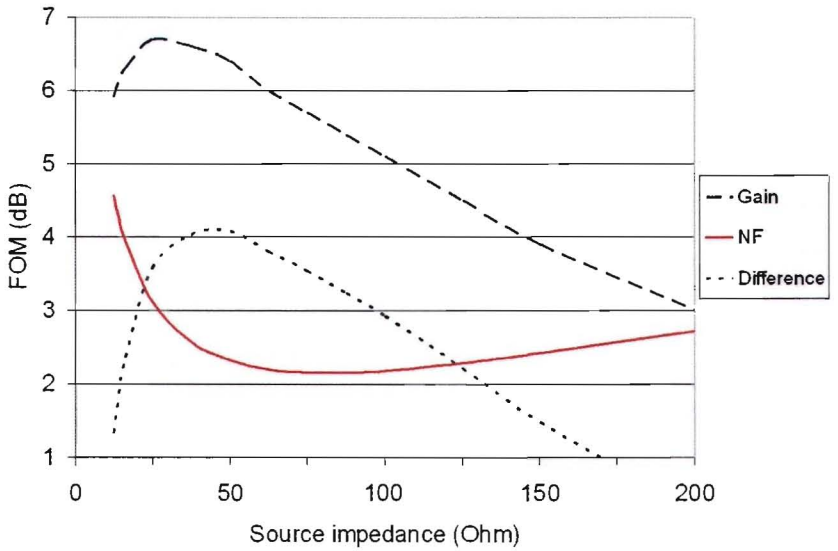


Figure 5.5: NF, s_{21} and the difference between them versus source impedance ($W_{MOST} = 30\mu$m).

The simulated output impedance has a real part that lies above the real part of the input impedance. The imaginary part behaves inductive, and can thus be canceled using a shunt capacitor. This capacitor value is in the order of magnitude of the parasitic capacitance of the transformer, so if the transformer is chosen correctly, it can be omitted.

5.2 Dual stage design

To be able to provide enough gain, more stages are needed. One stage gives a s_{21} of approximately 6.5 dB, so two stages should be able to provide approximately 13 dB, ideally. Decided was to look at a two stage design, because a three stage design gives more complexity and consumes more current. In case of a two stage design, the overall noise figure is dominated by the first stage. The second stage is dominant concerning IIP_3. So when designing the two stages, it is important to optimize the first design for both noise figure and gain. For the second stage the important parameters are IIP_3 and gain. Simulations were performed for a cascade of two stages each having a different transistor width and component parameters chosen using the results of the previous section. The results concerning gain are given in figure 5.6.

As can be seen, the gain is maximal for $W_1 > W_2$. Reason for this is the output impedance of the first stage and the input impedance of the second stage. To have maximal gain, the input impedance of the second stage should be high in comparison to the output impedance of the first stage. This is achieved with a wide transistor in the input stage and a small transistor in the second stage.

Next feature to be investigated is the noise figure. The simulation results of noise figure versus the MOST widths of the first and second stage show the variation is very small. The noise figure achieved in the two stage is approximately equal to 3-3.1 dB. For the choice of which transistor combination to be used, the noise performance can be neglected. This

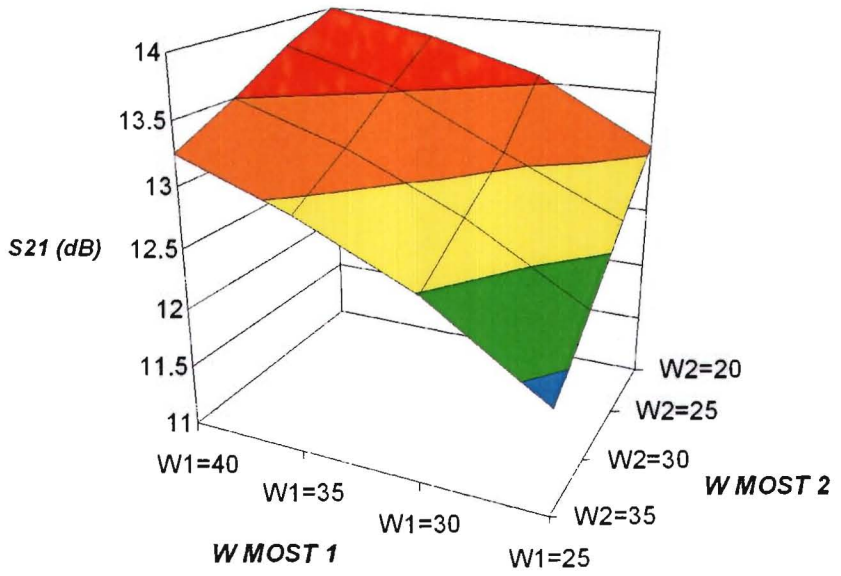
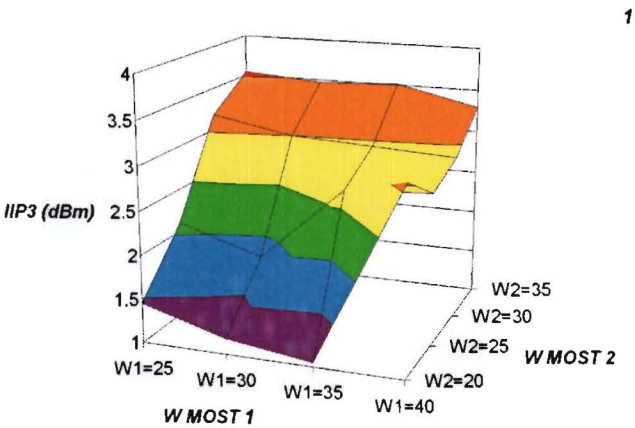
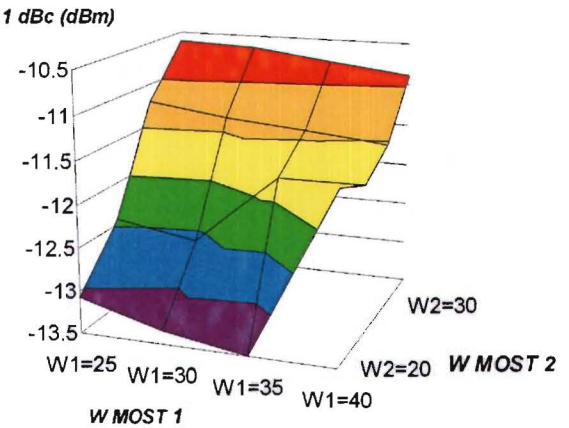


Figure 5.6: s_{21} versus MOST 1 width (first stage) and MOST 2 width (second stage).

is expected because the noise figure is dominated by the first stage and is approximately constant over the variation of the MOST width (as seen in calculation and simulation). After the gain and noise performance, linearity is investigated. IIP_3 and 1 dB_c simulations are shown in figures 5.7(a) and 5.7(b).



(a) IIP_3 versus W_1 and W_2.



(b) 1 dB_c versus W_1 and W_2.

Figure 5.7: Simulation results for the two stage circuit concerning IIP_3 and 1 dB_c.

As expected the best performance concerning linearity are found for wide transistors. It is also clear that the transistor width of the second stage is dominant for both IIP_3 and 1 dB_c performance, as expected.

Next issue to consider is the feasibility of the components to be used. During simulations using Momentum, it became clear that an inductor value of approximately 150 pH is the maximum value possible to be used at 60 GHz concerning the resonance frequency. The

biggest inductor in the design is the gate inductance used to resonate with the capacitive input impedance. Based on the simulations a choice was made to have $W_1 > W_2$, mainly because of gain considerations. The biggest resulting inductor then is the gate inductance of the second stage. Because the output impedance of the first stage behaves inductive, the gate inductance connecting the two stages can do with a slight lower value than in the case of a single stage excitation. The smallest value of W_2 possible concerning the gate inductance is found to be approximately 25 μm.

The biggest value of W_1 is given by the minimal source inductance possible. This value was found to be 30 pH during simulations in Momentum. The transistor width having maximal performance with this source inductance is 35 μm. With this combination, there is both good performance concerning gain and linearity. Another reason not to choose it wider, is keeping the power consumption low. Increasing power will give rise to problems with the electro-migration of the metal. The resulting schematic is shown in figure 5.8. Because simulations show performance doesn't change that much, the same transformer was chosen to be used for both stages.

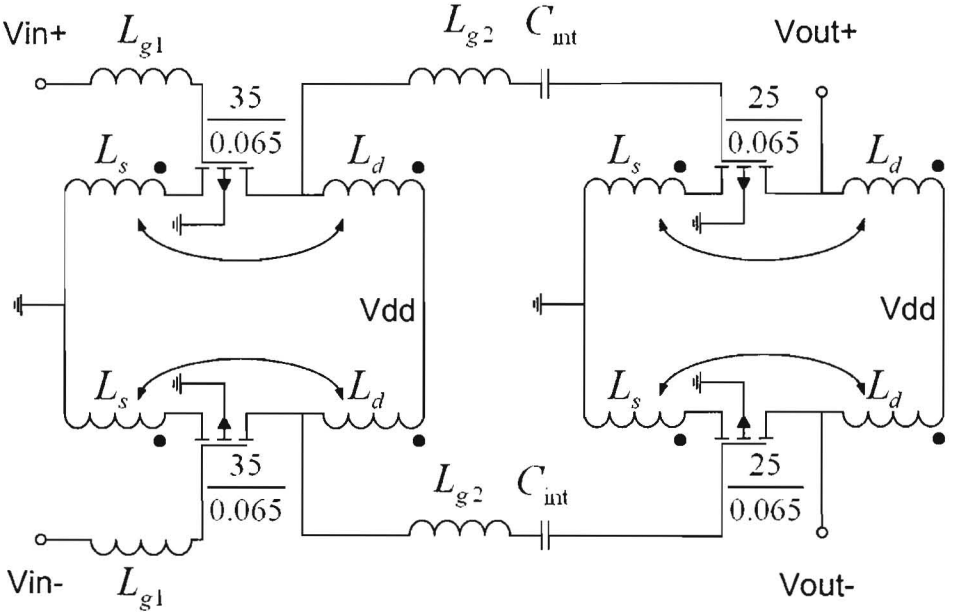


Figure 5.8: Two stage design.

5.3 Common mode

The LNA needs to behave fully differential. This means the common mode gain should be minimized. Therefore a certain common mode rejection needs to be included. Common mode signals arise from CM input signals and due to component mismatches. In figure 5.9 there are two branches indicated. Signal current flowing through these branches result in common mode signals at the output.

So to suppress common mode signals, the signal current flowing through these branches should be suppressed. This should be done in such a way the amplification of the differential

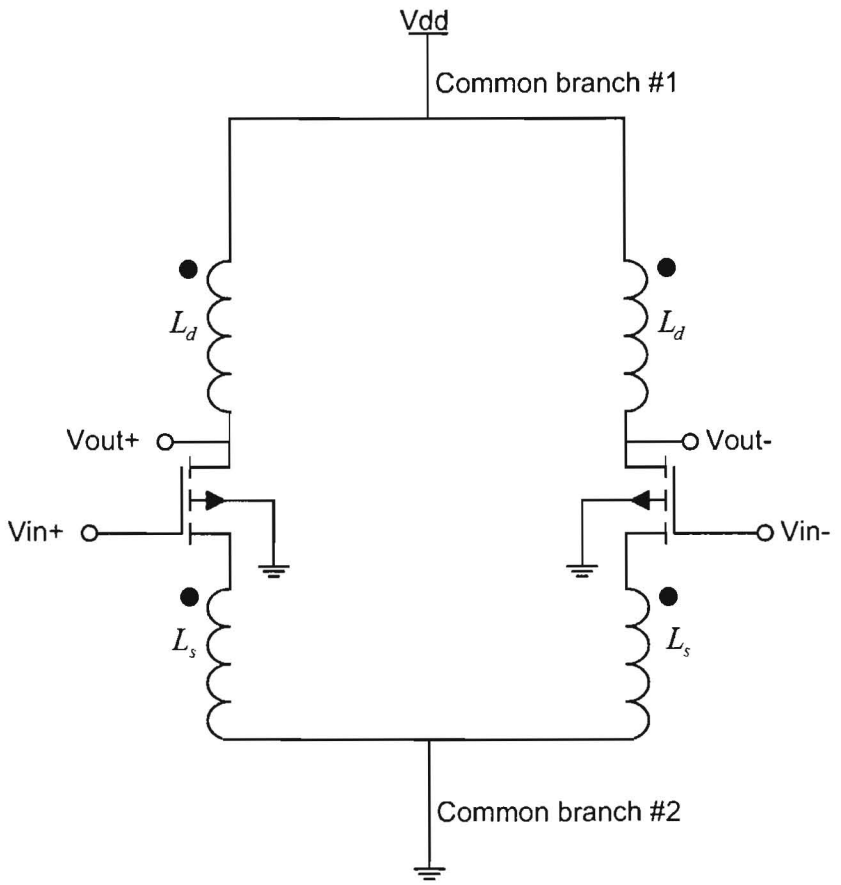


Figure 5.9: Common branches in the circuit.

signal is not deteriorated. There are several ways to do this. It should be noted the CM stability must be checked during this step.

5.3.1 Current source

First common mode rejection method investigated is the use of a current source to create a virtual ground (see figure 5.10). For differential signals the virtual ground node acts as a real ground. For common mode signals on the other hand, the virtual ground node acts as an infinite impedance, assuming an ideal current source.

This means no common mode signal current can flow through the LNA, so the common mode signal at the output is suppressed. The differential gain is the same as without the current source.

This common mode rejection method can be successful only when a current source can be created with a high output impedance. If the output impedance of the current source is too low, there will also be a common mode signal current flow through the current source. This results in a common mode signal on the output.

To create a current source, a transistor was used. The supply voltage of the complete circuit is 1.2 V. To get maximal performance, the voltage drop over the amplifier is approximately 750 - 800 mV. This leaves 400 - 450 mV for the current source V_{ds}. Because of this

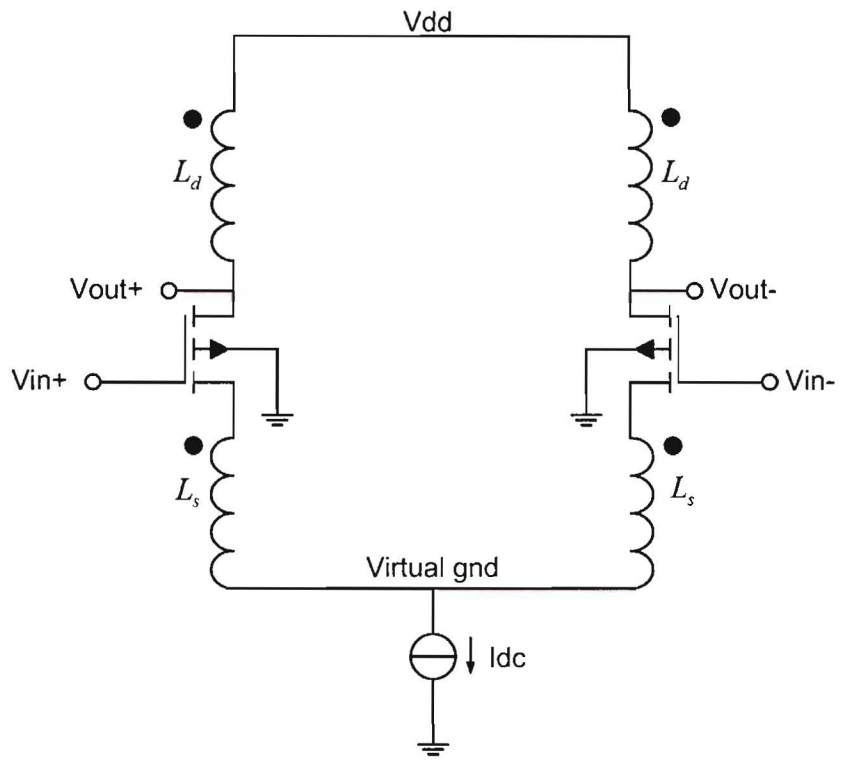


Figure 5.10: Current source added to create virtual ground.

low drain-source voltage, the current source has to be made very wide. Simulations show a current source width of approximately 370 μm in combination with a transistor in the amplifier of 35 μm. Because parasitics in the current source also scale with transistor width, these also become big. Simulations show a common mode rejection ratio using this method of approximately 2 dB per stage. Reason for this low CMRR is the low output impedance of the current source.

5.3.2 Current source with common mode feedback

To increase the output impedance of the current source, feedback can be used. The schematic of how to implement this is shown in figure 5.11. The two resistances R_1 and R_2 are connected to the gate of the current source. If these resistances are chosen to have equal values, the signal at the gate of the current source consists solely of the common mode signal present at the output. This way a common mode rejection is created for both CM input signals and CM signals arising at the output due to component mismatches.

These resistances should also be chosen in such a way, they do not load the differential output to much. Therefore the output impedance of the LNA should be $<< (R_1 + R_2)$. This is also were the bottleneck arises to implement this in the given technology at 60 GHz. At the input of the current source there is a big capacitance present. This in combination with the high impedance of the feedback resistances makes this trick unsuitable for this LNA.

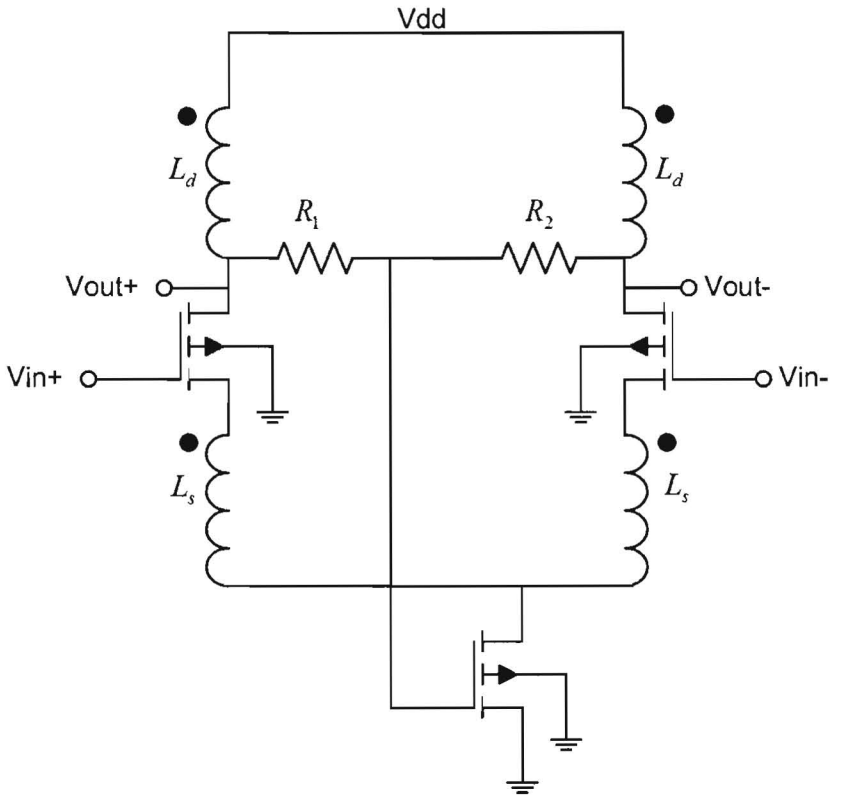


Figure 5.11: Current source with common mode feedback added.

5.3.3 Resistor

Because of the difficulty of achieving a high impedance using a current source, a simple resistor is considered as an alternative. Simulations were performed with a resistor at both branches of interest, located in figure 5.9. Simulations show adding a resistor at common branch # 2 gives little common mode rejection and lowers the input impedance causing it to become negative in some cases (leading to $K-$factor < 1, so possible instability). Most successful for achieving a high CMRR appeared to be a resistor at common branch # 1. Because of this resistor, the common mode equivalent circuit looks as follows:

The resistor in the equivalent circuit behaves as a resistor of double resistance. This is because in common mode, the current of two identical stages flows through the resistor. The difference of this common mode circuit in comparison to the differential mode circuit concerning gain, is the presence of the resistor in series with the drain inductance. This results in a low Q-factor of the load of the circuit. Because the gain of the voltage voltage transformer feedback topology is lowered by a low Q-factor of the load inductance, the common mode is suppressed. Simulations show a common mode rejection of > 5 dB per stage.

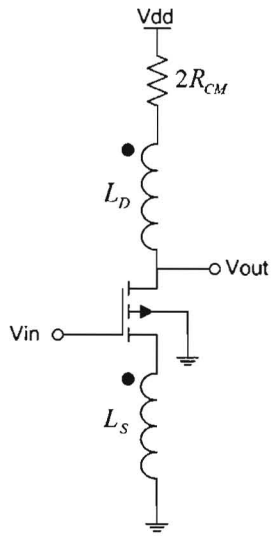


Figure 5.12: Common mode equivalent circuit.

Chapter 6

Impact of layout

To implement the design on chip, a layout has to be made. In the layout the components are physically being connected to each other. This cannot be created automatically, so it has to be done by hand. Many problems arise during this step.

The first problem encountered is the generation of many unavoidable effects, called parasitic effects. These effects can be modeled with capacitors, resistances and inductances between the various nodes. During the layout it is possible to do an RC-extraction using Cadence. This RC-extraction adds the main parasitic components to the design. Then a simulation can be done including all these components. If the performance is deteriorated too heavily, the layout should be improved.

This extraction method only gives values for parasitic capacitances and resistances, so no inductance. If also parasitic inductance extraction is needed, an EM-simulator such as ADS Momentum must be used. But because EM-simulations in Momentum take a lot of time, it is not wise to use it continuously. Inductive effects are only of interest for relative big components, such as the interconnects between the inductors. Therefore only EM-simulations are performed on such structures.

Another difficulty are the design rules that have to be obeyed during the layout. Design rules give the designer restrictions on for example the maximum and minimum allowable line width for the various metal layers. Therefore not every structure is possible to implement on chip. Another design rule is the maximum allowable DC-current density through the metal lines. High current means a wide line so high capacitance.

Also a problem is the absence of many "default" components. This means that if a component is wanted that's not present in the library, it has to be made by hand. This is valid for the transformers, some capacitors and the transmission lines used in the design. To model the behavior of these devices, ADS Momentum was used.

Design goal during the layout is to build the circuit in reality without deteriorating the performance to much. Therefore the distances used in the layout must be well below the (effective) wavelength. Because this design operates at 60 GHz, this is already a very short distance. The effective wavelength of these signals in this stack is only about 2.5 mm. This means the total RF-path in the LNA has to be minimized. So all components should be placed as short as possible to each other. This also gives rise to problems in the matching network. To be able to connect the LNA to the in and output bondpads, a certain distance has to be spanned. To model the effects present due to this, ADS Momentum has to be used.

Concluding it can be seen the layout is an important step in the design of the LNA.

Choices made in this step have big influence on the overall performance of the eventual amplifier. Therefore it is very important to look at different solutions and choose the best options.

6.1 MOST's

Because the dimensions in the layout of the transistors are very small, high parasitic capacitance can be created. These capacitances result in a lower f_t of the device. This can be prevented by choosing thin metal lines for the connections to drain, bulk, gate and source.

On the other hand, thin metal lines result in high resistances and low maximum DC current. The resistances result in bad noise performance (mainly due to the resistance in the gate) and also deteriorate the gain, and the low DC current sets a maximum on the biasing of the CMOS device. So during the layout of the transistors, there is a tradeoff between high f_t, low noise and maximum bias current.

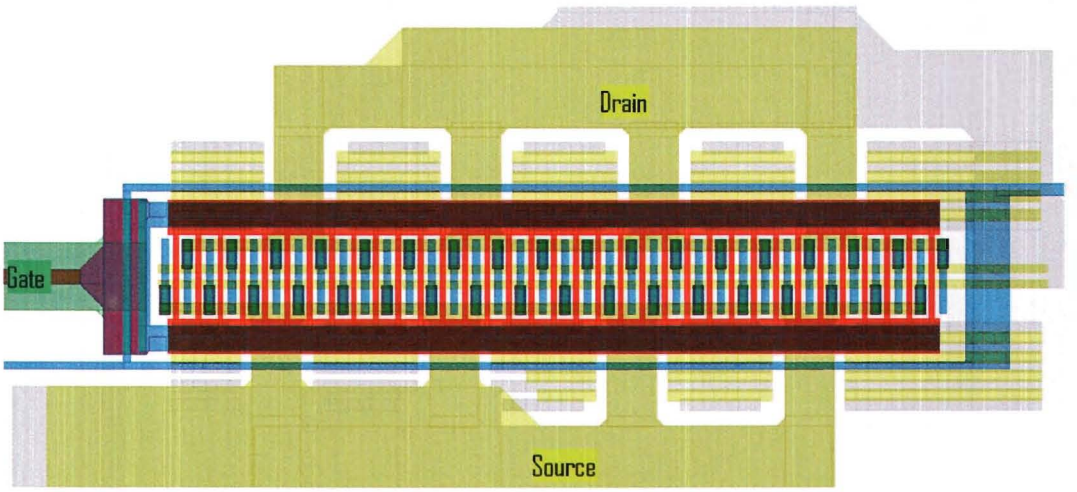


Figure 6.1: Transistor layout first stage (W = 35μm, L = 65nm, finger width = 1μm).

In figure 6.1 the layout of one transistor used in the first stage is shown. Using Cadence, it is possible to do an RC-extraction on the layout. This means an approximation of reality is made by including various parasitic resistances and capacitances in the transistor model due to the choices made in the layout. This way a very accurate model of the system is made after layout. To see any damage done by bad choices, simulations were done before and after layout. The layout of the transistor shown in figure 6.1 is optimized in such a way there is little difference between the performance with or without the extra effects obtained during RC-extraction.

To be able to have a DC-current through the transistor that is high enough for good performance, the connections to the drain and to the source have been made with a certain width and several metal layers in parallel.

The drain and source of the transistor are directly connected to the transformer. Therefore the distance between the transformer and the MOST is very small. In fact, the transistors lie exactly underneath the transformer. To prevent undesired effects due to coupling of the

transformer with the transistor, shielding has been placed between the transistor and the transformer. The shielding has been implemented using metal bars. Due to these metal lines, the electric field originating from the transformer is shortened above the transistor.

6.2 Transformer

To implement the transformer on chip, three metal layers are used. These layers are the two thickest copper layers for the drain inductor, and the aluminum layer on top for the source inductor. Because the DC-current of each transistor flows through L_d and L_s, both inductors have to meet a certain current density specification. This causes most problems for the source inductor. This is due to the low electro migration of aluminum. This, together with the demands from the previous sections, results in the chosen dimensions for the transformer. In figure 6.2 the transformer is shown (metal 1 is not shown).

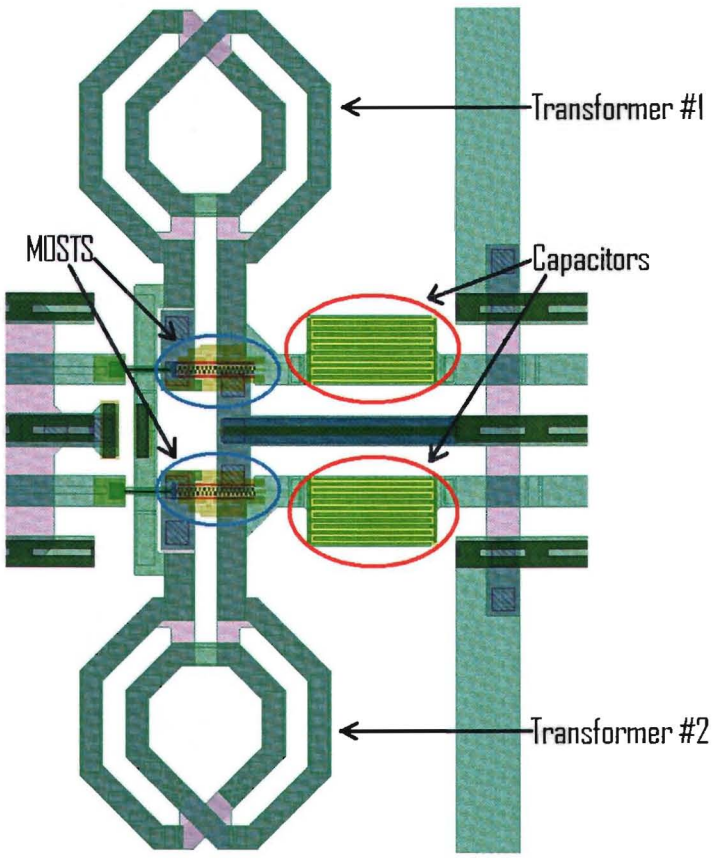


Figure 6.2: Transformer in the layout with underneath the transistors and the decoupling capacitors at the right.

As can be seen from this picture, the transistors are exactly underneath the transformers. This is to minimize the distance from the transistors to the transformers.

6.3 Coplanar wave guide

For interconnecting the two stages to each other and to the bondpads, coplanar wave guides (CPW's) are used. As a characteristic impedance 50 Ω is chosen, because the probes will be 50 Ω as well. The layout is shown in figure 6.3 using a current density plot.

Figure 6.3: Coplanar waveguide used in the layout.

To do simulations in Momentum, an approximation has been made by only including the top and bottom metal layers, because these are dominant for the behavior. Therefore a lower capacitance per unit length is expected in simulation than in reality, so a slight higher characteristic impedance. To describe the behavior of the T-line, the following model was used, which is valid for lengths shorter than $\approx \lambda_{eff}/20$ which is approximately 125 μm for 60 GHz in the stack used (see figure 6.4):

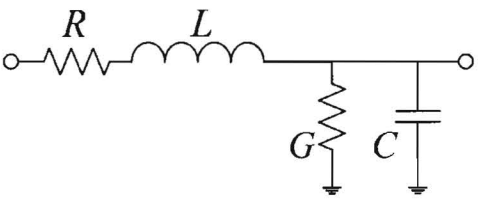


Figure 6.4: RLGC equivalent circuit of the CPW.

Using the telegrapher's equations the behavior can be described [5]. These are given in the appendix. To retrieve the information about the characteristic impedance and complex propagation constant from simulations and measurements, the **ABCD** matrix can be used (with d being the length of the transmission line). This matrix is given as follows for a transmission line:

$$\mathbf{ABCD} = \begin{bmatrix} \cosh\gamma d & Z_0 \sinh\gamma d \\ \frac{1}{Z_0}\sinh\gamma d & \cosh\gamma d \end{bmatrix}$$

$$\rightarrow Z_0 = \sqrt{\frac{B}{C}}$$

$$\rightarrow \gamma d = (\alpha + j\beta)d = \ln\left(A + Z_0 C\right)$$

$$\text{Loss} = \alpha = 4.343\left(\frac{R}{Z_0} + GZ_0\right) \text{ dB/unit length}$$

Simulation results show a Z_0 of 52.8 Ω and a loss of approximately 1.18 dB/mm at 60 GHz. The RLGC values are given below for the simulated CPW.

$$R = Re[Z_0 \cdot \gamma] \approx 12.6m\Omega/\mu m$$

$$L = \frac{Im[Z_0 \cdot \gamma]}{2\pi f} \approx 0.348pH/\mu m$$

$$G = Re\left[\frac{\gamma}{Z_0}\right] \approx 0.62\mu S/\mu m$$

$$C = Im\left[\frac{\gamma}{Z_0 \cdot 2\pi f}\right] \approx 0.13\text{fF}/\mu m$$

6.4 Shielding inductors and transformer

To prevent the EM field generated in the inductors and the transformer to penetrate the substrate, a shield will be used. The shield has to be implemented in such a way there is as little deterioration of the inductor performance as possible. To do so, the shield is implemented with a certain pattern. The shield is shown in figure 6.5 situated between the inductor and the substrate.

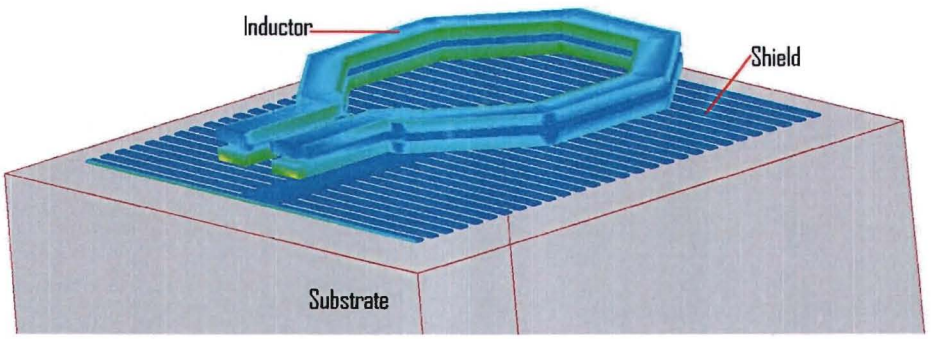


Figure 6.5: Inductor with patterned shield above the substrate.

Because of the horizontal lines there is almost no eddy current possible in the shield. Therefore the effect on the performance of the inductor is small. But because the EM field is shortened by the shield, there is little field penetrating the substrate. To see the effect of the shield on the inductor, simulations are performed using Momentum. The minimal line width of the used metal in the shield is 0.1μm. This is not possible for simulation in Momentum because of memory reasons. Therefore simulations were performed using line widths of 2μm, 1 μm and 0.7μm. The biggest effect on the performance of the inductor is observed in the Q-factor. The simulation results concerning the Q-factor are shown in figure 6.6.

As can be seen from this figure, the smaller the line width is chosen, the higher the Q-factor becomes. Also with increasing frequency, a smaller line width must be chosen to have the same relative difference in deterioration of the Q-factor. At 60 GHz the Q-factor without

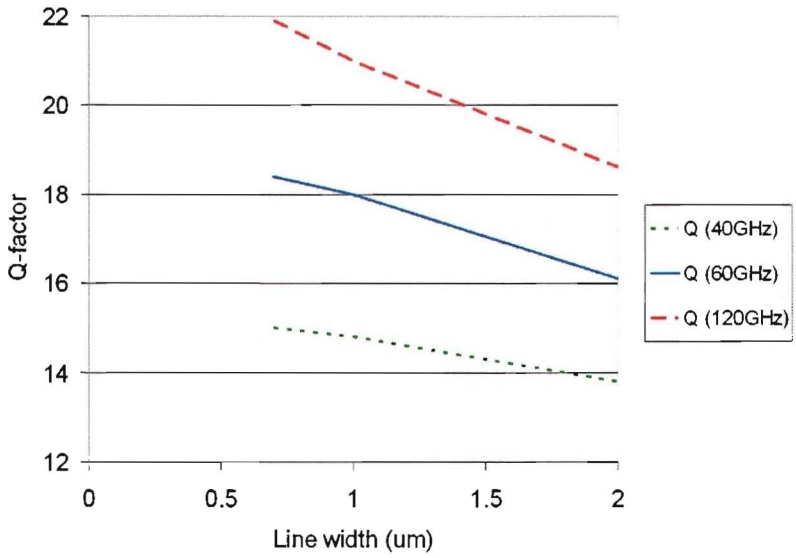


Figure 6.6: Q-factor for different frequencies versus line width.

shield is equal to 22. If the line in figure 6.6 is extrapolated to smaller line widths, it will not reach 22. So the shield will give some deterioration concerning the Q-factor, even when the minimal line width of 0.1 μm is chosen, but the effect will be small. Therefore the line width in the shield is chosen to be this minimal value.

Decided was to keep the shield floating to minimize the capacitance to ground. This will result in a higher resonance frequency.

6.5 Inductors

The LNA uses four inductors besides the transformers. Two from the bondpad to the input of the first stage, and two between the two stages. Because these components have a big size compared to the other components, they must be placed at a certain physical distance from the rest of the layout. Also the field generated in these components must be kept away from other components as much as possible to avoid undesired coupling. Therefore the inductors will have a shield as discussed in section 6.4 and the connections to the inductors will be made with coplanar wave guides as discussed in section 6.3. The used structure for the inductors is shown in figure 6.7.

Simulations in Momentum show a slight higher inductance due to the bends used to connect the inductor to the CPW. This effect has been taken into account during the design. The resulting Q-factors of the first and second stage inductors are respectively 15 and 13.

6.6 Capacitances

In the design two types of capacitors are used. One type to filter the power supply and bias voltages, and another type to provide a DC-decoupling between the first and second stage.

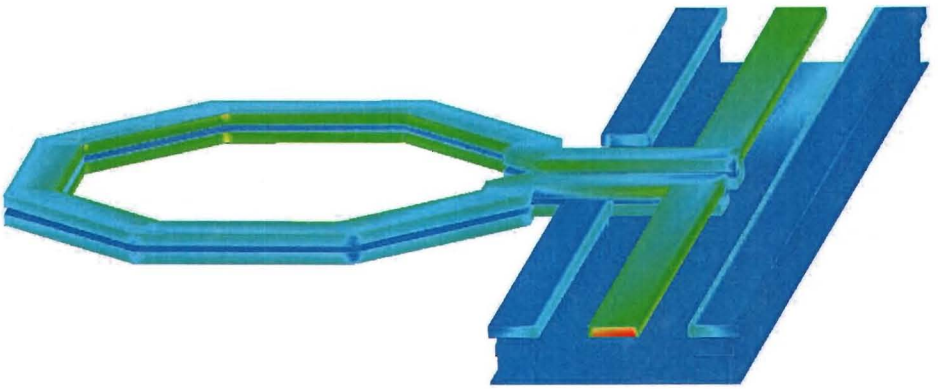


Figure 6.7: First stage inductor with CPW interconnect.

The capacitors used to filter the DC-voltages are fringe capacitors using every metal layer. These capacitors will have a certain capacitance to substrate, but this is not a problem because there is also a DC-voltage present, namely ground. In total there is 12 pF of capacitance to ground made by the capacitors to filter the power supply voltage. To filter the bias voltages there is approximately 2 pF per bias voltage in added capacitors. The layout is designed is such a way there is high capacitance between the DC-paths by making small distances between them.

The second capacitor type is used for DC-decoupling between the first and second stage and therefore transports the RF-signal. It is desirable in this capacitor to have a high capacitance value with a high Q and low capacitance to ground (substrate). Therefore only the three top copper metal layers have been used, so there is more distance between the capacitor and the substrate. A drawback of this approach is the fact that there will be less capacitance in this topology compared to the capacitors with all metal layers. A decoupling capacitance of approximately 120 fF was made this way. In figure 6.2 this capacitor is shown.

6.7 Resistors

For the common mode rejection, resistances will be used. These resistances must be able to transport the complete DC-current of the stage. Therefore a certain width has to be reached. Also important in designing the resistances is to keep the W/L ratio smaller than 1, to reach a reliable resistance value. In figure 6.8 the layout of a resistor is shown. The red areas indicate a resistor. On top and at the bottom there is a connection present.

To prevent a W/L ratio smaller than 1, the resistor has been divided in several parallel resistors of higher value. Next to the middle four resistances, two dummy resistances are placed. This is also to increase the reliability, because the resistances at the far left or far right are usually worse.

Another resistor is used in the biasing of the transistors. These resistances must be quite large to avoid loading of the input. Resistance values of approximately 40 kΩ are chosen for this. To obtain such a high resistance value, an extra layer in the layout is needed.

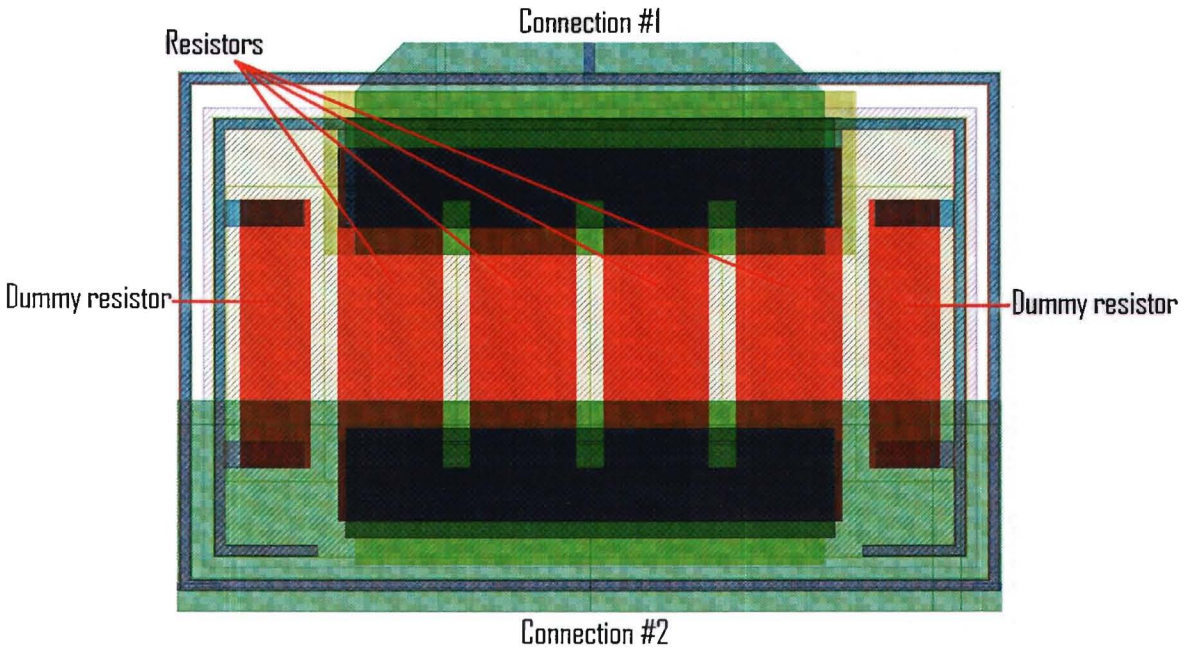


Figure 6.8: Layout CMR resistor.

6.8 Total layout

After putting all components together the total layout is formed. This is shown in figures 6.9, 6.10 and 6.11. The left bondpad is the differential input, the right bondpad is the differential output (both GSGSG). Both signal bondpads have an ESD diode included to prevent damaging by static discharge. To get the in and output signals to the bondpads, the coplanar wave guides are used. The two stages are build around this CPW.

The top and bottom bondpads are GPPG pads and are power supply and bias voltages respectively. To provide low ohmic connections from the bondpads to the circuit, wide metal lines are used and the DC lines are situated on top of each other to increase capacitance between them.

To shift the reference planes for the measurements, de-embedding structures have been included. These are open, short and load. After de-embedding the reference planes are shifted to the input of the inductor, and the output of the second stage. This way there is a possibility to measure the performance of the LNA solely, without the bondpads.

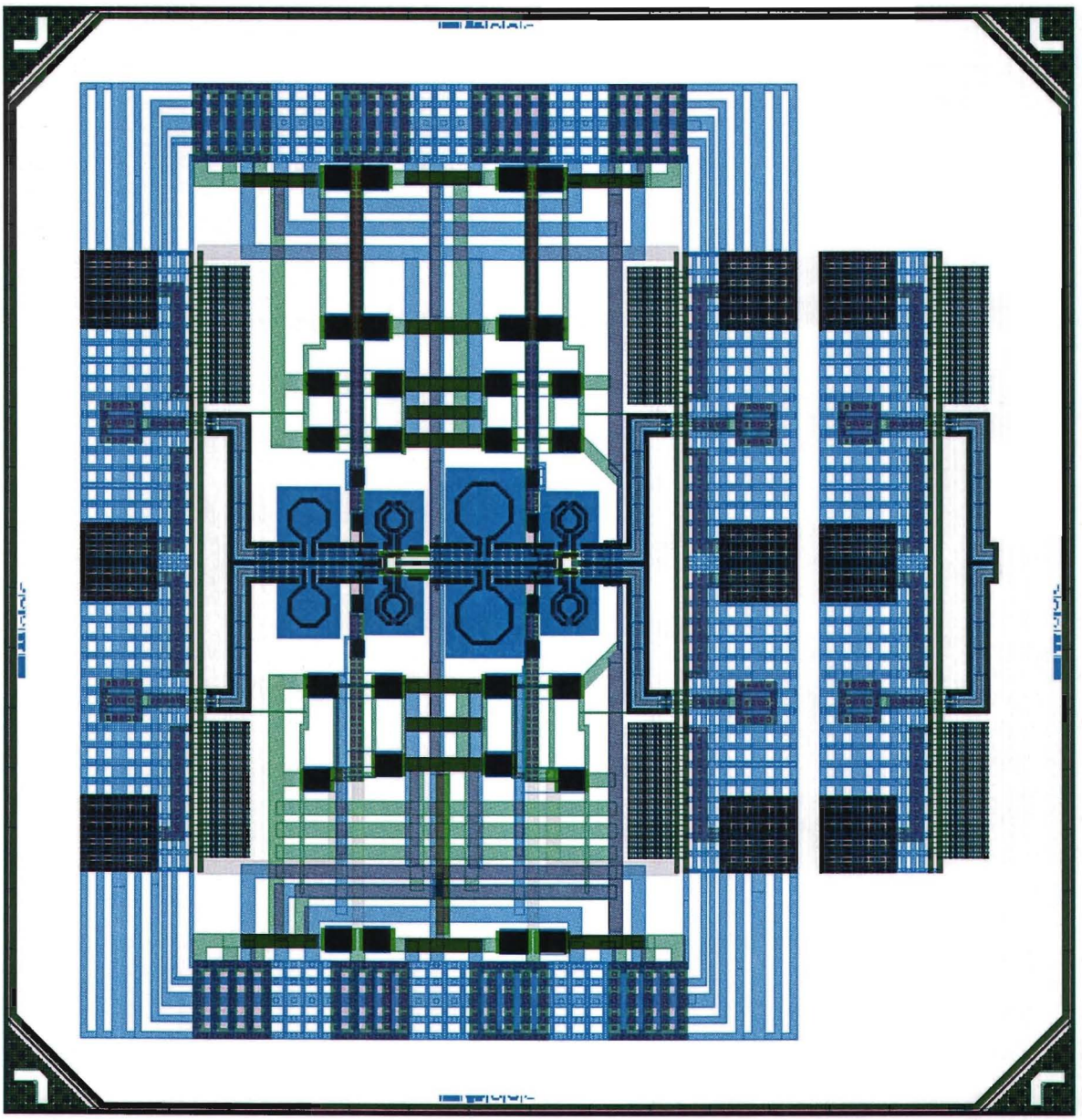


Figure 6.9: Complete layout voltage voltage transformer feedback LNA (left) and one de-embedding structure (short, right).

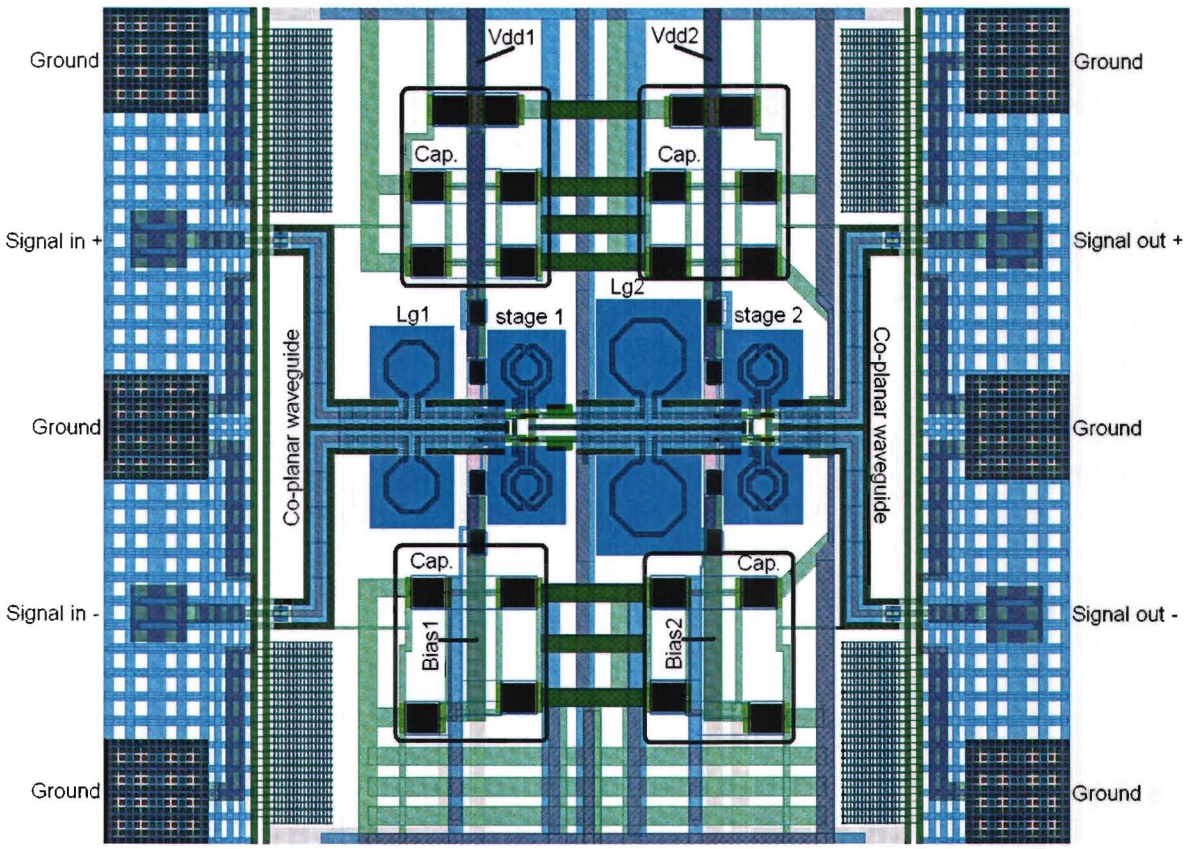


Figure 6.10: The complete LNA. At the left the differential input can be seen and on the right the differential output, both using CPWs. To provide low ohmic connections from the power supply bondpads to the circuit, wide metal lines are used and the DC lines are situated on top of each other to increase capacitance between them. DC capacitances are used (indicated by the black squares) to filter the supply and bias voltages at the indicated positions. The squares underneath the inductors are the shields. From left to right can be seen: The first gate inductances, stage 1, the second gate inductances and stage 2.

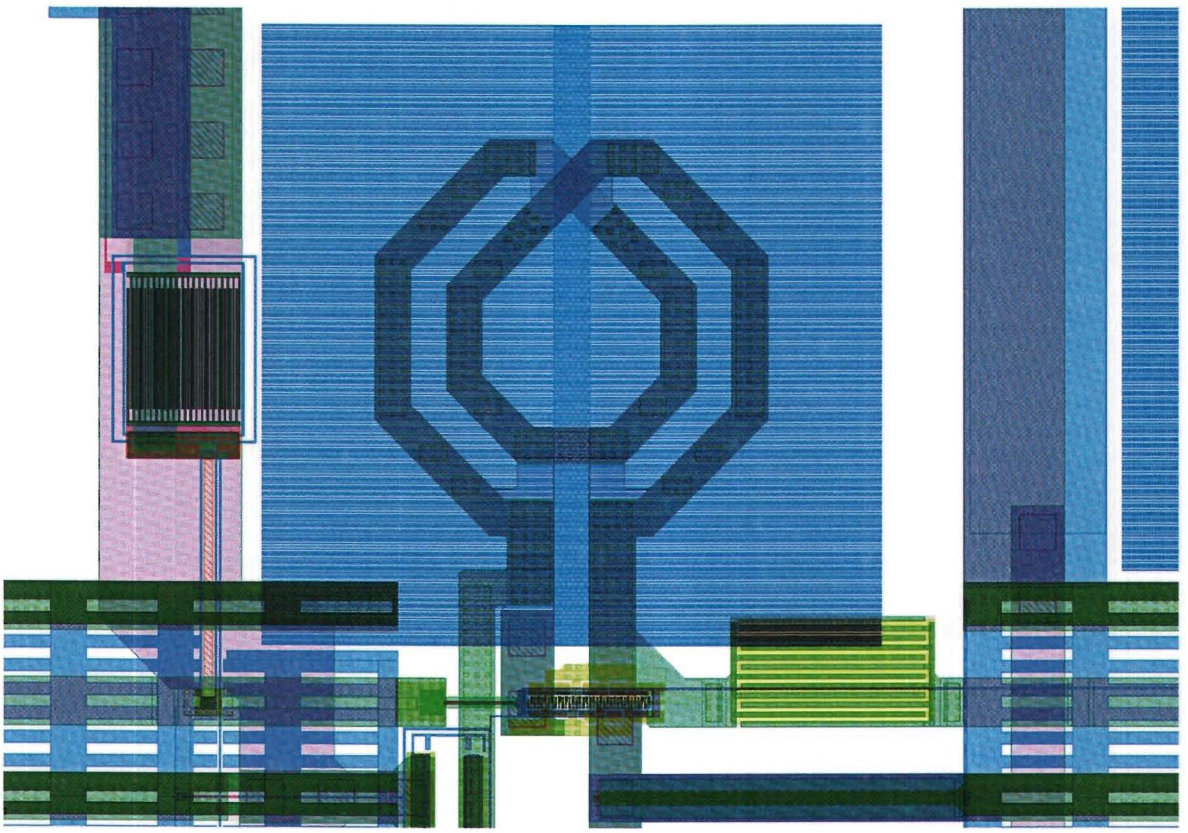


Figure 6.11: Close-up first stage.

Chapter 7

Simulations

During the complete layout traject, simulations were performed to see whether the performance is deteriorated by choices made in the layout. Goal during this stage was to obtain approximately the same performance of the circuit after the layout. It was seen the performance did not change very much, but the gain became a little less, and the NF increased a little bit. In this section the simulated performance after layout will be presented.

7.1 Noise figure and Gain

The main parameters for the LNA are noise figure and the gain. These parameters are quite sensitive to the variation of the Q-factors of the inductors used. Simulations performed in Momentum showed Q-factors around 14 for the gate inductors. Therefore these values were used during simulations in Cadence. In figure 7.1 the gain and noise figure is shown over the frequency band of interest. As can be seen from this figure, the gain flatness of 0.5 dB over the entire bandwidth has been achieved. The gain is approximately equal to 10.6 dB and the noise figure is 3.8 dB at maximum.

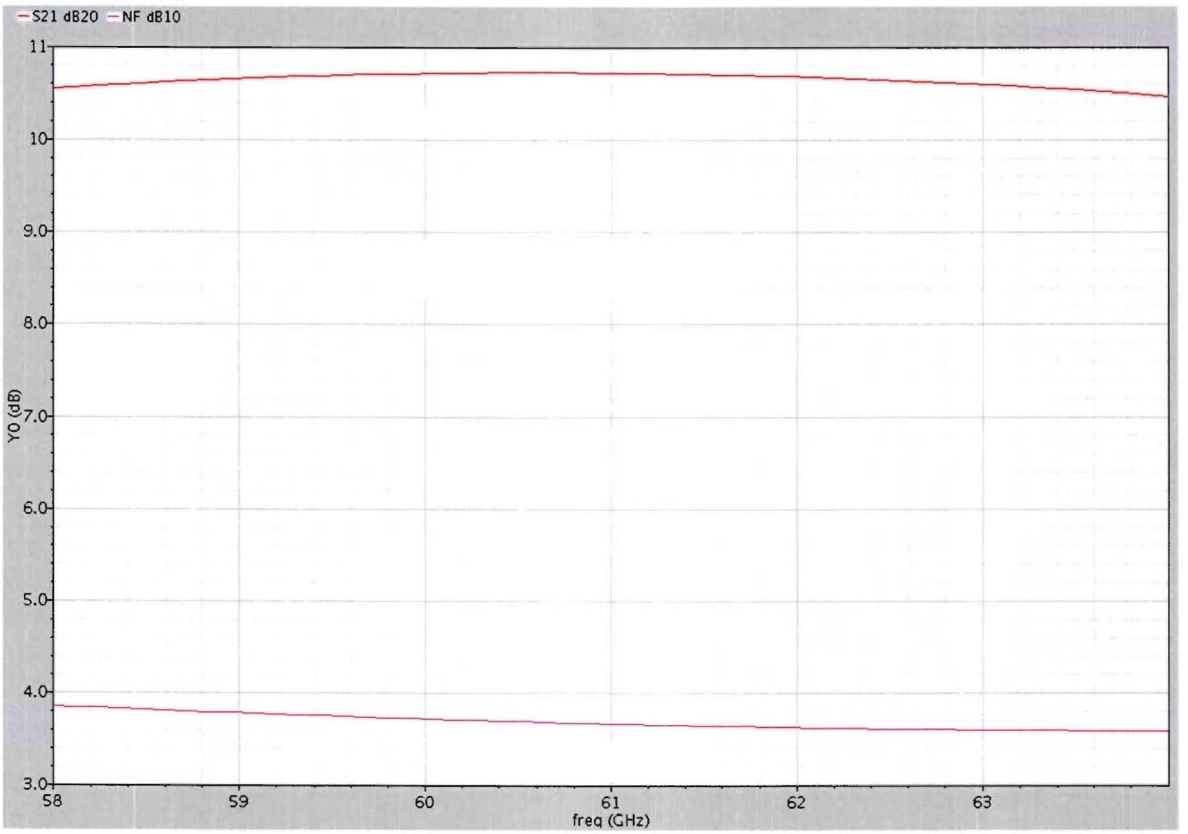


Figure 7.1: NF and s_{21} performance over the bandwidth of interest.

If the bias voltage of the first stage is varied, the performance of the LNA changes as shown in figure 7.2. As can be seen there is an optimum at $V_{bias_1} \approx 0.82$ V.

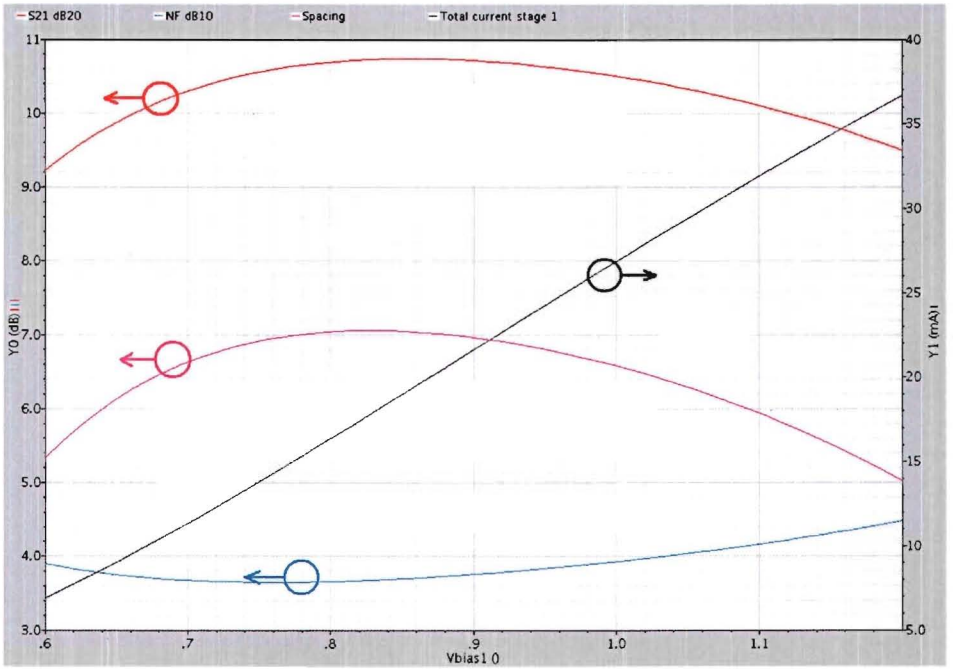


Figure 7.2: NF and s_{21} performance over variation of V_{bias_1}.

The variation of the bias voltage of the second stage leads to the following NF and s_{21} variation (figure 7.3). As can be seen the variation of the noise figure is most dominant as a function of V_{bias_1}, as expected according to Friis equation. The optimal value of V_{bias_2} is approximately equal to 0.8 V.

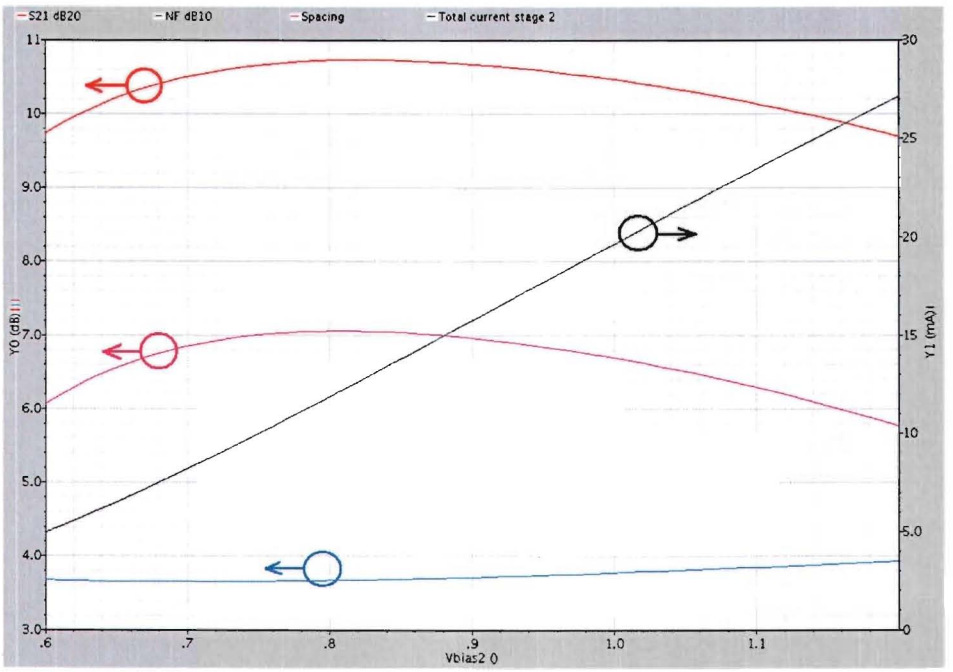


Figure 7.3: NF and s_{21} performance over variation of V_{bias_2}.

Next the variation of s_{21} and the NF is simulated as a function of Z_{src}. The imaginary part is equal to 0 using the gate inductor, so a purely resistive source results. The variation is given in figure 7.4. As can be seen there is an optimum concerning both gain and NF, and they are not equal to each other. In reality the input impedance is set to a certain value, so there is a trade-off. But as can be seen the variation is not that critical. During simulations a source impedance of 30 Ω is chosen.

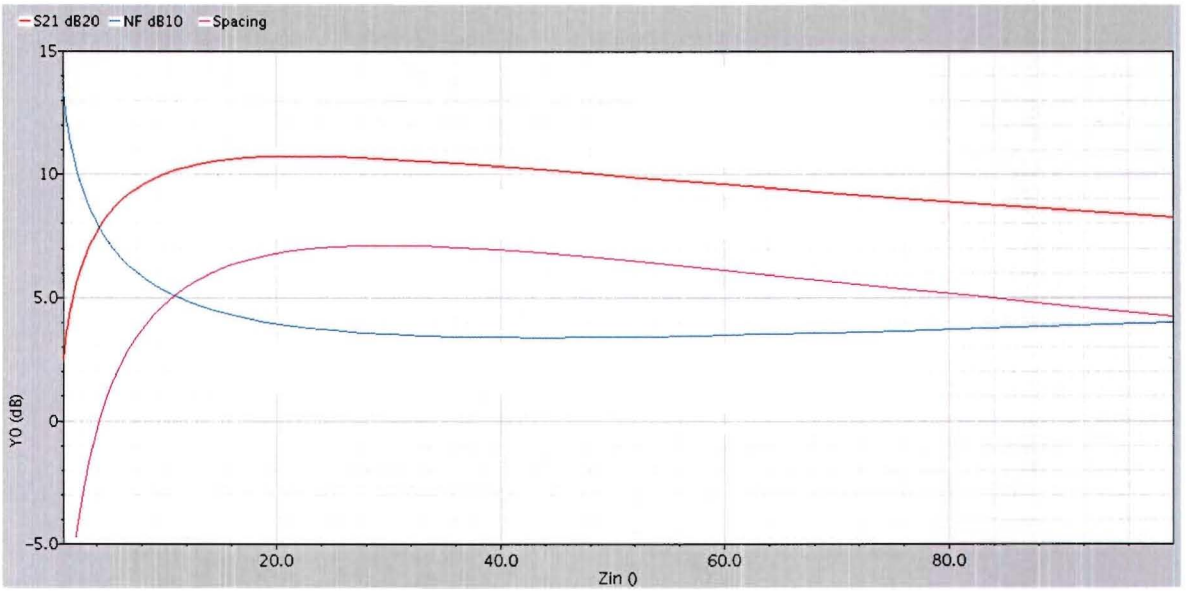


Figure 7.4: NF and s_{21} performance over Z_{src} variation.

7.2 IP_3 and 1 dB_c

To investigate the linearity of the LNA, the IP_3 and 1 dB_c gain have been simulated. The results are shown in figures 7.5 and 7.6.

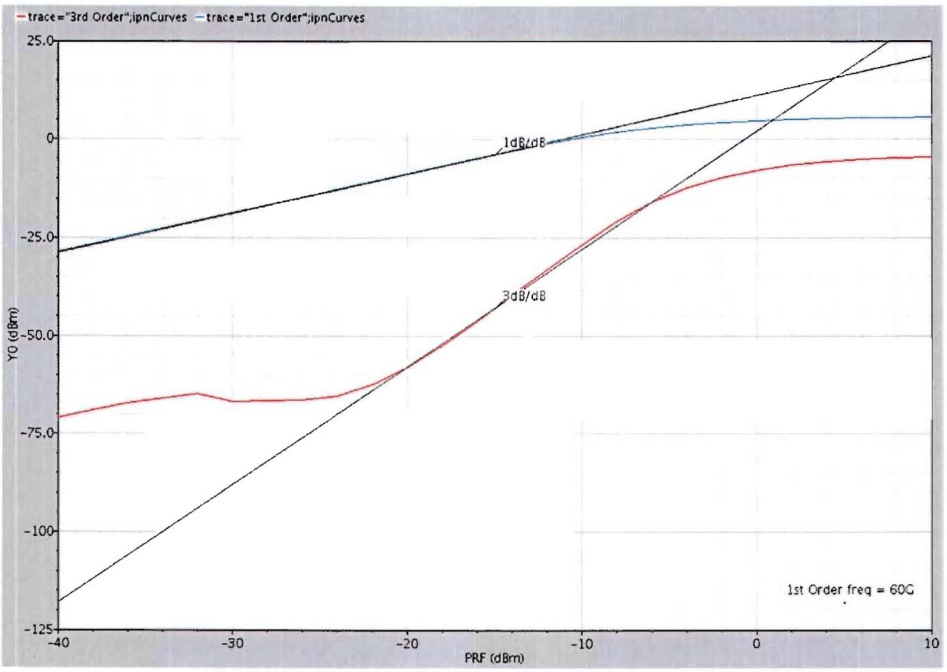


Figure 7.5: IP_3 simulation. $IIP_3 \approx 4$ dBm.

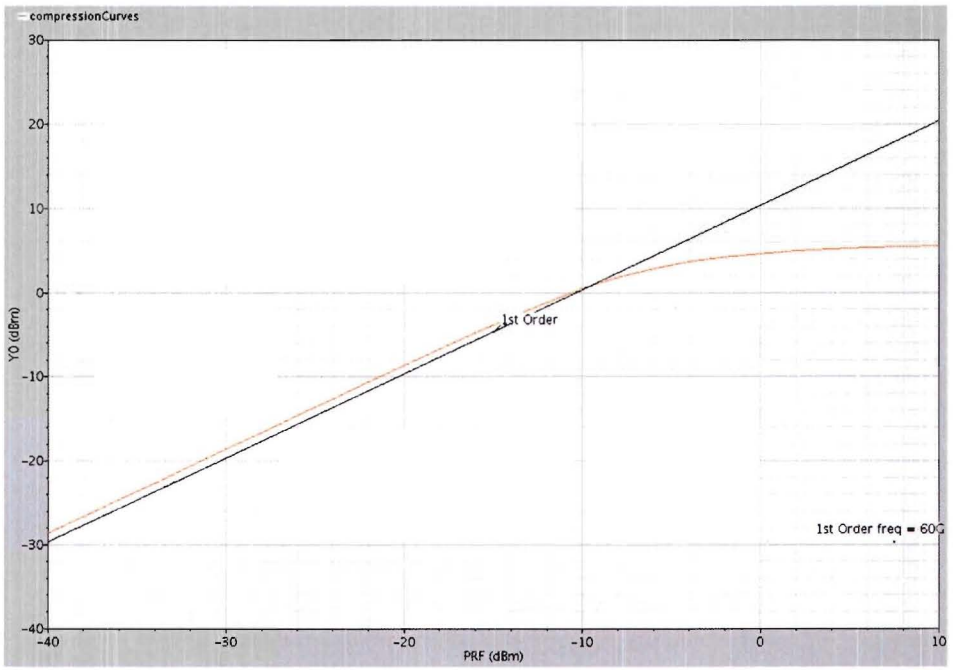


Figure 7.6: Output power versus input power. 1 $dB_c \approx$ -9.8 dBm.

7.3 S-parameters

The simulated s-parameters are shown in figure 7.7.

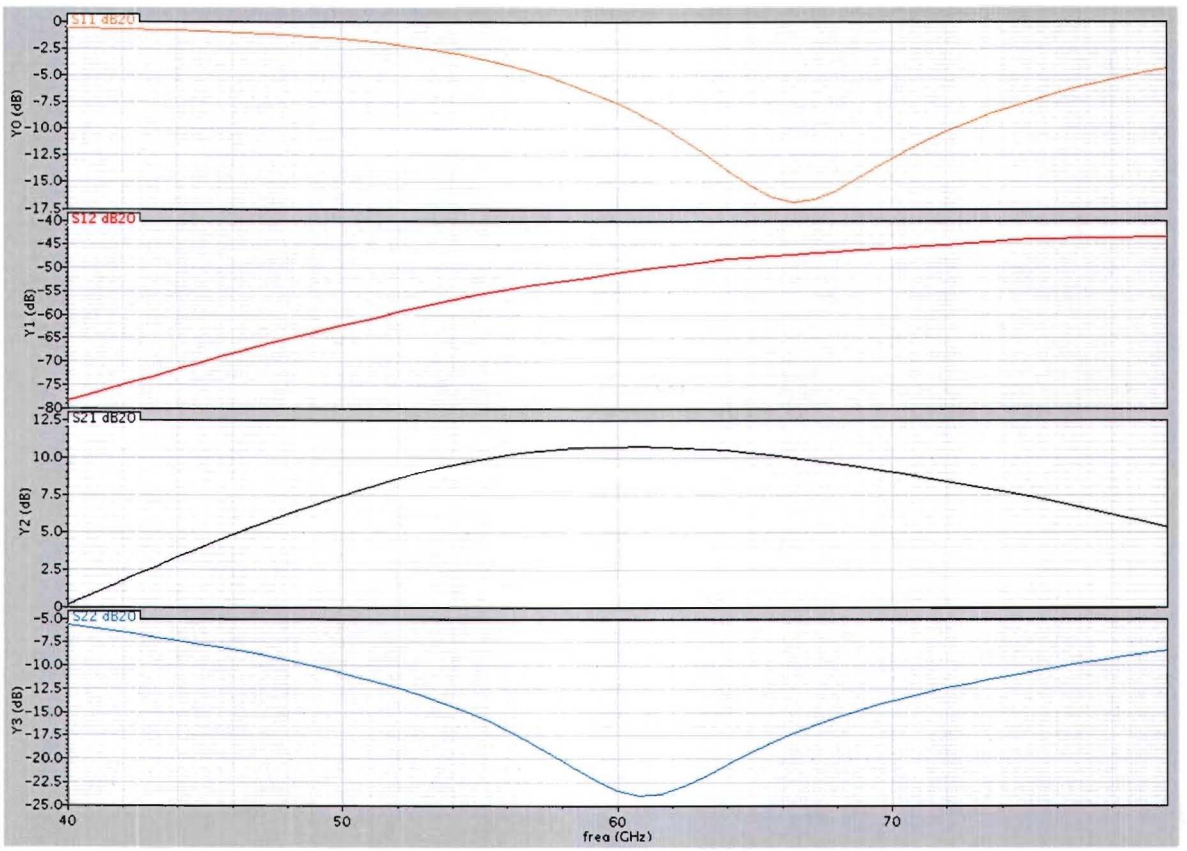


Figure 7.7: Simulated s-parameters.

The s_{11}-parameter indicates the absorbed power generated from the source to LNA. As can be seen the input match has been set to a higher frequency. This has been done because this way the gain in the operating bandwidth remains flat. At minimum the s_{11} is approximately -17 dB.

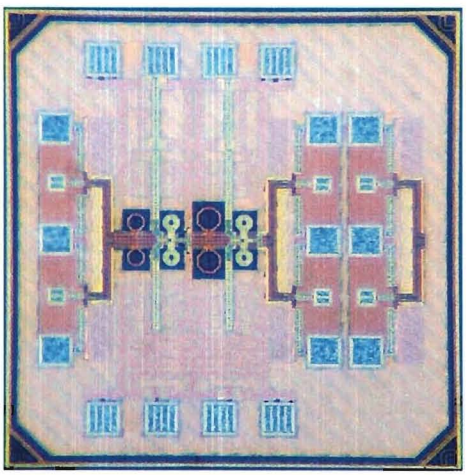
The s_{22}-parameter indicates the absorbed power from the LNA to the output. This is matched to the center frequency located at 61 GHz and has a minimal value of approximately -23 dB and stays under -20 dB in the operating bandwidth.

The s_{12}-parameter indicates the signal flow from output to input. It stays below -40 dB over the simulated bandwidth. This low value is obtained using the output isolation trick discussed in section 2.5.1.

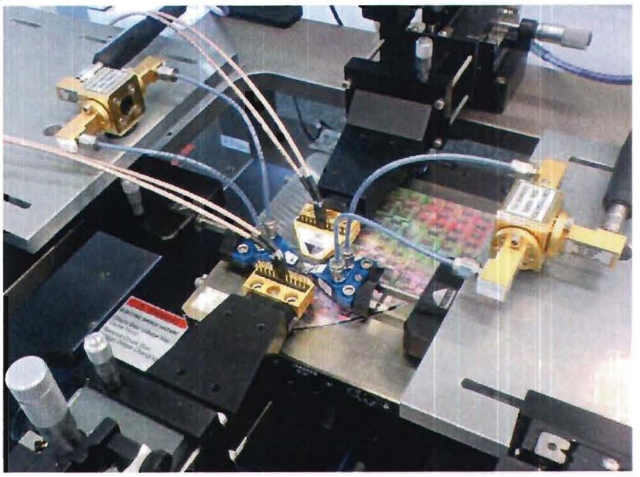
Chapter 8

Measurement results

In this chapter the measurement results of the 60 GHz fully differential LNA are presented. Four different measurements have been performed, namely a DC measurement including power consumption, S-parameters (common and differential mode), the noise figure and large signal measurements.



(a) Chip microphotograph of the LNA.



(b) Measurement setup.

Figure 8.1: Pictures.

8.1 DC measurement and power consumption at constant biasing

The measured current consumption of the LNA is given in figure 8.2. As can be seen the measured values show a small deviation from the simulated results. The total power consumption at both biasing voltages equal to 0.82 V is 17.3 mA + 12.5 mA = 29.8 mA. The supply voltage has been set to 1.2 V resulting in a total power consumption of **35.8 mW** at this biasing setting.

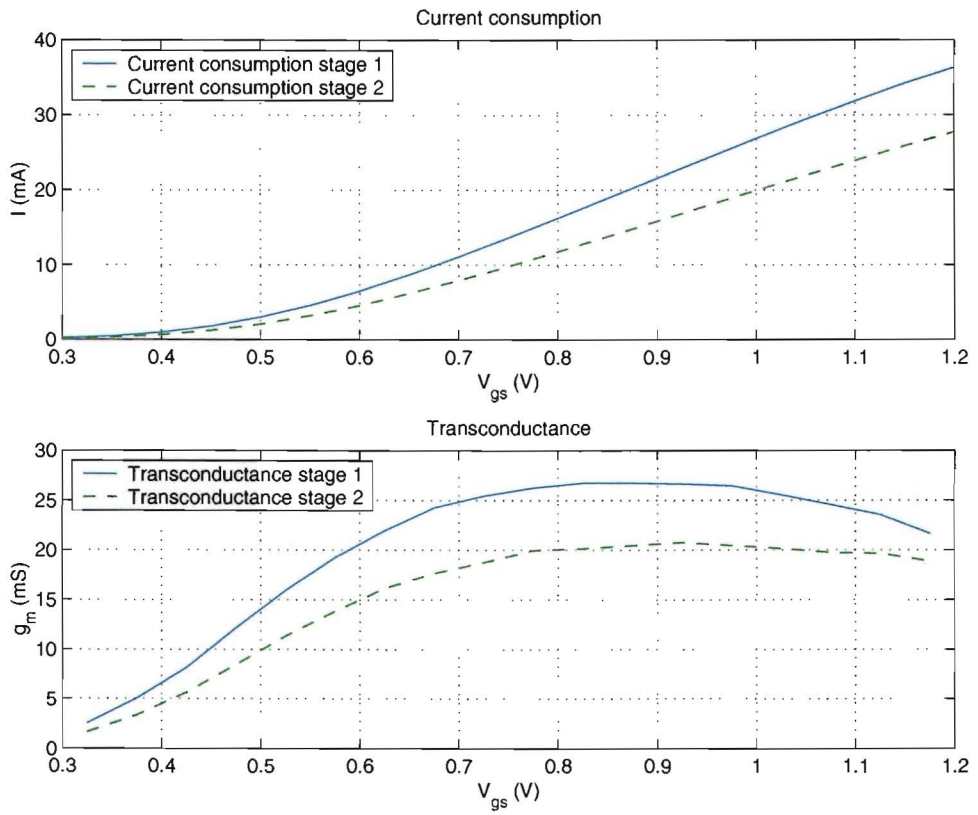


Figure 8.2: Current consumption of the first and second stage of the LNA as a function of the gate-source voltage V_{gs}. The derivative of the current consumption has been determined to evaluate the transconductance of the MOSFETs, which is shown in the lower graph.

During the measurements of the S-parameters and noise figure values for V_{gs_1} of 0.7 and 0.82 Volt were used and values for V_{gs_2} of 0.75 and 0.82 Volt were used. The simulated current consumption at these biasing levels is compared against the measured values and listed in the table below:

V_{bias}	*Simulated* I_{bias}	*Measured* I_{bias}	*Difference*
$V_{gs_1} = 0.7$	11.2 mA	11 mA	2 %
$V_{gs_1} = 0.82$	18.5 mA	17.3 mA	7 %
$V_{gs_2} = 0.75$	10 mA	9.8 mA	2 %
$V_{gs_2} = 0.82$	13.5 mA	12.5 mA	8 %

It can be seen the bias current shows small deviation from the simulated results for low bias voltage levels, but the difference increases when the bias level is increased.

8.2 S-Parameters

To measure important characteristics such as input impedance, output impedance, transducer gain and available gain of the LNA the S-parameters have also been measured. This has been done both for differential and common mode excitation.

To measure the S-parameters the measurement setup shown in figure 8.3 has been used. The Magic-T's (waveguide baluns) provide the translation from a single ended excitation to a differential excitation, if connected correctly. They can also be connected to provide a common mode excitation. To be able to measure the S-parameters of the LNA, the influences of the cables in combination with the Magic-T's and probes will be removed from the measurement using a calibrated sequence. The effects of the bondpad, ESD diode and transmission line on the measurements will be removed afterwards using a de-embedding procedure.

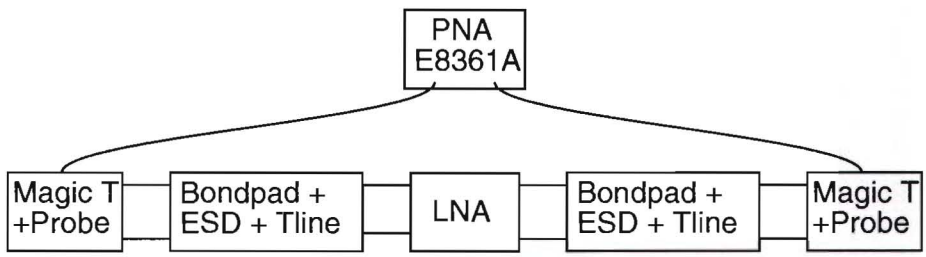


Figure 8.3: Measurement setup to measure S-parameters.

8.2.1 De-embedding structures

To de-embed the effects of the bondpad connection with the ESD diode and the transmission line an open short combination is often used. This is actually not possible at high frequencies because the model used during this de-embedding procedure is not valid anymore because of the decreasing wavelength. Therefore a load structure was added, which enables the extraction of the full S-parameter matrix of the structure to be removed from the measurement. The measurement results of these structures is shown in figure 8.4.

Using these measurements the S-parameters of the line can be calculated. The input reflection coefficient Γ_{in} as a function of the S-parameters of the line is given below [5]:

$$\Gamma_{in} = S_{11} + \frac{S_{21}S_{12}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{8.1}$$

If we assume $S_{21} = S_{12}$, which is a valid assumption for a passive network, the equation becomes:

$$\Gamma_{in} = S_{11} + \frac{S_{21}^2\Gamma_L}{1 - S_{22}\Gamma_L} = S_{11} + \frac{S_{12}^2\Gamma_L}{1 - S_{22}\Gamma_L} \tag{8.2}$$

This formula in combination with the knowledge Γ_L is equal to the values listed in the table below, gives three equations with three unknown values.

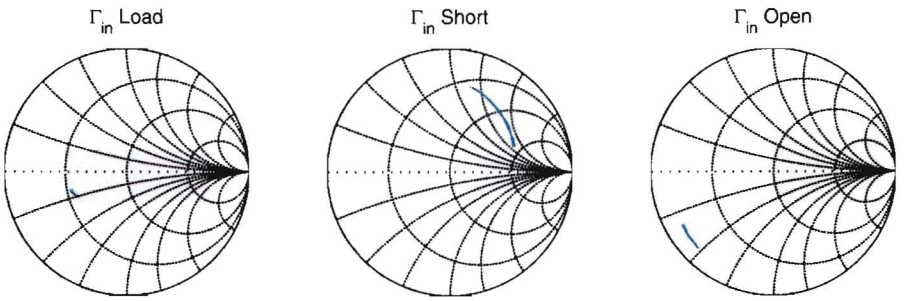


Figure 8.4: Input reflection coefficients of the de-embedding structures load, short and open.

Structure	Γ_L
Load	0
Short	-1
Open	1

If these equations are solved, the following S-parameters for the bondpad with the ESD diode and transmission line result (figure 8.5).

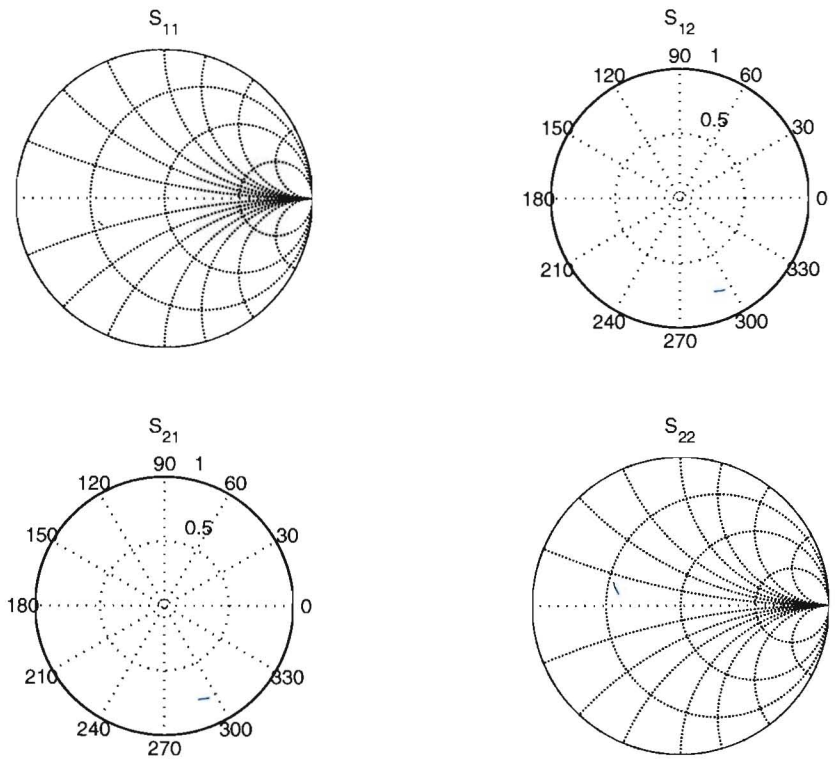


Figure 8.5: Resulting S-parameters of the bondpad with the ESD diode and transmission line.

The de-embedding procedure that has to be used now looks as follows:

- Calculate the T-matrix using the S-matrix of both the structure to be de-embedded and the measurement data [5]:

$$\mathbf{T} = \begin{bmatrix} \frac{1}{S_{21}} & -\frac{S_{22}}{S_{21}} \\ \frac{S_{11}}{S_{21}} & S_{12} - \frac{S_{11}S_{22}}{S_{21}} \end{bmatrix}$$

- Calculate the T-matrix of the LNA using the following equation: $T_{LNA} = T_{struct}^{-1} T_{raw} T_{struct}^{-1}$
- Calculate the S-matrix of the LNA using the following equation [5]:

$$\mathbf{S} = \begin{bmatrix} \frac{T_{21}}{T_{11}} & T_{22} - \frac{T_{21}T_{12}}{T_{11}} \\ \frac{1}{T_{11}} & -\frac{T_{12}}{T_{11}} \end{bmatrix}$$

8.2.2 Differential mode response

In figure 8.6 the differential S-parameters of the LNA are shown (after de-embedding). Because the port impedances are not equal to 100 Ω, S_{21} is actually equal to the transducer gain G_t with $Z_{src} = 30\Omega$ and $Z_{load} = 100\Omega$ with a shunt capacitance of 30 fF.

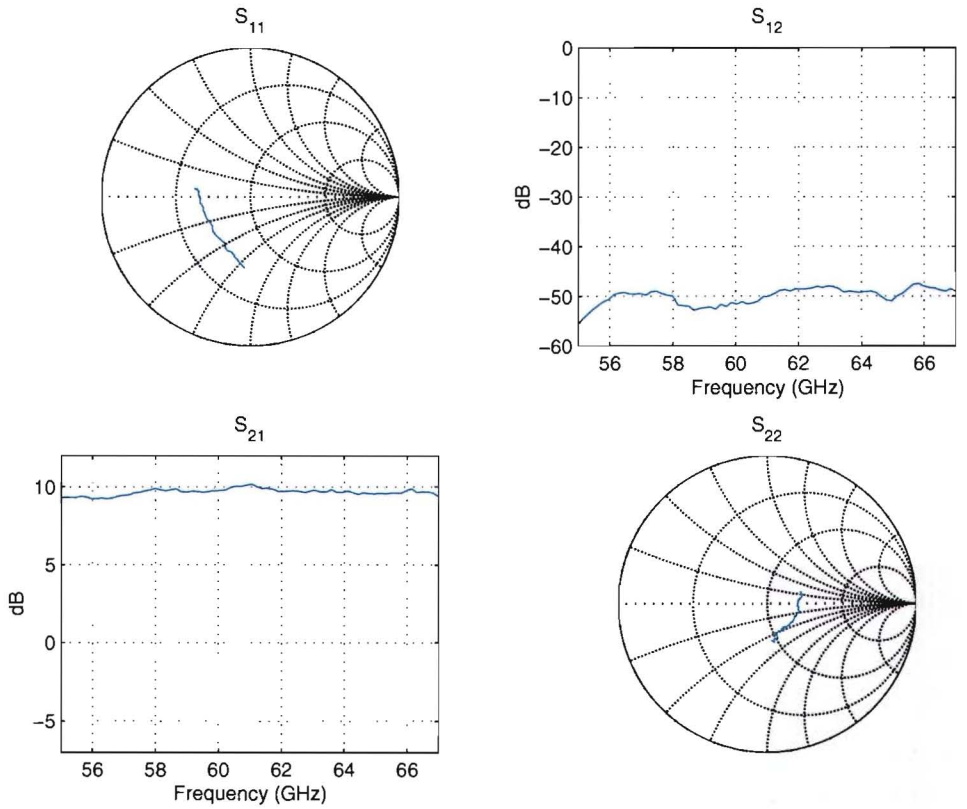


Figure 8.6: Measured S-parameters with $Z_{src} = 30\Omega$ and $Z_{load} = 100\Omega$ with a shunt capacitance of 30 fF.

$$G_t = \frac{1 - |\Gamma_s|^2}{|1 - \Gamma_s \Gamma_{in}|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - \Gamma_L S_{22}|^2} \tag{8.3}$$

It can be seen G_t **is approximately equal to 10 dB at 61 GHz** (maximum value). In the band from 58-64 GHz a **gain deviation of approximately ± 0.25 dB has been measured**. To see the G_t deviation as a function of the source impedance, Γ_s has been varied over the range which corresponds to source impedances of 1-100 Ω. The result is shown in figure 8.7.

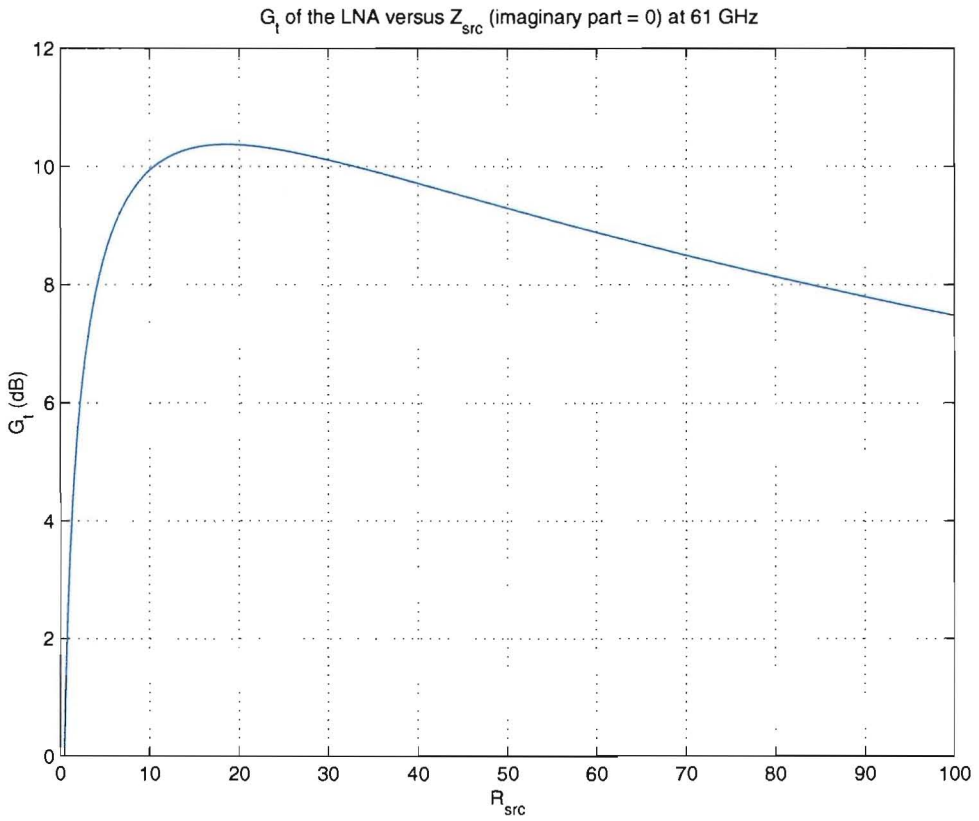


Figure 8.7: Measured transducer gain G_t at 61 GHz as a function of Z_{src}. Z_{load} has again been set to 100Ω with a shunt capacitance of 30 fF.

It can be seen the maximum gain is achieved for a source impedance equal to approximately 20 Ω, the same value as has been observed in simulations. It is also seen the gain variation is not very sensitive to variations in source resistance.

Next the group delay has been calculated from the measurement results of the LNA. This is shown in figure 8.8. The group delay has been calculated as follows:

$$\text{Group delay} = -\frac{\partial\theta}{\partial\omega} \tag{8.7}$$

In which θ is equal to the phase of the S_{21}-parameter.

The average value of the group delay is equal to ≈ 20 ps. It can be seen it stays approximately constant over the entire frequency range[1].

[1]The variation is mainly due to measurement inaccuracy

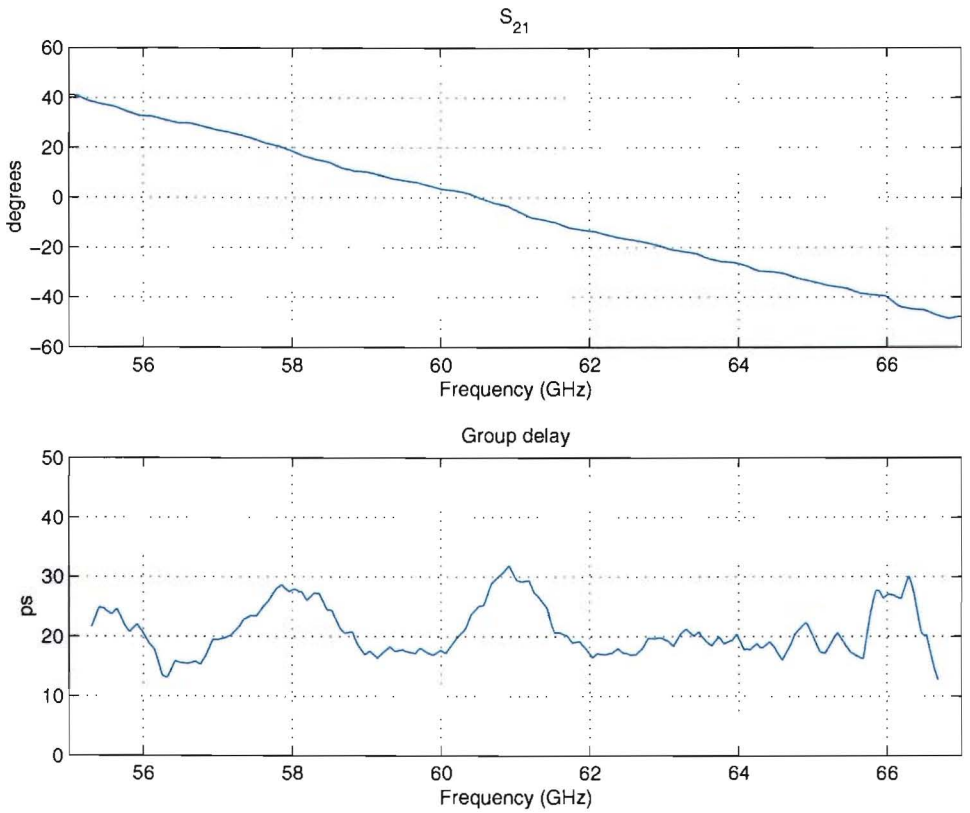


Figure 8.8: Measured group delay.

Lastly the K-factor is given of the LNA in differential mode. The K-factor is defined as follows:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2}{2|S_{12}S_{21}|} \tag{8.8}$$

In which

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{8.9}$$

If the K-factor is greater than one and $|\Delta|$ is smaller than one, the amplifier is unconditionally stable [5]. Because S_{11} and S_{22} are both < 1 and $|S_{12}| << |S_{21}|$, Δ also is smaller than one. The K-factor is plotted in the following figure:

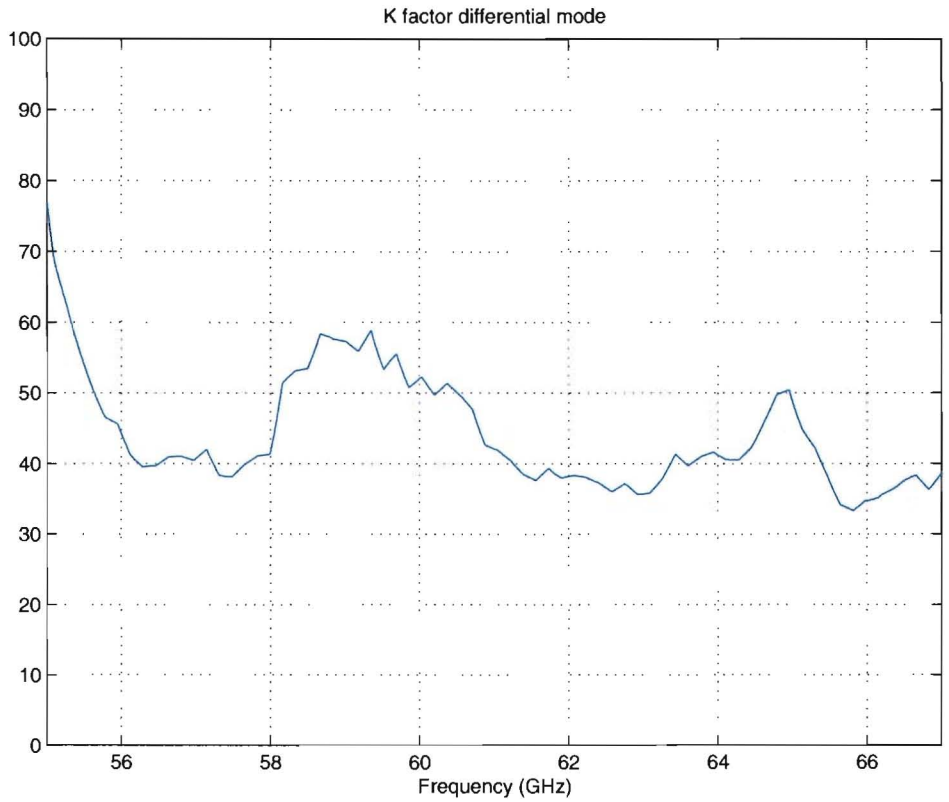


Figure 8.9: K-factor in differential mode

As can be seen the K-factor is $>> 1$ in the complete band measured, resulting in unconditional stability for differential mode signals.

8.2.3 Common mode response

To measure the common mode response the baluns are connected in such a way they provide common mode signals at in and output. The resulting S-parameters after de-embedding are shown in figure 8.10. Again the S_{21} parameter actually represents the transducer gain for the same reasons as already discussed in the previous section. It can be seen the transducer gain in common mode is equal to approximately -2 dB, resulting in a **common mode rejection of**

approximately 12 dB. Although this value is not very high, it does come in close agreement with the simulated value.

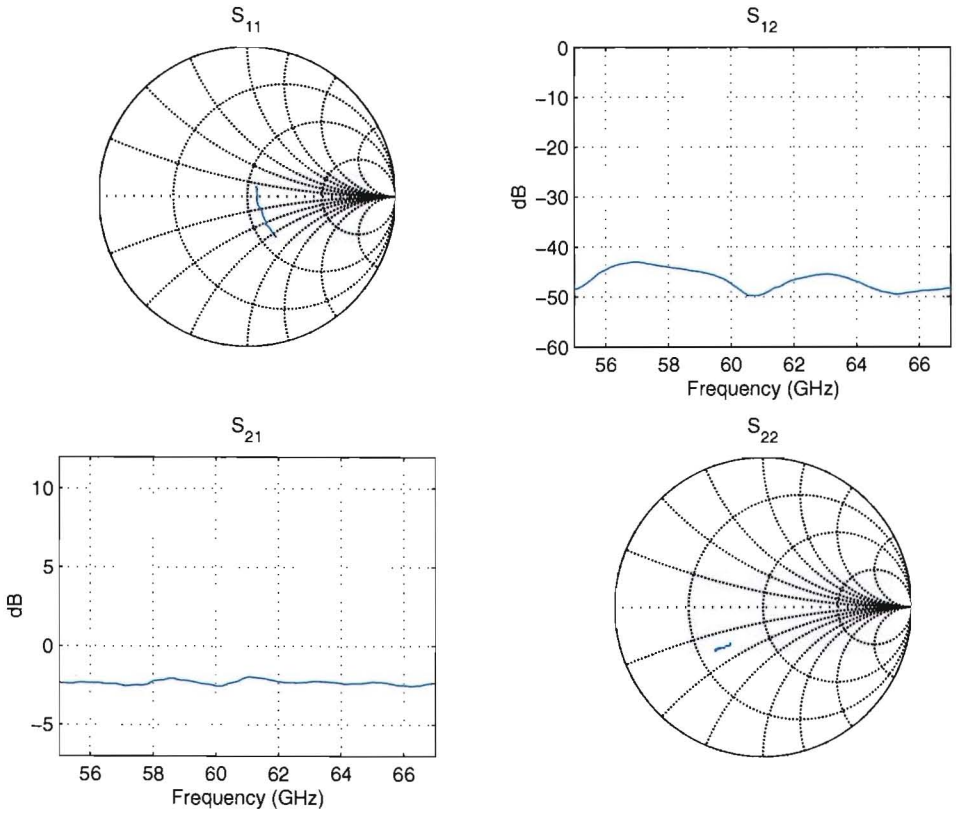


Figure 8.10: Measured S-parameters with $Z_{src} = 7.5\Omega$ and $Z_{load} = 25\Omega$ with a shunt capacitance of 120 fF.

Also the K-factor is calculated of the LNA in common mode. Again because S_{11} and S_{22} are both < 1 and $|S_{12}| << |S_{21}|$, Δ also is smaller than one. The K-factor is shown in the following figure:

As can be seen the K-factor is $>> 1$ in the complete band measured, resulting in unconditional stability for common mode signals.

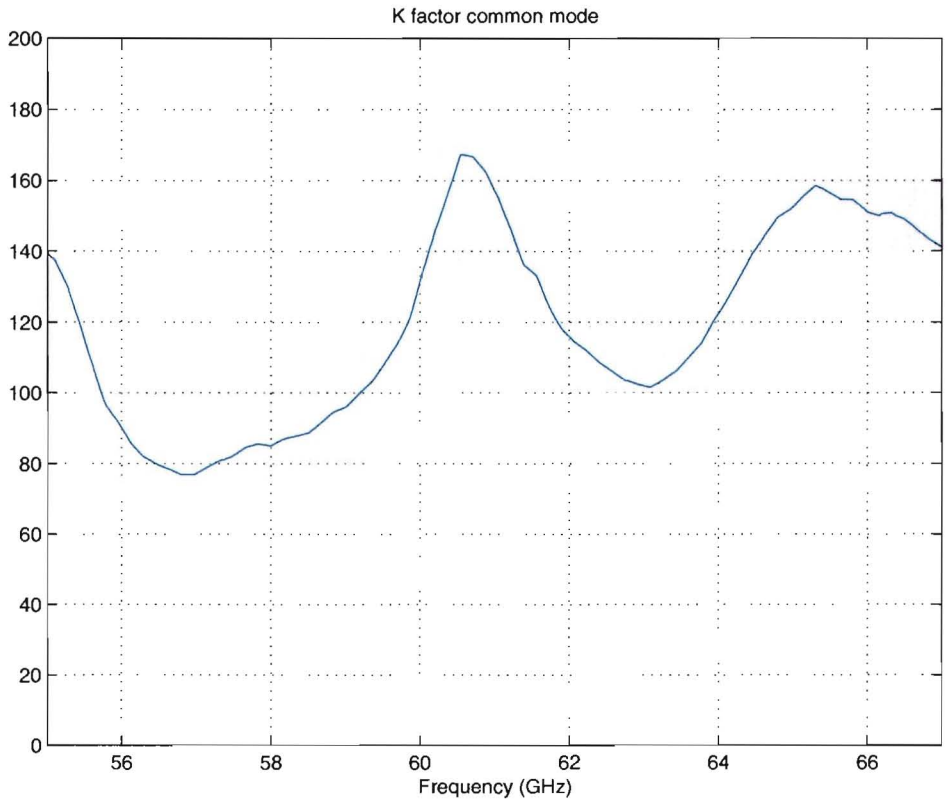
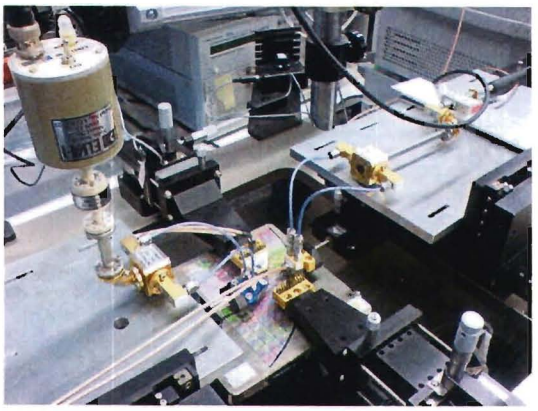


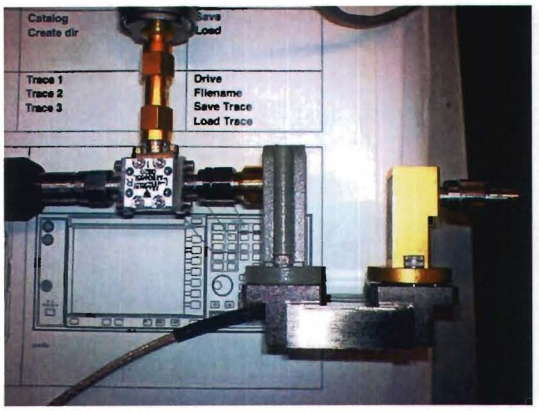
Figure 8.11: K-factor in common mode

8.3 Noise figure

To measure the noise figure of the LNA the measurement setup shown in figure 8.12(a) has been used. The noise has been measured from 59.5 GHz up to 66 GHz. No measurements below this band were performed because the noise source is not defined in this region.



(a) Measurement setup during the noise figure measurement. At the left the noise source can be seen. Waveguides have been used as much as possible to reduce losses.



(b) Downconversion mixer and 60 GHz amplifier.

Figure 8.12: Pictures.

During the NF measurements the equipment in the output path has been calibrated out. The resulting structure over which the noise figure was measured is shown in figure 8.13 schematically.

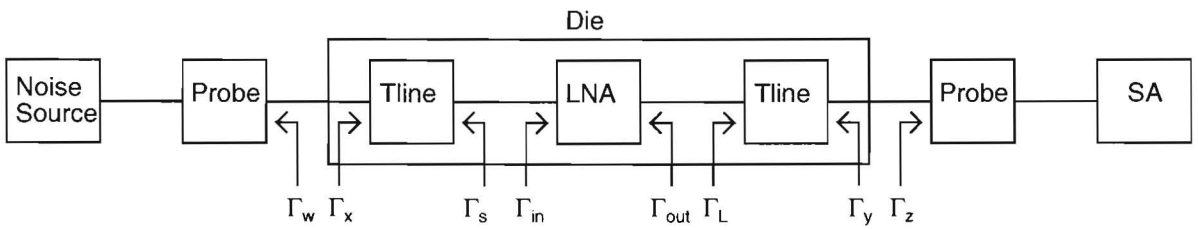


Figure 8.13: Cascade of different stages during the noise measurement.

To be able to calculate the noise figure of the LNA, Friis formula can be used:

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_{AV,1}} + \frac{F_3 - 1}{G_{AV,1}G_{AV,2}} + \cdots \tag{8.10}$$

In which F_x is the noise factor of stage x and $G_{AV,x}$ is the available gain of stage x. Because the noise factor of a passive structure is equal to the inverse of its available gain, the noise factor of the LNA can be calculated when the available gain of every stage is known, and the total noise figure is known. Measurement have been performed be able to calculate these quantities.

The available gain of the probes is measured to be approximately equal to -4 dB. To calculate the available gain of the bondpad with ESD diode and transmission line the S-parameters can be used. Therefore the following formula was used [5]:

$$G_{AV} = \frac{1 - |\Gamma_s|^2}{|1 - \Gamma_s S_{11}|^2} |S_{21}|^2 \frac{1}{1 - |\Gamma_{out}|^2} \tag{8.11}$$

The same was done for the LNA. As can be seen the equation for the available gain is dependent on the source impedance (reflection coefficient). Therefore this quantity also has to be derived for every part in the cascade. Assumed was the Γ_s for the probes is equal to 0, which is a valid assumption for the probe at the input, but not for the probe on the output (Γ_y in figure 8.13). But the effect of the output probe is negligible on the overall calculation, and therefore it is neglected. Γ_w is assumed to be zero because of the lossy probe. Γ_s is equal to the Γ_{out} of the first Tline:

$$\Gamma_s = S_{22} + \frac{S_{21}^2 \Gamma_w}{1 - S_{22}\Gamma_w} = S_{22} \tag{8.12}$$

The noise figure of the LNA is dependent of the source impedance. This source impedance is given below in figure 8.14.

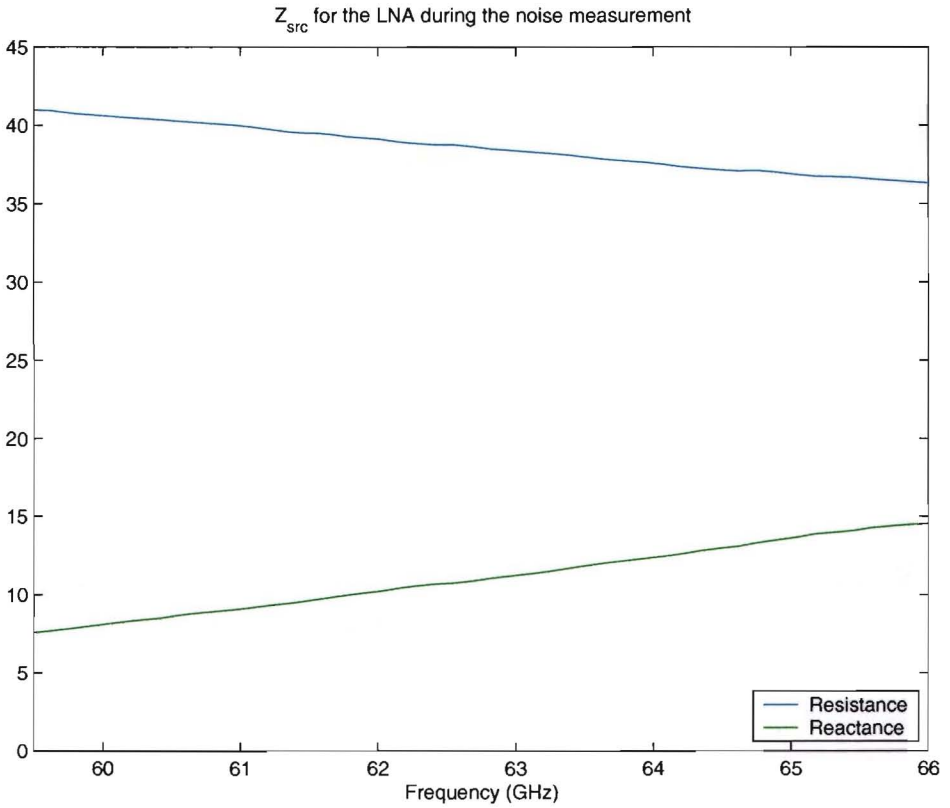


Figure 8.14: Source impedance used during the noise measurements.

It can be seen Z_{src} is mainly resistive with a resistance of approximately 40 Ω and a reactance of approximately 10 Ω. As can be seen in the simulations this value will result in

approximately NF_{min}, so this value is approximately equal to $Z_{src,opt,NF}$.

Γ_{out} is equal to the Γ_{out} of the LNA:

$$\Gamma_{out} = S_{22} + \frac{S_{21}S_{12}\Gamma_s}{1 - S_{22}\Gamma_s} \tag{8.13}$$

With these calculations it is possible to calculate all the available gains of the different stages in the cascade. Using this Γ_{out} the available gain of the second Tline can also be calculated. The available gains of the first and second Tline are respectivily $\approx$ -1.1 dB and $\approx$ -2.5 dB. The resulting available gain of the LNA is given in figure 8.15.

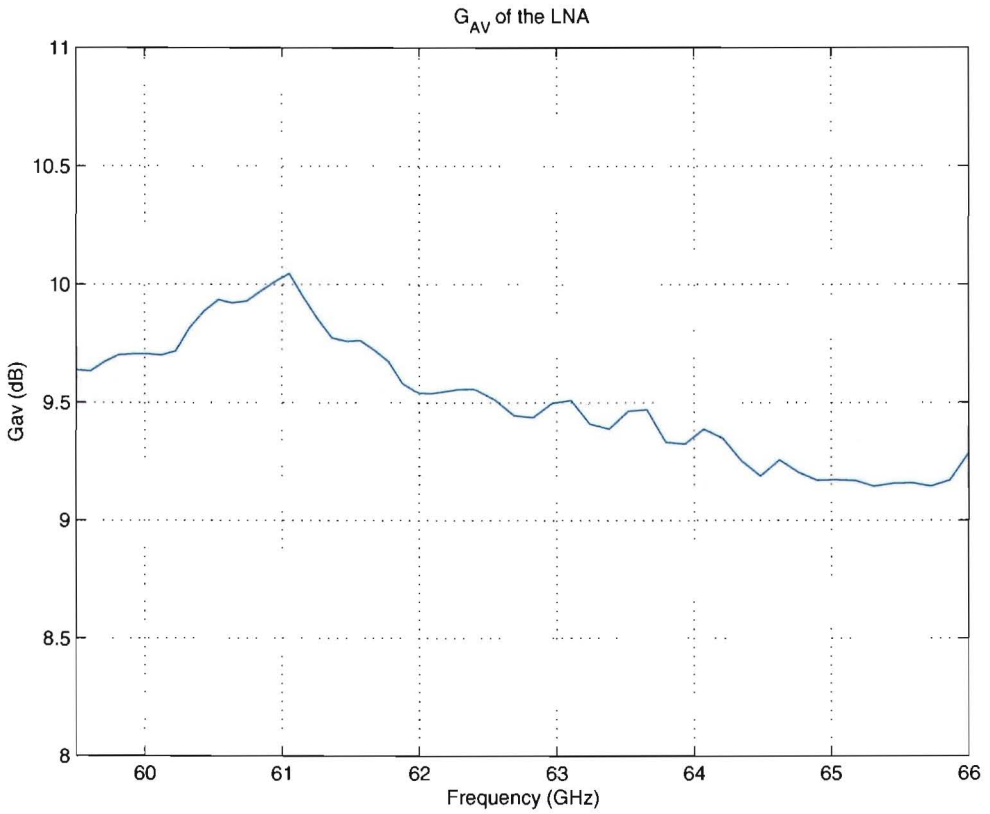


Figure 8.15: Calculated available gain of the LNA with $Z_{src,opt,NF}$.

The resulting measured noise figure of the LNA is given in figure 8.16. **The average value of the NF over the complete measured bandwidth is $\approx$ 3.8 dB.**

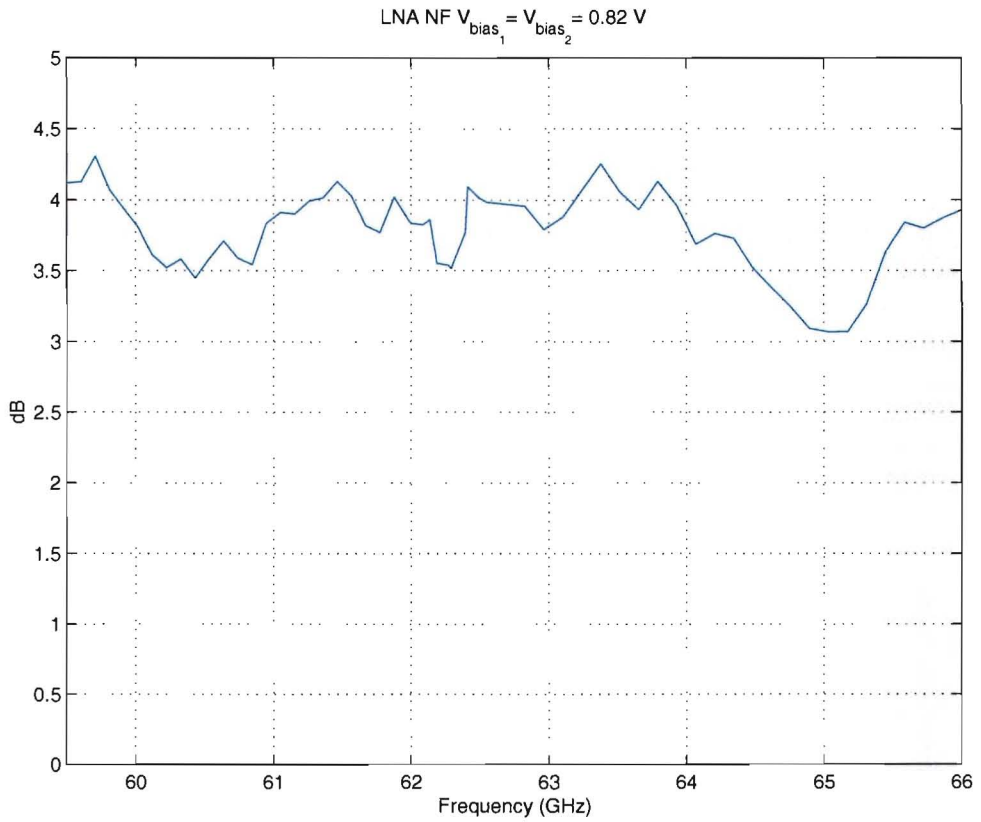


Figure 8.16: Measured noise figure of the LNA.

8.4 Large signal measurements

To investigate the linearity of the circuit the OIP_3, IIP_3 and 1 dB compression point have been measured.

8.4.1 IP_3

To measure the IP_3 of the LNA almost the same setup is used as during the noise figure measurement. The cascade is shown in figure 8.17.

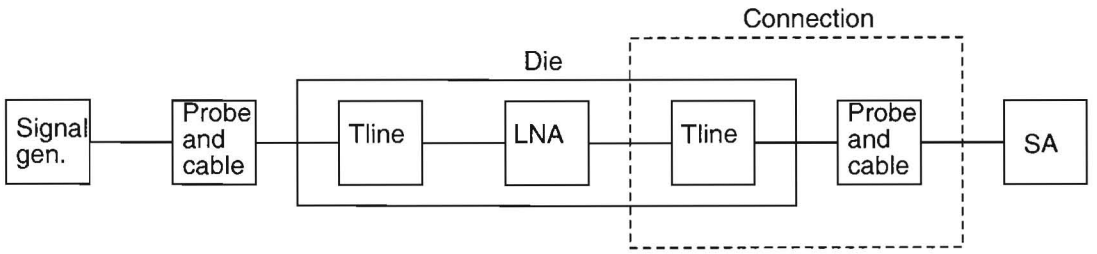


Figure 8.17: Cascade of different stages during the IP_3 measurement.

The power measured by the spectrum analyzer (SA) is equal to the power delivered to its input impedance of 50 Ω (P_{SA}). The loss of the probes with the cables is measured at 57.5 GHz and at 60 GHz, and are respectively 9.87 dB and 9.7 dB per probe cable combination with in and output terminated with the characteristic impedance. This structure is assumed to have a $\Gamma_{in} = 0$ when terminated with the spectrum analyzer which is assumed to have an input impedance of 50 Ω. Therefore the power loss of this structure is assumed to be equal to the measured loss. Also the S-parameters of the transmission lines with the bondpads are known. Using this information it is possible to calculate the power delivered by the LNA to the transmission line (P_{Tline}) at the output. Therefore the power gain has to be calculated.

$$G_p = \frac{1}{1-|\Gamma_{in}|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \tag{8.14}$$

$$\frac{P_{SA}}{P_{Tline}} = G_{p,connection} \tag{8.15}$$

$$G_{p,connection} = G_{p,Tline} \cdot G_{p,cable+probe} \tag{8.16}$$

The power gain of the connection at the output of the LNA to the spectrum analyzer for the two frequencies used is given in the table below:

Frequency	$G_{p,connection}$
57.5 GHz	-10.9 dB
60 GHz	-10.7 dB

Using these numbers the OIP_3 can be calculated using the measurement results. This is shown for 57.5 GHz and for 60 GHz in the following figures:

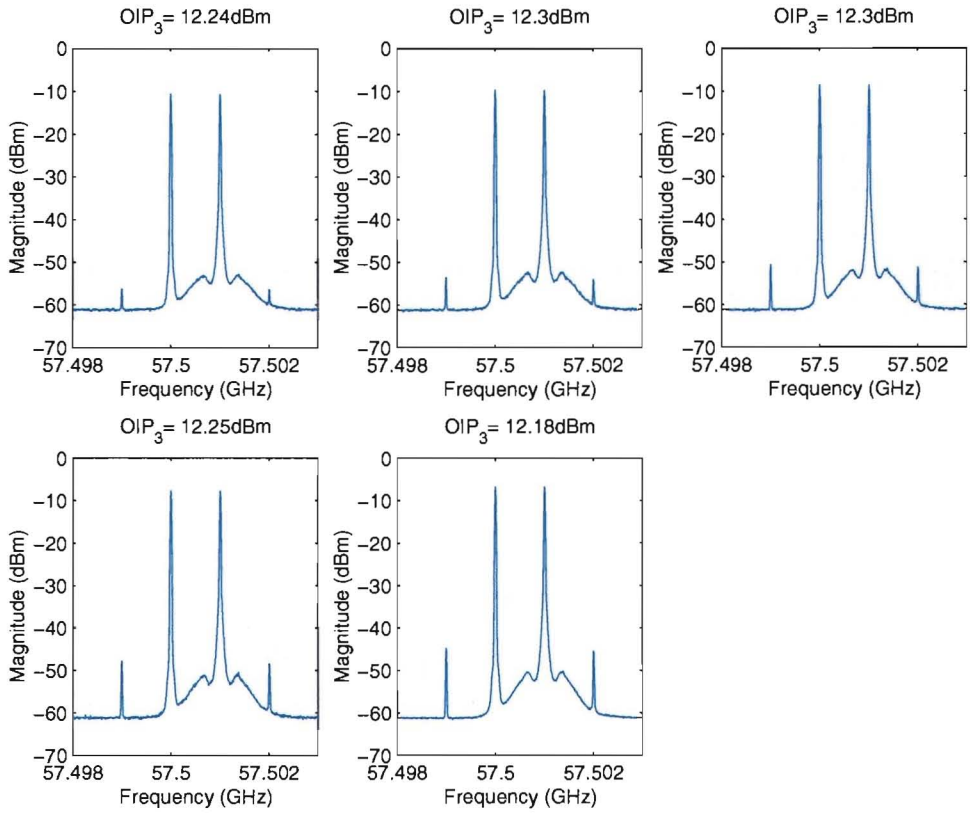


Figure 8.18: Measured OIP_3 at 57.5 GHz.

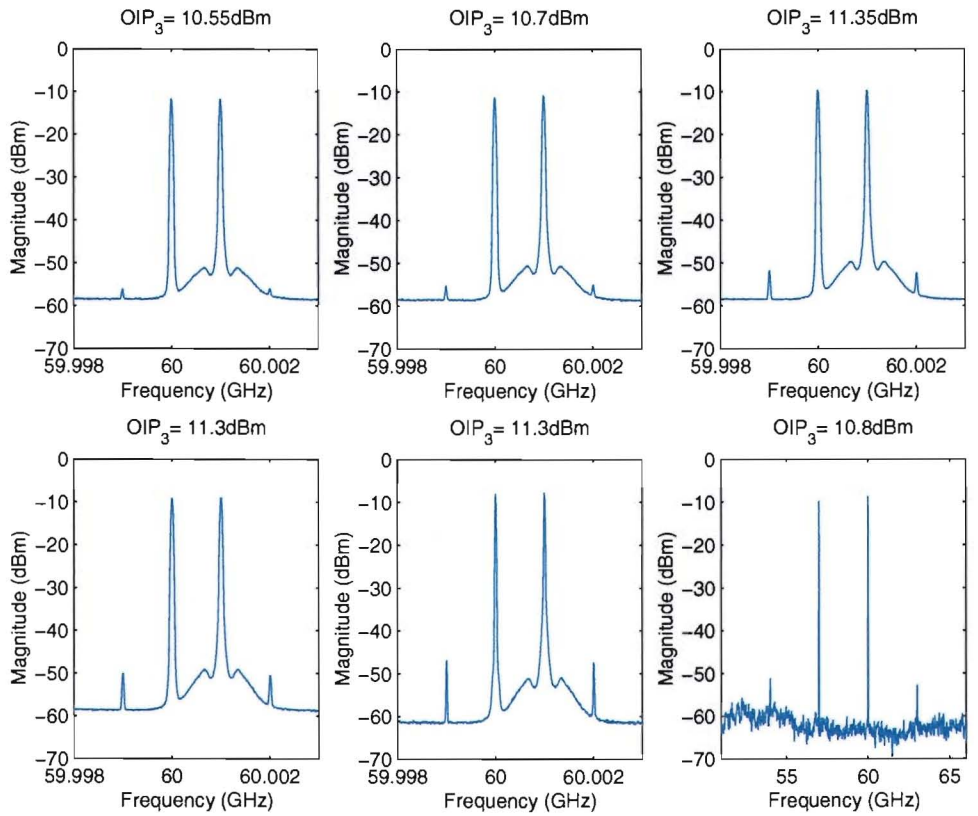


Figure 8.19: Measured OIP_3 at 60 GHz. The lower right plot shows a wideband measurement using a two tone signal with a spacing of 3 GHz.

Measured transducer power gain G_t at 57.5 GHz and 60 GHz of the LNA with the applied in and output impedances by the transmission lines are both approximately equal to 7.2 dB. With this information the IIP_3 can be calculated to be equal to approximately **5 dBm at 57.5 GHz** and **4 dBm at 60 GHz**.

8.4.2 1 dB compression point

In figure 8.20 the output power delivered to the load as a function of the available input power is plotted.

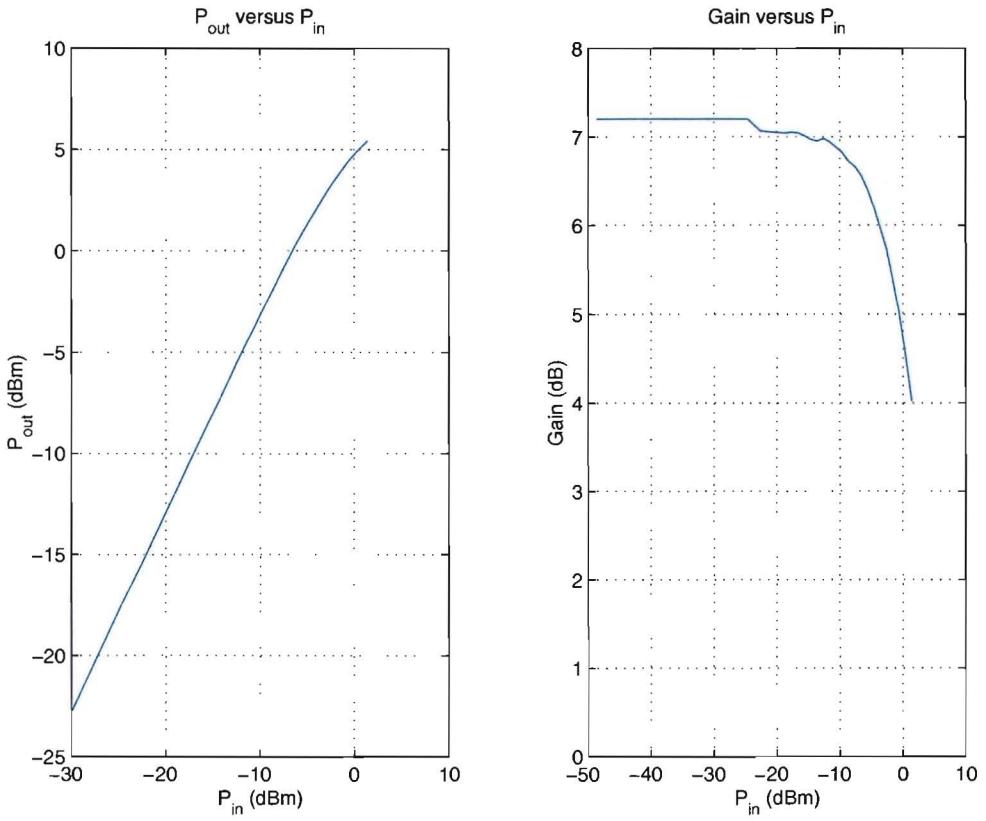
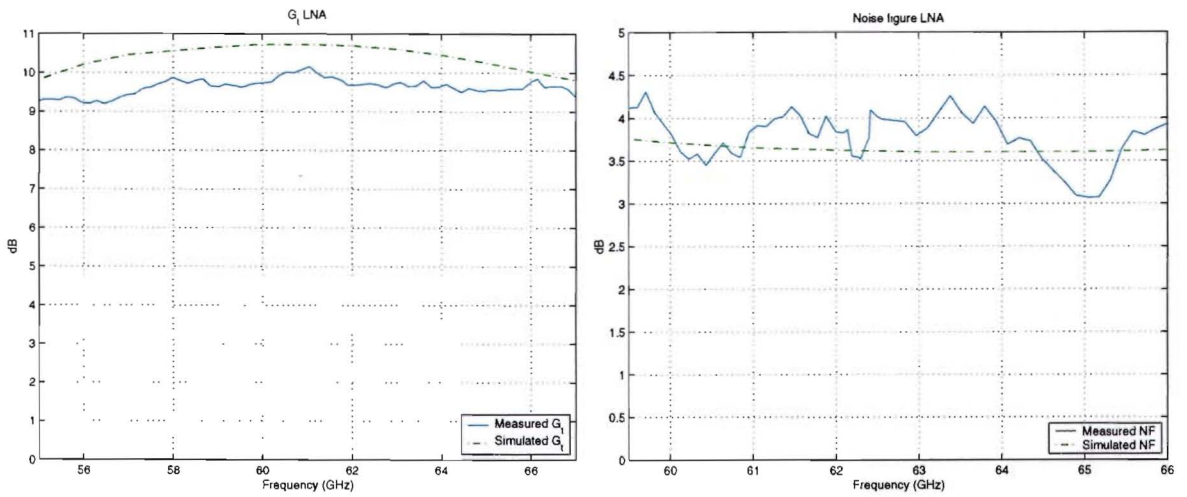


Figure 8.20: Measured P_{out} versus P_{in} and resulting gain. It can be seen the **1 dB compression point is situated at approximately -4.6 dBm.**

8.5 Comparison simulation vs. measurement

To compare the simulated results obtained after layout and the measured results after tape-out, the transducer gain and noise figure of the LNA are compared in figure 8.21. It can be seen the simulated results show great similarity with the measured results.



(a) Simulated versus measured transducer gain G_t.

(b) Simulated versus measured noise figure.

Figure 8.21: Comparison simulated versus measured results fully balanced LNA 58-64 GHz.

Chapter 9

Conclusions and recommendations

A comparison was made between a g_m-boosted CG topology and two voltage-voltage transformer feedback LNA's (with and without cascode), all differential. The voltage-voltage transformer feedback LNA without cascode was designed and taped out in CMOS 65 nm technology. At the time of this writing this LNA was not measured yet but simulations were very promising, taking many parasitics and EM simulations for the various passive devices into account. Because of the use of a CS MOST as an active device without the use of a cascode MOST for gate drain capacitance neutralization, the noise figure is kept very low. High gain flatness has been achieved because of the use of (transformer) feedback. All design goals stated were met except for the gain. But because the noise figure is much lower than stated in the specifications, this can be solved in the next stage. The next stage is therefore allowed to have a higher noise figure but higher gain to have the same overall performance. Another possibility is adding another stage to the LNA, resulting in a low NF, but higher power consumption.

Also a single transformer was designed, simulated and taped out to verify the simulation in Momentum with reality. The measurement results show small deviation from the results obtained in simulation concerning inductance and coupling factor. Q-factors were difficult to measure accurately.

To keep NF low and s_{21} high, the losses in the matching network should be kept very low. Therefore it is important to keep the distance between the bondpads, L_{g1} and the first stage as short as possible. Also R_g of the MOSTs used have big influence and should be kept low. On the other hand, small R_g states more metal to be used in the gate connection and higher capacitance (lower f_t), so there is a trade-off.

Chapter 10

My own contributions

- Analysis and comparison of four configurations for the LNA using gain, noise performance including R_g and channel noise and input impedance characteristics;
- Extract behavior model for use in circuit simulator ADS using C_{gs}, C_{gd}, g_m, R_{ds} and a channel noise source;
- Intensive use of Momentum (EM simulator) for modeling of transformers, transmission lines and inductors used in the design;
- Complete systematic on chip transformer design:
  - Metal line width determination;
  - Determine the structure to be used;
  - Fit lumped transformer model to Momentum simulation;
- Systematic design V-V transformer feedback LNA;
- Layout transformer and V-V transformer feedback LNA;
- Measurement transformer;
- Investigate calibration methods for high frequencies.

Bibliography

[1] X. Li, S. Shekhar and D. J. Allstot, G_m-Boosted Common-Gate LNA and Differential Colpitts VCO/QVCO in 0.18-μm CMOS in IEEE J. Solid-State Circuits, Vol. 40, No. 12, Dec. 2005 Symp., 2004, pp. 97100.

[2] J. R. Long, Monolithic transformers for silicon RF IC design in IEEE J. Solid-State Circuits, vol. 35, no. 9, pp. 13681382, Sep. 2000.

[3] D. J. Cassan and J. R. Long, A 1-V Transformer-Feedback Low-Noise Amplifier for 5-GHz Wireless LAN in 0.18-μm CMOS in IEEE J. Solid-State Circuits, Vol. 38, No. 3, Mar. 2003

[4] P. E. Allen, D. R. Holberg, CMOS Analog Circuit Design 2nd edition, Oxford University Press 2002

[5] G. Gonzalez, Microwave Transistor Amplifiers 2nd edition, Prentice Hall 1997

[6] R. K. Mongia, I. J. Bahl, P. Bhartia and J. Hong, RF and Microwave Coupled-line Circuits 2nd edition, Artech House 2007

Appendix A

Appendix

A.1 Telegrapher's equations

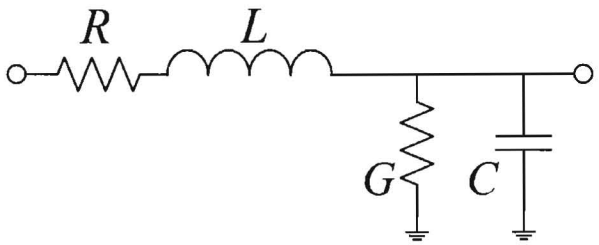


Figure A.1: RLGC equivalent circuit of the CPW.

Each section Δx is modeled by a resistance R (Ω/m), inductance L (H/m), capacitance C (F/m) and conductance G (S/m). Therefore the following equations hold:

$$v(x,t) - v(x+\Delta x,t) = R\Delta x \cdot i(x,t) + L\Delta x \frac{\partial i(x,t)}{\partial t}$$

And

$$i(x,t) - i(x+\Delta x,t) = G\Delta x \cdot v(x,t) + C\Delta x \frac{\partial v(x,t)}{\partial t}$$

Divide by Δx and taking the limit as $\Delta x \to 0$ results in:

$$\frac{\partial v(x,t)}{\partial x} = -Ri(x,t) - L\frac{\partial i(x,t)}{\partial t}$$

And

$$\frac{\partial i(x,t)}{\partial x} = -Gv(x,t) - C\frac{\partial v(x,t)}{\partial t}$$

For a sinusoidal excitation ($f(x)$ and $g(x)$ are real functions):

$$v(x,t) = f(x)\cos(\omega t + \phi(x)) = Re[f(x)\, e^{j(\omega t + \phi(x))}] = Re[f(x)\, e^{j\phi(x)}\, e^{j\omega t}]$$

And

$$i(x,t) = g(x)\cos(\omega t + \eta(x)) = Re[g(x)\, e^{j(\omega t+\eta(x))}] = Re[g(x)\, e^{j\eta(x)}\, e^{j\omega t}]$$

Introducing the following phasor quantities:

$$V(x) = f(x)\, e^{j\phi(x)}$$

$$I(x) = g(x)\, e^{j\eta(x)}$$

$$\rightarrow \frac{\partial}{\partial x} Re[V(x)\, e^{j\omega t}] = -R \cdot Re[I(x)\, e^{j\omega t}] - L\frac{\partial}{\partial t} Re[I(x)\, e^{j\omega t}]$$

$$\rightarrow \frac{\partial}{\partial x} Re[I(x)\, e^{j\omega t}] = -G \cdot Re[V(x)\, e^{j\omega t}] - C\frac{\partial}{\partial t} Re[V(x)\, e^{j\omega t}]$$

These equations can be rewritten as:

$$Re\Big[\Big(\frac{dV(x)}{dx} + (R + j\omega L)I(x)\Big)\, e^{j\omega t}\Big] = 0$$

And

$$Re\Big[\Big(\frac{dI(x)}{dx} + (G + j\omega C)V(x)\Big)\, e^{j\omega t}\Big] = 0$$

This results in the following equations:

$$\frac{dV(x)}{dx} = -(R + j\omega L)I(x)$$

And

$$\frac{dI(x)}{dx} = -(G + j\omega C)V(x)$$

$$\rightarrow \frac{d^2V(x)}{dx^2} - (R + j\omega L)(G + j\omega C)V(x) = 0$$

Introducing the complex propagation constant γ:

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}$$

$$\frac{d^2V(x)}{dx^2} - \gamma^2 V(x) = 0$$

The general solution for this second order differential equation is (with A and B being complex constants):

$$V(x) = A\, e^{-\gamma x} + B\, e^{\gamma x}$$

$$I(x) = \frac{-1}{R + j\omega L}\frac{dV(x)}{dx} = \frac{\gamma}{R + \omega L}[A\,e^{-\gamma x} + B\,e^{\gamma x}]$$

Introducing the characteristic impedance Z_0:

$$Z_0 = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

$$\rightarrow I(x) = \frac{A}{Z_0}A\,e^{-\gamma x} + \frac{B}{Z_0}A\,e^{\gamma x}$$

In general $\omega L > R$ and $\omega C > G$. So Z_0 and γ can also be expressed as follows [6]:

$$Z_0 = \sqrt{\frac{L}{C}}$$

$$\gamma = j\omega\sqrt{LC}\Big[1 + \frac{R}{2j\omega L} + \frac{G}{2j\omega C}\Big]$$

The propagation constant γ consists of a phase constant β and an attenuation constant α.

$$\rightarrow \beta = \omega\sqrt{LC} \text{ rad/unit length}$$

$$\rightarrow \alpha = \frac{1}{2}\Big(\frac{R}{Z_0} + GZ_0\Big) \text{ Np/unit length}$$

To model the loss in dB/unit length, α must be multiplied by 8.686.

$$\rightarrow \alpha = 4.343\Big(\frac{R}{Z_0} + GZ_0\Big) \text{ dB/unit length}$$

A.2 Linearity, differential vs. single ended

To compare the performance concerning higher order distortion in a single ended situation to a differential situation, this will be calculated for both stages, starting with the single ended. The large signal output current of a single MOST can be approximated by the following Taylor expansion:

$$I_{out}(V_{in}) \approx I_{out}(V_b) + \frac{I'_{out}(V_b)}{1!}(V_{in} - V_b) + \frac{I''_{out}(V_b)}{2!}(V_{in} - V_b)^2 + \frac{I'''_{out}(V_b)}{3!}(V_{in} - V_b)^3 + \ldots$$

If only the AC behavior is taken into account and $I'_{out}(V_b) = g_m$, the expression converges to the following with g'_m and g''_m being the first and second derivatives of g_m respectively.

$$I_{out}(V_{in}) \approx g_m V_{in} + \frac{g'_m}{2!}V_{in}^2 + \frac{g''_m}{3!}V_{in}^3 + \ldots$$

For a sinusoidal excitation this expression becomes:

$$I_{out}(A\cos(\omega t)) \approx g_m A\cos(\omega t) + \frac{g'_m A^2}{2!}\cos^2(\omega t) + \frac{g''_m A^3}{3!}\cos^3(\omega t) + \dots$$

$$\approx g_m A\cos(\omega t) + \frac{g'_m A^2}{2!\cdot 2}\Big(1+\cos(2\omega t)\Big) + \frac{g''_m A^3}{3!\cdot 4}\Big(3\cos(\omega t)+\cos(3\omega t)\Big) + \dots$$

$$\approx \frac{g'_m A^2}{2!\cdot 2} + \Big(g_m A + 3\frac{g''_m A^3}{3!\cdot 4}\Big)\cos(\omega t) + \frac{g'_m A^2}{2!\cdot 2}\cos(2\omega t) + \frac{g''_m A^3}{3!\cdot 4}\cos(3\omega t) + \dots$$

In the differential situation the output current is the difference of output current of two single ended stages, one exited with $V_{in}/2$ and the other with $-V_{in}/2$. The Taylor expansion for the large signal AC output current then looks as follows:

$$I_{out}(V_{in}) \approx g_m\Big(\frac{V_{in}}{2} - \frac{-V_{in}}{2}\Big) + \frac{g'_m}{2!}\Big(\Big(\frac{V_{in}}{2}\Big)^2 - \Big(\frac{-V_{in}}{2}\Big)^2\Big) + \frac{g''_m}{3!}\Big(\Big(\frac{V_{in}}{2}\Big)^3 - \Big(\frac{-V_{in}}{2}\Big)^3\Big) + \dots$$

As can be seen the second order distortion cancels by using the differential topology. This cancellation holds for all even order distortions because $x^{2n} = (-x)^{2n}$ (for all $n \in \mathbb{N}$). For a sinusoidal excitation the expression becomes:

$$I_{out}(A\cos(\omega t)) \approx g_m A\cos(\omega t) + \frac{g''_m}{3!}\Big(\frac{A}{2}\cos(\omega t)\Big)^3 - \frac{g''_m}{3!}\Big(-\frac{A}{2}\cos(\omega t)\Big)^3 + \dots$$

$$\approx g_m A\cos(\omega t) + \frac{g''_m A^3}{3!\cdot 4}\cos^3(\omega t) + \dots$$

$$\approx \Big(g_m A + 3\frac{g''_m A^3}{3!\cdot 16}\Big)\cos(\omega t) + \frac{g''_m A^3}{3!\cdot 16}\cos(3\omega t) + \dots$$

As can be seen also the odd order distortion is less compared to the single ended situation. Therefore a better IP_3 performance is expected for the differential situation compared to the single ended situation, but of course the differential situation will consume twice the power due to the use of two MOSTs.

A.3 Noise factor, differential vs. single ended

To calculate the noise factor of a differential system (as shown in figure A.2), also the half circuit concept may be used if the following holds:

$$\overline{v_{n,1}^2} = \overline{v_{n,2}^2}$$

$$\overline{i_{n,1}^2} = \overline{i_{n,2}^2}$$

$$E[v_{n,1}\cdot v_{n,2}] = E[i_{n,1}\cdot i_{n,2}] = E[v_{n,1}\cdot i_{n,2}] = E[i_{n,1}\cdot v_{n,2}] = 0$$

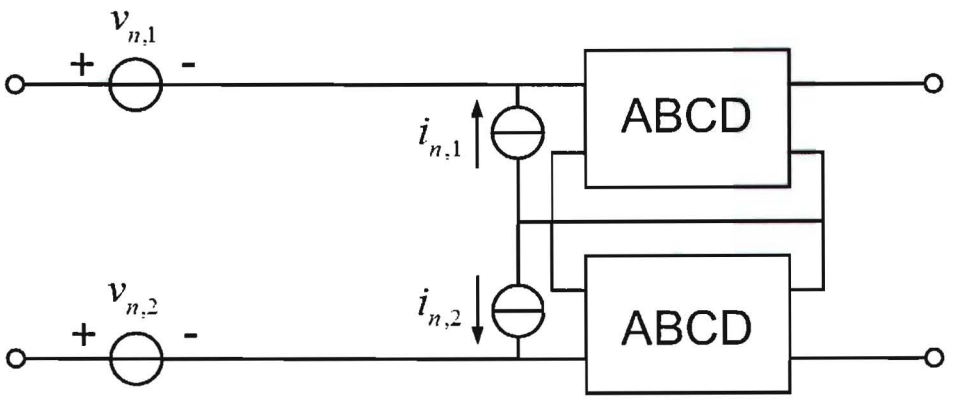


Figure A.2: Differential system with all noise sources brought to the single ended inputs

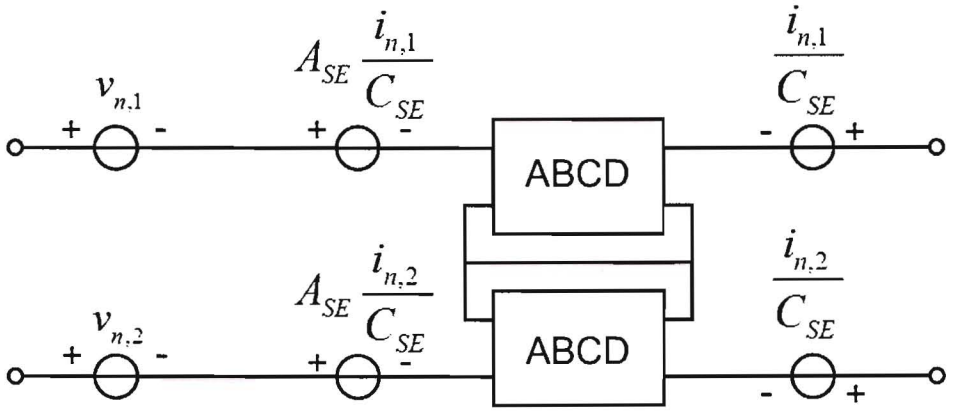


Figure A.3: Current noise sources brought to the input and output

The noise sources can be brought to the differential input as shown in figures A.3 and A.4.

The ABCD matrix of a differential circuit can be derived from the ABCD matrix of the single ended circuit as follows:

$$\begin{bmatrix} A_D & B_D \\ C_D & D_D \end{bmatrix} = \begin{bmatrix} A_{SE} & 2 \cdot B_{SE} \\ \frac{C_{SE}}{2} & D_{SE} \end{bmatrix}$$

The four voltage sources due to the current noise sources cancel because $A_D = A_{SE}$. The resulting noise sources due to the current noise sources are:

$$\frac{C_D i_{n,1}}{C_{SE}} = \frac{i_{n,1}}{2}$$

$$\frac{C_D i_{n,2}}{C_{SE}} = \frac{i_{n,2}}{2}$$

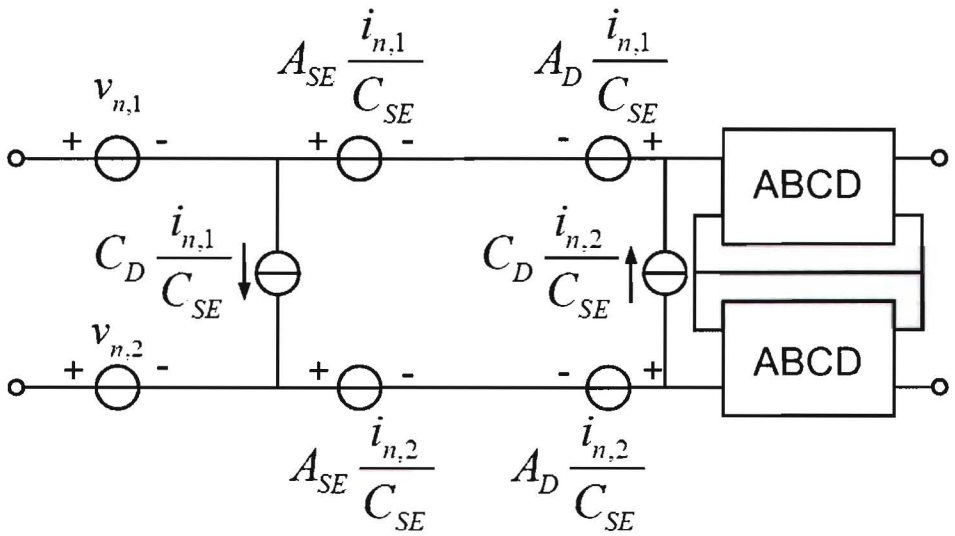


Figure A.4: All noise sources referred to the input

Because of the statements at the start of this section, the resulting input noise looks as follows:

$$|\overline{v_{n,in}}|^2 = |\overline{v_{n,1}} + \overline{i_{n,1}} \cdot \frac{Z_{src}}{2}|^2 + |\overline{v_{n,2}} + \overline{i_{n,2}} \cdot \frac{Z_{src}}{2}|^2$$

$$|\overline{v_{n,in}}|^2 = 2 \cdot |\overline{v_n} + \overline{i_n} \cdot \frac{Z_{src}}{2}|^2$$

The noise factor of the differential situation then becomes:

$$F_D = \frac{4ktR_{src} + 2 \cdot |\overline{v_n} + \overline{i_n} \cdot \frac{Z_{src}}{2}|^2}{4ktR_{src}}$$

$$F_D = 1 + \frac{|\overline{v_n} + \overline{i_n} \cdot \frac{Z_{src}}{2}|^2}{4kt\frac{R_{src}}{2}}$$

The noise factor of the single ended situation is:

$$F_{SE} = 1 + \frac{|\overline{v_n} + \overline{i_n} \cdot Z_{src}|^2}{4ktR_{src}}$$

So conclusion is the noise figure for the differential situation and for the single ended situation are related in the following way:

$$F_D(Z_{src}) = F_{SE}\left(\frac{Z_{src}}{2}\right)$$

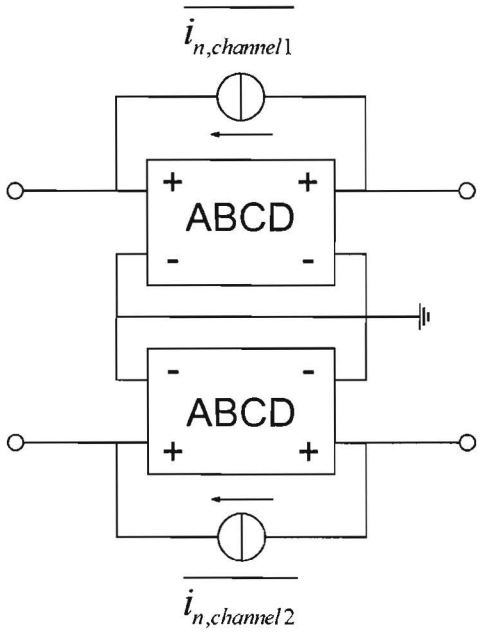


Figure A.5: The location of the channel noise in the differential common gate stage

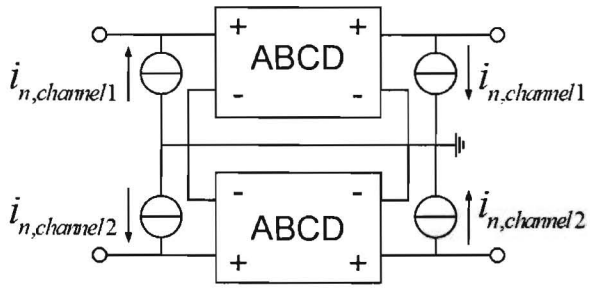


Figure A.6: Channel noise sources moved to input and output

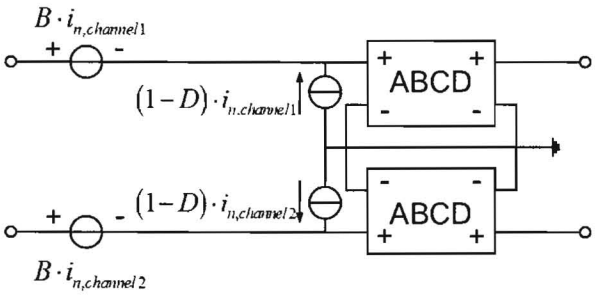


Figure A.7: Channel noise sources referred to the input

A.4 Noise factor calculation of the g_m-boosted CG LNA

To calculate the noise factor of the g_m-boosted common gate LNA, all noise sources have to be referred to the input. In figures A.5, A.6 and A.7 it is explained how this can be done for the channel noise.

The input referred noise voltage due to the channel noise looks as follows for the single ended circuit. Later it will be adjusted for the differential case as already explained in the appendix.

$$\overline{v_{n,in,channel}^2} = |B + (D-1)Z_{src}|^2 4kT\gamma g_m$$

To calculate the ABCD-parameters, also the single ended circuit is used. The small signal equivalent circuit of the first stage (without cascode) is shown in figure A.8. The impedance seen looking into the next common gate stage is modeled by Z_{load}. After having calculated the ABCD-parameters of the single ended circuit, they can also be easily calculated for the differential case as shown previously.

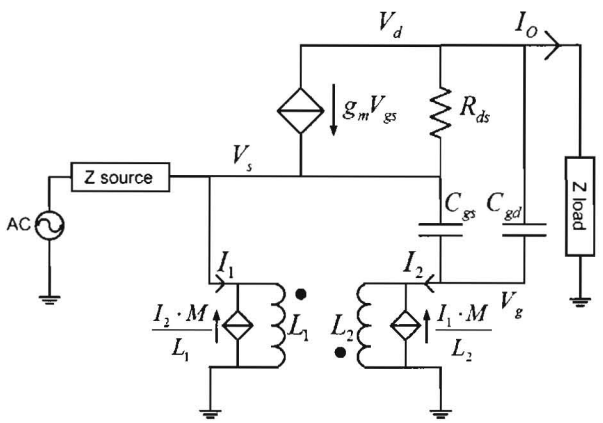


Figure A.8: Small signal equivalent circuit of the g_m-boosted common gate LNA

The node equations of the small signal equivalent circuit are given below (k is the coupling between the two inductors):

$$\mathbf{Y} = \begin{bmatrix} sC_{gs} + g_m + \frac{1}{R_{ds}} + \frac{1}{s(1-k^2)L_1} & -sC_{gs} - g_m - \frac{k}{s(1-k^2)\sqrt{L_1 L_2}} & -\frac{1}{R_{ds}} \\ -sC_{gs} - \frac{k}{s(1-k^2)\sqrt{L_1 L_2}} & s(C_{gs} + C_{gd}) + \frac{1}{s(1-k^2)L_2} & -sC_{gd} \\ -g_m - \frac{1}{Rds} & g_m - sC_{gd} & \frac{1}{Z_{load}} + sC_{gd} + \frac{1}{R_{ds}} \end{bmatrix}$$

$$\mathbf{Y} \cdot \begin{bmatrix} V_s \\ V_g \\ V_d \end{bmatrix} = \begin{bmatrix} I_{in} \\ 0 \\ 0 \end{bmatrix}$$

For the calculation of the B and D parameters, R_{ds} has been ignored to ease the calculations. Simulations show a bit higher noise factor due to this. But the optimum stays approximately constant.

$$B \approx \frac{s^2(1-k^2)L_2(C_{gd}+C_{gs})+1}{s^3(1-k^2)L_2C_{gs}C_{gd}+s^2(1-k^2)L_2C_{gd}g_m+sknC_{gd}+g_m(1-kn)}$$

$$D \approx \frac{s^3(1-k^2)L_2C_{gs}C_{gd}+s^2(1-k^2)L_2C_{gd}g_m+sn^2C_{gd}+s(n^2-2kn+1)C_{gs}+g_m(1-kn)+\frac{1}{sL_1}}{s^3(1-k^2)L_2C_{gs}C_{gd}+s^2(1-k^2)L_2C_{gd}g_m+sknC_{gd}+g_m(1-kn)}$$

$$n = \sqrt{L_2/L_1}$$

If the coupling $k \rightarrow -1$, the higher order terms disappear:

$$B \approx \frac{1}{g_m(1+n)-snC_{gd}}$$

$$D \approx \frac{sn^2C_{gd}+s(1+n)^2C_{gs}+g_m(1+n)+\frac{1}{sL_1}}{g_m(1+n)-snC_{gd}}$$

$$\rightarrow \overline{v^2_{n,in,channel}} \approx \left|\frac{1+Z_{src}(s(1+n)nC_{gd}+s(1+n)^2C_{gs}+\frac{1}{sL_1})}{g_m(1+n)-snC_{gd}}\right|^2 4kT\gamma g_m$$

To minimize the input referred noise due to the channel noise, L_1, C_{gs} and C_{gd} can be chosen to resonate at the operating frequency. To do so, L_1 should be chosen to have the following value:

$$L_1 = \frac{1}{\omega^2((1+n)nC_{gd}+(1+n)^2C_{gs})}$$

$$\overline{v^2_{n,in,channel}} \approx \left|\frac{1}{g_m(1+n)-snC_{gd}}\right|^2 4kT\gamma g_m$$

The expression consists a pole at:

$$\omega_{pole} = \frac{g_m(1+n)}{nC_{gd}} > \frac{g_m}{C_{gd}} > \frac{g_m}{C_{gd}+C_{gs}} = 2\pi f_t$$

The position of the pole is beyond the f_t of the device so this effect can be ignored. The resulting input referred noise voltage due to the channel noise then looks as follows:

$$\overline{v^2_{n,in,channel}} \approx \frac{4kT\gamma}{g_m(1+n)^2}$$

Next the influence of the noise due to R_g will be investigated. Goal is to define one ABCD matrix of the complete system with the influence of V_n included. Therefore the definition of the ABCD matrix is given:

$$\mathbf{ABCD} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \cdot \begin{bmatrix} V_{out} \\ I_{out} \end{bmatrix} = \begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix}$$

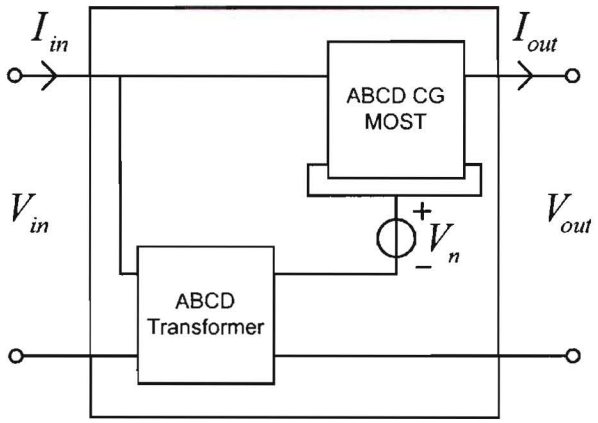


Figure A.9: Building one ABCD matrix out of two matrices and the noise source due to R_g.

And the following equation must hold:

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} - \begin{bmatrix} A & B \\ C & D \end{bmatrix} \cdot \begin{bmatrix} V_{out} \\ I_{out} \end{bmatrix} = 0$$

$$\mathbf{ABCD}_{MOST,CG} = \begin{bmatrix} A_M & B_M \\ C_M & D_M \end{bmatrix}$$

$$\mathbf{ABCD}_{Transformer} = \begin{bmatrix} A_T & B_T \\ C_T & D_T \end{bmatrix} = \begin{bmatrix} \frac{1}{kn} & \frac{s(1-k^2)nL_1}{k} \\ \frac{1}{sknL_1} & \frac{n}{k} \end{bmatrix}$$

V_{in}, I_{in}, V_{out} and I_{out} are defined as follows:

$$V_{in} = V_{in,M} + V_n + V_{out,T} = V_{in,T}$$

$$I_{in} = I_{in,M} + I_{in,T}$$

$$V_{out} = V_{out,M} + V_n + V_{out,T}$$

$$I_{out} = I_{out,M} = I_{in,M} + I_{out,T}$$

Combining these equations gives the ABCD matrix of the complete system. If V_n is looked at input referred, it results in a voltage and a current source as follows:

$$V_{n,in,R_g} = \frac{A_T - A_M A_T}{A_M + A_T + B_T C_M - 1} \cdot V_n$$

$$I_{n,in,R_g} = \frac{-A_T C_M + C_T - A_M C_T - B_T C_M C_T + A_T C_M D_T}{A_M + A_T + B_T C_M - 1} \cdot V_n$$

If R_{ds} and R_g are neglected in this step, the following approximation results:

$$V_{n,in} \approx \frac{g_m - sC_{gd}}{s^2(1-k^2)L_2C_{gd}(sC_{gs}+g_m) + sknC_{gd} + g_m(1-kn)} \cdot V_n$$

$$I_{n,in} \approx \frac{1}{sL_1} \cdot \frac{-s^2(1-kn)L_1C_{gd}(sC_{gs}+g_m) + g_m - sC_{gd}}{s^2(1-k^2)L_2C_{gd}(sC_{gs}+g_m) + sknC_{gd} + g_m(1-kn)} \cdot V_n$$

For high negative coupling this results in:

$$V_{n,in,R_g} \approx \frac{g_m - sC_{gd}}{g_m(1+n) - snC_{gd}} \cdot V_n \approx \frac{V_n}{1+n}$$

$$I_{n,in,R_g} \approx \frac{1}{sL_1} \cdot \frac{g_m - sC_{gd}}{g_m(1+n) - snC_{gd}} \cdot V_n \approx \frac{V_n}{s(1+n)L_1}$$

This results in the following input referred noise due to R_g:

$$\overline{v^2_{n,in,R_g}} \approx \frac{4kTR_g}{(1+n)^2}\left|1 + \frac{Z_{src}}{sL_1}\right|^2$$

The noise factor then becomes:

$$F_{g_m-boosted,SE} \approx 1 + \frac{R_g}{(1+n)^2R_{src}}\left|1 + \frac{Z_{src}}{sL_1}\right|^2 + \frac{\gamma}{g_m(1+n)^2R_{src}}$$

If $X_{src,SE}$ is chosen to be equal to $\approx -\omega L_1$, the noise due to R_g becomes very small. The noise contribution due to R_g is already much smaller than due to the channel noise if realistic values are filled in, so it can be neglected, resulting in:

$$F_{g_m-boosted,SE} \approx 1 + \frac{\gamma}{g_m(1+n)^2R_{src}}$$

And for the differential case:

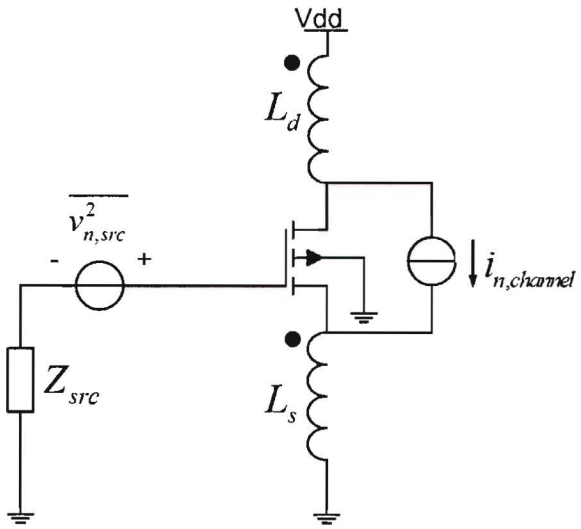
$$F_D(Z_{src}) = F_{SE}\left(\frac{Z_{src}}{2}\right)$$

$$\rightarrow F_{g_m-boosted} \approx 1 + \frac{2\gamma}{g_m(1+n)^2R_{src}}$$

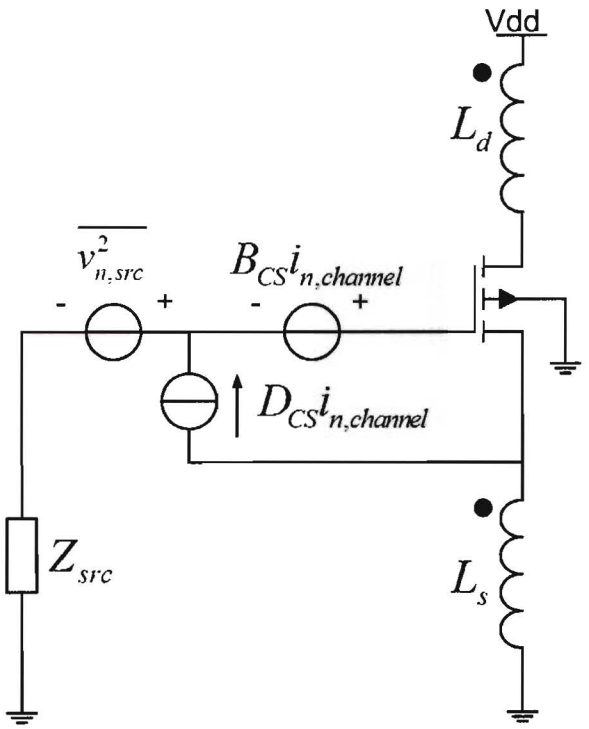
A.5 Noise factor calculation of the V-V transformer FB LNA

To determine the noise factor of the voltage voltage transformer feedback LNA, the channel noise has to be referred to the input.

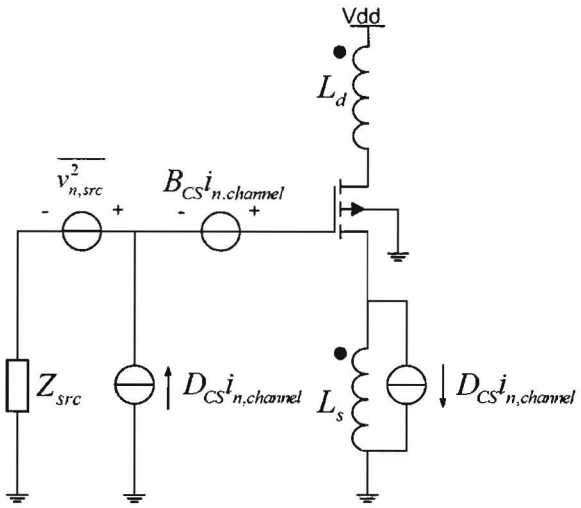
In the last step, the ABCD parameters for the circuit with the signal between the source and ground seen as the output are used. This way the current source connected between the ground and the source of the MOST can be moved to the input. Besides the channel noise the noise generated in the gate resistance also has to be included. This noise source is already



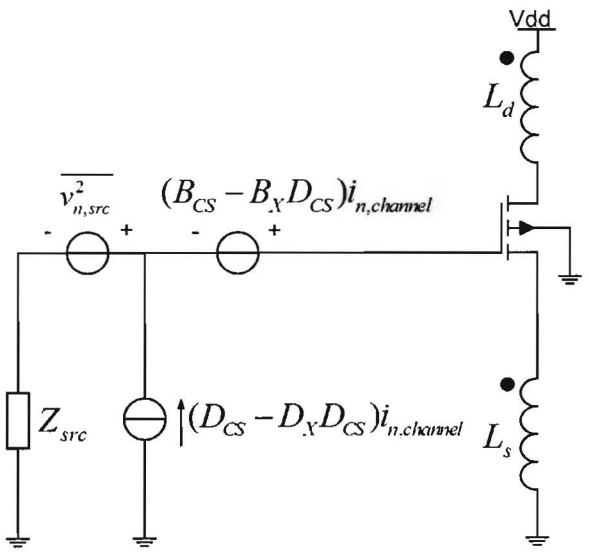
(a) Channel noise in MOST.



(b) Channel noise referred to the input of the MOST.



(c) Current noise source split in two sources.



(d) Channel noise referred to the input of the LNA.

at the input of the system. The total noise contribution referred to the input for the single ended circuit then looks as follows:

$$\overline{v_{n,in}^2} = 4kTR_g + |(B_{CS} - B_xD_{CS}) + (D_{CS} - D_xD_{CS})Z_{src}|^2 4kT\gamma g_m$$

For the calculation of the input referred noise B_{CS}, D_{CS}, B_x and D_x need to be known. The parameters for the common source are already known from section 2.1.

$$B_{CS} = \frac{1 + sR_g(C_{gs} + C_{gd})}{sC_{gd} - g_m}$$

$$D_{CS} = \frac{s(C_{gs} + C_{gd})}{sC_{gd} - g_m}$$

Because g_m/C_{gd} and $1/(R_g(C_{gs}+C_{gd}))$ both are $> g_m/(C_{gs}+C_{gd}) = \omega_t$, these parameters can be approximated by:

$$B_{CS} \approx \frac{-1}{g_m}$$

$$D_{CS} \approx \frac{-s(C_{gs} + C_{gd})}{g_m}$$

$$D_x =$$

$$\frac{s^3(1-k^2)L_dC_{gs}C_{gd} + s^2(1-k^2)L_dC_{gd}(g_m + \frac{1}{R_{ds}}) + \frac{s^2(1-k^2)L_dC_{gs}}{R_{ds}} + s(C_{gs} + C_{gd})}{s^3(1-k^2)L_dC_{gs}C_{gd} + s^2(1-k^2)L_dC_{gd}(g_m + \frac{1}{R_{ds}}) + \frac{s^2(1-k^2)L_dC_{gs}}{R_{ds}} + s(C_{gs} + knC_{gd}) + g_m(1-kn)}$$

If $\frac{n}{k} = -\frac{C_{gs}}{C_{gd}}$

$$D_x|_{\frac{n}{k}=-\frac{C_{gs}}{C_{gd}}} = \frac{s^3(1-k^2)L_dC_{gs}C_{gd} + s^2(1-k^2)L_dC_{gd}(g_m + \frac{1}{R_{ds}}) + \frac{s^2(1-k^2)L_dC_{gs}}{R_{ds}} + s(C_{gs} + C_{gd})}{s^3(1-k^2)L_dC_{gs}C_{gd} + s^2(1-k^2)L_dC_{gd}(g_m + \frac{1}{R_{ds}}) + \frac{s^2(1-k^2)L_dC_{gs}}{R_{ds}} + g_m(1-kn)}$$

For high coupling $D_x|_{\frac{n}{k}=-\frac{C_{gs}}{C_{gd}}}$ converges to:

$$\lim_{k\to-1} D_x|_{\frac{n}{k}=-\frac{C_{gs}}{C_{gd}}} = \frac{s(C_{gs} + C_{gd})}{g_m(1+n)}$$

The B parameter has the same denominator as the D parameter, so when the output isolation is applied ($n/k = -C_{gs}/C_{gd}$), the formula also becomes smaller. The resulting formula is still quite big so an approximation will be given for high coupling. For high coupling $B_x|_{\frac{n}{k}=-\frac{C_{gs}}{C_{gd}}}$ converges to:

$$\lim_{k\to-1} B_x|_{\frac{n}{k}=-\frac{C_{gs}}{C_{gd}}} = \frac{1 + sR_g(C_{gs} + C_{gd})}{g_m(1+n)} \approx \frac{1}{g_m(1+n)}$$

The input referred noise then looks as follows:

$$\lim_{k\to-1} \overline{v_{n,in}^2}\Big|_{\frac{n}{k}=-\frac{C_{gs}}{C_{gd}}} \approx$$

$$4kTR_g + \left|\left(\frac{s(C_{gs}+C_{gd})}{g_m^2(1+n)} - \frac{1}{g_m}\right) + Z_{src}\cdot\left(\frac{s^2(C_{gs}+C_{gd})^2}{g_m^2(1+n)} - \frac{s(C_{gs}+C_{gd})}{g_m}\right)\right|^2 4kT\gamma g_m$$

With resulting single ended noise factor:

$$\lim_{k\to -1} F_{SE}\big|_{\frac{n}{k}=-\frac{C_{gs}}{C_{gd}}} \approx$$

$$1 + \frac{R_g}{R_{src}} + \frac{\gamma g_m}{R_{src}}\left|\left(\frac{s(C_{gs}+C_{gd})}{g_m^2(1+n)} - \frac{1}{g_m}\right) + Z_{src}\cdot\left(\frac{s^2(C_{gs}+C_{gd})^2}{g_m^2(1+n)} - \frac{s(C_{gs}+C_{gd})}{g_m}\right)\right|^2$$

Differentially the noise factor becomes (as discussed in section A.3):

$$\lim_{k\to -1} F_{diff}\big|_{\frac{n}{k}=-\frac{C_{gs}}{C_{gd}}} \approx$$

$$1 + 2\frac{R_g}{R_{src}} + 2\frac{\gamma g_m}{R_{src}}\left|\left(\frac{s(C_{gs}+C_{gd})}{g_m^2(1+n)} - \frac{1}{g_m}\right) + \frac{Z_{src}}{2}\cdot\left(\frac{s^2(C_{gs}+C_{gd})^2}{g_m^2(1+n)} - \frac{s(C_{gs}+C_{gd})}{g_m}\right)\right|^2$$

If a source impedance is chosen with a real and inductive part ($Z_{src} = R_{src} + sL_{src}$) to tune out the capacitive effects and thereby lower the noise factor, it becomes:

$$F_{diff} \approx 1+2\frac{R_g}{R_{src}}+2\frac{\gamma g_m}{R_{src}}\left|\left(\frac{s(C_{gs}+C_{gd})}{g_m^2(1+n)}-\frac{1}{g_m}\right)+\frac{R_{src}+sL_{src}}{2}\cdot\left(\frac{s^2(C_{gs}+C_{gd})^2}{g_m^2(1+n)}-\frac{s(C_{gs}+C_{gd})}{g_m}\right)\right|^2$$

To find the optimal value for L_{src} the partial derivative is taken:

$$\frac{\partial F}{\partial L_{src}} \approx \gamma\omega^2\frac{(\omega^2 L_{src}(C_{gs}+C_{gd})-2)(\omega^2(C_{gs}+C_{gd})^2+g_m(1+n)^2)}{g_m^3 R_{src}(1+n)^2}$$

$$\frac{\partial F}{\partial L_{src}} = 0$$

$$\rightarrow L_{src,opt,NF} \approx \frac{2}{\omega^2(C_{gs}+C_{gd})}$$

The same can be done for R_{src}. If L_{src} is chosen to have this optimal value for noise, the resulting optimal value for R_{src} is as follows:

$$\rightarrow R_{src,opt,NF} \approx \frac{2}{\sqrt{\gamma}}\cdot\frac{g_m(1+n)\sqrt{g_m R_g}}{\omega(C_{gd}+C_{gs})\sqrt{\omega^2(C_{gd}+C_{gs})^2+g_m^2(1+n)^2}}$$

$$R_{src,opt,NF} \approx 2\frac{\omega_t}{\omega}(1+n)\cdot\sqrt{\frac{g_m R_g}{\gamma g_m^2\frac{\omega^2}{\omega_t^2}+\gamma g_m^2(1+n)^2}}$$

$$R_{src,opt,NF} \approx 2\frac{\omega_t}{\omega}(1+n)\cdot\sqrt{\frac{R_g}{\gamma g_m\left(\frac{\omega^2}{\omega_t^2}+(1+n)^2\right)}}$$

Because $\omega \approx \omega_t/2$ for 60 GHz in CMOS 65 nm, the optimal source resistance is approximately equal to:

$$R_{src,opt,NF} \approx 4(1+n) \cdot \sqrt{\frac{R_g}{\gamma g_m\left(\frac{1}{4}+(1+n)^2\right)}}$$

$$R_{src,opt,NF} \approx 4\sqrt{\frac{R_g}{\gamma g_m}}$$

If R_g becomes small, $R_{src,opt,NF}$ also becomes small. The resulting noise figure with $Z_{src,opt,NF}$ is as follows:

$$F_{min} \approx \frac{2\sqrt{\frac{R_g\gamma}{g_m}}\omega(C_{gd}+C_{gs}) \cdot \sqrt{\omega^2(C_{gd}+C_{gs})^2 + g_m^2(1+n)^2} + g_m(1+n)}{g_m(1+n)}$$

If the dependence of the various transistor parameters are seen proportional of transistor width W, the resulting dependence of the noise figure as a function of transistor width can be observed:

$$F_{min} \propto \frac{\sqrt{\frac{1/W}{W}}W \cdot \sqrt{W^2+W^2} + W}{W} = \frac{W+W}{W} = 1$$

So the minimum noise factor is independent of the chosen transistor width. A further approximation of the minimum noise figure can be given in the form:

$$F_{min} \approx \frac{2\sqrt{\frac{R_g\gamma}{g_m}}\omega(C_{gd}+C_{gs}) \cdot \sqrt{\omega^2+\omega_t^2(1+n)^2} + \omega_t(1+n)}{\omega_t(1+n)}$$

Because $\omega_t^2(1+n)^2 > \omega^2$, F_{min} is approximately equal to:

$$F_{min} \approx 1 + 2\sqrt{\frac{R_g\gamma}{g_m}} \cdot \omega(C_{gd}+C_{gs}) = 1 + 2\frac{\omega}{\omega_t} \cdot \sqrt{R_g\gamma g_m}$$

The resulting minimal noise figure at 60 GHz is approximately:

$$F_{min} \approx 1 + \sqrt{R_g\gamma g_m}$$

If R_g again becomes small, the minimal noise factor also becomes small.

Fully Balanced Low Noise Amplifier 58 - 64 GHz in CMOS 65 nm

Erwin J.G. Janssen

Eindhoven University of Technology
e.j.g.janssen@student.tue.nl

***Abstract*—The unlicensed band around 60 GHz enables gigabit communication. This paper describes the design, simulation and tape-out of a 60 GHz differential LNA. It makes use of a transformer for feedback and C_{gd} neutralization purposes. Therefore the characteristics of a transformer were investigated comparing calculations, simulations and measurements. To decide which topology to use, a comparison was made between a common gate and a common source topology, both using transformer feedback. The resulting LNA achieves simulated s_{21} of 10.7 dB with gain flatness of 0.2-0.3 dB, NF of 3.6-3.8 dB, IIP_3 of 4 dBm and 1 dB_c of -9.8 dBm, while consuming 35 mW at 1.2 V.**

I. Introduction

The increasing demand for higher data rate in RF communication links requires the use of more bandwidth. Around 60 GHz, 6 GHz of unlicensed bandwidth is available which enables data rates of several gigabits per second. To implement such systems, modern CMOS technology is interesting because of its promise to use digital signal processing combined with RF front end electronics. This enables the integration of a full system on chip. Several problems have to be conquered to succeed this challenge.

In order to achieve the required 6 GHz bandwidth ($\approx$ 9.8 %) for the LNA, feedback must be applied. At these high frequencies the use of coupled structures such as transformers to apply this feedback become interesting because of their low noise contribution, low DC-voltage drop and because their dimensions are not such a big issue anymore. To investigate the performance of such a device on chip, a transformer was designed, taped out and measured for verification.

Another difficulty is the fact that modern CMOS technologies operate at low supply voltages making the use of several cascoded MOSTs difficult. Therefore solutions must be found by using as little stacked devices as possible.

Then there are also the numerous parasitic effects that have to be taken into account in order to model the behavior of the system correctly. To implement the LNA, different active topologies were investigated (CS, CG) using both calculations and simulation, resulting in an implementation on chip.

In section II, different topologies are investigated after which a decision is made. In section III the modeling, simulation and design of transformers is addressed, resulting in the tape-out and measurement of a transformer on chip. In section IV the design of the LNA is discussed and in section V the impact of the layout on this design is explained. In section VI simulation results are reported. At the moment of this writing no measurement results of the LNA were available yet.

II. Topologies

In a literature search different topologies were investigated to implement a differential LNA at 60 GHz. Starting point for this search is the use of feedback to achieve high gain flatness. An interesting way of applying feedback at 60 GHz is making use of transformers. Applying feedback is possible over some different active topologies such as common gate and common source. First a comparison will be given for these two topologies. After this comparison several topologies using feedback will be investigated for the 60 GHz LNA. Eventually a decision will be made between the different topologies based on the noise, s_{21} and input impedance performance.

A. Common source

With the CS topology the source is connected to AC ground and the gate is connected to the signal source. To compare the topologies the voltage and current gain will be determined using the ABCD-parameters. Also the input impedance and noise factor will be calculated.

$$A^{-1} = \left.\frac{V_{out}}{V_{in}}\right|_{I_{out}=0} \approx \frac{sC_{gd} - g_m}{\frac{1}{R_{ds}} + sC_{gd}}$$

$$D^{-1} = \left.\frac{I_{out}}{I_{in}}\right|_{V_{out}=0} \approx \frac{sC_{gd} - g_m}{s(C_{gs} + C_{gd})}$$

Because $g_m > \frac{1}{R_{ds}}$, the CS topology has both voltage, and current gain bigger than one possible (up to a certain frequency). To calculate the noise factor F_{CS}, the noise generated in the transistor channel and the noise due to the gate resistance have been taken into account.

$$F_{CS} \approx 1 + \frac{R_g}{R_{src}} + \frac{\gamma}{g_m R_{src}}\left|1 + Z_{src}(sC_{gs} + sC_{gd})\right|^2$$

To minimize F_{CS}, Z_{src} must have a certain inductance $\rightarrow$ $Z_{src} = R_{src} + sL_{src}$. To determine the optimal value for L_{src}, the derivative is taken and made equal to zero. This results in the following optimal source inductance and F_{CS} (with $\omega_t = \frac{g_m}{C_{gs}+C_{gd}}$):

$$\frac{\partial F_{CS}}{\partial L_{src}} = 0 \rightarrow L_{src,opt,NF} = \frac{1}{\omega^2(C_{gs} + C_{gd})}$$

$$F_{CS} \approx 1 + \frac{R_g}{R_{src}} + \frac{\gamma\omega^2}{\omega_t^2} g_m R_{src}$$

As can be seen from this formula, maximizing ω_t lowers the noise factor. Therefore g_m must be maximized, at the cost of power consumption. Because $\omega/\omega_t \approx 1/2$ for 60 GHz in CMOS 65 nm (at optimal biasing):

$$F_{CS} \approx 1 + \frac{R_g}{R_{src}} + \frac{\gamma}{4} g_m R_{src}$$

To determine the optimal source resistance, again the derivative is taken (this time to R_{src}) and made equal to zero:

$$\frac{\partial F_{CS}}{\partial R_{src}} = 0 \rightarrow R_{src,opt,NF} \approx 2\sqrt{\frac{R_g}{\gamma g_m}}$$

$$\rightarrow F_{CS,min} \approx 1 + \sqrt{\gamma g_m R_g}$$

As can be seen the minimum noise factor becomes small for small R_g. Last feature to determine is the input impedance.

$$Z_{in} = R_g +$$

$$\frac{sC_{gd}(R_{ds}||Z_{load}) + 1}{s^2 C_{gd} C_{gs}(R_{ds}||Z_{load}) + sC_{gd}(g_m(R_{ds}||Z_{load}) + 1) + sC_{gs}}$$

As can be seen the effect of C_{gd} on the input impedance is being multiplied by $g_m(R_{ds}||Z_{load})$. This is the Miller effect. This also causes a path from the drain to the source (output to input). When the CS topology is used in an LNA, this signal path should be blocked to prevent instability. The Miller capacitance (C_m) is equal to $g_m(R_{ds}||Z_{load})C_{gd}$. If the effect of C_m is big, the input impedance converges to:

$$Z_{in} = R_g + \frac{1}{sC_{gs} + g_m}$$

On the other hand, if the effect of C_m is small, the input impedance converges to:

$$Z_{in} = R_g + \frac{1}{s(C_{gd} + C_{gs})}$$

So the input impedance will be between these extremes, depending on Z_{load}. The situation with little Miller effect has the same L_{src} for both power match and F_{min}.

B. Common gate

With the CG topology the gate of the MOST is connected to AC ground and the source is connected to the signal source. The same parameters are calculated for the CG as for the CS.

$$A^{-1} = \left.\frac{V_{out}}{V_{in}}\right|_{I_{out}=0} \approx \frac{g_m + \frac{1}{R_{ds}}}{sC_{gd} + \frac{1}{R_{ds}}}$$

$$D^{-1} = \left.\frac{I_{out}}{I_{in}}\right|_{V_{out}=0} \approx \frac{g_m + \frac{1}{R_{ds}}}{sC_{gs} + g_m + \frac{1}{R_{ds}}}$$

Because D^{-1} is always ≤ 1, the current gain of the CG topology is ≤ 1. Therefore only voltage gain is possible. F_{CG} including the MOST channel noise as well as the noise generated in R_g looks as follows (neglecting R_{ds}):

$$F_{CG} \approx 1 + \frac{R_g}{R_{src}}\left|\frac{g_m - sC_{gd}(sC_{gs}Z_{src} + g_m Z_{src} + 1)}{g_m}\right|^2 + \frac{\gamma g_m}{R_{src}}\left|\frac{1 + sZ_{src}C_{gs}}{g_m}\right|^2$$

If Z_{src} is formed with a resistive and an inductive part, again an inductance can be chosen to lower F_{CG}. To find the optimal value of L_{src}, the derivative of the noise factor is taken and made equal to zero.

$$\frac{\partial F_{CG}}{\partial L_{src}} = 0 \rightarrow$$

$$L_{src,opt,NF} \approx \frac{R_g C_{gd}(\omega^2 C_{gd} C_{gs} - g_m^2) + C_{gs}\gamma g_m}{\omega^2 R_g C_{gd}^2(\omega^2 C_{gs}^2 + g_m^2) + \omega^2 C_{gs}^2 \gamma g_m}$$

For small R_g, $L_{src,opt,NF} \rightarrow \frac{1}{\omega^2 C_{gs}}$. To find $R_{src,opt,NF}$, also the derivative is taken and made equal to zero:

$$\frac{\partial F_{CG}}{\partial R_{src}} = 0 \rightarrow$$

$$R_{src,opt,NF} \approx \frac{g_m^2}{2} \cdot \frac{\sqrt{\omega^2 R_g^2 C_{gd}^2 + R_g \gamma g_m}}{\omega^2 R_g C_{gd}^2(\omega^2 C_{gs}^2 + g_m^2) + \omega^2 C_{gs}^2 \gamma g_m}$$

The resulting F_{min} is approximately equal to:

$$F_{CG,min} \approx 1 + \omega R_g C_{gd} + 2\frac{\omega}{\omega_t} \cdot \sqrt{\omega^2 R_g^2 C_{gd}^2 + R_g \gamma g_m}$$

As can be seen from this formula, also for the common gate topology maximizing ω_t lowers the noise factor. Therefore g_m must be maximized, at the cost of power consumption. If realistic values are filled in at 60 GHz in CMOS 65 nm, $F_{CG,min}$ is approximately equal to:

$$\rightarrow F_{CG,min} \approx 1 + \sqrt{R_g \gamma g_m}$$

As can be seen the F_{min} becomes small for small R_g. Next feature is the input impedance. If Z_{load} is assumed small (which is the case when using a cascode), the input impedance ($= R_{in} + sX_{in}$) is approximately:

$$R_{in} \approx \frac{g_m + \frac{1}{R_{ds}}}{(g_m + \frac{1}{R_{ds}})^2 + \omega^2 C_{gs}^2} \approx \frac{g_m}{g_m^2 + \omega^2 C_{gs}^2}$$

$$X_{in} \approx \frac{-\omega C_{gs}}{(g_m + \frac{1}{R_{ds}})^2 + \omega^2 C_{gs}^2} \approx \frac{-\omega C_{gs}}{g_m^2 + \omega^2 C_{gs}^2}$$

This input impedance is an important feature of the CG topology. It gives the designer the freedom to choose an input impedance by setting the biasing of the MOST. By doing this, matching between the LNA and the antenna can be provided.

$$L_{src,match} = \frac{C_{gs}}{g_m^2 + \omega^2 C_{gs}^2} \neq L_{src,NF}$$

As can be seen there is a tradeoff between the optimal inductance concerning noise performance and input match.

C. Discussion CS - CG

As shown in sections II-A and II-B the F_{min} and voltage gain of both topologies are approximately equal:

$$F_{CS,min} \approx F_{CG,min} \approx 1 + \sqrt{R_g \gamma g_m}$$

$$A_{CS}^{-1} \approx A_{CG}^{-1} \approx \frac{g_m + \frac{1}{R_{ds}}}{sC_{gd} + \frac{1}{R_{ds}}}$$

Main disadvantage of the CS stage is the presence of the Miller effect. This has to be blocked, what will result in an input resistance equal to R_g, which is usually small and results in a high Q input (feedback can change this). Main disadvantage of the CG stage is the current gain ≤ 1. This results in a higher noise contribution of the next stage in the LNA, and thereby deteriorating the overall noise performance.

D. G_m-boosted common gate

The first topology discussed as a candidate for the 60 GHz LNA is the g_m-boosted CG LNA. For the active part this topology makes use of a CG stage. As seen in the previous part this has as an advantage that there is an easy way of providing a wideband input match. After applying this, the biasing of the transistor is set to a certain value resulting in a certain noise figure. When using g_m-boosting, a lower noise figure can be achieved with the common gate stage while still maintaining the input match criterion [1]. The schematic of the g_m-boosted CG LNA is shown in figure 1.

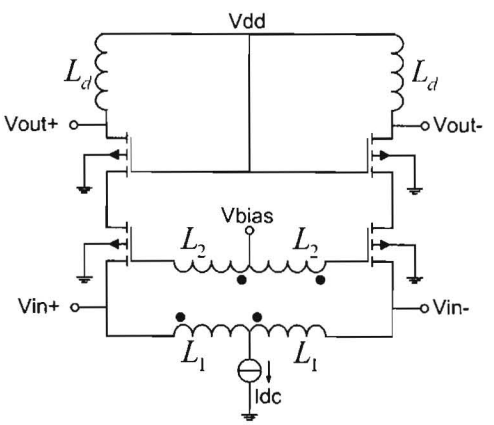


Fig. 1. G_m-boosted common gate LNA. The left combination of L_1 and L_2 forms a transformer as well as the right combination. The CG input stage is followed by another CG stage, so a cascode. This is done to increase the output impedance and it increases output isolation. Because the common gate topology only gives voltage gain, the output impedance must be high to provide enough gain. The biasing of the transistors is done at the inductors.

1) Input impedance: To calculate the input impedance the small signal circuit shown in figure 2 is used. An ideal cascode is assumed, so $Z_{load} = 0$. The input impedance with C_{gd}, R_g and R_{ds} neglected looks as follows (for high coupling):

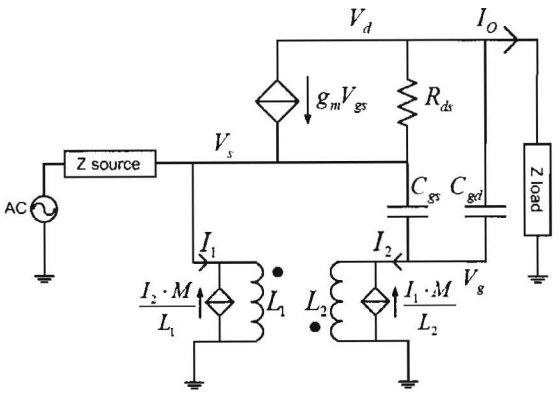


Fig. 2. Small signal equivalent circuit of the g_m-boosted common gate LNA (single ended). Z_{load} models the next stage, so the cascode MOST.

$$Z_{in} \approx \frac{2}{sC_{gs}(1+n)^2 + g_m(1+n) + \frac{1}{sL_1}}$$

$$\rightarrow L_1 = \frac{1}{\omega^2 C_{gs}(1+n)^2}$$

$$Z_{in} \approx \frac{2}{g_m(1+n)}$$

As can be seen from this formula, $Re[Z_{in}]$ of the g_m-boosted CG LNA is approximately lowered by a factor of $\frac{1}{1+n}$ in comparison of the conventional CG stage. This is due to the amplification between the source and gate.

2) Noise factor: If L_1 is chosen equal to the value determined in section II-D1, the noise factor looks as follows (with R_{ds} neglected and $k \rightarrow -1$):

$$F_{g_m-boosted} \approx 1 + \frac{2R_g}{(1+n)^2 R_{src}} \left|1 + \frac{Z_{src}}{2sL_1}\right|^2 + \frac{2\gamma}{g_m(1+n)^2 R_{src}}$$

As can be seen the noise factor can be lowered by increasing g_m, n and R_{src}, and lowering R_g. If the noise due to R_g is neglected and R_{src} is chosen to match the real part of the input impedance, the noise factor for the g_m-boosted CG LNA looks as follows:

$$F_{g_m-boosted} \approx 1 + \frac{\gamma}{1+n}$$

As can be seen from this formula, for high transformer coupling the noise factor is lowered by $(1+n)$. This formula suggests the noise factor can be made arbitrarily low by increasing n. This is not true because there are also other noise sources present in the LNA such as the induced gate noise [1]. Also the presence of the cascode transistor will deteriorate the noise figure. The noise figure will therefore be higher in reality and n will have a certain optimum. Simulations have been used to determine the exact value of F and optimal n.

3) Voltage gain: To determine the voltage gain, R_{ds} and C_{gd} are disconnected from the drain and connected to ground to model the cascode. Resulting voltage gain is as follows:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{g_m Z_{load}(s^2(1-k^2)L_2C_{gd} + 1 - kn)}{s^2(1-k^2)L_2(C_{gd}+C_{gs}) + 1}$$

$$\rightarrow L_1 = \frac{L_2}{n^2} = \frac{1}{\omega^2 n^2 (1-k^2)(C_{gd}+C_{gs})}$$

If L_1 is chosen as indicated, the voltage gain is maximal. This is a different value as for lowering NF. There is a notch in the transfer for $\omega = \frac{1-kn}{(1-k^2)L_2C_{gd}}$. Operation around this point should be prevented. If $k \rightarrow -1$, A_v converges to:

$$A_v = \frac{V_{out}}{V_{in}} = g_m(1+n)Z_{load}$$

E. Voltage-voltage transformer feedback LNA

The second topology discussed as a candidate for the implementation of the 60 GHz LNA is the voltage-voltage transformer feedback LNA (see figure 3). This topology uses a CS MOST as an active part. Advantage of a CS is the combination of high voltage and current gain. Disadvantage is the signal path from output to input through C_{gd}. By using the voltage-voltage transformer feedback LNA topology this is blocked without the use of the conventional cascode, increasing voltage headroom for the MOST and lowering F.

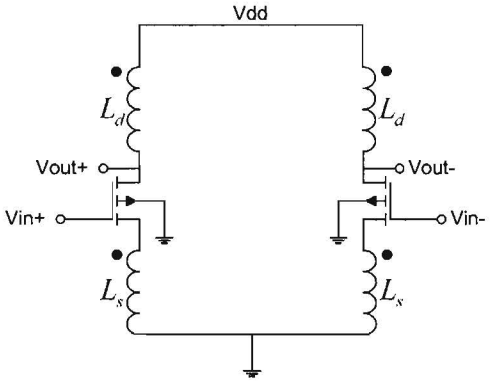


Fig. 3. Voltage voltage transformer feedback LNA. The left combination of L_d and L_s forms a transformer as well as the right combination.

1) Output isolation: The small signal equivalent circuit of the V-V transformer feedback LNA is shown in figure 4. To apply output isolation, the transformer can be used [3]. The transfer function $\frac{V_g}{V_{out}}$ of the circuit is calculated using the half circuit concept and looks as follows for low frequencies:

$$\lim_{s\rightarrow 0} \frac{V_g}{V_{out}} = \frac{C_{gd} + \frac{k}{n}C_{gs}}{C_{gd}+C_{gs}}$$

$$\frac{V_g}{V_{out}} = 0 \rightarrow \frac{n}{k} = -\frac{C_{gs}}{C_{gd}}$$

The magnitude of V_g versus V_{out} is shown in figure 5.

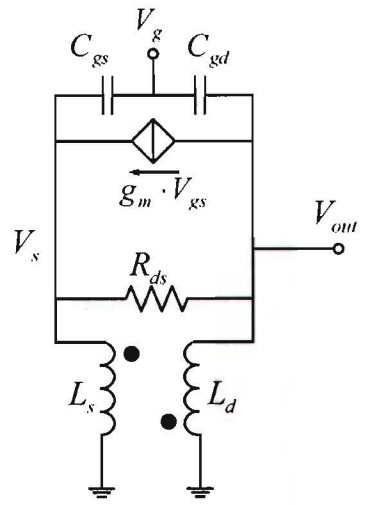


Fig. 4. Lumped element model of the V-V transformer feedback topology (single ended). The output signal at the drain (V_{out}) is connected via C_{gd} to V_g. The transformer copies V_{out} to V_s, which is connected to V_g through C_{gs}. This way the output signal can be canceled at V_g.

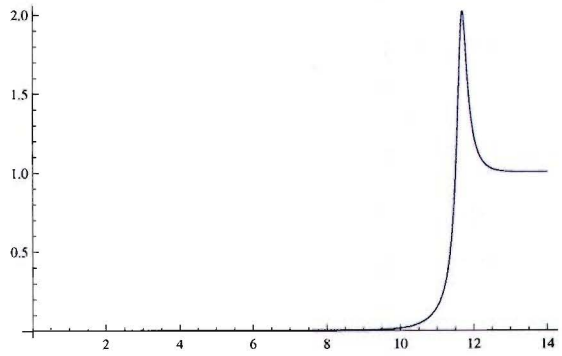


Fig. 5. Magnitude response $\frac{V_g}{V_{out}}$ with $\frac{n}{k} \approx -\frac{C_{gs}}{C_{gd}} \approx -3$ ($n = 2$, $k = -0.667$ and $L_s = 30pH$). A 30 μm MOST has been used. The horizontal axis shows the frequency on a logarithmic scale. There is good output isolation for frequencies below 1-10 GHz. For frequencies from 10-200 GHz the output isolation becomes worse. Above 200 GHz there is no isolation anymore under the given circumstances, but because the used MOST model is not valid anymore at these high frequencies, these results cannot be trusted.

2) Voltage gain: The voltage gain for high coupling with R_{ds} neglected and $\frac{n}{k} = -\frac{C_{gs}}{C_{gd}}$ is equal to:

$$A_v = \frac{V_{out}}{V_{in}} \approx \frac{-g_m n(1+n)}{sn^2C_{gd} + sC_{gs} + g_m(1+n) + \frac{1}{sL_s}}$$

$$\rightarrow L_s = \frac{1}{\omega^2(n^2C_{gd} + C_{gs})}$$

If L_s is chosen this value, A_v becomes maximal and equal to n. So to have high A_v, n should be high.

3) Input impedance: If L_s is chosen the value for maximal voltage gain and $\frac{n}{k} = -\frac{C_{gs}}{C_{gd}}$, Z_{in} for high coupling and neglecting R_{ds} looks as follows:

$$Z_{in} \approx 2R_g + \frac{2}{j\omega C_{gd}(1+n)}$$

So the input resistance is $\approx 2R_g$. Simulations show that for a coupling smaller then one, the input resistance can become negative for $-\frac{n}{k} > \frac{C_{gs}}{C_{gd}}$. This should be prevented, because a negative input resistance can result in instability.

4) Noise factor: The noise factor looks as follows (with $Z_{src} = R_{src} + sL_{src}$):

$$F_{VVfeedback} \approx 1 + 2\frac{R_g}{R_{src}} + 2\frac{\gamma g_m}{R_{src}}\left|\left(\frac{s(C_{gs}+C_{gd})}{g_m^2(1+n)} - \frac{1}{g_m}\right)\right.$$
$$\left. + \frac{R_{src}+sL_{src}}{2}\cdot\left(\frac{s^2(C_{gs}+C_{gd})^2}{g_m^2(1+n)} - \frac{s(C_{gs}+C_{gd})}{g_m}\right)\right|^2$$

If L_{src} is chosen to have the following inductance, the noise factor is minimized:

$$L_{src,opt,NF} = \frac{2}{\omega^2(C_{gs}+C_{gd})} \approx L_{src,match}$$

$R_{src,opt,NF}$ is given in the following equation:

$$R_{src,opt,NF} \approx 4\sqrt{\frac{R_g}{\gamma g_m}} \neq R_{src,match} = 2R_g$$

If R_g becomes small, $R_{src,opt,NF}$ also becomes small. The resulting noise factor with $Z_{src,opt,NF}$ is as follows:

$$F_{min} \approx 1 + \frac{2\omega}{\omega_t}\cdot\sqrt{R_g\gamma g_m},\ @\ 60\ \text{GHz} \rightarrow \approx 1 + \sqrt{R_g\gamma g_m}$$

When a power match is created ($R_{src} = 2R_g$, $L_{src} = L_{src,match}$), the noise factor looks as follows:

$$F_{match} \approx 2 + \frac{\gamma\omega^2 g_m R_g}{\omega_t^2}\left(1 + \frac{\omega^2}{\omega_t^2(1+n)^2}\right) \approx 2$$

So when a power match is applied a noise figure of at least 3dB can be achieved.

F. Discussion g_m-boosted CG vs. V-V transformer FB LNA

To make a decision which topology to choose, they will be compared using the calculations and simulations. A choice will be made based on noise and gain performance and the input impedance. Because the calculations are not as accurate as the models used in circuit simulator Cadence, simulations were performed for the different topologies. The voltage-voltage transformer feedback topology was simulated with and without the use of a cascode. By using a cascode there is output isolation available due to the CG after the CS stage, so there is more freedom in choosing n and k. This assures a higher output impedance enabling higher gain. Because of the use of an extra active stage the noise performance is expected to be worse. Simulations were performed for each circuit in a short period and gave the following results:

	G_m-boost.	V-V FB	V-V FB (casc.)
Gain	7.5 dB	6 dB	10 dB
NF	7 dB	3 dB	6.5 dB

The gain of the V-V transformer FB topology with cascode is highest and the gain of the V-V transformer FB LNA without cascode is worst, but it has a very low noise figure, all as expected. The g_m-boosted CG has the worst noise performance, but higher gain than the V-V transformer feedback LNA without cascode. Based on these observations a choice was made to continue with the V-V transformer feedback LNA without cascode and use two stages to achieve enough gain.

III. Transformers

Every topology of interest for the implementation of the 60 GHz LNA makes use of a transformer for feedback purposes. Therefore a study was done on the behavior and modeling of the transformer, and its physical limitations in the CMOS 65 nm technology. First calculations are performed, and after that EM simulations are done to see the impact of the various parasitics. Also a single transformer has been taped-out to measure the transformer parameters and verify with the calculations and simulations.

A. Transformer model using parasitics

To model the behavior of the transformer, the schematic as seen in figure 6 has been used.

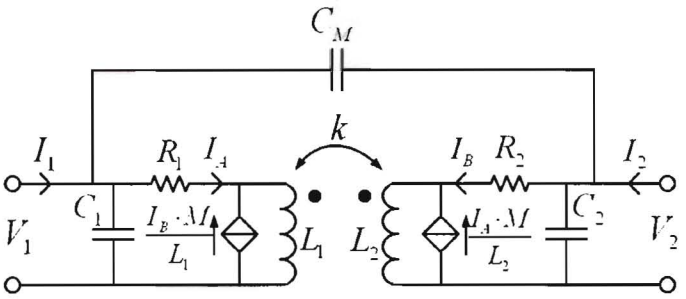


Fig. 6. Transformer circuit with parasitics. $M = k\sqrt{L_1 L_2}$, k = coupling factor [2].

1) Transfer function: The transfer function of this schematic looks as follows (with the resistances neglected and $L_2 = n^2 L_1$):

$$\left.\frac{V_2}{V_1}\right|_{I_2=0} = \frac{s^2(1-k^2)L_2C_m + kn}{s^2(1-k^2)L_2(C_2+C_m)+1}$$

In which n denotes the winding ratio of L_1 and L_2 [2]. If the parasitic capacitors are neglected, the transfer function converges to kn. As can be seen the transfer function has a double zero due to the interwinding capacitance C_m. This zero results in a notch only for positive coupling and is situated at the following frequency:

$$f_{notch} = \frac{1}{2\pi}\sqrt{\frac{kn}{(1-k^2)L_2C_m}}$$

There occurs a resonance resulting in maximum voltage gain at the following frequency:

$$f = \frac{1}{2\pi\sqrt{(1-k^2)L_2(C_2+C_m)}}$$

The transfer function for positive and negative coupling is given in figure 7.

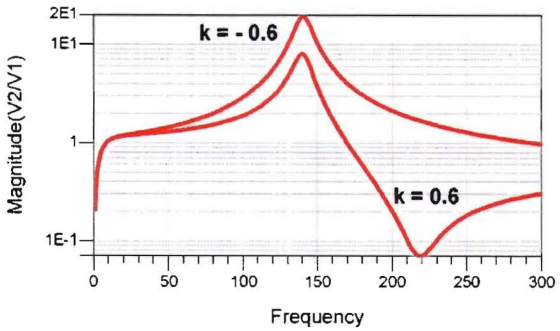


Fig. 7. Transfer function of a transformer with positive and negative coupling. As expected the resonance is independent of the sign of the coupling, but only for positive coupling a notch occurs. Values used: L_1 = 25 pH, L_2 = 100 pH, R_1 = 0.9 Ω, R_2 = 3.7 Ω, C_1 = 2.5 fF, C_2 = 10 fF and C_m = 10 fF.

2) Input impedance: Z_{in} for high positive and negative coupling looks as follows (with resistances neglected):

$$\lim_{k\to 1} Z_{in}|_{I_2=0} = \frac{sL_1}{s^2L_1C_1 + s^2L_2C_2 + s^2(1-n)^2L_1C_m + 1}$$

$$\lim_{k\to -1} Z_{in}|_{I_2=0} = \frac{sL_1}{s^2L_1C_1 + s^2L_2C_2 + s^2(1+n)^2L_1C_m + 1}$$

For low frequencies the input impedance behaves as an inductance, and for high frequencies as a capacitor. There occurs a resonance at the following frequency:

$$\rightarrow \lim_{k\to 1} f_{res} = \frac{1}{2\pi\sqrt{L_1C_1 + L_2C_2 + (1-n)^2L_1C_m}}$$

$$\rightarrow \lim_{k\to -1} f_{res} = \frac{1}{2\pi\sqrt{L_1C_1 + L_2C_2 + (1+n)^2L_1C_m}}$$

In the case of negative coupling there is a lower resonance frequency concerning input impedance due to C_m compared to positive coupling. If the effect due to C_m is made negligible, the resonance frequency converges to $\frac{1}{2\pi\sqrt{L_1C_1+L_2C_2}}$. For an inductor on chip the parasitics scale approximately with the inductance value, so the biggest inductor has the highest value of both L and C. This results in approximately the following resonance frequency for $n > 1$ and small C_m:

$$\rightarrow f_{res} \approx \frac{1}{2\pi\sqrt{L_{big}C_{big}}}$$

With L and C of the biggest inductor. So the unloaded resonance frequency of both inductors with high mutual coupling is dictated by the biggest inductor. The inductance seen at the input of the given transformer, is shown in figure 8 for positive and negative coupling using the same values as for figure 7.

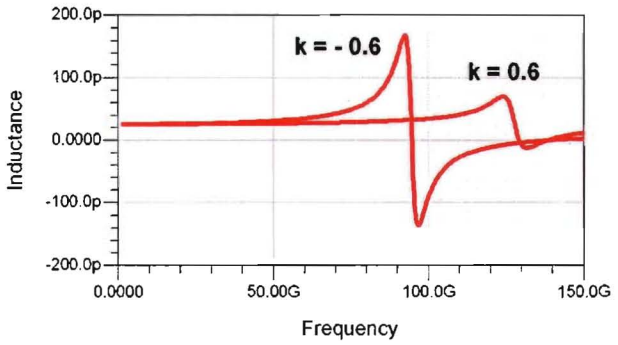


Fig. 8. Inductance seen at the input of a transformer with positive and negative coupling. It can be seen the case with negative coupling has the lowest resonance frequency for the input impedance.

B. Design of a transformer

Main design goals for a transformer are the primary and secondary inductances, the Q-factors and resonance frequencies of both inductors, and the mutual coupling. The transformer has to be implemented on chip, so metal thickness and distance between metal layers are fixed and certain design rules have to be obeyed. Remaining design variables are which metals to use, metal line width and the structure. Because the highest metals are the thickest available and have lowest coupling with the substrate, these layers have been chosen.

To choose the metal width, simulations with a top metal line (length = 10 μm) are performed varying the line width resulting in a certain inductance, capacitance and resistance per unit length. Because the following relation holds, the amount of inductance is linked to the amount of capacitance assuming a lossless situation (L in H/m and C in F/m, v_p = phase velocity = constant [4]).

$$v_p = \frac{1}{\sqrt{LC}} \rightarrow L = \frac{1}{v_p^2 C}$$

So if high capacitance per unit length is created, low inductance per unit length results. This is also what simulations show. High capacitance is created when a wide metal line width is chosen, so to achieve high inductance with little parasitic capacitance (high f_{res}), a small line width is preferred. On the other hand, a small line width results in high resistance per unit length, so deteriorates the Q-factor. To see the trade-off between f_{res} and Q-factor they were determined for an inductance of 70 pH, see figure 9.

Last feature is the structure. The transformer needed for the implementation of the LNA should have (high) negative coupling. For low coupling, the two inductors should be placed far apart. On the other hand for high coupling, the inductors should be placed as close as possible. An interesting way of providing high coupling is to use two metal layers exactly underneath each other. This way there is very little distance so there will be high coupling, but C_m will be high. Simulations gave max. coupling factors of approximately 0.8, so k varies from 0 to 0.8 (or from 0 to -0.8 for negative coupling). In figure

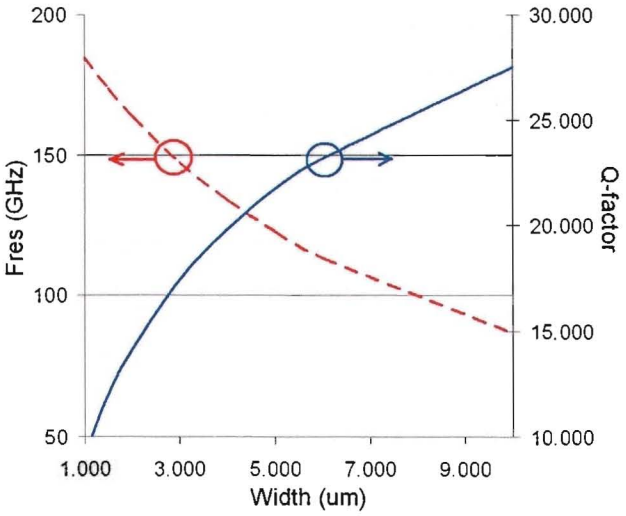


Fig. 9. Resonance frequency and Q-factor of an inductor of 70 pH as a function of metal width. A choice was made based on these observations to use a metal width of 3-4 μm.

10 it is explained how the transformer should be connected to have positive or negative coupling.

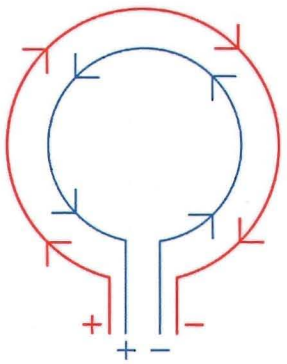


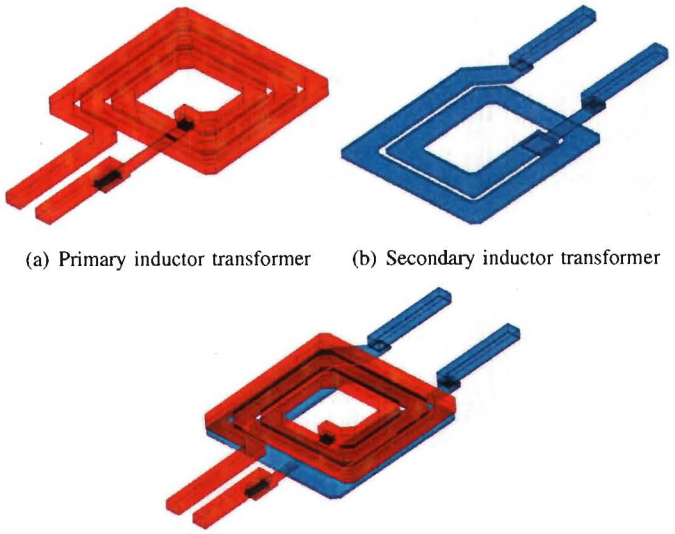
Fig. 10. If the outer inductor is exited, a current flow from the positive potential to the negative will result. This will result in a current flow in the inner inductor as well, but in the opposite direction. The voltage induced will be as shown in the figure. If both inductors are connected to ground at the same side, a transformer with positive coupling results. On the other hand, if the outer inductor is connected to ground on one side, and the inner inductor is connected to ground on the other side, negative coupling results.

C. Single transformer tape-out

To verify the behavior of a transformer on chip with simulation results in EM simulator ADS Momentum, a transformer was designed and taped out, using the design plan discussed in section III-B. The resulting structure is shown in figures 11(a), 11(b) and 11(c).

1) Simulation: The simulation results for inductance and Q-factor are shown in figures 12 and 13. The simulated coupling factor at 20 GHz is approximately 0.7.

2) Layout: The layout of the transformer is shown in figure 14. The used waveguides have a characteristic impedance of 50 Ω, because the measurement setup is also at 50 Ω (100 Ω diff.). The influence of the waveguides and bondpads on the measurement can not be simulated in ADS Momentum along because of memory reasons. So to be able to measure



(a) Primary inductor transformer (b) Secondary inductor transformer

(c) Complete transformer structure

Fig. 11. Transformer taped out for verification EM simulation vs. reality. To have $n \approx 1.5$ the primary inductor has three turns and the secondary has two turns. To have high coupling the two inductors are placed exactly on top of each other.

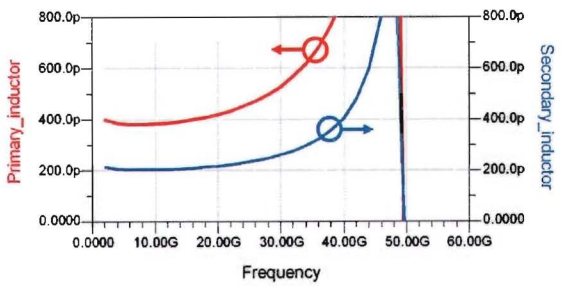


Fig. 12. Simulated inductances. L_p is approximately 400 pH and L_s is approximately 200 pH for low frequencies. Because of the resonance ($f_{res} \approx$ 50 GHz) the inductor values increase for frequencies 20-50 GHz. Above f_{res} the structure behaves capacitive.

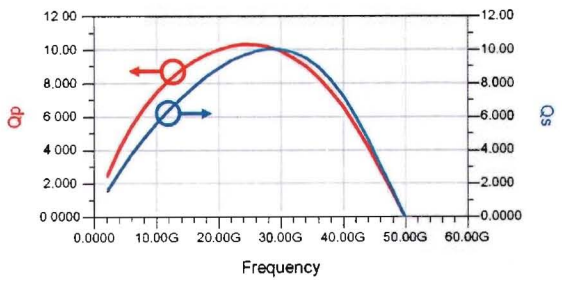


Fig. 13. Simulated Quality factors. The Q-factor is defined as $\frac{Im[Z]}{Re[Z]}$. For low frequencies $Im[Z]$ increases linearly with f and $Re[Z]$ stays approximately constant, so the Q-factor also increases linearly with f. But for higher frequencies $Im[Z]$ becomes negative (capacitive behavior), the lines go down again. In fact $Re[Z]$ also increases a little bit due to the skin effect but this does not go as fast as the $Im[Z]$.

the transformer solely, also de-embedding structures have been included. Three structures were prepared, one with the CPWs left open, one with the CPWs shorted, and one with a line connecting the top bondpads with the bottom bondpads. Because of area reasons only the open and short structures were taped out, resulting in less reliability for the de-embedding at high frequencies because of the missing line structure.

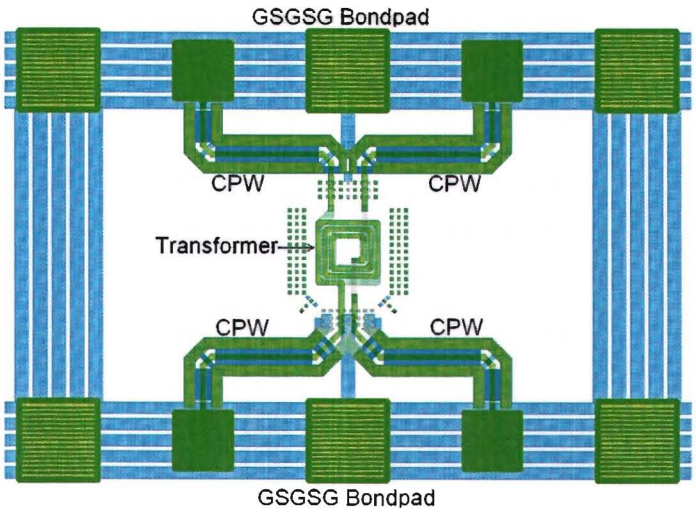


Fig. 14. Layout of the transformer. As can be seen the transformer is in the center. The metal dots next to the transformer are there to fulfill the metal density rules of the TSMC process. The transformer is connected to the GSGSG (G = ground, S = signal) bondpads on the top and bottom by using coplanar waveguides.

3) Measurement: The transformer was taped out in August 2007 and was measured several months later. The measurement was performed for 10 - 40 GHz. The measurements above this frequency range were very difficult (if not impossible) due to the missing de-embedding structure. The measured coupling at 20 GHz is approximately 0.67. The measurement results concerning inductance are shown in figure 15.

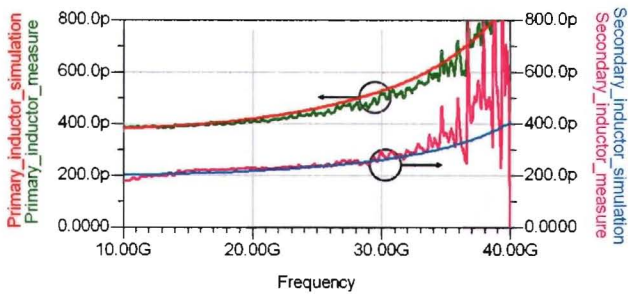


Fig. 15. Measured and simulated inductances. As can be seen the results are quite similar to the simulation. Biggest deviation is observed for the high frequency behavior of the secondary inductance.

In the following table the measured values are compared with the simulated values, for low frequencies:

Parameter	Simulation	Measurement
L_p	$\approx$ 385 pH	$\approx$ 385 pH
L_s	$\approx$ 200 pH	$\approx$ 200 pH
Coupling	$\approx$ 0.7	$\approx$ 0.67

The inductances are approximately the same, but simulations give little more coupling than seen in reality.

IV. Design V-V feedback LNA

To design the LNA, circuit level simulations were performed in Cadence using the PSP MOST model, and EM simulations for various passive devices. Design goal used is maximizing the space between the NF and s_{21} parameter. Next the IIP_3 performance is determined. Then a choice was made looking at the possibility of the design in reality.

A. Single stage design

1) Starting point based on calculations: From calculations the initial values for the different components have been determined:

$$L_s = \frac{1}{\omega^2(n^2 C_{gd} + C_{gs})}$$

If L_g is chosen as follows, there is both input match and optimal noise performance:

$$L_{g,match} \approx \frac{1}{\omega^2 C_{gd}(1+n)} \approx \frac{1}{\omega^2(C_{gs}+C_{gd})} = L_{g,opt,NF}$$

These values will differ from the values to be used in Cadence because the models used are much simpler than the models Cadence uses. To provide output isolation the following statement should hold:

$$\frac{n}{k} = -\frac{C_{gs}}{C_{gd}}$$

To have high gain, n should be high, so also k should be high.

2) Noise figure and s_{21}: During simulations, lower optimal values for L_s and L_g were found. Reason for this are the extra parasitics (capacitors) in the components. After several simulations the exact component values including parasitics were determined to give maximal performance. These gave the performance shown in figure 16.

3) IIP_3 and 1 dB_c: Next, simulations were performed for IIP_3 and 1 dB_c. These are shown in figures 17 and 18.

4) In and output impedances: To tune out the imaginary part of the input impedance two inductors equal to L_g are used. This sets the center frequency of the pass-band of the LNA. The real part of the input impedance is approximately equal to $2R_g$. To maximize s_{21}, $R_{src} = R_{in} \approx 2R_g \neq R_{src,opt,NF}$. Therefore a tradeoff has to be applied for this (see figure 19).

The simulated output impedance has a real part that lies above the real part of the input impedance. The imaginary part behaves inductive, and can thus be canceled using a shunt C. This capacitor value is in the order of magnitude of the parasitic capacitance of the transformer, so if chosen correctly it can be omitted.

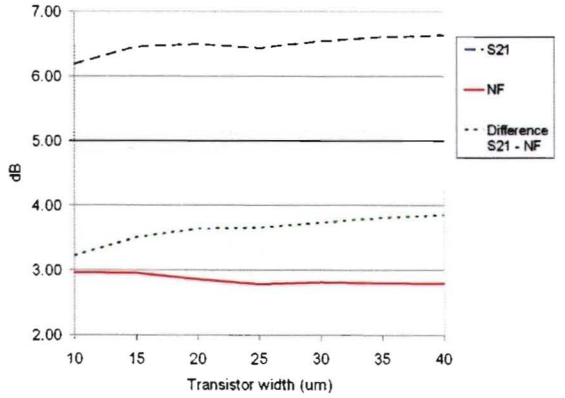


Fig. 16. Simulation results of s_{21} and NF versus MOST width using a transformer with n = 1.81 and k = -0.7 to -0.8. The circuit has two MOSTs with equal W. Performance changes little, but big W gives better results. On the other hand a big W consumes more power for a certain bias current density through the channel. So concerning NF and gain every W can be chosen, if component feasibility is not taken into account.

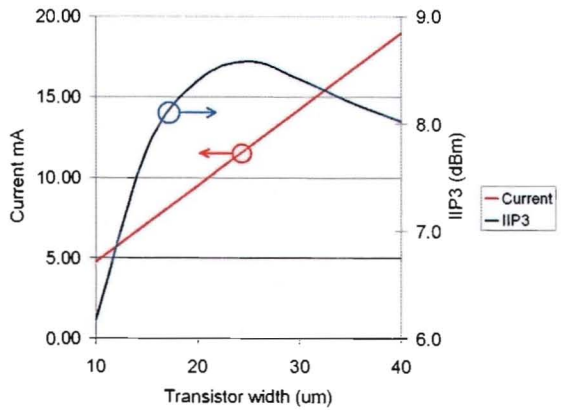


Fig. 17. Simulation results of IIP_3 and DC current consumption versus MOST width. Maximum IIP_3 is achieved using a transistor W of 20 - 30 μm.

B. Dual stage design

To achieve enough gain, more stages are needed. One stage gives a s_{21} of approximately 6.5 dB, so ideally two stages provide approximately 13 dB. The overall NF is dominated by the first stage. The second stage is dominant concerning IIP_3. So the first stage will be optimized for NF and s_{21}, and the second stage for IIP_3 and gain. Simulations showed little difference concerning NF varying W_1 and W_2, so concerning NF every combination can be chosen. Simulation results concerning s_{21} are given in figure 20 for two stages cascaded. After the gain and noise performance, linearity is investigated. IIP_3 and 1 dB_c show the same trend. In figure 21 the behavior is shown.

A choice was made to have $W_1 > W_2$, because of the higher gain. Taking feasibility of the components into account, a maximum inductor of $\approx$ 150 pH is found concerning f_{res}. The biggest inductor in the design is L_g, and because $W_1 > W_2$, $L_{g2} > L_{g1}$. This results in $W_{min} \approx 25\ \mu\text{m} = W_2$.

The biggest value of W is given by the minimal L_s possible.

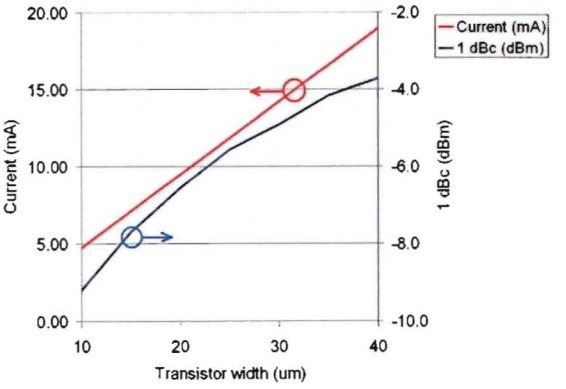


Fig. 18. Simulation results of 1 dB_c and DC current consumption versus MOST width. The 1 dB_c increases with transistor width. This can be explained from the fact that the big transistor uses lower impedance levels to operate optimal, so it can generate higher output current levels, while maintaining the same voltage levels. On the other hand a higher 1 dB_c takes a higher power consumption.

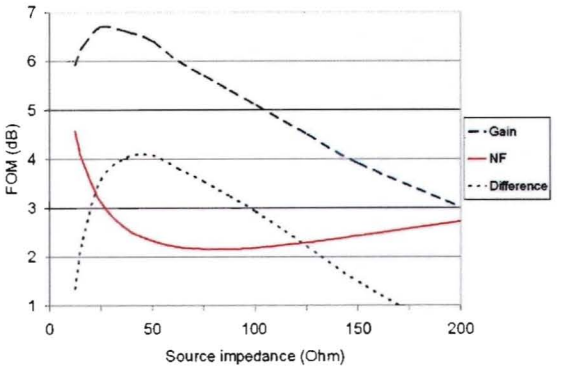


Fig. 19. NF, s_{21} and the difference between them versus source impedance ($W_{MOST} = 30\mu$m).

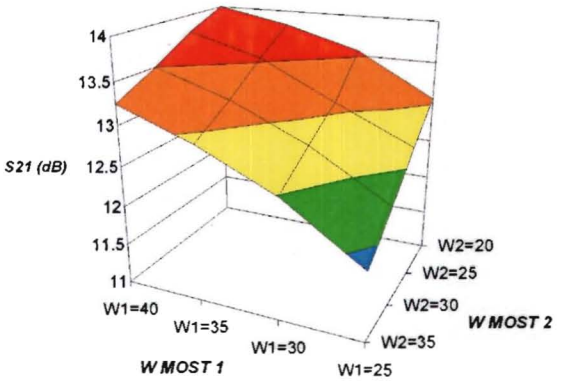


Fig. 20. s_{21} versus MOST 1 width (first stage) and MOST 2 width (second stage), both in μm. s_{21} is maximal for $W_1 > W_2$. This is because $R_{out,1} > R_{in,2}$ if $W_1 = W_2$. To have high gain, it is desirable to have $R_{out,1} \leq R_{in,2}$. This is achieved with a wide transistor in the input stage and a small transistor in the second stage.

This value was found to be $\approx$ 30 pH during simulations in Momentum. Therefore $W_{max} \approx 35\ \mu$m. Also big W gives high power consumption and will give rise to problems with

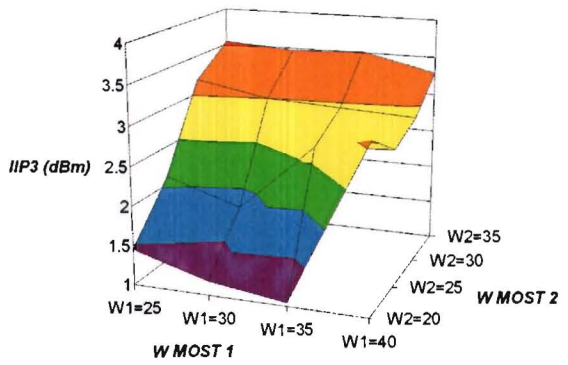


Fig. 21. IIP_3 versus W_1 and W_2, both in μm. As expected the best performance concerning linearity is found for a wide transistor in the second stage.

the electro-migration of the metal. So $W_1 = 35\ \mu\text{m} > W_2 = 25\ \mu\text{m}$. The resulting schematic is shown in figure 22.

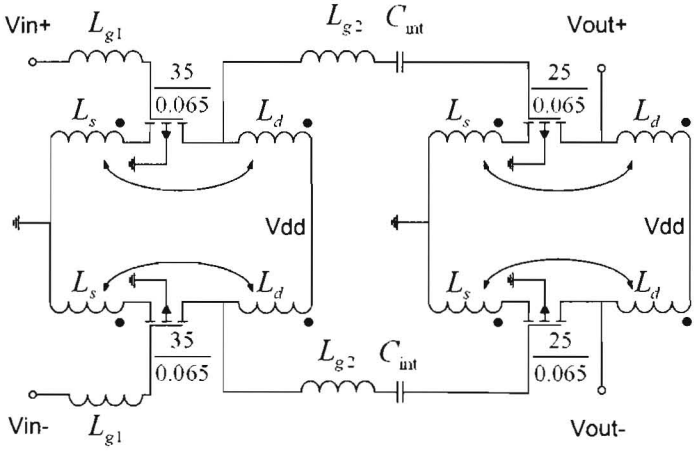


Fig. 22. Two stage design without biasing and CMR resistance. To connect both stages C_{int} has been used to enable different DC-voltages.

C. Transformer implemented LNA

Next a transformer for the LNA will be designed. This transformer has to be implemented in a slight different stack used in section III-C. First design goal is stated by the output isolation requirement $\frac{n}{k} = -\frac{C_{gs}}{C_{gd}}$ which is approximately 2.25 in the used technology. Design goals concerning inductance and Q-factor have been set using circuit simulations in Cadence. To design the transformer again the same procedure is followed as in section III-B. Resulting structure is shown in figure 23.

To be able to do s-parameter simulations in Cadence using this transformer model, a s-parameter dataset is generated in Momentum and imported in Cadence. Therefore a very wideband simulation was done from 8 MHz to 300 GHz. This is done to include frequency dependent behavior to determine for example the stability. For DC-resistance a low frequency simulation is needed because of the skin effect (8 MHz).

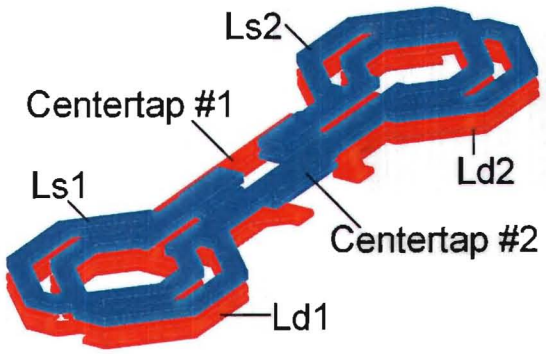


Fig. 23. Structure with on top two times L_s and below two times L_d. The primary inductor has two turns and the secondary has one turn, in combination with the parallel connections this results in a $n \approx 1.7$ ($L_p \approx 90$ pH, $L_s \approx 30$ pH). To have high coupling the two inductors are placed exactly on top of each other also resulting in high interwinding capacitance C_m. Therefore the match capacitance needed at the output can be omitted as will be discussed in section IV-A4. Q-factors are $Q_p \approx 11$ and $Q_s \approx 10$. Simulated coupling is ≈ -0.75. Also visible are the 2 centertaps for connecting V_{dd} and Gnd. The structure is chosen this way to have easy fit in the layout.

D. Common mode

CM signals arise from CM input signals and due to component mismatches. These signals corrupt the differential signal and can make the LNA instable so CM signals should be suppressed. Goal is to have little CM gain and keep DM gain as high as possible maintaining CM and DM stability.

Current flowing through the center taps of the transformer to AC ground gives rise to CM signals. Therefore a high impedance must be created at these points. A high impedance using a current source is not possible due to the low V_{dd}. Therefore a resistor is considered as an alternative. Simulations were performed with a resistor between DC ground and the transformer. This gives little CMR and lowers the input impedance causing it to become negative resulting in instability. Most successful for achieving a high CMR appeared to be a resistor between V_{dd} and the transformer. The CM equivalent circuit for a single stage is shown in figure 24.

V. Impact of Layout

The layout is a very important step in the design of any RF-circuit. This cannot be created automatically, so it has to be done manually. Choices made in this step have big influence on the overall performance of the eventual system, and many problems arise during this step, such as the generation of parasitic effects. These can be modeled by capacitors, resistors and inductances. The dominant resistive and capacitive effects were taken into account by RC-extraction in the circuit simulator Cadence. If also inductive effects needed modeling Momentum has been used.

Then there are also the design rules that have to be obeyed during the layout. Metal lines have a minimal and maximal allowed width, setting a lower and upper bound to the added parasitics. Also the DC-current states a minimal line width due to the electro migration of the metal. Another problem is the absence of many "default" components. For example the

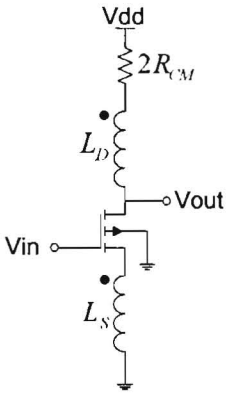


Fig. 24. Single stage CM equivalent circuit. This resistor behaves as a resistor of double resistance in common mode. In the DM circuit this resistor is not seen. This results in a lower Q-factor of the load of the circuit in CM. Because the gain is lowered much by a low Q-factor of the load inductance, the CM gain is suppressed. Simulations show a CMR of $>$ 5 dB per stage.

transformer and some capacitors used in this design had to be designed manually, satisfying the electrical performance criteria, design rules, DC-current and easy positioning in the layout. Finally it is important to keep all distances for interconnect short because the on chip wavelength at 60 GHz is $\approx$ 2.5mm, see figure 25.

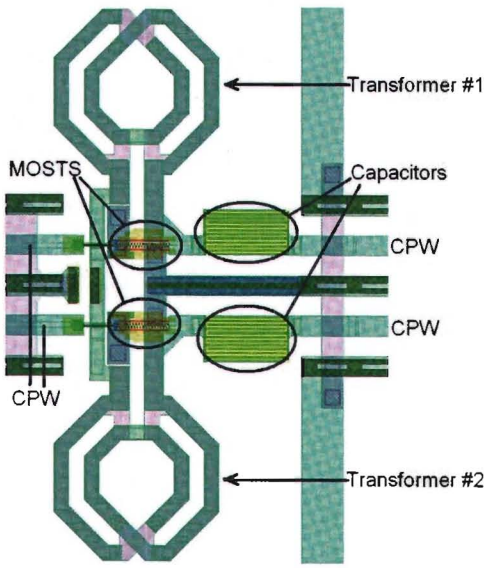


Fig. 25. Close up of the first stage. Because of the differential structure, there are two transformers, MOSTs and capacitors. At the left the CPWs are seen for the input and on the right the CPWs for connection to the second stage. Because of the short wavelength, it is important to keep distances small. Therefore the MOSTs are placed underneath the transformers. To avoid the field generated in the transformers penetrating the MOSTs, metal lines are placed between them.

For interconnecting the two stages to each other and to the bondpads, coplanar wave guides (CPWs) are used. They are shown in figure 26 using a current density plot.

The LNA uses four inductors besides the transformers. The layout of these inductors is done in such a way they have little

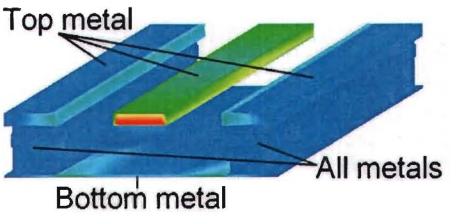


Fig. 26. Coplanar waveguide used in the layout. As Z_0 50 Ω is chosen, because the probes will be 50 Ω as well. The signal line is made with the top metal. Two ground planes are placed at both sides of the signal line by stacking all metals. The bottom metal below the signal line is also defined as ground to reduce substrate effects. To do simulations in Momentum, an approximation has been made by only including the top and bottom metal layers. Therefore a lower capacitance per unit length is expected in simulation than in reality, so a slight higher Z_0. Simulations show $Z_0 \approx 52.8\Omega$ and loss of $\approx$1.18 dB/mm.

coupling with the other components and the substrate, and the highest Q-factor as possible, see figure 27.

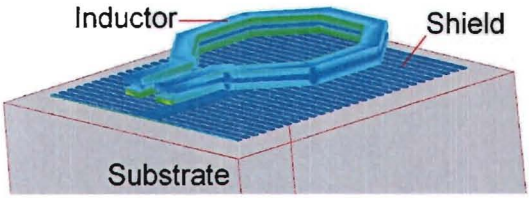


Fig. 27. Inductor with patterned shield above the substrate. Because of the horizontal metal lines in the shield there is only little eddy current possible. Therefore the effect on the performance of the inductor is small. But because the EM field is shortened, there is little field penetrating the substrate. The shield is left floating, this results in a high f_{res}. The connection of the inductors to the other components is done by the CPWs. This also provides low coupling to other components and the substrate. The Q-factor is enlarged by using two metal lines in parallel. Simulations in Momentum have been used to determine the inductance, f_{res} and Q-factor.

In figure 28 the complete LNA is shown. To shift the reference planes for the measurements, again de-embedding structures have been included. These are open, short and load.

VI. Simulations

During the complete layout traject, simulations were performed to see whether the performance is deteriorated by choices made in the layout. Goal during this stage was to obtain approximately the same performance of the circuit after the layout. It was seen the performance did not change much, but s_{21} became a little less and the NF increased a little bit due to the various added parasitics. These parameters are also quite sensitive to the variation of the Q-factors of the inductors used, mainly L_g. Simulations performed in Momentum showed Q-factors around 14 for the gate inductors. Therefore these values were used during simulations in Cadence. Optimal performance concerning gain is achieved with a $R_{src} \approx 22$ Ω. Optimal performance concerning noise is achieved with $R_{src} \approx 45$ Ω. Simulations were performed with $R_{src} = 30$ Ω. This resulted in a s_{21} of $\approx$ 11-12 dB max before layout and $\approx$ 10.7 dB max after layout. The noise figure before layout was $\approx$ 3.2 dB and after layout it became $\approx$ 3.6-3.8

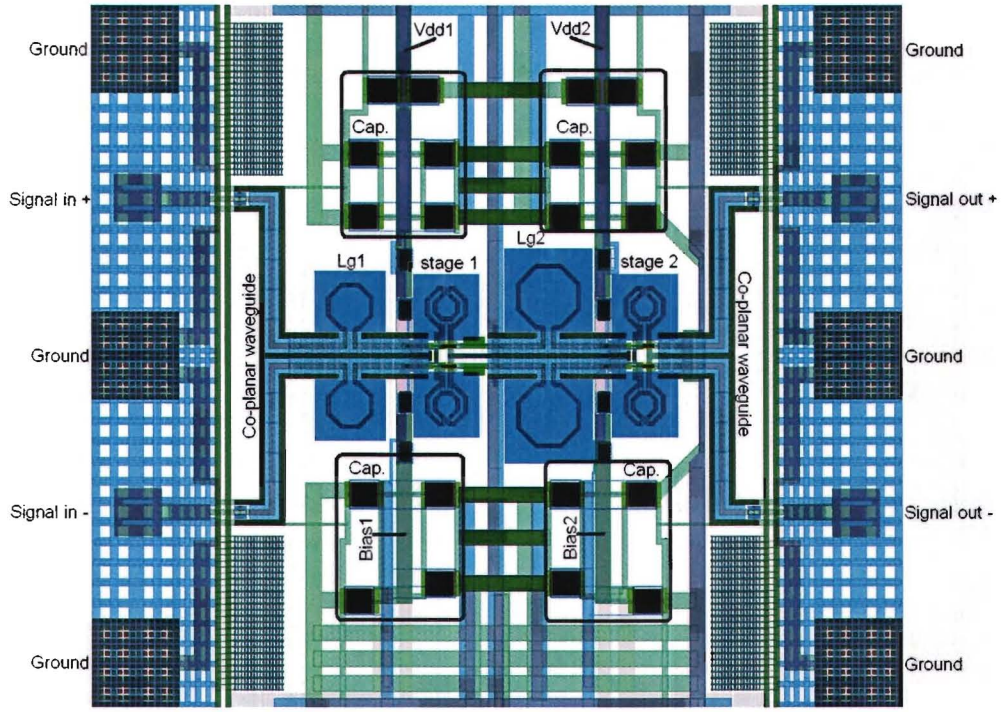


Fig. 28. The complete LNA. At the left the differential input can be seen and on the right the differential output, both using CPWs. To provide low ohmic connections from the power supply bondpads to the circuit, wide metal lines are used and the DC lines are situated on top of each other to increase capacitance between them. DC capacitances are used (indicated by the black squares) to filter the supply and bias voltages at the indicated positions. The squares underneath the inductors are the shields. From left to right can be seen: The first gate inductances, stage 1, the second gate inductances and stage 2.

dB. A gain flatness of 0.2-0.3 dB over the entire bandwidth has been achieved. Simulated $IIP_3 \approx 4$ dBm and 1 $dB_c \approx$ -9.8 dBm. The power consumption is ≈ 35 mW at 1.2 V. Due to the output isolation a s_{12} of less than -40 dB has been simulated in the band of interest. The s_{11}-parameter indicates the absorbed power generated from the source to LNA and is at minimum $\approx$ -17 dB at 68 GHz to further achieve the gain flatness. The s_{22}-parameter indicates the absorbed power from the LNA to the output ($R_{load} = 100\Omega$). This is matched to the center frequency located at 61 GHz and has a minimal value of approximately -23 dB and stays under -20 dB in the operating bandwidth.

VII. Conclusion

A 60 GHz differential LNA and a transformer were designed and taped out, both in CMOS 65 nm technology. The measurement results of the transformer show small deviation from the results obtained in simulation. At the time of this writing the LNA was not measured yet but simulations were very promising, taking many parasitics and EM simulations into account. Because of the use of a CS MOST as an active device without the use of a cascode MOST for gate drain capacitance neutralization, the noise figure is kept very low. High gain flatness has been achieved because of the use of feedback.

VIII. Recommendations

To keep NF low and s_{21} high, the losses in the matching network should be kept very low. Therefore it is important to keep the distance between the bondpads, L_{g1} and the first stage as short as possible. Also R_g of the MOSTs used have big influence and should be kept low. On the other hand, small R_g states more metal to be used in the gate connection and higher capacitance (lower f_t), so there is a trade-off.

IX. Acknowledgment

The author would like to thank Reza Mahmoudi of Eindhoven University for his helpful support and suggestions during the project and the co-workers of NXP Semiconductors for enabling the tape-out and for their helpful support during the layout phase, especially Edwin van der Heijden, Anton de Graauw and Dennis Jeurissen. The author would like to thank Philips research for enabling the tape-out of the transformer.

References

[1] X. Li, S. Shekhar and D. J. Allstot, G_m-Boosted Common-Gate LNA and Differential Colpitts VCO/QVCO in 0.18-μm CMOS *IEEE J. Solid-State Circuits*, Vol. 40, No. 12, Dec. 2005 Symp., 2004, pp. 97100.

[2] J. R. Long, Monolithic transformers for silicon RF IC design *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 13681382, Sep. 2000.

[3] D. J. Cassan and J. R. Long, A 1-V Transformer-Feedback Low-Noise Amplifier for 5-GHz Wireless LAN in 0.18-μm CMOS *IEEE J. Solid-State Circuits*, Vol. 38, No. 3, Mar. 2003

[4] G. Gonzales, *Microwave Transistor Amplifiers* 2nd edition, Prentice Hall 1997

[5] R. K. Mongia, I. J. Bahl, P. Bhartia and J. Hong, *RF and Microwave Coupled-line Circuits* 2nd edition, Artech House 2007