MASTER

Design and implementation of a spread-spectrum modem based on two TMS320C50 digital signal processors

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Design and implementation of a spread-spectrum modem based on two TMS320C50 Digital Signal Processors

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Summary

In 1992, a project was started at the Telecommunications Division to study the feasibility of picoterminal satellite communication networks using spread-spectrum modulation. A picoterminal is an extremely small VSAT (Very Small Aperture Terminal) with an antenna diameter of up to several decimeters. To exploit the satellite communication system, spread-spectrum multiple access (SSMA) is the most suitable multiple-access technique. One of the objectives of this project is to come to a realization of a picoterminal.

As part of the picoterminal project, the hardware of a picoterminal modem was designed based on two Texas Instruments TMS320C50 digital signal processors. The modem must be able to improve the performance of the already existing modem based on one TMS320C25 digital signal processor. This C25-modem has sufficient processing power to operate as baseband transmitter with a chip rate of 64 kChip/s. However, due to the limited processor performance, as an IF receiver it can process about 16 kChip/s.

The new signal processing board for the modem consists of two TMS320C50s. Each processor has its own local memory consisting of program memory and data memory. Global memory is used for communicating between the two processors. Transmitting and receiving spread-spectrum signals is done using a digital-to-analog converter and an analog-to-digital converter, respectively. Communication with the outside world is done using a 16-bit parallel interface, two serial ports and a TDM-serial port especially designed for communication with other TMS320C50s. Communication with the personal computer is done using a PC-communications interface. Facilities for testing and debugging of the TMS320C50s are provided.

Implementation of the modem was done by creating schematic diagrams using a design program for electronic circuits. After verification of the schematic diagrams, component placement was performed while taking EMC considerations in account. Finally, the routing process was started to lay the signal lines on the printed circuit board efficiently. After fabrication of the printed circuit board, components were soldered on the board. Thus, the hardware for the implementation of a high-performance version of the picoterminal modem was designed and realized.

List of abbreviations

Abbreviation	Meaning
ADC	Analog-to-Digital Converter
ALU	Arithmetic Logic Unit
ARAU	Auxiliary Register Arithmetic Unit
BPSK	Binary Phase-Shift Keying
CALU	Central Arithmetic Logic Unit
CDMA	Code-Division Multiple Access
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CWSR	Control Wait-State Register
DAC	Digital-to-Analog Converter
DARAM	Dual-Access Random Access Memory
DIL	Dual-In-Line
DPSRAM	Dual-Port Static Random Access Memory
DRR	Data Receive Register
DSP	Digital Signal Processor
DSSS	Direct-Sequence Spread-Spectrum
DXR	Data Transmit Register
EMC	Electro Magnetic Compatibility
EPROM	Erasable Programmable Read-Only Memory
GREG	Global Memory Allocation Register
HIGH Z	High-Impedant
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IPTR	Interrupt Vector Pointer
IRQ	Interrupt Request
I/O	Input/Output
IOWSR	I/O Wait-State Register
JTAG	Joint Test Action Group
LOW Z	Low-Impedant
LSB	Least-Significant Bit/Byte
MSB	Most-Significant Bit/Byte
OpAmp	Operational Amplifier

OTR	Out of Range
PC	Personal Computer
PCB	Printed Circuit Board
PDWSR	Program/Data Wait-State Register
PGA	Pin Grid Array
PLCC	Plastic Lead Chip Carrier
PLD	Programmable Logic Device
PLL	Phase Locked Loop
PLU	Parallel Logic Unit
PMST	Processor Mode Status Register
PQFP	Plastic Quad Flat Pack
RAM	Random-Access Memory
ROM	Read Only Memory
RSR	Receive Shift Register
SARAM	Single-Access Random Access Memory
SHA	Sample-Hold Amplifier
SPC	Serial Port Control Register
SRAM	Static Random Access Memory
SSMA	Spread-Spectrum Multiple Access
SWDS	Software Development System
TAP	Test Access Port
TDM	Time-Division Multiplex
TDR	Test Data Register
TTL	Transistor-Transistor Logic
VSAT	Very Small Aperture Terminal
XSR	Transmit Shift Register

Contents

1 Introduction

1.1 The picoterminal project

When personal computers (PCs) were introduced, they were used primarily as stand-alone workstations for such applications as word processing or spreadsheet analysis. Then the market exploded with demands for distributed processing applications, which created the need to interconnect PCs via telecommunications facilities such as local area networks and via wide area networks. An example of such a wide area network is a network using Very Small Aperture Terminals (VSATs). A VSAT is a satellite ground station with an antenna diameter of approximately 1 to 2½ meters. Due to its relative large diameter, a VSAT is difficult to transport. Therefore, smaller VSATs are required which are portable, more practical and user-friendly but have low bit rates. An extremely small VSAT is called a picoterminal and has an antenna diameter of up to several decimeters. It can operate at data rates of several tens to a few hundred bits per second. Possible applications of a picoterminal satellite communication system are for example data-collection platforms and alarm systems, consisting of a number of distant terminals and one hub-station, that collects the data. Such a system is illustrated in Figure 1.1.

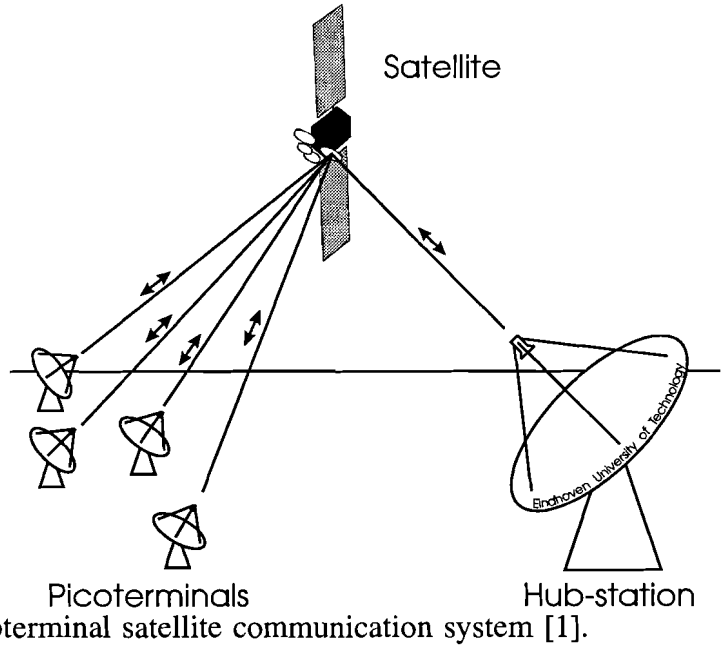


Figure 1.1 A picoterminal satellite communication system [1].

From Figure 1.1 it can be seen that multiple terminals are communicating with each other using a satellite and a hub-station. Therefore, the use of a multiple-access technique is necessary. The most suitable multiple-access technique for a picoterminal communication system operating at low data rates is code-division multiple access (CDMA), also called spread-spectrum multiple access (SSMA). In this technique, the signal of each user is modulated with a unique spreading signal. The resulting wideband signal from all users may use the same channel at the same time.

At the Telecommunications Division, a project was started to study the feasibility of picoterminal satellite communication networks using spread-spectrum modulation [2]. One of the objectives of this project was to come to a realization of such a picoterminal. In 1993, Diederen[1] designed a picoterminal modem based on the TMS320C25 Digital Signal Processor. Properties of this modem are listed in Section 1.4. This report describes the design and hardware implementation of the improved picoterminal modem based on two TMS320C50 Digital Signal Processors.

1.2 Spread Spectrum Communications

Before the design of the improved spread-spectrum modem is described, some information about spread-spectrum communications is given in this section.

Spread spectrum refers to the modulation technique used with digital communication. A communication system is a spread-spectrum system if the transmitted signal satisfies the next two criteria:

1) The bandwidth of the transmitted signal is much larger than the message bandwidth.

2) The transmission bandwidth is determined by some (spreading) function that is independent of the message and is known to the receiver.

Spread spectrum has three major advantages. Firstly, spreading the transmitted signal causes the bandwidth of the transmitted signal to increase and the spectral power density of that transmitted signal to decrease. This decreased spectral power density makes it more difficult to detect the signal, resulting in a low probability of detection. Secondly, a spread-spectrum system has a high level of interference rejection. In military situations, intentional jamming of enemy's signals is made very difficult because the jammer is unaware of the signal characteristics when this signal is generated with a spreading

function. In civil communications, interference from other users arises in multiple-access communications in which a number of users share a common channel bandwidth. Signals from different users may be distinguished from one another if every user impresses his own spreading function on the transmitted signal. A receiver can recover the information desired if it knows the corresponding transmitted spreading function. Finally, if a spreading function used to spread the spectrum is only known to the transmitter and the receiver, some kind of message privacy will be obtained. Using spread-spectrum techniques, code division multiple access (CDMA) can be applied.

The simplest form of a spread-spectrum communication system is one that uses binary phase-shift keying (BPSK) direct-sequence spread-spectrum (DSSS) modulation. With this form of spread spectrum modulation, bandwidth is spreaded by direct modulation of a data signal with a wideband spreading signal. The data signal is characterized by the bit period T or by the bit rate $1/T$. The wideband spreading signal is characterized by its period T_c, mostly called chip period or by the chip rate $1/T_c$. To spread or despread a signal, a so-called pseudonoise (PN) code is used as the spreading function. A PN-code is generated by a PN-code generator which can be realized as a binary shift register with feedback. More information about spread-spectrum systems and PN-codes can be found in [2, 3].

1.3 Picoterminal implementation

Figure 1.2 illustrates the schematic diagram of the picoterminal transmitter. It consists of a spread-spectrum modulator, which multiplies the data signal with the spreading code and a BPSK modulator which modulates the spreaded data signal.

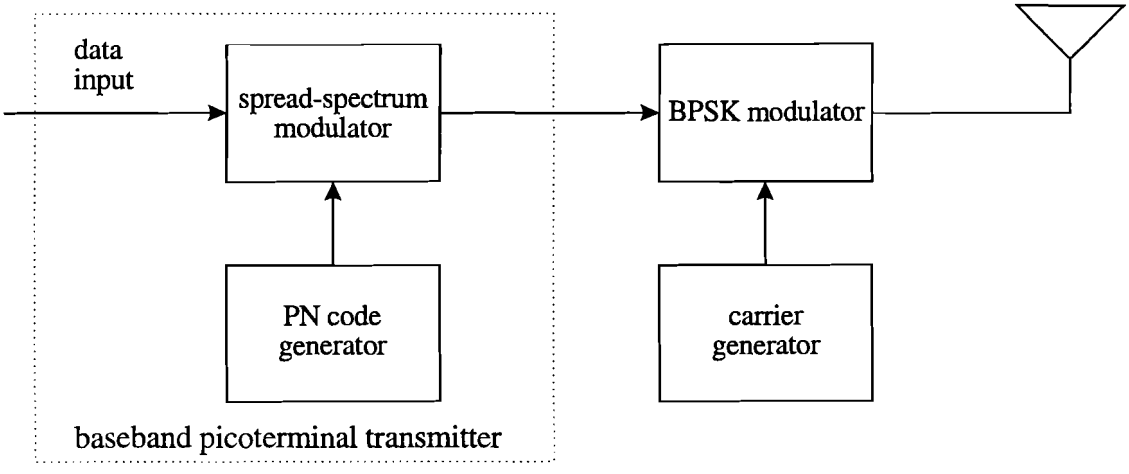


Figure 1.2 The picoterminal transmitter [1].

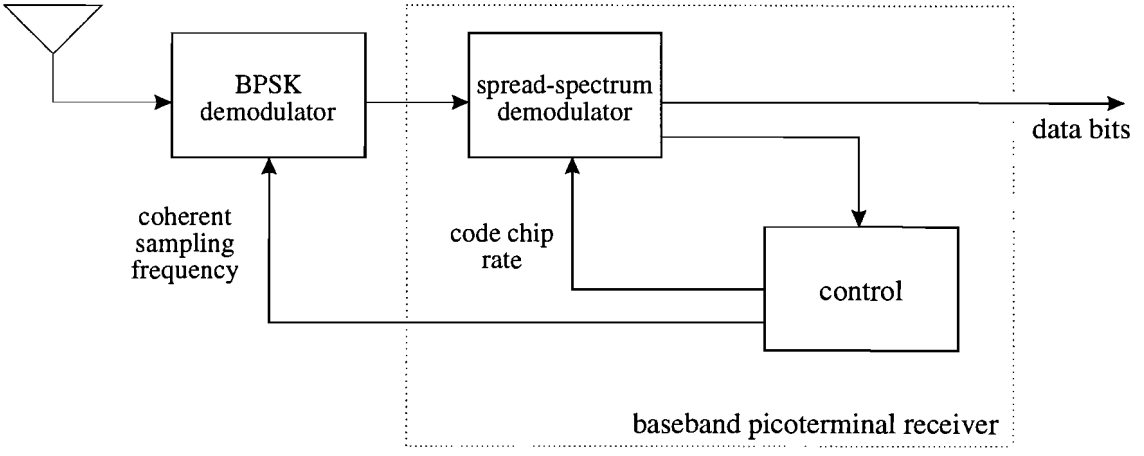


Figure 1.3 The picoterminal receiver.

The schematic diagram of the picoterminal receiver is shown in Figure 1.3. The picoterminal receiver consists of a BPSK demodulator, that is synchronized to the received waveform by means of the control circuit. The BPSK-demodulated signal is despreaded by the spread-spectrum demodulator through multiplication with the locally generated spreading code. The local spreading code is synchronized to the received signal by means of the control circuit. When synchronization is accomplished, the demodulated signal can be decoded. More information about the implementation of the picoterminal modem can be found in [1].

1.4 Properties of the existing modem

The hardware of the existing modem consists of [1, p. 31] :

- TMS320C25 Digital Signal Processor
- 50 MHz oscillator
- Reset circuit
- Wait-state generator
- Memory: 32K 16-bit words EPROM
  32K 16-bit words RAM
- I/O-selection circuit
- Digital-to-Analog Converter (DAC) and the transmit clock
- Analog-to-Digital Converter (ADC)
- Communications interface

The hardware has been situated on a single board. By setting jumpers, the modem can be configured as either a transmitter or a receiver. However, if transmitting and receiving spread-spectrum signals is to be done simultaneously, two modem prints are necessary and some alterations to each print must be carried out. For the receiver circuit, the D/A converter must be removed because the corresponding I/O port is then used to communicate with the off-board frequency synthesizer. Kamperman designed this programmable frequency synthesizer board to generate the sample signal for the A/D converter [2]. Communication to this frequency synthesizer board is done by plugging a flatcable connector in the IC-sockets of the unused buffers which are used for communication with the D/A converter. Therefore, the D/A converter must be removed from the receiver configuration.

Testing and debugging of the TMS320C25 DSP is done using the Software Development System (SWDS). SWDS is a PC-resident software development and debugging tool that provides real-time software simulation of the TMS320C25. The SWDS packet consists of a hardware board and specific software. The hardware is a single board to be plugged into a free expansion PC slot. It is equipped with a TMS320C25 device and memory. The board is connected to a 68-pin PGA-connector that is plugged into the IC-socket of the TMS320C25. In this way, the operation of the TMS320C25 is simulated by the PC board.

For communicating to slower off-chip devices (i.e. memories and peripherals), the TMS320C25 is capable of using wait-states. Access to the off-chip devices can be extended with one or more clock cycles. For this purpose, a wait-state generator is designed [1, p. 34-37].

Using the modem print, the spread-spectrum modulator and demodulator have been realized. The modulator can generate chip rates up to 64 kHz. Due to the limited performance of the TMS320C25, the demodulator only operates with chip rates up to 16 kHz.

Recommendations listed in [1, p. 55 and 62] must be taken into account for future design:

- it is possible to write to the EPROM transceivers. This causes a databus conflict that can damage the transceiver ICs, but more probably the digital signal processor;
- reading the analog-to-digital converter is only allowed if the read instruction is executed from the on-chip RAM and is followed by another instruction that requires on-chip memory access (e.g. a NOP instruction). Otherwise, a bus conflict can occur that can damage the hardware;

- On the existing modem, the least significant bit (LSB) of the ADC databus has been connected to the LSB of the TMS320C25 databus; in future design it is better to connect the most significant bit (MSB) of the ADC databus to the MSB of the processor's databus. In this way, the sign bit of the ADC is then also the sign bit of the input word that the processor reads into memory;
- to prevent the OpAmp connected to the output of the digital-to-analog converter to oscillate due to capacitive load of connected coaxial cables, a resistor of 39 Ω must be connected from the output of the OpAmp to the output BNC plug and the feedback loop; this specific resistance also makes the output impedance of the OpAmp equal to the impedance of the coaxial cables connected (50 Ω);
- A hardware error in the communications interface must be corrected. When the personal computer changes the address of the communications interface, an unwanted interrupt is generated on the digital signal processor.

1.5 Improving the existing modem

The existing modem has sufficient power to operate as baseband transmitter with f_c = 64 kChip/s. However, as an IF receiver it can process about f_c = 16 kChip/s. Replacing the TMS320C25 by the TMS320C50 will double the processing speed of the receiver. Using a multi-processor design with two TMS320C50 DSPs operating in parallel will quadruple the processing speed, thus obtaining a chip rate of 64 kChip/s for the receiver. The reason why the TMS320C50 DSP was chosen is explained in depth in [4]. Furthermore, the modem hardware must be powerful to support the following additional functions [4]:

- Fast code acquisition
- Accounting for carrier Doppler shift and oscillator phase noise
- Receiver control
- Implementing the frequency synthesizer in software
- Data detection and data transfer to and from the user
- Measurement options such as multi-user simulation and noise generation

Using a multi-processor design with two TMS320C50 DSPs in parallel will not only enhance the processing speed of the receiver but will provide two timers, more interrupt lines and more I/O ports.

From a hardware point of view, there are also good reasons to design a new modem using two TMS320C50 DSPs. Disadvantages and hardware errors of the existing modem can be corrected. Recommendations can be followed to improve the performance of the new

modem. Functional blocks of the already existing modem must be checked to see if they can also be used for the new modem.

Before designing the improved modem based on two TMS320C50s, some design considerations are made based on the properties of the TMS320C25 modem:

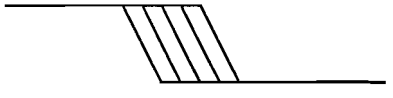
- Improving the processing speed of the receiver configuration can be done by choosing a different analog-to-digital converter (see Section 8.4 of [4]) and passing the digital samples from the analog input signal to both TMS320C50s. In this way, both TMS320C50s perform calculations on the sample values simultaneously.
- The TMS320C25 modem is not capable of transmitting and receiving simultaneously using one hardware board. In the new modem design, one processor can operate as a transmitter and the other processor as a receiver. If necessary, both processors can operate as a receiver while one of the processors operates also as a transmitter.
- Communicating with the frequency synthesizer board using unused IC-sockets must be avoided. In the new modem design, a completely new 16-bit parallel interface must be designed which is capable of reading and writing to external devices including the frequency synthesizer board.
- The function of the frequency synthesizer board can be implemented in software using the TMS320C50 timer. In this case, no external hardware is required.
- The Software Development System as was used with the TMS320C25 modem is no longer necessary because the TMS320C50 is equipped with a JTAG interface for testing and debugging purposes. The great advantage is that it is no longer necessary to remove the processors from the board as was done at the TMS320C25 modem.
- The wait-state generator as implemented on the TMS320C25 modem board is no longer necessary because the TMS320C50 is equipped with an internal software wait-state generator.
- The communications interface, the D/A converter circuitry, the I/O-selection circuit and the DSP memory can be copied from the TMS320C25 modem.
- Recommendations and hardware errors listed in Section 1.4 and [1, p. 55 and 62] have to be taken into account.

Using the TMS320C25 modem made by Diederen and the design considerations listed above, the improved modem based on two TMS320C50 Digital Signal Processors was designed and implemented in hardware. This report describes the design and implementation in detail. Chapter 2 discusses the new modem based on its functional block diagram. Furthermore, properties of the TMS320C50 are described. In chapter 3, the

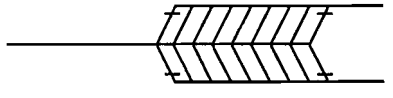
reset and oscillator circuitry are described. Chapter 4 discusses in detail the implementation of local program and data memory and global memory. For each type of memory, the choice of the IC, the interfacing to the TMS320C50 and timing aspects are discussed. Furthermore, communications between the memory devices are studied extensively to prevent busconflicts. Also, communications with I/O ports are described. It will be shown that the I/O-selection circuit designed by Diederen[1] is also sufficient to operate with the TMS320C50 and is therefore implemented in the new modem design. In chapter 5, the analog-to-digital converter circuit and the digital-to-analog converter circuit are described. The ADC circuit consists of a new ADC and a sample switch which passes samples to both processors alternatingly. The DAC circuit is the same as was used with the TMS320C25 modem. Chapter 6 explains the several forms of communicating with the outside world: the JTAG interface for testing and debugging of TMS320C50s, the serial port for communication with external serial devices, the TDM serial port for communicating with up to seven other TMS320C50 devices, the communications interface for communicating with the personal computer and the parallel interface for communications with other external parallel devices (i.e. the frequency synthesizer). Chapter 7 describes some software configurations which must be made for full use of the possibilities of the hardware: remapping of interrupt vectors, configuring the amount of on-chip and global memory in software and how the internal software wait-state generator of the TMS320C50 can be programmed for 0, 1, 2, 3 or 7 wait-states. Chapter 8 explains the implementation of the modem: creating schematic diagrams, component placement and routing the printed circuit board. Finally, chapter 9 discusses conclusions and recommendations.

In this report, signals and pins denoted with a '*' are active low. Numbers ending with 'b' or 'h' are binary or hexadecimal, respectively. TTL IC timings are taken from the 0° to 70° C range (commercial ICs). In timing tables, 'n' denotes the number of wait states.

Key to waveform diagrams



Signal changes from high to low within this time



Signal changes from high-impedance state to valid logic level during this time

2 The new modem

2.1 Introduction

This chapter introduces the new modem based on two TMS320C50 Digital Signal Processors. Section 2.2 discusses the properties of the new modem based on its block diagram. Section 2.3 gives a general overview of the main properties of the TMS320C50.

2.2 Block diagram of the modem hardware

The electronic circuit of the baseband modem can be divided into several functional blocks. Figure 2.1 shows the block diagram of the modem. The functional blocks are listed below:

- Two digital signal processors : TMS320C50(1) and TMS320C50(2)
- 32K 16-bit words EPROM
- 32K 16-bit words local RAM
- a maximum of 2K 16-bit words Global RAM
- Memory selection circuitry
- I/O-selection circuitry
- Reset circuit
- Oscillator Circuit
- JTAG Interface
- Analog-to-Digital Converter + ADC Switch
- Digital-to-Analog Converter
- Transmit clock
- 16-bit Parallel Interface to the frequency-synthesizer board
- Two Serial Ports
- Time-Division Multiplexed (TDM) Serial Port
- Communications Interface with PC

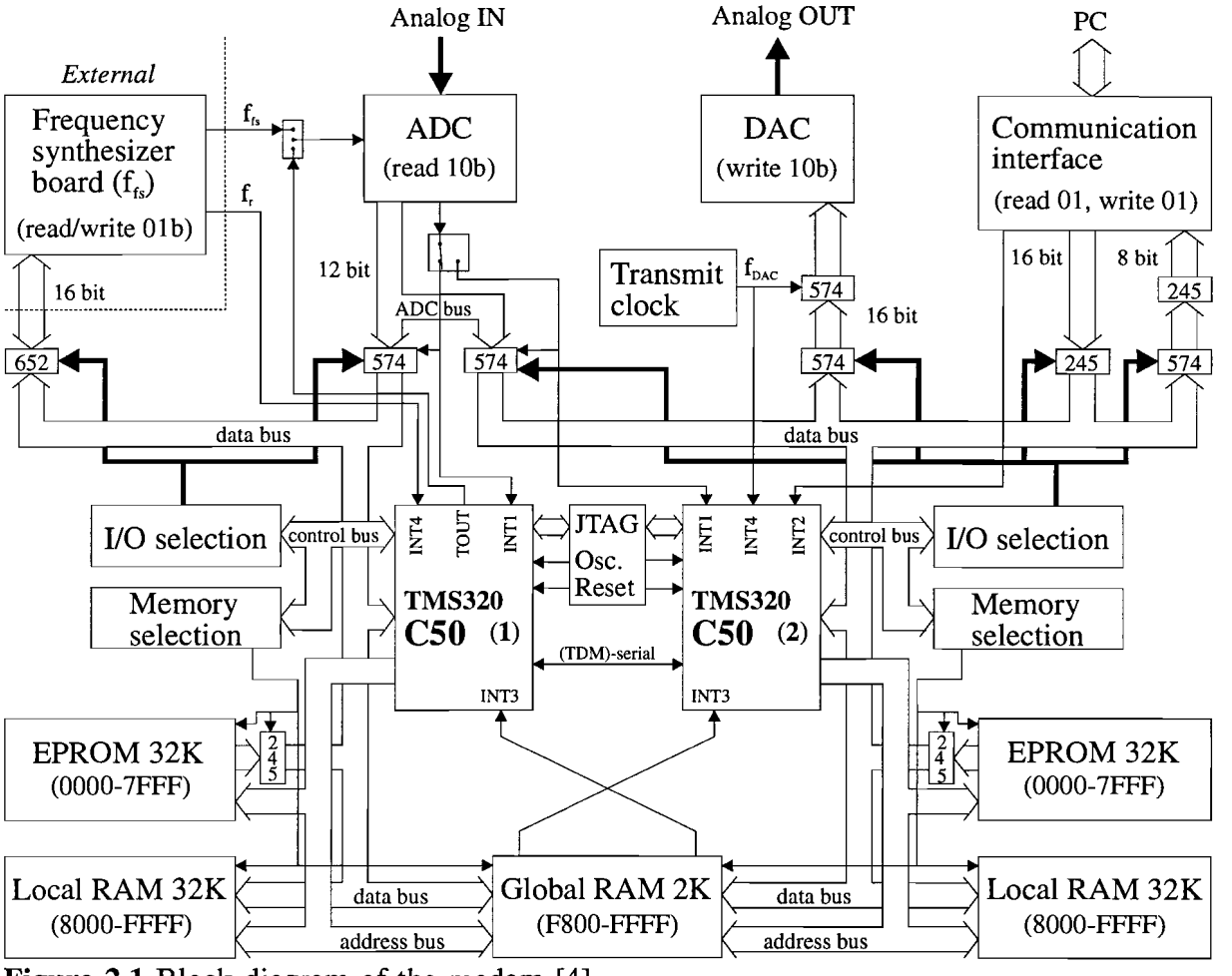


Figure 2.1 Block diagram of the modem [4].

The main elements of the modem are the TMS320C50 DSPs. Each TMS320C50 has its own local memory. This local memory consists of 32K EPROM for program code storage and 32K RAM for local data and program storage. Global memory is used for communicating between the two DSPs. Selection of these memory devices is done with the memory selection circuit. Selection of I/O ports (i.e. ADC, DAC, communications interface, parallel interface) is done using the I/O-selection circuit.

Another way of communicating between both processors can be done using the TDM-serial port. This port has been designed especially for intercommunication between up to eight TMS320C50s. Furthermore, each DSP has been provided with a serial port for communicating to external serial devices. Both serial ports are situated on the connector.

For reset purposes, a reset circuit was connected to both TMS320C50s. It provides an automatic reset at power-up, but user-generated resets can be generated using an external reset button. Furthermore, an oscillator circuit was provided to generate the clock

frequency. This clock frequency can be divided-by-one or divided-by-two to provide the internal machine cycle. This feature simplifies the choice of an appropriate oscillator.

Another feature of the TMS320C50 is the JTAG interface. It offers real-time debugging facilities for both DSPs. During tests, the JTAG interface is connected to an XDS510 board manufactured by Texas Instruments. Therefore, the modem board was provided with a special connector. Replacing a DSP by a target connector as was done with the TMS320C25-modem is no longer necessary.

For transmitting and receiving analog signals, a Digital-to-Analog Converter (DAC) with the transmit clock and an Analog-to-Digital Converter (ADC) are used. The DAC is connected to TMS320C50(2) and is necessary to be able to simulate multiple users and to perform digital chip-pulse shaping. The transmit clock can produce frequencies from 8 kHz to 1024 kHz and is useful for implementing different chip rates. The ADC is connected to both TMS320C50s using a sample-switch. This switch passes the incoming samples alternatingly to TMS320C50(1) and TMS320C50(2). In this manner, calculations on samples can be performed simultaneously. In the design, it is also possible to pass all samples to one DSP.

To sample the incoming analog signal at the right moments, a frequency-synthesizer designed by Kamperman[2] is used. To communicate properly with this frequency-synthesizer or any other device, a 16-bit read/write parallel interface was designed. This interface allows data to be written to an external device (e.g. the frequency-synthesizer) or allows data to be read from a device.

The communications interface is included for communication with a personal computer (PC). With the PC, data (8-bit bytes or 4-bit nibbles) are transmitted and received to and from the modem. The communications interface is the same as was used by Diederen[1].

To access the A/D-converter, the D/A-converter, the communications interface and the parallel interface, the I/O-selection circuit is used.

2.3 Properties of the TMS320C50

The key features of the TMS320C50 DSP are listed below.

- advanced Harvard-type architecture
- 35-/50-ns single-cycle fixed-point instruction execution time (28.6/20 MIPS)

- 9K x 16-bit single-cycle on-chip program/data RAM
- 2K x 16-bit single-cycle on-chip boot ROM
- 1056 x 16-bit dual-access on-chip data RAM
- 224K x 16-bit maximum addressable external memory space (64K program, 64K data, 64K I/O and 32K global)
- 16-bit addressbus and 16-bit databus
- 32-bit arithmetic logic unit (ALU)/accumulator
- 16-bit parallel logic unit (PLU)
- Context-switch registers for automatic save and restore of strategic CPU-controlled registers during an interrupt service routine
- Full-duplex synchronous serial port for direct communication between the TMS320C50 and another serial device
- Time-division multiplexed (TDM) serial port for communication between other TMS320C50 devices
- 64K addressable parallel I/O ports, sixteen of which are memory mapped
- Sixteen software-programmable wait-state generators for program, data and I/O memory spaces
- Divide-by-one and divide-by-two clock options
- On-chip clock generator
- JTAG boundary scan logic (IEEE standard, 1149.1)
- 5-V static CMOS technology with two power-down modes
- 132-pin plastic quad flat pack package (PQFP)

2.3.1 CPU

The TMS320C50 has been designed with an advanced Harvard-type architecture that maximizes the processing power by maintaining two separate memory bus structures, program and data, for full-speed execution. Special instructions support data transfers between the two spaces.

The TMS320C50 architecture is built around two major buses: the program bus and the data bus. The program bus carries the instruction code and immediate operands from program memory. The data bus carries the data obtained from data memory. Together, the program and data buses can carry data from on-chip data memory and internal or external program memory to the multiplier in a single cycle.

The TMS320C50 performs 2s-complement arithmetic, using the 32-bit arithmetic logic unit (ALU) and accumulator. The ALU is a general-purpose arithmetic unit that uses 16-

bit words taken from data memory or derived from immediate instructions. The ALU can also perform Boolean operations. The accumulator stores the output from the ALU and is also the second input to the ALU.

In addition to the main ALU, there is a parallel logic unit (PLU) that executes logic operations on data without affecting the contents of the accumulator. The PLU is used for setting, testing or toggling multiple bits in a control/status register or any data memory location.

The multiplier performs 16 x 16-bit 2s-complement multiplication with a 32-bit result in a single-instruction cycle. The fast on-chip multiplier allows the TMS320C50 to efficiently perform fundamental DSP operations such as convolution, correlation and filtering.

Eight levels of hardware stack save the contents of the program counter during interrupts. Eleven context-switch registers are available for storing strategic CPU-controlled registers during an interrupt service routine.

The TMS320C50 possesses a high degree of parallelism; that is, while the data are being operated upon by the central ALU (CALU), arithmetic operations may also be executed in the auxiliary register arithmetic unit (ARAU).

2.3.2 On-/Off-chip Memory

The TMS320C50 features several forms of on-chip and off-chip memory:

- 2K x 16-bit on-chip programmable ROM. This memory is used for booting from slower external ROM or EPROM to fast on-chip or external RAM. ROM can be selected during reset by driving the MP/*MC-pin low.
- 1056 x 16-bit on-chip dual-access RAM (DARAM). This RAM can be accessed twice per machine cycle. This block of memory is primarily intended to store data values, but can also be used to store program code as well as data.
- 9K x 16-bit on-chip single-access RAM (SARAM). This RAM can be accessed only once per machine cycle. This memory is software configurable as program and/or data memory space.
- 224K x 16-bit maximum addressable off-chip memory. More details on this external memory can be found in Section 4.2.

2.3.3 Parallel I/O Ports

The TMS320C50 has a total of 64K addresses for I/O ports, sixteen of which are memory-mapped in data memory space. These ports can be addressed by the IN instruction or the OUT instruction. The memory-mapped I/O ports can be accessed with any instruction that reads or writes data memory. An active-low *IS signal indicates a read/write operation via an I/O port and becomes active when the IN or OUT instruction is used. For the sixteen memory-mapped I/O ports, the *IS signal becomes also active when memory accesses are performed. I/O ports can be accessed using the I/O-selection circuit, described in Section 4.7.

2.3.4 Serial I/O Ports

The TMS320C50 carries two high-speed serial ports. These serial ports are capable of operating at a bit rate of up to one-fourth the machine cycle rate (7.15 MHz). One of the two circuits is a synchronous, full-duplex serial port. Its transmitter and receiver are double buffered and individually controlled by maskable external interrupt signals. Data are framed either as bytes or as words. The second circuit is a full-duplex serial port that can be configured either for synchronous or for time-division multiplexed (TDM) operations. The TDM serial port is used in multiprocessor applications. Section 6.3 and 6.4 describe the serial ports in detail.

2.3.5 JTAG-scanning logic

The JTAG scanning logic circuitry is used for debugging and testing purposes only. The JTAG scan logic provides the boundary scan to and from the interfacing devices. Also, it can be used to test the pin-to-board connections as well as to perform operational tests on those peripheral devices that surround the TMS320C50. It has been interfaced to another internal scanning logic circuitry, which has access to all of the on-chip resources. Thus, the TMS320C50 can perform on-board emulation by means of the JTAG serial scan pins and the emulation-dedicated pins. Section 6.2 details the JTAG interface.

2.3.6 Software Waitstate Generator

Software wait-state logic has been incorporated without external hardware into the TMS320C50 for interfacing with slower off-chip memory and I/O devices. This circuitry consists of 16 wait-state generating circuits and is user-programmable to operate 0, 1, 2, 3 or 7 wait states. Section 7.5 details how the wait-state generator must be programmed.

2.3.7 Divide-by-One Clock

The divide-by-one clock feature on the TMS320C50 consists of an on-chip phase locked loop (PLL) peripheral which provides the capability to supply a clock cycling at the machine cycle rate of the CPU. It reduces the system's high-frequency noise that is due to a high-speed switching clock. The PLL has a maximum operating frequency of 28.6 MHz.

2.3.8 Hardware Timer

The TMS320C50 features a 16-bit timing circuit. The timer is an on-chip down-counter that can be used to periodically generate CPU interrupts. The timer is decremented by one at every CLKOUT1 cycle (= internal machine cycle rate). A timer interrupt is generated each time the counter decrements to zero. This timer can be stopped, restarted, reset or disabled by specific status bits.

2.3.9 General-Purpose I/O Pins

The TMS320C50 has two general-purpose I/O-pins that are software controlled. The *BIO pin is a branch control input pin and the XF pin is an external flag output pin. The *BIO pin can be used to monitor peripheral device statuses. By polling this pin, a branch can be conditionally executed when the *BIO input is active (low). The XF (external flag) pin signals to external devices via software. Special instructions are provided to set or reset the XF pin.

2.3.10 Interrupts

The TMS320C50 has four external, maskable user interrupts (*INT1-*INT4) that external devices can use to interrupt the processor; there is one external nonmaskable interrupt (*NMI). Internal interrupts are generated by the serial port, the timer, the TDM port and the software interrupt instructions. Reset (*RS) is an external interrupt that can be used at any time to put the TMS320C50 into a known state. Reset is typically applied after power-up when the machine is in an unknown state. The TMS320C50 has been provided with an *RS-pin. Driving the *RS signal low causes the TMS320C50 to terminate execution and forces the program counter to zero. Interrupt priorities are set so that reset has the highest priority and *INT4 has the lowest priority.

The TMS320C50 samples the external interrupt pins multiple times to avoid noise-generated interrupts. To detect an active interrupt, the TMS320C50 must sample the signal low on at least three consecutive machine cycles. Once an interrupt is detected, the TMS320C50 must sample the signal high on at least two consecutive machine cycles to be able to detect another interrupt. The minimum interrupt acknowledge time is defined as eight cycles:

- three cycles to externally synchronize the interrupt
- one cycle for the interrupt to be recognized by the CPU
- four cycles to execute the INTR instruction and flush the pipeline.

On the ninth cycle, the interrupt vector is fetched.

It is often necessary to copy program code from slower EPROM to faster RAM. In this case, interrupt vectors which reside in program space at address 0h should be remapped, otherwise an interrupt service routine starts with a branch instruction executed from the rather slow EPROM. Section 7.2 explains how interrupt vectors are mapped at address 0h in program memory space and can be remapped to the beginning of any block of 2K-words.

3 System Control Circuitry

3.1 Introduction

The system control circuitry performs important functions in system initialization and operation. In this chapter, a crystal oscillator circuit design and a power-up reset circuit design are presented.

3.2 Oscillator circuit

The TMS320C50 can use either its internal oscillator or an external frequency source for a clock. Furthermore, it is possible to inject twice the frequency required and performing a divide-by-two on this frequency in order to obtain the internal machine cycle. To perform these possibilities, the TMS320C50 has been provided with two clock input pins and two clock output pins:

- X2/CLKIN1 (input) : input pin to the internal oscillator from the crystal. If the internal oscillator is not used, a clock may be input to the device on this pin. The internal machine cycle is half this clock rate.
- CLKIN2 (input) : divide-by-one input clock for driving the internal machine rate.
- CLKOUT1 (output) : master clock output signal. This signal cycles at the machine-cycle rate of the TMS320C50.
- X1 (output) : output pin from the internal oscillator for the crystal. If the internal oscillator is not used, this pin should be left unconnected.

The clock mode is determined by the CLKMD1 and CLKMD2 clock mode pins on the TMS320C50. Table 3.1 shows the four possible clock modes [5, p. A-10].

Table 3.1 Four possible clock modes.

CLKMD1	CLKMD2	Clock Source
0	0	External divide-by-two clock option with the internal oscillator disabled.
0	1	Reserved
1	0	External divide-by-one clock option.
1	1	External divide-by-two option. Internal divide-by-two clock option with an external crystal.

Using the clock mode pins and the clock input/output pins from the TMS320C50, the following clock options can be made:

- **External Divide-by-Two Clock Option with the internal oscillator disabled**

  An external frequency source can be used by injecting the frequency directly into X2/CLKIN1, with X1 left unconnected. This external frequency is divided by two to generate the internal machine cycle. The internal oscillator is disabled.

- **External Divide-by-One Clock Option**

  An external frequency source can be used by injecting the frequency directly into CLKIN2, with X1 left unconnected and X2/CLKIN1 connected to +5 Volts. This external frequency is divided by one to generate the internal machine cycle.

- **External Divide-by-Two Clock Option**

  An external frequency source can be used by injecting the frequency directly into X2/CLKIN1, with X1 left unconnected. This external frequency is divided by two to generate the internal machine cycle.

- **Internal Divide-by-Two Clock Option with External Crystal**

  The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN1. The frequency of CLKOUT1 is one-half the crystal's oscillating frequency.

To choose a crystal for the TMS320C50, the following considerations in the modem design were made:

- the crystal must operate at 28.57 MHz or 57.14 MHz (divide-by-two clock option). These frequencies produce a machine-cycle time of 35 ns, which is the minimum cycle time for the TMS320C50.
- according to the timing requirements for the clock input of the TMS320C50, the rise and fall times of the injected frequency must be at most 5 ns (see [5, p. A-12]).
- an external crystal oscillator must be used. This is a single device in a DIL-package just requiring a supply voltage for operation. The output is a TTL-compatible square-wave with good frequency stability.
- the clock options external divide-by-two and external divide-by-one must be made using jumpers.

A DIL-packaged crystal oscillator operating at 28.57 MHz or 57.14 MHz is not available. The nearest frequencies available are 25 MHz and 50 MHz. The SG-51KT, as was used by Diederen[1], is chosen for the crystal oscillator. The properties of this crystal oscillator are listed below:

- Output frequency 25 MHz or 50 MHz.
- Output signal's frequency stability of ±100 ppm.
- Oscillation start time of 10 ms max.
- Fan out of 5 TTL max.
- Pin compatible with full size metal can.
- Packaged in plastic 14-pin DIP IC-socket.

The output signal of the SG-51KT/25 MHz has a rise and fall time of at most 8 ns. This does not satisfy the requirements made by the TMS320C50. For the SG-51KT/50 MHz, these timings are both 6 ns. This is also not sufficient, but it will not be so destructive. Therefore, the 50 MHz version of the SG-51KT is chosen. However, the output signal of the oscillator is buffered by a 74F14 Schmitt-trigger inverter. This inverter ensures fast rise and fall times. In this case, the 25 MHz version of the SG-51KT is also appropriate. CLKMD1 and CLKMD2 must both be set high to provide a divide-by-two on the clock frequency in order to obtain the correct machine cycle.

Figure 3.1 shows the oscillator circuit and the external divide-by-one/divide-by-two clock selection circuit. The output of the crystal oscillator (U47) is buffered by a 74F14 Schmitt-trigger inverter (U46) to ensure fast rise and fall times.

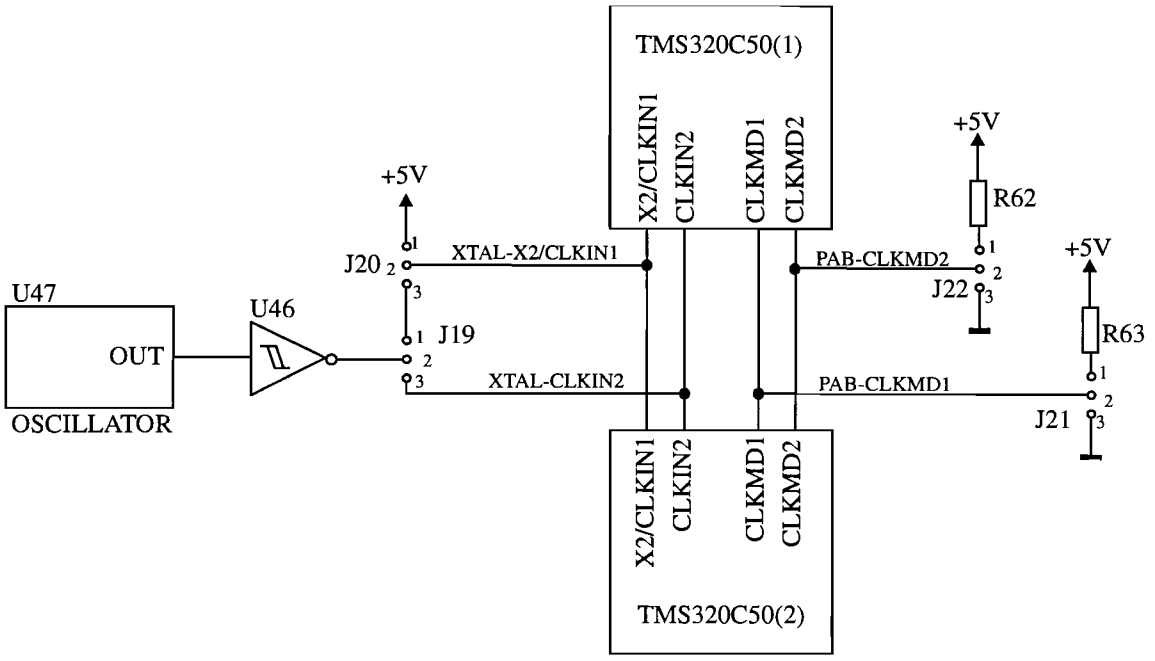


Figure 3.1 The TMS320C50s with the oscillator circuit.

Jumpers J19, J20, J21 and J22 are implemented to enable the clock options as is shown in Table 3.2.

Table 3.2 Jumpersettings oscillator circuit.

J19	J20	J21	J22	Clock Mode Selection
12	23	23	23	External Divide-by-Two Clock Option; Internal oscillator disabled
12	23	12	12	External Divide-by-Two Clock Option; Internal oscillator enabled
23	12	12	23	External Divide-by-One Clock Option

The signal lines from the oscillator circuit labelled XTAL-X2/CLKIN1 and XTAL-CLKIN2 are connected to X2/CLKIN1 and CLKIN2 of both TMS320C50s. Also the signal lines from the divide-by-one/divide-by-two clock selection circuit are connected to the corresponding input pins from both the TMS320C50s.

3.3 Reset circuit

For reset purposes, the TMS320C50 has been provided with an *RS pin. For correct system operation after power-up, a reset signal must be asserted low for several clock cycles so that data lines are put into the high-impedance state and address lines are driven low. According to the reset timing requirements of the TMS320C50, the reset low pulse duration must be at least $12H$ ns, where H is defined as half a machine cycle. For a TMS320C50 operating at 28.57 MHz, H=17.5 ns so the reset pulse must be low for at least 210 ns. As was explained in Section 3.2, the TMS320C50 in the modem design operates at 25 MHz. Therefore, the reset pulse must be low for at least 240 ns. Upon power-up, it takes 10 ms before the crystal oscillator reaches a stable operating state (see Appendix 4 for the oscillator data sheets). Therefore at power-up, the reset circuit should generate a low pulse on the reset line until the oscillator is stable. The duration of the low pulse on the reset pin is approximately 167 ms, which is the time it takes for the capacitor to fully change to 1.5 Volt. This is the voltage at which the reset input switches from a logic level 0 to a logic level 1.

It seems that the duration of the reset pulse is too long compared to the setup time of the crystal oscillator. However, it offers the possibility to choose other crystal oscillators which may have longer setup times. Besides, the reset pulse is generated only during initialization before actual communications begin. The reset pulse can also be generated externally. This is achieved pushing reset button S1 or asserting the CONN-*RESET-pin on CONN1 low (see Sheet 6 of Appendix 1).

Figure 3.2 shows the reset circuit. Resistor R1 and capacitor C1 determine the duration of the reset-low pulse (R1 = 1 MΩ and C1 = 0.47 μF). Schmitt-trigger inverters (U46) are used to shape the reset signal. The output signal line labelled *RESET is connected to the *RS-input pins from both TMS320C50s, to the 2x32-pin connector CONN1 as output signal and is also used throughout the modem design.

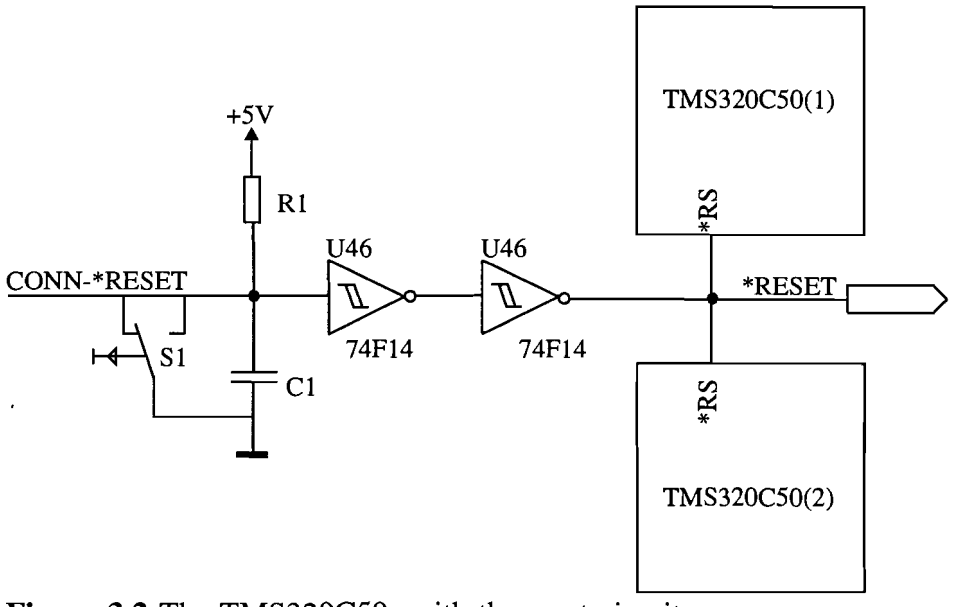


Figure 3.2 The TMS320C50s with the reset circuit.

4 Memory and I/O-ports

4.1 Introduction

This chapter describes the configuration and hardware implementation of the modem memory and I/O ports. Section 4.2 introduces the TMS320C50 memory. Section 4.3 describes the implementation of the modem memory. Section 4.4, 4.5 and 4.6 describe the interfacing of local program memory, local data memory and global data memory to the TMS320C50. Section 4.7 describes the I/O-selection circuit for access to I/O ports. Finally, Section 4.8 lists the problems that arise when different devices are communicating with each other.

4.2 TMS320C50 memory

The TMS320C50 external memory has been organized into four individually selectable spaces: program, local data, global data and input/output ports (I/O). These spaces provide an address range of 224K 16-bit words. The 64K program space contains the instructions to be executed. The 64K local data space stores data used by the instructions. The 32K global data space can share data with other processors within the system or can serve as additional data space. The 64K I/O-space interfaces to external memory-mapped peripherals and can also serve as extra data storage space.

The TMS320C50 has a 16-bit addressbus, so it can address up to 64K words. This is insufficient for addressing the available memory spaces. Therefore, the TMS320C50 has been equipped with four memory select signals:

- *PS (Program Select) for program memory,
- *DS (Data Select) for data memory,
- *IS (I/O Select) for I/O-memory,
- *BR (Bus Request) for global memory.

For example, addressing program memory for fetching an instruction results in generating a memory address in the range of 0 to 64K and activating *PS. External control logic uses the memory select signals to select the appropriate memory ICs.

For full speed, zero wait-states memory access, on-chip memory is available on the TMS320C50. This on-chip memory consists of 2K 16-bit words of boot ROM (Read Only Memory), 9K words of program/data SARAM (Single-access Random Access Memory) and 1056 words of data DARAM (Dual-access Random Access Memory). The on-chip boot ROM resides in program space at address 0 and contains a device test and boot code. The 9K block of SARAM can be mapped to program and/or data spaces and resides at address 800h in either space. The 1056 words of DARAM are configured in three blocks: block B0 and B1 consist of 512 words each and block B2 consists of 32 words. Block B0 can also be configured as program RAM (see Figure 4.1).

Figure 4.1 shows the TMS320C50 memory maps [5, p. 6-3].

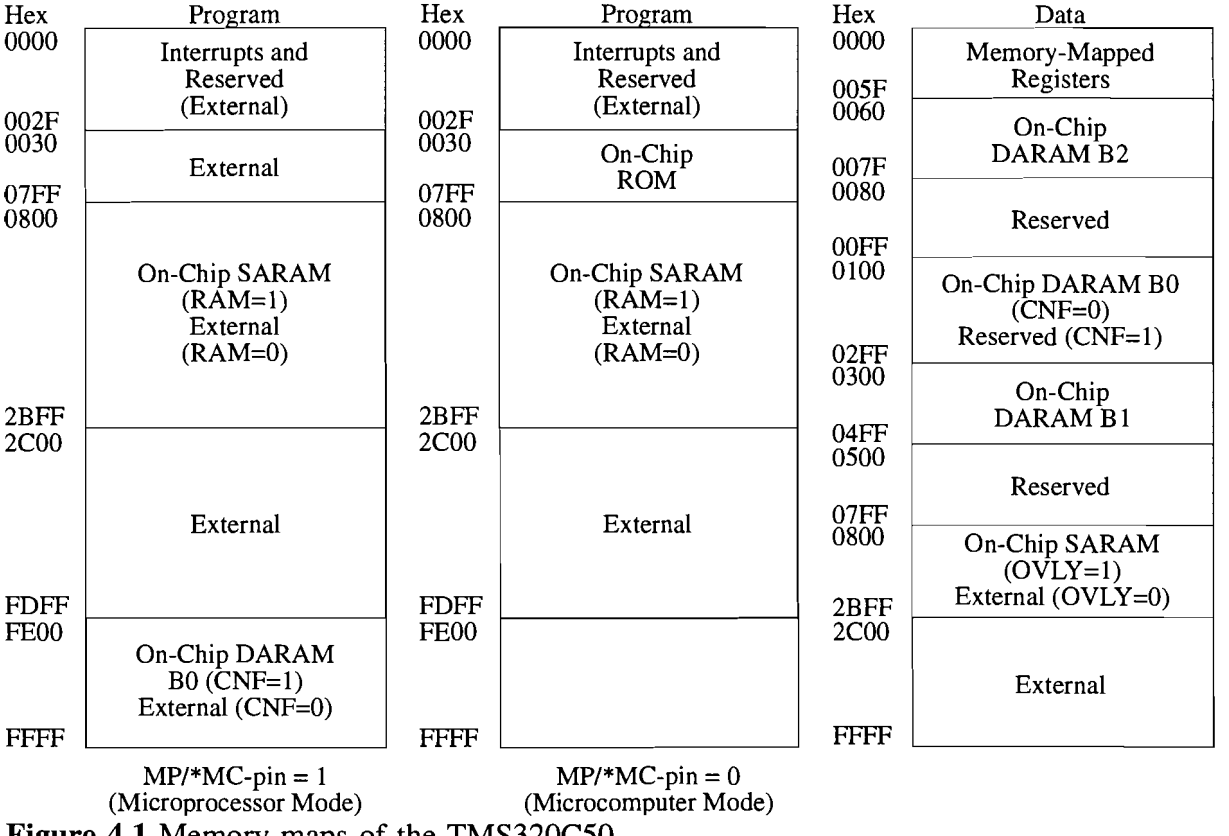


Figure 4.1 Memory maps of the TMS320C50.

The MP/*MC-pin (Microprocessor/Microcomputer mode-pin) can be used to enable/disable the on-chip ROM. If this pin is high, the TMS320C50 is configured as a microprocessor: the on-chip ROM is disabled and the device starts running from address 0 at off-chip memory. If this pin is low, the TMS320C50 is configured as a microcomputer: the on-chip ROM is enabled and the device starts running from on-chip ROM. The MP/*MC-pin is sampled only at reset.

4.3 Modem memory

The memory of the modem consists of local memory and global memory. Local memory consists of program and data memory used by one processor. Global memory consists of data memory used by both processors. The TMS320C50 program and data memory can both address up to 64K 16-bit words. In the modem configuration, the memory select signals *PS and *DS are not used. Therefore, only a total of 64K words are available for local and global memory.

The implementation of local memory uses two 32K 8-bit EPROMs (Erasable Programmable Read Only Memory) for program code and two 32K 8-bit Static RAMs (SRAMs) for program and data. From address 0h to 7FFFh, the EPROMs are addressed. From address 8000h to 7FFFh, Static RAM can be accessed. The EPROMs are mainly used for program code storage but can also contain look-up tables. The Static RAMs are mainly used for data storage. However, part of the 32K Static RAM can be reserved for program memory: by copying program code from slower EPROM to faster RAM, execution of program is faster. Because *PS and *DS are not used, any arbitrary partition of the 32K words RAM into program memory and data memory is allowed. Local program memory can be expanded by configuring the on-chip SARAM and block B0 of DARAM as program memory. Also, local data memory can be expanded by using the on-chip SARAM and block B1 and B2 of DARAM.

Part of the local data memory map can be configured as global memory. This is done in software using the "Global Memory Allocation Register" (GREG). Global memory is implemented with a 1K Dual-Port Static RAM (DPSRAM) consisting of a master and slave version. This DPSRAM provides simultaneous access to different memory locations. A 2K version of this DPSRAM is optional for it has the same pin configuration as the 1K version.

Figure 4.2 shows the modem memory map with the TMS320C50 configured as microprocessor. It is shown that the address range from 8000h to FFFFh can be divided in three parts:

- one part for program code : $8000h \leq address < xxxxh$
- one part for local data : $xxxxh \leq address < yyyyh$
- one part for global data : $yyyyh \leq address \leq FFFFh$

where *xxxx*h and *yyyy*h are defined as : $8000h \leq xxxxh < yyyyh$ and $F000h \leq yyyyh \leq FFFFh$.

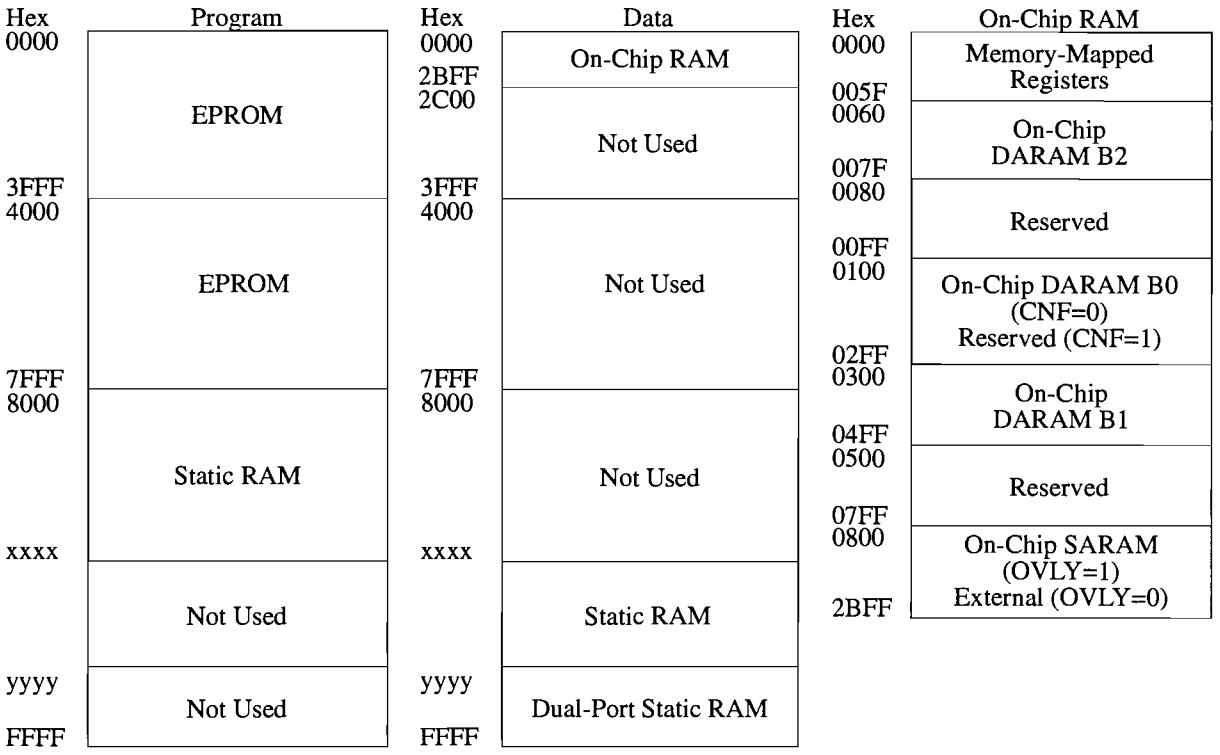


Figure 4.2 Practical memory maps of the modem.

The attentive reader may have noticed that the address ranges of SARAM and DARAM overlap the address range of the EPROM. Software can configure SARAM and DARAM to reside inside or outside the program/data address map. When they are mapped into program/data space, the TMS320C50 automatically accesses them when it addresses within their bounds. An address outside their bounds results in access to off-chip memory. Section 7.3 explains how on-chip memory is to be configured to reside in the memory map.

4.4 Implementing local program memory

4.4.1 Choosing an EPROM

The EPROM used is the AM27C256 EPROM. This EPROM is pin-compatible with the NMC27C256 EPROM used by Diederen[1]. The main reason to choose the AM27C256 instead of the NMC27C256 is the low price of the AM27C256. The features of this EPROM important to the modem design are listed below:

- 32K x 8-bit ultraviolet erasable programmable read only memory
- maximum access time of 150 ns
- maximum output disable time of 30 ns

- low power consumption: - active power : 80 mW.
  - standby power : 100 µW.
- *CE- and *OE-control signals, 15-bit address input, 8-bit data output

Detailed information about this EPROM can be found in Appendix 4, p. 171.

Before the EPROM can be interfaced to the TMS320C50, some design considerations are made:

- The EPROM is used to store program code. At reset, the TMS320C50 must be aware that program code is resided in EPROM and must start code execution from off-chip memory. This can be achieved connecting the MP/*MC-pin of the TMS320C50 to 5 Volts (see Section 4.2).

- Communication between EPROM and TMS320C50 will require wait-states. Therefore, execution of program code in EPROM cannot be recommended. To solve this speed problem, program code can be copied from slower EPROM to faster SARAM or external RAM. The Static RAM is used for local data storage but can also be used as program memory. In software, interrupt vectors which are located at address 0000h in EPROM, must be remapped to Static RAM. Otherwise, execution of interrupts is performed with wait states. Remapping interrupts is explained in Section 7.2.

- Although the EPROM is merely used for program code, it must also be possible to store data (constants) in EPROM. This data can only be read by the processor.

- The output disable time of the EPROM is too long to guarantee that no busconflicts will occur during other TMS320C50 external memory accesses. Therefore, the output pins of the EPROM must be connected to the TMS320C50 databus using buffer ICs.

4.4.2 Interfacing EPROM to the TMS320C50

The EPROM is a 32K x 8-bit IC. For a 16-bit databus, two EPROMs are used. The output disable time of the EPROMs is too long to guarantee that no busconflict will occur if two consecutive read cycles are executed (see Section 4.4.3 for more details on EPROM timing requirements and Section 4.8 for more information on consecutive reads). Therefore, two transceiver ICs (74F245) are used to buffer the datalines.

Figure 4.3 illustrates the TMS320C50s with the EPROMs connected.

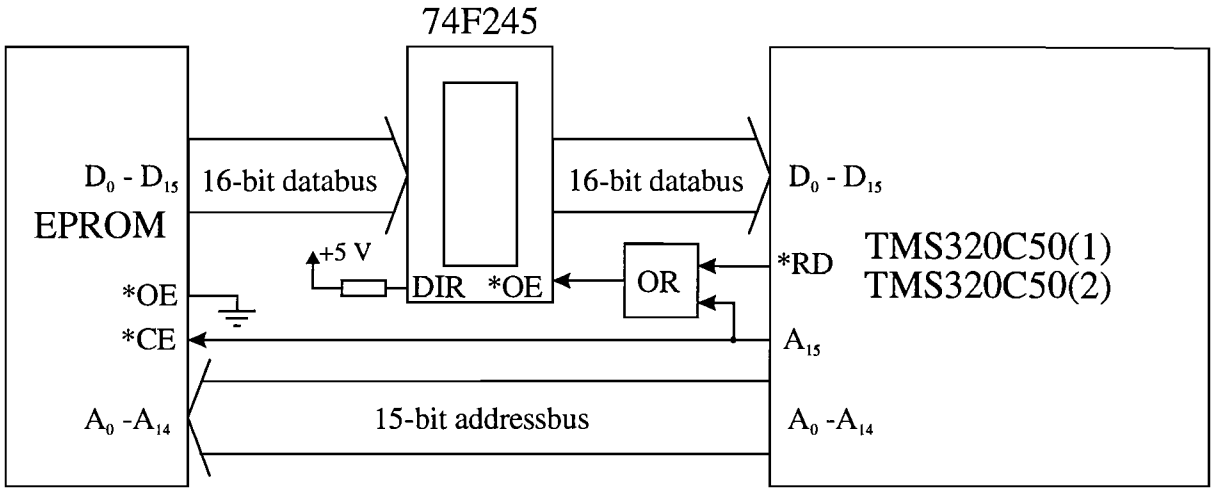


Figure 4.3 The TMS320C50s with the EPROMs.

The EPROM has been provided with a 15-bit addressbus and an 8-bit databus. Furthermore, it has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (*CE) is the power control and is used for device selection. Output Enable (*OE) is the output control and is used to gate data to the output pins.

As was mentioned in Section 4.3, the TMS320C50 provides the memory control signals *PS and *DS to distinguish program memory from data memory. *PS and *DS are useful if the address range of program memory overlaps the address range of data memory. In this case, it is not known which memory space is accessed when a memory address is generated. Therefore, *PS and *DS can be used to access the appropriate memory.

In the modem design, *PS and *DS are not used. From the address ranges of EPROM and Static RAM, it can be seen that the selection between these memory areas is made by addressline A_{15}.

In Section 4.4.1, it was recommended to use EPROM also for data storage. Selecting EPROM with A_{15} and *PS as was done by Diederen[1] implies the EPROM only to be used for program code. By omitting *PS, program code and data can be read from EPROM.

The attentive reader may have noticed that for proper operation the EPROMs can be continuously selected (i.e. *CE of the EPROM is always active low). In this case, the EPROM is always active and therefore dissipating 80 mW. By deselecting the EPROM, it

dissipates only 100 μW. Because the EPROM is only used during initialization, power can be saved by deselecting the EPROM.

Examining Figure 4.3, the attentive reader may also have noticed that if A_{15} is connected to *CE of the EPROM and to *OE of the transceiver IC, power as well as the OR-port for the selection of the transceiver ICs can be saved. For consecutive reads from EPROM, timing requirements are guaranteed. But for memory accesses to static RAM ICs, TMS320C50 write data can still be at the databus while selecting EPROM and therefore connecting the EPROM databus with the TMS320C50 databus.

The Output Enable (*OE) of the EPROM is connected to ground. Therefore, the EPROM databus is always low-impedant. This is not a problem because the datalines are buffered by two 74F245 transceiver ICs.

Read Select(*RD) of the TMS320C50 cannot be directly connected to the Output Enable of the 74F245 transceiver IC because this signal is also used when performing a read cycle to other devices. This will result in a busconflict that will either destroy the EPROMs, the transceiver ICs or the TMS320C50. This problem is solved by connecting *RD together with A_{15} using an OR-gate to *OE of the transceiver IC.

In the previous design of the modem made by Diederen[1], it was possible to write to the EPROM ICs. They were selected using *STRB together with *PS_LOW [1, p. 39]. *STRB becomes active low if an external memory access is done. So, a read cycle and a write cycle make *STRB active low. Therefore, writing to EPROM was possible. In the new design, this problem is solved because the TMS320C50 provides two extra signals for read and write cycles: Read Select (*RD) and Write Enable (*WE). Using only *RD for modem selection, writing to the EPROMs is made impossible.

4.4.3 EPROM Timing Requirements

A TMS320C50 operating at 28.57 MHz has a machine cycle of 35 ns. With the 25 MHz clock, the internal machine cycle of the TMS320C50 is 40 ns. Timing requirements tables listed in [5] define H as half a machine cycle, so H=20 ns and $2H$=40 ns.

Figure 4.4 shows the EPROM read cycle timing diagram together with the appropriate TMS320C50 timings. The relevant access and output disable times of the TMS320C50, the EPROM and the buffer IC are listed in Table 4.1.

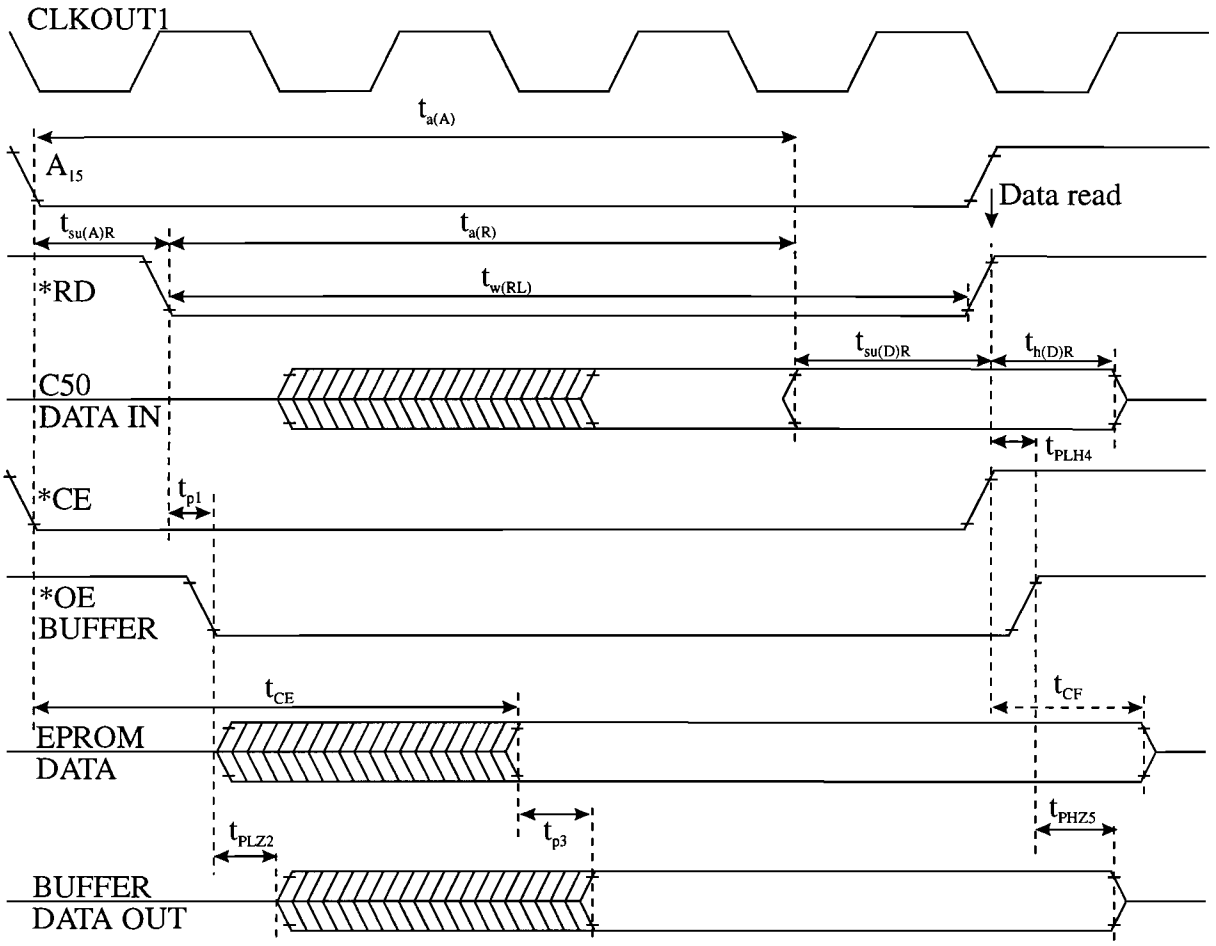


Figure 4.4 EPROM Read Cycle Timing Diagram.

Table 4.1 Relevant TMS320C50, EPROM, buffer and OR-gate timings.

Symbol	Parameter	Device	Min (ns)	Max (ns)
$t_{a(A)}$	Read data access from address valid	TMS320C50		$2H$-15 + n·$2H$
$t_{a(R)}$	Read data access time after *RD low	TMS320C50		H-10 + n·$2H$
$t_{su(A)R}$	Address valid before *RD low	TMS320C50	H-10	
t_{CE}	*CE Low to Output Valid	EPROM		150
t_{p3}	Propagation delay Input to Output	BUFFER	2.5	7.0
t_{PLH4}	*RD High to *OE High	OR-gate	3.0	6.6
t_{PHZ5}	*OE ↑ to Output High-Z	BUFFER	1.0	7.5

From Figure 4.4 and Table 4.1, the following two key timing requirements can be derived:

- The EPROM is selected using addressline A_{15}, so the key timing requirement is $t_{a(A)}$: the time read data can be accessed by the TMS320C50 after address becomes valid. After selection of the EPROM, it takes at most t_{CE} ns before data are on the EPROM output pins. After t_{p3} ns, data are transferred from the transceiver input pins to the transceiver output pins. For $t_{a(A)}$, the following relation must hold:

$$t_{CE,\ EPROM} + t_{p3,\ BUFFER} \leq t_{a(A),\max,\ TMS320C50} \tag{4.1}$$

- $t_{a(R)}$ is the time read data can be accessed by the TMS320C50 after *RD goes low. From Figure 4.4 it follows that in worst-case conditions, the following relation must be true:

$$t_{CE,\ EPROM} + t_{p3,\ BUFFER} \leq t_{su(A)R,\min,C50} + t_{a(R),\max,C50} \tag{4.2}$$

The access time of the EPROM is too long for the TMS320C50 to operate with zero wait states. For proper operation, the minimum number of wait-states must be calculated. Substituting H=20 and the values from Table 4.1 in (4.1) gives a minimum of 4 wait-states. However, the built-in software waitstate generator of the TMS320C50 can only be programmed with 0, 1, 2, 3 or 7 wait states. So, the EPROM is accessed using seven wait states. Because the EPROM is only accessed during initialization, seven wait states are not a problem. Section 7.5 explains how to program the wait-state generator.

By substituting n=7 in the TMS320C50 timings listed in Table 4.1, the reader can verify that timing requirements are met.

There are some more timing requirements to satisfy, concerning data setup times, data hold times and output enable and disable times. These timings and the remaining timings shown in Figure 4.4 are listed in Table 4.2.

Table 4.2 Other TMS320C50, EPROM, BUFFER and OR-gate timings.

Symbol	Parameter	Device	Min (ns)	Max (ns)
$t_{su(D)R}$	Read data setup time before *RD ↑	TMS320C50	10	
$t_{w(RL)}$	*RD low pulse duration	TMS320C50	H-2 + n·2H	H+2 + n·2H
$t_{h(D)R}$	Read data hold time after *RD high	TMS320C50	0	
t_{CF}	*CE High to Output High Z	EPROM		30
t_{pl}	*RD Low to *OE Low	OR-gate	3.0	6.3
t_{PLZ2}	*OE Low to Buffer output Low Z	BUFFER	2.0	9.0

- The TMS320C50 requires read data to be valid at least $t_{su(D)R}$ ns before the actual data is read. This requirement is guaranteed because data are valid within the time constraint of $t_{a(R),max}$.

- After *RD goes low, it takes at least 5.0 ns ($t_{pl,min}$ + $t_{PLZ2,min}$) before the databus becomes low-impedant. This timing is important when accessing other devices: previous data must be removed from the databus before the EPROMs are accessed. Section 4.8 describes the communication between (memory) devices.

- After the read operation, data may stay on the databus at least $t_{h(D)R}$ ns. In worst-case, data are on the databus for at most 14.1 ns ($t_{PLH4,max}$ + $t_{PHZ5,max}$). This timing is important when accessing other devices: EPROM data must be removed from the databus before other devices are accessed in order to prevent busconflicts. Section 4.8 describes the communication between (memory) devices.

- The EPROM databus becomes high-impedant after at most t_{CF} ns. Due to the separation of databuses by transceiver ICs, this timing is not important and busconflicts will not occur.

4.5 Implementing local data memory

4.5.1 Choosing a Static RAM IC

The IC used for implementing local data memory is the CY7C199 Static RAM (SRAM) IC. The features of this SRAM important to the modem design are listed below:

- 32K x 8-bit words
- maximum access time of 15 ns
- maximum output disable time of 7 ns
- automatic power-down feature, reducing the power consumption by 81% when deselected
- *CE-, *OE- and *WE-control signals
- 15-bit addressbus, 8-bit databus

The 15ns version of the CY7C199 was chosen for the following reasons:

- the CY7C199 was also used in the modem made by Diederen[1]
- the CY7C199-15ns satisfies TMS320C50 timing requirements
- access to the CY7C199 can be done using zero wait states
- the CY7C199-15ns was deliverable from stock.

4.5.2 Interfacing Static RAM to the TMS320C50

Figure 4.5 illustrates the TMS320C50s with the Static RAMs (SRAM) connected.

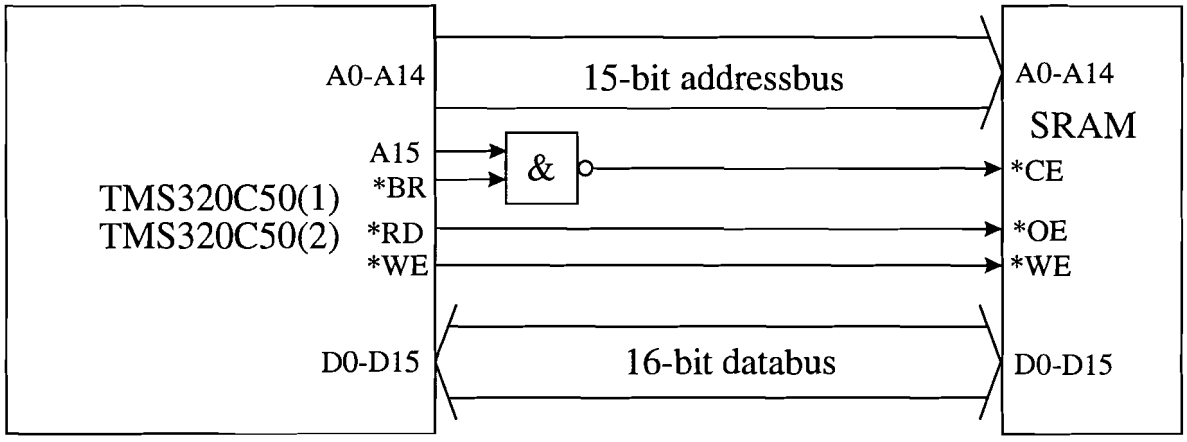


Figure 4.5 The TMS320C50s with the SRAMs.

The SRAM is a 32K x 8-bit IC. For a 16-bit databus, two SRAMs are used. The SRAM has three control functions:

- Chip Enable (*CE) is used for device selection.
- Output Enable (*OE) is used for enabling the I/O-pins for output when reading the device.
- Write Enable (*WE) is used for enabling the I/O-pins for input when writing to the device.

As was explained in Section 4.4.2, distinction between EPROM and SRAM is made using addressline A_{15}. But if a part of the local data memory map is configured as global memory, the address range of the SRAM also includes the Dual-Port SRAM. So, distinction between SRAM and Dual-Port SRAM must also be made. This distinction can be made using the Bus Request-pin (*BR) available on the TMS320C50. This pin is asserted low during access of the external global data memory space. Table 4.3 shows how the different memory devices can be selected using A_{15} and *BR.

Table 4.3 Memory Device Selection Table.

A_{15}	*BR	Memory Device
L	X	EPROM
X	L	DP-SRAM
H	H	SRAM

Note: X = Don't Care
L = Low Voltage
H = High Voltage

Table 4.3 shows that only if A_{15} and *BR are both asserted high, local data RAM is accessed. This function can be realized using a 2-input NAND-gate with its output connected to *CE of the CY7C199.

Diederen[1] used the *STRB and R/*W signals from the TMS320C25 DSP for selection of the CY7C199 SRAM IC. The TMS320C50 DSP has two additional memory interface signals to reduce the amount of external interfacing circuitries: *RD and *WE. The *RD pin is directly connected to the *OE pin of the CY7C199 and the *WE pin is directly connected to the *WE pin of the CY7C199. This alleviates the need of gating *STRB and R/*W to generate the equivalent signals.

4.5.3 SRAM Timing Requirements

Section 4.5.1 described the considerations leading to the choice of the CY7C199-15ns for local data memory. This section explains why the 15ns version of the CY7C199 was chosen based on timing requirements. This can be done using the read cycle timing diagram shown in Figure 4.6. Table 4.4 lists the relevant read cycle timings.

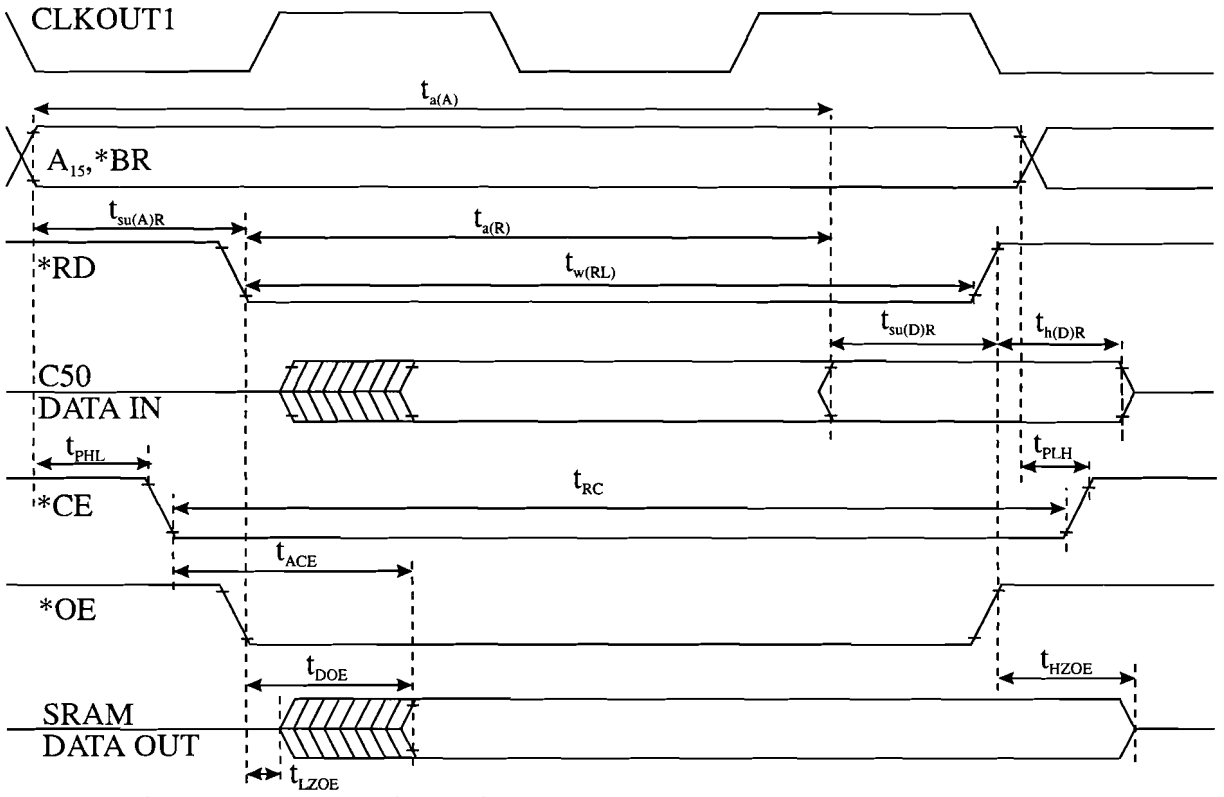


Figure 4.6 SRAM Read Cycle Timing Diagram.

Table 4.4 Relevant TMS320C50, NAND and SRAM read cycle timings.

Symbol	Parameter	Device	Min (ns)	Max (ns)
$t_{a(A)}$	Read data access from address valid	TMS320C50		$2H$-15 + n·$2H$
$t_{a(R)}$	Read data access time after *RD low	TMS320C50		H-10 + n·$2H$
t_{PHL}	A_{15}, *BR High to *CE Low	NAND	2.0	5.3
t_{ACE}	*CE Low to Data Valid	SRAM		15
t_{DOE}	*OE Low to Data Valid	SRAM		7

Important timings for the read cycle are $t_{a(A),max}$ and $t_{a(R)}$:

- $t_{a(A),max}$ is the maximum read data access time of the TMS320C50. After this time, data must be on the databus. The CY7C199 is selected using a NAND-gate, so the following relation must hold:

$$t_{ACE,max,SRAM} + t_{PHL,max,NAND} \leq t_{a(A),max,C50} \tag{4.3}$$

where $t_{ACE,max}$ is the maximum access time of the SRAM after *CE becomes valid and $t_{PHL,max,NAND}$ is the propagation delay of the NAND-gate.

Substituting the values of $t_{a(A),max}$ and $t_{PHL,max}$ from Table 4.4 in (4.3) gives the following relation for $t_{ACE,max}$:

$$t_{ACE,max} \leq (n+1)2H - 20.3 \quad (4.4)$$

Table 4.5 shows which versions of the CY7C199 satisfy (4.4) using zero or one waitstate.

Table 4.5 Allowable CY7C199 versions based on t_{ACE}.

# w.s.	t_{ACE}	-12	-15	-20	-25	-35	-45
n=0	19.7	X	X				
n=1	59.7	X	X	X	X	X	X

- $t_{a(R),max}$ is the maximum read data access time of the TMS320C50 after *RD is asserted low. The CY7C199 must put valid data on the databus within $t_{a(R),max}$ ns. The *RD-pin of the TMS320C50 is directly connected to the *OE-pin of the CY7C199, so the following relation must hold:

$$t_{DOE,max} \leq t_{a(R),max} \quad (4.5)$$

Substituting the value of $t_{a(R)}$ from Table 4.4 in (4.5) gives a second key timing requirement the CY7C199 must satisfy. Table 4.6 shows which versions of the CY7C199 satisfy (4.5) using zero or one waitstate.

Table 4.6 Allowable CY7C199 versions based on t_{DOE}.

# w.s.	t_{DOE}	-12	-15	-20	-25	-35	-45
n=0	10	X	X	X	X		
n=1	50	X	X	X	X	X	X

There are some more timing requirements to satisfy, concerning data setup times, data hold times and output disable times. These timings and the remaining timings shown in Figure 4.6 are listed in Table 4.7.

- The SRAM requires the read cycle time to be at least t_{RC} ns. This is the time the *CE-input of the SRAM is active low. *CE is related to the address timing, so the SRAM timing requirement is met because the address

Table 4.7 Other TMS320C50, NAND and SRAM timings.

Symbol	Parameter	Device	Min (ns)	Max (ns)
$t_{su(A)R}$	Address valid before *RD low	TMS320C50	H-10	
$t_{w(RL)}$	*RD low pulse duration	TMS320C50	H-2 + n·2H	H+2 + n·2H
$t_{su(D)R}$	Read data valid before *RD high	TMS320C50	10	
$t_{h(D)R}$	Read data hold after *RD high	TMS320C50	0	
t_{PLH}	A_{15} or *BR Low to *CE High	NAND	2.4	6.0
t_{RC}	Read Cycle Time	SRAM	15	
t_{LZOE}	*OE Low to Low Z	SRAM	0	
t_{HZOE}	*OE High to High Z	SRAM		7

is valid for at least one machine cycle.

- The TMS320C50 requires data to be valid at least $t_{su(D)R}$ ns before *RD is asserted high. This timing requirement is met because data are valid at most t_{DOE} after *OE goes active low and *OE stays active low for at least $t_{w(RL),min}$ ns.

- For proper operation, the SRAM requires the address to be valid prior to or coincident with *CE transition low. Because the *CE-input is connected to A_{15} and *BR using a 2-input NAND-gate, address is valid before *CE is asserted low.

From Table 4.5 and Table 4.6 it follows that the 12ns-version and the 15ns-version of the CY7C199 can be used when external read cycles are performed using zero or one wait states. The other versions can only be used when using one wait state. The aim is to perform external memory accesses without any wait states, so the 12ns-version and the 15ns-version of the CY7C199 are appropriate. The 15ns-version is chosen for it is deliverable from stock.

The CY7C199-15ns satisfies timing requirements concerning the memory read cycle. For the memory write cycle, timings must be checked in order to verify if the 15ns-version operates correctly.

Figure 4.7 shows the SRAM write cycle timing diagram. Table 4.8 lists the write cycle timings. The NAND-timings are not listed for they are the same as listed in Table 4.4.

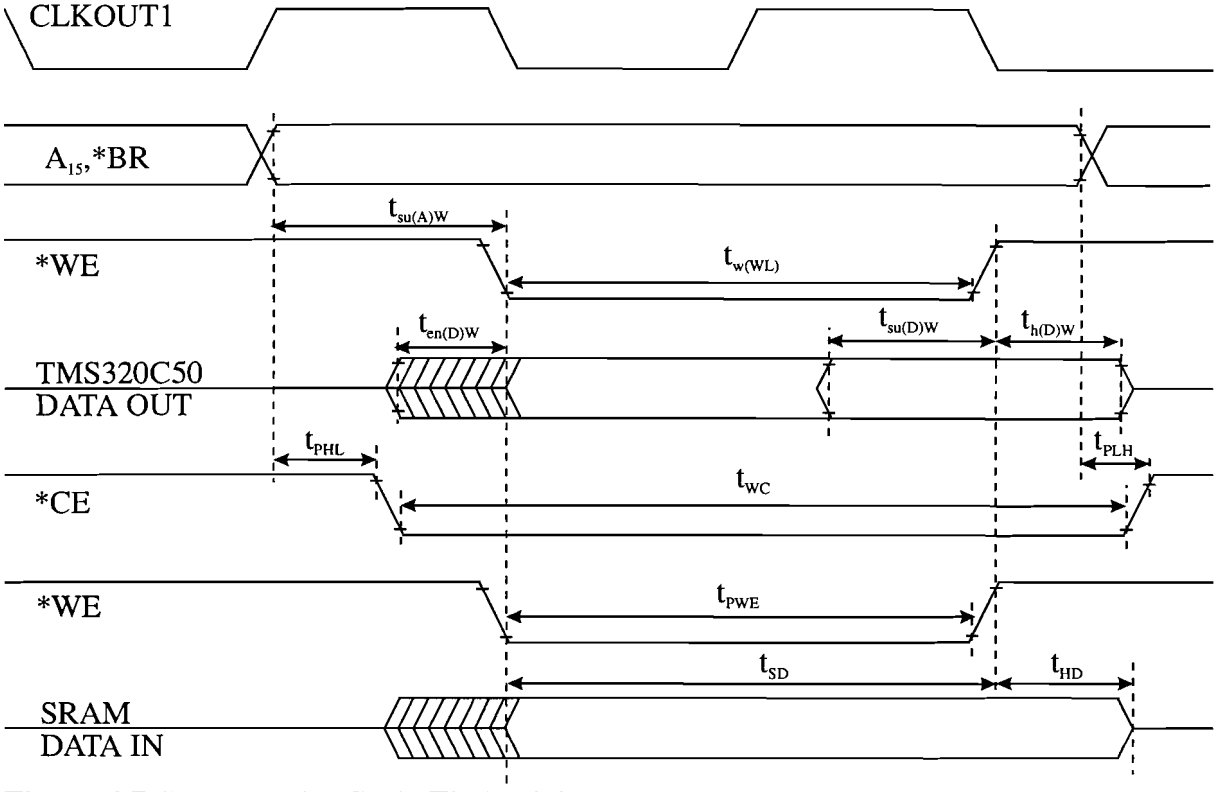


Figure 4.7 SRAM Write Cycle Timing Diagram.

Table 4.8 TMS320C50 and SRAM write cycle timings.

Symbol	Parameter	Device	Min (ns)	Max (ns)
$t_{su(A)W}$	Address valid before *WE low	TMS320C50	*H*-5	
$t_{w(WL)}$	*WE low pulse duration	TMS320C50	2*H*-2 + *n*·2*H*	2*H*+2 + *n*·2*H*
$t_{su(D)W}$	Write data valid before *WE high	TMS320C50	2*H*-20	2*H*
$t_{h(D)W}$	Write data hold time after *WE high	TMS320C50	*H*-5	*H*+10
$t_{en(D)W}$	Enable time, *WE to data bus high Z	TMS320C50	-5	
t_{WC}	Write Cycle Time	SRAM	15	
t_{PWE}	*WE Pulse Width	SRAM	9	
t_{SD}	Data Set-Up to Write End	SRAM	9	
t_{HD}	Data Hold from Write End	SRAM	0	

The important timing for the write cycle is $t_{su(D)W}$:

- $t_{su(D)W}$ is the time write data on the databus are valid before *WE is asserted high. For proper operation, $t_{su(D)W}$ must exceed t_{SD}, i.e. the time the SRAM wants write data to be on the databus. *WE of the TMS320C50 is directly

connected to the *WE-pin of the SRAM, so the following relation holds for the CY7C199-15ns:

$$t_{su(D)W} \geq t_{SD} \tag{4.6}$$

Substituting the values from Table 4.8 in (4.6) shows that the SRAM timing requirement is met.

There are two other important timings:

- The CY7C199 expects the *WE pulse width t_{PWE} to exceed 9 ns. From Table 4.8 it can be seen that the minimal TMS320C50 *WE low pulse duration $t_{w(WL)}$ exceeds the minimal CY7C199 *WE pulse width.
- $t_{h(D)W}$ is the time TMS320C50 write data are valid on the databus after *WE is asserted high. This timing is important when communicating with other (memory) devices in order to prevent busconflicts. Section 4.8 explains the importance of this timing.

4.6 Implementing global data memory

4.6.1 Choosing a global memory implementation

As was explained in Section 2.2, communication between processors can be done using global memory. In general, this type of memory permits two or more processors independent access to any location in memory. However, when processors want to access the same memory location, some form of arbitration scheme is necessary. This arbitration scheme must prevent simultaneous memory accesses at the same location in global data memory.

Figure 4.8 illustrates an example of a global memory interface. For the global data memory, the SRAM ICs from Section 4.5 could be used. In order to avoid busconflicts when both processors attempt to access the global memory, buffers are provided. Furthermore, arbitration logic is necessary to avoid access to the same memory locations. This global memory interface seems easy and logical. However, some problems arise when implementing this global memory interface in hardware.

For each processor, the databus and addressbus must be buffered. Using an 8-bit transceiver IC for a buffer, a total of eight transceiver ICs are necessary. Furthermore, four transceiver ICs must be bidirectional for buffering the databuses. The arbitration logic

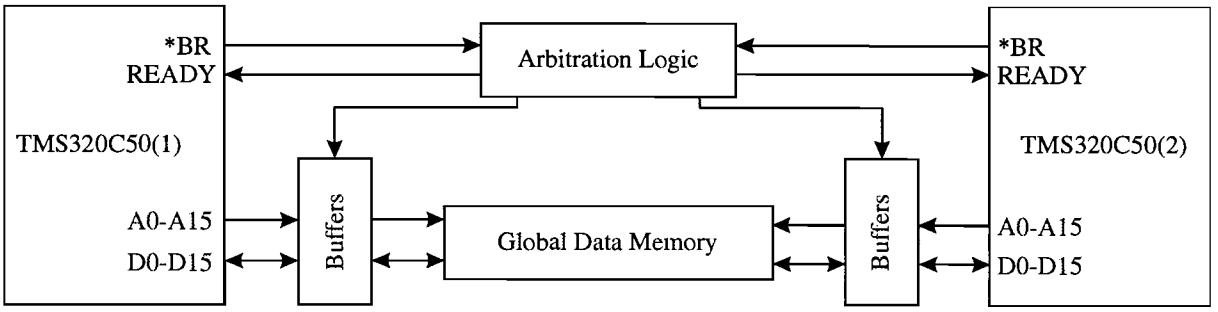


Figure 4.8 Global memory interface.

must be implemented in order to meet the following specifications:

- using the *BR-signal to enable communication between one processor and the global memory.
- determine whether data are transferred to or from the global memory.
- generate a READY-signal when both processors attempt to access the same memory location. When a processor receives the READY-signal, execution of program is halted for as long as READY is active, i.e. for as long as the other processor has access to the global memory.

For the latter specification, the READY-signal does not need to be generated when a semaphore construction is implemented. A semaphore is a protected variable whose value can be accessed and altered by one processor only.

When processor 1 wants to access global memory, it sets the semaphore. If access is granted (i.e. the semaphore variable is not used by other processes), the semaphore is reset and the processor can perform its alterations in global data memory. When processor 2 wants to access global memory, it checks if the semaphore is set. If it is already in use, the process is halted until the semaphore is returned by processor 1, i.e. when the semaphore is set. When the semaphore is returned, processor 2 can perform its alterations in global data memory.

If access to global memory is implemented using semaphores, integrity of global memory is guaranteed. However, when processors want to access different memory locations, semaphores are also used but not necessary.

If all the above considerations about the global memory interface have to be implemented in hardware, it takes a lot of time and effort to realize the interface. There is, however, a perfect solution to this problem: a Dual-Port Static RAM (DPSRAM) IC. A DPSRAM is a memory IC with two separate data- and addressbuses and separate control signals permitting independent access for reads and writes to any location in memory.

Furthermore, it is equipped with an arbitration logic to prevent two processors access to the same memory location at the same time.

The DPSRAM IC is chosen from Cypress Semiconductors. The reason to choose this IC is that interfacing and read and write timing requirements are the same as for the SRAM IC. To choose the appropriate DPSRAM IC for the modem design, advantages and disadvantages of the DPSRAM ICs were compared. The results are shown in Table 4.9.

Before choosing the appropriate DPSRAM, some considerations are made:

- Each DPSRAM has an 8-bit databus. In the modem configuration, a 16-bit databus is used. So, the DPSRAM must be able to expand the databus, i.e. using a master/slave construction.
- The DPSRAM must be equipped with either a Busy arbitration scheme or a semaphore construction to ensure that both processors will not access the same memory location simultaneously. The Busy logic signals that a processor is trying to access the same memory location currently being accessed by the other port. The semaphore construction permits software handshaking between processors.
- The DPSRAM must be deliverable from stock and no minimum number of ICs have to be purchased.

Table 4.9 The Cypress Semiconductor Dual-Port SRAM ICs.

	CY7C130 CY7C140	CY7C131 CY7C141	CY7C132 CY7C142	CY7C136 CY7C146	CY7B134	CY7B135	CY7B1342	CY7B138	CY7B139	CY7B144	CY7B145
# Memory	1Kx8 bits	1Kx8 bits	2Kx8 bits	2Kx8 bits	4Kx8 bits	4Kx8 bits	4Kx8 bits	4Kx8 bits	4Kx9 bits	8Kx8 bits	8Kx9 bits
Expand to 16-bits ?	Yes	Yes	Yes	Yes	No	No	No	Yes	Yes	Yes	Yes
access time	25, 30, 35, 45, 55	25, 30, 35, 45, 55	25, 30, 35, 45, 55	25, 30, 35, 45, 55	20, 25, 35	20, 25, 35	20, 25, 35	15, 25, 35	15, 25, 35	15, 25, 35	15, 25, 35
Control Signals *CE *R/*W *OE	 Yes Yes Yes	 Yes Yes Yes	 Yes Yes Yes	 Yes Yes Yes	 Yes Yes Yes	 Yes Yes Yes	 Yes Yes Yes	 Yes Yes Yes	 Yes Yes Yes	 Yes Yes Yes	 Yes Yes Yes
BUSY-arbitration	Yes	Yes	Yes	Yes	No	No	No	Yes	Yes	Yes	Yes
INT flag	Yes	Yes	No	Yes	No	No	No	Yes	Yes	Yes	Yes
Sem. Flag	No	No	No	No	No	No	Yes	Yes	Yes	Yes	Yes
Delivery from Stock?	Yes	Yes	No	No	?	?	?	No	No	?	?
Package	48-pin DIP/LCC/ QFP	52-pin PLCC/ LCC	48-pin DIP/LCC	52-pin PLCC/ LCC	48-pin DIP/LCC	52-pin PLCC/ LCC	52-pin PLCC/ LCC	68-pin PLCC/ LCC/PGA	68-pin PLCC/ LCC/PGA	68-pin PLCC/ LCC/PGA	68-pin PLCC/ LCC/PGA
Min. Delivery?	No	No	No	No	?	?	?	19 pieces	19 pieces	?	?

Note: ? = No information available.

From Table 4.9, the following conclusions can be made:

- the CY7B134/CY7B135 are not appropriate for they do not allow a 16-bit configuration. Furthermore, there is no *BUSY-pin, so simultaneous access to memory is possible.
- the CY7B1342 is not appropriate for it does not allow a 16-bit configuration. It is equipped with a *SEM-pin, so simultaneous access to memory can be made impossible in software.
- the CY7B138/CY7B144 are not appropriate because at least nineteen ICs have to be purchased.
- the CY7B139/CY7B145 are not appropriate for they have a 9-bit databus.
- the CY7C130/CY7C131/CY7C140/CY7C141 (=1Kx8 DPSRAM master/slave) and the CY7C132/CY7C136/CY7C142/CY7C146 (=2Kx8 DPSRAM master/slave) are appropriate for the modem design.

From the two appropriate DPSRAMs, the 1Kx8 version was deliverable from stock. To implement a 16-bit configuration, a master and a slave version are needed. From the 1Kx8 version, the appropriate pin configuration has to be chosen to expand the amount of global memory, if necessary. When comparing the pin configurations of the 1Kx8 and the 2Kx8 versions, the PLCC 52-pin version of both DPSRAMs have the same pin layout. However, the 2Kx8 version is equipped with two extra addresslines but the corresponding pins on the 1Kx8 version are not connected. In the modem configuration, the 1Kx8 version is used. If the amount of global memory is not satisfactory, the 2Kx8 version could be used.

The above considerations lead to the choice of the CY7C131 master DPSRAM and the CY7C141 slave DPSRAM. The features of the CY7C131/CY7C141 are listed again:

- 1K x 8-bit words
- maximum access time of 25 ns
- maximum output disable time of 15 ns
- automatic power-down feature
- *CE-, *OE- and R/*W-control signals
- 10-bit addressbus, 8-bit databus
- *BUSY and *INT flags.

Section 4.6.3 will show that the 25ns version of the CY7C131/CY7C141 satisfies TMS320C50 timing requirements.

4.6.2 Interfacing DPSRAM to the TMS320C50s

Figure 4.9 shows the DPSRAMs connected to the TMS320C50s.

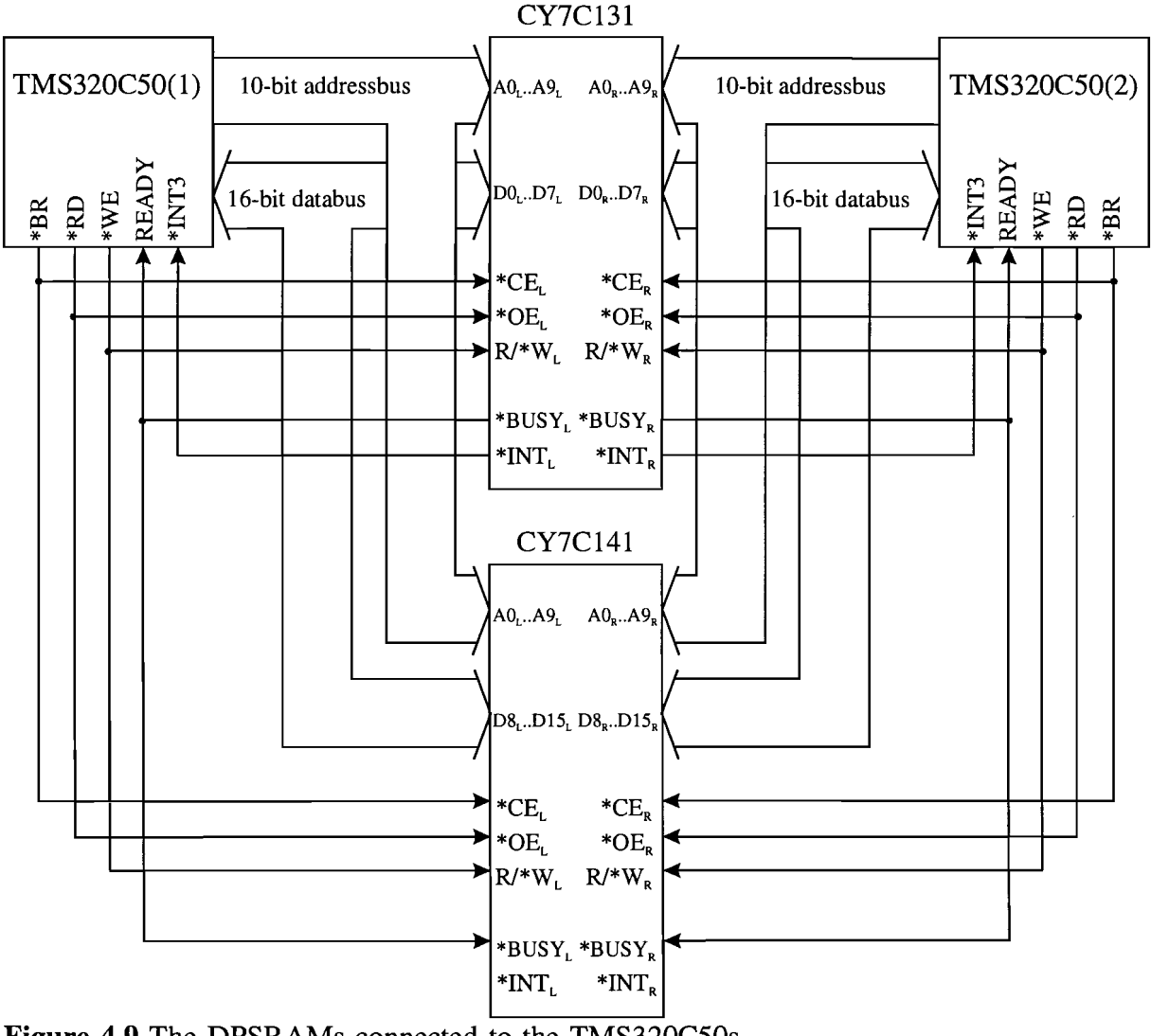


Figure 4.9 The DPSRAMs connected to the TMS320C50s.

The DPSRAM is a 1K x 8-bit IC. For a 16-bit databus, a master (CY7C131) and a slave (CY7C141) version are used. The DPSRAM is provided with a 10-bit addressbus and an 8-bit databus. It has five control functions:

- Chip Enable (*CE) is used for device selection.
- Output Enable (*OE) is used for enabling the I/O-pins for output when reading the device
- Read/Write Enable (R/*W) is used for enabling the I/O-pins for input when writing to the device.

- *$BUSY_L$ and *$BUSY_R$ are used to control simultaneous memory location access. If both ports' *CE are asserted low, the Busy logic will determine which port has access.
- *INT_L and *INT_R permit communication between ports. When the left port writes to location FFFh, the right port's interrupt flag (*INT_R) is set. This flag is cleared when the right port reads that same location. Setting the left port's interrupt flag (*INT_L) is accomplished when the right port writes to location FFEh. This flag is cleared when the left port reads location FFEh.

As was shown in Table 4.3, global memory is accessed if and only if *BR is asserted low. So, *BR is directly connected to *CE. As was done with the SRAM in Section 4.5.2, the TMS320C50 *RD and *WE signals are directly connected to *OE and R/*W pins of the DPSRAM.

The *BUSY output pins of the master DPSRAM are connected to the *BUSY input pins of the slave DPSRAM and to the READY input pins of the TMS320C50s. When both processors are attempting to access the same memory location, the Busy logic of the master DPSRAM will assert *BUSY low, thus inserting wait states to the TMS320C50. If the slave would not have been provided with the outcome of the Busy logic of the master, memory contention in the slave will occur. This will probably result in destruction of the DPSRAM IC or the TMS320C50.

The *INT pins of the master DPSRAM are connected to the *INT3 input pins from the TMS320C50. Only the *INT pins from the CY7C131 DPSRAM are used because writing to FFFh or FFEh results in interrupts from both DPSRAMs and an interrupt from only one DPSRAM is required.

4.6.3 DPSRAM Timing Requirements

Section 4.6.1 described the considerations leading to the choice of the CY7C131/CY7C141-25ns for global data memory. This section explains why the 25ns version of the DPSRAM was chosen based on timing requirements. This can be done using the read cycle timing diagram shown in Figure 4.10. The relevant read cycle timings are listed in Table 4.10.

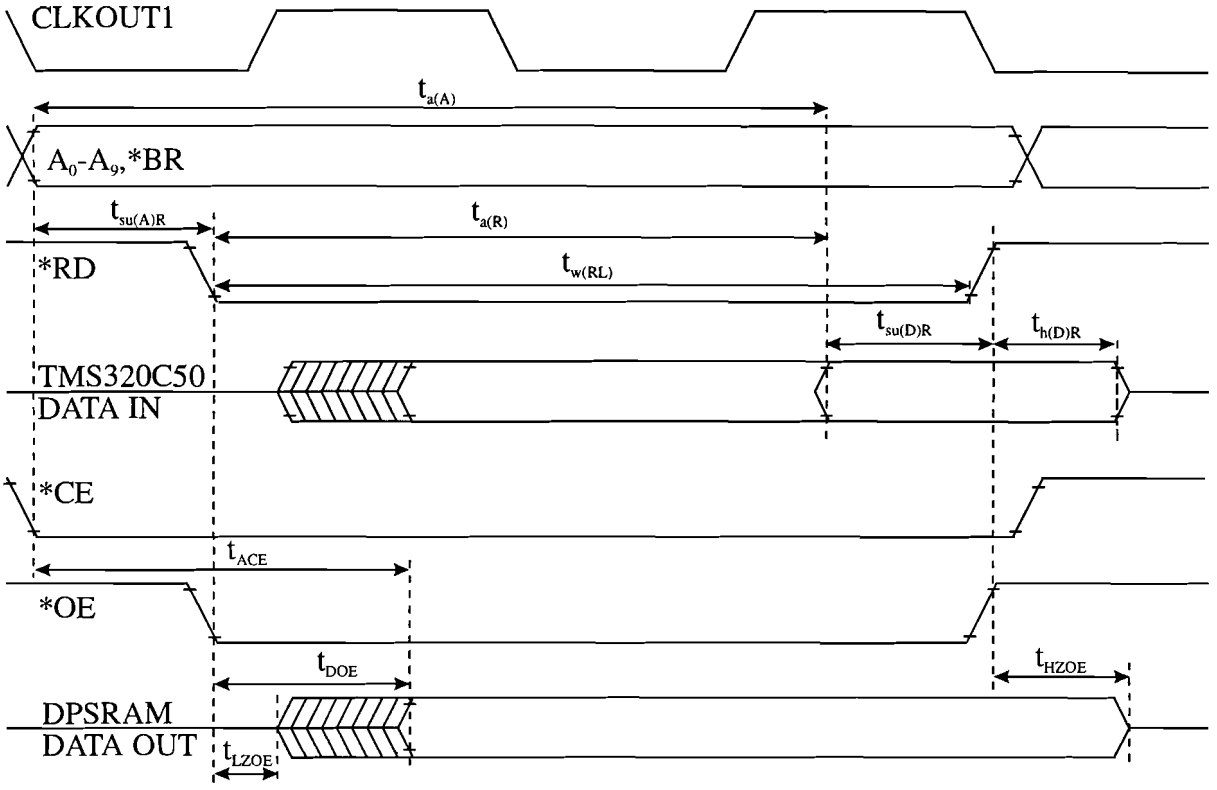


Figure 4.10 DPSRAM Read Cycle Timing Diagram.

Table 4.10 Relevant TMS320C50 and DPSRAM read cycle timings.

Symbol	Parameter	Device	Min (ns)	Max (ns)
$t_{a(A)}$	Read data access from address valid	TMS320C50		$2H$-15 + n·$2H$
$t_{a(R)}$	Read data access time after *RD low	TMS320C50		H-10 + n·$2H$
t_{ACE}	*CE Low to Data Valid	DPSRAM		25
t_{DOE}	*OE Low to Data Valid	DPSRAM		15

The derivations for the read and write cycle timing requirements are the same as for the CY7C199 from Section 4.5.3. In this section, only the formulas are presented.

Important timings for the read cycle are $t_{a(A),max}$ and $t_{a(R)}$:

- $t_{a(A),max}$: the CY7C131/CY7C141 are selected using the *BR-signal. Timings for the *BR signals are the same as for address timings, so the following relation must hold:

$$t_{ACE,max,DPSRAM} \leq t_{a(A),max,TMS320C50} \tag{4.7}$$

where $t_{ACE,max}$ is the maximum access time of the DPSRAM after address becomes valid. When substituting the value of $t_{a(A),max}$ from Table 4.10 in (4.7), an overview can be made of CY7C131/CY7C141 versions that satisfy (4.7) using zero or one waitstate. This overview can be found in Table 4.11.

Table 4.11 Allowable CY7C131/CY7C141 versions based on t_{ACE}.

# w.s.	t_{ACE}	25	30	35	45	55
n=0	25	X				
n=1	65	X	X	X	X	X

- $t_{a(R),max}$: the *RD-pin of the TMS320C50 is directly connected to the *OE-pin of the CY7C131/CY7C141, so the following relation must hold:

$$t_{DOE,max,DPSRAM} \leq t_{a(R),max,C50} \tag{4.8}$$

Substituting the value of $t_{a(R)}$ from Table 4.10 in (4.8) gives a second key timing requirement the CY7C131/CY7C141 must satisfy. Table 4.12 shows which versions of the CY7C131/CY7C141 satisfy (4.8) using zero or one waitstate.

Table 4.12 Allowable CY7C131/CY7C141 versions based on t_{DOE}.

# w.s.	t_{DOE}	25	30	35	45	55
n=0	10					
n=1	50	X	X	X	X	X

There are some more timing requirements to satisfy, concerning data setup times, data hold times and output disable times. These timings and the remaining timings shown in Figure 4.10 are listed in Table 4.13. Descriptions of these timings are listed in Section 4.5.3.

Table 4.13 Other TMS320C50 and DPSRAM timings.

Symbol	Parameter	Device	Min (ns)	Max (ns)
$t_{su(A)R}$	Address valid before *RD low	TMS320C50	H-10	
$t_{w(RL)}$	*RD low pulse duration	TMS320C50	H-2 + n·2H	H+2 + n·2H
$t_{su(D)R}$	Read data valid before *RD high	TMS320C50	10	
$t_{h(D)R}$	Read data hold after *RD high	TMS320C50	0	
t_{LZOE}	*OE Low to Low Z	DPSRAM	3	
t_{HZOE}	*OE High to High Z	DPSRAM		15

From Table 4.11 and Table 4.12 it follows that the fastest DPSRAM will only operate using one wait state. So, the 25 ns version of the CY7C131/CY7C141 is chosen for the modem design.

The CY7C131/CY7C141-25ns satisfies timing requirements concerning the memory read cycle. For the memory write cycle, timings must be checked in order to verify if the TMS320C50 satisfies DPSRAM write timing requirements.

Figure 4.11 shows the DPSRAM write cycle timing diagram. Table 4.14 lists the write cycle timings.

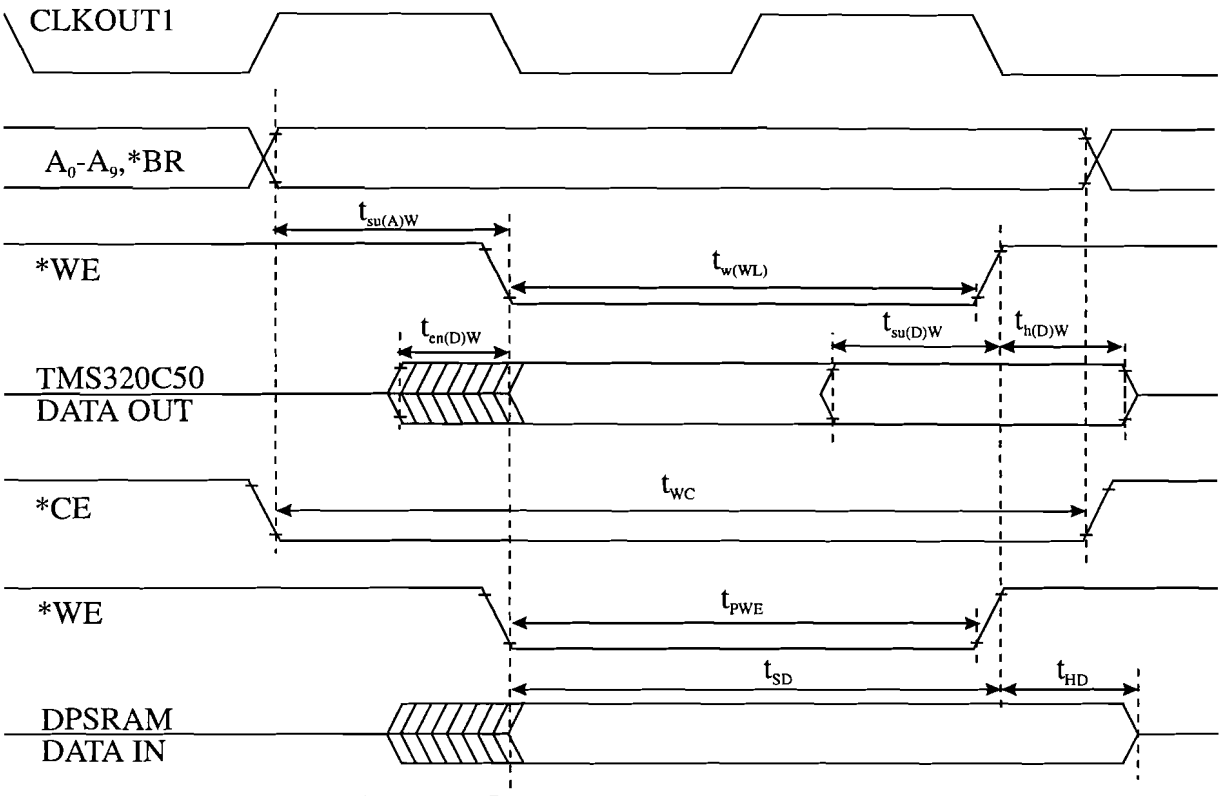


Figure 4.11 DPSRAM Write Cycle Timing Diagram.

Table 4.14 TMS320C50 and DPSRAM write cycle timings.

Symbol	Parameter	Device	Min (ns)	Max (ns)
$t_{su(A)W}$	Address valid before *WE low	TMS320C50	*H*-5	
$t_{w(WL)}$	*WE low pulse duration	TMS320C50	2*H*-2 + *n*·2*H*	2*H*+2 + *n*·2*H*
$t_{su(D)W}$	Write data valid before *WE high	TMS320C50	2*H*-20	2*H*
$t_{h(D)W}$	Write data hold time after *WE high	TMS320C50	*H*-5	*H*+10
$t_{en(D)W}$	Enable time, *WE to data bus high Z	TMS320C50	-5	
t_{WC}	Write Cycle Time	DPSRAM	25	
t_{PWE}	*WE Pulse Width	DPSRAM	15	
t_{SD}	Data Set-Up to Write End	DPSRAM	15	
t_{HD}	Data Hold from Write End	DPSRAM	0	

The important timing for the write cycle is $t_{su(D)W}$:

- $t_{su(D)W}$: for proper operation, $t_{su(D)W}$ must exceed t_{SD}. *WE of the TMS320C50 is directly connected to the R/*W-pin of the DPSRAM, so the following relation holds for the CY7C131/CY7C141-25ns:

$$t_{su(D)W} \geq t_{SD} \tag{4.9}$$

  Substituting the values from Table 4.14 in (4.9) shows that the DPSRAM timing requirement is met.

There is one more timing requirement to satisfy:

- The DPSRAM expects the R/*W pulse width to exceed t_{PWE} ns. From Table 4.14 it can be seen that the minimal TMS320C50 *WE low pulse duration exceeds the minimal DPSRAM R/*W pulse width.

So far, this section showed that the DPSRAM-25 ns satisfies TMS320C50 timing requirements based on memory read and write cycles. However, the DPSRAM also communicates with the TMS320C50 using the *BUSY and *INT signals. These timings must also satisfy TMS320C50 timing requirements.

The datasheets of the TMS320C50 list the interrupt timings [5, p. A-17]. The minimum low pulse duration of an interrupt (either synchronous or asynchronous) is $6H$+15 ns, i.e. three machine cycles. This timing requirement must be met to ensure that an interrupt is synchronized as explained in Section 2.3.10. According to Section 4.6.2, the DPSRAM interrupt is set when a write is performed to a specified location (FFFh for the left port and FFEh for the right port). This interrupt is cleared when the location is read. Reading memory can only be performed from the interrupt service routine which can only be executed when the interrupt was received successfully. So, due to the DPSRAM's interrupt generation logic, interrupt timing requirements are met.

When a processor wants to access global memory, it asserts the bus request (*BR) signal low. However, it is not aware if the other processor wants to access the global memory at the same time or if it has already access to the global memory. To prevent simultaneous access to the same memory location, the master DPSRAM is provided with an arbitration logic. The arbitration logic determines which processor may access the global memory. The master DPSRAM is provided with a *BUSY output pin which is asserted either high or low according to the outcome of the arbitration logic. When a processor's access to global memory is denied, the *BUSY output is asserted low. Because the *BUSY output is connected to the READY input of the TMS320C50, the processor will know when

access to the DPSRAM is denied and will delay its memory access until *BUSY goes high again (i.e. access to the DPSRAM is granted).

Figure 4.12 shows the *BUSY timing diagram of the CY7C131/141.

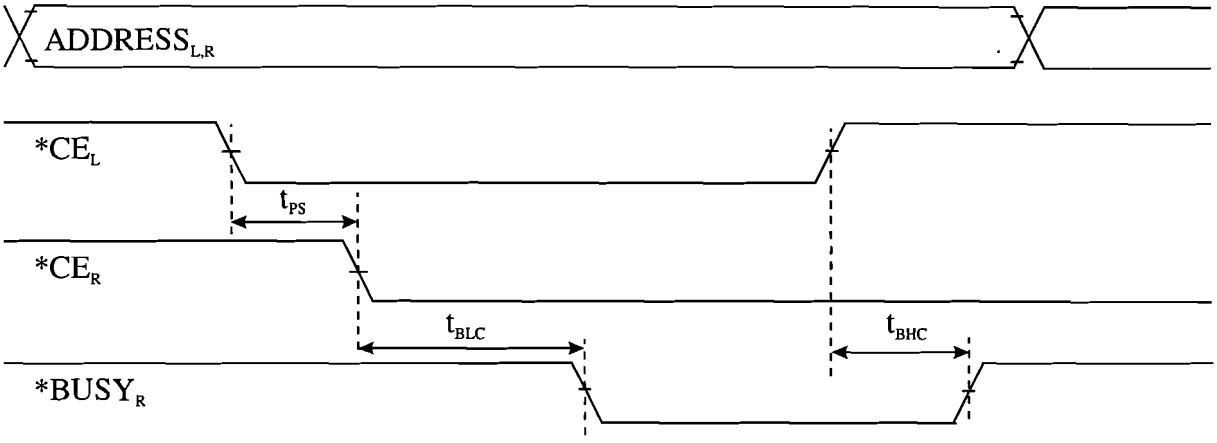


Figure 4.12 DPSRAM Busy Timing Diagram.

If both *CEs are asserted low and an address match occurs within 5 ns (t_{PS}) of each other, the *BUSY logic will determine which processor has access. *BUSY will be asserted low t_{BLC} ns ($t_{BLC} \leq 20$ ns) after *CE is taken low. Figure 4.12 shows that the left port gets access to the DPSRAM so the right port's *BUSY is asserted low. The timing diagram and the timings are the same when the right port gets access to the DPSRAM.

Before checking *BUSY timings with READY timing requirements, a general description of generating wait states using the READY signal is given. The READY input on the TMS320C50 is used for externally generating wait states. The TMS320C50 samples the READY pin at the rising edge of CLKOUT1. If READY is low, the TMS320C50 waits one machine cycle and samples READY again. If READY is high, the TMS320C50 concludes its external memory cycle. The external READY pin is sampled only after the internal software wait states are completed.

For a TMS320C50 read cycle, *RD goes low at the rising edge of CLKOUT1, i.e. at the same time the READY pin is sampled. READY must be stable some time before and after the rising edge of CLKOUT1 to prevent unwanted wait states to be inserted or wanted wait states to be skipped. A zero wait-state memory access contains one rising edge and one falling edge of CLKOUT1. At the rising edge, *RD goes low and READY is sampled. At the falling edge, data are read. So, if a zero wait-state memory access is to be delayed with externally generated wait states, READY must be low before *RD falls (i.e. the rising edge of CLKOUT1) otherwise READY is sampled high and no wait states are inserted.

Figure 4.13a shows a zero wait-state read cycle with READY low before the rising edge of CLKOUT1. Figure 4.13b shows the same read cycle with READY low after the rising edge of CLKOUT1.

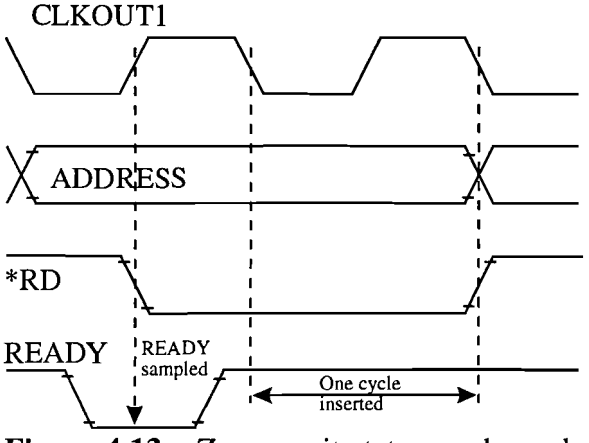


Figure 4.13a Zero wait-state read cycle with one external wait state.

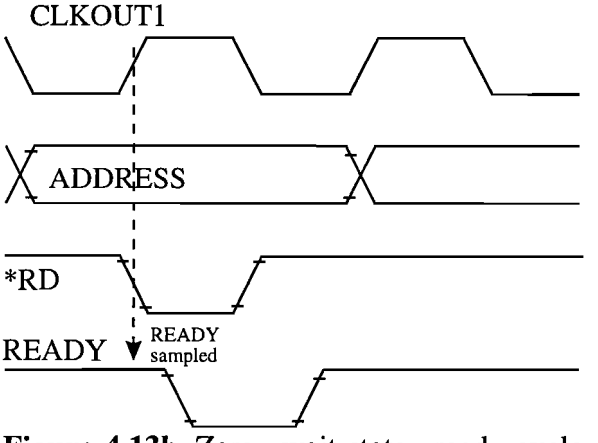


Figure 4.13b Zero wait-state read cycle with no external wait states.

In Figure 4.13a, READY is low before the rising edge of CLKOUT1, i.e. the time READY is sampled. Therefore, an extra wait state is inserted. In Figure 4.13b, READY goes low after the rising edge of CLKOUT1. The TMS320C50 samples READY as being high, so no extra wait state is inserted. Data are read at the falling edge of CLKOUT1.

A multiple wait-state memory access contains several rising and falling edges of CLKOUT1. To insert external wait-states, READY must be low before the last rising edge of CLKOUT1 before data are supposed to be read by the processor. Figure 4.14 shows a read cycle delayed by one internally generated wait state and by one READY-generated wait state. Timings are listed in Table 4.15.

Because the external READY input is sampled only after the internal software wait state is completed, READY may change during the extended read cycle. However, it must be low before the last rising edge of CLKOUT1 of the read cycle. At this point in time, the internal software wait state is completed and the external READY input is sampled. Figure 4.14 shows that READY is low, so an extra wait state is inserted. If more wait states are to be inserted, READY must stay low. If not, READY must go high before the next rising edge of CLKOUT1. Figure 4.14 shows that only one external wait state is inserted because READY is high before the last rising edge of CLKOUT1.

For a TMS320C50 write cycle, *WE goes low at the falling edge of CLKOUT1. READY is sampled at the rising edge of CLKOUT1. For correct insertion of wait states, the TMS320C50 expects READY to be low after *WE falls. Figure 4.15 shows a one wait-

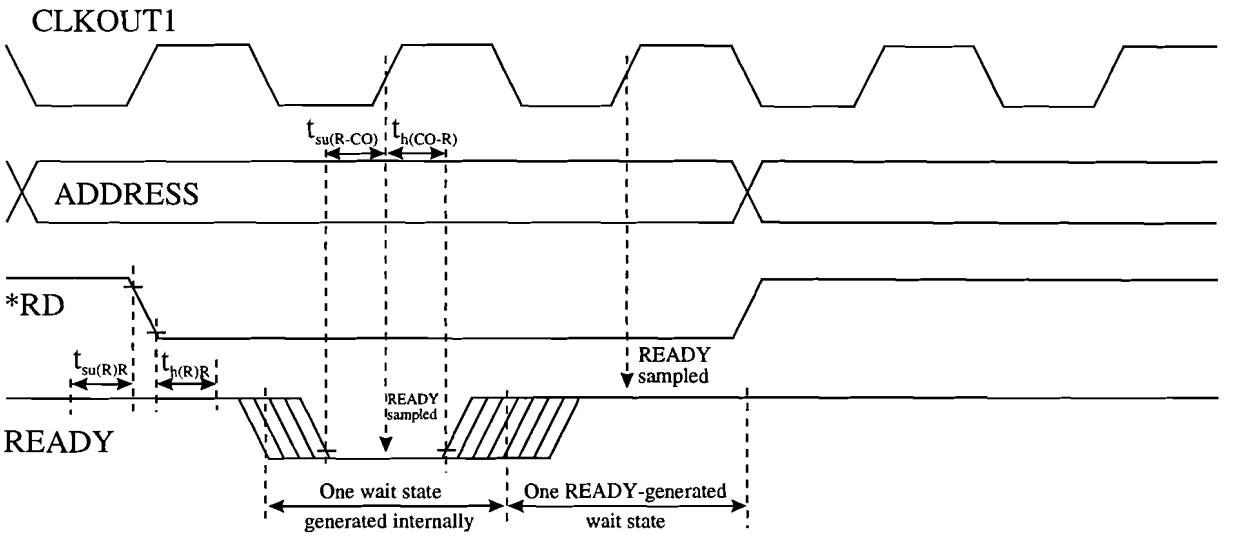


Figure 4.14 One wait-state read cycle delayed by one READY-generated wait state.

state write cycle delayed by one READY-generated wait-state. Timings are listed in Table 4.15. READY may change during the internal wait state but must be low before READY is sampled at the last rising edge of CLKOUT1 before *WE goes high again. In this way, the write cycle is delayed with one wait state. At the next rising edge of CLKOUT1, READY is high again so no wait states are inserted. For a zero wait-state write cycle, READY must be low before and after the rising edge of CLKOUT1 before *WE goes high.

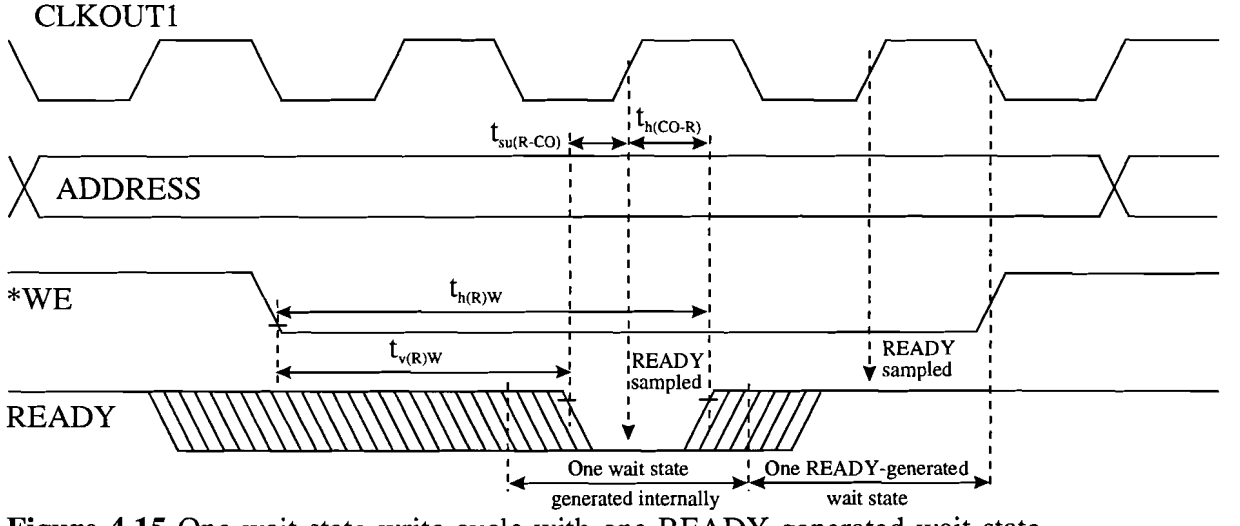


Figure 4.15 One wait-state write cycle with one READY-generated wait-state.

Using the timings from Table 4.15 and Figure 4.12, READY timing requirements for the DPSRAM can be derived. Access to the DPSRAM is done using one wait state. *BUSY goes low after at most 20 (= t_{BLC}) ns. Figure 4.14 shows that READY must be low after

Table 4.15 Ready timing requirements.

Symbol	Parameter	Min (ns)
$t_{su(R-CO)}$	READY setup time before CLKOUT1 rises	10
$t_{h(CO-R)}$	READY hold time after CLKOUT1 rises	0
$t_{su(R)R}$	READY setup time before *RD falls	10
$t_{h(R)R}$	READY hold time after *RD falls	5
$t_{v(R)W}$	READY valid after *WE falls	*H*-15
$t_{h(R)W}$	READY hold after *WE falls	*H*+5

1½ machine cycle from ADDRESS valid. Figure 4.15 shows that READY must be low after 2½ machine cycles from ADDRESS valid. Due to the internal wait state, READY will be low in time before it is sampled, therefore READY timing requirements are met.

4.7 I/O-selection circuit

The TMS320C50 has a total of 64K addresses for parallel input/output ports. I/O port accesses are defined as accesses during which the I/O-select signal (*IS) is active. Accessing the I/O ports can be done with the IN and OUT instruction. In [1], an I/O-selection circuit has been designed to access the A/D converter, the D/A converter, the parallel port and the DIP-switches. The I/O-selection circuit is illustrated in Figure 4.16. The I/O-selection is accomplished by the 74F138 1-of-8 decoder. It accepts addresslines A_0 and A_1 and the control signal R/*W of the TMS320C50 as inputs and when enabled, provides eight active low outputs. The device is enabled by *STRB and by *IS.

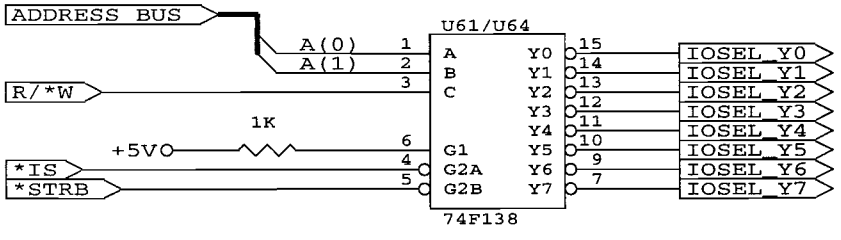


Figure 4.16 I/O-selection circuit.

Each TMS320C50 is interfaced to an I/O-selection circuit. The I/O-selection circuit is the same as was used with the previous modem. The port addresses of TMS320C50(1) and TMS320C50(2) are listed in Table 4.16 and Table 4.17.

Table 4.16 I/O port addresses TMS320C50(1).

Port address	IN operation	OUT operation
0h	to connector (*Y4)	to connector (*Y0)
1h	16-bit parallel interface (*Y5)	16-bit parallel interface (*Y1)
2h	A/D converter (*Y6)	to connector (*Y2)
3h	to connector (*Y7)	to connector (*Y3)

Table 4.17 I/O port addresses TMS320C50(2).

Port address	IN operation	OUT operation
0h	to connector (*Y4)	to connector (*Y0)
1h	communication interface (*Y5)	communication interface (*Y1)
2h	A/D converter (*Y6)	D/A converter (*Y2)
3h	to connector (*Y7)	to connector (*Y3)

In the modem configuration, the I/O-select signals are used to read from and write to internal devices (A/D converter, D/A converter, 16-bit parallel interface, communications interface) and to external devices by means of I/O-select signals which are situated on the 2x32-pin connector CONN1. The I/O-select signals can be used on the high-to-low transition or the low-to-high transition. When reading the devices, the high-to-low transition is used to reset flip-flops and to enable the output pins of buffer ICs. When writing the devices, the low-to-high transition is used to clock data into the buffers ICs. The next paragraph will show that reading and writing the devices is justified because data are valid at the time they are clocked in.

Figure 4.17 shows the I/O-selection read timing diagram. Table 4.18 lists the I/O-selection timings. The inputs A_0, A_1, R/*W and *IS are all referenced as ADDRESS timings.

For read cycles, *STRB goes low and ADDRESS becomes valid with the falling edge of CLKOUT1. Due to the internal device logic used to generate ADDRESS relative outputs (A_0, A_1, *IS, R/*W), transitions on the addressbus and related outputs typically occur somewhat later than control-line transitions (CLKOUT1, *STRB, *WE, *RD). Therefore, *IS activates the *Y_n outputs. After $t_{PHL,max}$ ns from ADDRESS valid, the I/O-select signal *Y_n ($0 \leq n \leq 7$) becomes active. If *Y_n is used to enable the output pins of the buffer ICs, it is the task of these buffer ICs to present valid data before *STRB goes high again. If

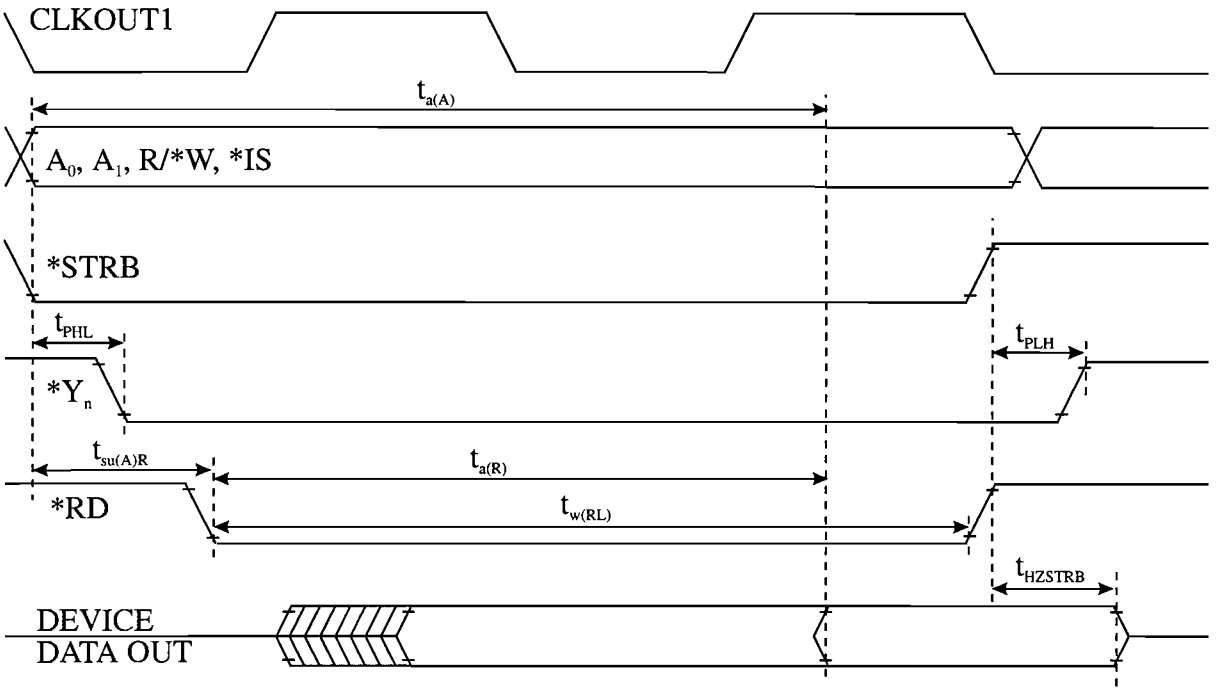


Figure 4.17 I/O-selection Read Timing Diagram.

Table 4.18 I/O-selection Read Timings.

Symbol	Parameter	Device	Min (ns)	Max (ns)
$t_{a(A)}$	Read data access from address valid	TMS320C50		$2H$-15 + n·$2H$
$t_{a(R)}$	Read data access from *RD valid	TMS320C50		H-10 + n·$2H$
$t_{su(A)R}$	Address valid before *RD low	TMS320C50	H-10	
$t_{w(RL)}$	*RD low pulse duration	TMS320C50	H-2 + n·$2H$	H+2 + n·$2H$
t_{PHL}	Propagation delay A, B, C	74F138	4.0	9.0
t_{PLH}	Propagation delay A, B, C	74F138	3.5	8.0
t_{HZSTRB}	*STRB High to High Z	Others		-

necessary, a read cycle can be extended by implementing I/O-port wait states in software.

Figure 4.18 shows the I/O-selection write timing diagram. Table 4.19 lists the I/O-selection timings. For the write cycle, ADDRESS is valid for at least $t_{su(A)W}$ ns before *STRB becomes active. So, *STRB determines the I/O-select signal timing. After $t_{PHL,max}$ ns from *STRB valid, *Y_n becomes active. For the write cycle, the low-to-high transition of *Y_n is important. On the rising edge of *STRB, it takes at most t_{PLH} ns before *Y_n is asserted high. After *Y_n goes high, data are valid for at least 7.0 ($t_{h(D)W,min}$ - $t_{PLH,max}$) ns.

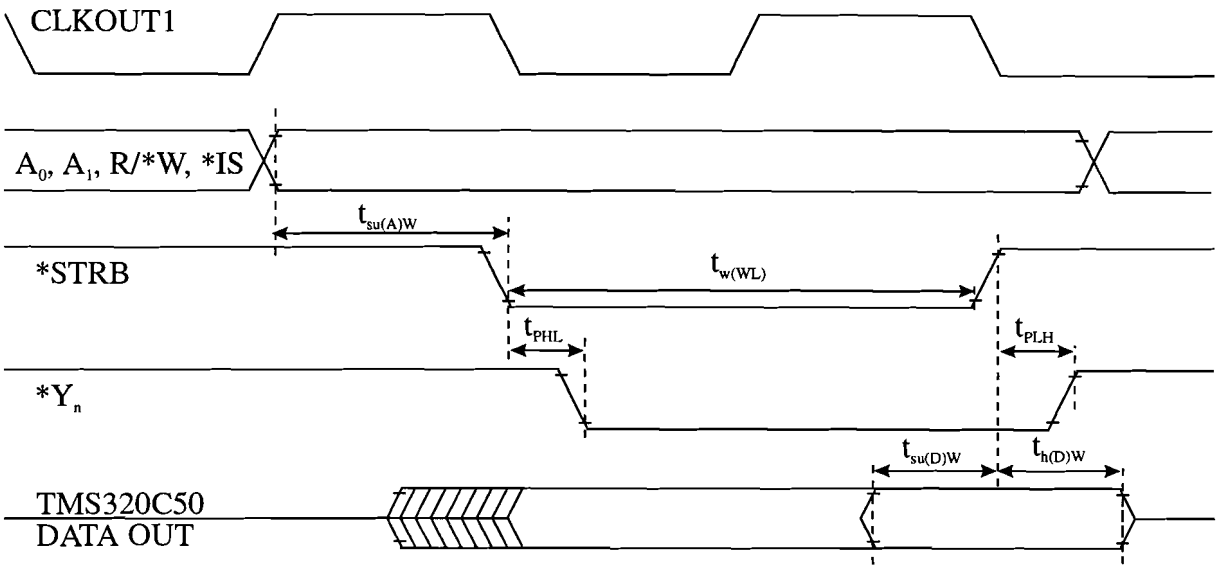


Figure 4.18 I/O-selection Write Timing Diagram.

Table 4.19 I/O-selection Write Timings.

Symbol	Parameter	Device	Min (ns)	Max (ns)
$t_{su(A)W}$	Address valid before *WE low	TMS320C50	*H*-5	
$t_{w(WL)}$	*WE low pulse duration	TMS320C50	2*H*-2 + *n*·2*H*	2*H*+2 + *n*·2*H*
$t_{su(D)W}$	Write data valid before *WE high	TMS320C50	2*H*-20	2*H*
$t_{h(D)W}$	Write data valid after *WE high	TMS320C50	*H*-5	*H*+10
t_{PHL}	Propagation delay *G2A, *G2B	74F138	3.0	7.5
t_{PLH}	Propagation delay *G2A, *G2B	74F138	3.5	8.0

4.8 Communicating between memory devices

Sections 4.4, 4.5 and 4.6 derived timing requirements for the various memory devices regarding one read and one write cycle. In practice, however, multiple read and write cycles in different order between different memory devices occur. Because each device is capable of activating the commonly shared databus, busconflicts can occur. To avoid these busconflicts, communication between each memory device must be checked on output enable and disable timings.

Access to I/O ports is done using memory read and write cycles. Therefore, the devices that are activated by the I/O-select signals (i.e. 74F245, 74F574 and 74F652 ICs) must also be checked to prevent busconflicts.

When executing program code, the TMS320C50 uses the databus to fetch instructions from external program memory and to fetch and store data in external data memory. These databus accesses consist of a multiple of four different access combinations: two consecutive read cycles, a read cycle followed by a write cycle, a write cycle followed by a read cycle and two consecutive write cycles. The TMS320C50 uses *RD and *WE to denote an external read or write cycle. In order to prevent busconflicts, external writes always require two cycles. All external writes immediately preceded by an external read or immediately followed by an external read require three machine cycles.

Communicating between (memory) devices is controlled by the TMS320C50. It allows one device to put data on the databus. The other devices are deselected due to the memory and I/O-selection circuitry. At the end of the write cycle, the device must remove its data and make the databus high-impedant before the TMS320C50 grants access to another device. Otherwise, busconflicts can occur. It will be shown that each device that performs a write cycle makes the databus high-impedant before another device is activated.

Table 4.20 lists the devices which have access to the databus with their output enable and disable timings. The output enable timings specify when the databus becomes low-impedant before valid data are on the databus. The output disable timings specify when the databus becomes high-impedant. Note that these timings are valid when a specific device performs a write cycle.

Table 4.20 Device output enable and disable timings (for device write cycles).

Device	Minimum Output Enable timing (ns)	Maximum Output Disable timing (ns)
TMS320C50	$t_{en(D)W} = -5$	$t_{h(D)W} = H+10 = 30$
EPROM/74F245	$t_{PLZ} = 5.0$	$t_{PHZ} = 14.1$
SRAM	$t_{LZOE} = 0$	$t_{HZOE} = 7$
DPSRAM	$t_{LZOE} = 3$	$t_{HZOE} = 15$
74F245	$t_{PZH} = 2.0$	$t_{PHZ} = 7.5$
74F574	$t_{PZH} = 2.0$	$t_{PHZ} = 6.0$
74F652	$t_{PZH} = 3.5$	$t_{PLZ} = 15.5$

Note: • SRAM/DPSRAM timings are taken from *OE valid (t_{LZOE} and t_{HZOE}).
• See section 4.4.3 for the derivation of the maximum EPROM output enable and disable timings.

- Minimum output enable timings from commercial TTL ICs are derived according to $\min(t_{PZH,min}, t_{PZL,min})$.
  Maximum output disable timings are derived according to $\max(t_{PHZ,max}, t_{PLZ,max})$.

For each combination of external read and write cycles, timing diagrams will show that busconflicts will not occur:

Read cycle followed by a read cycle or a write cycle:

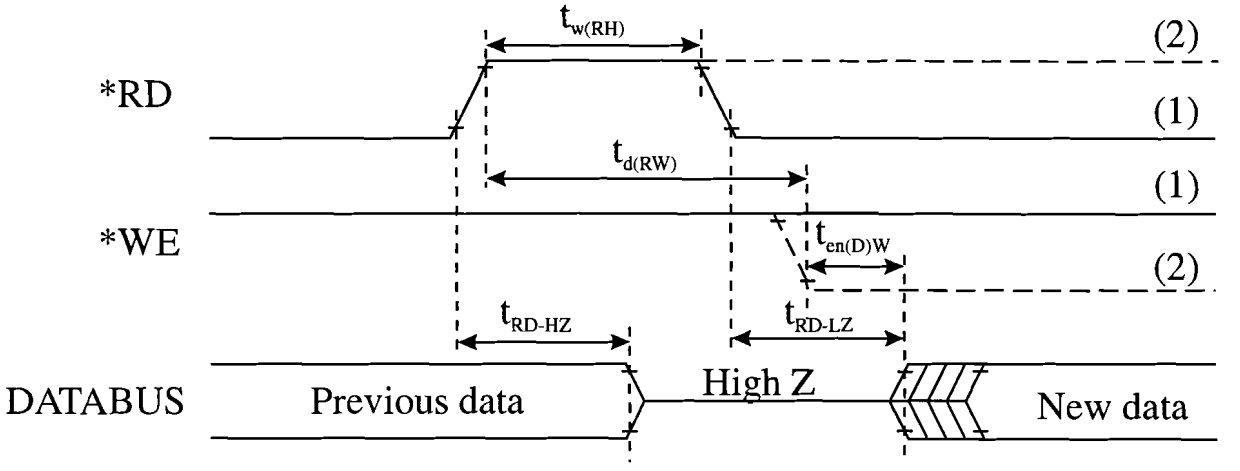


Figure 4.19 Timing diagram read-read (1) and read-write (2) cycle.

Table 4.21 Read/Read and Read/Write timings.

Symbol	Parameter	Device	Timing (ns)
$t_{w(RH)}$	*RD high pulse duration	TMS320C50	$\geq H$-2
$t_{d(RW)}$	Delay time, *RD high to *WE low	TMS320C50	$\geq 2H$-5
$t_{en(D)W}$	Enable time, *WE to databus driven	TMS320C50	$\geq$ -5
t_{RD-HZ}	Output Disable Timing from *RD high	Other devices	-
t_{RD-LZ}	Output Enable Timing from *RD low	Other devices	-

Figure 4.19 shows the timing diagram for two consecutive read cycles (1) and for a read cycle followed by a write cycle (2). At the rising edge of *RD, device data are read by the TMS320C50. Device data stay valid on the databus for at most t_{RD-HZ} ns after *RD goes high. For two consecutive read cycles, *RD goes low again after 18 ($t_{w(RH)}$) ns, thus enabling the databus after t_{RD-LZ} ns. From Table 4.20, the worst-case combination can be chosen: the 74F652 has a maximum output disable timing of 15.5 ns and the CY7C199 has a minimal output enable timing of 0 ns. It is evident that the output disable timing of

the 74F652 does not exceed the *RD high pulse duration, thus no busconflicts will occur. For a read cycle followed by a write cycle, *WE goes low after 35 ($t_{d(RW)}$) ns after *RD goes high. The databus is enabled within $t_{en(D)W}$ ns. The worst-case combination is a read cycle from the 74F652 (output disable time of 15.5 ns) and a write cycle from the TMS320C50 (output enable time of -5 ns). The minimum time the databus is high-impedant is 14.5 ns, resulting in no busconflicts.

Write cycle followed by a write cycle or a read cycle:

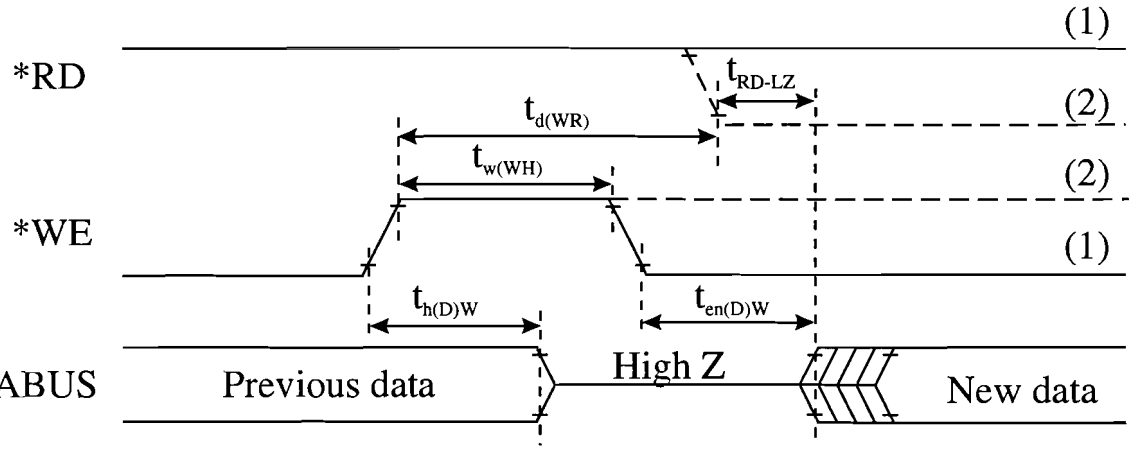


Figure 4.20 Timing diagram write-write (1) and write-read (2) cycle.

Table 4.22 Write/Write and Write/Read timings.

Symbol	Parameter	Device	Timing (ns)
$t_{w(WH)}$	*WE high pulse duration	TMS320C50	≥ 2*H*-2
$t_{d(WR)}$	Delay time, *WE high to *RD low	TMS320C50	≥ 2*H*-10
$t_{en(D)W}$	Enable time, *WE to databus driven	TMS320C50	≥ -5
$t_{h(D)W}$	Write data valid after *WE high	TMS320C50	≤ *H*+10
t_{RD-LZ}	Output Enable Timing from *RD low	Other devices	-

Figure 4.20 shows the timing diagram for two consecutive write cycles (1) and for a write cycle followed by a read cycle (2). At the rising edge of *WE, data are read by the devices. TMS320C50 data stay valid on the databus for at most 30 ($t_{h(D)W}$) ns after *WE goes high. For two consecutive write cycles, *WE goes low again after 38 ($t_{w(WH)}$) ns. The TMS320C50 enables the databus within -5 ($t_{en(D)W}$) ns, i.e. the databus is enabled 33 ns after *WE goes high. Two TMS320C50 write cycles produce the worst-case situation. While data can stay on the databus for at most 30 ns, the time between two write cycles is

33 ns: no busconflicts will occur. For a write cycle followed by a read cycle, *RD goes low after 30 ($t_{d(WR)}$) ns after *WE goes high. The databus is enabled within t_{RD-LZ} ns. The worst-case combination is a write cycle from the TMS320C50 and a read cycle from the CY7C199, resulting in a worst-case high-impedant databus time of 0 ns.

The attentive reader should have noticed that when the TMS320C50 operates at its maximum frequency of 28.6 MHz (= machine cycle of 35 ns), $t_{h(D)W,max}$ exceeds $t_{d(WR)}$. In worst-case situations, TMS320C50 write data can still be on the databus when a read cycle is started, thus resulting in a possible databus conflict.

5 The A/D- and D/A converter

5.1 Introduction

This chapter discusses the implementation of the Analog-to-Digital Converter circuit and the Digital-to-Analog Converter circuit. Section 5.2 explains why the receiver configuration is to be improved. Section 5.3 describes the implementation of the ADC circuit. Section 5.4 describes the features of the D/A converter circuit with the transmit clock.

5.2 Improving the existing receiver configuration

One of the main reasons for designing a new modem with two DSPs is the fact that the receiving part of the already existing modem needed more processing power. Section 1.4 explained that the IF receiver can process about f_c = 16 kChip/s. To achieve a chiprate of 64 kChip/s, a modem equipped with two TMS320C50 DSPs would be satisfactory. In order to enhance the performance of the modem, the samples taken from the analog signal must be passed to both DSPs alternatingly. In this way, both DSPs can perform their calculations on the samples simultaneously, resulting in an increase of processing speed.

The task of the receiver is to produce the databits from the incoming chip samples. The sample moments of the A/D converter are chosen in such a way that the analog signal is sampled at maxima and minima and at zero-crossings of the IF-carrier. The samples obtained at the maxima and minima are called I-samples, the samples at zero-crossings Q-samples. Calculations have to be performed on these samples. These calculations merely consist of multiplying the I-samples with +1 or -1 in order to obtain the chipcode at baseband. After correlating the chipcode with the local PN-sequence, it is possible to identify the databit (0 or 1). To obtain maximum efficiency, the calculations have to be performed on both TMS320C50s at the same time. This is achieved by passing the I-samples to one TMS320C50 and the Q-samples to the other TMS320C50.

To implement the previous design considerations, a new ADC circuit is designed with a new analog-to-digital converter and a switch which passes the samples to both TMS320C50s. Section 5.3 will explain the ADC circuit in detail.

5.3 The ADC circuit

Figure 5.1 shows the functional blocks of the ADC circuit.

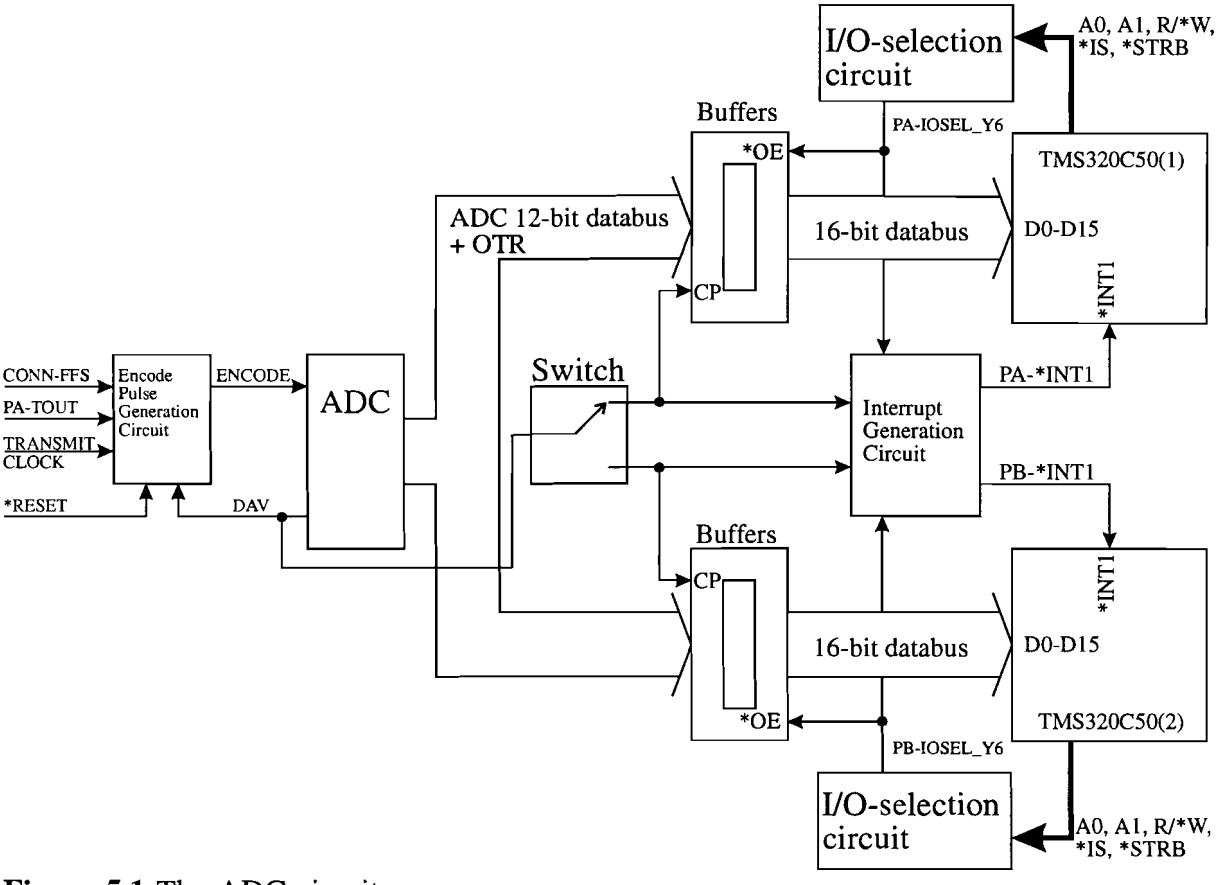


Figure 5.1 The ADC circuit.

The ADC circuit consists of :

- encode pulse generation circuit : this circuit generates the ENCODE-pulse necessary for the analog-to-digital conversion and satisfying ADC timing requirements.
- ADC : the AD1671 analog-to-digital converter.
- ADC-switch : this switch passes samples from the ADC alternatingly to the TMS320C50(1) and TMS320C50(2) or to only one TMS320C50.
- buffers : buffers are required to disconnect the TMS320C50 databuses from the ADC databus to avoid busconflicts and illegal write operations to the ADC.
- interrupt set/reset circuit : this circuit generates interrupts at the TMS320C50s when a sample value is clocked into the buffers.

Before each functional block is described in detail, a global description of the operation of the ADC circuit is given.

A rising edge of either f_{fs} from the external frequency synthesizer via the connector, the timer from TMS320C50(1) or the internal transmit clock initiates the conversion cycle. The ADC performs an analog-to-digital conversion on the analog signal. After the ADC puts the sample data on the databus, the switch determines which DSP can process the data. Data are clocked into the internal registers of the appropriate buffers and the DSP is interrupted. After receiving the interrupt, the interrupt service routine reads data from the databus. By activating I/O-select signal *Y6, the output pins of the buffers are enabled and data are put on the TMS320C50 databus. *Y6 also clears the interrupt so the DSP can receive the next interrupt. After data are read, the I/O-select signal becomes inactive, therefore disabling the output pins of the buffers.

Sections 5.3.1 to 5.3.4 explain in detail the functional blocks of the ADC circuit.

5.3.1 The pulse generation circuit

The analog-to-digital conversion is initiated by a low-to-high transition on the ENCODE input of the ADC. This transition is made using one of the following signals:

- the sample frequency f_{fs} from the frequency synthesizer board, available on connector CONN1 via the parallel interface.
- the transmit clock available on the modem board.
- the TMS320C50(1) timer. With this timer, the frequency synthesizer could be implemented in software and therefore the external frequency synthesizer board could be omitted [4].

Using jumpers J1, J2 and J3, a selection between these input signals can be made as shown in Table 5.1.

There are two ways to start the analog-to-digital conversion on the AD1671 (see also the datasheets of the AD1671 in Appendix 4, p. 184):

1) generate an ENCODE pulse for at least 20 ns and at most 50 ns. When the AD1671 asserts DAV high, new data are on the output pins. This option is shown in Figure 5.2a.

Table 5.1 Jumper settings for the ENCODE pulse generation.

J1	J2	J3	Input clock
12	--	--	Sample frequency f_{fs} from frequency synthesizer
--	12	--	Transmit clock
--	--	12	Timer TMS320C50(1)

Note : -- : not connected

2) assert ENCODE high for at least 20 ns. After the AD1671 asserts DAV low, the ENCODE pulse must also be asserted low. When DAV is asserted high, new data are on the output pins. This option is shown in Figure 5.2b.

Descriptions of timings are listed in Table 5.2.

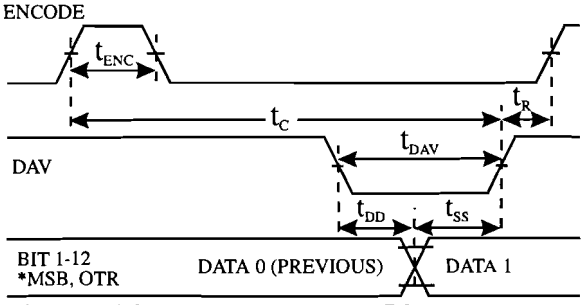


Figure 5.2a Encode Pulse HIGH.

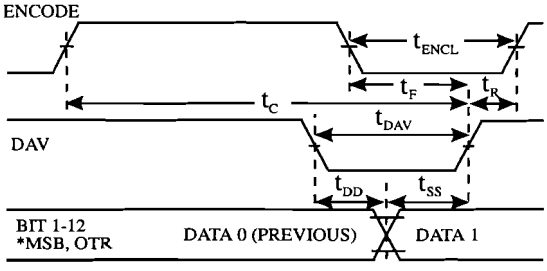


Figure 5.2b Encode pulse LOW.

Table 5.2 Switching specifications AD1671.

Symbol	Parameter	Min (ns)	Typ (ns)	Max (ns)
t_C	Conversion Time			800
t_{ENC}	ENCODE Pulse Width High	20		50
t_{ENCL}	ENCODE Pulse Width Low	20		
t_{DAV}	DAV Pulse Width	150		300
t_F	ENCODE Falling Edge Delay	0		
t_R	Start New Conversion Delay	20		
t_{DD}	Data and OTR Delay from DAV ↓	20	75	
t_{SS}	Data and OTR Valid before DAV ↑	20	75	

The disadvantage of option 1) is that the ENCODE pulse must be well-defined. If the pulse width of a signal is not known or cannot be altered, this conversion method cannot be used. Diederen used a monostable-multivibrator IC to maximize the low-time of a

signal [1, p. 49]. However, this IC was not designed to produce pulse signals with a 50 ns low time.

The advantage of option 2) is that the pulse width may exceed 50 ns but must be asserted low after DAV goes low. In this case, a pulse generation circuit is necessary to assert ENCODE low. This can be achieved using a D-flipflop. The realization of the pulse generation circuit is shown in Figure 5.3.

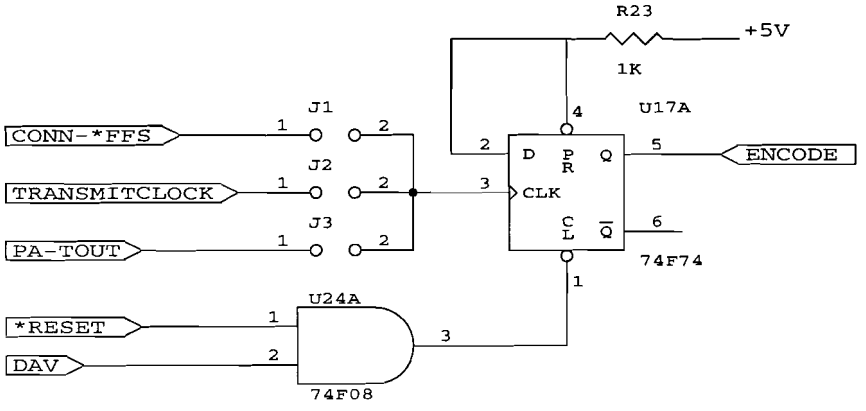


Figure 5.3 The pulse generation circuit.

At the rising edge of the clock input of D-flipflop U17, ENCODE goes high and stays high. A low-to-high transition on the ENCODE input initiates an analog-to-digital conversion. When the AD1671 asserts DAV low, the D-flipflop is reset, thus asserting the ENCODE input low. At power-up or after a reset, the D-flipflop is also reset, so the ENCODE input is low before any conversion is started.

The D-flipflop introduces a timing delay of t_{PLH} ns from clock high to Q high, where t_{PLH} is defined as : $3.8 \leq t_{PLH} \leq 7.8$ ns. This results in a timing delay between the desired sample moment and the time the sample is actually taken by the ADC. However, this time is a fixed delay and does not disturb the receiver because the Costas carrier recovery loop in the receiver will compensate for it [2, 4].

5.3.2 The Analog-to-Digital Converter

For analog-to-digital conversion of the received signal, the AD1671 from Analog Devices is used. The features of the AD1671 are listed below:

- resolution of 12 bits
- maximum sampling rate of 1.250 Msamples/s
- On-Chip Sample-and-Hold Amplifier and Voltage Reference
- Low Power Dissipation: 570 mW.
- No missing codes guaranteed.
- Input Ranges : -2.5 to +2.5 Volts bipolar
  -5.0 to +5.0 Volts bipolar
  : 0 to +2.5 Volts unipolar
  0 to +5 Volts unipolar
- Out of Range output bit indicates when the input signal is beyond the AD1671's input range.
- Output data is available in unipolar/bipolar offset or bipolar twos complement binary format.
- 28-pin DIP or 28-pin PLCC package.

Section 8.4 of [4] explains in detail why the AD1671 was chosen for the new modem.

Figure 5.4 shows the AD1671 with resistors, capacitors and jumpers as implemented on the modem board. The datasheets of the AD1671 list the pin description (see Appendix 4, p. 187).

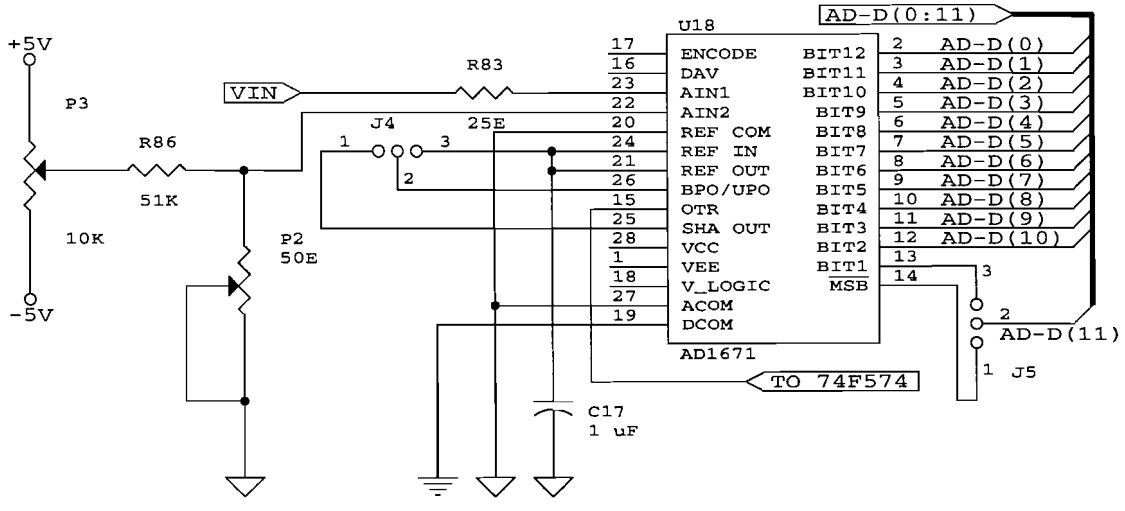


Figure 5.4 The AD1671 Analog-to-Digital Converter.

An analog-to-digital conversion is initiated by providing an active high level on the ENCODE pin of the AD1671. The falling edge of the ENCODE pulse is specified to operate within 50 ns after the rising edge of ENCODE or after the falling edge of DAV (Data Available) as described in Section 5.3.1. During the conversion, the AD1671 asserts DAV low. At this time, previous data can be read from the output pins of the ADC. Upon completion of conversion, DAV is set high and new data are on the output pins BIT1(MSB) - BIT12(LSB).

The AD1671 will flag an out-of-range (OTR) condition when the analog input voltage is beyond the input range of the converter. OTR is set low when the analog input voltage is within the input range. OTR is set high and will remain high when the analog input voltage exceeds the input range by typically ½ LSB from the centre of the ± full-scale output codes. OTR will remain high until the analog input is within the input range and another conversion is completed. The OTR pin (pin 15) is directly connected to the LSB (D0) of the TMS320C50 databuses using the 74F574 transceiver ICs. When obtaining the sample data from the ADC, a modulo 2 operation will determine if the input voltage was out of range.

The AD1671 provides both MSB and *MSB outputs, delivering data in positive true straight binary format for unipolar input ranges and positive true offset binary or twos complement format for bipolar input ranges. Twos complement format minimizes software overhead (no data conversion) which is especially important in high speed data transfer. The MSB (BIT1) and *MSB output pins are connected to the ADC-databus using jumper J5. Table 5.3 lists the two possible output data formats with the corresponding jumper settings.

Table 5.3 Jumper setting for the AD1671 output data format.

J5	*MSB/BIT1	Output data format
12	*MSB	twos complement range
23	BIT1	positive true binary range

The AD1671 can be configured to operate with unipolar (0 V to +5 V, 0 V to +2.5 V) or bipolar (±5 V, ±2.5 V) inputs (see also Appendix 4). In the modem design, only two input ranges are implemented: unipolar 0 V to +5 V and bipolar ±5 V. Jumper J4 is provided to choose between these two input ranges as shown in Table 5.4.

Table 5.4 Jumper setting for 0V - 5V / ± 5V input range.

J4	Input range
12	Unipolar (0-5 V)
23	Bipolar (± 5V)

The other two input ranges (unipolar 0 V to +2.5 V and bipolar ±2.5 V) are not implemented because the analog input signal from the transmitter is a bipolar ±5V signal. Furthermore, extra hardware (i.e. AD845 opamp, (variable) resistors, jumpers) was necessary to implement the other two input ranges. The resistors shown in Figure 5.4 are necessary to calibrate the AD1671 for both input ranges. More information about the calibration procedures can be found in Appendix 4, p. 191.

Note that for receiving spread-spectrum signals the unipolar 0-5 Volt input range is not used. However, no extra hardware was necessary to implement this feature and it made the ADC circuit somewhat flexible.

5.3.3 The ADC-switch with the buffers

To enhance the processing speed of the modem, the digital sample values are passed alternatingly to TMS320C50(1) and TMS320C50(2). This is done using the ADC-switch shown in Figure 5.5.

The main element of the ADC-switch is the D-flipflop (U17). Its *Q-output is directly connected to the D-input. Data at the D-input are transferred to the Q- and *Q-outputs on the low-to-high transition of the clock. Data at the *Q-output are transferred back to the D-input before the next low-to-high transition of the clock. Timing requirements for the switch are guaranteed because the D-flipflop expects data to hold for at least 1.0 ns after the rising edge of the clock. However, data are on the output pins at least 3.8 ns after the rising edge of the clock. The D-flipflop is reset at power-up, by a user-defined reset or in hardware using jumper J6. In this way, the Q-output is at a low voltage and the *Q-output at a high voltage.

The switch was designed to pass the samples to either the TMS320C50(1), alternatingly to TMS320C50(1) and TMS320C50(2) or to TMS320C50(2). Jumpers J6 to J12 determine which processor(s) get(s) the samples as is shown in Table 5.5.

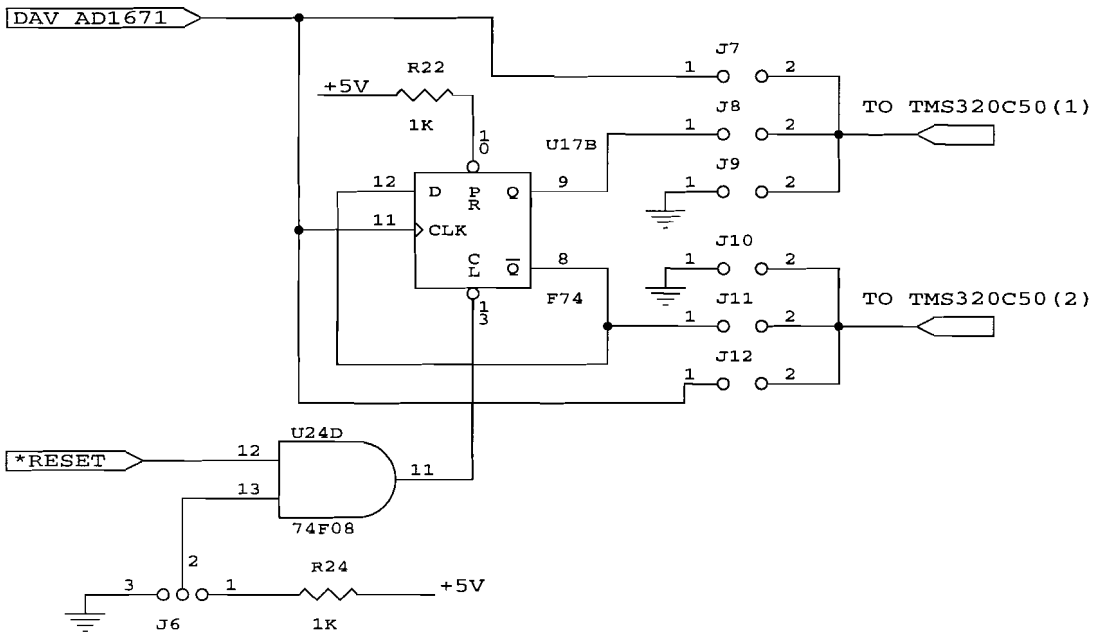


Figure 5.5 The ADC-switch.

Table 5.5 Jumpersettings for the ADC-switch.

J6	J7	J8	J9	J10	J11	J12	Samples to :
23	12	--	--	12	--	--	TMS320C50(1)
12	--	12	--	--	12	--	TMS320C50(1) and TMS320C50(2)
23	--	--	12	--	--	12	TMS320C50(2)

At the rising edge of DAV (i.e. new data are available on the AD1671 output pins), output Q gets a low-to-high transition and clocks the data into the 74F574 transceiver ICs. At the same time, an interrupt is generated at the processor. Output *Q gets a high-to-low transition and does not clock data into the 74F574 transceiver ICs for they are positive edge-triggered ICs. Furthermore, no interrupt is generated at the processor. Due to the switch, at the next rising edge of DAV, output *Q gets a low-to-high transition and clocks data into the transceiver ICs. In this manner, sample data are passed alternatingly to both TMS320C50s.

When the samples are passed to only one processor, the D-flipflop is not used. Jumper J6 resets this D-flipflop to prevent unwanted signal changes on the Q- and *Q-outputs. Furthermore, the clock inputs of the unselected 74F574 transceiver ICs and the interrupt set/reset circuit are connected to digital ground. In this way, no unwanted data are clocked into the transceiver ICs and no unwanted interrupts are generated. The DAV output of the

AD1671 is directly connected to the clock input of the transceiver ICs and to the interrupt set/reset circuit.

When passing samples to both TMS320C50s alternatingly, each processor has two sample periods available for reading and processing the sample instead of one sample period. It is not possible to pass groups of samples to both DSPs. This can be done using the global memory.

When the AD1671 puts data on the databus, only one TMS320C50 will process the data while the other TMS320C50 may also use the databus for other purposes. Therefore, buffers are provided to prevent busconflicts. The buffers of the ADC-switch consist of four 74F574 transceiver ICs (U19 to U22), two for each 16-bit databus. The 74F574 clocks data on the input pins into its internal register at the rising edge of the clock. Data must hold at least 1.5 ns after the rising edge of the clock but may change after the hold time. Data from the internal register are put on the output pins (i.e. on the TMS320C50 databus) when *OE is asserted low. This is accomplished when the TMS320C50 reads the data using the IN instruction. The IN instruction activates I/O-select signal *Y6 which enables the output pins from the 74F574.

5.3.4 The interrupt set/reset circuit

The interrupt set/reset circuit is designed to interrupt the TMS320C50 when AD1671 data are available and to reset the interrupt when it is acknowledged by the TMS320C50. Figure 5.6 shows the interrupt set/reset circuit.

The interrupt set/reset circuit consists of two D-flipflops which generate the interrupts at the TMS320C50s. The flipflops are reset at power-up to get defined outputs and by using the I/O-select signal *Y6.

At reset, the *Q-outputs are inactive (i.e. at a high voltage). Therefore, no unwanted interrupt is generated. At the low-to-high transition of the clock, *Q becomes active low and generates an interrupt at the TMS320C50 *INT1 pin. After the TMS320C50 detects the interrupt, the interrupt service routine reads data from the databus using the IN instruction. The IN instruction enables I/O-select signal *Y6 from the I/O-selection circuit. *Y6 enables the buffers (see Section 5.3.3) and clears the interrupt by resetting the D-flipflop. While *Y6 is active low, the D-flipflop is inactive. Therefore, unwanted low-to-high transitions on the clock input will not generate interrupts. After the data are read, *Y6 becomes inactive, thus activating the D-flipflop for generating following interrupts.

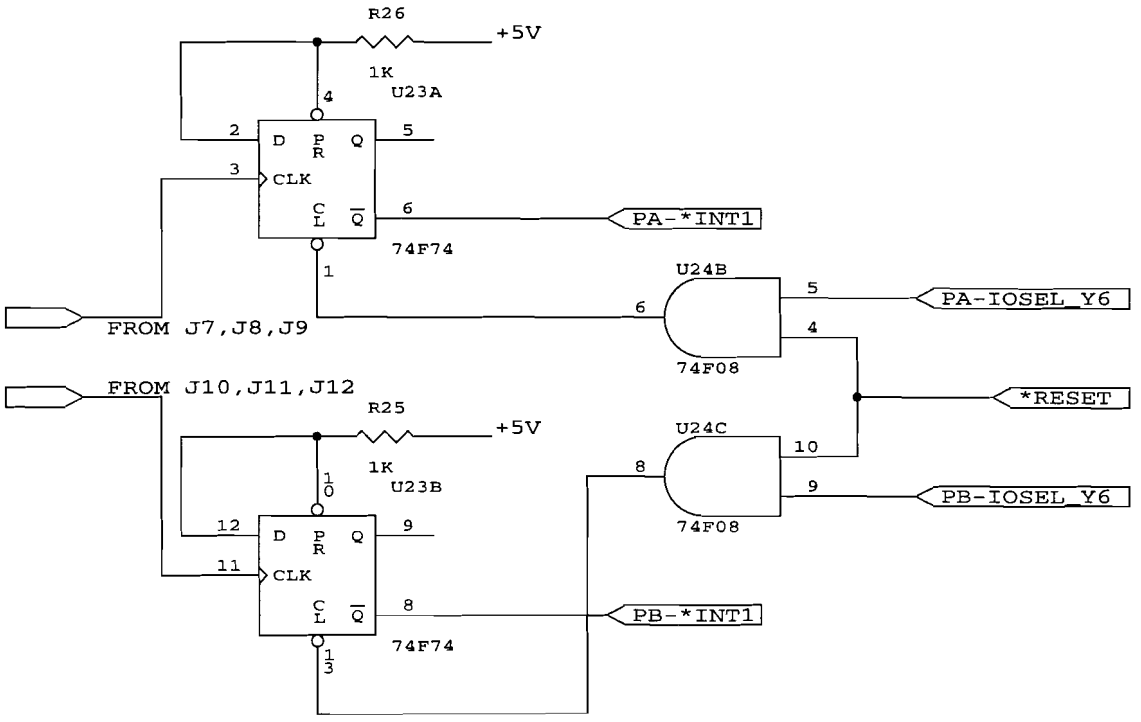


Figure 5.6 Interrupt set/reset circuit.

The TMS320C50 expects an interrupt to be valid for at least three clock cycles. This timing requirement is guaranteed because the interrupt is reset at the same time data are read from the databus. Reading the databus is done from the interrupt service routine, which will only be executed after receiving the interrupt correctly.

5.4 The Digital-to-Analog converter

The modem must be able to operate as transmitter and receiver at the same time. Therefore, one TMS320C50 is equipped with a digital-to-analog converter (DAC) to provide multi-user simulation (see also Section 5.11 of [1]). The DAC circuit is the same as was used with the TMS320C25 modem. Section 8.2 of [4] explains why the same circuit is used.

The DAC used is the AD568 from Analog Devices. The features of this DAC are listed below:

- 12-bit monolithic D/A converter
- 10.24 mA Full-Scale Output
- Settling time of 1 LSB in 35 ns.
- TTL / CMOS compatible digital inputs

The full scale output of the DAC corresponds to a current of 10.24 mA. This current must be converted to a voltage to transmit the analog spread-spectrum signals. This current-to-voltage conversion is done using the AD840 opamp from Analog Devices as is specified in the AD568 datasheets. Figure 5.7 shows the DAC with the opamp and the transmit clock.

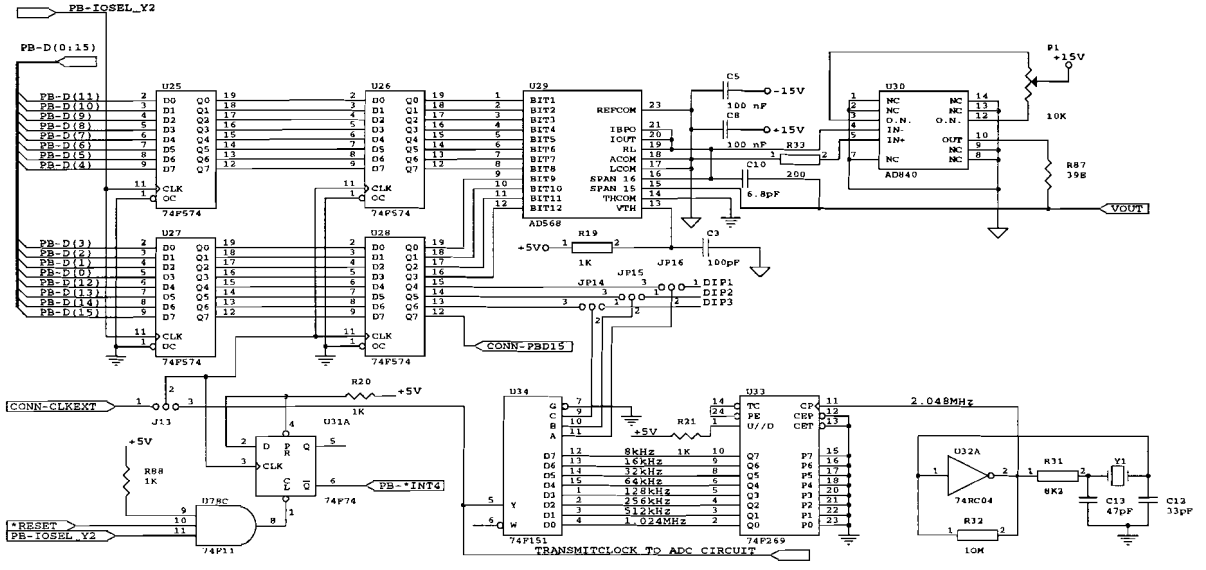


Figure 5.7 Buffered bipolar-voltage output digital-to-analog converter with interrupt-generation circuit and transmitclock [1].

The configuration implemented is bipolar and has a +5.12 to -5.12 V voltage output. The settling-time of the opamp is 100 ns. With the variable resistor P1, the offset voltage of the opamp can be adjusted to zero.

The DAC circuit is the same as was used by Diederen[1]. However, two modifications were made. Diederen used the *IACK-signal from the TMS320C25 processor to disable the interrupt generated by D-flipflop U20B (see Figure 5.11 of [1]). However, resetting the D-flipflop can also be done using I/O-select signal *Y2 of the TMS320C50(2) I/O-selection circuit. This method of resetting D-flipflops is used throughout the modem design and it saves an extra OR-gate. For the second modification, a resistor of 39 Ω (R87) is connected from the output of the opamp to the output BNC plug and the feedback loop. This resistor prevents the opamp connected to the output of the digital-to-analog converter to oscillate due to capacitive load of connected coaxial cables (see the datasheets of the AD840 in Appendix 4). Furthermore, this specific resistance also makes the output impedance of the opamp equal to the impedance of the coaxial cables connected.

The AD568 DAC has no input buffer, so external buffers are necessary. It has a 12-bit digital input therefore two external transceiver ICs (U26, U28) are required. The transmit procedure is as follows. On the rising edge of the transmit clock (which is either internal from the transmit clock circuit or external from the connector CONN-CLKEXT), data are clocked into the buffers (U26, U28). Within approximately 100 ns, data on the output pins of the buffers are converted to an analog bipolar voltage. The transmit clock generates an interrupt (*INT4) at the TMS320C50(2) using D-flipflop U31. The corresponding interrupt service routine writes the next word to be converted to the second buffers (U25, U27) which are the inputs to the first buffers. Then, on the next rising edge of the transmit clock, the whole procedure repeats itself.

Note that BIT1 of the DAC is the MSB and BIT12 is the LSB. Therefore, bit 11 of the TMS320C50(2) databus is connected to BIT1 and bit 0 of the databus is connected to BIT12. Bits 12 to 14 of the databus can be used for programming the transmit clock.

The output Q7 (bit 15, labelled CONN-PBD15) of U28 is connected to the 2x32-pin connector CONN1 (pin C30). This pin can be used as a general purpose output signal.

The internal transmit clock has an adjustable frequency of 8 kHz to 1.024 MHz and consists of an oscillator circuit, a binary counter and an 8-bit multiplexer. The oscillator is based on crystal (Y1), oscillating at 2.048 MHz and a CMOS inverter (U32). This square wave is the input of a 8-bit binary counter (U33), which serves as a divider circuit. The eight outputs have frequencies from 8 kHz (Q7) to 1.024 MHz (Q0). The eight input multiplexer (U34) selects one of the outputs of the counter to serve as transmit clock signal. The multiplexer is controlled by three select inputs A, B, and C, which can be set by DIP-switches DIP1 to DIP3 or programmed in software. Three unused outputs of buffer U28 (Q4 to Q6) provide the select inputs which can be programmed. Selection between DIP-switches and software can be made by setting jumpers J14 to J16. By connecting pins 1 and 2 of these jumpers, selection is made by DIP-switches; selection by software is made by connecting pins 2 and 3.

The output of the transmitter can also be clocked out by an external clock signal in order to generate other output frequencies. The choice between the internal or external transmit clock is made by jumper J13 (connection if pins 2 and 3 for internal transmit clock, pins 1 and 2 for external transmit clock). The external clock also generates an interrupt at the processor.

6 Communicating with the outside world

6.1 Introduction

This chapter describes the design of several forms of communication of the modem board with the outside world. Section 6.2 describes the history and implementation of the JTAG-interface required for debugging and testing the TMS320C50s using an external debugger. Section 6.3 gives information about the design of the serial port for communication with other (off-board) serial devices. Section 6.4 describes the implementation of the TDM serial port. Section 6.5 describes the implementation and operation of the communications interface. Hardware errors in the previous design are corrected in the new design. Finally, section 6.6 describes the implementation and operation of the general-purpose 16-bit parallel interface for communication with off-board devices.

6.2 JTAG-Interface

6.2.1 Introduction to the JTAG-Interface

The ongoing miniaturization within integrated circuits (ICs) has led to an increased number of gates and a very large number of functions per chip. Consequently, more pins per IC are needed leading to an ever decreasing distance between ICs on the printed circuit board (PCB). The miniaturization has made it more difficult to access these highly loaded PCBs mechanically for in-circuit testing.

The basic idea to circumvent the access problems for test purposes was to add a shift register cell next to each I/O pin of the component. During test mode, these cells are used to control the status of an output pin and read the status of an input pin. This allows for testing the board interconnections. Since the shift register cells are located at the IC's boundary (I/O pins), these cells are referred to as Boundary Scan Cells. According to the IEEE 1149.1, the input to the serial test data path is called Test Data Input (TDI) and the output is called Test Data Output (TDO).

Figure 6.1 shows an example where two ICs are connected to each other. Shift register cells have been added between the IC's 'core logic' and the I/O pins to provide a serial test data path through all ICs.

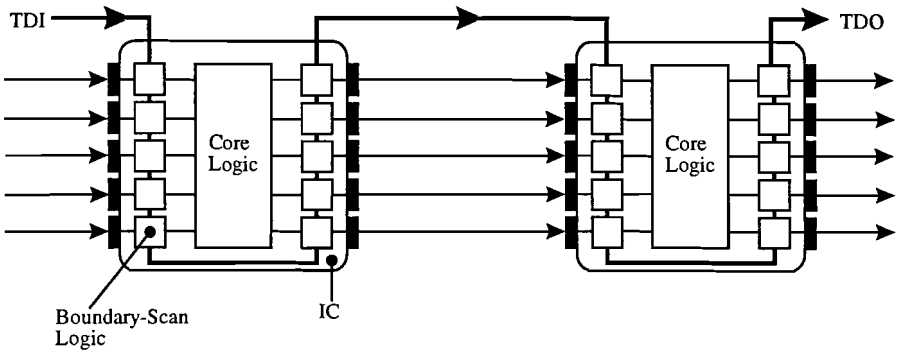


Figure 6.1 ICs with shift registers and scan path [6].

With these cells, testing the board connections as well as testing the internal core logic is possible.

The Boundary-Scan registers should have three important properties:

- they must be 'invisible' during normal operation of the IC's core logic;
- they must be able to isolate the IC interconnections on the board from the IC cores to allow testing the external IC connections;
- they should be able to isolate the IC from its surroundings on the PCB to also allow testing of the internal core logic.

6.2.2 The Boundary-Scan Test Standard

The IEEE 1149.1 distinguishes four basic hardware elements:

- the Test Access Port (TAP)
- the TAP Controller
- the Instruction Register
- a group of Test Data Registers (TDRs)

The TAP provides access to the many test support functions built into an IC. It consists of four input connections, one of which is optional and one output connection. The optional input connection is the *TRST pin. The TAP Controller provides signals to shift test data into TDI and test result data out of TDO and performs the actual test actions. The Instruction Register allows test instructions to be shifted into every IC. A test instruction defines the Test Data Register to be addressed and the test to be performed.
A detailed description of the four hardware elements is given in [6]. For the implementation of the JTAG-interface, the test signals connected to the Test Access Port are listed:

- **The Test Clock Input (TCK)**

  The TCK signal allows the Boundary-Scan part of the ICs to operate synchronously and independently of the built-in system clocks. TCK permits clocking test instructions and data into or out of the register cells.

- **The Test Mode Select Input (TMS)**

  The logic signals received at the TMS input are interpreted by the TAP Controller to control the test operations. The signals are decoded in the TAP Controller to generate the required control signals inside the chip. When TMS is not driven it must be held at a logic 1.

- **The Test Data Input (TDI)**

  Serial input data to this port is fed either into the instruction register or into a test data register. When TDI is not driven, a logic 1 must be present.

- **The Test Data Output (TDO)**

  Depending on the state of the TAP controller, the contents of either the instruction register or a data register are serially shifted out towards the TDO. When no data is shifted through the cells, the TDO driver is set to an inactive state.

- **The Test Reset Input (*TRST)**

  The TAP's test logic is asynchronously forced into its reset mode when a logic 0 is applied to the *TRST pin.

Using these pins, the implementation of the JTAG-interface for the modem configuration can be carried out.

6.2.3 Implementing the JTAG-Interface

The TMS320C50 JTAG-interface can be connected to an XDS510 emulator cable pod manufactured by Texas Instruments. Multiple processors may be daisy-chained to enable easy debugging of a multi-processor configuration. The TMS320C50 JTAG-interface is a superset of the IEEE 1149.1 standard and consists of the signals listed in Table 6.1.

Table 6.1 JTAG Signal Description.

Pin	Signal	Description
1	TMS	JTAG test mode select
3	TDI	JTAG test data input
7	TDO	JTAG test data output
11	TCK	JTAG 10-MHz test clock
2	*TRST	JTAG test reset
13	EMU0	Emulation pin 0
14	EMU1/*OFF	Emulation pin 1
5	PD	Presence detect
9	TCK_RET	JTAG test clock return

Before designing the JTAG-interface, two design considerations were made:

- The XDS510 emulator cable pod provides only a 10 MHz test clock. This frequency is far too low for the modem to operate at full speed. Therefore, an option must be provided to choose a clock operating at a higher frequency. The maximum clock frequency at which the XDS510 can operate is 28.6 MHz. So, by using an external 25 MHz oscillator, testing and debugging facilities can be performed for the TMS320C50s operating at normal speed (= 25 MHz).

- The emulator must be able to debug both TMS320C50s but also a single TMS320C50-device. When debugging a single TMS320C50, the other TMS320C50 must not be removed from its socket and must not be recipient to the JTAG test signals.

Four configurations can be made in hardware using the jumpers:

- **Multiprocessor-configuration (both TMS320C50(1) and TMS320C50(2) are recipient to JTAG signals):**

  In this configuration, both TMS320C50s are daisy-chained. TDI of TMS320C50(1) and TDO of TMS320C50(2) are connected to the JTAG-interface and TDO of TMS320C50(1) is connected to TDI of TMS320C50(2).

- **Single processor configuration (either TMS320C50(1) or TMS320C50(2) is recipient to JTAG signals):**

  One TMS320C50 is connected to the JTAG-interface while the other TMS320C50 device ignores the JTAG-signals. By connecting the *TRST-pin of the appropriate device to ground, the TMS320C50 operates in the fundamental mode thus ignoring the JTAG-signals.

- **Using the emulator 10 MHz test clock:**

  In this configuration, the TMS320C50s are directly connected to the JTAG test clock emerging from the emulator.

- **Using a system clock for test purposes:**

  This can be achieved using the machine-cycle rate of the CPU. Although the TMS320C50 has been provided with a CLKOUT1-pin, this pin cannot be used to generate the system test clock because it goes into high-impedance when the JTAG test signal EMU1/*OFF is active low. In order to use a test clock operating under all conditions, an extra crystal oscillator IC can be used.

Figure 6.2 shows a multi-processor configuration. Using jumpers J23 to J29, a daisy-chained configuration (TDO-TDI daisy-chained) or a single processor configuration can be defined. In the modem design, it was made possible to use either a crystal oscillator or the emulator cable pod clock to generate the test clock. In this case, the TCK signal is left unconnected and the output from the crystal oscillator is directly connected to the TCK-inputs of the TMS320C50s and to the TCK_RET input of the emulator using a buffer. The choice between the test clock from the emulator or the crystal oscillator can be made using jumpers J28 and J29 as shown in Figure 6.2. Table 6.2 lists the allowed jumper settings for the single-/multi-processor configurations.

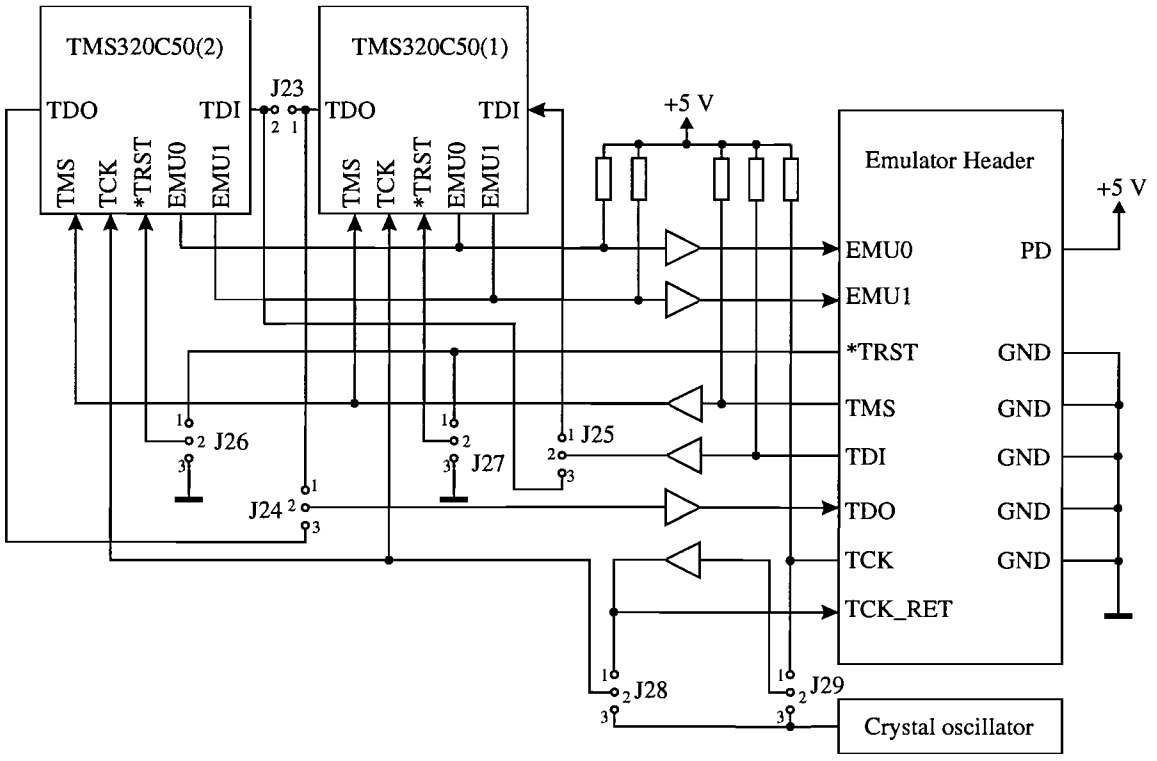


Figure 6.2 Single-/Multi-processor configuration with jumpers [7].

Table 6.2 Allowable jumper settings for the JTAG interface.

J23	J24	J25	J26	J27	J28	J29	Description
12	23	12	12	12	X	X	Multiprocessor-configuration
--	12	12	23	12	X	X	'C50(1) active, 'C50(2) inactive
--	23	23	12	23	X	X	'C50(1) inactive, 'C50(2) active
X	X	X	X	X	23	23	Use crystal for test clock
X	X	X	X	X	12	12	Use emulator (10 MHz) test clock

Note: - 12 = pins 1 and 2 of the jumper are connected
- 23 = pins 2 and 3 of the jumper are connected
- -- = no pins are connected
- X = don't care

The JTAG signals are buffered to isolate the processors from the emulator and provide adequate signal drive for the target system. This buffering is done using the 74F365 buffer IC. The input buffers for TMS, TDI and TCK have pull-up resistors to 5 Volts. This will hold these signals at a known value when the cable pod is not connected. The EMU0 and EMU1 signals also have pull-up resistors to 5 Volts. This will provide a signal rise time

less than 10 μs, therefore meeting the minimum timing requirements of the IEEE 1149.1 specification.

The PD signal of the JTAG-interface must be connected to 5 Volts. This PD signal is a reference to the emulator and indicates that the emulation cable is connected and that the target is powered up.

The attentive reader should have noticed that the JTAG-interface on the modem board is equipped with an extra oscillator block. This is done because the JTAG-interface can put the TMS320C50 in idle mode, thus putting all outputs in high-impedance state. In this way, a clock signal from the TMS320C50's CLKOUT1 output pin cannot be obtained.

6.3 Serial Port

The TMS320C50 has been provided with a full duplex on-chip serial port for direct communication with serial devices. The serial port may also be used for intercommunication between processors in multiprocessing applications. However for these purposes, the TMS320C50 has been equipped with a second time-division-multiplexed (TDM) serial port that allows the TMS320C50 to communicate serially with up to seven other TMS320C50 devices (see Section 6.4 for more information about the TDM-port).

The features of the TMS320C50 serial port are listed below:

- data can be transmitted/received as 8-bit bytes or 16-bit words
- two modes of operation: - burst mode (periods of inactivity between packet transmits on the serial port)
  - continuous mode (continuous stream of data bits)
- maximum operating frequency is CLKOUT1/4 (7.15 Mbit/s at 35 ns clock cycle)
- reset possibility, allowing the TMS320C50 to run in a lower power mode of operation.

Table 6.3 lists the pins used in serial port operation. Three signals are necessary to connect the transmit pins of the transmitting device with the receive pins of the receiving device. The transmitted serial data signal (DX) sends the actual data. The transmit frame synchronization signal (FSX) initiates the transfer (at the beginning of the packet), and the transmit clock signal (CLKX) clocks the bit transfer. The corresponding pins on the receiver device are DR, FSR and CLKR, respectively.

Table 6.3 Serial Port Pins.

Pins	Description	Connector CONN1 pin numbers	
		TMS320C50-1	TMS320C50-2
CLKX	Transmit clock signal	A11	A20
CLKR	Receive clock signal	A14	A23
DX	Transmitted serial data signal	A12	A21
DR	Received serial data signal	A15	A24
FSX	Transmit frame synchronization signal	A10	A19
FSR	Receive frame synchronization signal	A13	A22

The serial port signals of both TMS320C50s, as listed in Table 6.3, are connected to the 2x32-pin connector CONN1. When the TMS320C50 wants to communicate with an external device using the serial port, connections must be made according to Figure 6.3.

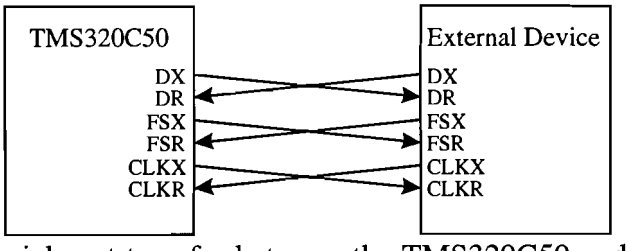


Figure 6.3 Two-way serial port transfer between the TMS320C50 and an external device.

A detailed description of the implementation and operation of the serial port inside the TMS320C50 is listed in [5, Section 5.5].

6.4 TDM Serial Port

The TMS320C50 has a time-division-multiplexed (TDM) serial port that allows the device to communicate serially with up to seven other TMS320C50 devices. The port can be configured to operate in multiprocessing mode or stand-alone mode. When in stand-alone mode, the port operates as described in Section 6.3. The TDM-port supports eight TDM channels. Figure 6.4 shows the TDM port architecture. Up to eight devices can be placed on the four-wire serial bus.

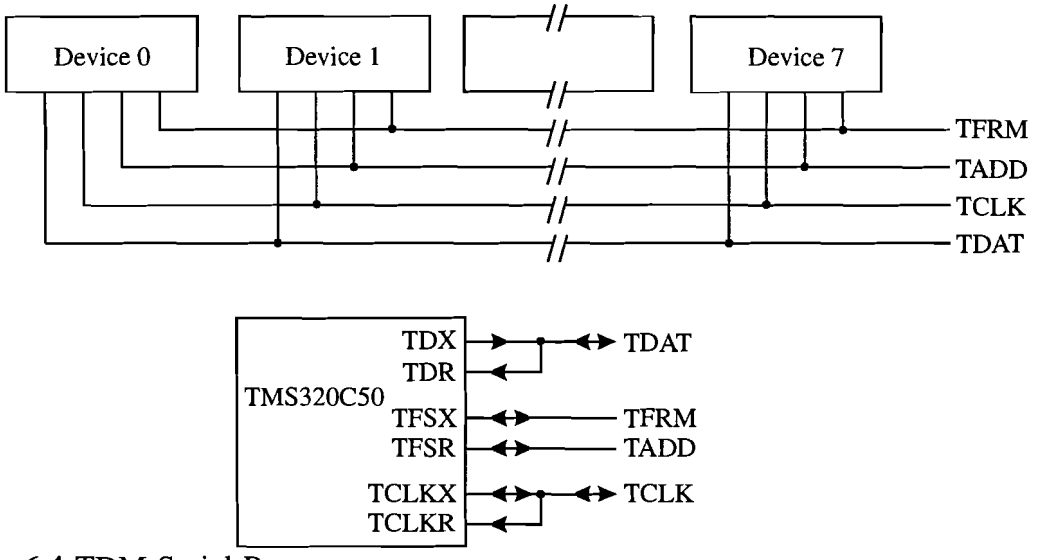


Figure 6.4 TDM Serial Port.

The four-wire bus consists of clock, frame and data (TCLK, TFRM and TDAT) wires plus an additional wire (TADD) that carries the device addressing information. The TADD line determines which devices in the TDM configuration can execute a valid TDM receive on that time slot. The TDAT and TCLK lines are formed by connecting TDX to TDR and TCLKX to TCLKR, respectively.

On the modem board, the TDM lines of both TMS320C50s are connected according to Figure 6.4. Furthermore, for communication with other TMS320C50 devices, the four-wire bus is connected to pins A25 to A28 of the 2x32-pin connector CONN1. A detailed description of the implementation and operation of the TDM serial port is listed in [5, Section 5.6].

6.5 Communications Interface

The spread-spectrum modem is equipped with an interface to communicate with a personal computer (PC). The communications interface and protocol have already been described in [1] but some hardware errors are corrected for the new modem. Figure 6.5 shows the improved communications interface.

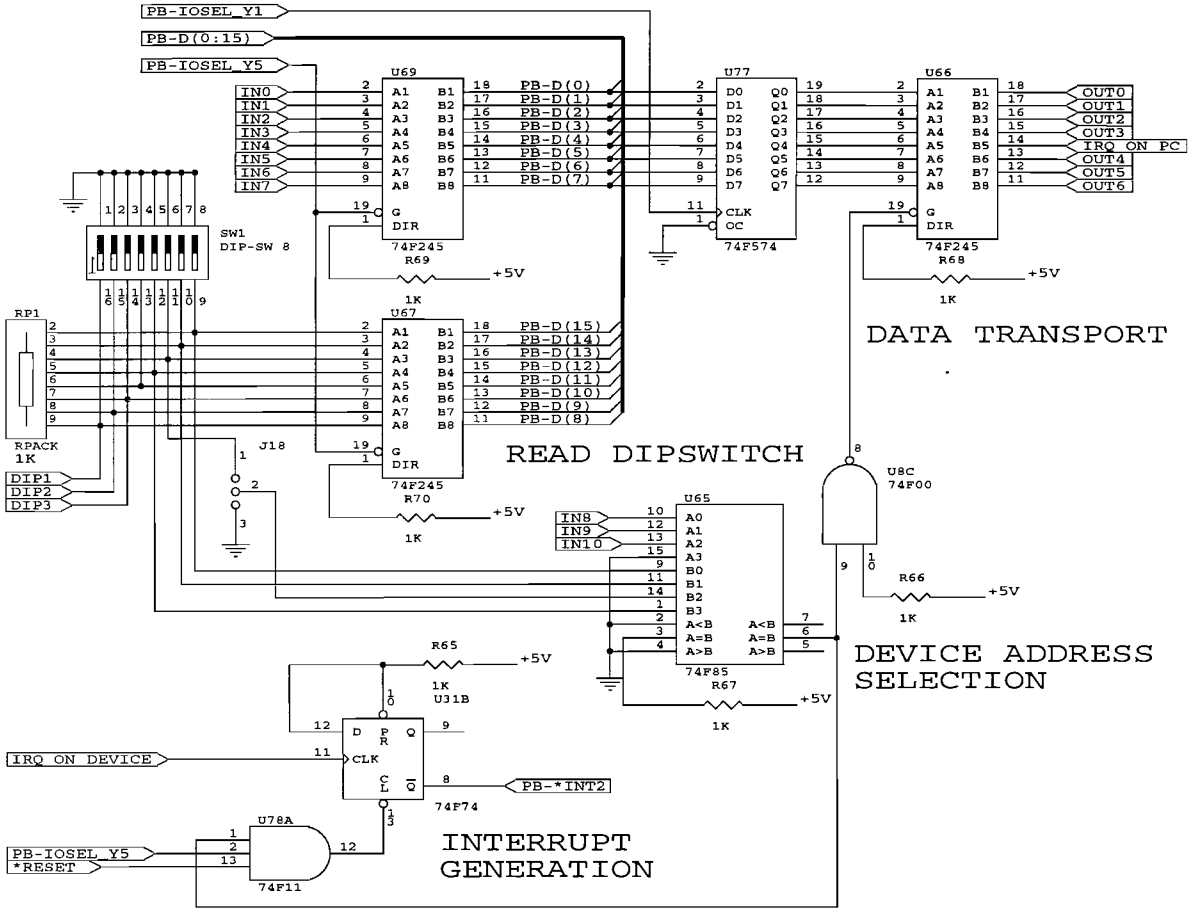


Figure 6.5 The communications-interface hardware [1].

The communications interface consists of four functional blocks:

- data transport
- reading DIP-switch settings
- device address selection
- interrupt generation

Communication is fully interrupt driven on both the personal computer as well as on the modem. Both the personal computer and the modem can initiate communication. However,

the modem must be selected by the personal computer to be able to start communication. Selection of the modem is done using the device address selection circuit. The modem is selected if the address set by the DIP-switches is the same as the one addressed by the personal computer via inputs IN8 to IN10. The DIP-switches 6 to 8 of SW1 specify the device's address. This means that up to eight devices can exchange data with the personal computer. Comparison of the inputs A0-A3 and B0-B3 is done using the 74F85 Comparator (U65). Figure 6.5 shows that input pin A=B (pin 3) is connected to 5 Volts. When inputs A0-A3 equal inputs B0-B3, output A=B (pin 6) is asserted high. This pin can be used for device selection.

Two hardware errors were corrected in the device selection circuit:

- In the previous communications interface, changing the device's address via the three device-select lines IN8-IN10 provided an unwanted interrupt on the digital signal processor [1, p. 62]. Diederen recommended to change the order of the flipflop U20A and the NAND port U21B. In the new communications interface, this recommendation is not followed. Instead, a functionally better solution is implemented. The outcome of output pin A=B of U65 can be seen as a sort of key: if the device is selected, output A=B permits further access to the communications interface; if the device is not selected, output A=B prevents further access. Connecting A=B (together with *RESET and PB-IOSEL_Y5) to the reset input of the D-flipflop will reset the flipflop when a device is not selected and will activate the flipflop when a device is selected. In this way, no unwanted interrupts will occur when a device is not selected, even when the personal computer changes the address.
- Comparing the hardware of the previous and the new communications interface will show that jumper JP10 on the previous interface is removed. This is done because the function of JP10 can also be implemented using DIP-switch 5. Switch 5 is connected to the B3 input of U65 and is compared to the A3 input which is always at a low voltage. So switch 5 acts like an ON/OFF switch without changing the device's address in hardware.

If the personal computer starts communication, a positive edge of 'IRQ ON DEVICE' on U31 generates an interrupt (PB-*INT2) on the TMS320C50(2) and at the same time, data from the personal computer are put on pins IN0-IN7. The interrupt causes the TMS320C50(2) to start the interrupt service routine which uses the IN-instruction to obtain data from the TMS320C50 databus. The IN-instruction asserts I/O-select signal *Y5 low, which enables the 74F245 output pins and resets the interrupt PB-*INT2 by resetting D-flipflop U31. After *Y5 is asserted low, it takes at most 9.0 ns before data from the input pins are on the output pins. From Section 4.7 it follows that, in worst-case, data are on the output pins before *STRB goes high (i.e. within $t_{a(R)}$ ns).

If communication is initiated by a device, a 4-bit word is clocked into buffer U77 and a hardware interrupt on the personal computer is generated by a positive edge of 'IRQ ON PC'. Data is clocked into U77 using I/O-select signal *Y1. Section 4.7 proved that, for the write operation, data are valid before and after *Y1 goes high. If the device is selected, data are put on the output pins OUT0-OUT3 by transceiver U66, which is enabled by the A=B output of comparator U65. OUT4-OUT6 are general-purpose output pins.

Because more space is available on the modem board, the input and output lines of the communications interface are situated on a 25-pin female Centronics connector. In this way, communication between PC and the modem is carried out using standard Centronics cable and connectors. Table 6.4 shows the communications-interface pinout.

Table 6.4 The communications-interface pinout as implemented on the transceiver.

Pin nr.	I/O	Function	Pin nr.	I/O	Function
1	Input	IRQ on device	10	Output	IRQ on PC
2	Input	IN0	11	Output	OUT3
3	Input	IN1	12	Output	OUT2
4	Input	IN2	13	Output	OUT1
5	Input	IN3	14	Input	Device select 0
6	Input	IN4	15	Output	OUT0
7	Input	IN5	16	Input	Device select 1
8	Input	IN6	17	Input	Device select 2
9	Input	IN7	18-25		Digital Ground

6.6 Communicating with the parallel interface

In the spread-spectrum receiver designed by Diederen[1], a frequency synthesizer was used to generate the sample signal f_{fs} for the A/D-converter on the signal-processing board. The output-frequency f_{fs} can be altered in software to equalize f_{fs} with the desired frequency in steps of 100 Hz. However, to enhance this resolution, the frequency synthesizer also generates a 10 kHz reference signal which is fed to the modem for interrupt generation. By means of this interrupt, the TMS320C50 can enhance the frequency resolution of f_{fs} to 10 Hz [2, 4].

In the previous modem design, sending a byte to the frequency-synthesizer was done using the databus from the D/A-converter: the D/A-converter was removed because it was only used in the transmit configuration and a flatcable connector was plugged into the IC-sockets of the unused buffers. In the new modem configuration, a general-purpose 16-bit parallel interface is designed for communication to the frequency synthesizer or to any other external parallel device. This parallel interface is an extension of the DAC-port of the TMS320C50(2) and is capable of reading or writing 16-bit words. The design aspects are listed below:

- general-purpose 16-bit parallel interface for read from and write to an external device, e.g. the frequency-synthesizer board.
- buffered data transfer to avoid busconflicts when the TMS320C50 accesses other devices.
- device-selection must be done using the I/O-select lines from the I/O-selection circuit.
- possibility to read/write 8-bit and 16-bit words.

Figure 6.6 shows the 16-bit parallel interface.

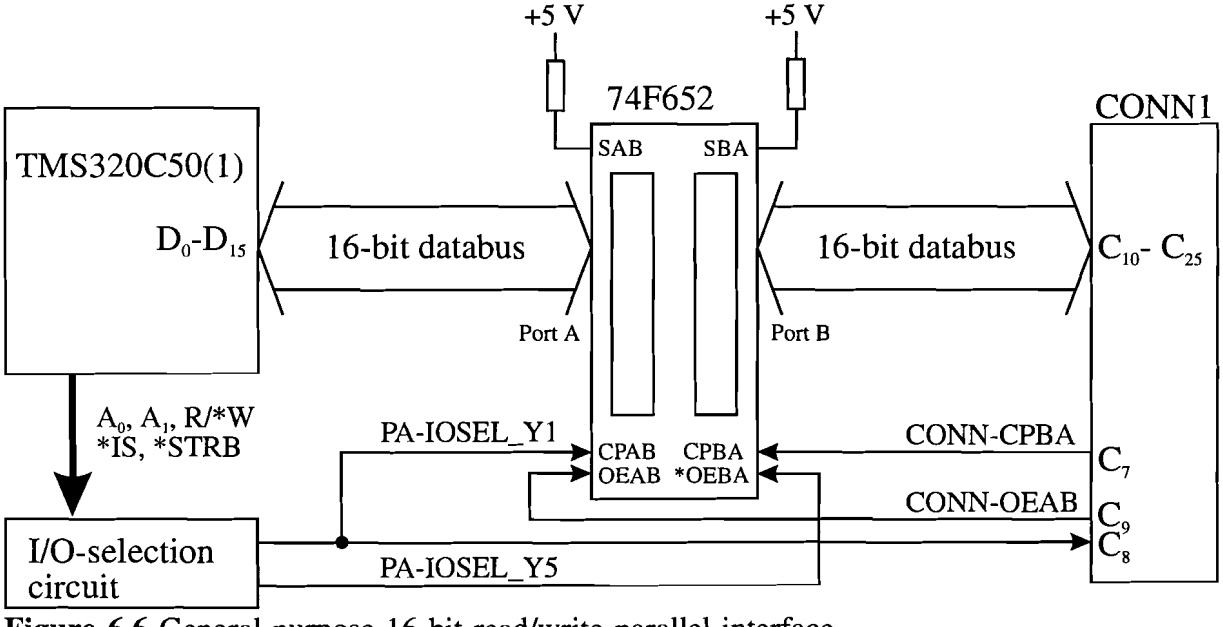


Figure 6.6 General-purpose 16-bit read/write parallel interface.

The 74F652 is an octal transceiver/register with two bidirectional databuses. It contains two 8-bit registers (A0-A7/B0-B7), two clock inputs (CPAB/CPBA), two output enable pins (OEAB/*OEBA) and two select input pins (SAB/SBA). Data can be stored in the internal registers (SAB/SBA is High) or transferred to the opposite databus in real time

(SAB/SBA is Low). For the 16-bit parallel interface, two 74F652 transceiver ICs are required.

The following signals are used for the parallel interface:

- PA-IOSEL_Y1 : line *Y1 from the I/O-selection circuit of processor TMS320C50(1). Used to clock the data from the TMS320C50 into the 74F652 and to interrupt the external device (not the frequency synthesizer) that data are ready in the registers.
- CONN-CPBA : signal from the external device to clock its data into the 74F652.
- CONN-OEAB : signal from the external device to enable the output of the 74F652 to transport data from port A to port B. Connected to +5 Volts for communication with the frequency-synthesizer.
- PA-IOSEL_Y5 : line *Y5 from the I/O-selection circuit of processor TMS320C50(1). Used to enable the output of the 74F652 to transport data from port B to port A.

Two additional signals are used to interrupt the TMS320C50(1) to read the data from the parallel interface:

- CONN-FCONTROL : 10 kHz control frequency of the frequency synthesizer.
- TRANSMITCLOCK : signal from the transmit clock circuit.

The signals labelled with CONN are input signals from the 2x32-pin connector CONN1. Furthermore, PA-IOSEL_Y1 is an output signal situated on the connector CONN1. The operation of the parallel interface is described below.

Data transfer through the 74F652 can be done in real-time or by using interrupts. The real-time data transfer option is not implemented because it can cause databus conflicts. Connecting inputs SAB and SBA to +5 Volts disables the real-time data transfer option.

The interrupt generation circuit for the parallel interface is shown in Figure 6.7. It is used for interrupting the TMS320C50(1) when data are clocked into the 74F652 by the external device. The interrupt is initiated by a low-to-high transition of either the transmit clock or the control frequency from the connector. The interrupt is disabled at reset and when either I/O-select signals *Y1 or *Y5 are enabled.

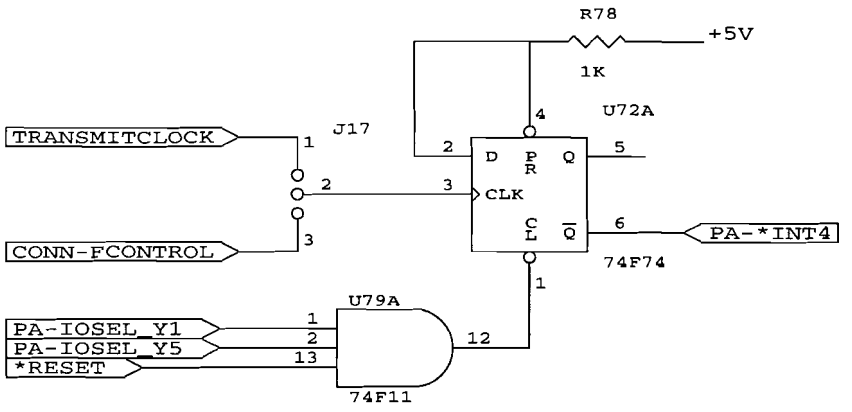


Figure 6.7 Interrupt generation circuit for the parallel interface.

Writing to the parallel interface:

Writing to the parallel interface is done using the OUT instruction. This instruction asserts I/O-select signal *Y1 of the I/O-selection circuit low (see Table 4.16) and TMS320C50 write data are put on the databus. At the rising edge of *Y1, data are clocked into the 74F652. Note that data are still valid during the low-to-high transition of *Y1 (see Section 4.7). *Y1 is also situated on connector CONN1. In this way, the external device is aware when data are clocked in the buffers. Data can be transferred to the device when it asserts CONN-OEAB low. When OEAB is connected to digital ground, TMS320C50 write data are always transferred directly to the parallel interface after they are clocked into the 74F652. This option is useful for the frequency synthesizer board.

Reading from the parallel interface:

After the external device puts data on the parallel interface databus, it asserts CONN-CPBA high. At the rising edge of CONN-CPBA, data are clocked into the 74F652. The device asserts CONN-FCONTROL high to generate an interrupt at the TMS320C50(1). The interrupt service routine uses the IN instruction to obtain data from the device. The IN instruction asserts I/O-select signal *Y5 low, which enables the *OEBA pin. Data from the 74F652 are put on the TMS320C50 databus. When *Y5 goes high, data are read from the databus and the output enable pins are disabled.

7 Software Configurations

7.1 Introduction

This chapter describes some software configurations which must be made for full use of the possibilities of the hardware. Section 7.2 describes how the interrupt vectors can be remapped to any other location in program memory. This is particularly useful when program code is copied from slower EPROM to faster RAM. Section 7.3 shows how on-chip memory can be used together with off-chip memory without address range overlap. Section 7.4 discusses how the amount of global memory can be configured in software. Section 7.5 shows how the internal software wait-state generator of the TMS320C50 can be programmed for 0, 1, 2, 3 or 7 wait-states.

7.2 Remapping interrupts

As was described in Section 4.4.1, accessing the EPROMs is done using seven wait-states. For faster program execution, program code is copied from EPROM to faster RAM. Interrupt vectors which reside at address 0h in program memory must also be moved from EPROM to RAM otherwise fetching the interrupt vector takes also seven wait-states before the interrupt service routine is executed. This section explains how these interrupt vectors can be remapped.

The reset, interrupt and trap vectors are addressed in program space. After the processor takes the trap, it loads the program counter with the trap address and executes code at the vector location. Two words are reserved at each vector location for a branch instruction to the appropriate interrupt service routine. Table 7.1 shows the interrupt vector addresses after reset.

At reset, these vectors are mapped absolutely to address 0h in program space. The vectors can be remapped by loading the interrupt vector pointer (IPTR) bits in the Processor Mode Status Register (PMST) with the appropriate 2K-word page boundary address. The PMST register is one of the twenty-eight core processor registers that are mapped into the data memory space. It contains extra status and control information for control of the enhanced features of the TMS320C50 core. This register resides at address 7h in the data memory space. Figure 7.1 shows the organization of the PMST register. The five bits of the IPTR-

Table 7.1 TMS320C50 Interrupt Vector Addresses.

Name	Location		Priority	Function
	Dec	Hex		
*RS	0	0	1	External reset signal
*INT1	2	2	3	External user interrupt #1
*INT2	4	4	4	External user interrupt #2
*INT3	6	6	5	External user interrupt #3
TINT	8	8	6	Internal timer interrupt
RINT	10	A	7	Serial port receive interrupt
XINT	12	C	8	Serial port transmit interrupt
TRNT	14	E	9	TDM port receive interrupt
TXNT	16	10	10	TDM transmit interrupt
*INT4	18	12	11	External user interrupt #4
----	20-33	14-21		Reserved
TRAP	34	22		Software trap instruction
NMI	36	24	2	Nonmaskable interrupt
----	38-41	26-29		Reserved for emulation and test
----	42-47	2A-2F		Software interrupts

field offer the possibility to remap the interrupt vectors to the beginning of 32 2K-word pages.

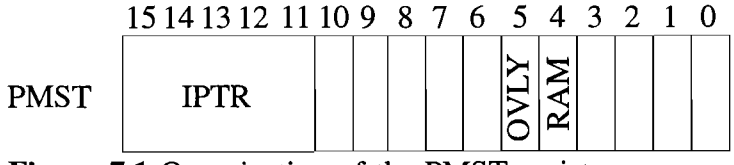


Figure 7.1 Organization of the PMST-register.

In the modem design, program code from EPROM (start address is 0h) is copied to RAM (start address is 8000h). Therefore, the IPTR-field must contain the value 10h. In software, the OPL-instruction performs an OR-operation on the contents of a specified data memory address:

```
OPL #08000h, PMST    ; Remap vectors to start at 8000h
```

The reset vector cannot be remapped because reset loads the IPTR with 0s. Therefore, the reset vector will always be fetched at location 0h in program memory.

7.3 Configuring on-chip memory

As was explained in section 4.2, the TMS320C50 has been provided with 9K words of on-chip program/data SARAM and 1056 words of on-chip data DARAM. However, the address ranges of these on-chip memories overlap the address range of the EPROM. Software configurations are needed in order to access the on-chip memory as well as the EPROM. This can be done using the processor mode status register (PMST) shown in Figure 7.1 and the status register ST1.

Bits 4 and 5 of the PMST are used for configuring on-chip memory. Bit 4 (RAM) enables mapping of on-chip SARAM blocks into program space. Setting RAM to one maps the memory block in program space. Setting RAM to zero removes the memory block from the program space. Bit 5 (OVLY) enables on-chip SARAM cells to be mapped into data space. If OVLY is set to one, the block of memory is mapped into data space. If it is set to zero, the memory block is not addressable in data space. Both bits are set to zero at reset. From status register ST1, the CNF bit is used. If this bit is set to zero, the DARAM blocks are mapped to data space; otherwise, block B0 is mapped to program space. Table 7.2 shows the program memory configuration using the CNF bit and the RAM bit.

Table 7.2 TMS320C50 Program memory configuration control.

CNF	RAM	SARAM	DARAM B0	Off-Chip
0	0			0000-FFFF
0	1	0800-2BFF		0000-07FF
				2C00-FFFF
1	0		FE00-FFFF	0000-FDFF
1	1	0800-2BFF	FE00-FFFF	0000-07FF
				2C00-FDFF

Table 7.3 shows the data memory configuration using the CNF bit and the OVLY bit.

Table 7.3 TMS320C50 Data memory configuration control.

CNF	OVLY	DARAM B0	DARAM B1	DARAM B2	SARAM	Off-Chip
0	0	100h-2FFh	300h-4FFh	60h-7Fh		800h-FFFFh
0	1	100h-2FFh	300h-4FFh	60h-7Fh	800h-2BFFh	2C00h-FFFFh
1	0	-	300h-4FFh	60h-7Fh		800h-FFFFh
1	1	-	300h-4FFh	60h-7Fh	800h-2BFFh	2C00h-FFFFh

Setting/resetting bits in the PMST register is done using the OPL-instruction. Setting/resetting the CNF bit is done using the SETC/CLRC-instruction.

7.4 Configuring global memory

Another register from the twenty-eight core processor registers is the global memory allocation register (GREG). It is a memory-mapped register which resides at address 5h in page zero of the data memory space. This register specifies part of the TMS320C50 data memory as global external memory. Figure 7.2 shows the structure of the GREG register.

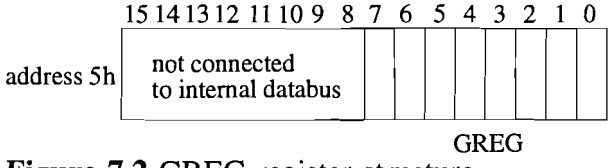


Figure 7.2 GREG register structure.

GREG is an 8-bit register connected to the eight LSBs of the internal databus. The upper eight bits of location 5h are nonexistent.

The contents of GREG determine the size of the global memory space between 256 and 32K words. As was described in Section 4.6.1, only 1K words of global memory is present on the modem board. This 1K Dual-port SRAM can be changed by the 2K-words version. Table 7.4 shows the legal values of GREG for the modem design and corresponding global memory spaces.

Table 7.4 Global Data Memory Configurations.

GREG Value	Local Memory		Global Memory	
	Range	# Words	Range	# Words
00000000	0h-FFFFh	65536	-	0
11111000	0h-F7FFh	63488	F800h-FFFFh	2048
11111100	0h-FBFFh	64512	FC00h-FFFFh	1024
11111110	0h-FDFFh	65024	FE00h-FFFFh	512
11111111	0h-FEFFh	65280	FF00h-FFFFh	256

7.5 Programming the software wait-state generator

Software-programmable wait-state generators can be used to extend external bus cycles by up to seven machine cycles. This provides a convenient means for interfacing external devices that do not satisfy the full-speed access-time requirements of the TMS320C50. The software-programmable wait-state generators are controlled by two 16-bit wait-state registers (PDWSR and IOWSR) and a 5-bit control register (CWSR). Wait states for the program and data spaces are specified in the lower and upper halves of the program/data wait-state register (PDWSR) respectively. Wait states for I/O space are specified in the I/O wait-state register (IOWSR). The control wait-state register (CWSR) controls the mapping between wait-state register contents and the number of wait states.

The program and data space each consist of 64K addresses. Each 64K space can be viewed as being composed of four 16K-word blocks. The PDWSR reserves two bits for each 16K-word block of program or data memory. The value of a 2-bit field in PDWSR specifies the number of wait states to be inserted for each access in the given space and address range. Figure 7.3 shows the association of the 2-bit fields of the PDWSR with each 16K-word memory segment.

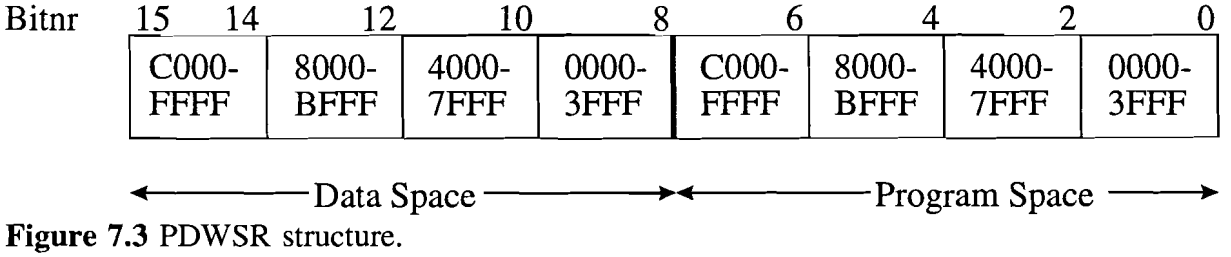


Figure 7.3 PDWSR structure.

From Figure 7.3 it can be seen that assigning wait states for access to the EPROMs, bits 0-3 have to be initialized. For access to the (DP)SRAMs, bits 4-7 have to be initialized.

The IOWSR can be mapped in either of two ways, as specified by the BIG bit in the CWSR register. If BIG=0, each of eight pairs of memory-mapped I/O ports has its own 2-bit field in IOWSR as is shown in Figure 7.4.

Bitnr	15 14	12	10	8	6	4	2	0
	Port 14/15	Port 12/13	Port 10/11	Port 8/9	Port 6/7	Port 4/5	Port 2/3	Port 0/1

Figure 7.4 IOWSR structure (BIG=0).

Note that the entire I/O space is configured with wait states because port n/(n+1) has the same number of wait states as port (16·m+n)/(16·m+n+1) with $0 \leq n \leq 14$ and $0 \leq m \leq 3$. If BIG=1, the 64K I/O space is divided into eight 8K-word address blocks with each block having an independently programmable number of wait states. Figure 7.5 shows the association of the bits in the IOWSR with the eight memory segments.

Bitnr	15 14	12	10	8	6	4	2	0
	E000-FFFF	C000-DFFF	A000-BFFF	8000-9FFF	6000-7FFF	4000-5FFF	2000-3FFF	0000-1FFF

Figure 7.5 IOWSR structure (BIG=1).

The wait-state fields of PDWSR and IOWSR can be filled with four binary values. However, five different number of wait-states can be implemented. This is solved using the control wait-state register (CWSR). The four bits in the CWSR allow the user to select one of two mappings between 2-bit wait-state fields and the number of wait states for the corresponding space as shown in Table 7.5.

If bit n of CWSR is set to zero, the number of wait states for external accesses in the space associated with bit n is equal to the wait-state value as specified in the 2-bit field of the PDWSR or IOWSR. If bit n is set to one, the number of wait states is determined by the last column of Table 7.5. Figure 7.6 shows the CWSR structure.

Bit n	4	3	2	1	0
	BIG mode	I/O upper	I/O lower	Data	Program

Figure 7.6 CWSR structure.

Table 7.5 Wait-State Field Values and Wait States as a Function of CWSR Bit n.

Wait-State Field of PDWSR or IOWSR (Binary Value)	No. of Wait States (CWSR Bit n = 0)	No. of Wait States (CWSR Bit n = 1)
00	0	0
01	1	1
10	2	3
11	3	7

Bit 2 represents the lower-half of the I/O space: Port 0 - Port 7 if BIG=0 or 0000h-7FFFh if BIG=1. Bit 3 represents the upper-half of the I/O space: Port 8 - Port 15 if BIG=0; 8000h-FFFFh if BIG=1.

The next example will show how the software wait-state generator is to be programmed. For the modem design, the EPROMs (0000h-7FFFh) are accessed using seven wait states, the SRAMs (8000h-FBFFh) are accessed using zero wait states and the DPSRAMs (FC00h-FFFFh) are accessed using one wait state. From Table 7.5, it follows that for seven wait states bit 0 (for program space) of the CWSR is set to 1. The bits in PDWSR corresponding with the address range of the EPROMs are filled with the value 11b. For zero or one wait states, bit 1 (for data space) of the CWSR may either be 0 or 1. The bit field in PDWSR corresponding with the SRAM address range are filled with the value 00b and the bit field corresponding with the DPSRAM address range are filled with 01b. This leads to the following contents of the CWSR and the PDWSR (X is don't care):

CWSR = XXXX1b
PDWSR = 01 00 XX XX XX XX 11 11b

In the modem design, the distinction between program memory and data memory is not made. In order to prevent equal address ranges to be programmed with a different number of wait states, it is recommended that the PDWSR bits from the same address ranges are assigned the same values. In this case, PDWSR = 01 00 11 11 01 00 11 11b.

Accessing I/O ports 0/1 and 6/7 with two wait states results in the following contents of CWSR and IOWSR:

CWSR = 0X0XXb
IOWSR = XX XX XX XX 10 XX XX 10b

8 Implementing the new modem

8.1 Introduction

The previous chapters described the functional blocks of the modem in detail. This chapter discusses the implementation of the functional blocks to come to a realization of the new modem. The implementation process consists of five steps:

1) creating the schematic diagrams using a design program for electronic circuits (Section 8.2).
2) Electro Magnetic Compatibility (EMC) considerations must be taken into account for better performance and less radiation of the printed circuit board (PCB) (Section 8.3).
3) Print layout and component placement. Using the EMC considerations, great care should be taken for positioning of components on the printed circuit board (Section 8.4).
4) Routing (Section 8.5).
5) Soldering the components, testing the print and preparing the print for the modem configuration (Section 8.6).

8.2 Creating the Schematic Diagrams

To come to a realization of the modem, the first step is to create the schematic diagrams using the design considerations of the functional blocks described in chapters 3 to 6. The actual design of the printed circuit board is done at the Centrale Technische Dienst (CTD, Central Technical Service) of the Eindhoven University of Technology. They are equipped with software to develop printed circuit boards: the DAZIX Intergraph Schematic Entry program for drawing the schematic diagrams and the StarTrak Router for routing the PCB. The advantage of this Schematic Entry program is that it runs on a Sun workstation with a user-friendly graphics user interface. Furthermore, when placing the components, gate swapping or pin swapping automatically changes the drawings made with the Schematic Entry program. Although OrCAD can also be used to generate the schematic diagrams, this method is not recommended. OrCAD generates a netlist, in which all parts of the circuit and all connections between parts are listed in a specific format. This netlist is used

at the CTD to design the printed circuit board. However, gate and pin swapping will not change the drawings made by OrCAD.

Appendix 1 comprises the schematic diagrams of the modem. Before describing the sheets in detail, some general information about schematic entry is given below:

- data/address-buses must be labelled D(0:15) and A(0:15), respectively. The names may change (e.g. PA-D(0:15) or PB-D(0:15)) but the brackets and the colon must be used to denote the number of data/address-lines. Signal lines from the data/address-buses are labelled using brackets (e.g. PA-D(0)). Note that these brackets may not be omitted.
- signal lines with the same label are connected physically. Furthermore, connecting two pins together using a wire is the same as labelling the two pins with the same label without making the connection. See also the PA-*BR, PA-*WE, PA-*RD and PA-READY signals of the DPSRAM on sheet 5.
- labelled signal lines with a port symbol are signal lines also used on other sheets.
- the label REPEAT=n is used to denote that the corresponding component is repeated n times.
- some ICs do not have a power supply pin and a ground pin because these pins are defined implicitly. When defining components, labels can be assigned to pin numbers. It is possible to assign VCC and GND to the corresponding pin numbers without the necessity to draw the actual pins.
- All inputs of TTL ICs which must at a high voltage are connected to +5 Volts using a 1K pull-up resistor.

For each schematic diagram, some design considerations are listed:

Sheet 1/2:

- All unused input pins of the TMS320C50 should be connected to +5 Volts with or without an external 100K pull-up resistor.
- All unused outputs of the TMS320C50 should be left unconnected.
- The power supply lines for the TMS320C50, the EPROMs, the SRAMs and the TTL ICs are decoupled using 0.1 µF ceramic capacitors (see Section 8.3).
- The *BIO input pin and XF output pin are situated on the 2x32-pin connector and therefore buffered using two-input AND gates.
- The *NMI and PA-*INT2 input pins are not buffered because interrupt generation must be done using a D-flipflop. Furthermore, these pins will not be used so they are connected to +5 Volts at connector CONN1.

- The (TDM) serial port signals are connected to +5 Volts/digital ground using 100K pull-up/pull-down resistors. This is done to define these signals when they are in high-impedance mode, therefore preventing unwanted signals on the (TDM) serial port [8].

Sheet 3:

- Resistors R83 and R86 do not belong to the E12 range. Therefore, a standard resistor is assigned the appropriate value. In the modem design, R83 is 24.9 Ω and R86 is 51 kΩ.
- At first, pins T7 and T8 were provided to make a connection between analog and digital ground as specified in the AD1671 datasheets. Later, this connection was made at the power connector. Pins T7 and T8 are now used for analog and digital ground references during test procedures.
- The REF OUT pin is decoupled using a 1 µF tantalum capacitor to analog ground according to the AD1671 data sheets.

Sheet 4:

- A 7 pF capacitor (C10) is not available. Therefore, a 6.8 pF capacitor is used.
- Resistor R33 (200 Ω) does not belong to the E12 range. Therefore, a standard resistor is assigned the appropriate value.

Sheet 5:

- According to the datasheets of the CY7C131/CY7C141 DPSRAM, the *BUSY output of the master DPSRAM and the *INT output are open drain outputs and require pull-up resistors.

Sheet 6:

- Capacitors are provided to decouple the power supply lines from the AD1671, the AD568 and the AD840 in accordance with the data sheets.
- All unused TTL gates are listed with their inputs connected to digital ground.

The modem board is equipped with four connectors: a 2x32-pin male connector (CONN1), a 25-pin female Centronics connector (CONN2), a 14-pin male flatcable connector (CONN3) and the power connector. Furthermore, two BNC-connectors are provided for analog input and output signals. Design considerations for each connector are listed below (for pin locations, see Appendix 2).

2x32-pin connector:

- to communicate with serial devices, the serial port signals of both TMS320C50s are situated on the connector.

- to communicate with other TMS320C50 devices, the TDM serial port signals are situated on the connector.
- the 16-bit parallel interface control signals and its databus are situated on the connector for communication with external devices.
- CONN-*RESET is provided to perform an externally generated reset.
- *RESET is provided to reset external devices after a modem reset.
- *BIO, *NMI and XF signals from both TMS320C50s are provided to control the processors externally (generating an interrupt, asserting *BIO low for a branch instruction to be executed).
- the unused I/O-select signals from both I/O-selection circuits are situated on the connector to access/control external devices.
- VCC and GND are provided as outputs for test purposes.
- The unused interrupt *INT2 from TMS320C50(1) is situated on the connector as an extra external interrupt generation possibility.

25-pin female Centronics connector:

- all communications interface signals are situated on the connector according to [1, Table 6.2].

14-pin flatcable connector:

- all JTAG interface signals are situated on the connector according to the specifications in [5, Appendix E].

Power connector:

- The power connector is equipped with ±15 Volts, ±5 Volts and analog and digital ground. This special connector is used because the digital ICs can have a maximum (worst-case) supply current of 5 A. This is far too much to be supplied by pins from the 2x32-pin connector as was done in [1].

8.3 EMC Considerations

Before components are placed on the printed circuit board and routing is performed, some EMC considerations must be taken into account. These considerations are necessary because components and connections can interfere to each other and to other printed circuit boards. Some rules on positioning of components and routing are presented in [1, 9].

The EMC considerations for the multilayer PCB design are listed below:

- keep digital and analog circuitry separated;
- oscillators and clock circuits should be located near the centre of the PCB. This minimizes coupling to I/O runs and places the higher-frequency sources in the centre of the power and ground distribution system;
- initiate placing the oscillator circuit, processor, memory, and fast I/O;
- make critical signals first priority in the layout, so they can be handled most effectively
- keep connections as short as possible;
- isolated digital and analog power supplies should be used when mixing digital and analog circuitry on a PCB. Single-point common grounding of the analog and digital power supplies should be performed at one point and one point only;
- add decoupling capacitors. These should be placed as close as possible to the power pins of the integrated circuits. High-frequency decoupling should be done with ceramic capacitors since the inductance of the capacitor is less than with other types;

Some supplementary rules on analog circuitry:

- keep related parts very close together and connections very short;
- circuits must be separated to keep unwanted interaction among them to a minimum;
- the surrounding space can be floated with ground, thus improving the ground plane distribution and further isolating the circuits;
- add decoupling capacitors.

Decoupling capacitors are placed for two purposes. They supply transient current to the chip during gate switching. Secondly, they limit the size of a potential radiating loop associated with the power supply to a switching gate. To minimize this radiation, special IC-sockets with decoupling capacitors assembled in it are provided.

8.4 Layout and Component Placement

Using the EMC considerations from Section 8.3, the layout of the printed circuit board (PCB) can be carried out (see Appendix 1). The PCB is a multilayer PCB with 4 layers:

- layer 1 : component/signal layer
- layer 2 : digital ground plane
- layer 3 : +5 Volts power supply plane
- layer 4 : solder/signal layer

The digital ground and +5 Volts power supply planes of the multi-layer PCB offer great advantages with regard to EMC problems and routing:

- no ground power and supply power runs across the PCB are necessary. This results in easier routing of signal lines;
- the shortest connections possible between ICs and their power supply units;
- less radiation due to the smaller area of the current loop;
- low-impedance.

Component placement and the routing process are related to each other. A well-considered and time-consuming component placement results in an easier and faster routing process.

The components are placed according to the functional block diagram of Figure 2.1. For a good component placement, the following design considerations are made:

- the oscillator (U47), the 74F14 Schmitt-trigger inverter (U46) and jumpers J19 and J20 are placed as close to the TMS320C50s as possible in order to obtain signal lines with the same length. In this way, both TMS320C50s will operate synchronously.
- the 74F11 three input OR-gate is used twice on the board although one 74F11 would be satisfactory. However, two gates of the 74F11 were used for the communication interface while the third gate was used for the 16-bit parallel interface. To avoid long signal lines, two ICs were used: U78 was placed in the vicinity of the communication interface and U79 was placed near the parallel interface.
- the analog circuitry is separated from the digital circuitry. Furthermore, it is placed at the front of the PCB close to the BNC connectors. To reduce EMC problems, an analog ground plane is placed directly beneath the analog circuitry.
- the connectors are placed at the end of the PCB except for the power connector. It is placed close to the analog circuitry to avoid long analog power supply and ground lines across the PCB.
- to facilitate the solder process, all DIP IC-sockets are placed either in vertical or in horizontal direction with pin 1 always pointing in the same direction. However, some IC-sockets are placed opposite the directions in cases where easier signal routing prevailed.

- BNC-connectors are now mounted on the PCB to shorten signal lines and to prevent antenna radiation.
- all DIP IC-sockets for TTL ICs have been equipped with decoupling capacitors. The PLCC and PQFP IC-sockets have not been equipped with decoupling capacitors so they are provided externally. The D/A converter and opamp require their own capacitors so DIP IC-sockets are used without decoupling capacitors.
- the components are placed in such a way that space between components is available to facilitate the routing process.

When placing components, the software allows the user to perform gate swapping or pin swapping. This is done to obtain the shortest possible overall wire length and to minimize routing complexity. Figure 8.1 shows the gate and pin swapping method.

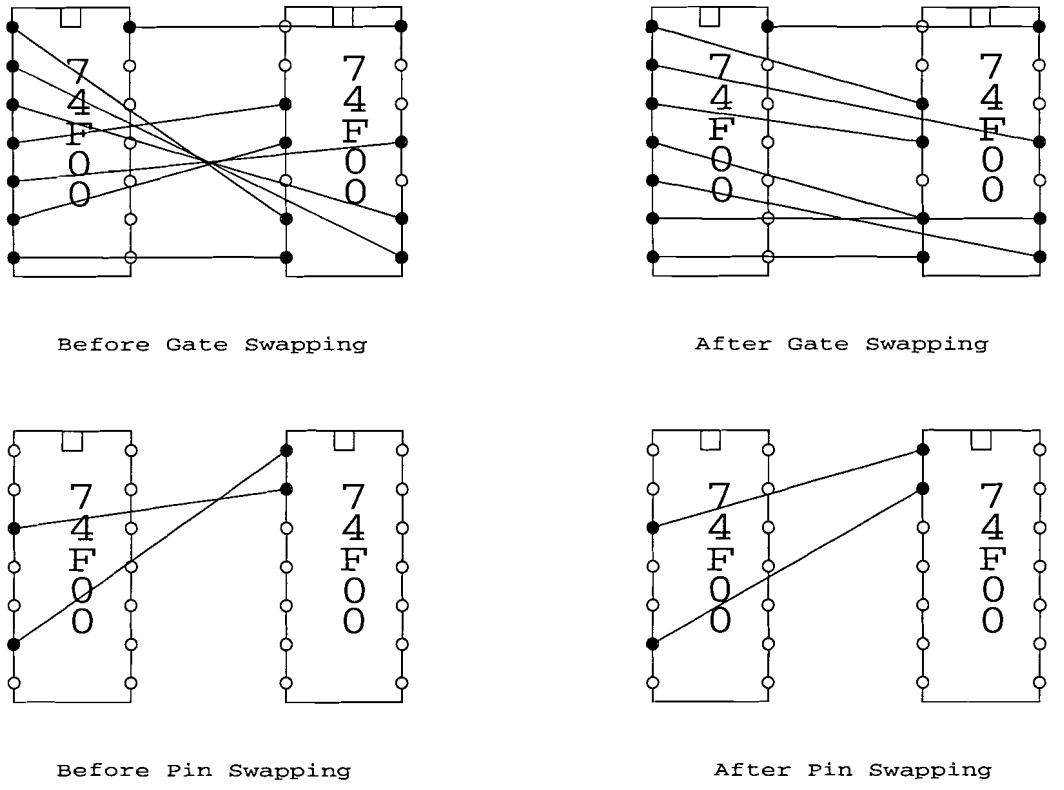


Figure 8.1 Gate and pin swapping.

Note that pins 1 and 2 of the 74F00 IC in Figure 8.1 are input pins, therefore pin swapping is allowed.

8.5 Routing

After components are placed on the printed circuit board, routing can begin. The routing process can be done either manually or automatically. Manual routing is done in the following cases:

- the oscillator signal lines to both TMS320C50s must be of equal length in order to prevent unwanted timing delays to occur.
- simple signal lines can be routed manually (see Figure 8.2).
- memory routing (see Figure 8.3).

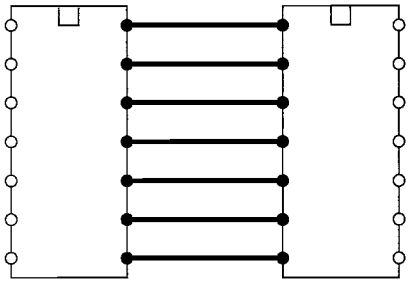


Figure 8.2 Simple routing.

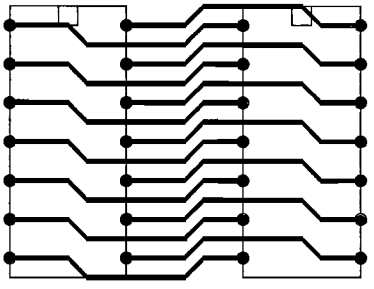


Figure 8.3 Memory routing.

From the initial 1264 connections on the printed circuit board, over 650 connections were done manually. Note that due to the digital 0 V and +5 V planes, connections for the supply voltage are performed automatically.

After manual routing, the StarTrak router available on the CTD workstations is started. The router performs the following passes:

- single pass
- iterative pass
- finishing pass
- iterative pass
- finishing pass
- final finishing

A single pass tries to make connections just once. If a connection is not made, it is left open to be routed after the single pass. An iterative pass performs several iterations. After each pass, the program examines traces that block paths to unconnected pins. On succeeding passes, the program reroutes the blocking traces and attempts to complete the

rest of the connections. A (final) finishing pass shortens signal paths, substitutes diagonals for staircases and removes unneeded vias (= connection between layers 1 and 4).

Sheets 8 and 9 of Appendix 1 show the outcome of the manual/automatic routing process.

8.6 Testing the printed circuit board

After the printed circuit board is manufactured, components can be soldered and test procedures can be carried out. Within the time constraints, it was not possible to perform these test procedures.

The printed circuit board can now be used as part of the baseband picoterminal. The next step is to implement the spread-spectrum modem in software using the PCB. Some hardware settings must be installed before the PCB can be used as a picoterminal.

The following pins on the 2x32-pin connector have to be tied to +5 Volts using a pull-up resistor (only if they are not used):

- PA-*NMI, PB-*NMI
- PA-*BIO, PB-*BIO
- PA-*INT2

For communication to the external frequency synthesizer board, the following pins on the 2x32-pin connector must be defined:

- CONN-CPBA may be either Low or High but no Low-to-High transition may occur.
- CONN-OEAB must be low to enable the output pins of the 74F652 ICs, therefore transferring TMS320C50 write data to the frequency board.

Table 8.1 lists the jumper settings. Appendix 2 lists the description of jumper settings and connector pins.

Table 8.1 Jumper settings

Jumper	Setting	Jumper	Setting
J1	12	J16	X
J2	--	J17	23
J3	--	J18	X
J4	23	J19	12
J5	12	J20	23
J6	12	J21	23
J7	--	J22	23
J8	12	J23	12
J9	--	J24	23
J10	--	J25	12
J11	12	J26	12
J12	--	J27	12
J13	X	J28	12
J14	X	J29	12
J15	X		

Note : -- = not connected
X = don't care; either 12 or 23

9 Conclusions and Recommendations

9.1 Conclusions

- For the picoterminal project, the hardware of a baseband spread-spectrum picoterminal was designed and implemented. The design was done according to the functional block diagram. Memory ICs were chosen in concurrence with TMS320C50 timing requirements. It was shown that communicating with different (memory) ICs does not result in databus conflicts.

- Communicating between the two TMS320C50s is done using global memory. This memory was implemented using a Dual-Port SRAM. With this DPSRAM IC, two processors can independently access different global memory locations simultaneously.

- To enhance the processing speed of the receiver part of the modem, a new analog-to-digital conversion circuit was designed. For this ADC circuit, a new A/D-converter was used and a sample switch was designed. For the transmitter part of the modem, the digital-to-analog circuit of the previous modem was used in the new modem.

- Testing and debugging is now done using the JTAG-interface. The hardware required was designed and implemented. Testing and debugging can be done using the Texas Instruments XDS510 emulator.

- Two serial ports are implemented on the signal board to communicate with serial external devices. Furthermore, the two TMS320C50s can communicate with other external TMS320C50 devices using the TDM serial port option. A new parallel interface was designed for communication with parallel external devices. The PC-communications interface as was used with the previous modem is also used for the new modem. Communicating with the personal computer is now done using standard Centronics cable/connectors.

- Some software configurations were presented which must be taken into account when the TMS320C50s are to be programmed.

- The signal processing board was realized using the Schematic Entry program of the Centrale Technische Dienst (CTD) at the Eindhoven University. After schematic entry, component placement and routing was performed to obtain the signal runs on the printed circuit board. The PCB was manufactured and components were soldered on it. The signal processing board is now ready to be tested.

- The function of the signal processing board is dependent on the software implementation. Therefore, the board could also be used for general signal processing applications such as a telephone modem or sound blaster.

9.2 Recommendations

For future printed circuit board design, some recommendations are presented:

- Future printed circuit boards are to be realized using the Schematic Entry program and StarTrak router of the Centrale Technische Dienst (CTD) of the Eindhoven University of Technology. In this way, designing printed circuit boards is more flexible and user-friendly. Furthermore, when placing the components, gate swapping or pin swapping automatically changes the drawings made with the Schematic Entry program.

- To implement the features of the spread-spectrum picoterminal, the TMS320C50 processors need to be programmed. Before software is designed to access the global memory, a communication protocol must be set up in which communication to the global memory is well-defined.

- The unused inputs (PA-*NMI, PB-*NMI, PA-*BIO, PB-*BIO, PA-*NMI) of the 2x32-pin connector CONN1 must be connected to +5 Volts at the connector. In future it is better to use jumpers at the PCB to connect the unused inputs to +5 Volts. If the inputs are used, jumper settings are altered to use the input pins on the connector.

- For future PCB design, it is better to use programmable logic devices (PLDs) instead of TTL ICs. In this way, logical functions can be programmed on one IC. This saves a lot of space on the PCB and occasional errors can be corrected easily.

- Research must be performed to investigate whether the communications interface as implemented on the modem print can be replaced by a standard interface used on personal computers or notebooks.

- In future, the input signals CONN-FFS and CONN-FCONTROL and the signal TRANSMITCLOCK should be implemented using BNC connectors. This prevents the connector CONN1 from being soldered with wires to obtain these signals.

- Before the signal board can be used as part of the picoterminal, testing the signal board is required. This testing must be done with great care so no errors will occur when placing the ICs on the board.

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Appendix 1: Schematic Diagram, Component Placement and Print Layout of the Modem Print

This appendix gives an overview of the hardware designed. Figure A.1.1 and Figure A.1.2 show the TMS320C50(1) and the TMS320C50(2) with their local memory and I/O-selection circuits. Figure A.1.3 shows the ADC circuit with the pulse generation circuit, the A/D converter, the switch with its buffers and the interrupt generation circuit. Figure A.1.4 shows the DAC circuit with the D/A converter and the opamp, the transmit clock and the 16-bit parallel interface. Figure A.1.5 shows the global memory implementation and the communications interface. Finally, Figure A.1.6 shows the reset and oscillator circuit, the JTAG interface, the connectors and decoupling capacitors for the analog circuitry.

Figure A.1.7 shows the component placement on the printed circuit board (PCB) where the black marks on each jumper denote pin 1. Figure A.1.8 and Figure A.1.9 show the component side (layer 1) and the solder side (layer 4) of the designed PCB, respectively.

Figure A.1.1 The TMS320C50(1) with its local memory and the I/O selection circuit.

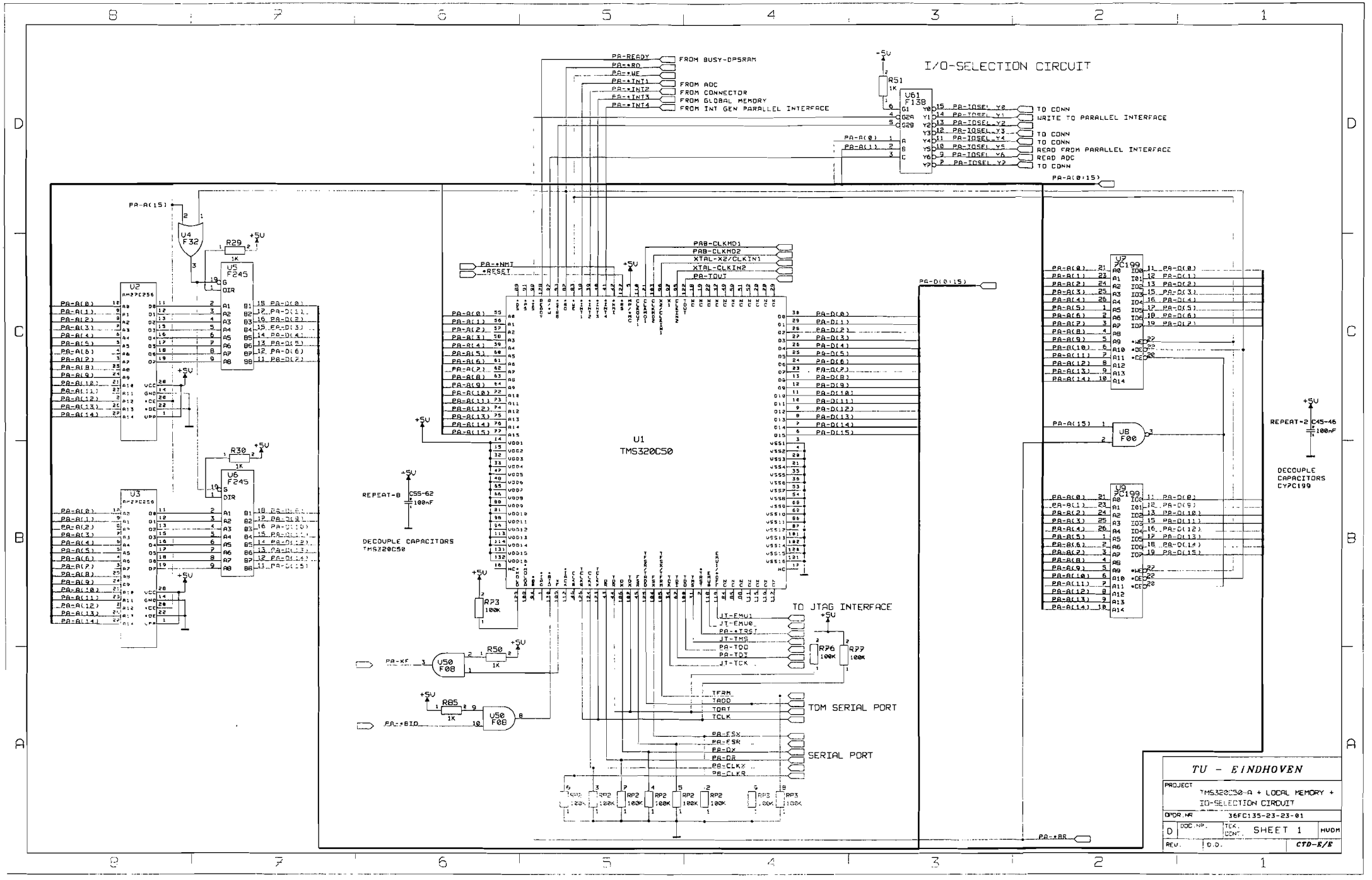


Figure A.1.2 The TMS320C50(2) with its local memory and the I/O selection circuit.

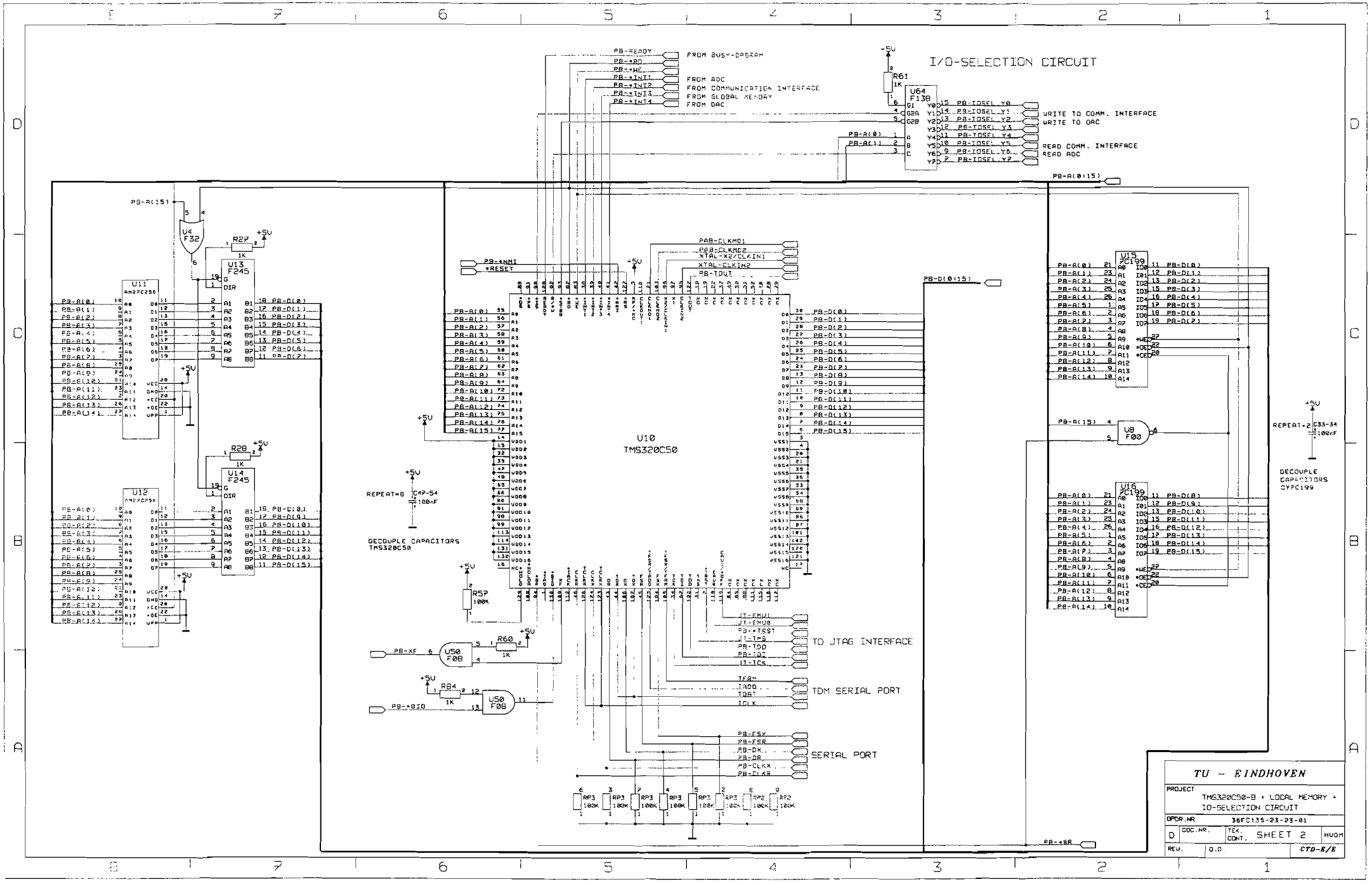


Figure A.1.3 The ADC circuit.

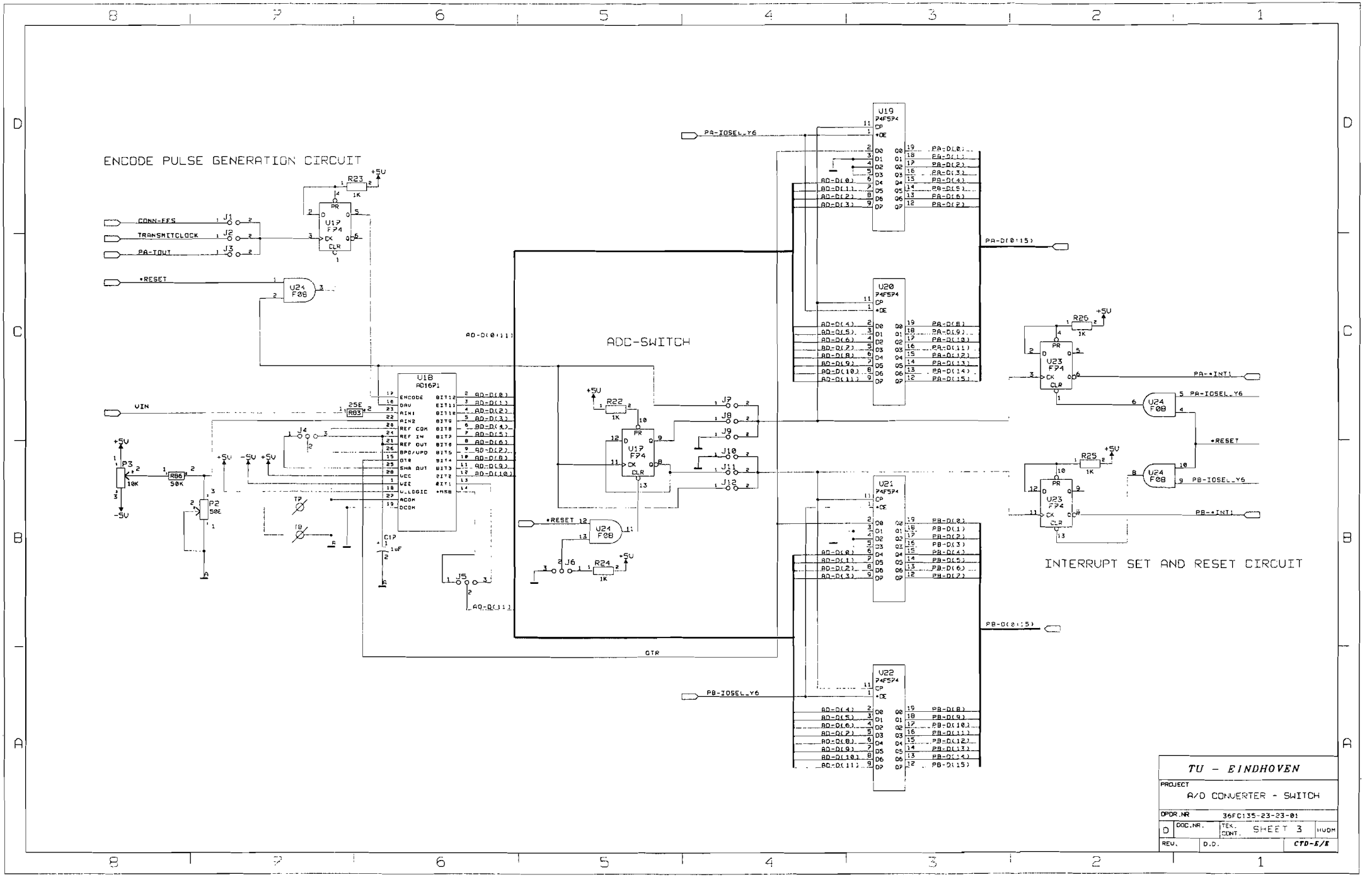


Figure A.1.4 The DAC circuit with the transmitclock and the 16-bit parallel interface.

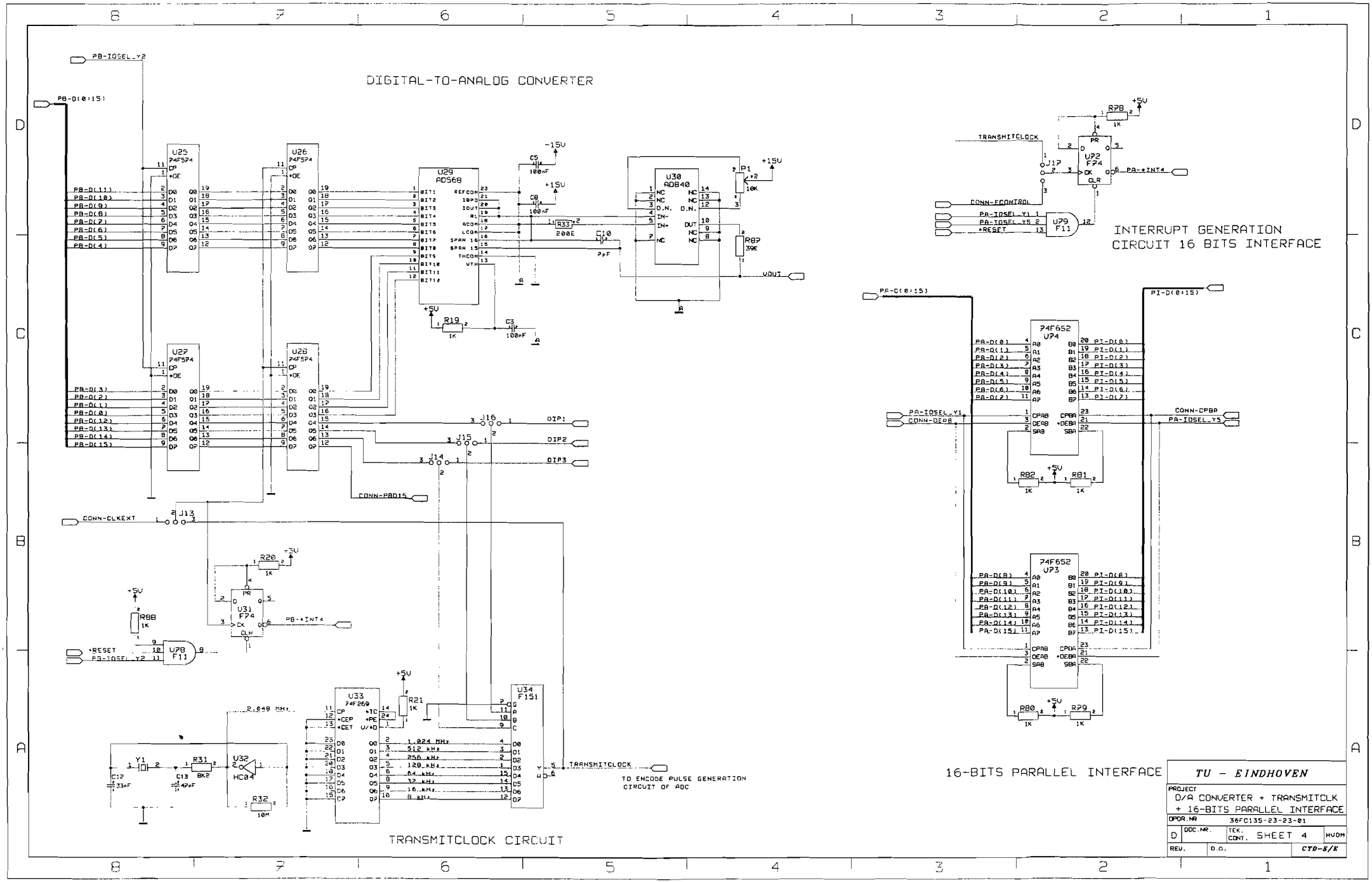


Figure A.1.5 The global memory and the communications interface.

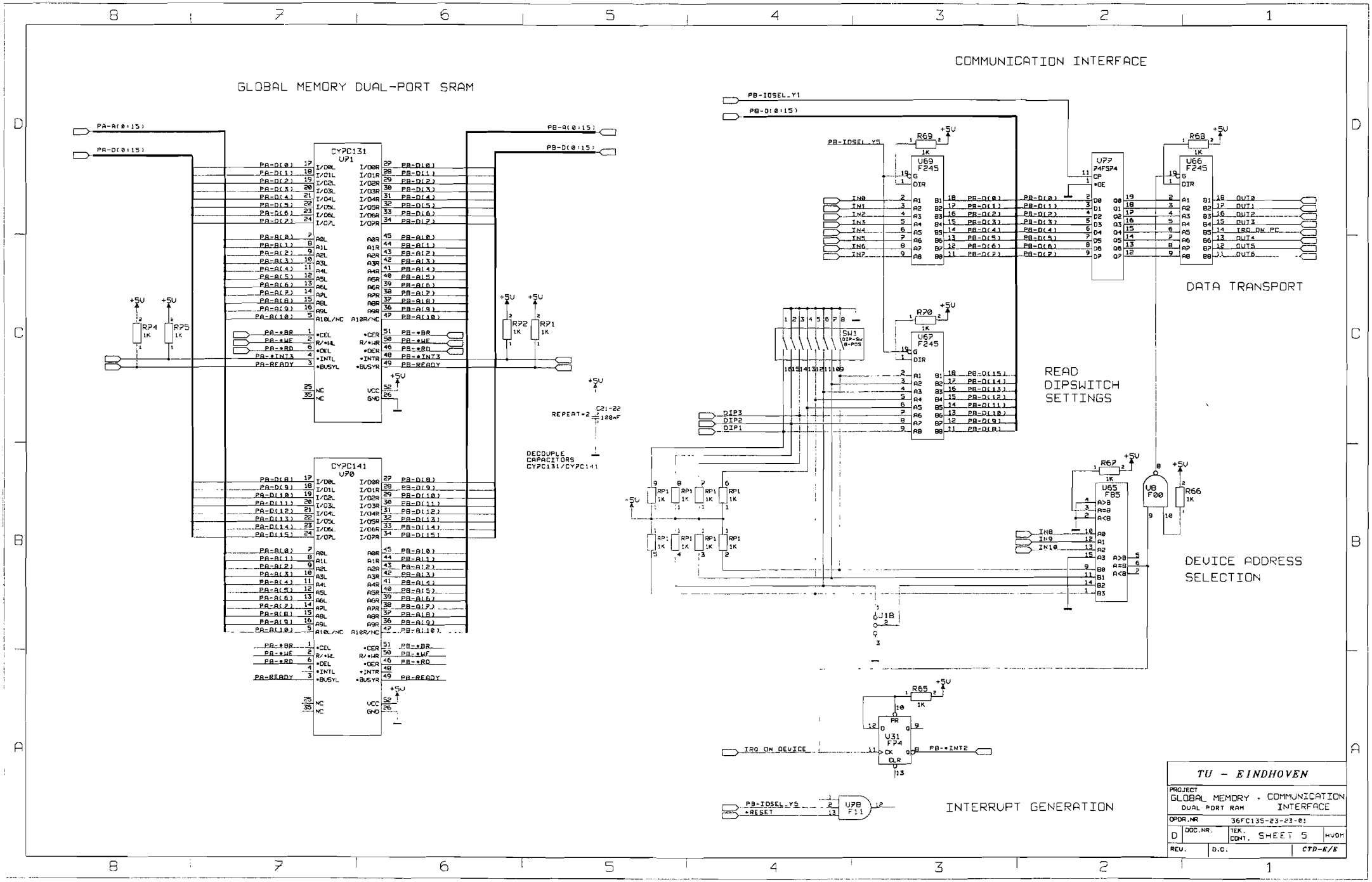


Figure A.1.6 The reset and oscillator circuit, the JTAG interface and the connectors.

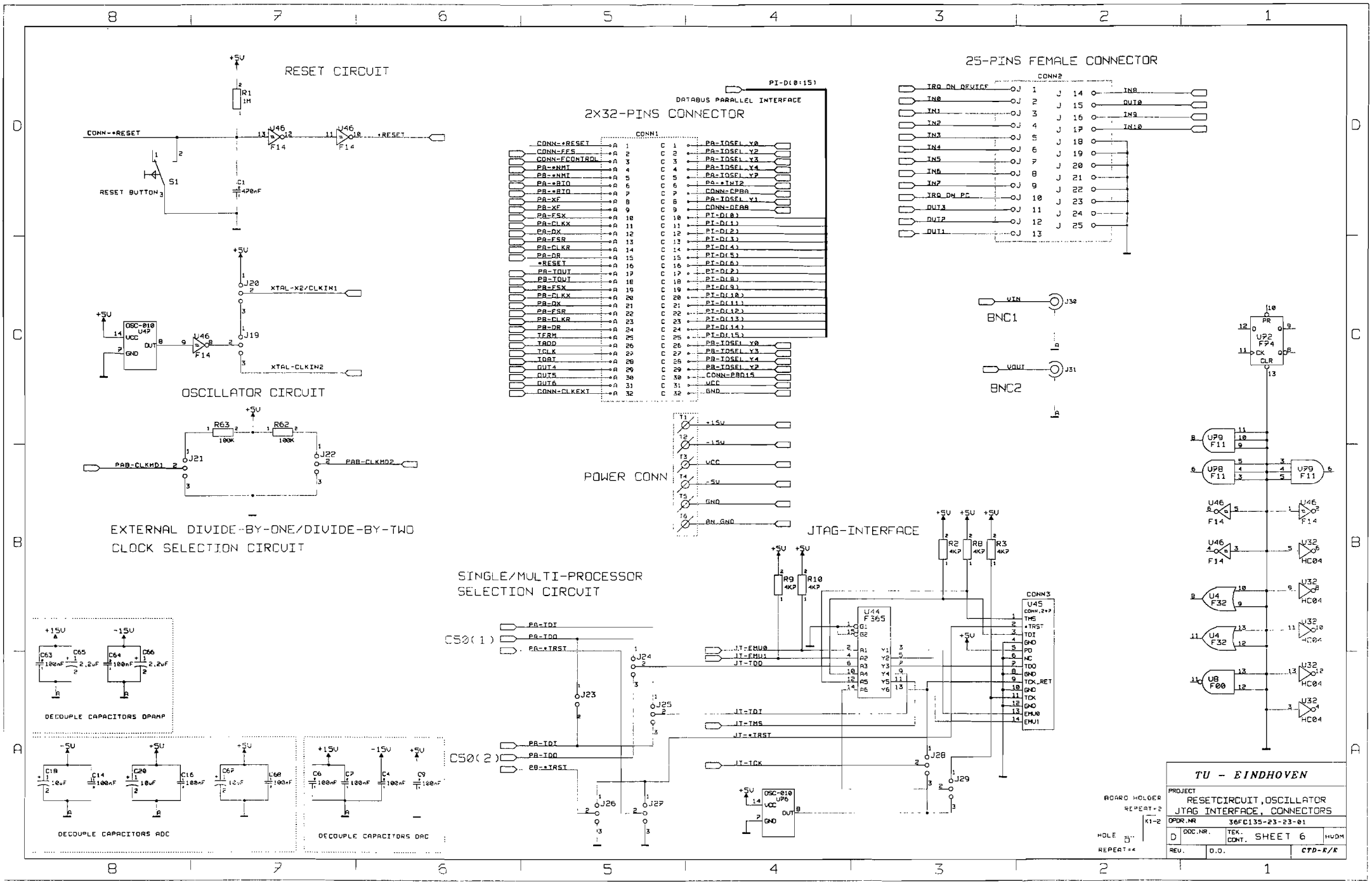
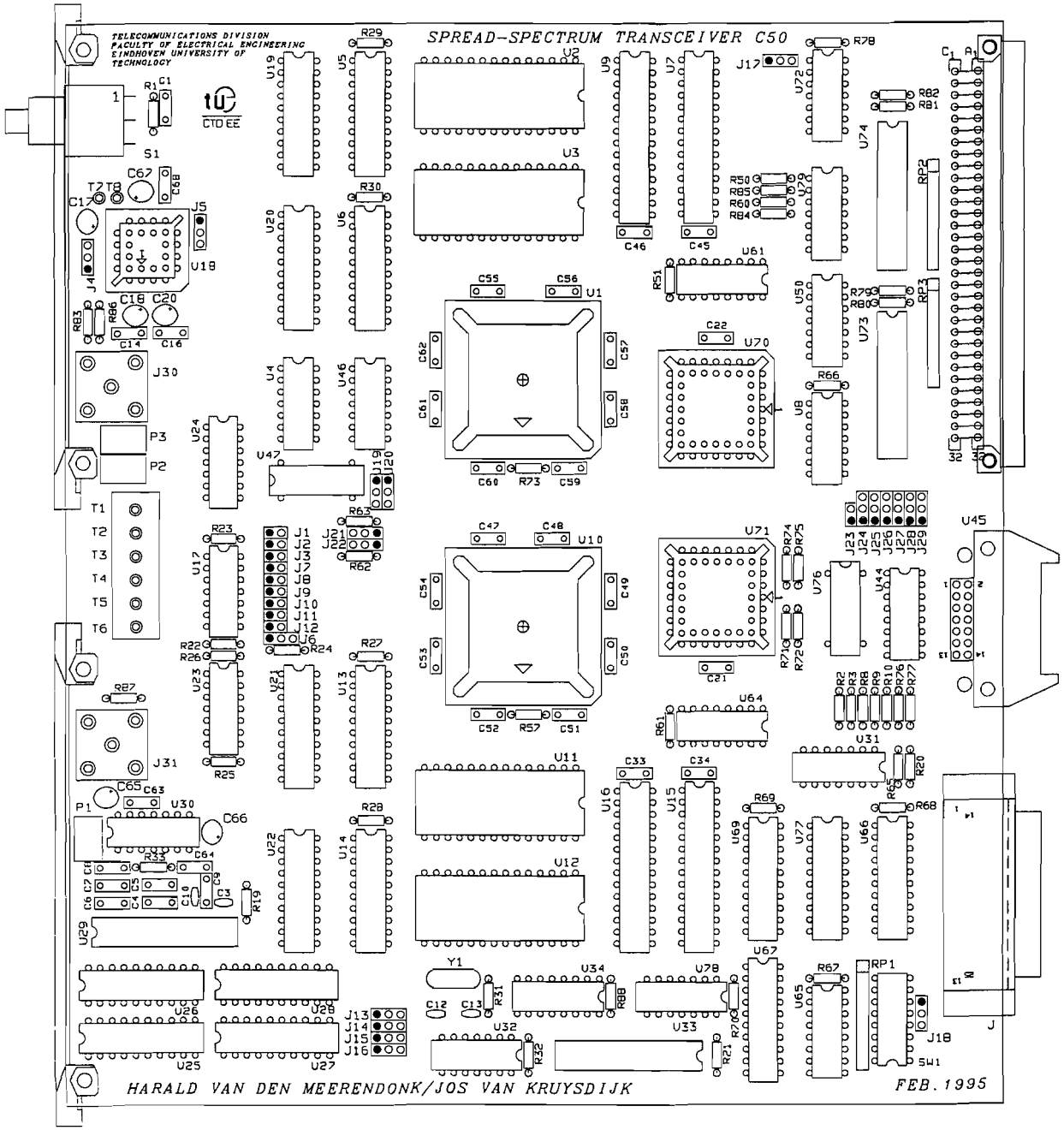
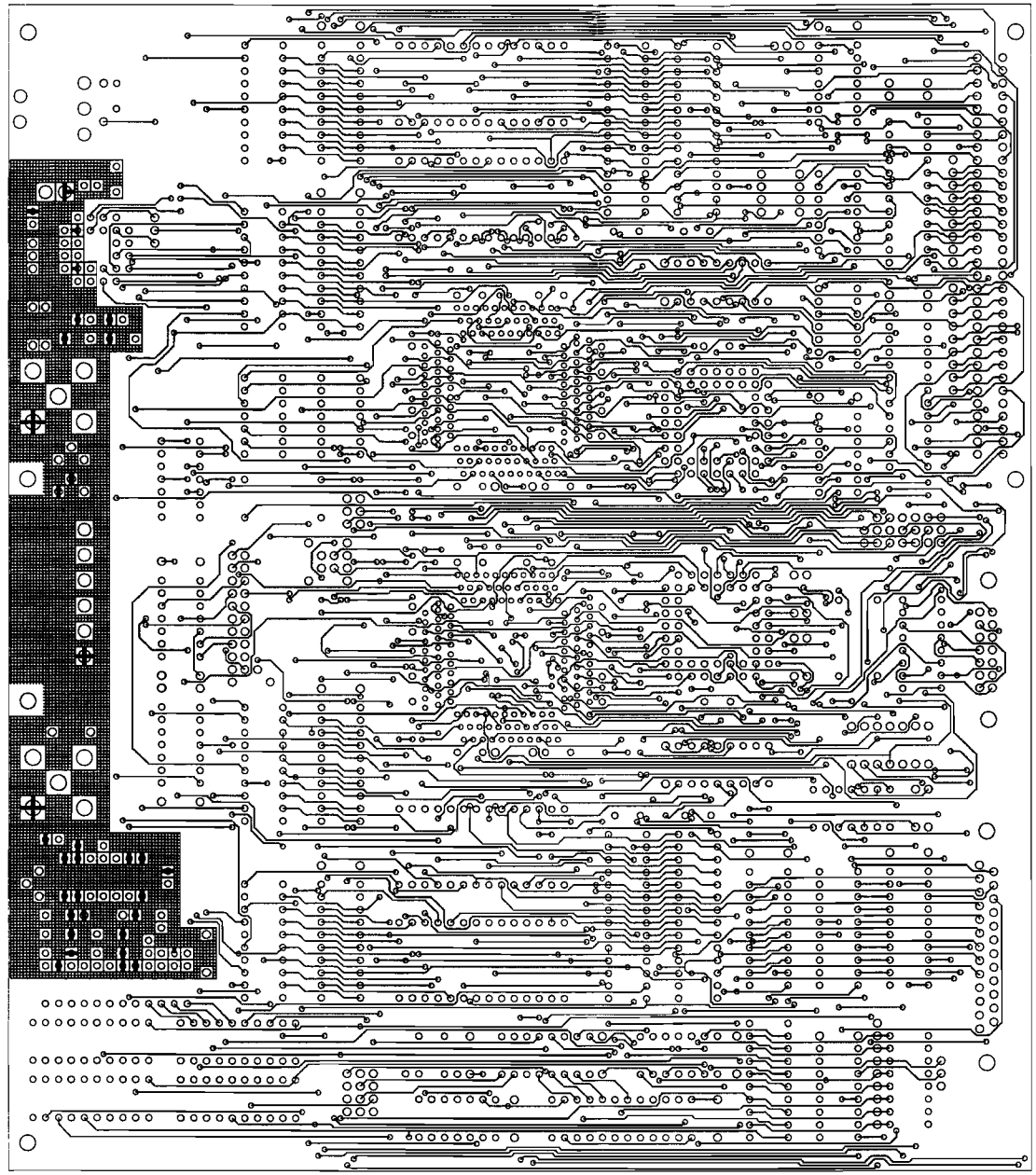


Figure A.1.7 Component placement of the transceiver.



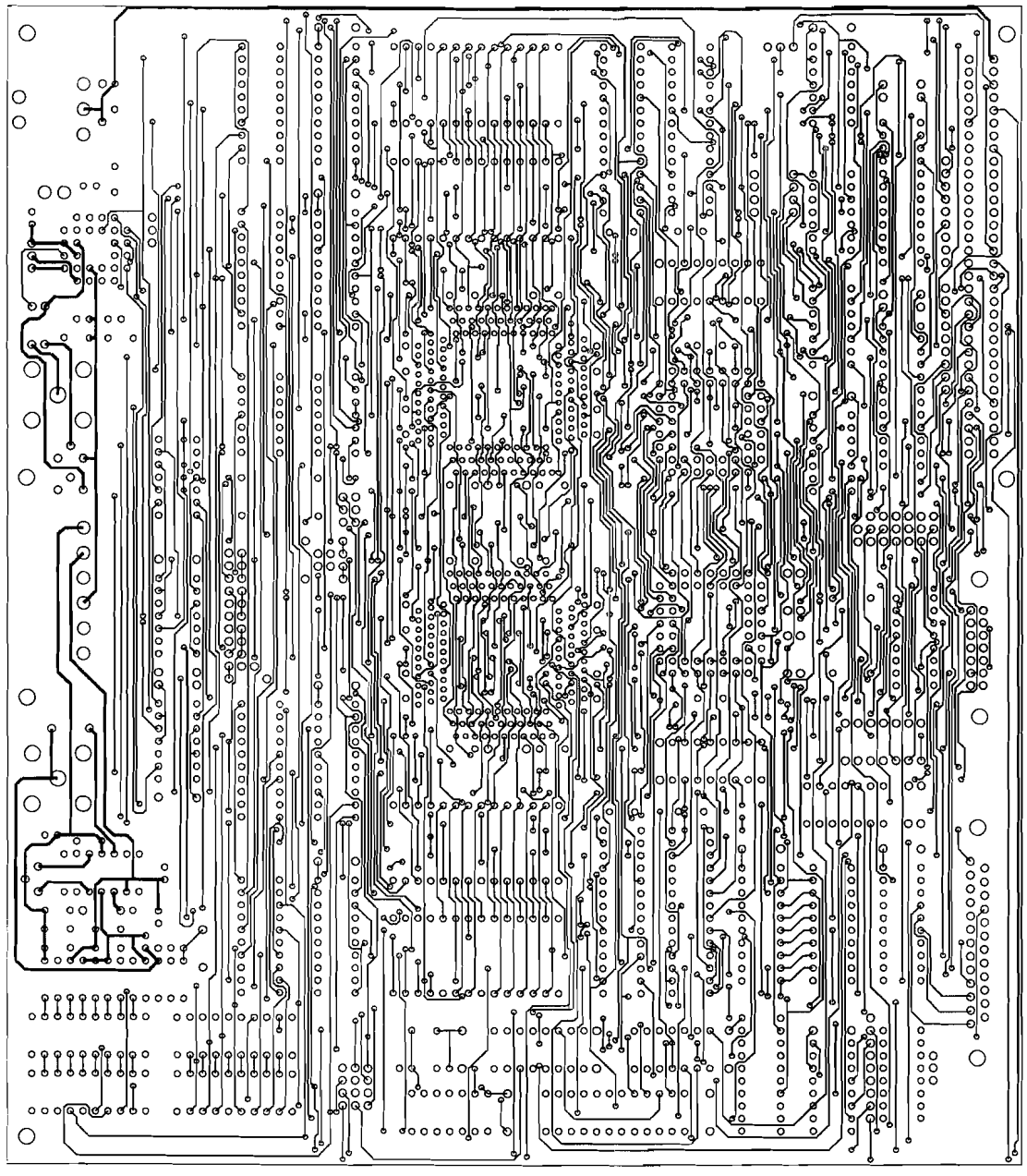
CTD EE	TU - EINDHOVEN CTD - E/E	PROJECT	TRANSCEIVER C50 COMPONENT PLACEMENT 4-LAYER MULTILAYER 233X200
A3	TEK. HVDM/JVK	OPDR.NR.	36FC/135/23/23/01
	CONT.	DATUM 15-2-1995	REV.

Figure A.1.8 The component-layer runs (trace layer 1).



tU CTD EE	TU - EINDHOVEN CTD - E/E	PROJECT	TRANSCEIVER CS0 TRACE LAYER 1
A3	TEK. JVK	OPDR.NR.	36FC/135/23/23/01
	CONT.	DATUM 15-2-1995	REV.

Figure A.1.9 The solder-layer runs (trace layer 4).



tu CTD EE	TU - EINDHOVEN CTD - E/E	PROJECT	TRANSCEIVER C50 TRACE LAYER 4
A3	TEK. HVDM/JVK	OPDR.NR.	36FC/135/23/23/01
	CONT.	DATUM 15-2-1995	REV.

Appendix 2: Jumper settings, connectors

Table A.1.1 Jumper settings for the modem.

J1 to J3 - jumper settings for the pulse generation circuit:

J1	J2	J3	Input clock
12	--	--	Sample frequency f_{fs} from frequency synthesizer
--	12	--	Transmit clock
--	--	12	Timer TMS320C50(1)

Note: For correct operation, either J1 or J2 or J3 is connected.

J4 - jumper setting for unipolar or bipolar mode of operation of the ADC:

Unipolar (0-5 V)	12
Bipolar (± 5V)	23

J5 - jumper for selection of the output data format of the ADC:

J5	*MSB/BIT1	Output data format
12	*MSB	twos complement range
23	BIT1	positive true binary range

J6 to J12 - jumpers for processor selection for receiving samples:

J6	J7	J8	J9	J10	J11	J12	Samples to :
23	12	--	--	12	--	--	TMS320C50(1)
12	--	12	--	--	12	--	TMS320C50(1) and TMS320C50(2)
23	--	--	12	--	--	12	TMS320C50(2)

J13 - jumper for selection of the transmit clock to control the DAC input buffers:

Internal transmit clock	23
External transmit clock	12

J14 to J16 - jumpers for selection of the internal transmit clock frequency:

Selection by DIP-switches 1 to 3	12
Selection by software	23

J17 - jumper for selection of the clock input to interrupt the TMS320C50 (parallel interface):

Transmit clock as clock input	12
Control frequency from connector as input	23

J18 - jumper for selection of the communications interface device:

Device number is set by DIP-switches 6 to 8	12
Device number is set by DIP-switches 7 and 8	23

J19 to J22 - jumpers for selection of the divide by one/divide by two processor clock:

J19	**J20**	**J21**	**J22**	**Clock Mode Selection**
12	23	23	23	External Divide-by-Two Clock Option; Internal oscillator disabled
12	23	12	12	External Divide-by-Two Clock Option; Internal oscillator enabled
23	12	12	23	External Divide-by-One Clock Option

J23 to J29 - jumpers for the JTAG-interface:

J23	J24	J25	J26	J27	J28	J29	Description
12	23	12	12	12	X	X	Multiprocessor-configuration
--	12	12	23	12	X	X	'C50-1 active, 'C50-2 inactive
--	23	23	12	23	X	X	'C50-1 inactive, 'C50-2 active
X	X	X	X	X	23	23	Use crystal for test clock
X	X	X	X	X	12	12	Use emulator (10 MHz) test clock

Note: - 12 = pins 1 and 2 of the jumper are connected
- 23 = pins 2 and 3 of the jumper are connected
- -- = no pins are connected
- X = don't care

JTAG connector (U4, CONN3)

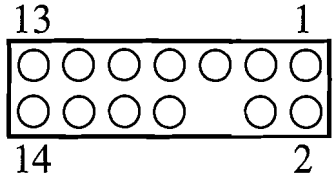


Table A.1.2 XDS510 Header Signals.

Pin	Signal	Function	Pin	Signal	Function
1	TMS	Input	8	GND	
2	*TRST	Input	9	TCK_RET	Output
3	TDI	Input	10	GND	
4	GND		11	TCK	Input
5	PD (+5V)	Output	12	GND	
6	No pin		13	EMU0	Input/Output
7	TDO	Output	14	EMU1	Input/Output

Power connector

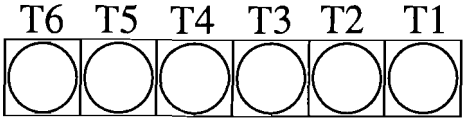


Table A.1.3 Power signals.

Pin	Signal	Pin	Signal
T1	+15 Volt	T4	-5 Volt
T2	-15 Volt	T5	Dig. Gnd
T3	+5 Volt	T6	An. Gnd

25-pins female Centronics connector

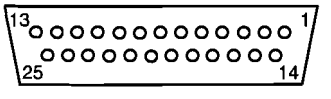


Table A.1.4 25-pins female Centronics connector.

Pin nr.	I/O	Function	Pin nr.	I/O	Function
1	Input	IRQ on device	10	Output	IRQ on PC
2	Input	IN0	11	Output	OUT3
3	Input	IN1	12	Output	OUT2
4	Input	IN2	13	Output	OUT1
5	Input	IN3	14	Input	Device select 0
6	Input	IN4	15	Output	OUT0
7	Input	IN5	16	Input	Device select 1
8	Input	IN6	17	Input	Device select 2
9	Input	IN7	18-25		Ground

2x32-pin connector CONN1

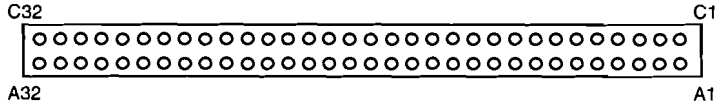


Table A.1.5: 2x32 pins CONN1-connector pin names.

Pin	Pin name	Function	Pin	Pin name	Function
A1	CONN-*RESET	Input for reset	C1	PA-IOSEL_Y0	Output
A2	CONN-FFS	Input sample freq.	C2	PA-IOSEL_Y2	Output
A3	CONN-FCONTROL	Input	C3	PA-IOSEL_Y3	Output
A4	PA-*NMI	Input	C4	PA-IOSEL_Y4	Output
A5	PB-*NMI	Input	C5	PA-IOSEL_Y7	Output
A6	PA-*BIO	Input	C6	PA-*INT2	Input
A7	PB-*BIO	Input	C7	CONN-CPBA	Par.Int Clock Input
A8	PA-XF	Output	C8	PA-IOSEL_Y1	Par.Int Output
A9	PB-XF	Output	C9	CONN-OEAB	Par.Int Input
A10	PA-FSX	Ser.Port	C10	PI-D(0)	Par.Int Databus
A11	PA-CLKX	Ser.Port	C11	PI-D(1)	Par.Int Databus
A12	PA-DX	Ser.Port	C12	PI-D(2)	Par.Int Databus
A13	PA-FSR	Ser.Port	C13	PI-D(3)	Par.Int Databus
A14	PA-CLKR	Ser.Port	C14	PI-D(4)	Par.Int Databus
A15	PA-DR	Ser.Port	C15	PI-D(5)	Par.Int Databus
A16	*RESET	Output	C16	PI-D(6)	Par.Int Databus
A17	PA-TOUT	Timer Output	C17	PI-D(7)	Par.Int Databus
A18	PB-TOUT	Timer Output	C18	PI-D(8)	Par.Int Databus
A19	PB-FSX	Ser.Port	C19	PI-D(9)	Par.Int Databus
A20	PB-CLKX	Ser.Port	C20	PI-D(10)	Par.Int Databus
A21	PB-DX	Ser.Port	C21	PI-D(11)	Par.Int Databus
A22	PB-FSR	Ser.Port	C22	PI-D(12)	Par.Int Databus
A23	PB-CLKR	Ser.Port	C23	PI-D(13)	Par.Int databus
A24	PB-DR	Ser.Port	C24	PI-D(14)	Par.Int Databus
A25	TFRM	TDM Ser.Port	C25	PI-D(15)	Par.Int Databus
A26	TADD	TDM Ser.Port	C26	PB-IOSEL_Y0	Output
A27	TCLK	TDM Ser.Port	C27	PB-IOSEL_Y3	Output
A28	TDAT	TDM Ser.Port	C28	PB-IOSEL_Y4	Output
A29	OUT4	Programm.	C29	PB-IOSEL_Y7	Output
A30	OUT5	Programm.	C30	CONN-PBD15	Programm. Output
A31	OUT6	Programm.	C31	VCC	+5V Output
A32	CONN-CLKEXT	Ext.Clock	C32	GND	Dig Gnd Output

Appendix 3: List of the components used

Quantity	Part Name	Part Description	Reference Designator
2	TMS320C50	Digital Signal Processor	U1, U10
4	AM27C256	32Kx8 UV Erasable CMOS PROM	U2, U3, U11, U12
1	74F32	Quad Two-Input OR Gate	U4
7	74F245	Octal Transceiver (3-State)	U5, U6, U13, U14, U66, U67, U69
4	CY7C199	32K x 8 Static RAM	U7, U9, U15, U16
1	74F00	Quad Two-Input Nand Gate	U8
4	74F74	Dual D-Type Flip-Flop	U17, U23, U31, U72
1	AD1671	Analog-to-Digital Converter	U18
9	74F574	Octal D Flip-Flop (3-State)	U19-U22, U25-U28, U77
2	74F08	Quad Two-Input And Gate	U24, U50
1	AD568	Digital-to-Analog Converter	U29
1	AD840	Opamp	U30
1	74HC04	Hex Inverter	U32
1	74F269	8-Bit Bidirectional Binary Counter	U33
1	74F151A	8-Input Multiplexer	U34
1	74F365	Hex Buffer/Driver (3-State)	U44
1	74F14	Hex Inverter Schmitt Trigger	U46
2	SG51/KT	Crystal Oscillator 50 MHz	U47, U76
2	74F138	1-Of-8 Decoder/Demultiplexer	U61, U64
1	74F85	4-Bit Magnitude Comparator	U65
1	CY7C141	1Kx8 Dual-Port Static RAM slave	U70
1	CY7C131	1Kx8 Dual-Port Static RAM master	U71
2	74F652	Octal Transceiver/Register, Non-Inverting	U73, U74
2	74F11	Triple Three-Input And Gate	U78, U79

Quantity	Part Description	Reference Designator
1	Resistor 1/4W 1M	R1
5	Resistor 1/4W 4K7	R2, R3, R8-R10
34	Resistor 1/4W 1K	R19-R30, R50, R51, R60, R61, R65-R72, R74, R75, R78-R82, R84, R85, R88
1	Resistor 1/4W 8K2	R31
1	Resistor 1/4W 10M	R32
1	Resistor 1/4W 200	R33
6	Resistor 1/4W 100K	R57, R62, R63, R73, R76, R77
1	Resistor 1/4W 24,9	R83
1	Resistor 1/4W 51K	R86
1	Resistor Pack 1K	RP1
2	Resistor Pack 100K	RP2, RP3
1	Resistor 1/4W 39	R87
1	Electrolytic Capacitor 0.47 µF	C1
1	Ceramic Capacitor 100 pF	C3
33	Ceramic Capacitor 0.1 µF	C4-C9, C14, C16, C21, C22, C33, C34, C45-C64, C68
1	Ceramic Capacitor 6.8 pF	C10
1	Ceramic Capacitor 33 pF	C12
1	Ceramic Capacitor 47 pF	C13
1	Tantalum Capacitor 1 µF	C17
3	Tantalum Capacitor 10 µF	C18, C20, C67
2	Tantalum Capacitor 2.2 µF	C65, C66

Quantity	Part Description	Reference Designator
1	2.048 MHz Crystal	Y1
2	Potmeter 10K	P1, P3
1	Potmeter 50	P2
1	Reset Button	S1
1	8 position Dip-Switch	SW1
10	2-pin Jumper	J1-J3, J7-J12, J23
19	3-pin Jumper	J4-J6, J13-J22, J24-J29
2	BNC Connector	J30, J31
1	25-pin D-Connector Female	J
1	2x32-pin Din Connector Male	A, C
1	14-pin Flatcable Connector, Male	U45
1	6-pin Power Connector	T1-T6
2	External Pins	T7, T8
2	DIP IC socket 4-pin, 300 mil, 0.1 µF Decoupling Capacitor	U47, U76
12	DIP IC socket 14-pin, 300 mil, 0.1 µF Decoupling Capacitor	U4, U8, U17, U23, U24, U31, U32, U46, U50, U72, U78, U79
1	DIP IC socket 14-pin, 300 mil, No Decoupling Capacitor	U30
5	DIP IC socket 16-pin, 300 mil, 0.1 µF Decoupling Capacitor	U34, U44, U61, U64, U65
16	DIP IC socket 20-pin, 300 mil, 0.1 µF Decoupling Capacitor	U5, U6, U13, U14, U19-U22, U25-U28, U66, U67, U69, U77
3	DIP IC socket 24-pin, 300 mil, 0.1 µF Decoupling Capacitor	U33, U73, U74
1	DIP IC socket 24-pin, 300 mil, No Decoupling Capacitor	U29

Quantity	Part Description	Reference Designator
4	DIP IC socket 28-pin, 300 mil, No Decoupling Capacitor	U7, U9, U15, U16
4	DIP IC socket 28-pin, 600 mil, 0.1 μF Decoupling Capacitor	U2, U3, U11, U12
1	PLCC IC socket 28-pin	U18
2	PLCC IC socket 52-pin	U70, U71
2	PQFP IC socket 132-pin	U1, U10

Appendix 4: Data sheets of the components used

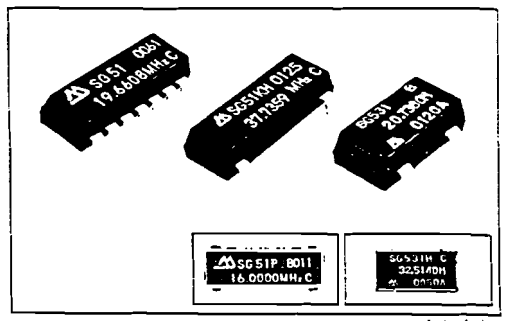
This appendix comprises the data sheets of the most important components used. These components are:

FULL SIZE DIP HIGH FREQUENCY CRYSTAL OSCILLATOR

SG-51 series

HALF SIZE DIP HIGH FREQUENCY CRYSTAL OSCILLATOR

SG-531 series



Actual size

■Specifications (characteristics)

Item		Symbol	SG-51/51K/51P/51E, SG-531/531P	SG-51T/51KT/51PT, SG-531T/531PT	SG-51KT/51PT, SG-531T/531PT	Remarks
			Specifications			
Output frequency range		fo	1.0250MHz to 26.0000MHz	26.0001MHz to 36.0000MHz	36.0001MHz to 50.3500MHz	
Power source voltage	MAX. supply voltage	V_{DD}-GND	−0.3V to −7.0V	−0.3V to +7.0V	−0.3V to +7.0V	
	Operating voltage	V_{DD}	5.0V±0.5V	5.0V±0.5V	5.0V±0.5V	
Temperature range	Storage temp.	T_{STG}	−55°C to +125°C	−55°C to +100°C	−55°C to +100°C	
	Operating temp.	T_{OPR}	−10°C to −70°C	−10°C to −70°C	−10°C to +70°C	
Soldering condition (lead part)		T_{SOL}	Under 260°C within 10 sec.	Under 260°C within 10 sec.	Under 260°C within 10 sec.	Package less than 150°C
Frequency stability		Δf/fo	B : ± 50ppm, C : ±100ppm	B : ± 50ppm, C : ±100ppm	B : ± 50ppm, C : ±100ppm	−10°C to +70°C
Current consumption		Iop	25mA MAX.	35mA MAX.	50mA MAX.	No load condition
Duty		Tw/T	40% to 60% * (45% to 55% *1)	40% to 60% ** (45% to 55% *1)	40% to 60% **	* : 1.4V or 1/2 V_{DD} level ** : 1.4V level
Output voltage		V_{OH}	V_{DD}−0.4V MIN.	V_{DD}−0.4V MIN.	2.4V MIN.	I_{OH} = −400μA
		V_{OL}	0.4V MAX. *	0.4V MAX. *	0.4V MAX. **	*: I_{OL} = 16mA, **: I_{OL} = 8mA
Output load condition (fan out)	TTL	N	10 TTL MAX.	10 TTL (30pF) MAX.	5 TTL (15pF) MAX.	
	C-MOS	CL	50pF MAX.			
Output enable/standby input voltage		V_{IH}	2.0V MIN.	2.0V MIN.	2.0V MIN.	
		V_{IL}	0.8V MAX.	0.8V MAX.	0.8V MAX.	
Output disable current		I_{OT}	12mA MAX.	20mA MAX.	25mA MAX.	$\overline{OE}$ = GND
Standby current		I_{ST}	310μA MAX.			$\overline{ST}$ = GND
Output rise time		t_{TLH}	8nsec. MAX.	10nsec. MAX.	6nsec. MAX.	Refer to output waveform chart (page 9)
Output fall time		t_{THL}	8nsec. MAX.	8nsec. MAX.	6nsec. MAX.	
Oscillation start time		t_{OSC}	4msec. MAX.	10msec. MAX.	10msec. MAX.	More than for 1ms until V_{DD}=0V→4.5V Time at 4.5V to be 0sec.
Aging		fa	±5ppm/year MAX.	±5ppm/year MAX.	±5ppm/year MAX.	Ta=25°C, V_{DD}=5V, first year
Shock resistance		S. R.	±20ppm MAX.	±20ppm MAX.	±20ppm MAX.	Drop test of 3 times on a hard board from 75cm height or excitation test with 3000G×0.3ms×1/2 sine wave in 3 directions.

Note: · Unless otherwise stated, characteristics (specifications) shown in the above table are based on the rated operating temperature and voltage condition.
· External by-pass capacitor is recommended.

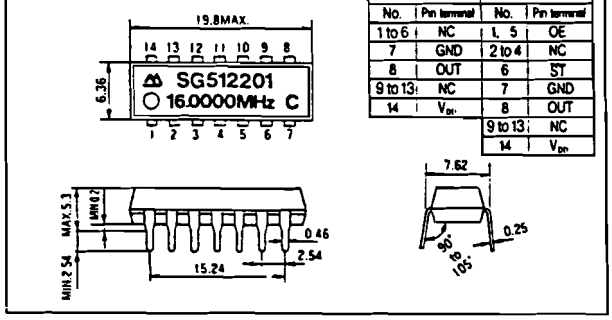
■Frequency correspondence table

Model \ Frequency	1MHz	26MHz	50MHz	66.67MHz
SG-51/51K/51E,SG-531/531P	▼	▼	▼	▼
SG-51T/51KT/51ET,SG-531T/531PT	▼	▼	▼	▼ (SG-51T: Up to 36MHz)
SG-51PH/51YH,SG-531PH/531YH	▼	▼	▼	▼

■External Dimensions

(Unit : mm)

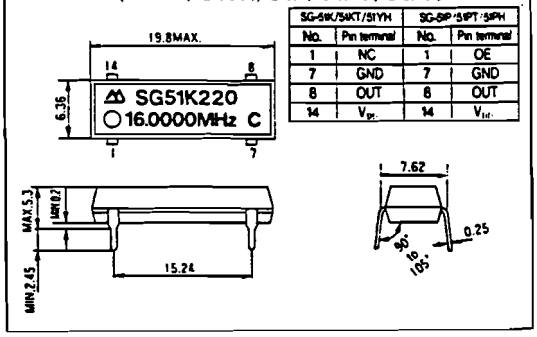
● SG-51/51T/51E



SG-51/51T		SG-51E	
No.	Pin terminal	No.	Pin terminal
1 to 6	NC	1, 5	OE
7	GND	2 to 4	NC
8	OUT	6	ST
9 to 13	NC	7	GND
14	V_{DD}	8	OUT
		9 to 13	NC
		14	V_{DD}

(Unit : mm)

● SG-51K/51KT/51YH/51P/51PT/51PH



SG-51K/51KT/51YH		SG-51P/51PT/51PH	
No.	Pin terminal	No.	Pin terminal
1	NC	1	OE
7	GND	7	GND
8	OUT	8	OUT
14	V_{DD}	14	V_{DD}

■Features

SG-51 series

- Pin compatible with full size metal can
- Packaged in plastic 14 pin DIP
- Auto insertable
- Provided with output enable and standby functions

SG-531 series

- Pin compatible with half size metal can
- Provided with output enable function

Common

- Cylindrical type AT cut quartz crystal built-in, thus assuring high reliability
- Possible with 386 CPU
- Use of C-MOS IC enables reduction of current consumption

* Item		Symbol	SG-51PH/51YH,SG-531PH/531YH	
			Specifications	Remarks
Output frequency range		fo	26.0001MHz to 66.6667MHz	
Power source voltage	MAX. supply voltage	V_{DD}-GND	−0.3V to +7.0V	
	Operating voltage	V_{DD}	5.0V ±0.5V ※2	
Temperature range	Storage temperature	T_{STG}	−55°C to +100°C	
	Operating temperature	T_{OPR}	−10°C to +70°C	
Soldering condition (lead part)		T_{SOL}	Under 260°C within 10sec	Package less than 150°C
Frequency stability		Δf/fo	(B: ±50ppm)C ±100ppm	−10°C to −70°C. B type is possible up to 55MHz. please consult us.
Current consumption		Iop	35mA MAX.	No load condition Up to 45MHz : 21mA MAX.
Duty		Tw/T	40% to 60%	1/2 V_{DD} level
Output voltage		V_{OH}	V_{DD} −0.4V MIN.	I_{OH} = −4mA
		V_{OL}	0.4V MAX.	I_{OL} =4mA
Output load condition(Fan out)	TTL	N		
	C-MOS	CL	50pF MAX.	
Output enable/standby input voltage		V_{IH}	2.0V MIN.	
		V_{IL}	0.8V MAX.	
Output disable current		I_{OE}	20mA MAX.	OE=GND. Up to 45MHz : 15mA MAX.
Standby current		I_{ST}		
Output rise time		t_{TLH}	7nsec.MAX. ※2	Over 45MHz : 5ns. MAX. Refer to output waveform chart (page 9)
Output fall time		t_{THL}	7nsec.MAX. ※2	
Oscillation start time		t_{osc}	10msec.MAX.	More than for 1ms until V_{EO}=0V−4.5V Time at 4.5V to be 0sec.
Aging		fa	±5ppm/year MAX.	Ta=25°C V_{DD}=5V. first year
Shock resistance		S.R.	±20ppm MAX.	Drop test of 3 times on a hard board from 75cm height or excitation test with 3000G×0.3ms×1/2 sine wave in 3 directions in 3directions

※1 It is possible depending on condition, reference data (page 24).

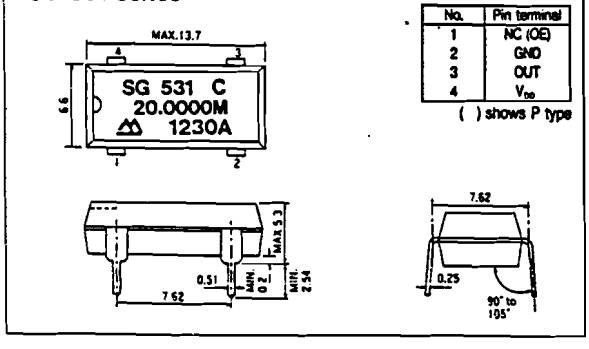
※2 AC characteristics of 386 CPU. (V_{DD}=5V ±0.25V, Load : CL≦50pF, Ta=−10 to +70°C, Refer to output waveform chart of 386 CPU).

Output frequency		26.001MHz to 36.000MHz		40.000MHz		45.000MHz to 50.000MHz		50.001MHz to 66.667MHz		Unit	Remarks
Item	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
CLK high time	t2a	9		8		7		6.25		ns	2V level
CLK high time	t2b	5		5		4		4.5		ns	Under 45MHz : V_{IH} −0.8V level Over 45MHz : 3.7V level
CLK low time	t3a	9		8		7		6.25		ns	2V level
CLK low time	t3b	7		6		5		4.5		ns	2v level
CLK fall time	t4		8		8		7		4	ns	Under 45MHz : V_{DD} −0.8V to 0.8V Over 45MHz : 3.7V to 0.8V
CLK rise time	t5		9		9		7		4	ns	Under 45MHz : V_{IH} 0.8V to V_{DD} −0.8V Over 45MHz : 0.8V to 3.7V

■External Dimensions

(Unit : mm)

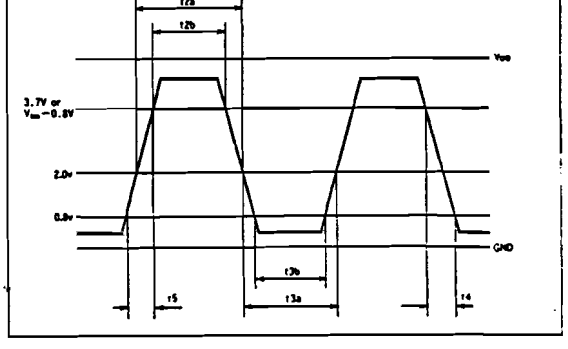
● SG-531 series



No.	Pin terminal
1	NC (OE)
2	GND
3	OUT
4	V_{DD}

( ) shows P type

■Waveform Chart of 386 CPU



CYPRESS SEMICONDUCTOR

CY7C199

32K x 8 Static RAM

Features

- High speed
  — 12 ns
- Fast t_{DOE}
- CMOS for optimum speed/power
- Low active power
  — 880 mW
- Low standby power
  — 165 mW
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

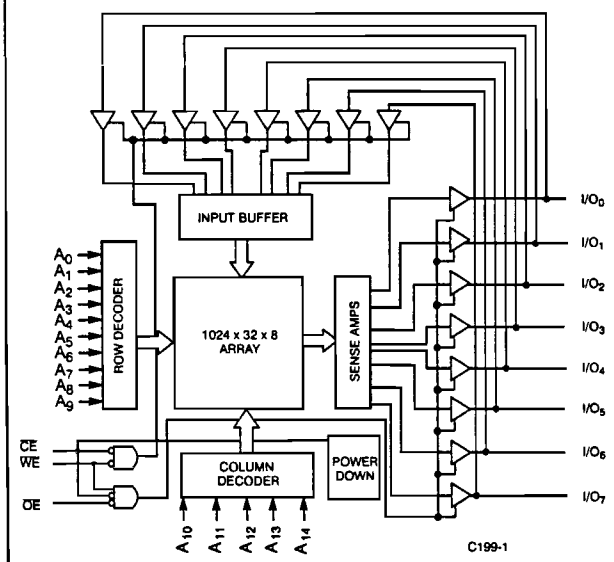
Functional Description

The CY7C199 is a high-performance CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and three-state drivers. This device has an automatic power-down feature, reducing the power consumption by 81% when deselected. The CY7C199 is in the standard 300-mil-wide DIP, SOJ and LCC packages.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

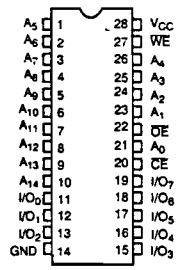
The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH. A die coat is used to ensure alpha immunity.

Logic Block Diagram



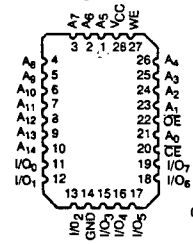
Pin Configurations

DIP/SOJ
Top View



C199-2

LCC
Top View



C199-3

Selection Guide

		7C199-12	7C199-15	7C199-20	7C199-25	7C199-35	7C199-45
Maximum Access Time (ns)		12	15	20	25	35	45
Maximum Operating Current (mA)	Commercial	160	155	150	150	140	
	Military		180	170	150	150	150
Maximum Standby Current (mA)		30	30	30	30	25	25

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... – 0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... – 0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[2]	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C199–12 Min.	7C199–12 Max.	7C199–15 Min.	7C199–15 Max.	7C199–20 Min.	7C199–20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage			–0.5	0.8	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–5	+5	–5	+5	–5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–5	+5	–5	+5	–5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			–300		–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{RC}	Com'l		160		155		150	mA
			Mil				180		170	
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			30		30		30	mA
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = 0	Com'l		10		10		15	mA
			Mil				15		15	

Shaded area contains preliminary information.

Notes:

1. $V_{IL(min.)}$ = –2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range[3] (continued)

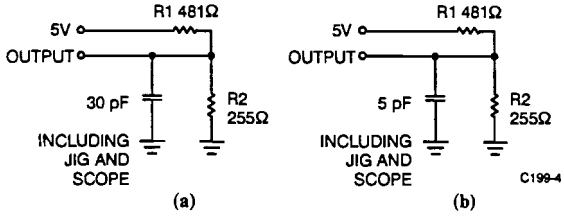
Parameter	Description	Test Conditions		7C199-25 Min.	7C199-25 Max.	7C199-35, 45 Min.	7C199-35, 45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		150		140	mA
			Mil		150		150	
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			30		25	mA
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f=0			15		15	mA

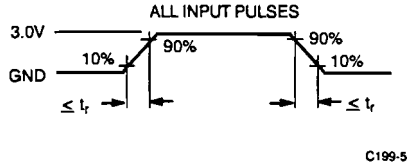
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		8	pF

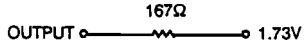
Note:
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[6]





Equivalent to: THÉVENIN EQUIVALENT



Note:
6. t_r ≤ 3 ns for the −12 and −15 speeds. t_r ≤ 5 ns for the −20 and slower speeds.

Switching Characteristics Over the Operating Range[3, 7]

Parameter	Description	7C199–12		7C199–15		7C199–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address to Data Valid		12		15		20	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		7		9	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[8]	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8, 9]		5		7		9	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]		5		7		9	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20	ns
WRITE CYCLE[10, 11]								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	9		10		15		ns
t_{AW}	Address Set-Up to Write End	9		10		15		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		9		15		ns
t_{SD}	Data Set-Up to Write End	8		9		10		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[9]		7		7		10	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	3		3		3		ns

Shaded area contains preliminary information.

Notes:

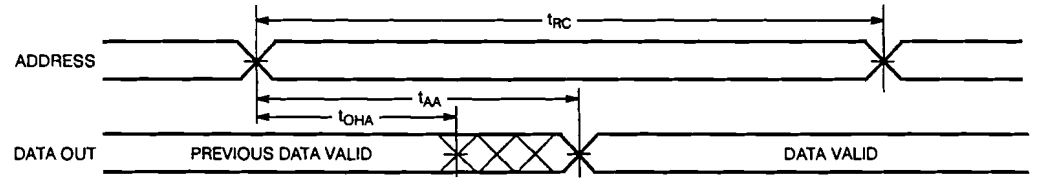
7. Test conditions assume signal transition time of 3 ns or less for −12 and −15 speeds and 5 ns or less for −20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled. $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Characteristics Over the Operating Range[3, 7] (continued)

Parameter	Description	7C199–25		7C199–35		7C199–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		16		16	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[8]	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8, 9]		11		15		15	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]		11		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		20		20		25	ns
WRITE CYCLE[10, 11]								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	18		22		22		ns
t_{AW}	Address Set-Up to Write End	20		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	18		22		22		ns
t_{SD}	Data Set-Up to Write End	10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[9]		11		15		15	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	3		3		3		ns

Switching Waveforms

Read Cycle No. 1[12, 13]

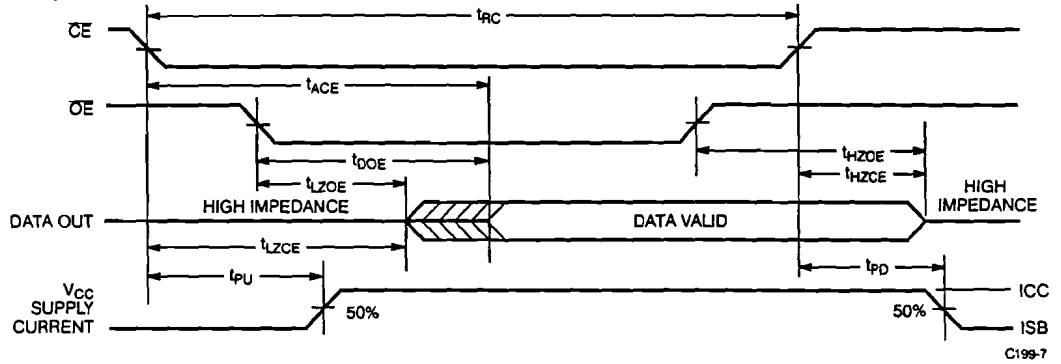


C199-6

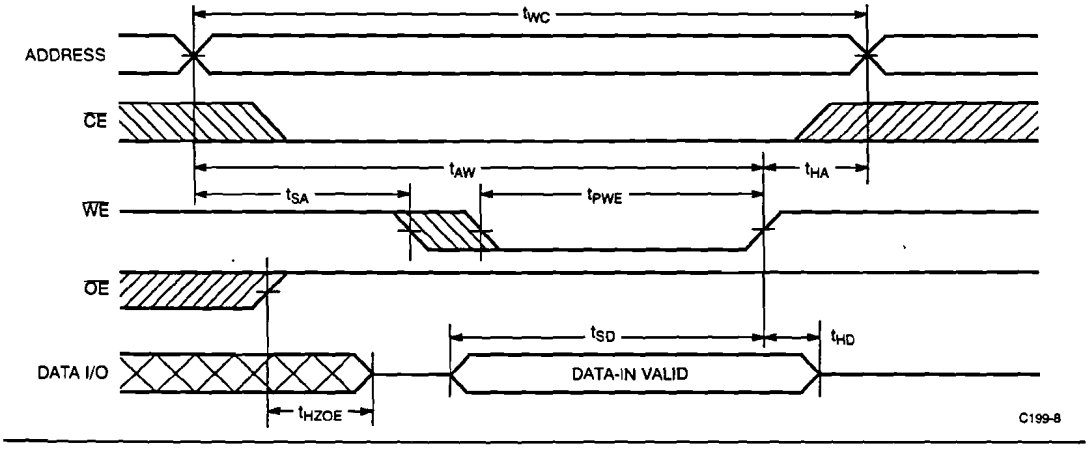
Notes:
12. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

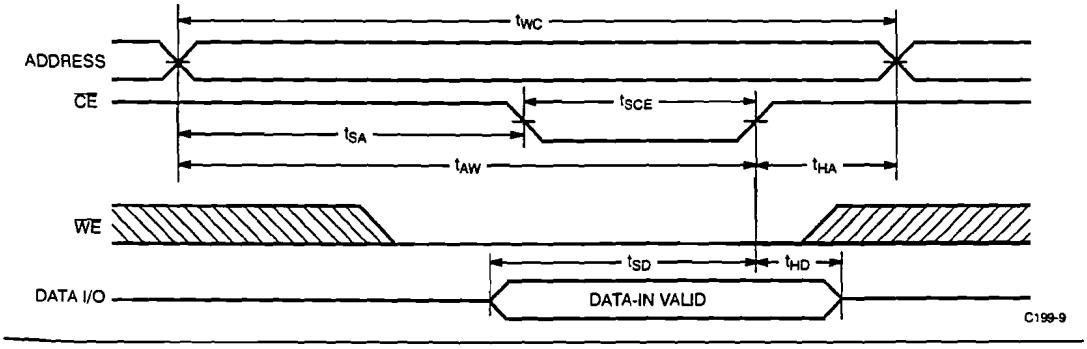
Read Cycle No. 2[13, 14]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[10, 15, 16]



Write Cycle No. 2 ($\overline{CE}$ Controlled)[10, 15, 16]

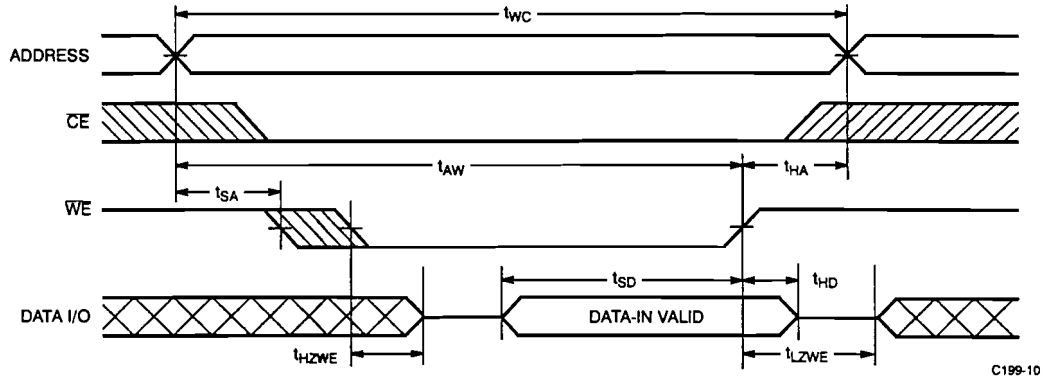


Notes:

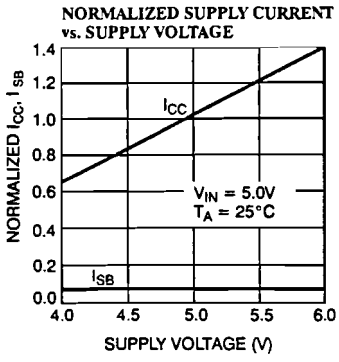
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
15. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

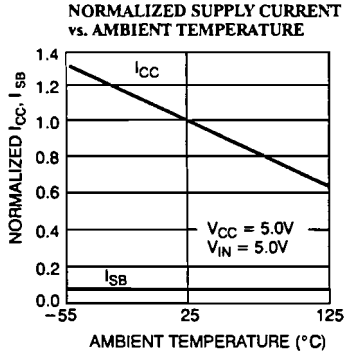
Switching Waveforms (continued)

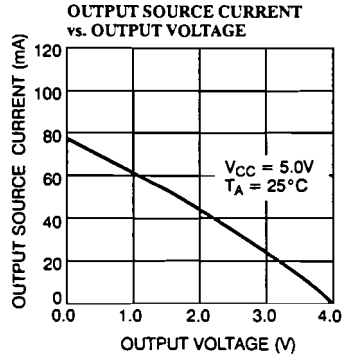
Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[11, 16]

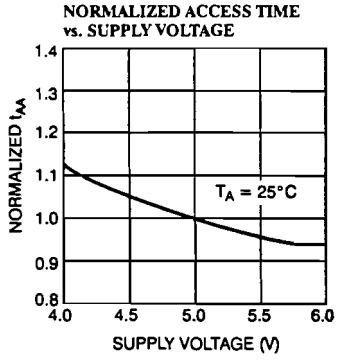


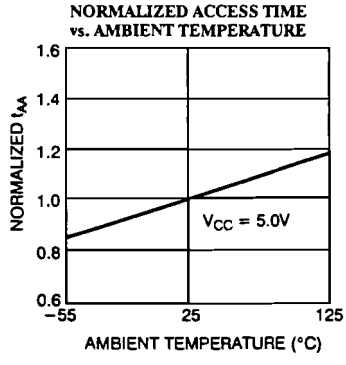
Typical DC and AC Characteristics

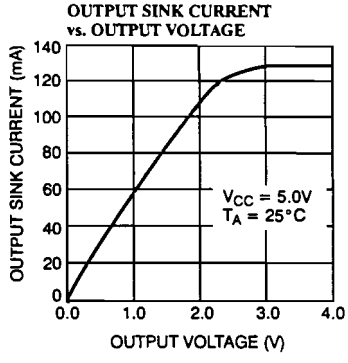






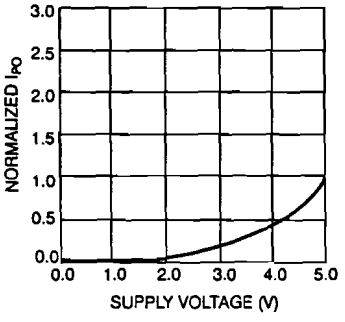




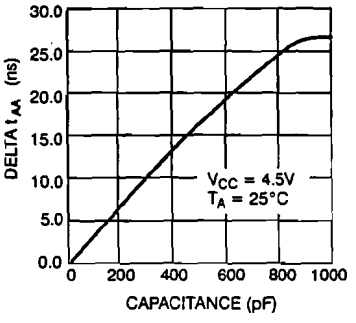


Typical DC and AC Characteristics (continued)

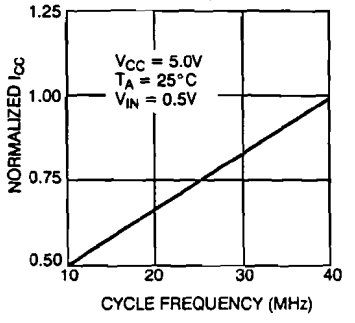
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C199-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199-12VC	V21	28-Lead Molded SOJ	
15	CY7C199-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199-15VC	V21	28-Lead Molded SOJ	
	CY7C199-15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
20	CY7C199-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199-20VC	V21	28-Lead Molded SOJ	
	CY7C199-20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199-20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
25	CY7C199-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199-25VC	V21	28-Lead Molded SOJ	
	CY7C199-25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199-25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C199-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199-35VC	V21	28-Lead Molded SOJ	
	CY7C199-35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199-35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
45	CY7C199-45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199-45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains preliminary information.

CY7C130/CY7C131
CY7C140/CY7C141

CYPRESS SEMICONDUCTOR

1K x 8 Dual-Port Static RAM

Features

- **0.8-micron CMOS for optimum speed/power**
- **Automatic power-down**
- **TTL compatible**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **Fully asynchronous operation**
- **Master CY7C130/CY7C131 easily expands data bus width to 16 or more bits using SLAVE CY7C140/CY7C141**
- **$\overline{BUSY}$ output flag on CY7C130/CY7C131; $\overline{BUSY}$ input on CY7C140/CY7C141**
- **$\overline{INT}$ flag for port-to-port communication**

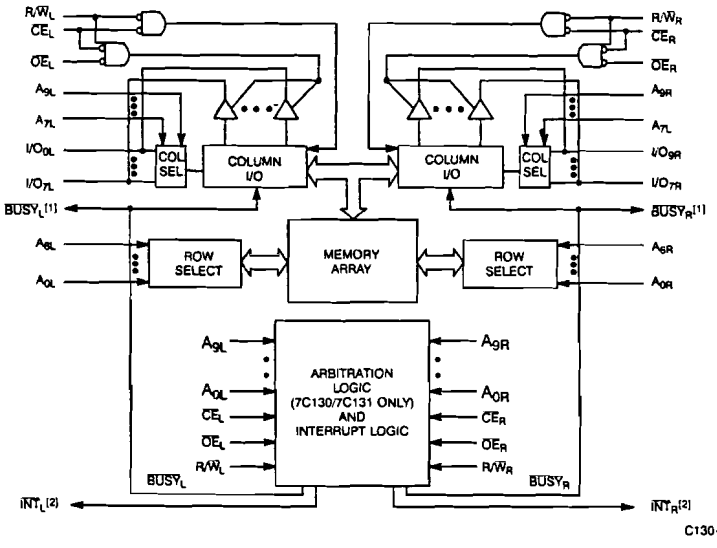
Functional Description

The CY7C130/CY7C131/CY7C140/CY7C141 are high-speed CMOS 1K by 8 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C130/CY7C131 can be utilized as either a standalone 8-bit dual-port static RAM or as a master dual-port RAM in conjunction with the CY7C140/CY7C141 slave dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ($\overline{CE}$), write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). Two flags are provided on each port, $\overline{BUSY}$ and $\overline{INT}$. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. $\overline{INT}$ is an interrupt flag indicating that data has been placed in a unique location (3FF for the left port and 3FE for the right port). An automatic power-down feature is controlled independently on each port by the chip enable ($\overline{CE}$) pins.

The CY7C130 and CY7C140 are available in both 48-pin DIP and 48-pin LCC. The CY7C131 and CY7C141 are available in both 52-pin LCC and PLCC.

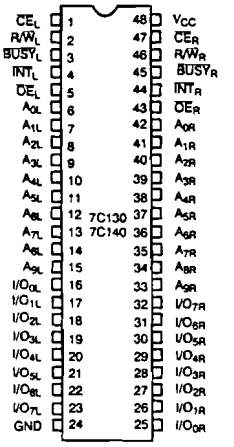
Logic Block Diagram



C130-1

Pin Configurations

DIP
Top View

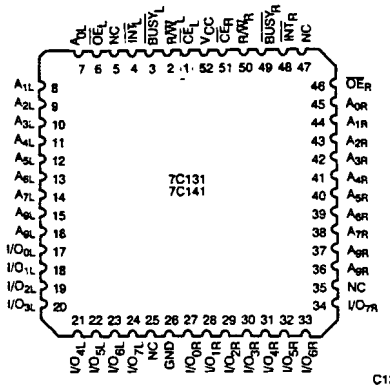


C130-2

Notes:
1. CY7C130/CY7C131 (Master): $\overline{BUSY}$ is open drain output and requires pull-up resistor. CY7C140/CY7C141 (Slave): $\overline{BUSY}$ is input.
2. Open drain outputs: pull-up resistor required.

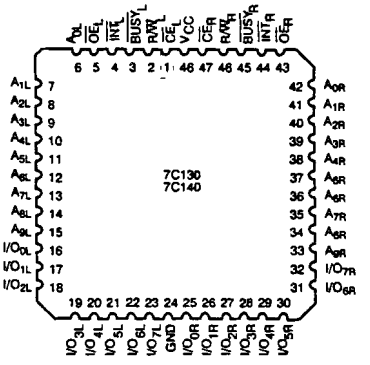
Pin Configurations (continued)

52-Pin LCC/PLCC
Top View



C130-3

48-Pin LCC/QFP
Top View



C130-4

Selection Guide

		7C130-25[3] 7C131-25 7C140-25 7C141-25	7C130-30 7C131-30 7C140-30 7C141-30	7C130-35 7C131-35 7C140-35 7C141-35	7C130-45 7C131-45 7C140-45 7C141-45	7C130-55 7C131-55 7C140-55 7C141-55
Maximum Access Time (ns)		25	30	35	45	55
Maximum Operating Current (mA)	Com'l/Ind	170	170	120	90	90
	Military			170	120	120
Maximum Standby Current (mA)	Com'l/Ind	65	65	45	35	35
	Military			65	45	45

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150 °C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	− 40°C to +85°C	5V ± 10%
Military[4]	− 55°C to +125°C	5V ± 10%

Notes:

3. 25-ns version available only in PLCC/LCC packages.
4. T_A is the "instant on" case temperature

Electrical Characteristics Over the Operating Range[5]

Parameter	Description	Test Conditions		7C130-25, 30[3] 7C131-25,30 7C140-25,30 7C141-25,30 Min.	Max.	7C130-35 7C131-35 7C140-35 7C141-35 Min.	Max.	7C130-45,55 7C131-45,55 7C140-45,55 7C141-45,55 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA			0.4		0.4		0.4	V
		I_{OL} = 16.0 mA[6]			0.5		0.5		0.5	
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		− 5	+5	− 5	+5	− 5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		− 5	+5	− 5	+5	− 5	+5	μA
I_{OS}	Output Short Circuit Current[7, 8]	V_{CC} = Max., V_{OUT} = GND			− 350		− 350		− 350	mA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[9]	Com'l		170		120		90	mA
			Mil				170		120	
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[9]	Com'l		65		45		35	mA
			Mil				65		45	
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, Active Port Outputs Open, f = f_{MAX}[9]	Com'l		115		90		75	mA
			Mil				115		90	
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0	Com'l		15		15		15	mA
			Mil				15		15	
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[9]	Com'l		105		85		70	mA
			Mil				105		85	

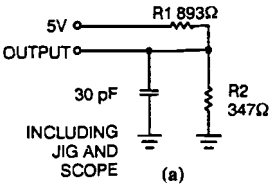
Capacitance[8]

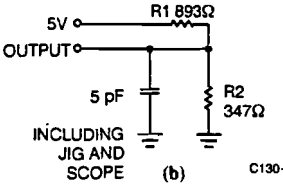
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	15	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

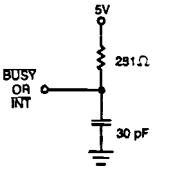
5. See the last page of this specification for Group A subgroup testing information.
6. $\overline{BUSY}$ and $\overline{INT}$ pins only.
7. Duration of the short circuit should not exceed 30 seconds.
8. Tested initially and after any design or process changes that may affect these parameters.
9. At f=f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of $1/t_{RC}$ and using AC Test Waveforms input levels of GND to 3V.
10. AC Test conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
11. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
12. AC Test Conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
13. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
14. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE} and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
15. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and R/$\overline{W}$ LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

AC Test Loads and Waveforms





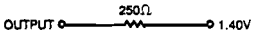
C130-5

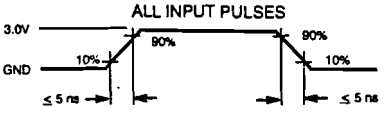


$\overline{\text{BUSY}}$ Output Load (CY7C130/CY7C131 ONLY)

C130-6

Equivalent to: THEVENIN EQUIVALENT





Switching Characteristics Over the Operating Range[5,11]

Parameter	Description	7C130-25[3] 7C131-25 7C140-25 7C141-25		7C130-30 7C131-30 7C140-30 7C141-30		7C130-35 7C131-35 7C140-35 7C141-35		7C130-45 7C131-45 7C140-45 7C141-45		7C130-55 7C131-55 7C140-55 7C141-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	25		30		35		45		55		ns
t_{AA}	Address to Data Valid[12]		25		30		35		45		55	ns
t_{OHA}	Data Hold from Address Change	0		0		0		0		0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[12]		25		30		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[12]		15		20		20		25		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[13]	3		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[13, 14]		15		15		20		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[13, 14]	5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[13, 14]		15		15		20		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		25		25		35		35		35	ns
WRITE CYCLE[15]												
t_{WC}	Write Cycle Time	25		30		35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		25		30		35		40		ns
t_{AW}	Address Set-Up to Write End	20		25		30		35		40		ns
t_{HA}	Address Hold from Write End	2		2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	15		25		25		30		30		ns
t_{SD}	Data Set-Up to Write End	15		15		15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High Z		15		15		20		20		25	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low Z	0		0		0		0		0		ns

Switching Characteristics Over the Operating Range[5,11] (continued)

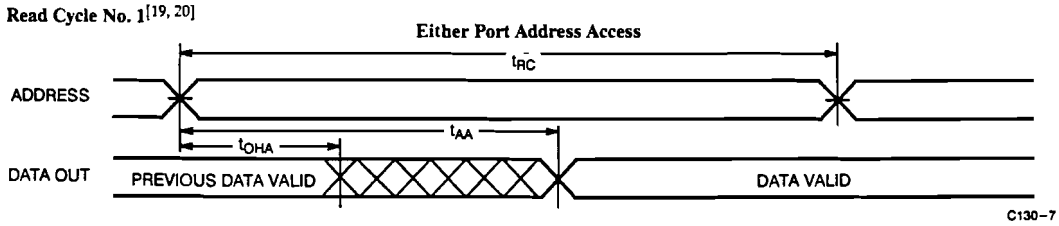
Parameter	Description	7C130-25[3] 7C131-25 7C140-25 7C141-25		7C130-30 7C131-30 7C140-30 7C141-30		7C130-35 7C131-35 7C140-35 7C141-35		7C130-45 7C131-45 7C140-45 7C141-45		7C130-55 7C131-55 7C140-55 7C141-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
BUSY/INTERRUPT TIMING												
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		20		20		20		25		30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch[16]		20		20		20		25		30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		20		20		20		25		30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH[16]		20		20		20		25		30	ns
t_{PS}	Port Set Up for Priority	5		5		5		5		5		ns
t_{WB}[17]	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	20		30		30		35		35		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Valid Data		25		30		35		45		45	ns
t_{DDD}	Write Data Valid to Read Data Valid		Note 18		Note 18		Note 18		Note 18		Note 18	ns
t_{WDD}	Write Pulse to Data Delay		Note 18		Note 18		Note 18		Note 18		Note 18	ns
INTERRUPT TIMING												
t_{WINS}	R/$\overline{W}$ to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{EINS}	$\overline{CE}$ to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{INS}	Address to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{OINR}	$\overline{OE}$ to $\overline{INTERRUPT}$ Reset Time[16]		25		25		25		35		45	ns
t_{EINR}	$\overline{CE}$ to $\overline{INTERRUPT}$ Reset Time[16]		25		25		25		35		45	ns
t_{INR}	Address to $\overline{INTERRUPT}$ Reset Time[16]		25		25		25		35		45	ns

Notes:

16. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
17. CY7C140/CY7C141 only.
18. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
    A. $\overline{BUSY}$ on Port B goes HIGH.
    B. Port B's address is toggled.
    C. $\overline{CE}$ for Port B is toggled.
    D. R/$\overline{W}$ for Port B is toggled during valid read.
19. R/$\overline{W}$ is HIGH for read cycle.
20. Device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
21. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
22. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or t_{HZWE} + t_{SD} to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.
23. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.

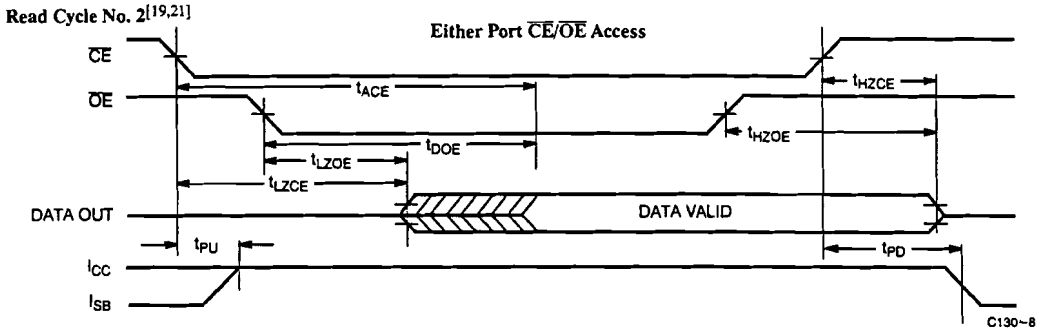
Switching Waveforms

Read Cycle No. 1[19, 20]

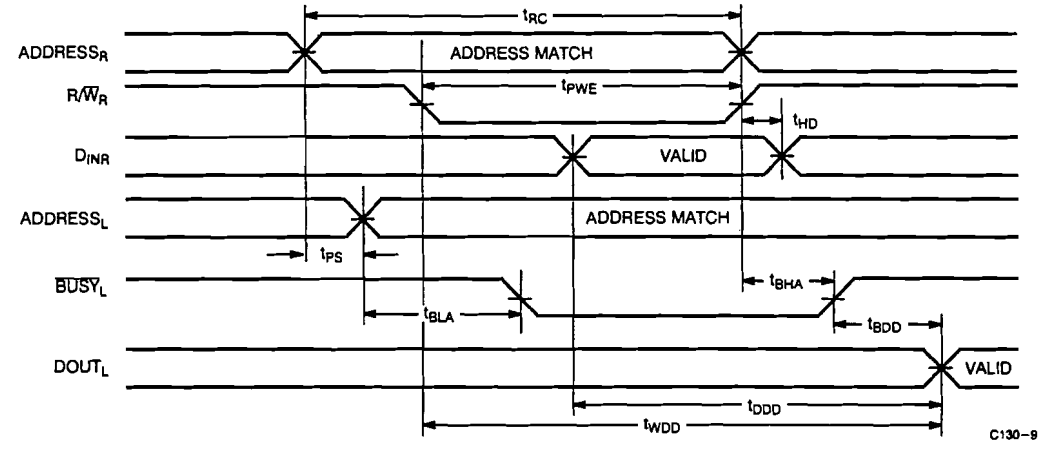


Switching Waveforms (continued)

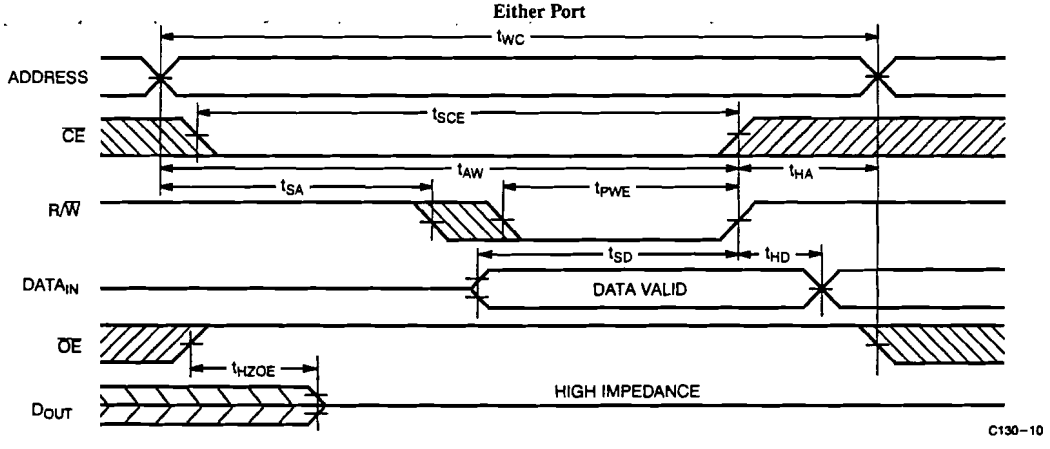
Read Cycle No. 2[19,21]



Read Cycle No. 3[20]

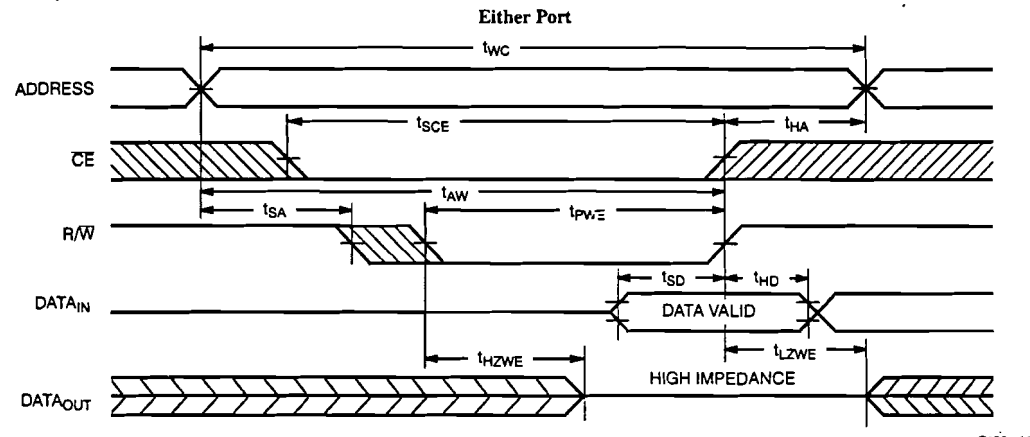


Write Cycle No.1 (OE Tri-States Data I/Os – Either Port)[15,22]



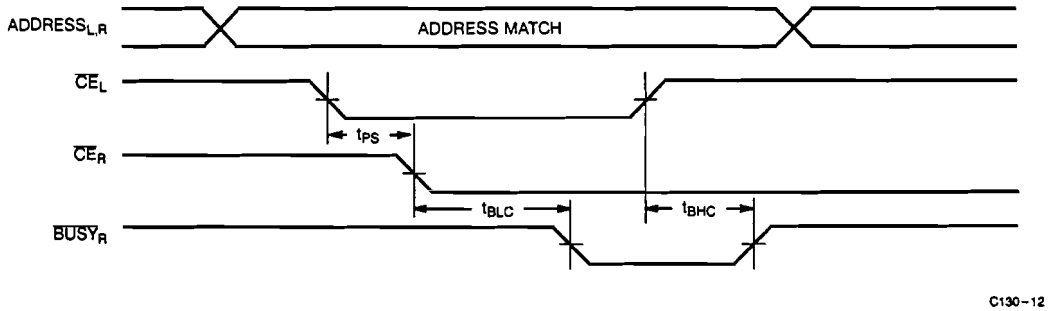
Switching Waveforms (continued)

Write Cycle No. 2 (R/$\overline{W}$ Tri-States Data I/Os – Either Port)[15,23]

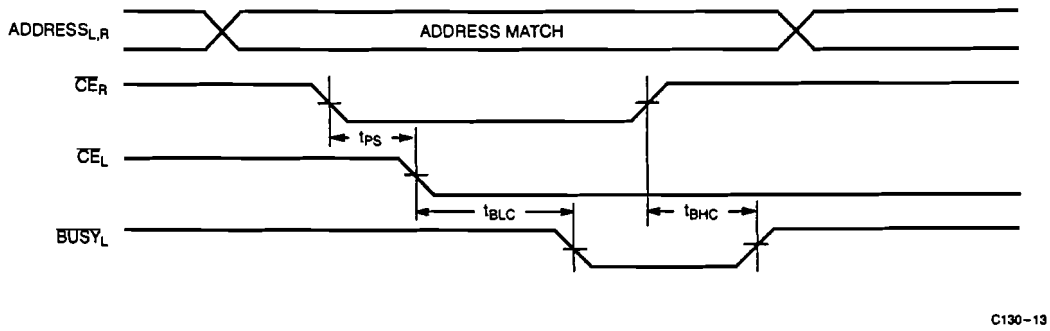


Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

$\overline{CE}_L$ Valid First:



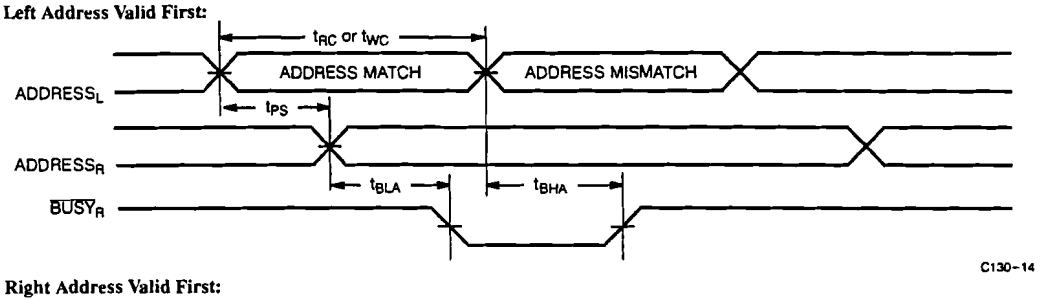
$\overline{CE}_R$ Valid First:



Switching Waveforms (continued)

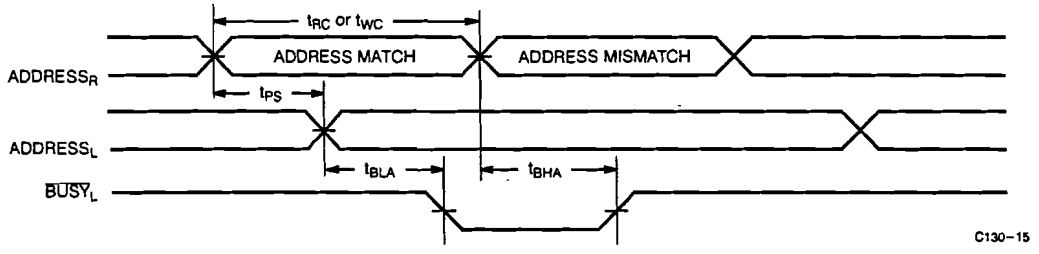
Busy Timing Diagram No. 2 (Address Arbitration)

Left Address Valid First:



C130-14

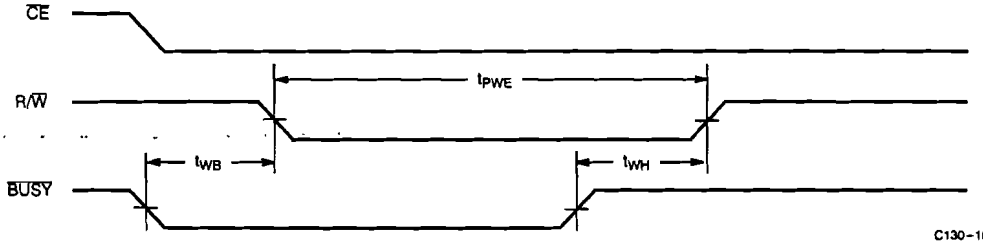
Right Address Valid First:



C130-15

Busy Timing Diagram No. 3

Write with $\overline{BUSY}$ (Slave: CY7C140/CY7C141)

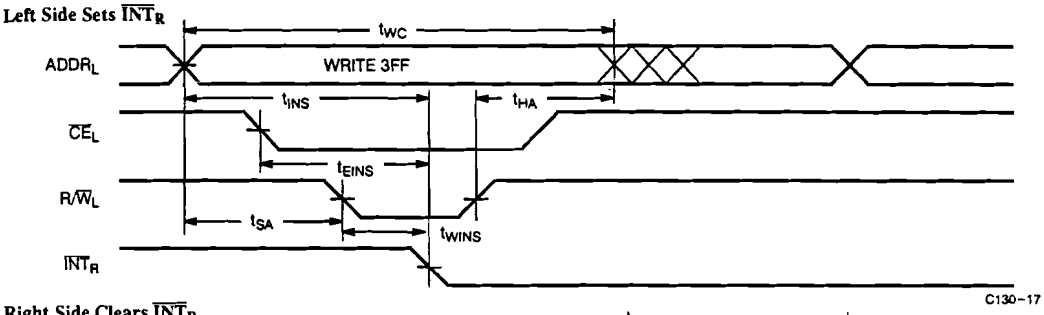


C130-16

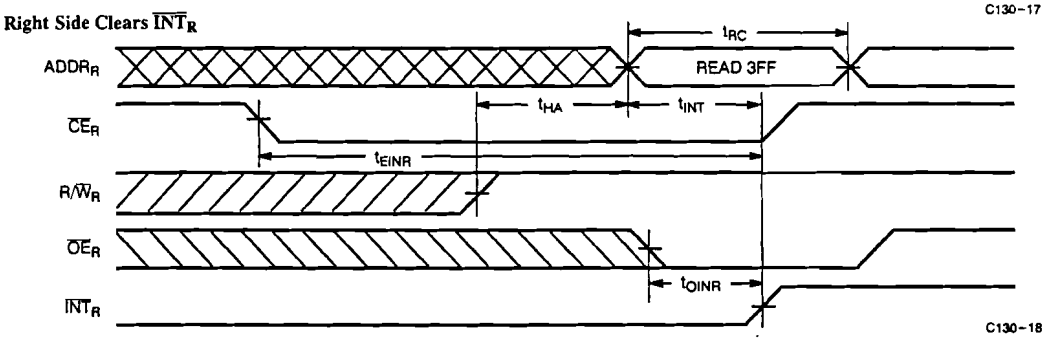
Switching Waveforms (continued)

Interrupt Timing Diagrams

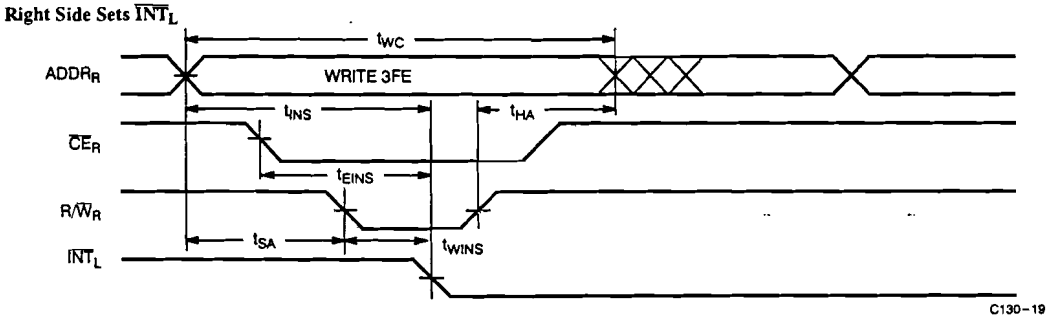
Left Side Sets $\overline{INT}_R$



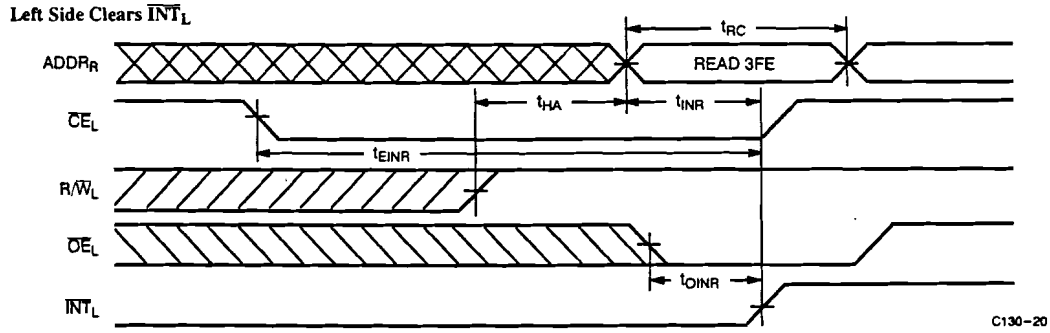
Right Side Clears $\overline{INT}_R$



Right Side Sets $\overline{INT}_L$

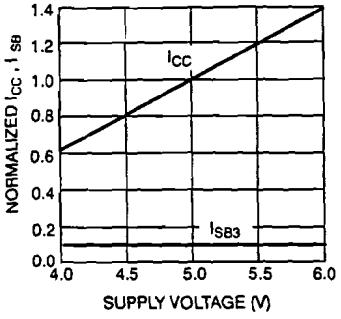


Left Side Clears $\overline{INT}_L$

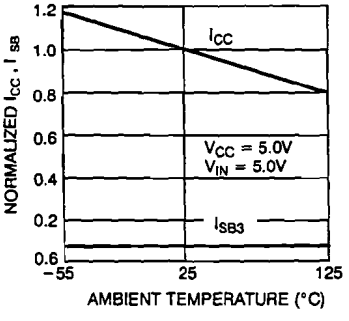


Typical DC and AC Characteristics

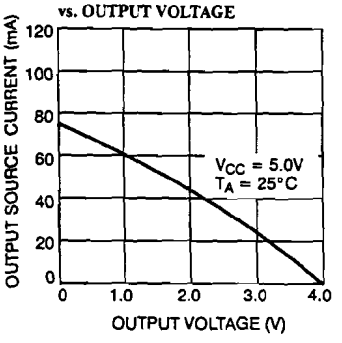
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



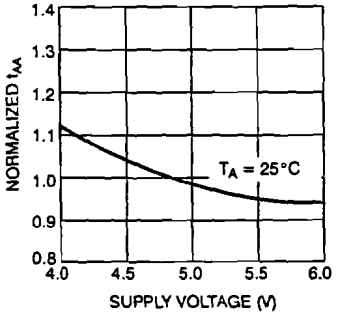
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



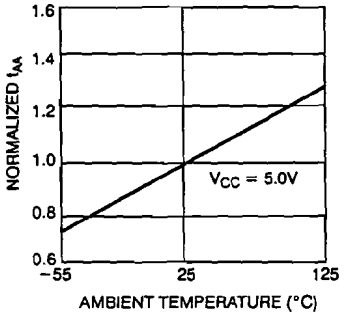
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



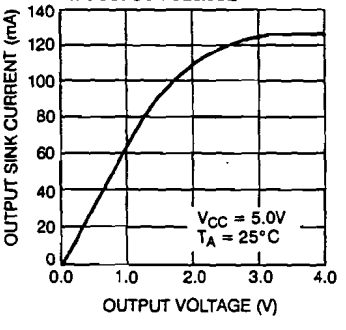
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



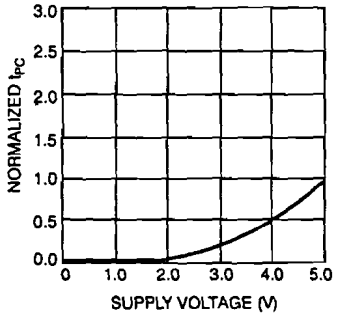
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



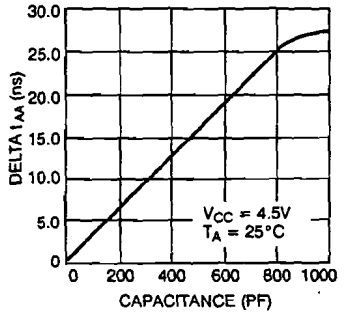
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



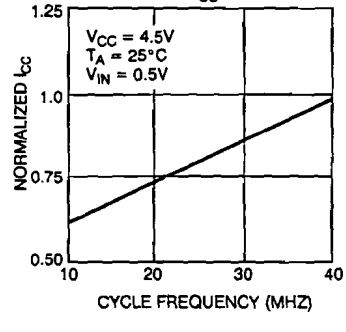
TYPICAL POWER–ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C130-30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130-30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C130-35PC	P25	48-Lead (600-Mil) Molded DIP	
	CY7C130-35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130-35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
	CY7C130-35FMB	F78	48-Lead Quad Flatpack	
	CY7C130-35LMB	L68	48-Square Leadless Chip Carrier	
45	CY7C130-45PC	P25	48-Lead (600-Mil) Molded DIP	
	CY7C130-45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130-45DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
	CY7C130-45FMB	F78	48-Lead Quad Flatpack	
	CY7C130-45LMB	L68	48-Square Leadless Chip Carrier	
55	CY7C130-55PC	P25	48-Lead (600-Mil) Molded DIP	
	CY7C130-55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130-55DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
	CY7C130-55FMB	F78	48-Lead Quad Flatpack	
	CY7C130-55LMB	L68	48-Square Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C131-25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
30	CY7C131-30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131-30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C131-35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131-35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131-35FMB	F78	48-Lead Quad Flatpack	Military
	CY7C131-35LMB	L69	52-Square Leadless Chip Carrier	
45	CY7C131-45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131-45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131-45FMB	F78	48-Lead Quad Flatpack	Military
	CY7C131-45LMB	L69	52-Square Leadless Chip Carrier	
55	CY7C131-55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131-55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131-55FMB	F78	48-Lead Quad Flatpack	Military
	CY7C131-55MB	L69	52-Square Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C140-30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140-30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C140-35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140-35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140-35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
	CY7C140-35FMB	F78	48-Lead Quad Flatpack	
	CY7C140-35LMB	L68	48-Square Leadless Chip Carrier	
45	CY7C140-45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140-45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140-45DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
	CY7C140-45FMB	F78	48-Lead Quad Flatpack	
	CY7C140-45LMB	L68	48-Square Leadless Chip Carrier	
55	CY7C140-55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140-55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140-55DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
	CY7C140-55FMB	F78	48-Lead Quad Flatpack	
	CY7C140-55LMB	L68	48-Square Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C141-25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
30	CY7C141-30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C141-35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141-35FMB	F78	48-Lead Quad Flatpack	Military
	CY7C141-35LMB	L69	52-Square Leadless Chip Carrier	
45	CY7C141-45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141-45FMB	F78	48-Lead Quad Flatpack	Military
	CY7C141-45LMB	L69	52-Square Leadless Chip Carrier	
55	CY7C141-55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141-55FMB	F78	48-Lead Quad Flatpack	Military
	CY7C141-55LMB	L69	52-Square Leadless Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1. 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Parameter	Subgroups
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{WINS}	7, 8, 9, 10, 11
t_{EINS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{OINR}	7, 8, 9, 10, 11
t_{EINR}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}[24]	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11

Note:
24. CY7C140/CY7C141 only.

Document #: 38-00027-I

FINAL

Am27C256

256 Kilobit (32,768 x 8-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - — 55 ns
- **Low power consumption**
  - — 20 µA typical CMOS standby current
- **JEDEC-approved pinout**
- **Single +5 V power supply**
- **±10% power supply tolerance available**
- **100% Flashrite™ programming**
  - — Typical programming time of 4 seconds
- **Latch-up protected to 100 mA from −1 V to Vcc + 1 V**
- **High noise immunity**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions
- **Standard 28-pin DIP, PDIP, 32-pin TSOP, LCC and LCC packages**
- **DESC SMD No. 5962–86063**

GENERAL DESCRIPTION

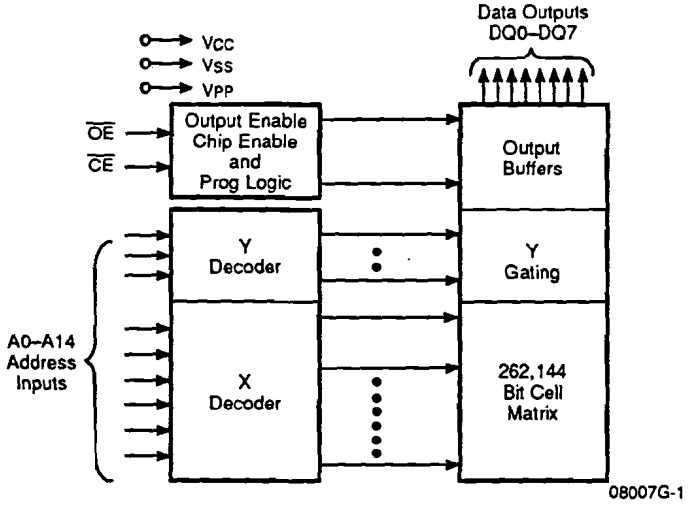
The Am27C256 is a 256K-bit ultraviolet erasable programmable read-only memory. It is organized as 32K words by 8 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages as well as plastic one time programmable (OTP) PDIP, TSOP, and PLCC packages.

Typically, any byte can be accessed in less than 55 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C256 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 80 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C256 supports AMD's Flashrite™ programming algorithm (100 µs pulses) resulting in typical programming time of 4 seconds.

BLOCK DIAGRAM



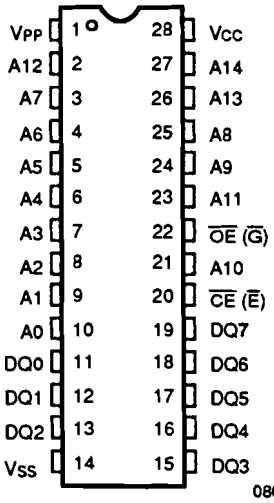
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C256						
Ordering Part No: Vcc ± 5%							-255
Vcc ± 10%	-55	-70	-90	-120	-150	-200	-250
Max Access Time (ns)	55	70	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	55	70	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access Time (ns)	35	40	40	50	65	75	100

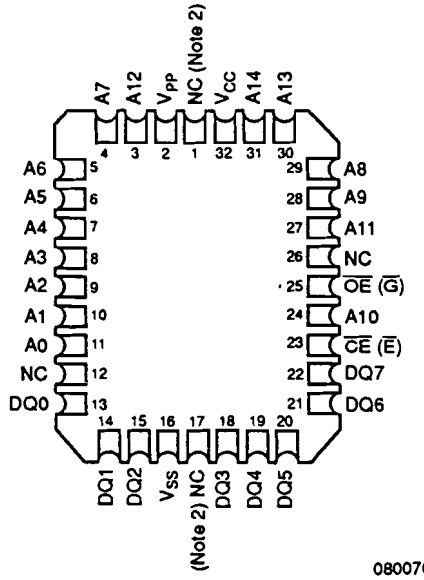
CONNECTION DIAGRAMS

Top View

DIP

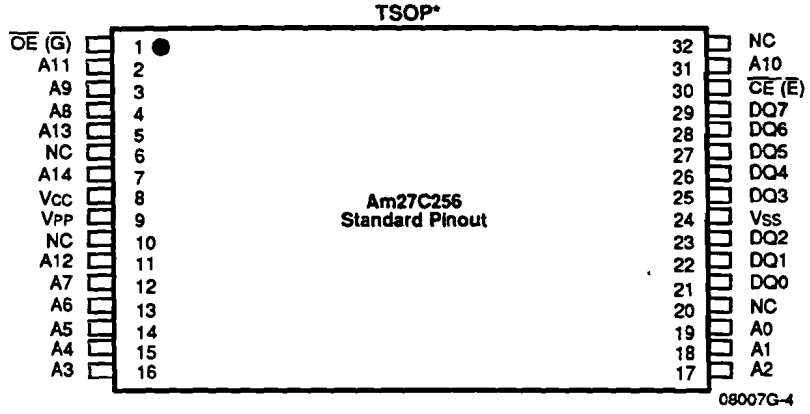


PLCC/LCC



Notes:

1. *JEDEC nomenclature is in parentheses.*
2. *Don't use (DU) for PLCC.*

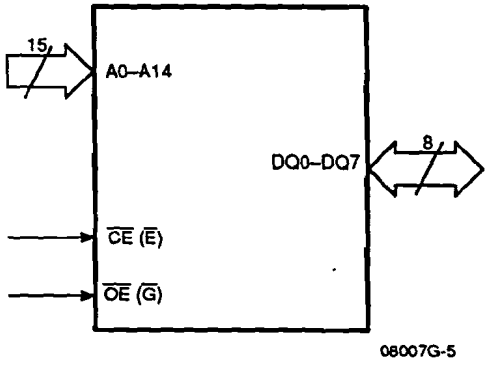


Contact local AMD sales office for package availability

PIN DESIGNATIONS

A0–A14	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable
DQ0–DQ7	=	Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
V_{SS}	=	Ground

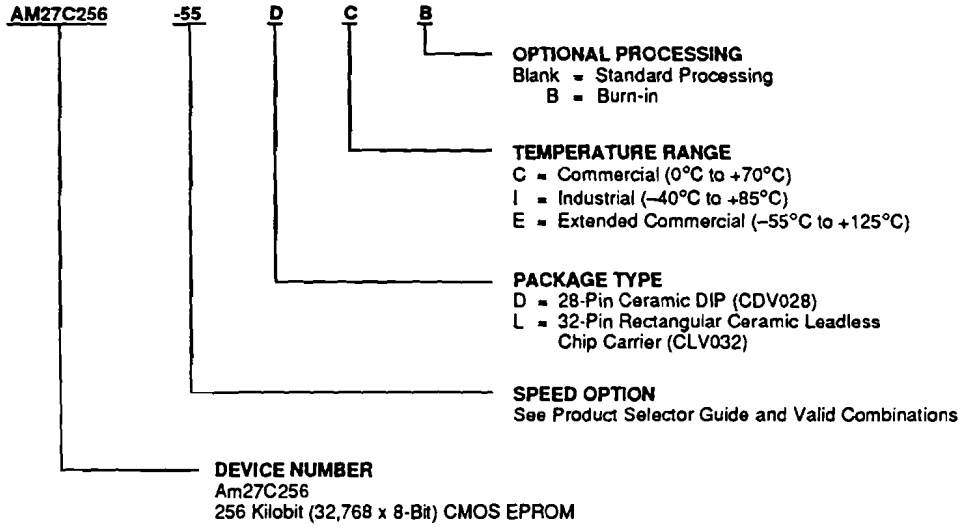
LOGIC SYMBOL



ORDERING INFORMATION

EPROM Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C256-55	DC, DCB, DI, DIB
AM27C256-70	LC, LCB, LI, LIB
AM27C256-90	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM27C256-120	
AM27C256-150	
AM27C256-200	
AM27C256-255	

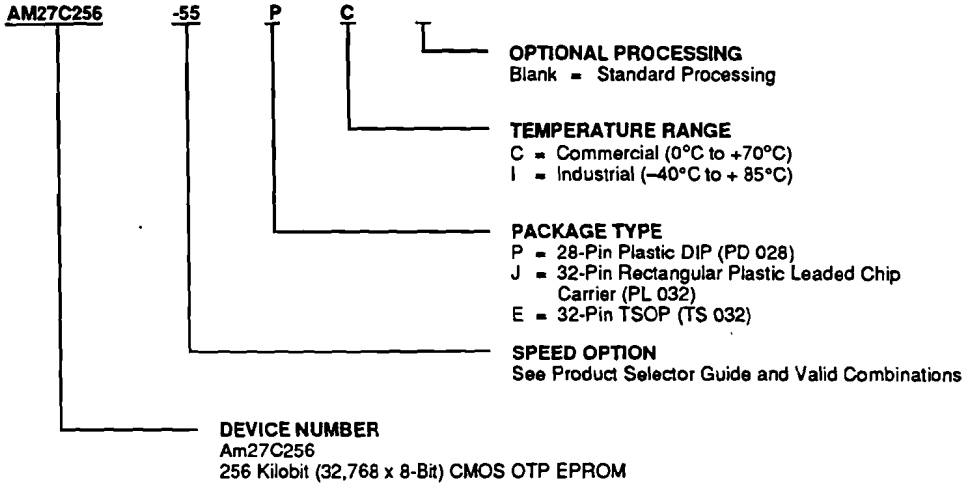
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

OTP Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C256-55	JC, PC, EC, JI, PI, EI
AM27C256-70	
AM27C256-90	
AM27C256-120	
AM27C256-150	
AM27C256-200	
AM27C256-255	

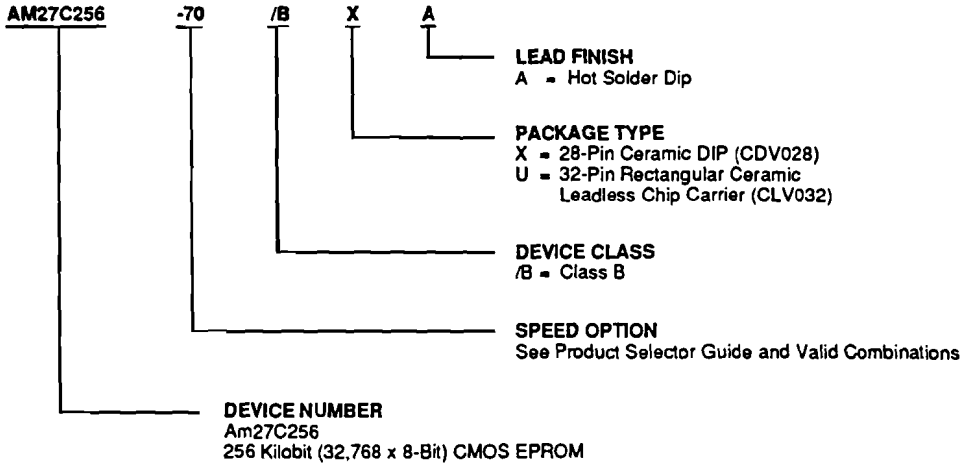
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Military APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C256-70	/BXA, /BUA
AM27C256-90	
AM27C256-120	
AM27C256-150	
AM27C256-200	
AM27C256-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C256

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C256 to an ultraviolet light source. A dosage of 15 W sec/cm² is required to completely erase an Am27C256. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Å—with intensity of 12,000 μW/cm² for 15 to 20 minutes. The Am27C256 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C256 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight will eventually erase the Am27C256 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C256

Upon delivery or after each erasure the Am27C256 has all 262,144 bits in the "ONE" or HIGH state. "ZEROs" are loaded into the Am27C256 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the V_{PP} pin, $\overline{OE}$ is at V_{IH}, and $\overline{CE}$ is at V_{IL}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 μs programming pulses and by giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C256. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP} = 5.25$ V.

Please refer to Section 6 for programming flow chart and characteristics.

Program Inhibit

Programming of multiple Am27C256 in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C256 may be common. A TTL low-level program pulse applied to an Am27C256 $\overline{CE}$ input with V_{PP} = 12.75 V ± 0.25 V, and $\overline{OE}$ High will program that Am27C256. A high-level $\overline{CE}$ input inhibits the other Am27C256 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH}, and V_{PP} between 12.5 V to 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C256.

To activate this mode, the programming equipment must force 12.0 V ± 0.5 V on address like A9 of the Am27C256. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A0 = V_{IL}$) represents the manufacturer code, and byte 1 ($A0 = V_{IH}$), the device code. For the Am27C256, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27C256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27C256 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 μA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C256 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1-µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	A0	A9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	V_{CC}	D_{OUT}
Output Disable		X	V_{IH}	X	X	V_{CC}	Hi-Z
Standby (TTL)		V_{IH}	X	X	X	V_{CC}	Hi-Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	V_{CC}	Hi-Z
Program		V_{IL}	V_{IH}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IH}	V_{IL}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	V_{IH}	X	X	V_{PP}	Hi-Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	V_{IL}	V_H	V_{CC}	01H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_H	V_{CC}	10H

Notes:

1. *$V_H = 12.0 V \pm 0.5 V$*
2. *X = Either V_{IH} or V_{IL}*
3. *A1 – A8 = A10 – A14 = V_{IL}*
4. *See DC Programming Characteristics for V_{PP} voltage during programming.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
- OTP Products ..... −65°C to +125°C
- All Other Products ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Voltage with Respect To V_{SS}
- All pins except A9, V_{PP}, V_{CC} (Note 1) ..... −0.6 V to V_{CC} + 0.5 V
- A9 and V_{PP} (Note 2) ..... −0.6 V to +13.5 V
- V_{CC} ..... −0.6 V to +7.0 V

Notes:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *For A9 and V_{PP} the minimum DC input is −0.5 V. During transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
- Case Temperature (T_C) ..... 0°C to +70°C

Industrial (I) Devices
- Case Temperature (T_C) ..... −40°C to +85°C

Extended Commercial (E) Devices
- Case Temperature (T_C) ..... −55°C to +125°C

Military (M) Devices
- Case Temperature (T_C) ..... −55°C to +125°C

Supply Read Voltages
- V_{CC} for Am27C256-XX5 ..... +4.75 V to +5.25 V
- V_{CC} for Am27C256-XX0 ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 2 and 4) (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}			1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{CC1}	Vcc Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 10 MHz, I_{OUT} = 0 mA			25	mA
I_{CC2}	Vcc TTL Standby Current	$\overline{CE}$ = V_{IH}			1.0	mA
I_{CC3}	Vcc CMOS Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V			100	µA
I_{PP1}	V_{PP} Current During Read	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27C256 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is –0.5 V. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

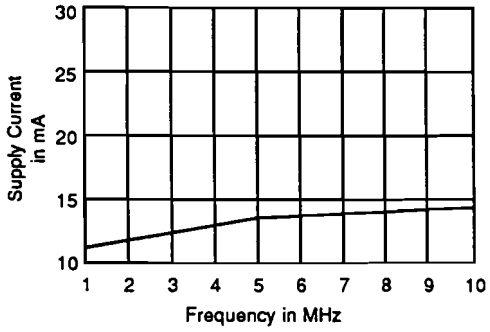


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

08007G-6

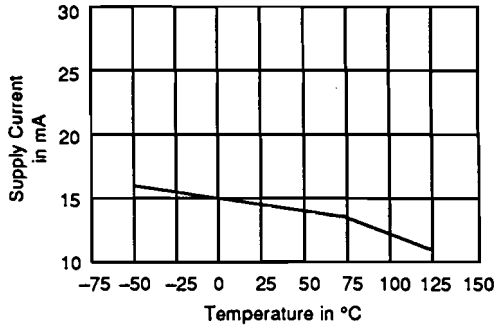


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 10 MHz

08007G-7

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CLV032		CDV028		PL 032		PD 028		TS 032		Unit
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0	11	14	8	12	8	12	6	10	10	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	10	14	8	12	8	12	8	10	12	14	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3 and 4) (for APL Products, Group A, Subgroups 9,10 and 11 are tested unless otherwise noted)

Parameter Symbols		Parameter Description	Test Conditions		Am27C256							Unit
JEDEC	Standard				-55	-70	-90	-120	-150	-200	-255 -250	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	–	–	
				Max	55	70	90	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	–	–	
				Max	55	70	90	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	–	–	–	–	–	–	–	
				Max	35	40	40	50	50	50	50	ns
t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	–	–	–	–	–	–	–	
				Max	25	25	25	30	30	30	30	ns
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	0	0	
				Max	–	–	–	–	–	–	–	ns

Notes:

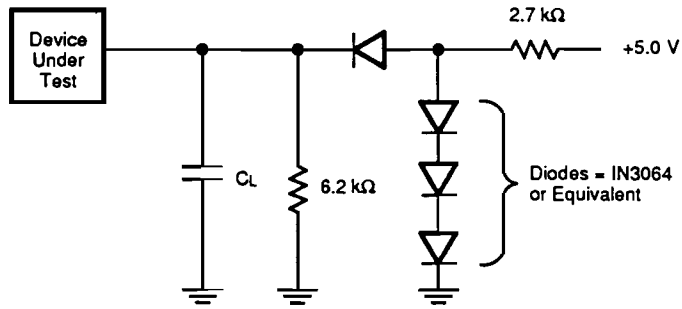
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. **Caution:** *The Am27C256 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *For the -55 and -70:*

   Output Load: 1 TTL gate and C_L = 30 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0 V to 3 V
   Timing Measurement Reference Level: 1.5 V for inputs and outputs

   For all other versions:

   Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V inputs and outputs

SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance (30 pF for –55, –70)

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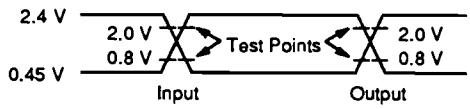
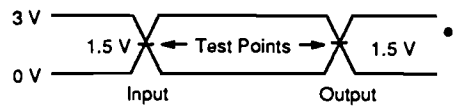
SWITCHING TEST WAVEFORM



AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns.



08007G-9

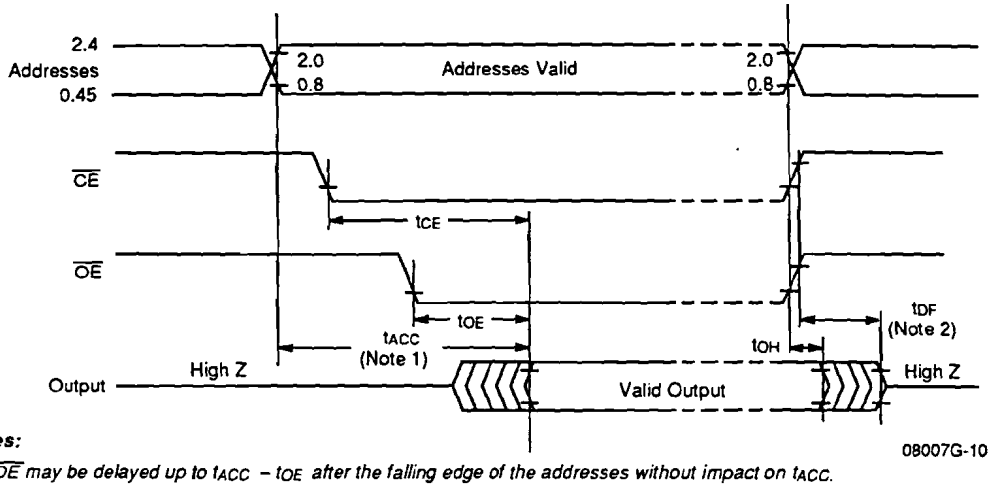
AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns for -55 and -70.

KEY TO SWITCHING TEST WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedence "Off" State

KS000010

SWITCHING WAVEFORMS



08007G-10

Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

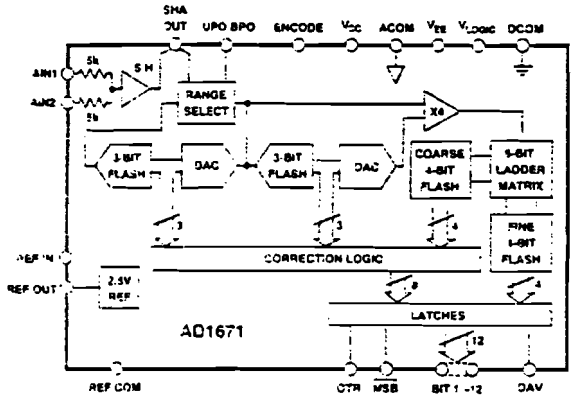
Complete 12-Bit 1.25 MSPS Monolithic A/D Converter

AD1671

FEATURES

Conversion Time: 800 ns
1.25 MHz Throughput Rate
Complete: On-Chip Sample-and-Hold Amplifier and Voltage Reference
Low Power Dissipation: 570 mW
No Missing Codes Guaranteed
Signal-to-Noise Plus Distortion Ratio
f_{IN} = 100 kHz: 70 dB
Pin Configurable Input Voltage Ranges
Twos Complement or Offset Binary Output Data
28-Pin DIP and 28-Pin Surface Mount Package
Out of Range Indicator

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1671 is a monolithic 12-bit, 1.25 MSPS analog-to-digital converter with an on-board, high performance sample-and-hold amplifier (SHA) and voltage reference. The AD1671 guarantees no missing codes over the full operating temperature range. The combination of a merged high speed bipolar/CMOS process and a novel architecture results in a combination of speed and power consumption far superior to previously available hybrid implementations. Additionally, the greater reliability of monolithic construction offers improved system reliability and lower costs than hybrid designs.

The fast settling input SHA is equally suited for both multiplexed systems that switch negative to positive full-scale voltage levels in successive channels and sampling inputs at frequencies up to and beyond the Nyquist rate. The AD1671 provides both reference output and reference input pins, allowing the on-board reference to serve as a system reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application.

The AD1671 uses a subranging flash conversion technique, with digital error correction for possible errors introduced in the first part of the conversion cycle. An on-chip timing generator provides strobe pulses for each of the four internal flash cycles. A single ENCODE pulse is used to control the converter. The digital output data is presented in twos complement or offset binary output format. An out-of-range signal indicates an overflow condition. It can be used with the most significant bit to determine low or high overflow.

The performance of the AD1671 is made possible by using high speed, low noise bipolar circuitry in the linear sections and low power CMOS for the logic sections. Analog Devices' ABCMOS-1 process provides both high speed bipolar and 2-micron CMOS devices on a single chip. Laser trimmed thin-film resistors are used to provide accuracy and temperature stability.

The AD1671 is available in two performance grades and three temperature ranges. The AD1671J and K grades are available over the 0°C to +70°C temperature range. The AD1671A grade is available over the −40°C to −85°C temperature range. The AD1671S grade is available over the −55°C to +125°C temperature range.

PRODUCT HIGHLIGHTS

The AD1671 offers a complete single chip sampling 12-bit, 1.25 MSPS analog-to-digital conversion function in a 28-pin package.

The AD1671 at 570 mW consumes a fraction of the power of currently available hybrids.

An OUT OF RANGE output bit indicates when the input signal is beyond the AD1671's input range.

Input signal ranges are 0 V to −5 V unipolar or ±5 V bipolar, selected by pin strapping, with an input resistance of 10 kΩ. The input signal range can also be pin strapped for 0 V to −2.5 V unipolar or ±2.5 V bipolar with an input resistance of 10 MΩ.

Output data is available in unipolar, bipolar offset or bipolar twos complement binary format.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
Telex: 924491 Cable: ANALOG NORWOODMASS

AD1671—SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −5 V ± 5%, unless otherwise indicated)

Parameter	AD1671J/A/S Min	AD1671J/A/S Typ	AD1671J/A/S Max	AD1671K Min	AD1671K Typ	AD1671K Max	Units
RESOLUTION	12			12			Bits
CONVERSION TIME			800			800	ns
ACCURACY							
Integral Nonlinearity (INL)		±1.5	±2.5		±0.7	±1.5	LSB
Differential Nonlinearity (DNL)	11			12			Bits
No Missing Codes	11 Bits Guaranteed			12 Bits Guaranteed			
Unipolar Offset[1] (+25°C)			±9			±9	LSB
Bipolar Zero[1] (+25°C)			±10			±10	LSB
Gain Error[1, 2] (+25°C)		0.1	0.35		0.1	0.35	% FSR
TEMPERATURE COEFFICIENTS[3]							
Unipolar Offset			±15			±15	ppm/°C
Bipolar Zero			±15			±15	ppm/°C
Gain Error[3]			±30			±30	ppm/°C
Gain Error[4]			±20			±20	ppm/°C
POWER SUPPLY REJECTION[5]							
V_{CC} (+5 V ± 0.25 V)			±2			±2	LSB
V_{LOGIC} (+5 V ± 0.25 V)			±2			±2	LSB
V_{EE} (−5 V ± 0.25 V)			±2			±2	LSB
ANALOG INPUT							
Input Ranges							
Bipolar	−2.5		−2.5	−2.5		+2.5	Volts
	−5.0		−5.0	−5.0		+5.0	Volts
Unipolar	0		+2.5	0		+2.5	Volts
	0		−5.0	0		+5.0	Volts
Input Resistance							
(0 V to +2.5 V or ±2.5 V Range)		10			10		MΩ
(0 V to +5.0 V or ±5 V Range)	8	10	12	8	10	12	kΩ
Input Capacitance		10			10		pF
Aperture Delay		15			15		ns
Aperture Jitter		20			20		ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage	2.475	2.5	2.525	2.475	2.5	2.525	Volts
Output Current							
Unipolar Mode			−2.5			+2.5	mA
Bipolar Mode			+1.0			−1.0	mA
LOGIC INPUTS							
High Level Input Voltage, V_{IH}	2.0			2.0			Volts
Low Level Input Voltage, V_{IL}			0.8			0.8	Volts
High Level Input Current, I_{IH} (V_{IN} = V_{LOGIC})	−10		−10	−10		+10	μA
Low Level Input Current, I_{IL} (V_{IN} = 0 V)	−10		+10	−10		+10	μA
Input Capacitance, C_{IN}		5			5		pF
LOGIC OUTPUTS							
High Level Output Voltage, V_{OH} (I_{OH} = 0.5 mA)	2.4			2.4			Volts
Low Level Output Voltage, V_{OL} (I_{OL} = 1.6 mA)			0.4			0.4	Volts
POWER SUPPLIES							
Operating Voltages							
V_{CC}	+4.75		+5.25	+4.75		+5.25	Volts
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	Volts
V_{EE}	−4.75		−5.25	−4.75		−5.25	Volts
Operating Current							
I_{CC}		55	68		55	68	mA
I_{LOGIC}[6]		3	5		3	5	mA
I_{EE}		−55	−68		−55	−68	mA
POWER CONSUMPTION		570	750		570	750	mW
TEMPERATURE RANGE (SPECIFIED)							
J/K	0		+70	0		+70	°C
A D	−40		+85	−40		+85	°C
S	−55		+125	−55		+125	°C

NOTES
[1]Adjustable to zero with external potentiometers.
[2]Includes internal voltage reference error.
[3]−25°C to T_{MIN} and −25°C to T_{MAX}.
[4]Excludes internal reference drift.
[5]Change in gain error as a function of the dc supply voltage.
[6]Tested under static conditions. See Figure 15 for typical curve of I_{LOGIC} vs. load capacitance at maximum f_C.

Specifications subject to change without notice.

AC SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −5 V ± 5%, f_{SAMPLE} = 1 MSPS, f_{INPUT} = 100 kHz, unless otherwise noted)[1]

Parameter	AD1671J/A/S Min	AD1671J/A/S Typ	AD1671J/A/S Max	AD1671K Min	AD1671K Typ	AD1671K Max	Units
SIGNAL-TO-NOISE PLUS DISTORTION RATIO (S/N + D)							
−0.5 dB Input	68	70		70	71		dB
−20 dB Input		50			51		dB
EFFECTIVE NUMBER OF BITS (ENOB)	11.2			11.3			Bits
TOTAL HARMONIC DISTORTION (THD)		−80	−75		−83	−78	dB
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		−80	−77		−81	−78	dB
SMALL SIGNAL BANDWIDTH		12			12		MHz
FULL POWER BANDWIDTH		2			2		MHz
INTERMODULATION DISTORTION (IMD)[2]							
2nd Order Products		−80	−78		−80	−78	dB
3rd Order Products		−85	−78		−85	−78	dB

NOTES
[1] f_{IN} amplitude = −0.5 dB (9.44 V p-p) bipolar mode full scale unless otherwise indicated. All measurements referred to a 0 dB (±5 V) input signal, unless otherwise indicated.
[2] f_A = 99 kHz, f_B = 100 kHz with f_{SAMPLE} = 1 MSPS.
Specifications subject to change without notice.

SWITCHING SPECIFICATIONS (For all grades T_{MIN} to T_{MAX} with V_{CC} = +5 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −5 V ± 5%; V_{IL} = 0.8 V, V_{IH} = 2.0 V, V_{OL} = 0.4 V and V_{OH} = 2.4 V)

Parameters	Symbol	Min	Typ	Max	Units
Conversion Time	t_C			800	ns
ENCODE Pulse Width High (Figure 1a)	t_{ENC}	20		50	ns
ENCODE Pulse Width Low (Figure 1b)	t_{ENCL}	20			ns
DAV Pulse Width	t_{DAV}	150		300	ns
ENCODE Falling Edge Delay	t_F	0			ns
Start New Conversion Delay	t_R	20			ns
Data and OTR Delay from DAV Falling Edge	t_{DD}[1]	20	75		ns
Data and OTR Valid before DAV Rising Edge	t_{SS}[2]	20	75		ns

NOTES
[1] t_{DD} is measured from when the falling edge of DAV crosses 0.8 V to when the output crosses 0.4 V or 2.4 V with a 25 pF load capacitor on each output pin.
[2] t_{SS} is measured from when the outputs cross 0.4 V or 2.4 V to when the rising edge of DAV crosses 2.4 V with a 25 pF load capacitor on each output pin.
Specifications subject to change without notice.

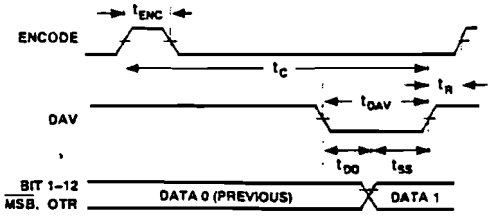


Figure 1a. Encode Pulse HIGH

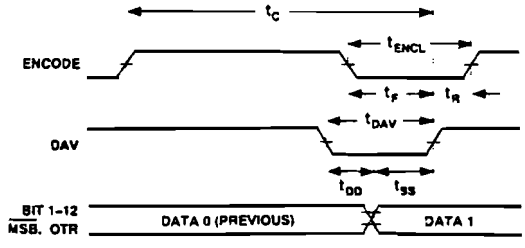


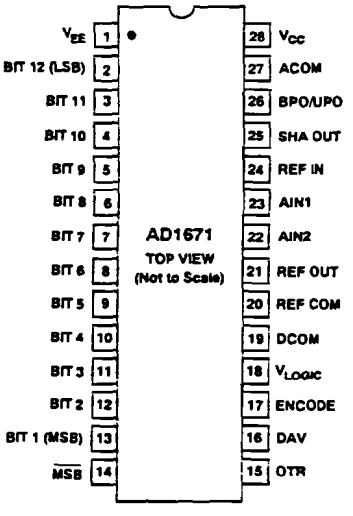
Figure 1b. Encode Pulse LOW

PIN DESCRIPTION

Symbol	Pin No.	Type	Name and Function
ACOM	27	P	Analog Ground.
AIN	22, 23	AI	Analog Inputs, AIN1 and AIN2. The AD1671 can be pin strapped for four input ranges: Range — Pin Strap — Signal Input 0 to +2.5 V, ±2.5 V — Connect AIN1 to AIN2 — AIN1 or AIN2 0 to +5 V, ±5 V — Connect AIN1 or AIN2 to ACOM — AIN1 or AIN2
BIT 1 (MSB)	13	DO	Most Significant Bit.
BIT 2–BIT 11	12–3	DO	Data Bits 2 through 11.
BIT 12 (LSB)	2	DO	Least Significant Bit.
BPO/UPO	26	AI	Bipolar or Unipolar Configuration Pin. See section on Input Range Connections for details.
DAV	16	DO	Data Available Output. The rising edge of DAV indicates an end of conversion and can be used to latch current data into an external register. The falling edge of DAV can be used to latch previous data into an external register.
DCOM	19	P	Digital Ground.
ENCODE	17	DI	The analog input is sampled on the rising edge of ENCODE.
$\overline{MSB}$	14	DO	Inverted Most Significant Bit. Provides twos complement output data format.
OTR	15	DO	Out of Range is Active HIGH when the analog input is out of range. See Output Data Format, Table III.
REF COM	20	AI	REF COM is the internal reference ground pin. REF COM should be connected as indicated in the Grounding and Decoupling Rules and Optional External Reference Connection Sections.
REF IN	24	AI	REF IN is the external 2.5 V reference input.
REF OUT	21	AO	REF OUT is the internal 2.5 V reference output.
SHA OUT	25	AO	No Connect for bipolar input ranges. Connect SHA OUT to BPO/UPO for unipolar input ranges.
V_{CC}	28	P	+5 V Analog Power.
V_{EE}	1	P	−5 V Analog Power.
V_{LOGIC}	18	P	+5 V Digital Power.

TYPE: AI = Analog Input; AO = Analog Output; DI = Digital Input; DO = Digital Output; P = Power.

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
V_{CC}	ACOM	−0.5	+6.5	Volts
V_{EE}	ACOM	−6.5	−0.5	Volts
V_{LOGIC}	DCOM	−6.5	+0.5	Volts
ACOM	DCOM	−1.0	+1.0	Volts
V_{CC}	V_{LOGIC}	−6.5	+6.5	Volts
ENCODE	DCOM	−0.5	V_{LOGIC}+0.5	Volts
REF IN	ACOM	−0.5	V_{CC}+0.5	Volts
AIN	ACOM	−11.0	+11.0	Volts
BPO/UPO	ACOM	−0.5	V_{CC}+0.5	Volts
Junction Temperature			+150	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

ORDERING GUIDE

Model[1]	Linearity	Temperature Range	Package Option[2, 3]
AD1671JQ	±2.5 LSB	0°C to +70°C	Q-28
AD1671KQ	±1.5 LSB	0°C to +70°C	Q-28
AD1671JP	±2.5 LSB	0°C to +70°C	P-28
AD1671KP	±1.5 LSB	0°C to +70°C	P-28
AD1671AQ	±2.5 LSB	−40°C to +85°C	Q-28
AD1671SQ	±2.5 LSB	−55°C to +125°C	Q-28

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to Analog Devices' Military Products Databook or current AD1671/883 data sheet.
[2]P = Plastic Leaded Chip Carrier; Q = Cerdip.
[3]Analog Devices reserves the right to ship side brazed ceramic packages in lieu of cerdip.

DEFINITIONS OF SPECIFICATIONS

INTEGRAL NONLINEARITY (INL)

Integral nonlinearity refers to the deviation of each individual code from a line drawn from "zero" through "full scale." The point used as "zero" occurs 1/2 LSB (1.22 mV for a 10 V span) before the first code transition (all zeros to only the LSB on). "Full-scale" is defined as a level 1 1/2 LSB beyond the last code transition (to all ones). The deviation is measured from the low side transition of each particular code to the true straight line.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from the ideal value. Thus every code has a finite width. Guaranteed no missing codes to 11 or 12-bit resolution indicates that all 2048 and 4096 codes, respectively, must be present over all operating ranges. No missing codes to 11 bits (in the case of a 12-bit resolution ADC) also means that no two consecutive codes are missing.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual from that point. This offset can be adjusted as discussed later. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustments.

BIPOLAR ZERO

In the bipolar mode the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2 LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

GAIN ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1 1/2 LSB below the nominal full scale (4.9963 volts for 5.000 volts full scale). The gain error is the deviation of the actual level at the last transition from the ideal level. The gain error can be adjusted to zero as shown in Figures 4 through 7.

TEMPERATURE COEFFICIENTS

The temperature coefficients for unipolar offset, bipolar zero and gain error specify the maximum change from the initial (+25°C) value to the value at T_{MIN} or T_{MAX}.

POWER SUPPLY REJECTION

One of the effects of power supply error on the performance of the device will be a small change in gain. The specifications show the maximum full-scale change from the initial value with the supplies at the various limits.

DYNAMIC SPECIFICATIONS

SIGNAL-TO-NOISE PLUS DISTORTION (S/N+D) RATIO

S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

EFFECTIVE NUMBER OF BITS (ENOB)

ENOB is calculated from the expression (S/N+D) = 6.02N + 1.76 dB, where N is equal to the effective number of bits.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

INTERMODULATION DISTORTION (IMD)

With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products of order (m+n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa − fb) and (fa − fb), and the third order terms are (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (2fb − fa). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals are of equal amplitude and the peak value of their sum is −0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

PEAK SPURIOUS OR PEAK HARMONIC COMPONENT

The peak spurious or peak harmonic component is the largest spectral component, excluding the input signal and dc. This

value is expressed in decibels relative to the rms value of a full-scale input signal.

APERTURE DELAY

Aperture delay is the difference between the switch delay and the analog delay of the SHA. This delay represents the point in time, relative to the rising edge of ENCODE input, that the analog input is sampled.

APERTURE JITTER

Aperture jitter is the variation in aperture delay for successive samples.

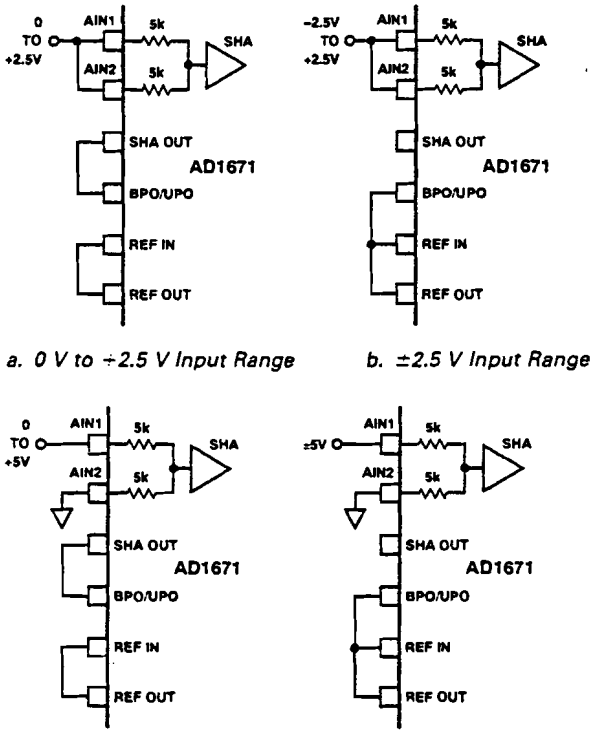
FULL POWER BANDWIDTH

The input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

THEORY OF OPERATION

The AD1671 uses a successive subranging architecture. The analog-to-digital conversion takes place in four independent steps or flashes. The sampled analog input signal is subranged to an intermediate residue voltage for the final 12-bit result by utilizing multiple flashes with subtraction DACs (see the AD1671 functional block diagram).

The AD1671 can be configured to operate with unipolar (0 V to +5 V, 0 V to +2.5 V) or bipolar (±5 V, ±2.5 V) inputs by connecting AIN (Pins 22, 23), SHA OUT (Pin 25) and BPO/UPO (Pin 26) as shown in Figure 2.



a. 0 V to +2.5 V Input Range *b. ±2.5 V Input Range*

c. 0 V to +5 V Input Range *d. ±5 V Input Range*

Figure 2. AD1671 Input Range Connections

The AD1671 conversion cycle begins by simply providing an active HIGH level on the ENCODE pin (Pin 17). The rising edge of the ENCODE pulse starts the conversion. The falling edge of the ENCODE pulse is specified to operate within a window of time, less than 50 ns after the rising edge of ENCODE or after the falling edge of DAV. The time window prevents digitally coupled noise from being introduced during the final stages of conversion. An internal timing generator circuit accurately controls SHA, flash and DAC timing.

Upon receipt of an ENCODE command the input voltage is held by the front-end SHA and the first 3-bit flash converts the analog input voltage. The 3-bit result is passed to a correction logic register and a segmented current output DAC. The DAC output is connected through a resistor (within the Range/Span Select Block) to SHA OUT. A residue voltage is created by subtracting the DAC output from SHA OUT, which is less than one eighth of the full-scale analog input. The second flash has an input range that is configured with one bit of overlap with the previous DAC. The overlap allows for errors during the flash conversion. The first residue voltage is connected to the second 3-bit flash and to the noninverting input of a high speed, differential, gain of eight amplifier. The second flash result is passed to the correction logic register and to the second segmented current output DAC. The output of the second DAC is connected to the inverting input of the differential amplifier. The differential amplifier output is connected to a two-step, backend, 8-bit flash. This 8-bit flash consists of coarse and fine flash converters. The result of the coarse 4-bit flash converter, also configured to overlap one bit of DAC 2, is connected to the correction logic register and selects one of 16 resistors from which the fine 4-bit flash will establish its span voltage. The fine 4-bit flash is connected directly to the output latches.

The internal timing generator automatically places the SHA into the acquire mode when DAV goes LOW. Upon completion of conversion (when DAV is set HIGH), the SHA has acquired the analog input to the specified level of accuracy and will remain in the sample mode until the next ENCODE command.

The AD1671 will flag an out-of-range condition when the input voltage exceeds the analog input range. OTR (Pin 15) is active HIGH when an out-of-range high or low condition exists. Bits 1–12 are HIGH when the analog input voltage is greater than the selected input range and LOW when the analog input is less than the selected input range.

AD1671 DYAMIC PERFORMANCE

The AD1671 is specified for dc and dynamic performance. A sampling converter's dynamic performance reflects both quantizer and sample-and-hold amplifier (SHA) performance. Quantizer nonlinearities, such as INL and DNL, can degrade dynamic performance. However, a SHA is the critical element which has to accurately sample fast slewing analog input signals. The AD1671's high performance, low noise, patented on-chip SHA minimizes distortion and noise specifications. Nonlinearities are minimized by using a fast slewing, low noise architecture and subregulation of the sampling switch to provide constant offsets (therefore reducing input signal dependent nonlinearities).

Figure 3 is a typical 2k point Fast Fourier Transform (FFT) plot of a 100 kHz input signal sampled at 1 MHz. The fundamental amplitude is set at −0.5 dB to avoid input signal clipping of offset or gain errors. Note the total harmonic distortion is approximately −81 dB, signal to noise plus distortion is 71 dB and the spurious free dynamic range is 84 dB.

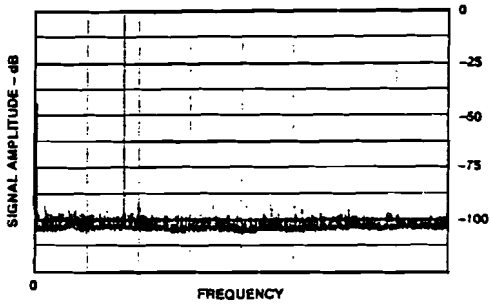


Figure 3. AD1671 FFT Plot, f_{IN} = 100 kHz, f_{SAMPLE} = 1 MHz

Figure 4 plots both S/(N+D) and Effective Number of Bits (ENOB) for a 100 kHz input signal sampled from 666 kHz to 1.25 MHz.

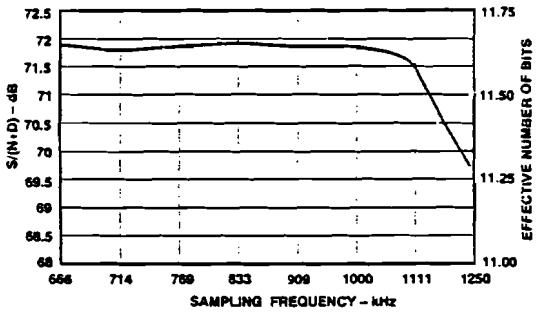


Figure 4. S/(N+D) vs. Sampling Frequency, f_{IN} = 100 kHz

Figure 5 is a THD plot for a full-scale 100 kHz input signal with the sample frequency swept from 666 kHz to 1.25 MHz.

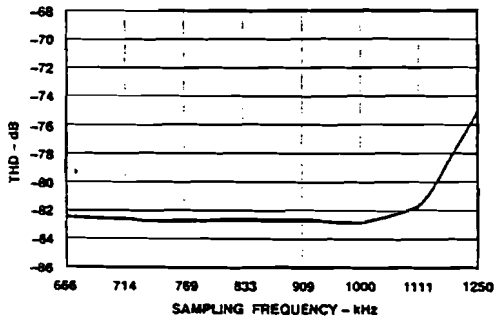


Figure 5. THD vs. Sampling Rate, f_{IN} = 100 kHz

The AD1671's SFDR performance is ideal for use in communication systems such as high speed modems and digital radios. The SFDR is better than 84 dB with sample rates up to 1.11 MHz and increases as the input signal amplitude is attenuated by approximately 3 dB. Note also the SFDR is typically better than 80 dB with input signals attenuated by up to −7 dB.

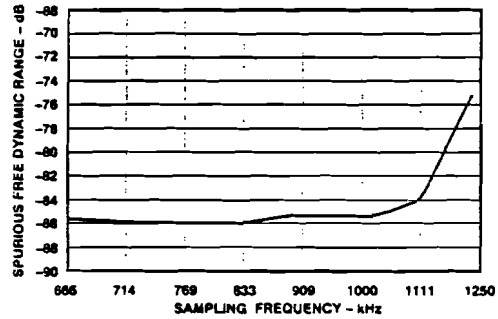


Figure 6. Spurious Free Dynamic Range vs. Sampling Rate, f_{IN} = 100 kHz

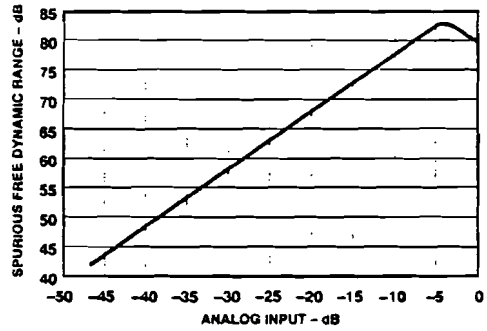


Figure 7. Spurious Free Dynamic Range vs. Input Amplitude, f_{IN} = 250 kHz

APPLYING THE AD1671

GROUNDING AND DECOUPLING RULES

Proper grounding and decoupling should be a primary design objective in any high speed, high resolution system. The AD1671 separates analog and digital grounds to optimize the management of analog and digital ground currents in a system. The AD1671 is designed to minimize the current flowing from REF COM (Pin 20) by directing the majority of the current from V_{CC} (+5 V–Pin 28) to V_{EE} (−5 V–Pin 1). Minimizing analog ground currents hence reduces the potential for large ground voltage drops. This can be especially true in systems that do not utilize ground planes or wide ground runs. REF COM is also configured to be code independent, therefore reducing input dependent analog ground voltage drops and errors. Code dependent ground current is diverted to ACOM (Pin 27). Also critical in any high speed digital design is the use of proper digital grounding techniques to avoid potential CMOS "ground bounce." Figure 3 is provided to assist in the proper layout, grounding and decoupling techniques.

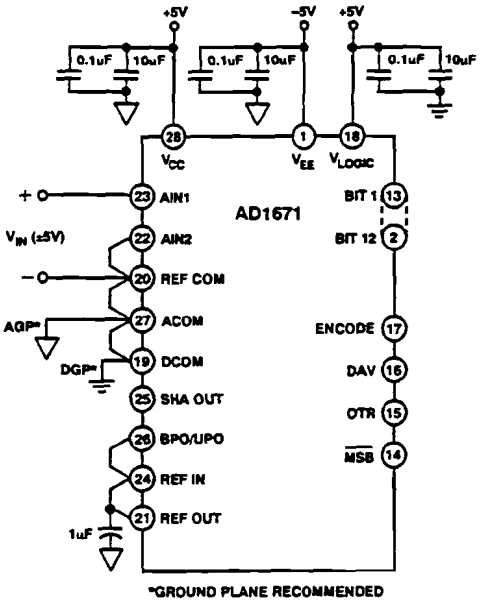


Figure 8. AD1671 Grounding and Decoupling

Table I is a list of grounding and decoupling rules that should be reviewed before laying out a printed circuit board.

Table I. Grounding and Decoupling Guidelines

Power Supply Decoupling	Comment
Capacitor Values	0.1 μF (Ceramic) and 1 μF (Tantalum) Surface Mount Chip Capacitors Recommended to Reduce Lead Inductance
Capacitor Locations	Directly at Positive and Negative Supply Pins to Common Ground Plane
Reference (REF OUT)	
Capacitor Value	1 μF (Tantalum) to ACOM
Grounding	
Analog Ground	Ground Plane or Wide Ground Return Connected to the Analog Power Supply
Reference Ground (REF COM)	Critical Common Connections Should be Star Connected to REF COM (as Shown in Figure 8)
Digital Ground	Ground Plane or Wide Ground Return Connected to the Digital Power Supply
Analog and Digital Ground	Connected Together Once at the AD1671

UNIPOLAR (0 V TO +5 V) CALIBRATION

The AD1671 is factory trimmed to minimize offset, gain and linearity errors. In some applications the offset and gain errors of the AD1671 need to be externally adjusted to zero. This is accomplished by trimming the voltage at AIN2 (Pin 22). The circuit in Figure 9 is recommended for calibrating offset and gain errors of the AD1671 when configured in the 0 V to +5 V input range. If the offset trim resistor R1 is used, it should be trimmed as follows, although a different offset can be set for a particular system requirement. This circuit will give approximately ±5 mV of offset trim range. Nominally the AD1671 is intended to have a 1/2 LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above it and below it). Thus, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2 LSB (0.61 mV for 5 V range).

The gain trim is done by applying a signal 1 1/2 LSBs below the nominal full scale (4.998 V for a 5 V range). Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111). This circuit will give approximately ±0.5% FS of adjustment range.

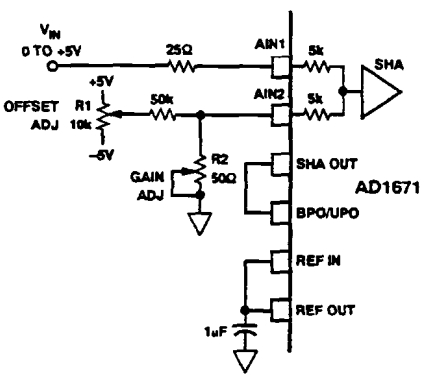


Figure 9. Unipolar (0 V to +5 V) Calibration

BIPOLAR (±5 V) CALIBRATION

The connections for the bipolar ±5 V input range is shown in Figure 10.

Bipolar calibration is similar to unipolar calibration. First, a signal 1/2 LSB above negative full scale (−4.9988 V) is applied and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1 1/2 LSB below positive full scale (+4.9963 V) is applied and R2 is trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

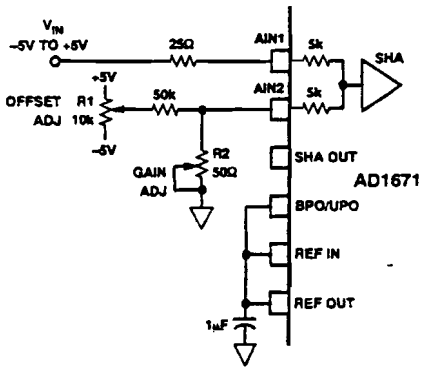


Figure 10. Bipolar (±5 V) Calibration

UNIPOLAR (0 V TO +2.5 V) CALIBRATION

The connections for the 0 V to +2.5 V input range calibration is shown in Figure 11. Figure 11 shows an example of how the offset error can be trimmed in front of the AD1671. The procedure for trimming the offset and gain errors is the same as for the unipolar 5 V range.

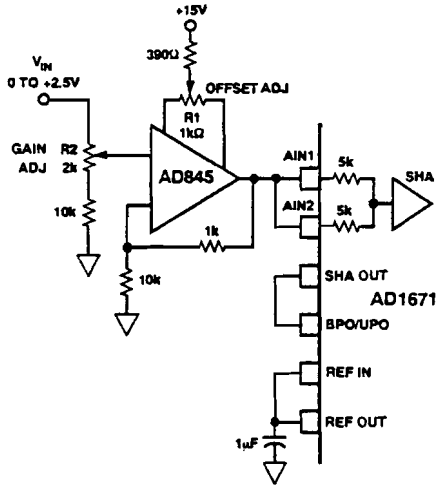


Figure 11. Unipolar (0 V to +2.5 V) Calibration

BIPOLAR (±2.5 V) CALIBRATION

The connections for the bipolar ±2.5 V input range is shown in Figure 12.

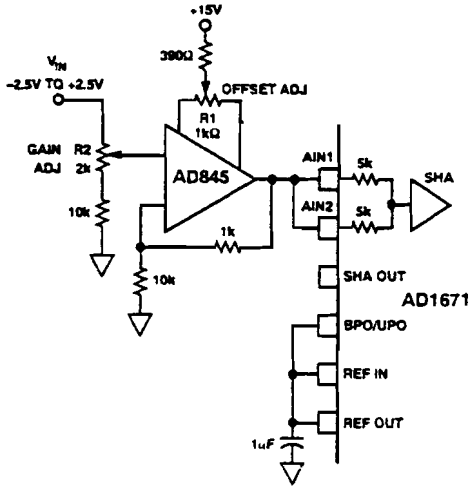


Figure 12. Bipolar (±2.5 V) Calibration

OUTPUT LATCHES

Figure 13 shows the AD1671 connected to the 74HC574 octal D-type edge-triggered latches with 3-state outputs. The latch can drive highly capacitive loads (i.e., bus lines, I/O ports) while maintaining the data signal integrity. The maximum setup and hold times of the 574 type latch must be less than 20 ns (t_{DD} and t_{SS} minimum). To satisfy the requirements of the 574 type latch the recommended logic families are S, AS, ALS, F or BCT. New data from the AD1671 is latched on the rising edge of the DAV (Pin 16) output pulse. Previous data can be latched by inverting the DAV output with a 7404 type inverter.

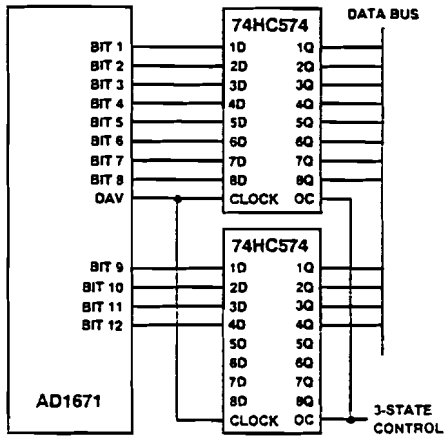


Figure 13. AD1671 to Output Latches

OUT OF RANGE

An out-of-range condition exists when the analog input voltage is beyond the input range (0 V to +2.5 V, 0 V to +5 V, ±2.5 V, ±5 V) of the converter. OTR (Pin 15) is set low when the analog input voltage is within the analog input range. OTR is set HIGH and will remain HIGH when the analog input voltage exceeds the input range by typically 1/2 LSB (OTR transition is tested to ±6 LSBs of accuracy) from the center of the ±full-scale output codes. OTR will remain HIGH until the analog input is within the input range and another conversion is completed. By logical ANDing OTR with the MSB and its complement, overrange high or underrange low conditions can be detected. Table II is a truth table for the over/under range circuit in Figure 14. Systems requiring programmable gain conditioning prior to the AD1671 can immediately detect an out-of-range condition, thus eliminating gain selection iterations.

Table II. Out-of-Range Truth Table

OTR	MSB	Analog Input Is
0	0	In Range
0	1	In Range
1	0	Underrange
1	1	Overrange

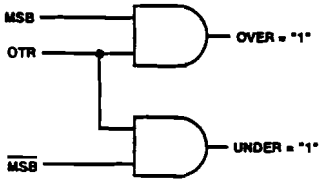


Figure 14. Overrange or Underrange Logic

Table III. Output Data Format

Input Range	Coding	Analog Input[1]	Digital Output	OTR[2]
0 V to +2.5 V	Straight Binary	≤ −0.0003 V	0000 0000 0000	1
		0 V	0000 0000 0000	0
		+2.5 V	1111 1111 1111	0
		≥ +2.5003 V	1111 1111 1111	1
0 V to +5 V	Straight Binary	≤ −0.0006 V	0000 0000 0000	1
		0 V	0000 0000 0000	0
		+5 V	1111 1111 1111	0
		≥ +5.0006 V	1111 1111 1111	1
−2.5 V to +2.5 V	Offset Binary	≤ −2.5006 V	0000 0000 0000	1
		−2.5 V	0000 0000 0000	0
		+2.5 V	1111 1111 1111	0
		≥ +2.4994 V	1111 1111 1111	1
−5 V to +5 V	Offset Binary	≤ −5.0012 V	0000 0000 0000	1
		−5 V	0000 0000 0000	0
		+5 V	1111 1111 1111	0
		≥ +4.9988 V	1111 1111 1111	1
−2.5 V to +2.5 V	Twos Complement (Using $\overline{MSB}$)	≤ −2.5006 V	1000 0000 0000	1
		−2.5 V	1000 0000 0000	0
		+2.5 V	0111 1111 1111	0
		≥ +2.4994 V	0111 1111 1111	1
−5 V to −5 V	Twos Complement (Using $\overline{MSB}$)	≤ −5.0012 V	1000 0000 0000	1
		−5 V	1000 0000 0000	0
		+5 V	0111 1111 1111	0
		≥ +4.9988 V	0111 1111 1111	1

NOTES
[1]Voltages listed are with offset and gain errors adjusted to zero.
[2]Typical performance.

OUTPUT DATA FORMAT

The AD1671 provides both MSB and $\overline{MSB}$ outputs, delivering data in positive true straight binary for unipolar input ranges and positive true offset binary or twos complement for bipolar input ranges. Straight binary coding is used for systems that accept positive-only signals. If straight binary coding is used with bipolar input signals, a 0 V input would result in a binary output of 2048. The application software would have to subtract 2048 to determine the true input voltage. Host registers typically perform math on signed integers and assume data is in that format. Twos complement format minimizes software overhead which is especially important in high speed data transfers, such as a DMA operation. The CPU is not bogged down performing data conversion steps, hence the total system throughput is increased.

OPTIONAL EXTERNAL REFERENCE

The AD1671 includes an on-board +2.5 V reference. The reference input pin (REF IN) can be connected to reference output pin (REF OUT) or a standard external +2.5 V reference can be selected to meet specific system requirements. Fast switching input dependent currents are modulated at the reference input. The reference input voltage can be held with the use of a capacitor. To prevent the AD1671's on-board reference from oscillating when not connected to REF IN, REF OUT must be connected to +5 V. It is possible to connect REF OUT to +5 V due to its output circuit implementation which shuts down the reference.

I_{LOGIC} vs. CONVERSION RATE

Figure 15 is the typical logic supply current vs. conversion rate for various capacitor loads on the digital outputs.

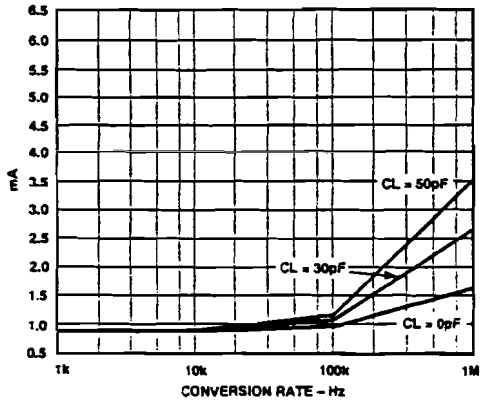


Figure 15. I_{LOGIC} vs. Conversion Rate for Various Capacitive Loads on the Digital Outputs

APPLICATIONS

AD1671 TO ADSP-2100A

Figure 16 demonstrates the AD1671 to ADSP-2100A interface. The 2100A with a clock frequency of 12.5 MHz can execute an instruction in one 80 ns cycle. The AD1671 is configured to perform continuous time sampling. The DAV output of the AD1671 is asserted at the end of each conversion. DAV can be used to latch the conversion result into the two 574 octal D-latches. The falling edge of the sampling clock is used to generate an interrupt (IRQ3) for the processor. Upon interrupt, the ADSP-2100A starts a data memory read by providing an address on the DMA bus. The decoded address generates OE for the latches and the processor reads their output over the DMA bus. The conversion result is read within a single processor cycle.

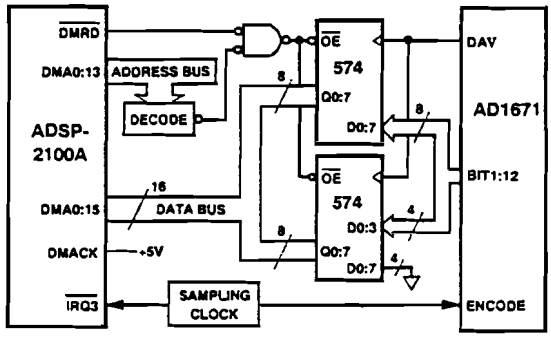


Figure 16. AD1671 to ADSP-2100A Interface

AD1671 TO ADSP-2101/2102

Figure 17 is identical to the 2100A interface except the sampling clock is used to generate an interrupt (IRQ2) for the processor. Upon interrupt the ADSP-2100A starts a data memory read by providing an address on the address (A) bus. The decode address generates OE for the D-latches and the processor reads their output over the Data (D) bus. Reading the conversion result is thus completed within a single processor cycle.

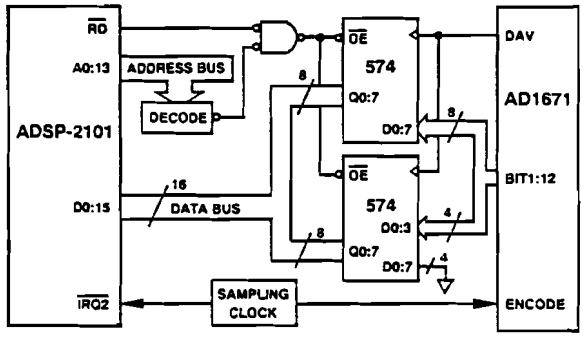
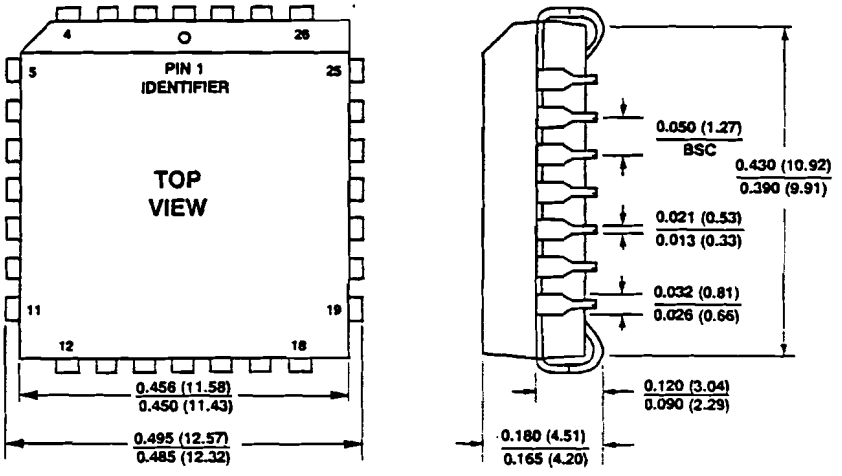


Figure 17. AD1671 to ADSP-2101/ADSP-2102 Interface

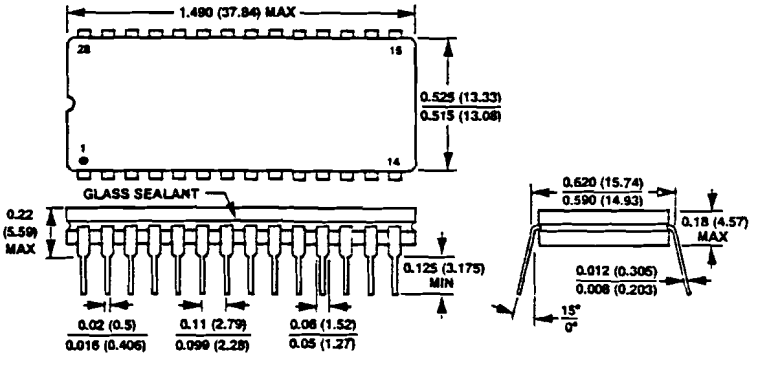
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead PLCC (P-28A) Package



28-Pin Cerdip (Q-28) Package



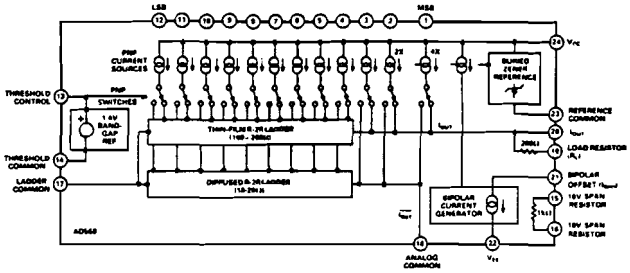
12-Bit Ultrahigh Speed Monolithic D/A Converter

AD568

FEATURES

- Ultrahigh Speed: Current Settling to 1LSB in 35ns
- High Stability Buried Zener Reference on Chip
- Monotonicity Guaranteed Over Temperature
- 10.24mA Full-Scale Output Suitable for Video Applications
- Integral and Differential Linearity Guaranteed Over Temperature
- 0.3" "Skinny DIP" Packaging
- Variable Threshold Allows TTL and CMOS Interface
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD568 is an ultrahigh-speed, 12-bit digital-to-analog converter (DAC) settling to 0.025% in 35ns. The monolithic device is fabricated using Analog Devices' Complementary Bipolar (CB) Process. This is a proprietary process featuring high-speed NPN and PNP devices on the same chip without the use of dielectric isolation or multichip hybrid techniques. The high speed of the AD568 is maintained by keeping impedance levels low enough to minimize the effects of parasitic circuit capacitances.

The DAC consists of 16 current sources configured to deliver a 10.24mA full-scale current. Multiple matched current sources and thin-film ladder techniques are combined to produce bit weighting. The DAC's output is a 10.24mA full scale (FS) for current output applications or a 1.024V FS unbuffered voltage output. Additionally, a 10.24V FS buffered output may be generated using an onboard 1kΩ span resistor with an external op amp. Bipolar ranges are accomplished by pin strapping.

Laser wafer trimming insures full 12-bit linearity. All grades of the AD568 are guaranteed monotonic over their full operating temperature range. Furthermore, the output resistance of the DAC is trimmed to 100Ω ± 1.0%. The gain temperature coefficient of the voltage output is 30ppm/°C max (K).

The AD568 is available in three performance grades. The AD568JQ and KQ are available in 24-pin cerdip (0.3") packages and are specified for operation from 0 to +70°C. The AD568SQ features operation from −55°C to +125°C and is also packaged in the hermetic 0.3" cerdip.

PRODUCT HIGHLIGHTS

1. The ultrafast settling time of the AD568 allows leading edge performance in waveform generation, graphics display and high-speed A/D conversion applications.
2. Pin strapping provides a variety of voltage and current output ranges for application versatility. Tight control of the absolute output current reduces trim requirements in externally-scaled applications.
3. Matched on-chip resistors can be used for precision scaling in high-speed A/D conversion circuits.
4. The digital inputs are compatible with TTL and +5V CMOS logic families.
5. Skinny DIP (0.3") packaging minimizes board space requirements and eases layout considerations.
6. The AD568 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD568/883B data sheet for detailed specifications.

AD568—SPECIFICATIONS (@ = +25°C, V_{CC}, V_{EE} = ±15V unless otherwise noted.)

Model	AD568J Min	AD568J Typ	AD568J Max	AD568K Min	AD568K Typ	AD568K Max	AD568S Min	AD568S Typ	AD568S Max	Units
RESOLUTION	12			12			12			Bits
ACCURACY[1]										
Linearity	−1/2		+1/2	−1/4		+1/4	−1/2		+1/2	LSB
T_{min} to T_{max}	−3/4		+3/4	−1/2		+1/2	−3/4		+3/4	LSB
Differential Nonlinearity	−1		+1	−1/2		+1/2	−1		+1	LSB
T_{min} to T_{max}	−1		+1	−1		+1	−1		−1	LSB
Monotonicity	GUARANTEED OVER RATED SPECIFICATION TEMPERATURE RANGE									
Unipolar Offset	−0.2		+0.2	*		*	*		*	% of FSR
Bipolar Offset	−1.0		+1.0	*		*	*		*	% of FSR
Bipolar Zero	−0.2		+0.2	*		*	*		*	% of FSR
Gain Error	−1.0		+1.0	*		*	*		*	% of FSR
TEMPERATURE COEFFICIENTS[2]										
Unipolar Offset	−5		+5	−3		+3	−5		+5	ppm of FSR/°C
Bipolar Offset	−30		+30	−20		+20	−30		+30	ppm of FSR/°C
Bipolar Zero	−15		+15	*		*	*		*	ppm of FSR/°C
Gain Drift	−50		+50	−30		+30	−50		+50	ppm of FSR/°C
Gain Drift (I_{OUT})	−150		+150	*		*	*		*	ppm of FSR/°C
DATA INPUTS										
Logic Levels (T_{min} to T_{max})										
V_{IH}	2.0		7.0	*		*	*		*	V
V_{IL}	0.0		0.8	*		*	*		*	V
Logic Currents (T_{min} to T_{max})										
I_{IH}	−10	0	+10	*	*	*	*	*	*	µA
I_{IL}	−0.5	−60	−100	*	*	*	*	−100	−200	µA
V_{TH} Pin Voltage		1.4			*			*		V
CODING	BINARY, OFFSET BINARY									
CURRENT OUTPUT RANGES	0 to 10.24, ±5.12									mA
VOLTAGE OUTPUT RANGES	0 to 1.024, ±0.512									V
COMPLIANCE VOLTAGE	−2		+1.2	*		*	*		*	V
OUTPUT RESISTANCE										
Exclusive of R_L	160	200	240		*			*		Ω
Inclusive of R_L	99	100	101		*			*		Ω
SETTLING TIME										
Current to										
±0.025%		35			*			*		ns to 0.025% of FSR
±0.1%		23			*			*		ns to 0.1% of FSR
Voltage										
50Ω Load[3], 0.512V p-p,										
to 0.025%		37			*			*		ns to 0.025% of FSR
to 0.1%		25			*			*		ns to 0.1% of FSR
to 1%		18			*			*		ns to 1% of FSR
75Ω Load[3], 0.768V p-p,										
to 0.025%		40			*			*		ns to 0.025% of FSR
to 0.1%		25			*			*		ns to 0.1% of FSR
to 1%		20			*			*		ns to 1% of FSR
100Ω (Internal R_L)[3], 1.024V p-p,										
to 0.025%		50			*			*		ns to 0.025% of FSR
to 0.1%		38			*			*		ns to 0.1% of FSR
to 1%		24			*			*		ns to 1% of FSR
Glitch Impulse[4]		350			*			*		pV-sec
Peak Amplitude		15			*			*		% of FSR
FULL-SCALE TRANSITION[5]										
10% to 90% Rise Time		11			*			*		ns
90% to 10% Fall Time		11			*			*		ns
POWER REQUIREMENTS										
+13.5V to +16.5V		27	32		*	*		*	*	mA
−13.5V to −16.5V		−7	−8		*	*		*	*	mA
Power Dissipation		525	625		*	*		*	*	mW
PSRR			0.05			*			*	% of FSR/V
TEMPERATURE RANGE										
Rated Specification[2]	0		70	0		70	−55		+125	°C
Storage	−65		+150	*		*	*		*	°C

NOTES
*Same as AD568J.
[1]Measured in $I_{IN,T}$ mode.
[2]Measured in V_{OUT} mode, unless otherwise specified. See text for further information.
[3]Total Resistance. Refer to Figure 3.
[4]At the major carry, driven by HCMOS logic. See text for further explanation.
[5]Measured in V_{OUT} mode.

Specifications shown in boldface are tested on all production units at final electrical test.
Specifications subject to change without notice.

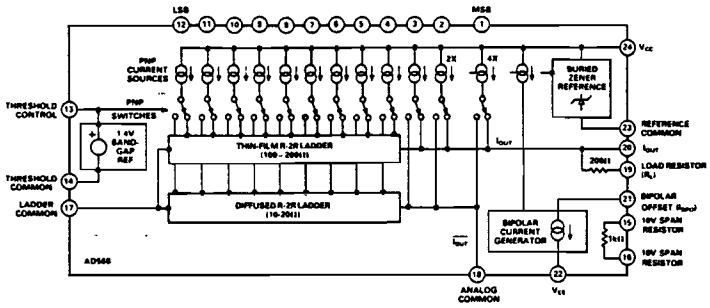
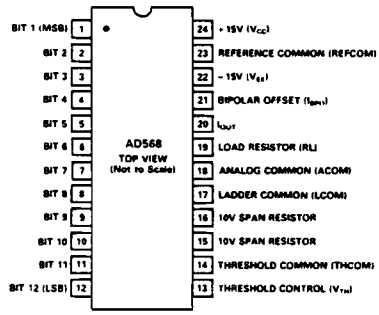


Figure 1. Functional Block Diagram

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS*

V_{CC} to REFCOM	0V to +18V
V_{EE} to REFCOM	0V to −18V
REFCOM to LCOM	+100mV to −10V
ACOM to LCOM	±100mV
THCOM to LCOM	±500mV
SPANs to LCOM	±12V
I_{BPO} to LCOM	±5V
I_{OUT} to LCOM	−5V to V_{TH}
Digital Inputs to THCOM	−500mV to +7.0V
Voltage Across Span Resistor	12V
V_{TH} to THCOM	−0.7V to +1.4V
Logic Threshold Control Input Current	5mA
Power Dissipation	1000mW
Storage Temperature Range	
Q (Cerdip) Package	−65°C to +150°C
Junction Temperature	175°C
Thermal Resistance	
θ_{ja}	75°C/W
θ_{jc}	25°C/W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model[1]	Package Option[2]	Temperature Range °C	Linearity Error Max. @ 25°C	Voltage Gain T.C. Max ppm/°C
AD568JQ	24-Lead Cerdip (Q-24)	0 to +70	±1/2	±50
AD568KQ	24-Lead Cerdip (Q-24)	0 to +70	±1/4	±30
AD568SQ	24-Lead Cerdip (Q-24)	−55 to +125	±1/2	±50

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD568/883B data sheet.
[2]Q = Cerdip. For outline information see Package Information section.

Definitions

LINEARITY ERROR (also called INTEGRAL NON-LINEARITY OR INL): Analog Devices defines linearity error as the maximum deviation of the actual analog output from the ideal output (a straight line drawn from 0 to FS) for any bit combination expressed in multiples of 1LSB. The AD568 is laser trimmed to 1/4LSB (0.006% of FS) maximum linearity error at +25°C for the K version and 1/2LSB for the J and S versions.

DIFFERENTIAL LINEARITY ERROR (also called DIFFERENTIAL NONLINEARITY or DNL): DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. Monotonic behavior requires that the differential linearity error not exceed 1LSB in the negative direction.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases.

UNIPOLAR OFFSET ERROR: The deviation of the analog output from the ideal (0V or 0mA) when the inputs are set to all 0s is called unipolar offset error.

BIPOLAR OFFSET ERROR: The deviation of the analog output from the ideal (negative half-scale) when the inputs are set to all 0s is called bipolar offset error.

BIPOLAR ZERO ERROR: The deviation of the analog output from the ideal half-scale output of 0V (or 0mA) for bipolar mode when only the MSB is on (100.....00) is called bipolar zero error.

GAIN ERROR: The difference between the ideal and actual output span of FS −1LSB, expressed in % of FS, or LSB, when all bits are on.

GLITCH IMPULSE: Asymmetrical switching times in a DAC give rise to undesired output transients which are quantified by their glitch impulse. It is specified as the net area of the glitch in nV-sec or pA-sec.

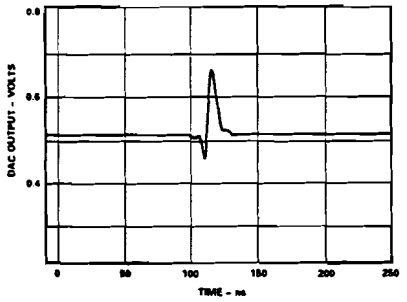


Figure 2. AD568 Glitch Impulse

COMPLIANCE VOLTAGE: The range of allowable voltage at the output of a current-output DAC which will not degrade the accuracy of the output current.

SETTLING TIME: The time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition.

Connecting the AD568

UNBUFFERED VOLTAGE OUTPUT

Unipolar Configuration

Figure 3 shows the AD568 configured to provide a unipolar 0 to +1.024V output range. In this mode, the bipolar offset terminal, Pin 21, should be grounded if not used for offset trimming.

The nominal output impedance of the AD568 with Pin 19 grounded has been trimmed to 100Ω, ± 1%. Other output impedances can be generated with an external resistor, R_{EXT}, between Pins 19 and 20. An R_{EXT} equalling 300Ω will yield a total output resistance of 75Ω, while an R_{EXT} of 100Ω will provide 50Ω of output resistance. Note that since the full-scale output current of the DAC remains 10.24mA, changing the load impedance changes the unbuffered output voltage accordingly. Settling time and full-scale range characteristics for these load impedances are provided in the specifications table.

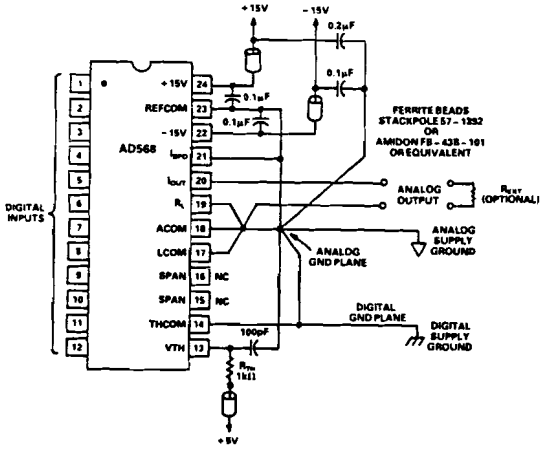


Figure 3. Unipolar Output Unbuffered 0 to +1.024V

Bipolar Configuration

Figure 4 shows the connection scheme used to provide a bipolar output voltage range of 1.024V. The bipolar offset (−0.512V) occurs when all bits are OFF (00 . . . 00), bipolar zero (0V)

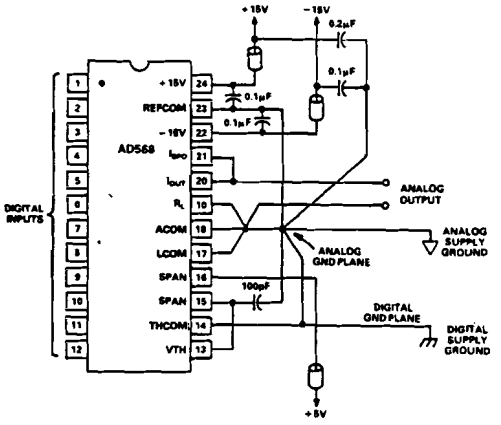


Figure 4. Bipolar Output Unbuffered ±0.512V

occurs when the MSB is ON with all other bits OFF (10 . . . 00), and full-scale minus 1LSB (0.51175V) is generated when all bits are ON (11 . . . 11). Figure 5 shows an optional bipolar mode with a 2.048V range. The scale factor in this mode will not be as accurate as the configuration shown in Figure 4, because the laser-trimmed resistor R_L is not used.

Figure 4 also demonstrates how the internal span resistor may be used to bias the V_{TH} pin (Pin 13) from a 5V supply. This eliminates the requirement for an external R_{TH} in applications that do not require the precision span resistor.

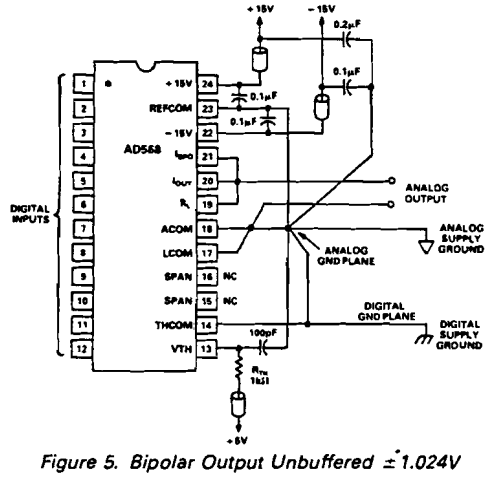


Figure 5. Bipolar Output Unbuffered ±1.024V

Optional Gain and Zero Adjustment

The gain and offset are laser trimmed to minimize their effects on circuit performance. However, in some applications, it may be desirable to externally reduce these errors further. In those cases, the following procedures are suggested.

UNIPOLAR MODE: (Refer to Figure 6)

Step 1 – Set all bits (BIT 1–BIT 12) to Logic "0" (OFF) – note the output voltage. This is the offset error.

Step 2 – Set all bits to Logic "1" (ON). Adjust the gain trim resistor so that the output voltage is equal to the desired full scale minus 1LSB plus the offset error measured in step 1.

Step 3 – Reset all bits to Logic "0" (OFF). Adjust the offset trim resistor for 0V output.

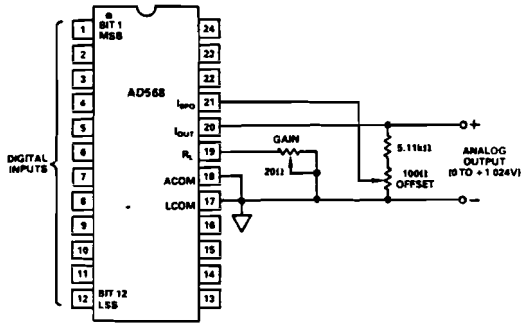


Figure 6. Unbuffered Unipolar Gain and Zero Adjust

BIPOLAR MODE (Refer to Figure 7)
Step 1 – Set bits to offset binary "zero" (10 . . . 00). Adjust the zero resistor to produce 0V at the DAC output. This removes the bipolar zero error.

Step 2 – Set all bits to Logic "1" (ON). Adjust gain trim resistor so the output voltage is equal to the desired full-scale minus 1LSB.

Step 3 – (Optional) If precise trimming of the bipolar offset is preferred to trimming of bipolar zero: set all bits to Logic "0" (OFF). Trim the zero resistor to produce the desired negative full scale at the DAC output.
Note: this may slightly compromise the bipolar zero trim.

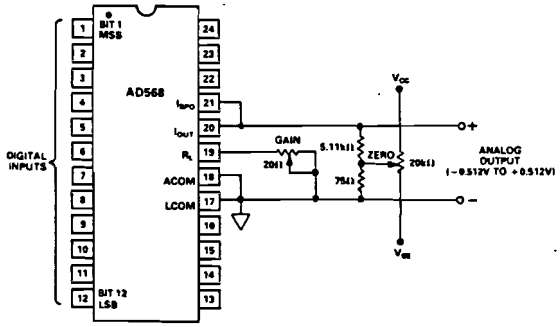


Figure 7. Bipolar Unbuffered Gain and Zero Adjust

BUFFERED VOLTAGE OUTPUT

For full-scale outputs of greater than 1V, some type of external buffer amplifier is required. The AD840 fills this requirement perfectly, settling to 0.025% from a 10V full-scale step in less than 100ns.

A 1kΩ span resistor has been provided on chip for use as a feedback resistor in buffered applications. Using R_{SPAN} (Pins 15, 16) introduces a 100mW code-dependent power source onto the chip which may generate a slight degradation in linearity. Maximum linearity performance can be realized by using an external span resistor.

Unipolar Inverting Configuration

Figure 8 shows the connections for producing a −10.24V full-scale swing. This configuration uses the AD568 in the current output mode into a summing junction at the inverting input terminal of the external op amp. With the load resistor R_L grounded, the DAC has an output impedance of 100Ω. This produces a noise gain of 11 from the noninverting terminal of the op amp, and hence, satisfies the stability criterion of the AD840 (stable at a gain of 10). The addition of a 5pF compensation capacitor across the 1kΩ feedback resistor produces optimal settling. Lower noise gain can be achieved by connecting R_L to I_{OUT}, increasing the DAC output impedance to approximately 200Ω, and reducing the noise gain to 6 (illustrated in Figure 9). While the output in this configuration will feature improved noise performance, it is somewhat less stable and may suffer from ringing. The compensation capacitance should be increased to 7pF to maintain stability at this reduced gain.

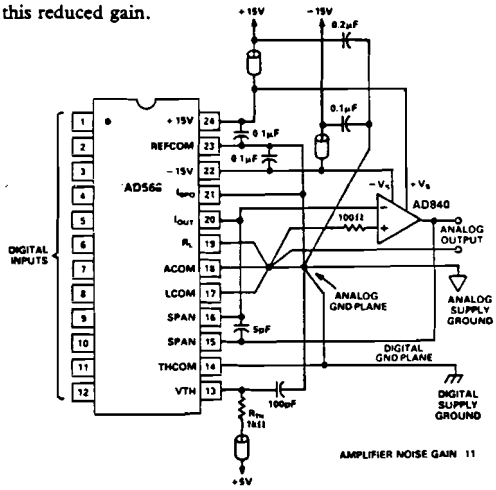


Figure 8. Unipolar Output Buffered 0 to −10.24V

Bipolar Inverting Configuration

Figure 9 illustrates the implementation of a +5.12V to −5.12V bipolar range, achieved by connecting the bipolar offset current, I_{BPO}, to the summing junction of the external amplifier. Note that since the amplifier is providing an inversion, the full-scale output voltage is −5.12V, while the bipolar offset voltage (all bits OFF) is +5.12V at the amplifier output.

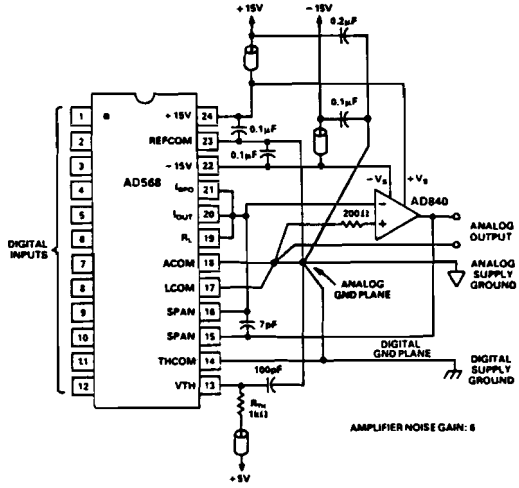


Figure 9. Bipolar Output Buffered ±5.12V

Noninverting Configuration

If a positive full-scale output voltage is required, it can be implemented using the AD568 in the unbuffered voltage output mode followed by the AD840 in a noninverting configuration (Figure 10). The noise gain of this topology is 10, requiring only 5pF across the feedback resistor to optimize settling.

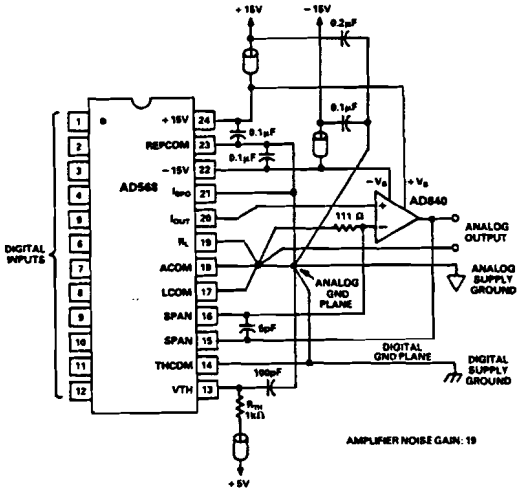


Figure 10. Unipolar Output Buffered 0 to +10.24V

Guidelines for Using the AD568

The designer who seeks to combine high speed with high precision faces a challenging design environment. Where tens of milliamperes are involved, fractions of an ohm of misplaced impedance can generate several LSBs of error. Increasing bandwidths make formerly negligible parasitic capacitances and inductances significant. As system performance reaches and exceeds that of the measurement equipment, time-honored test methods may no longer be trustworthy. The DAC's placement on the boundary between the analog and digital domains introduces additional concerns. Proper RF techniques must be used in board design, device selection, supply bypassing, grounding, and measurement if optimal performance is to be realized. The AD568 has been configured to be relatively easy to use, even in some of the more treacherous applications. The device characteristics shown in this datasheet are readily achievable if proper attention is paid to the details. Since a solid understanding of the circuit involved is one of the designer's best weapons against the difficulties of RF design, the following sections provide illustrations, explanations, examples, and suggestions to facilitate successful design with the AD568.

Current Output vs. Voltage Output

As indicated in Figures 3 through 10, the AD568 has been designed to operate in several different modes depending on the external circuit configuration. While these modes may be categorized by many different schemes, one of the most important distinctions to be made is whether the DAC is to be used to generate an output voltage or an output current. In the current output mode, the DAC output (Pin 20) is tied to some type of summing junction, and the current flowing from the DAC into this summing junction is sensed (e.g., Figures 8 and 9). In this mode, the DAC output scale is insensitive to whether the load resistor, R_L, is shorted (Pin 19 connected to Pin 20), or grounded (Pin 19 connected to Pin 18). However, this does affect the output impedance of the DAC current and may have a significant impact on the noise gain of the external circuitry. In the voltage output mode, the DAC's output current flows through its own internal impedance (perhaps in parallel with an external impedance) to generate a voltage, as in Figures 3, 4, 5, and 10. In this case, the DAC output scale is directly dependent on the load impedance. The temperature coefficient of the AD568's internal reference is trimmed in such a way that the drift of the DAC output in the voltage output mode is centered on zero. The current output of the DAC will have an additional drift factor corresponding to the absolute temperature coefficient of the internal thin-film resistors. This additional drift may be removed by judicious placement of the 1kΩ span resistor in the signal path. For example, in Figures 8 and 9, the current flowing from the DAC into the summing junction could suffer from as much as 150ppm/°C of thermal drift. However, since this current flows through the internal span resistor (Pins 15 and 16) which has a temperature coefficient that matches the DAC ladder resistors, this drift factor is compensated and the buffered voltage at the amplifier output will be within specified limits for the voltage output mode.

Output Voltage Compliance

The AD568 has a typical output compliance range of +1.2V to −2.0V (with respect to the LCOM Pin). The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, as shown in Figure 11, there is an equivalent output impedance of 200Ω in parallel with 15pF at the output terminal which produces an equivalent error current if the voltage deviates from the ladder common. This is a linear effect which does not change with input code. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown resulting in nonlinear performance. The positive compliance limit is not affected by the positive power supply, but is a function of output current and the logic threshold voltage at V_{TH}, Pin 13.

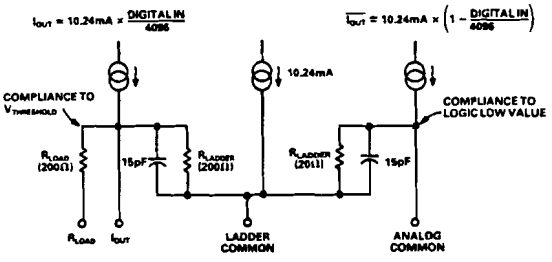


Figure 11. Equivalent Output

Digital Input Considerations

The AD568 uses a standard positive true straight binary code for unipolar outputs (all 1s full-scale output), and an offset binary code for bipolar output ranges. In the bipolar mode, with all 0s on the inputs, the output will go to negative full scale; with 111 . . . 11, the output will go to positive full scale less 1LSB; and with 100 . . 00 (only the MSB on), the output will go to zero.

The threshold of the digital inputs is set at 1.4V and does not vary with supply voltage. This is provided by a bandgap reference generator, which requires approximately 3mA of bias current achieved by tying R_{TH} to any $+V_L$ supply where

$$R_{TH} = \left(\frac{+V_L - 1.4V}{3mA}\right).$$

The input lines operate with small input currents to easily achieve interface with unbuffered CMOS logic. The digital input signals to the DAC should be isolated from the analog output as much as possible. To minimize undershoot, ringing, and possible digital feedthrough noise, the interconnect distances to the DAC inputs should be kept as short as possible. Termination resistors may improve performance if the digital lines become too long. The digital input should be free from large glitches and ringing and have maximum 10% to 90% rise and fall times of 5ns. Figure 12 shows the equivalent digital input circuit of the AD568.

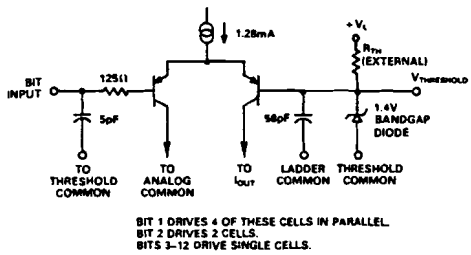


Figure 12. Equivalent Digital Input

Due to the high-speed nature of the AD568, it is recommended that high-speed logic families such as Schottky TTL, high-speed CMOS, or the new lines of FAST* TTL be used exclusively. Table I shows how DAC performance can vary depending on the driving logic used. As this table indicates, STTL, HCMOS, and FAST represent the most viable families for driving the AD568.

DAC PERFORMANCE VS. DRIVE LOGIC[1]

Logic Family	10-90% DAC Rise Time[2]	DAC SETTLING TIME[2,3] 1%	0.1%	0.025%	Glitch[4] Impulse	Maximum Glitch Excursion
TTL	11ns	18ns	34ns	50ns	2.5nV-s	240mV
LSTTL	11ns	28ns	46ns	80ns	950pV-s	160mV
STTL	9.5ns	16ns	33ns	50ns	850pV-s	150mV
HCMOS	11ns	24ns	38ns	50ns	350pV-s	115mV
FAST*	12ns	16ns	36ns	42ns	1.0nV-s	250mV

[1]All values typical, taken in test fixture diagrammed in Figure 13.
[2]Measurements are made for a 1V full-scale step into 100ΩDAC load resistance.
[3]Settling time is measured from the time the digital input crosses the threshold voltage (1.4V) to when the output is within the specified range of its final value.
[4]The worst case glitch impulse, measured on the major carry. DAC full scale is 1V.

Table I.

The variations in settling times can be attributed to differences in the rise time and current driving capabilities of the various families. Differences in the glitch impulse are predominantly dependent upon the variation in data skew. Variations in these specs occur not only between logic families, but also between different gates and latches within the same family. When selecting a gate to drive the AD568 logic input, pay particular attention to the propagation delay time specs: t_{PLH} and t_{PHL}. Selecting the smallest delays possible will help to minimize the settling time, while selection of gates where t_{PLH} and t_{PHL} are closely matched to one another will minimize the glitch impulse resulting from data skew. Of the common latches, the 74374 octal flip-flop provides the best performance in this area for many of the logic families mentioned above.

*FAST is a registered trademark of Fairchild Camera and Instrumentation Corporation.

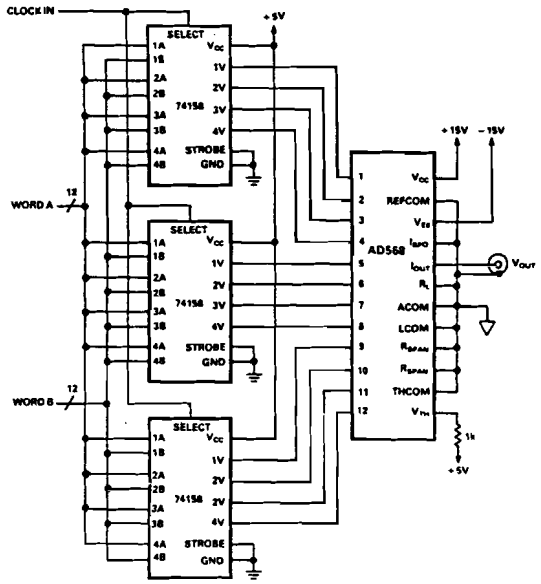


Figure 13. Test Setup for Glitch Impulse and Settling Time Measurements

Settling Time Considerations

As can be seen from Table I and the specifications page, the settling time of the AD568 is application dependent. The fastest settling is achieved in the current-output mode, since the voltage-output mode requires the output capacitance to be charged to the appropriate voltage. The DAC's relatively large output current helps to minimize this effect, but settling-time sensitive applications should avoid any unnecessary parasitic capacitance at the output node of voltage output configurations. Direct measurement of the fine scale DAC settling time, even in the voltage output mode, is extremely tricky: analog scope front ends are generally incapable of recovering from overdrive quickly enough to give an accurate settling representation. The plot shown in Figure 14 was obtained using Data Precision's 640 16-bit sampling head, which features the quick overdrive recovery characteristic of sampling approaches combined with high accuracy and relatively small thermal tail.

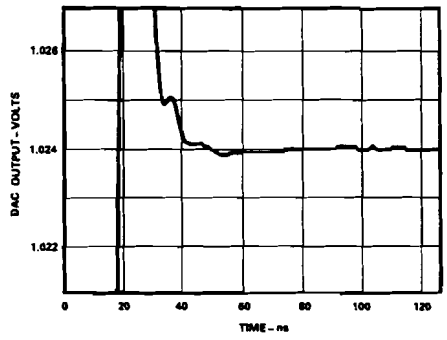


Figure 14. Zero to Full-Scale Settling

Glitch Considerations

In many high-speed DAC applications, glitch performance is a critical specification. In a conventional DAC architecture such as the AD568 there are two basic glitch mechanisms: data skew and digital feedthrough. A thorough understanding of these sources can help the user to minimize glitch in any application.

DIGITAL FEEDTHROUGH – As with any converter product, a high-speed digital-to-analog converter is forced to exist on the frontier between the noisy environment of high-speed digital logic and the sensitive analog domain. The problems of this interfacing are particularly acute when demands of high speed (greater than 10MHz switching times) and high precision (12 bits or more) are combined. No amount of design effort can perfectly isolate the analog portions of a DAC from the spectral components of a digital input signal with a 2ns risetime. Inevitably, once this digital signal is brought onto the chip, some of its higher frequency components will find their way to the sensitive analog nodes, producing a digital feedthrough glitch. To minimize the exposure to this effect, the AD568 has intentionally omitted the on-board latches that have been included in many slower DACs. This not only reduces the overall level of digital activity on chip, it also avoids bringing a latch clock pulse on board, whose opposite edge inevitably produces a substantial glitch, even when the DAC is not supposed to be changing codes. Another path for digital noise to find its way onto a converter chip is through the reference input pin. The completely internal reference featured in the AD568 eliminates this noise input, providing a greater degree of signal integrity in the analog portions of the chip.

DATA SKEW – The AD568, like many of its slower predecessors, essentially uses each digital input line to switch a separate, weighted current to either the output (I_{OUT}) or some other node (ANALOG COM). If the input bits are not changed simultaneously, or if the different DAC bits switch at different speeds, then the DAC output current will momentarily take on some incorrect value. This effect is particularly troublesome at the "carry points", where the DAC output is to change by only one LSB, but several of the larger current sources must be switched to realize this change. Data skew can allow the DAC output to move a substantial amount towards full scale or zero (depending upon the direction of the skew) when only a small transition is desired. Great care was taken in the design and layout of the AD568 to ensure that switching times of the DAC switches are symmetrical and that the length of the input data lines are short and well matched. The glitch-sensitive user should be equally diligent about minimizing the data skew at the AD568's inputs, particularly for the 4 or 5 most significant bits. This can be achieved by using the proper logic family and gate to drive the DAC, and keeping the interconnect lines between the logic outputs and the DAC inputs as short and as well matched as possible, particularly for the most significant bits. The top 6 bits should be driven from the same latch chip if latches are used.

Glitch Reduction Schemes

BIT-DESKEWING – Even carefully laid-out boards using the proper driving logic may suffer from some degree of data-skew induced glitch. One common approach to reducing this effect is to add some appropriate capacitance (usually several pF) to each of the 2 or 3 most significant bits. The exact value of each capacitor for a given application should be determined experimentally, as it will be dependent on circuit board layout and the type of driving logic used. Table II presents a few examples of how the glitch impulse may be reduced through passive deskewing.

BIT DELAY GLITCH REDUCTION EXAMPLES[1]

Logic Family	Gate	Uncompensated Glitch	Compensation Used	Compensated Glitch
HCMOS	74157	350pV-s	C2 = 5pF	250pV-s
STTL	74158	850pV-s	R1 = 50Ω, C1 = 7pF	600pV-s

NOTE
[1]Measurements were made using a modified version of the fixture shown in Figure 13, with resistors and capacitors placed as shown in Figure 15. Resistance and capacitance values were set to zero except as noted.

Table II.

As Figure 15 indicates, in some cases it may prove useful to place a few hundred ohms of series resistance in the input line to enhance the delay effect. This approach also helps to reduce some of the digital feedthrough glitch, as the higher frequency spectral components are being filtered out of the most significant bits' digital inputs.

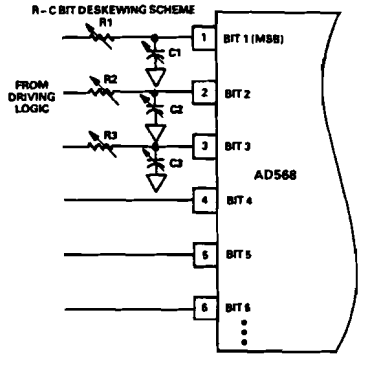


Figure 15. R–C Bit Deskewing Scheme

THRESHOLD SHIFT – It is also possible to reduce the data skew by shifting the level of logic voltage threshold, V_{TH} (Pin 13). This can be readily accomplished by inserting some resistance between the THRESHOLD COM pin (Pin 14) and ground, as in Figure 16. To generate threshold voltages below 1.4V, Pin 13 may be directly driven with a voltage source, leaving Pin 14 tied to the ground plane. As Note 2 in Table III indicates, lowering the threshold voltage may reduce output voltage compliance below the specified limits, which may be of concern in an unbuffered voltage output topology.

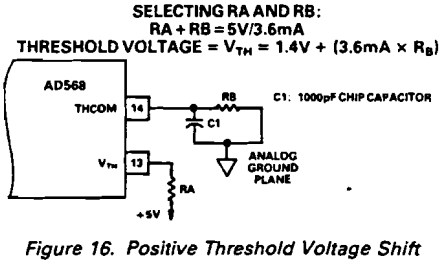


Figure 16. Positive Threshold Voltage Shift

Table III shows the glitch reduction achieved by shifting the threshold voltage for HCMOS, STTL, and FAST logic.

THRESHOLD SHIFT FOR GLITCH IMPROVEMENT[1]

Logic Family	Gate	Uncompensated Glitch	Modified Threshold[2]	Resulting Glitch
HCMOS	74HC158	350pV-s	1.7V	150pV-s
STTL	74S158	850pV-s	1.0V	200pV-s
FAST	74F158	1000pV-s	1.3V	480pV-s

NOTES
[1]Measurements made on a modified version of the circuit shown in Figure 13, with a 1V full scale.
[2]Use care in any scheme that lowers the threshold voltage since the output voltage compliance of the DAC is sensitive to this voltage. If the DAC is to be operated in the voltage output mode, it is strongly suggested that the threshold voltage be set at least 200mV above the output voltage full scale.

Table III.

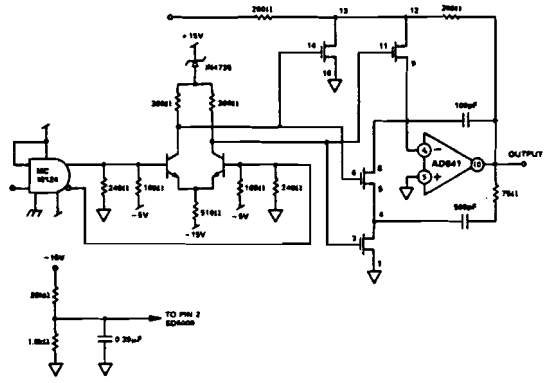


Figure 17. High Performance Deglitcher

Deglitching

Some applications may prove so sensitive to glitch impulse that reduction of glitch impulse by an order of magnitude or more is required. In order to realize glitch impulses this low, some sort of sample-and-hold amplifier (SHA)-based deglitching scheme must be used.

There are high-speed SHAs available with specifications sufficient to deglitch the AD568, however most are hybrid in design at costs which can be prohibitive. A high performance, low cost alternative shown in Figure 17 is a discrete SHA utilizing a high-speed monolithic op amp and high-speed DMOS FET switches.

This SHA circuit uses the inverting integrator architecture. The AD841 operational amplifier used (300MHz gain bandwidth product) is fabricated on the same high-speed process as the AD568. The time constant formed by the 200Ω resistor and the 100pF capacitor determines the acquisition time and also band limits the output signal to eliminate slew induced distortion.

A discrete drive circuit is used to achieve the best performance from the SD5000 quad DMOS switch. This switch driving cell is composed of MPS571 RF npn transistors and an MC10124 TTL to ECL translator. Using this technique provides both high speed and highly symmetrical drive signals for the SD5000 switches. The switches are arranged in a single-throw double-pole (SPDT) configuration. The 360pF "flyback" capacitor is switched to the op amp summing junction during the hold mode to keep switching transients from feeding to the output. This capacitor is grounded during sample mode to minimize its effect on acquisition time.

Circuit layout for a high speed SHA is almost as critical as the design itself. Figure 17 shows a recommended layout of the deglitching cell for a double sided printed circuit board. The layout is very compact with care taken that all critical signal paths are short.

Grounding Rules

The AD568 brings out separate reference, output, and digital power grounds. This allows for optimum management of signal ground currents for low noise and high-speed settling performance. The separate ground returns are provided to minimize changes in current flow in the analog signal paths. In this way, logic return currents are not summed into the same return path with the analog signals.

It is important to understand which supply and signal currents are flowing in which grounds so that they may be returned to the proper power supply in the best possible way.

The majority of the current that flows into the V_{CC} supply (Pin 24) flows out (depending on the DAC input code) either the ANALOG COMMON (Pin 18), the LADDER COMMON (Pin 17), and/or I_{OUT} (Pin 20).

The current in the LADDER COMMON is configured to be code independent when the output current is being summed into a virtual ground. If I_{OUT} is operated into its own output impedance (or in any unbuffered voltage output mode) the current in LADDER COMMON will become partially code dependent.

The current in the ANALOG COMMON (Pin 18) is an approximate complement of the current in I_{OUT}, i.e., zero when the DAC is at full scale and approximately 10mA at zero input code.

A relatively constant current (not code dependent) flows out the REFERENCE COMMON (Pin 23).

The current flowing out of the V_{EE} supply (Pin 22) comes from a combination of reference ground and BIPOLAR OFFSET (Pin 21). The plus and minus 15V supplies are decoupled to the REFERENCE COMMON.

The ground side of the load resistor R_L, ANALOG COMMON and LADDER COMMON should be tied together as close to the package pins as possible. The analog output voltage is then referred to this node and thus it becomes the "high quality" ground for the AD568. The REFERENCE COMMON (and Bipolar offset when not used), should also be connected to this node.

All of the current that flows into the V_{TH} terminal (Pin 13) from the resistor tied to the 5V logic supply (or other convenient positive supply) flows out the THRESHOLD COMMON (Pin 14). This ground pin should be returned directly to the digital ground plane on its own individual line.

The + 5V logic supply should be decoupled to the THRESHOLD COMMON.

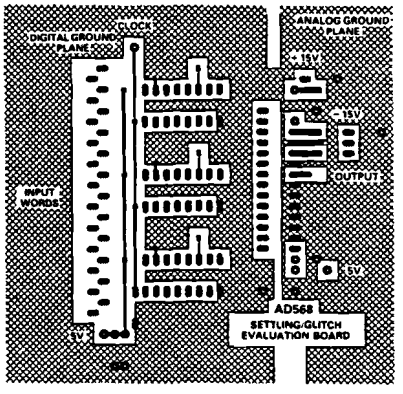
Because the V_{TH} pin is connected directly to the DAC switches it should be decoupled to the analog output signal common.

In order to preserve proper operation of the DAC switches, the digital and analog grounds need to eventually be tied together. This connection between the ground planes should be made within 1/2" of the DAC.

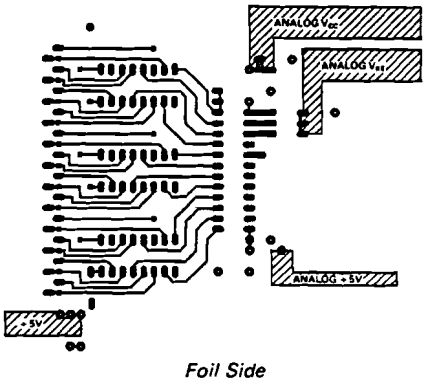
The Use of Ground and Power Planes

If used properly, ground planes can perform a myriad of functions on high-speed circuit boards: bypassing, shielding, current transport, etc. In mixed signal design, the analog and digital portions of the board should be distinct from one another, with the analog ground plane covering analog signal traces and the digital ground plane confined to areas covering digital interconnect.

The two ground planes should be connected at or near the DAC. Care should be taken to insure that the ground plane is uninterrupted over crucial signal paths. On the digital side, this includes the digital input lines running to the DAC and any clock lines. On the analog side, this includes the DAC output signal as well as the supply feeders. The use of wide runs or planes in the routing of power lines is also recommended. This serves the dual function of providing a low series impedance power supply to the part as well as providing some "free" capacitive decoupling to the appropriate ground plane. Figure 18 illustrates the PC board used for the circuit shown in Figure 13. This design was constructed on a simple two-layer board and illustrates many of the points discussed above. If more layers of interconnect are available, even better results are possible.



Component Side



Foil Side

Figure 18. Printed Circuit Board Layout

Using The Right Bypass Capacitors

Probably the most important external components associated with any high-speed design are the capacitors used to bypass the power supplies. Both selection and placement of these capacitors can be critical and, to a large extent, dependent upon the specifics of the system configurations. The dominant consideration in selection of bypass capacitors for the AD568 is minimization of series resistance and inductance. Many capacitors will begin to look inductive at 20MHz and above, the very frequencies we are most interested in bypassing. Ceramic and film-type capacitors generally feature lower series inductance than tantalum or electrolytic types. A few general rules are of universal use when approaching the problem of bypassing:

Bypass capacitors should be installed on the printed circuit board with the shortest possible leads consistent with reliable construction. This helps to minimize series inductance in the leads. Chip capacitors are optimal in this respect.

Some series inductance between the DAC supply pins and the power supply plane often helps to filter out high-frequency power supply noise. This inductance can be generated using a small ferrite bead.

High-Speed Interconnect and Routing

It is essential that care be taken in the signal and power ground circuits to avoid inducing extraneous voltage drops in the signal ground paths. It is suggested that all connections be short and direct, and as physically close to the package as possible, so that the length of any conduction path shared by external components will be minimized. When runs exceed an inch or so in length, some type of termination resistor may be required. The necessity and value of this resistor will be dependent upon the logic family used.

For maximum ac performance, the DAC should be mounted directly to the circuit board; sockets should not be used as they introduce unwanted capacitive coupling between adjacent pins of the device.

Applications

1μs, 12-BIT SUCCESSIVE APPROXIMATION A/D CONVERTER

The AD568's unique combination of high speed and true 12-bit accuracy can be used to construct a 12-bit SAR-type A/D converter with a sub-μs conversion time. Figure 19 shows the configuration used for this application. A negative analog input voltage is converted into current and brought into a summing junction with the DAC current. This summing junction is bidirectionally clamped with two Shottky diodes to limit its voltage excursion from ground. This voltage is differentially amplified and passed to a high-speed comparator. The comparator output is latched and fed back to the successive approximation register, which is then clocked to generate the next set of codes for the DAC.

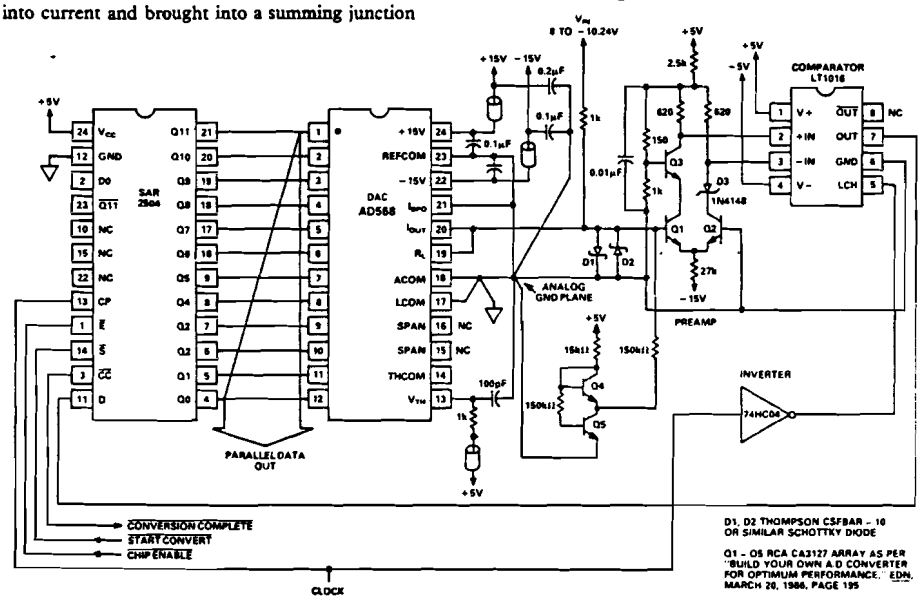


Figure 19. AD568 1μs Successive Approximation A/D Application

Circuit Details

Figure 20 shows an approximate timing budget for the A/D converter. If 12 cycles are to be completed in 1μs, approximately 80ns is allowed for each cycle. Since the Shottky diodes clamp the voltage of the summing junction, the DAC settling time approaches the current-settling value of 35ns, and hence uses up less than half the timing budget.

To maintain simplicity, a simple clock is used that runs at a constant rate throughout the conversion, with a duty cycle of approximately 90%. If absolute speed is worth the additional complexity, the clock frequency can be increased as the conversion progresses since the DAC must settle from increasingly smaller steps.

When seeking a cycle time of less than 100ns, the delays generated by the older generation SAR registers become problematic. Newer, higher speed SAR logic chips are becoming available in the classic 2504 pinout that cuts the logic overhead in half. One example of this is Zyrel's ZR2504.

Finding a comparator capable of keeping up with this DAC arrangement is fairly difficult: it must respond to an overdrive of 250μV (1LSB) in less than 25ns. Since no inexpensive comparator exists with these specs, special arrangements must be made. The LT1016 comparator provides relatively quick response, but requires at least 5mV of overdrive to maintain this speed. A discrete preamplifier may be used to amplify the summing junction voltage to sufficiently overdrive the comparator. Care must be exercised in the layout of the preamp/comparator block to avoid introducing comparator instability with the preamp's additional gain.

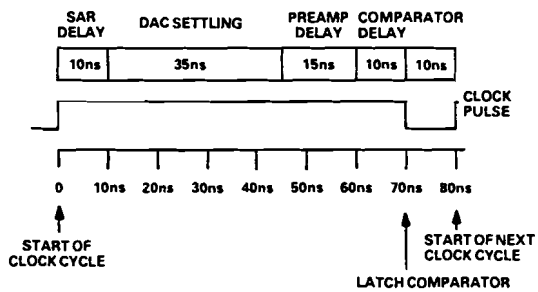


Figure 20. Typical Clock Cycle for a 1μs SAR A/D Converter

HIGH-SPEED MULTIPLYING DAC

A powerful use for the AD568 is found in multiplying applications, where the DAC controls the amplitude of a high-speed signal. Specifically, using the AD568 as the control voltage input signal for the AD539 60MHz analog multiplier and AD5539 wide-band op amp, a high-speed multiplying DAC can be built.

In the application shown in Figure 21, the AD568 is used in a buffered voltage output mode to generate the input to the AD539's control channel. The speed of the AD568 allows oversampling of the control signal waveform voltage, thereby providing increased spectral purity of the amplitude envelope that modulates the analog input channels.

The AD568 is configured in the unbuffered unipolar output mode. The internal 200Ω load resistor creates the 0-1V FS output signal, which is buffered and amplified to a 0-3V range suitable for the control channel of the AD539.

A 500Ω input impedance exists at Pin 1, the input channel. To provide a buffer for the 0-1V output signal from the AD568 looking into the impedance and to achieve the full-scale range, the AD841, high-speed, fast settling op amp is included. The gain of 3 is achieved with a 2kΩ resistor configured in follower mode with a 1kΩ pot and 500Ω resistor. A 20kΩ pot with connections to Pins 3, 4 and 12 is provided for offset trim.

The AD539 can accept two separate input signals, each with a nominal full-scale voltage range of ±2V. Each signal can then be simultaneously controlled by the AD568 signal at the common input channel, V_X. The current outputs from the two signal channels, Pins 11 and 14, applied to the AD5539 in a subtracting configuration, provide the voltage output signal:

$$V_{OUT} = \frac{D}{4096} \times \frac{V_{Y1} - V_{Y2}}{2V} \quad (0 \leq D \leq 4095)$$

For applications where only a single channel is involved, channel 2, V_{Y2}, is tied to ground. This provides:

$$V_{OUT} = \frac{D}{4096} \times \frac{V_{Y1}}{2V} \quad (0 \leq D \leq 4095)$$

Some AD539 circuit details: The control amplifier compensation capacitor for Pin 2, C_C, must have a minimum value of 3000pF to provide circuit stability. For improved bandwidth and feedthrough, the feedthrough capacitor between Pins 1 and 2 should be 5-20% of C_C. A Schottky diode at Pin 2 can improve recovery time from small negative values of V_X. Lead lengths along the path of the high-speed signal from AD568 should be kept at a minimum.

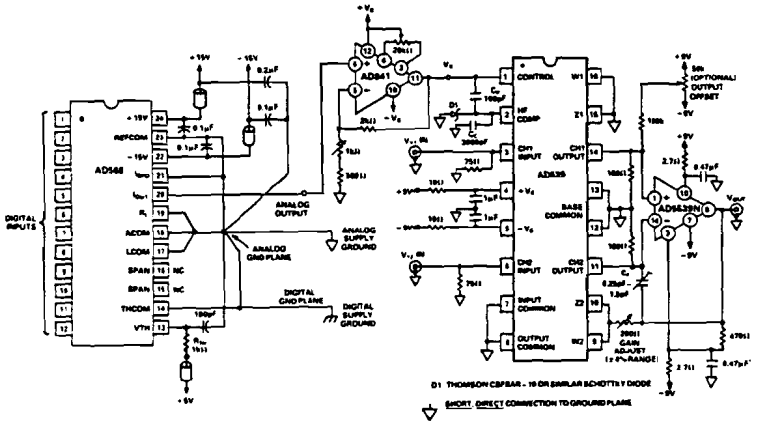


Figure 21. Wideband Digitally Controlled Multiplier

ANALOG DEVICES

Wideband, Fast Settling Op Amp

AD840

FEATURES

Wideband AC Performance
- Gain Bandwidth Product: 400 MHz (Gain ≥ 10)
- Fast Settling: 100 ns to 0.01% for a 10 V Step
- Slew Rate: 400 V/μs
- Stable at Gains of 10 or Greater
- Full Power Bandwidth: 6.4 MHz for 20 V p–p into a 500 Ω Load

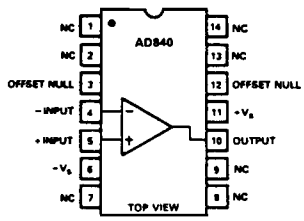
Precision DC Performance
- Input Offset Voltage: 0.3 mV max
- Input Offset Drift: 3 μV/°C typ
- Input Voltage Noise: 4 nV/$\sqrt{Hz}$
- Open-Loop Gain: 130 V/mV into a 1 kΩ Load
- Output Current: 50 mA min
- Supply Current: 12 mA max

APPLICATIONS

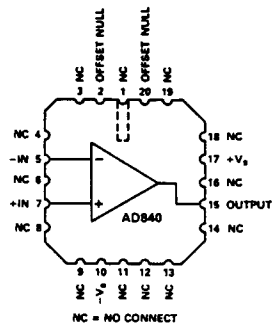
- Video and Pulse Amplifiers
- DAC and ADC Buffers
- Line Drivers
- Available in 14-Pin Plastic DIP, Hermetic Cerdip and 20-Pin LCC Packages and in Chip Form
- MIL-STD-883B Processing Available

CONNECTION DIAGRAMS

Plastic DIP (N) Package and Cerdip (Q) Package



LCC (E) Package



PRODUCT DESCRIPTION

The AD840 is a member of the Analog Devices' family of wide bandwidth operational amplifiers. This high speed/high precision family includes, among others, the AD841, which is unity-gain stable, and the AD842, which is stable at a gain of two or greater and has 100 mA minimum output current drive. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to its 400 MHz gain bandwidth product, the AD840 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in 100 ns for a 10 volt step.

The AD840 remains stable over its full operating temperature range at closed-loop gains of 10 or greater. It also offers a low quiescent current of 12 mA maximum, a minimum output current drive capability of 50 mA, a low input voltage noise of 4 nV/$\sqrt{Hz}$ and a low input offset voltage of 0.3 mV maximum (AD840K).

The 400 V/μs slew rate of the AD840, along with its 400 MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is ideally suited for use in high frequency signal conditioning circuits and wide bandwidth active filters. The extremely rapid settling time of the AD840 makes it the preferred choice for data acquisition applications which require 12-bit accuracy. The AD840 is also appropriate for other applications such as high speed DAC and ADC buffer amplifiers and other wide bandwidth circuitry.

APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD840 make it ideal for DAC and ADC buffers, line drivers and all types of video instrumentation circuitry.
2. The AD840 is truly a precision amplifier. It offers 12-bit accuracy to 0.01% or better and wide bandwidth, performance previously available only in hybrids.
3. The AD840's thermally balanced layout and the high speed of the CB process allow the AD840 to settle to 0.01% in 100 ns without the long "tails" that occur with other fast op amps.
4. Laser wafer trimming reduces the input offset voltage to 0.3 mV max on the K grade, thus eliminating the need for external offset nulling in many applications. Offset null pins are provided for additional versatility.
5. Full differential inputs provide outstanding performance in all standard high frequency op amp applications where circuit gain will be 10 or greater.
6. The AD840 is an enhanced replacement for the HA2540.

AD840—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD840J Min	AD840J Typ	AD840J Max	AD840K Min	AD840K Typ	AD840K Max	AD840S Min	AD840S Typ	AD840S Max	Units
INPUT OFFSET VOLTAGE[1]			0.2	1		0.1	0.3		0.2	1	mV
	T_{min} – T_{max}			1.5			0.7			2	mV
Offset Drift			5			3			5		μV/°C
INPUT BIAS CURRENT			3.5	8		3.5	5		3.5	8	μA
	T_{min} – T_{max}			10			6			12	μA
INPUT OFFSET CURRENT			0.1	0.4		0.1	0.2		0.1	0.4	μA
	T_{min} – T_{max}			0.5			0.3			0.6	μA
INPUT CHARACTERISTICS	Differential Mode										
Input Resistance			30			30			30		kΩ
Input Capacitance			2			2			2		pF
INPUT VOLTAGE RANGE											
Common Mode		±10	12		±10	12		±10	12		V
Common-Mode Rejection	V_{CM} = ±10 V	90	110		106	115		90	110		dB
	T_{min} – T_{max}	85			90			85			dB
INPUT VOLTAGE NOISE	f = 1 kHz		4			4			4		nV/√Hz
Wideband Noise	10 Hz to 10 MHz		10			10			10		μV rms
OPEN LOOP GAIN	V_O = ±10 V										
	R_{LOAD} = 1 kΩ	100	130		100	130		100	130		V/mV
	T_{min} – T_{max}	50	80		75	100		50	80		V/mV
	R_{LOAD} = 500 Ω	75			100			75			V/mV
	T_{min} – T_{max}	50			75			50			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} ≥ 500 Ω										
	T_{min} – T_{max}	±10			±10			±10			V
Current	V_{OUT} = ±10 V	50			50			50			mA
Output Resistance	Open Loop		15			15			15		Ω
FREQUENCY RESPONSE											
Gain Bandwidth Product	V_{OUT} = 90 mV p–p										
	A_V = –10		400			400			400		MHz
Full Power Bandwidth[2]	V_O = 20 V p–p										
	R_{LOAD} ≥ 500 Ω	5.5	6.4		5.5	6.4		5.5	6.4		MHz
Rise Time	A_V = –10		10			10			10		ns
Overshoot[3]	A_V = –10		20			20			20		%
Slew Rate[3]	A_V = –10	350	400		350	400		350	400		V/μs
Settling Time[3] –10 V Step	A_V = –10										
	to 0.1%		80			80			80		ns
	to 0.01%		100			100			100		ns
OVERDRIVE RECOVERY	–Overdrive		190			190			190		ns
	+Overdrive		350			350			350		ns
DIFFERENTIAL GAIN	f = 4.4 MHz		0.025			0.025			0.025		%
DIFFERENTIAL PHASE	f = 4.4 MHz		0.04			0.04			0.04		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±5		±18	±5		±18	±5		±18	V
Quiescent Current			12	14		12	14		12	14	mA
	T_{min} – T_{max}			16			16			18	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±18 V	90	100		94	100		90	100		dB
	T_{min} – T_{max}	80			86			80			dB
TEMPERATURE RANGE											
Rated Performance[4]		0		+75	0		+75	–55		+125	°C
TRANSISTOR COUNT	# of Transistors		72			72			72		

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.
[2]Full power bandwidth = slew rate/2π V_{PEAK}.
[3]Refer to Figures 22 and 23.
[4]"S" grade T_{min}–T_{max} specifications are tested with automatic test equipment at T_A = −55°C and T_A = +125°C.
All min and max specifications are guaranteed. Specifications shown in boldface are tested on all production units.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
  Plastic (N) . . . . . 1.5 W
  Cerdip (Q) . . . . . 1.3 W
  LCC (E) . . . . . 1.0 W
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Storage Temperature Range
  Q, E . . . . . −65°C to +150°C
  N . . . . . −65°C to +125°C
Junction Temperature (T_J) . . . . . +175°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

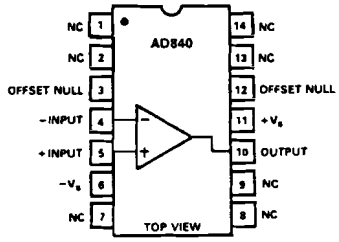
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C.

Thermal Characteristics:

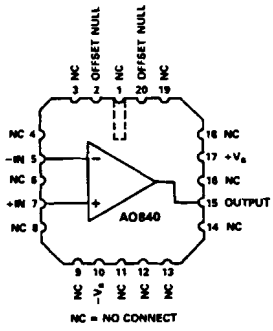
	θ_{JC}	θ_{JA}	Derate at
Cerdip Package	30°C/W	110°C/W	8.7 mW/°C
Plastic Package	30°C/W	100°C/W	10 mW/°C
LCC Package	35°C/W	150°C/W	6.7 mW/°C

Recommended Heat Sink:
Aavid Engineering[C] #602B

Plastic DIP (N) Package
and
Cerdip (Q) Package



LCC (E) Package



AD840 Connection Diagrams

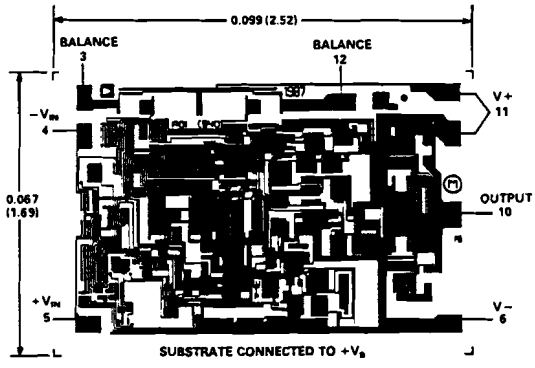
ORDERING GUIDE

Model[1]	Package Options[2]
AD840JN	N-14
AD840KN	N-14
AD840JQ	Q-14
AD840KQ	Q-14
AD840SQ	Q-14
AD840SQ-883B	Q-14
AD840SE-883B	E-20A

NOTES
[1]J and S Grade Chips also available.
[2]N = Plastic DIP; Q = Cerdip; E = LCC (Leadless Ceramic Chip Carrier). For outline information see Package Information section.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



AD840—Typical Characteristics (at +25°C and V_S = ±15 V, unless otherwise noted)

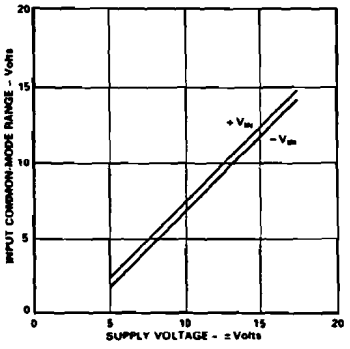


Figure 1. Input Common-Mode Range vs. Supply Voltage

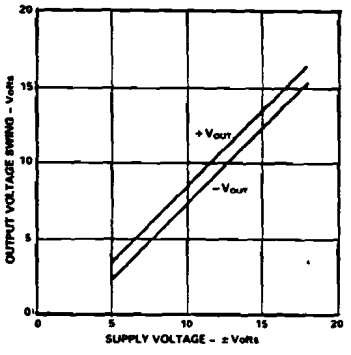


Figure 2. Output Voltage Swing vs. Supply Voltage

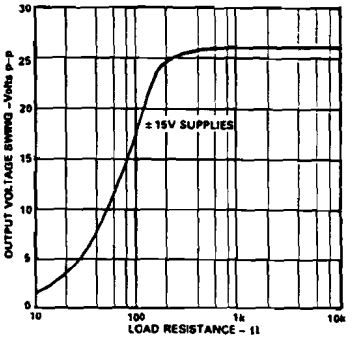


Figure 3. Output Voltage Swing vs. Load Resistance

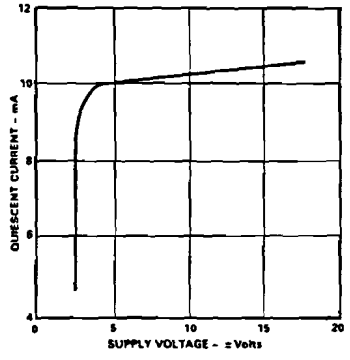


Figure 4. Quiescent Current vs. Supply Voltage

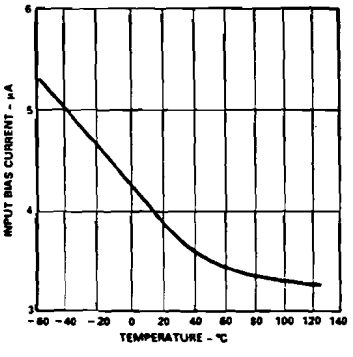


Figure 5. Input Bias Current vs. Temperature

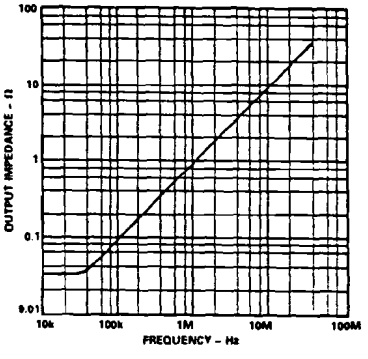


Figure 6. Output Impedance vs. Frequency

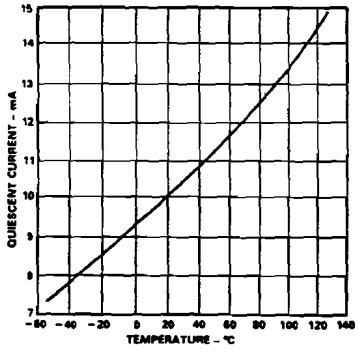


Figure 7. Quiescent Current vs. Temperature

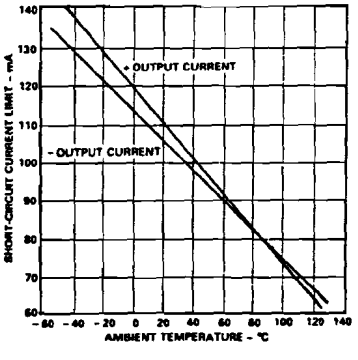


Figure 8. Short-Circuit Current Limit vs. Temperature

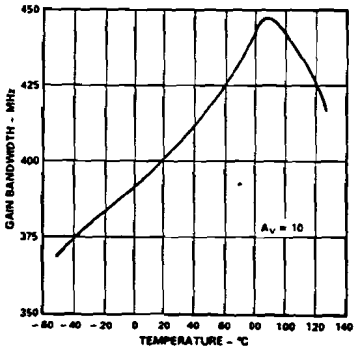


Figure 9. Gain Bandwidth Product vs. Temperature

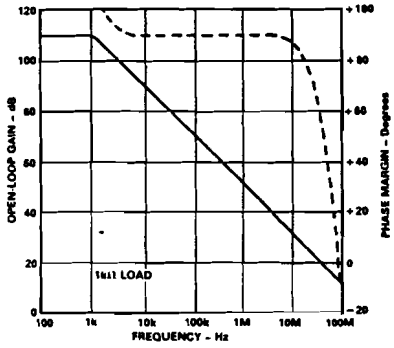


Figure 10. Open-Loop Gain and Phase Margin Phase vs. Frequency

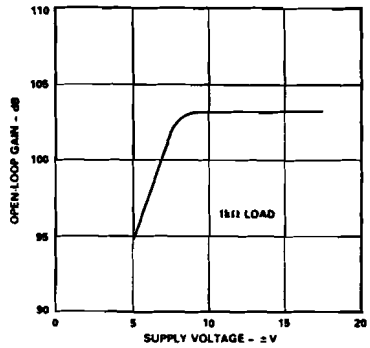


Figure 11. Open-Loop Gain vs. Supply Voltage

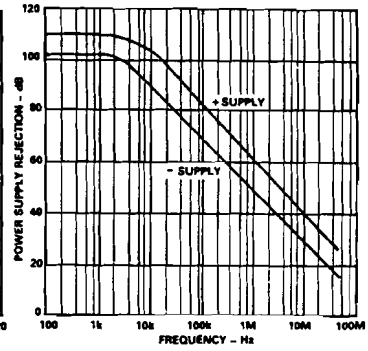


Figure 12. Power Supply Rejection vs. Frequency

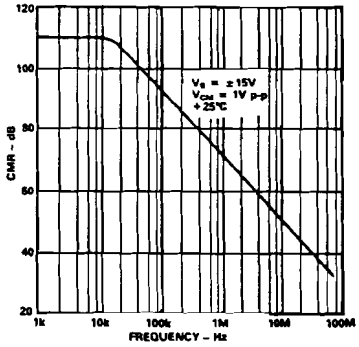


Figure 13. Common-Mode Rejection vs. Frequency

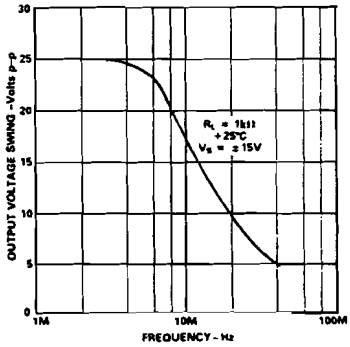


Figure 14. Large Signal Frequency Response

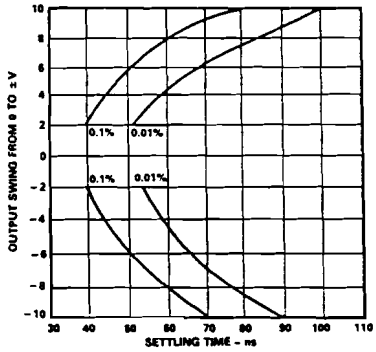


Figure 15. Output Swing and Error vs. Settling Time

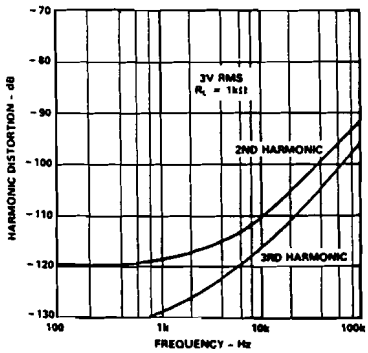


Figure 16. Harmonic Distortion vs. Frequency

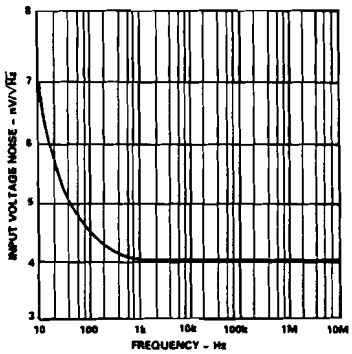


Figure 17. Input Voltage Noise Spectral Density

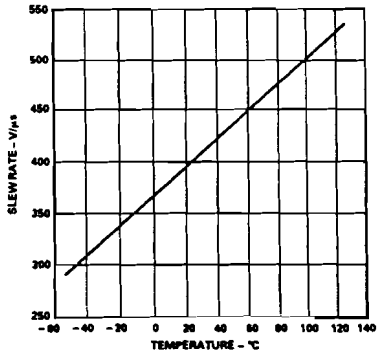


Figure 18. Slew Rate vs. Temperature

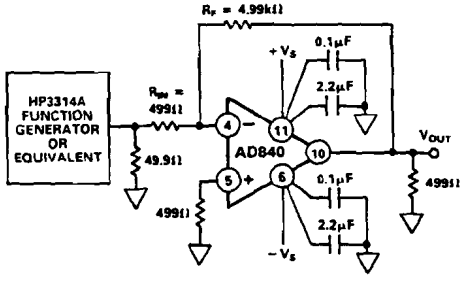


Figure 19a. Inverting Amplifier Configuration (DIP Pinout)

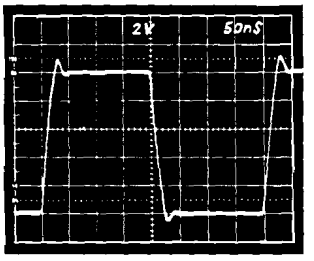


Figure 19b. Inverter Large Signal Pulse Response

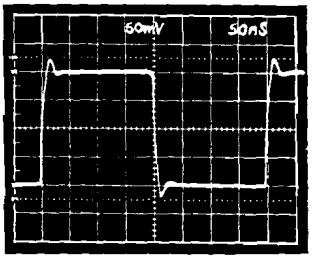


Figure 19c. Inverter Small Signal Pulse Response

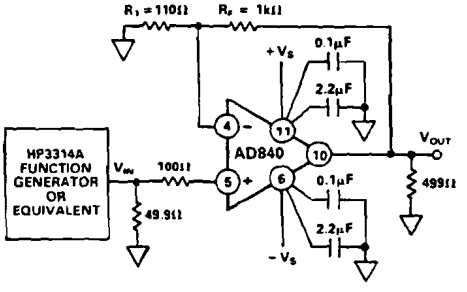


Figure 20a. Noninverting Amplifier Configuration (DIP Pinout)

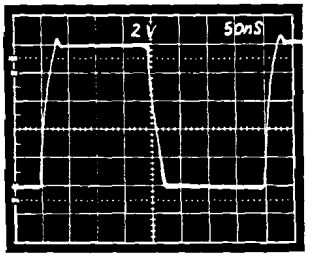


Figure 20b. Noninverting Large Signal Pulse Response

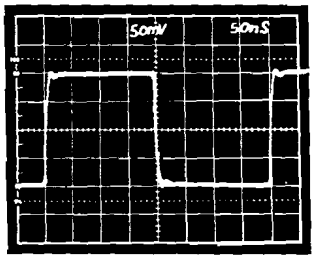


Figure 20c. Noninverting Small Signal Pulse Response

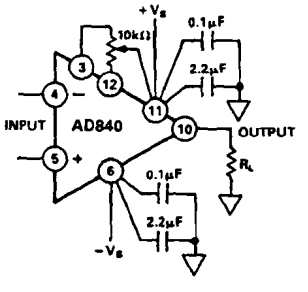


Figure 21. Offset Nulling (DIP Pinout)

OFFSET NULLING

The input offset voltage of the AD840 is very low for a high speed op amp, but if additional nulling is required, the circuit shown in Figure 21 can be used.

AD840 SETTLING TIME

Figures 22 and 24 show the settling performance of the AD840 in the test circuit shown in Figure 23.

Settling time is defined as:

> The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

This definition encompasses the major components which comprise settling time. They include (1) propagation delay through the amplifier; (2) slewing time to approach the final output value; (3) the time of recovery from the overload associated with slewing; and (4) linear settling to within the specified error band.

Expressed in these terms, the measurement of settling time is obviously a challenge and needs to be done accurately to assure the user that the amplifier is worth consideration for the application.

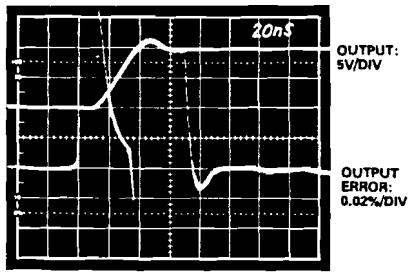


Figure 22. AD840 0.01% Settling Time

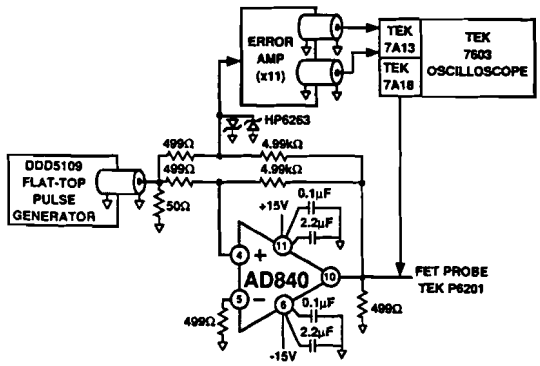


Figure 23. Settling Time Test Circuit

Figure 23 shows how measurement of the AD840's 0.01% settling in 100 ns was accomplished by amplifying the error signal from a false summing junction with a very high speed proprietary hybrid error amplifier specially designed to enable testing of small settling errors. The device under test was driving a 420 Ω load. The input to the error amp is clamped in order to avoid possible problems associated with the overdrive recovery of the oscilloscope input amplifier. The error amp amplifies the error from the false summing junction by 11, and it contains a gain vernier to fine trim the gain.

Figure 24 shows the "long-term" stability of the settling characteristics of the AD840 output after a 10 V step. There is no evidence of settling tails after the initial transient recovery time. The use of a junction isolated process, together with careful layout, avoids these problems by minimizing the effects of transistor isolation capacitance discharge and thermally induced shifts in circuit operating points. These problems do not occur even under high output current conditions.

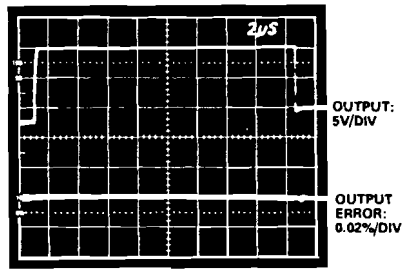


Figure 24. AD840 Settling Demonstrating No Settling Tails

GROUNDING AND BYPASSING

In designing practical circuits with the AD840, the user must remember that whenever high frequencies are involved, some special precautions are in order. Circuits must be built with short interconnect leads. Large ground planes should be used whenever possible to provide a low resistance, low inductance circuit path, as well as minimizing the effects of high frequency coupling. Sockets should be avoided, because the increased inter-lead capacitance can degrade bandwidth.

Feedback resistors should be of low enough value to assure that the time constant formed with the circuit capacitances will not limit the amplifier performance. Resistor values of less than 5 kΩ are recommended. If a larger resistor must be used, a small (±10 pF) feedback capacitor in connected parallel with the feedback resistor, R_F, may be used to compensate for these stray capacitances and optimize the dynamic performance of the amplifier in the particular application.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. A 2.2 μF capacitor in parallel with a 0.1 μF ceramic disk capacitor is recommended.

CAPACITIVE LOAD DRIVING ABILITY

Like all wideband amplifiers, the AD840 is sensitive to capacitive loading. The AD840 is designed to drive capacitive loads of up to 20 pF without degradation of its rated performance. Capacitive loads of greater than 20 pF will decrease the dynamic performance of the part although instability should not occur unless the load exceeds 100 pF. A resistor in series with the output can be used to decouple larger capacitive loads.

USING A HEAT SINK

The AD840 draws less quiescent power than most high speed amplifiers and is specified for operation without a heat sink. However, when driving low impedance loads the current to the load can be 4 to 5 times the quiescent current. This will create a noticeable temperature rise. Improved performance can be achieved by using a small heat sink such as the Aavid Engineering #602B.

HIGH SPEED DAC BUFFER CIRCUIT

The AD840's 100 ns settling time to 0.01% for a 10 V step makes it well suited as an output buffer for high speed D/A converters. Figure 25 shows the connections for producing a 0 to +10.24 V output swing from the AD568 35 ns DAC. With the AD568 in unbuffered voltage output mode, the AD840 is placed in noninverting configuration. As a result of the 1 kΩ span resistor provided internally in the AD568, the noise gain of this topology is 10. Only 5 pF is required across the feedback (span) resistor to optimize settling.

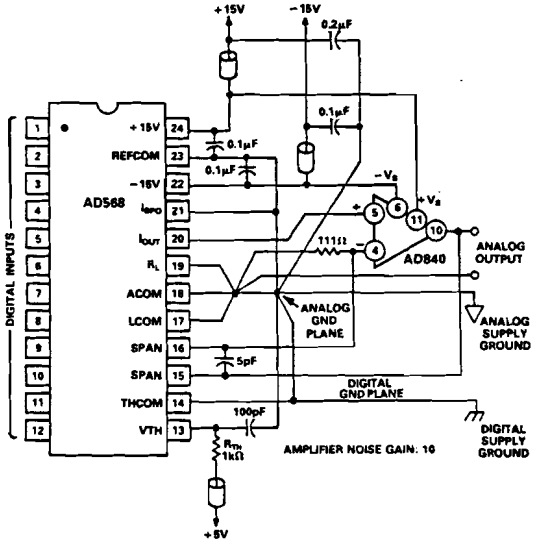


Figure 25. 0 to +10.24 V DAC Output Buffer

OVERDRIVE RECOVERY

Figure 26 shows the overdrive recovery capability of the AD840. Typical recovery time is 190 ns from negative overdrive and 350 ns from positive overdrive.

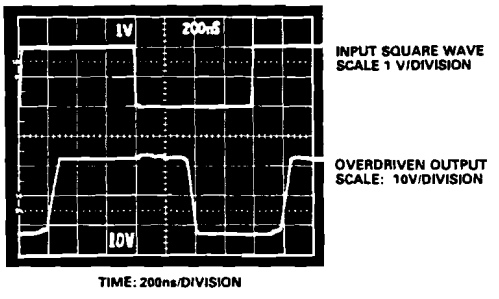


Figure 26. Overdrive Recovery

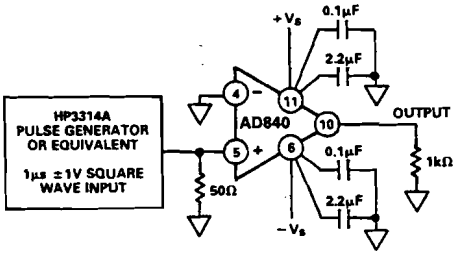


Figure 27. Overdrive Recovery Test Circuit