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DC characterization and noise analysis of submicron low-power, low-voltage CMOS technologies

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Award date:
1998

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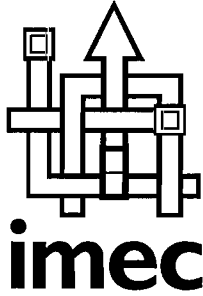

Technische Universiteit
Eindhoven

DC Characterization and Noise Analysis of Submicron Low-Power, Low-Voltage CMOS Technologies

M. van Heijningen

April 15, 1998

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Acknowledgments

I would like to thank all people who have contributed to the results presented in this report.

In the first place I am thankful to dr.ir. L.K.J. Vandamme for offering me the opportunity to graduate at the Inter-university Micro Electronics Center (IMEC) in Leuven, Belgium. I would also like to thank him for letting me use his noise measurement equipment, and for his hospitality.

I am grateful to my coach at IMEC, ir. E.P. Vandamme, who has taught me much about technology development and device operation. I thank him for the pleasant cooperation and the enjoyable time I have had at IMEC. I am also grateful to the other people of the ASP-CMOS division, who have assisted me in my work.

Finally I would like to thank my fellow students at IMEC for their friendship and useful discussions.

Abstract

This work deals with the DC characterization and noise analysis of submicron MOSFETs, produced with novel concepts, for low-power, low-voltage applications. First the DC behavior of these MOSFETs has been modeled with the BSIM3v3 SPICE model. The results have shown that BSIM3v3 is capable of modeling these novel MOSFETs very well. Also a special three-transistor macro-model has been investigated for transistors with halo implantations. This model also resulted in good simulations. The quality of the simulations depends largely on the quality of the parameter extraction routines. To obtain the best possible parameter set, an extraction method has been used, that allows parameters to be adapted and optimized by hand.

The study of DC behavior has shown that novel concepts are necessary to fabricate submicron MOSFETs for low supply voltages. Often, novel concepts have a positive influence on one aspect of the DC behavior, for example the threshold voltage roll-off, but have a negative influence on for example the junction capacitances. For each new technology a well balanced compromise of several concept has to be found to obtain the optimal MOSFET.

The noise analysis has been performed for several reasons: noise measurements can be used as a diagnostic tool, to study the quality of the MOSFETs and to study the influence of novel MOSFET concepts on the noise behavior. It has been shown that novel concepts can increase the noise by a factor 50. The use of an amorphous gate, instead of a poly gate, has been studied separately. This study has shown that the use of an amorphous gate, instead of a poly gate, increases the noise by a factor 5.

The modeling of the noise with a unified noise model, that incorporates both number fluctuations and correlated surface mobility fluctuations, shows the best fits with experimental results over all operating regimes. Such a type of noise model is implemented in the BSIM3v3 SPICE model. The noise has been simulated in all operating regimes (subthreshold, linear and saturation), and has shown very good agreement with the measurement data.

In order to extract good parameter values, necessary for the unified noise models, a novel two-parameter extraction method has been presented, using a few experimental results.

It has also been shown that the implementation of the BSIM3v3 noise model in SPICE is inaccurate in the subthreshold region for our technology. This is due to a technology depended parameter that has been assumed constant in SPICE. This makes the SPICE noise simulations in the subthreshold region only valid for a limited set of MOSFET technologies. An improved BSIM3v3 noise model is proposed.

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1 Introduction

The increase in demand for portable electronic equipment requires new Integrated Circuit (IC) technologies to operate at a low supply-voltage and have a low power consumption. Not only portable equipment, but also new very large scale integration (VLSI) designs require a low power consumption per transistor, due to the increasing number of transistors in these designs. Not reducing the power consumption of new ICs, will lead to reliability problems, due to the high operating temperature, or will require expensive cooling methods. To combine these voltage and power requirements with the ever decreasing device sizes requires special attention. New concepts for realizing low voltage, low power Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) have to be developed and investigated. This report will deal with the investigation of the DC behavior and noise analysis of several of these novel concepts.

The objective of this study can be split up into two main subject: the DC characterization and the noise analysis. DC related objectives are:

- To study the influence of novel MOSFET concepts on the DC behavior.
- To model the DC behavior of novel MOSFETs.
- To extract the parameters necessary for this modeling.
- To investigate the use of a special macro-model for transistors with a halo implant.

Noise related objectives are:

- To determine the influence of novel concepts on the noise behavior of the MOSFETs.
- To model the observed noise in all operating regimes with, if possible, one noise model.
- To extract the parameters, necessary for the noise modeling.

To achieve the objectives the following procedure will be followed:

First, the ability of the Berkeley Short-channel Insulated gate field effect transistor Model version 3v3.1 (BSIM3v3.1) Simulation Program with Integrated Circuit Emphasis (SPICE) model for these special transistors is investigated. Because of the special concepts that have been used to produce transistors, which must operate at low supply voltages, the modeling could be difficult. Although BSIM3v3 is one of the newest, and most complex, SPICE models, and can already model some special MOSFET concepts, it is still a simplification of reality. When using such a complex MOSFET model the quality of the parameter extraction is of major importance. Parameter extractions can no longer be performed manually in such complex models, but must be performed by software routines. Some attention will be paid to the present extraction routines and how to use these routines to extract the best parameter set. Because the SPICE models of the MOSFETs will be used later on in the noise analysis, it is very important that these simulations are accurate.

Instead of modeling a MOSFET with one transistor it is also possible to use a macro-model, consisting of a reference transistor and one or two transistors in series, to account for the special effects. The use of such a macro-model will also be investigated. First the DC characteristics will be modeled in this way, and later on these models will be used for the noise analysis. These kind of models have the advantage that the noise, coming from different parts of the

transistor, can be easily recognized, but the disadvantage is that the parameters for such models must be extracted manually, which is a very lengthy and difficult process.

The noise behavior is investigated for several reasons. It is important to know if these novel MOSFET concepts cause extra noise compared to conventional processed MOSFETs, and if they do, what causes this increase in noise. To understand the dominant noise sources it is also important to model the noise behavior, with existing or new models. Also the absolute value and type of noise can be used to give insight in the quality of processing.

The examined MOSFETs are part of test-chip designs and are processed with a $0.50\mu m$ low-voltage low-power Complementary Metal-Oxide-Semiconductor (CMOS) technology (PL5004) and a $0.25\mu m$ low-voltage low-power CMOS technology (PL7009). These technologies use respectively a 7 nm and a 4.5 nm gate oxide thickness and are intended for use with a 1.2 V supply voltage. With this supply-voltage the threshold voltage has to be in the range of 0.2-0.4 V. Also some measurements are performed on a 0.35 μm CMOS technology (PL6042). This technology uses a higher supply voltage of 3.3 V and has a gate oxide thickness of 7 nm.

This work is part of a project on novel MOSFET concepts for a low-voltage, low-power application in combination with decreasing device sizes.

2 CMOS device scaling, short-channel effects and novel transistor concepts

This section will start with a short introduction about the reasons for, and the problems associated with, downscaling CMOS transistors. Next, the short-channel effects will be explained in more detail. Then a number of novel concepts will be presented, which are proposed by several groups around the world. These new concepts intent to make the transistor function properly, despite its small size and low supply voltage.

2.1 CMOS device scaling

The downscaling of transistors is already going on for more than 20 years, resulting in transistors with smaller dimensions, a higher package density, faster circuits and lower power dissipation. Nowadays CMOS technology is the prevailing technology for VLSI designs. To prevent all kind of high-field problems, when the dimensions are scaled down at fixed supply voltage, a constant field scaling method is used by scaling all voltages down in the same way as the dimensions.

When designing special low voltage transistors the voltages are scaled down even more, which creates a number of new problems. The reason for using new low voltage technologies is that nowadays there is a big demand for portable electronic equipment, which must for example work with rechargeable batteries (1.2 V). For portable applications not only a low supply voltage is necessary, but also a low power consumption. Using a lower supply voltage leads to a lower power consumption ($P = fCV_{dd}^2/2$), although there are some difficulties associated with this rule (often the switching frequency and the total capacitance are increased, when using new technologies).

When scaling down the supply voltage, the threshold voltage must also be scaled down ($V_{th} \approx V_{dd}/5$). Recent trends show that the threshold voltage is not scaled down as much as the supply voltage. This is due to the fact that the subthreshold behavior of a MOSFET is nearly independent of oxide thickness, channel length and supply voltage. Scaling down the threshold voltage in the same way as the supply voltage would lead to very high off-state currents and power consumption ($P_{off} \sim exp(-V_{th})$). Also the leakage current of a MOSFET does not decrease when scaling down the MOSFET, but rather increases. As a result the minimal threshold voltage is kept at about 0.3 V and the minimum supply voltage 1.0 V [1]-[3].

2.2 Short-channel effect

The short-channel effect refers to the decrease of the threshold voltage in short-channel devices due to charge sharing between the gate and the source-drain regions. Sometimes this decrease of the threshold voltage is preceded by an increase (the reverse short-channel effect) due to the existence of a potential barrier at the edge of the channel to the source-drain junctions [4]. Figure 1 shows a possible dependence of the threshold voltage on the channel length.

To prevent this short-channel effect the gate-controlled depletion width must be retained, despite the smaller channel length. A schematic example of this is also shown in figure 1. The dashed lines represent the depletion width in the channel area. In figure 1 the top MOSFET has a depletion width mainly due to the source and drain influence. In the lower MOSFET the gate is in better control of the depletion width. This requires an increased channel-

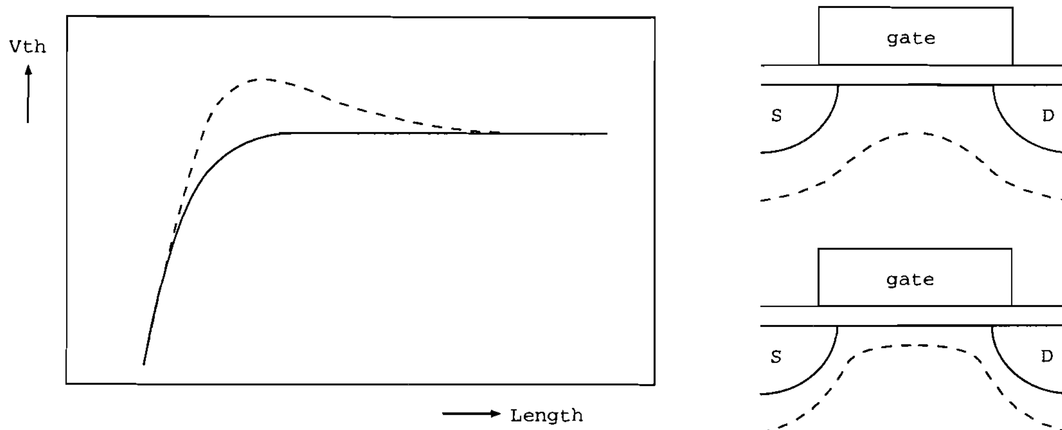


Figure 1: Short-channel effect

doping concentration, but will result in a higher threshold voltage (which was not intended). To overcome this problem several forms of channel engineering can be applied, for example a retrograde well (vertical channel engineering [2]) or the use of halo or SPI implantations (lateral channel engineering [3]).

2.3 Novel MOSFET concepts

In the next sections some novel MOSFET concepts will be discussed briefly. These new concepts are halo, Self-aligned Pocket Implantation (SPI), retrograde well, Lightly-Doped Drain (LDD) after spacer etch and High-Doped Drain (HDD) only.

2.3.1 Halo and SPI

Nowadays different kind of MOSFET-designs are being tested to produce smaller MOSFETs without the negative influence of short-channel effects [5]. One of these new concepts is the use of a halo implant. Although this concept exists already more than 10 years, it is still subject to much research [3] [6] [7]. The halo implant is a kind of lateral channel engineering: the concentration-profile in the lateral direction is changed. The word halo is not an acronym but is used to describe the effect of the implantation: a special layer is formed around the LDD implantation like an aura. Other terms used are Pocket Implanted (PI) MOSFET or Double Implanted (DI) MOSFET. Another technique which is slightly different, but produces the same halo layer, is the SPI.

The special process steps of a halo MOSFET are shown in figure 2. In the case of n-MOSFETs the halo implant consists of a boron implant after the LDD implant and before the HDD implant. The halo implant can be done at different energies and concentrations and also at different angles. The halo implant can be done without the use of an extra mask. This makes the implant rather low cost and easy to perform. The same mask as the LDD implant can be used because boron diffuses faster than phosphorus, and thus will be placed between the LDD region and the channel. The SPI technique produces more or less the same result. A SPI is made by etching away the spacers, after the LDD and HDD implantations and the forming of the drain, source and gate electrodes, and then performing a boron implantation. The electrodes function as a mask, so no extra mask is needed (self-aligned). The SPI creates

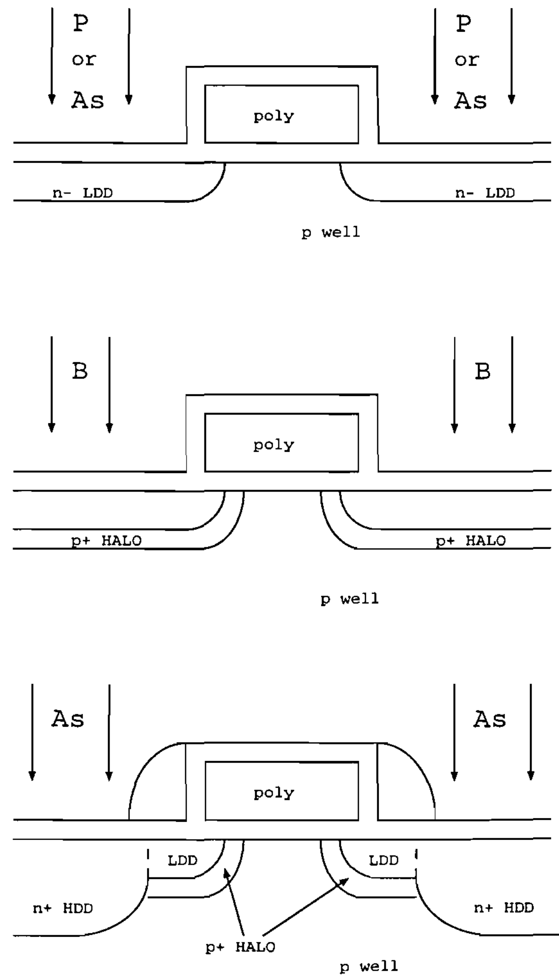


Figure 2: Halo process steps

a kind of pocket at the side of the source/drain junctions under the gate. As will be shown later on, a SPI is located more at the side of the junctions than a halo, which is also located at the bottom of the junctions.

The influence on the lateral channel doping profile is shown in figure 3. The influence of the extra halo implant can be regarded as an increase in the average channel doping, which will increase the threshold voltage for short channels. For longer channels the increase in average channel doping is negligible.

The halo implant is mainly used to prevent the threshold-voltage roll-off that occurs at small channel lengths. This threshold-voltage roll-off is one of the major restrictions in device scaling. But the halo implant can also be used to increase the drain/source punch through voltage due to the decrease of the depletion width. One of the drawbacks of this decreasing depletion width is the increase in junction capacitance, which can strongly degrade circuit performance.

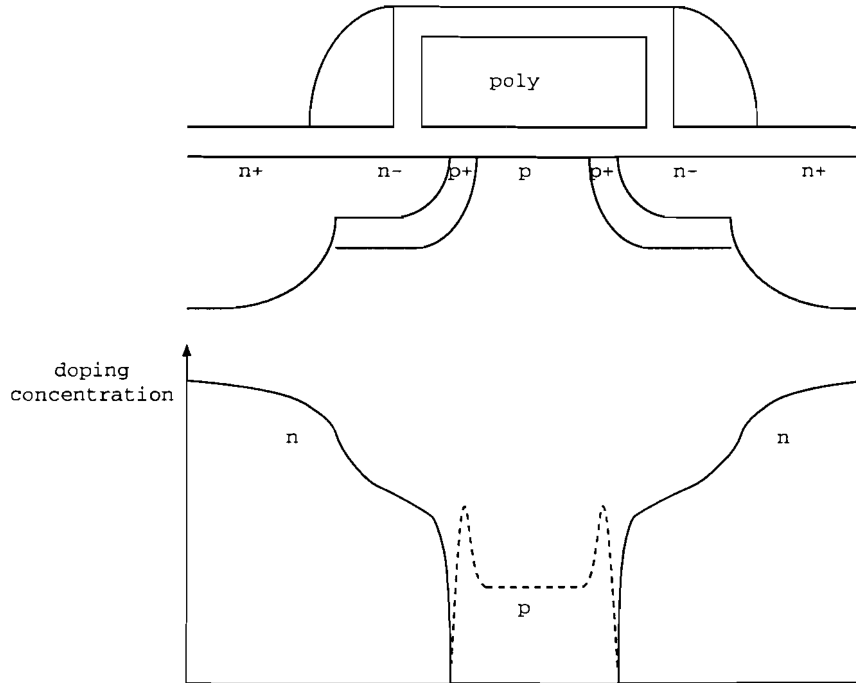


Figure 3: Lateral channel doping profile

2.3.2 Retrograde well

The usage of a retrograde well is a kind of vertical channel engineering, intended to allow a low threshold voltage without the disadvantages of a low doped substrate. In this way the threshold voltage is decoupled from the gate-controlled depletion width. The retrograde doping consists of a low doping directly under the gate, and a higher doping deeper into the substrate. When combining the retrograde well with a halo or SPI the optimum non-uniform doping profile can be obtained [1]. In figure 4 such a profile is depicted. Another advantage of the retrograde profile is that, due to the lower sub-surface doping concentration, the surface mobility will be larger. It has been reported that the use of a retrograde well in combination with a halo doping can substantially improve the short-channel effect [8]

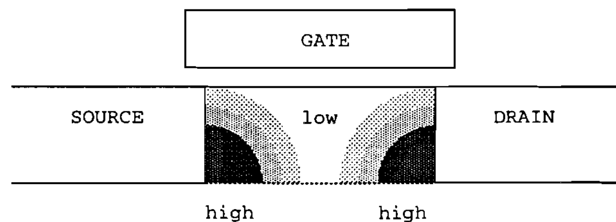


Figure 4: Optimum doping profile

2.3.3 HDD only

Originally the LDD-MOSFET was used to prevent junction breakdown in scaled down MOSFETs, which maintained a large supply voltage (5 V). The junction breakdown is closely related to the peak electric field in the junction. Due to shorter channel lengths and still using a large supply voltage the LDD region was necessary to obtain reliable MOSFETs. The main disadvantage of the LDD region is the increased source/drain series resistance and gate overlap capacitance.

When using a low supply voltage technology the LDD regions can be left out, and still obtain reliable MOSFET operation. This could also result in a lower series resistance, which will increase device speed and reduce power consumption. Also the overlap capacitance will be lowered, which again results in increased device speed.

2.3.4 LDD after spacer etch

When the LDD region is maintained, the parasitic effects can be decreased by implanting the LDD after silicidation and spacer etch. This process has been developed at IMEC [9]. Normally the LDD is implanted early in the process flow and a number of high temperature steps will follow afterwards. This causes the LDD to diffuse further, which will increase the underdiffusion.

When implanting the LDD later in the process flow, after the HDD and spacer etch, fewer temperature steps will follow and the extra diffusion is prevented. The main advantages of this process are lower series resistance, and shallower junctions

3 The BSIM3v3 MOSFET model

In this section the main parameters of the BSIM3v3 model that are important for short-channel MOSFETs will be discussed briefly. Some expressions for the threshold-voltage, mobility and drain-current are presented. For a more extensive description of this model, and the parameters presented in this section, the BSIM3v3 manual can be consulted [10].

3.1 Introduction

The BSIM3v3 MOSFET model is the latest physics-based, deep-submicron MOSFET model for digital and analog circuit designs from the Device Group at the University of California at Berkeley. BSIM3v3 is widely used by many semiconductor manufacturers world-wide for device modeling and deep submicron circuit design. Some of the features of this model are:

- A single current-voltage expression to describe current and output conductance characteristics from subthreshold to strong inversion as well as from the linear to the saturation regions.
- Width and Length dependencies of many parameters to ensure the model's ability to fit a variety of W/L ratios with a single set of parameters.

Physical characteristics that are included in the model are:

- Short and narrow channel effect on the threshold voltage.
- Non-uniform doping effects (in both lateral and vertical directions).
- Mobility reduction due to vertical field.
- Bulk charge effect.
- Carrier velocity saturation.
- Drain-induced barrier lowering (DIBL).
- Channel length modulation (CLM).
- Substrate current induced body effect (SCBE).
- Subthreshold conduction.
- Source/drain parasitic resistances.

3.2 Modeling the threshold voltage

Accurate modeling of the threshold voltage is one of the most important requirements for the precise description of electrical characteristics. The expression for the threshold voltage takes into account the following physical effects:

- Vertical non-uniform doping effect (incorporated into the parameters K1, K2 and Xt).

- Lateral non-uniform doping effect (parameter NLX).
- Short channel effects: drain/source charge sharing and DIBL (parameters DVT0, DVT1, DVT2, ETA0, ETAB and DSUB).
- Narrow channel effects (parameters K3, K3B, W0, DVT0W and DVT1W).

This leads to the following expression for the threshold voltage:

$$\begin{aligned} V_{th} &= VTH0 + K1\left(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s}\right) - K2V_{bseff} \\ &+ K1\left(\sqrt{1+\frac{NLX}{L_{eff}}} - 1\right)\sqrt{\Phi_s} + (K3 + K3BV_{bseff})\frac{TOX}{W_{eff}+W0}\Phi_s \\ &- DVT0W\left(exp(-DVT1W\frac{W_{eff}L_{eff}}{2l_{tw}}) + 2exp(-DVT1W\frac{W_{eff}L_{eff}}{l_{tw}})\right)(V_{bi} - \Phi_s) \\ &- DVT0\left(exp(-DVT1\frac{L_{eff}}{2l_t}) + 2exp(-DVT1\frac{L_{eff}}{l_t})\right)(V_{bi} - \Phi_s) \\ &- \left(exp(-DSUB\frac{L_{eff}}{2l_{t0}}) + 2exp(-DSUB\frac{L_{eff}}{l_{t0}})\right)(ETA0 + ETABV_{bseff})V_{ds} \end{aligned} \tag{1}$$

3.3 The mobility model

A good model for the surface carrier mobility is very critical to the accuracy of a MOSFET model. The scattering mechanisms responsible for surface mobility basically include phonon, coulombic and surface roughness scattering. The expression used in the BSIM3v3 model is (for the setting MOBMOD=1):

$$\mu_{eff} = \frac{U0}{1 + (UA + UC\ V_{bseff})\frac{V_{gs}+V_{th}}{TOX} + UB(\frac{V_{gs}+V_{th}}{TOX})^2} \tag{2}$$

3.4 Unified current expression

The BSIM3v3 model uses a single current expression for all regimes:

$$I_{ds} = \frac{I_{ds0}(V_{dseff})}{1 + \frac{R_{ds}I_{ds0}(V_{dseff})}{V_{dseff}}}\left(1 + \frac{V_{ds} - V_{dseff}}{V_A}\right)\left(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}}\right) \tag{3}$$

In this expression I_{ds0} is the unified linear current expression, V_{dseff} takes the transition from the linear to the saturation regime into account, V_A takes the channel length modulation and the drain induced barrier lowering into account and V_{ASCBE} represents the substrate current induced body effect. Also a correction factor is introduced for the parasitic source and drain resistances (R_{ds}).

3.5 Parameters to model new concepts

Non-uniform vertical channel doping is modeled by the use of three parameters: the channel doping N_{ch}, the substrate doping N_{sub} and the channel doping depth Xt. From these three values the parameters K1 and K2 can be calculated. Non-uniform vertical channel doping can occur when using for example a retrograde well.

Apart from vertical non-uniformity also lateral non-uniform doping is modeled. This is for example the case when using a halo-doping. The lateral non-uniform doping is modeled by the parameter NLX, that is calculated from the difference in doping concentration near the source and drain region and in the middle of the channel.

4 DC characterization and modeling

4.1 Introduction

Extracting the DC (and AC) parameters of MOSFETs is necessary to create models that can be used in circuit simulators. One of these models is the BSIM3v3 model presented before. This model can be used by various SPICE simulators to simulate complex analog and digital circuits.

Also, when using a physics based model like BSIM3v3, the extracted DC parameters can be used to characterize a new developed technology. Effects like under-diffusion (LINT) , series-resistance (RDSW), velocity-saturation (VSAT) and other effects can be determined qualitatively, and to some extend also quantitatively.

Since the BSIM3v3 model is so complex and contains so many parameters, the extraction of the parameters can no longer be performed by hand. Automated curve fitting techniques are needed to extract and optimize the parameters. But it is nearly impossible to automate the entire extraction procedure because a computer will never understand how a MOSFET operates and can only use mathematical routines to extract the parameters. This is why it is still necessary to guide the computer through the extraction routines and, when necessary, make changes by hand.

The software-program used in this work to extract the BSIM3v3 parameters is ICCAP. This program can automatically measure the DC characteristics of a MOSFET and, with the use of special extraction routines, extract a large number of the BSIM3v3 parameters. To obtain the best possible parameter set, an adapted extraction method has been developed, which allows more interaction from the user [11].

Since the SPICE BSIM3v3 model of the measured MOSFETs is also used to investigate the noise behavior, the modeling must be nearly perfect in the operating regions where the noise has been measured. As will be shown later on this is the case for almost all devices.

4.2 DC measurement setup

The measurement setup for the DC characterization is presented in figure 5.

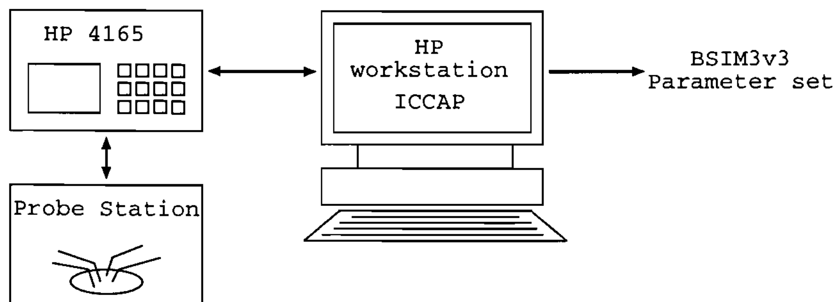


Figure 5: DC characterization

The software program ICCAP, running on a HP workstation, is driving a HP 4156 precision semiconductor parameter analyzer. This analyzer is connected to a probe-station so that measurements can be performed on wafer level.

To extract a good parameter set, an array of different sized devices is necessary. At least a large, short, narrow and small device are needed, but to extract more parameters also extra short and narrow devices are necessary. An example of such an array is given in figure 6.

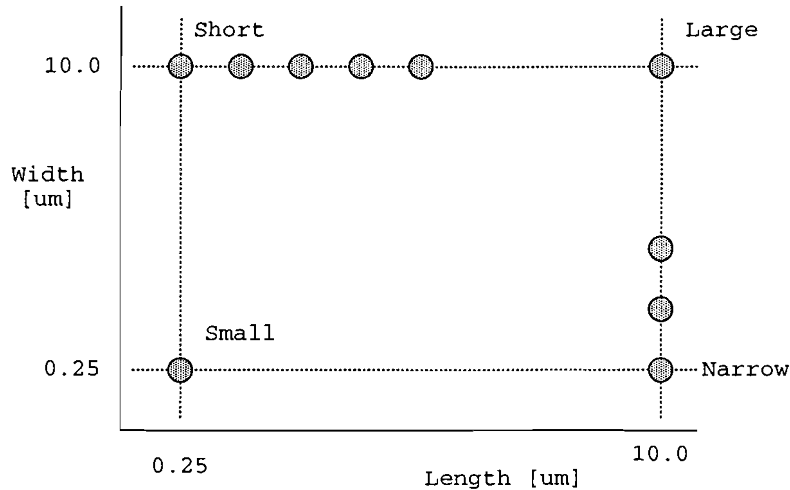


Figure 6: WL device array

4.3 Modeling the halo MOSFET

To investigate the influence of a halo doping on the DC characteristics of a MOSFET, a special SPICE macro-model is used. This macro-model consists of three transistors in series. The transistor in the middle is the reference transistor, that has no special implants. Connected to the drain and source side of this transistor are two special transistors to model the influence of the halo doping. In this model the drain and source resistance are modeled as separate components. Figure 7 shows this macro-model.

In this figure the channel lengths as used in the SPICE circuit are also indicated. By means of a trial and error method the BSIM3v3 parameter values for the halo transistors were found. It was tried to create the model for these special halo transistors with as few parameters as possible. All other parameters were either left to their default value, or were set to zero. The main parameters for the special halo transistors, that are of influence, are its channel length and threshold voltage. Also the mobility and the saturation velocity are adapted to make the SPICE simulation fit with the measured data.

Later on the use of such a model to model the noise behavior will be investigated.

4.4 Measurement results

Since the DC measurements resulted in an enormous amount of data (several curves measured on different WL ratios on several wafers of different technologies) only a subset will be presented here. Some results will be given for each measured technology.

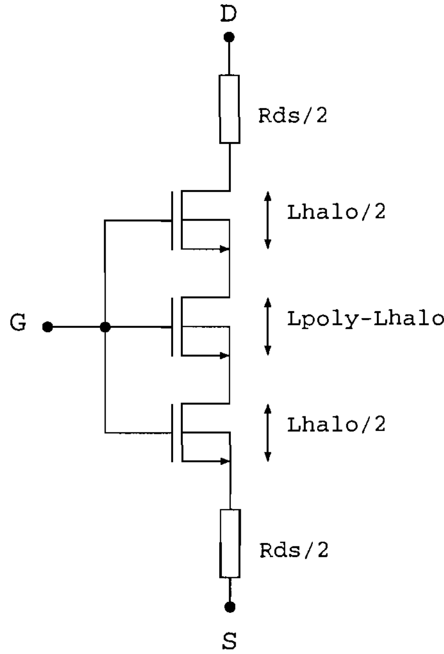


Figure 7: Halo MOSFET SPICE model

4.4.1 PL5004, 0.50 μm NMOS devices

All measurements were performed on n-MOSFET L-arrays. This means that the width of all transistors is the same, namely 10 μm, and that the length of the transistor varies. The different lengths are : 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 2.0, 5.0 and 10.0 μm.

Of this technology four different wafers have been measured: one reference device and three devices with halo implants. The halo implants differ in concentration, energy and implanted angle.

The automatic measurement is only performed on the reference wafer (wafer 3). For the reference MOSFETs, the BSIM3v3 parameter set is extracted, except for the series resistances in the source and drain connection. This is done because the series resistances are separate parts in the used noise model of the MOSFET. The value of the series resistances is extracted with ICCAP, but the BSIM3v3 parameter is afterwards set to zero and the series resistances are added as external resistors in the SPICE model of the MOSFET.

The models are created by fitting the measured data from Ids-Vgs curves at Vds=100 mV and Vds=1.2V for the channel lengths 0.5, 0.7, 1.0, 2.0, and 10.0 μm. For all conditions four devices have been measured on the same wafer. The results from the measurements and the simulation can be seen in figure 8.

These Id-Vg plots show that the DC characteristics can be modeled very well with this macro-model.

Since one of the objects of the extra halo implant is to create a flat threshold voltage as function of the gate length, also a plot is given of the measured threshold voltage. Figure 9 shows this plot. As can be seen, the reference wafer (w3) already shows a reverse short-channel effect, so the wafers with a halo implant have even a larger reverse short-channel effect. So for this particular technology the halo implant has no use. But for investigating the possible

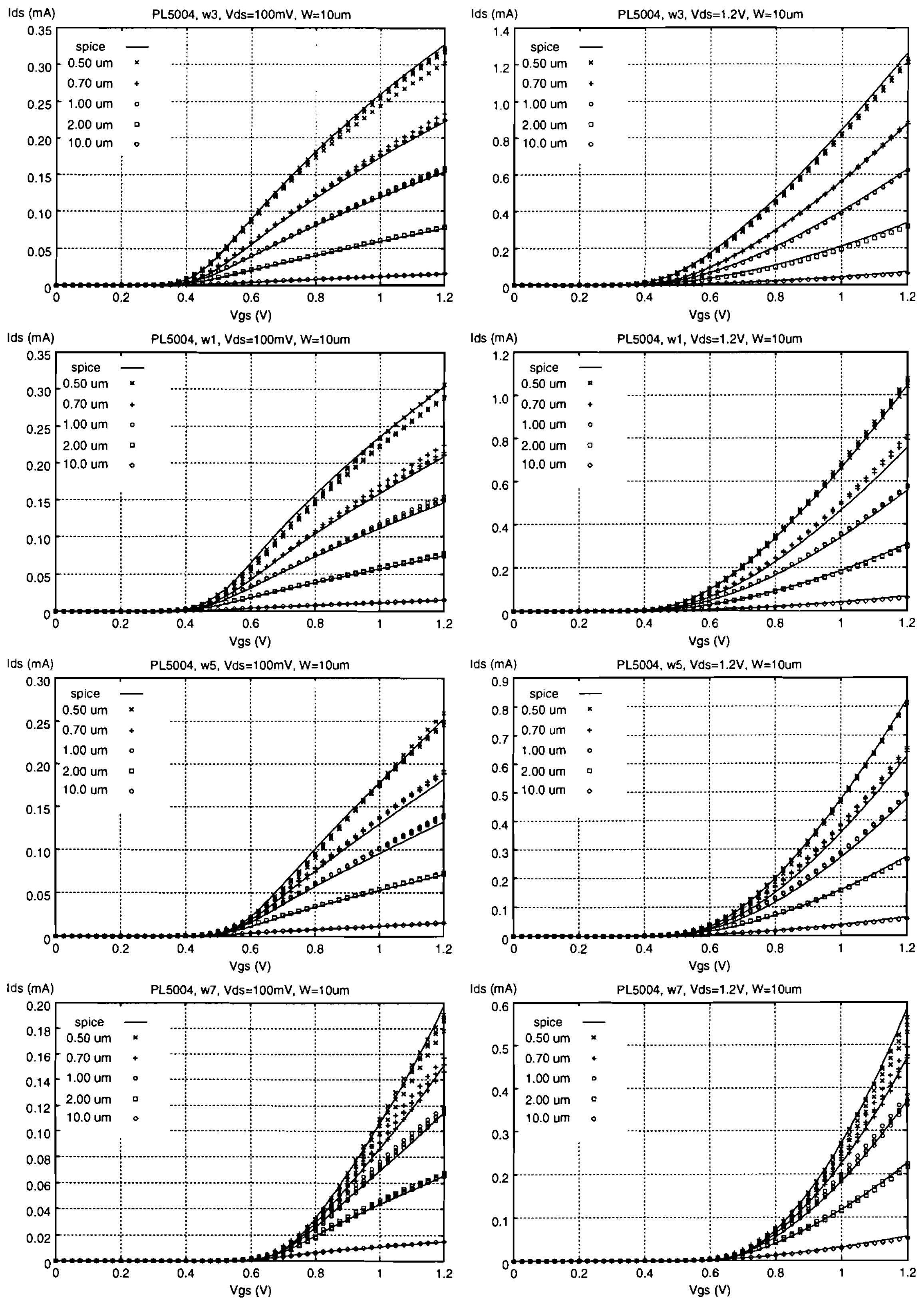


Figure 8: Measured and simulated nMOS id-vg curves

influence of the halo implant on the noise behavior the too large threshold voltage does not matter.

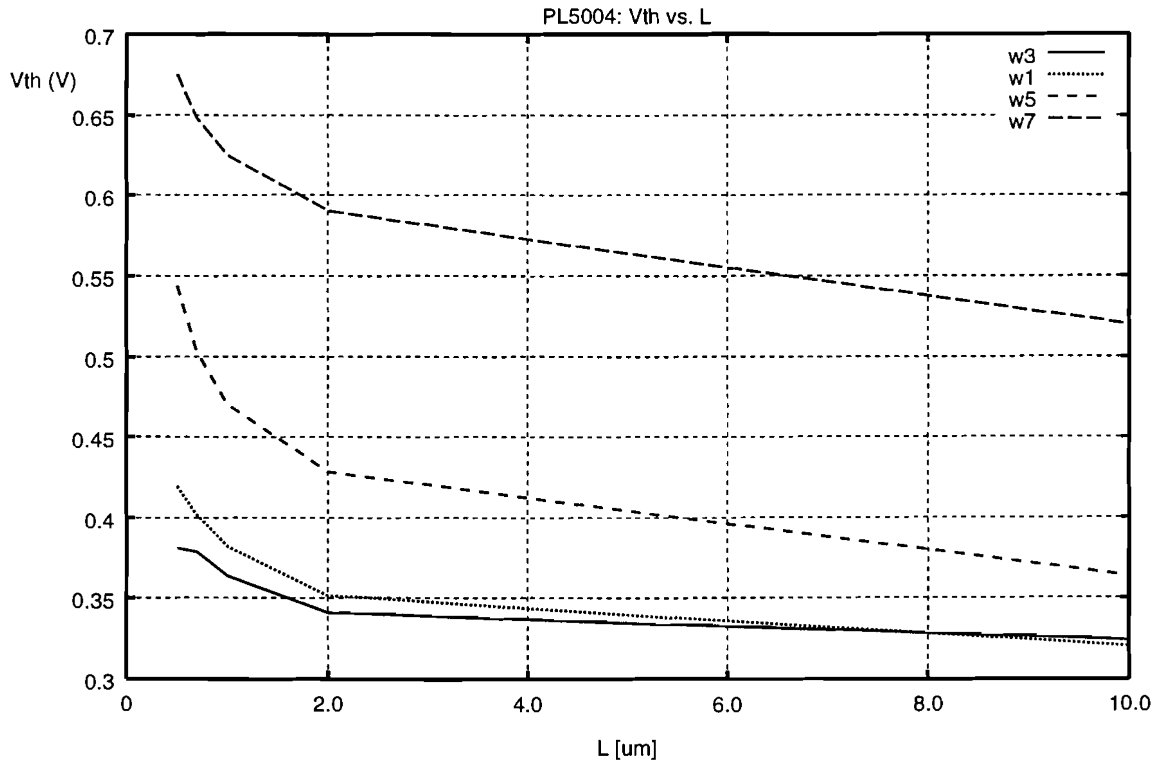


Figure 9: Threshold voltage as function of gate length

4.4.2 PL7009, 0.25 μm PMOS devices

The PL7009 is processed in a 0.25 μm CMOS technology with a 4.5 nm gate oxide thickness. Various novel MOSFET concepts have been tested with this run such as halos, SPIs, LDD after spacer etch, HDD only and different gate materials (poly and amorph).

From this run seven wafers have been measured for their DC characteristics (8, 10, 11, 14, 15, 17, 23). In the next table the special characteristics of the different wafers are given:

Wafer #	gate	spacers	halo/SPI	other special concepts
8	poly	nitride	halo	
10	amorph	oxide		
11	amorph	oxide	SPI	LDD after spacer etch
14	amorph	oxide	SPI	LDD after spacer etch (other dose than 11)
15	amorph	oxide	SPI	HDD only
17	amorph	oxide	halo	
23	amorph	nitride		HDD only, steep retrograde well

On all these wafers a WL-array has been measured with ICCAP and the BSIM3v3 parameters have been extracted. Only a subset of the total measurement results will be given here. First in figure 10 the Id-Vg and Id-Vd curves of wafer 8, 11 and 23 are presented, measured on a device with 10 μm width and 0.25 μm length. The Id-Vg curves have been measured at Vds = -20 mV. The Id-Vd curves have been measured at Vg = -0.80 V, Vg = -1.65 V and

Vg = -2.5 V. The wafers 8, 11 and 23 have been chosen because they are also used for noise measurements. The figure shows that the modeling is, though not perfect, reasonably good.

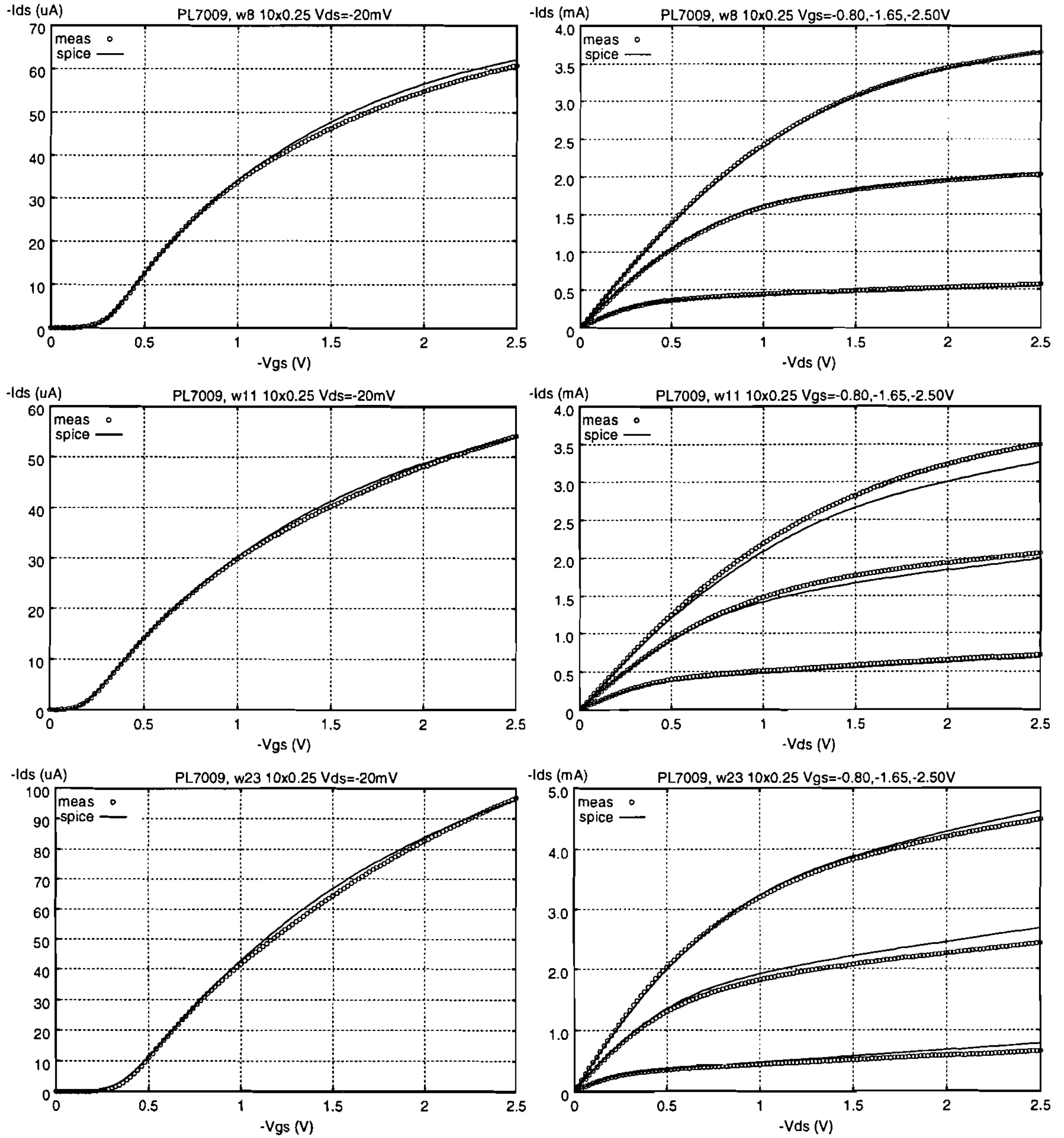


Figure 10: Measured and simulated pMOS id-vg and id-vd curves

To show that the BSIM3v3 model is scalable, figure 11 shows the measurements and simulations of four different devices from wafer 8: a large device (W=10 μm, L=10 μm), a short device (W=10 μm, L=0.25 μm), a narrow device (W=0.40 μm, L=10 μm) and a small device (W=0.40 μm, L=0.25 μm). The same bias-conditions have been used as in the previous measurement. Although the ICCAP routines used to extract the BSIM3v3 parameters do not extract the width dependency of the threshold voltage (and some other width related parameters) the modeling is reasonably good. The small device can be used to check the quality of the modeling because no parameters are extracted from this device.

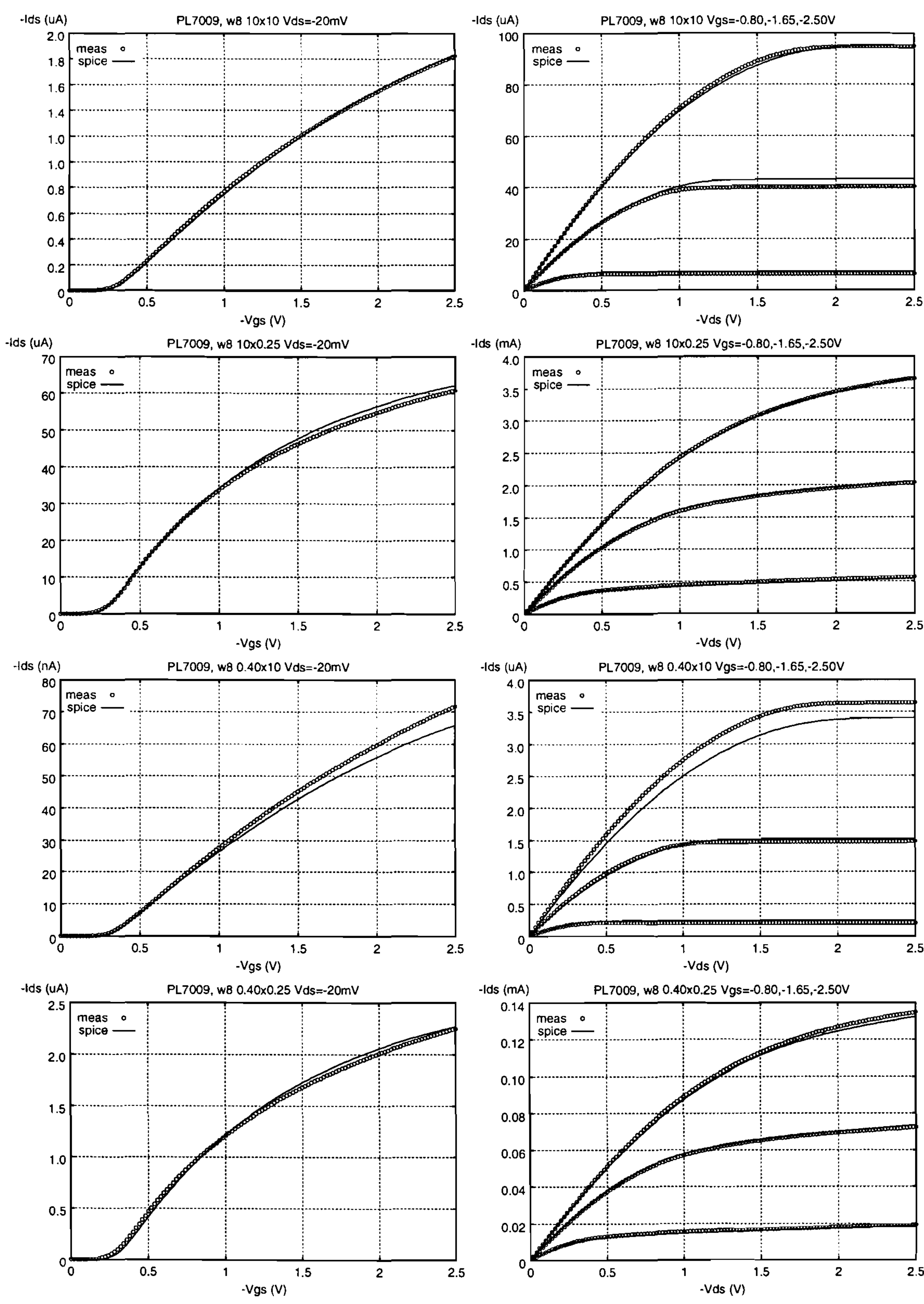


Figure 11: Measured and simulated pMOS id-vg and id-vd curves, different WL ratios

As mentioned before, one of the goals of these novel concepts is to obtain a threshold voltage that remains constant despite the decreasing channel length. Figure 12 shows the threshold voltage as function of the gate length of the measured wafers from PL7009. Note that the gate

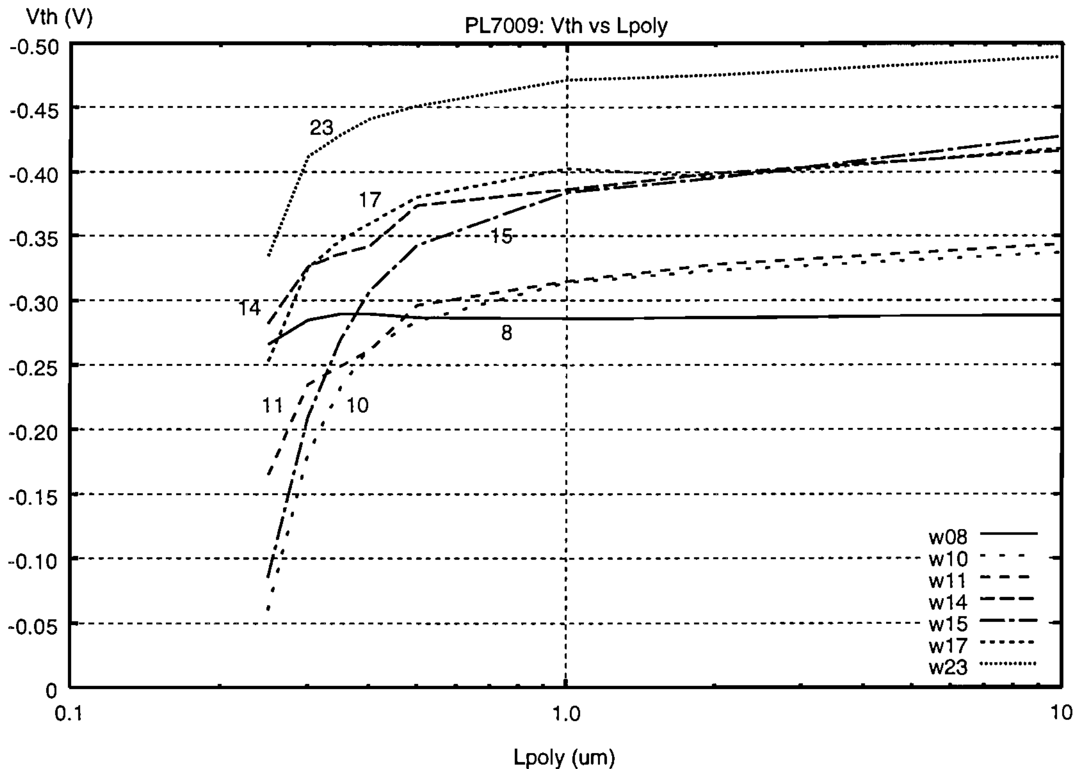


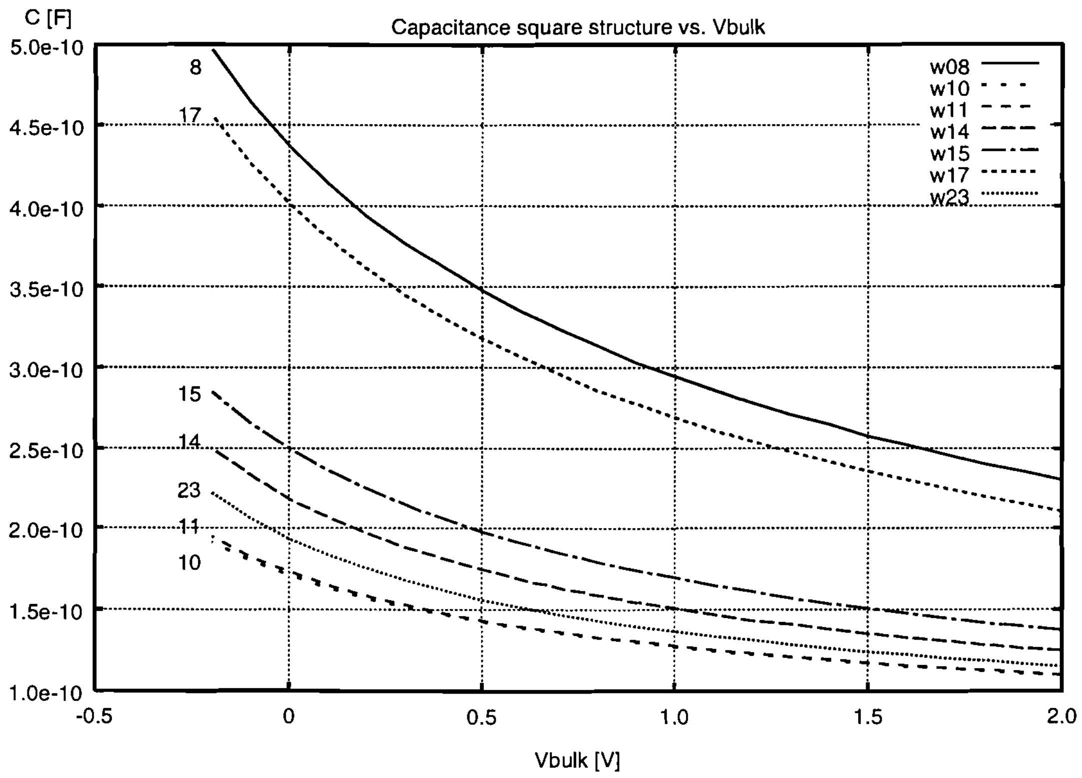
Figure 12: Threshold voltage as function of gate length

length is plotted on a logarithmic scale. This is done because the threshold voltage roll-off only starts at very short channel lengths. Only wafer 8 shows an almost flat threshold voltage curve. Conclusions that can be drawn form the figure are:

- The use of an LDD after spacer etch together with a SPI decreases the roll-off (comparing wafer 10 and 11)
- The concentration of the LDD and SPI has a large influence on the absolute value of the threshold voltage, but not so much on the roll-off (comparing wafer 11 and 14)
- The HDD only together with a SPI results in the largest roll-off

But not only the threshold voltage is important when investigating the influence of new concepts. Also the junction capacitance of the source/drain region to the substrate is important. To investigate the influence of the new concepts on the junction capacitance, measurements have been performed on two test structures: one with a very long sidewall compared to the area (meander), and one square area. The geometries of the two test structures are given below. The results of the capacitance measurements have been plotted in figure 13.

Structure	Area [m^2]	Perimeter [m]
Square	$2.5\ 10^{-7}$	$2.0\ 10^{-3}$
Meander	$2.5\ 10^{-7}$	0.487



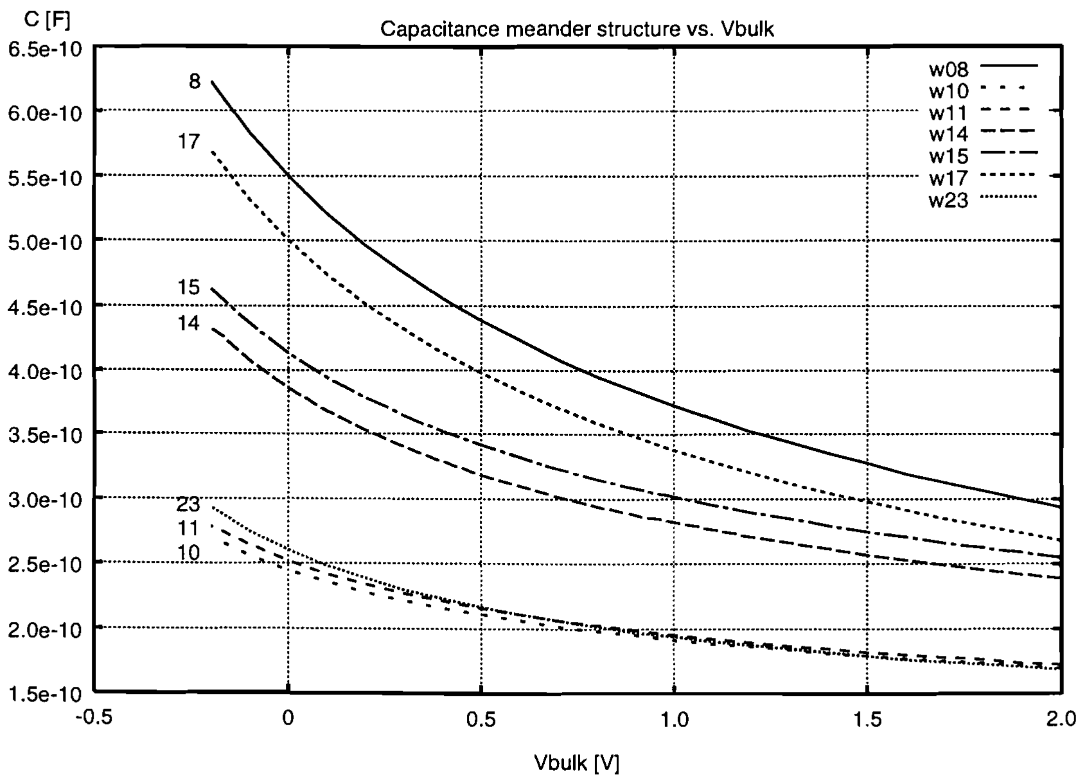


Figure 13: Area and sidewall junction capacitances as function of bulk voltage

The plot of the junction capacitances clearly shows that wafer 8 has the largest junction capacitance. This is caused by the halo implant that increases the substrate doping under the source/drain regions and will thus decrease the depletion width and increase the junction capacitance. Wafer 17 has also a halo implant and a large junction capacitance. One of the disadvantages of the halo implant is that it is not only located at the side of the source/drain junction, but also under the junctions. From the plot of the junction capacitances it can be seen that the SPI also increases the capacitance, but more on the side than at the bottom. Wafer 10 which has had no special implants has clearly the lowest junction capacitance.

These junction capacitance measurements are also used to extract the SPICE BSIM3v3 parameters CJ, MJ, PB, CJSW, MJSW and PBSW. SPICE simulations show that BSIM3v3 can model the junction capacitance as function of the bulk voltage very good.

4.4.3 PL6042, 0.35 μm PMOS devices

The PL6042 is processed in a 0.35 μm CMOS process with a 7 nm gate oxide. This is not a low-voltage technology like the PL5004 and PL7009, but is intended for use with a 3.3 V supply voltage. This run was added later to the measured wafers in order to investigate the difference in noise behavior between an amorphous gate and a poly gate. This investigation was performed because the noise measurements from the PL7009 already showed a large difference in noise behavior between wafer 8 and 23, but because not only the gate material of these wafers is different it is difficult to predict the cause of the difference in noise behavior.

The PL6042 contains, amongst others, two wafers that only differ in the gate material: wafer 3 (amorph) and wafer 8 (poly). Because the noise analysis with BSIM3v3 requires also the DC parameters, measurements with ICCAP have been performed on a WL-array on both wafers. Figure 14 shows the measured and simulated Id-Vg and Id-Vd curves of a large (width=7 μm, length= 7 μm) and a short (width=7 μm, length= 0.5 μm) device from wafer 3 and wafer 8. The Id-Vg curve has been measured at Vds = -50 mV. The Id-Vd curve has been measured at Vg = -1.1 V, Vg = -2.2 V and Vg = -3.3 V.

Figure 14 shows that the modeling, especially in the linear regime, is almost perfect.

Because the, later presented, difference in noise could be related to the mobility, the plot in figure 15 shows the mobility as function of the gate voltage of the two wafers. To plot this function the mobility expression (2) from the BSIM3v3 model is used, together with the extracted SPICE parameters.

The plot shows that the mobility of wafer 3, with amorph, is only slightly higher than the the mobility of wafer 8. This small difference can absolutely not account for the large difference in the observed noise behavior. This again proves that noise analysis, together with DC characterization, is a tool to investigate the influence that new materials and concepts can have on the behavior of the MOSFET.

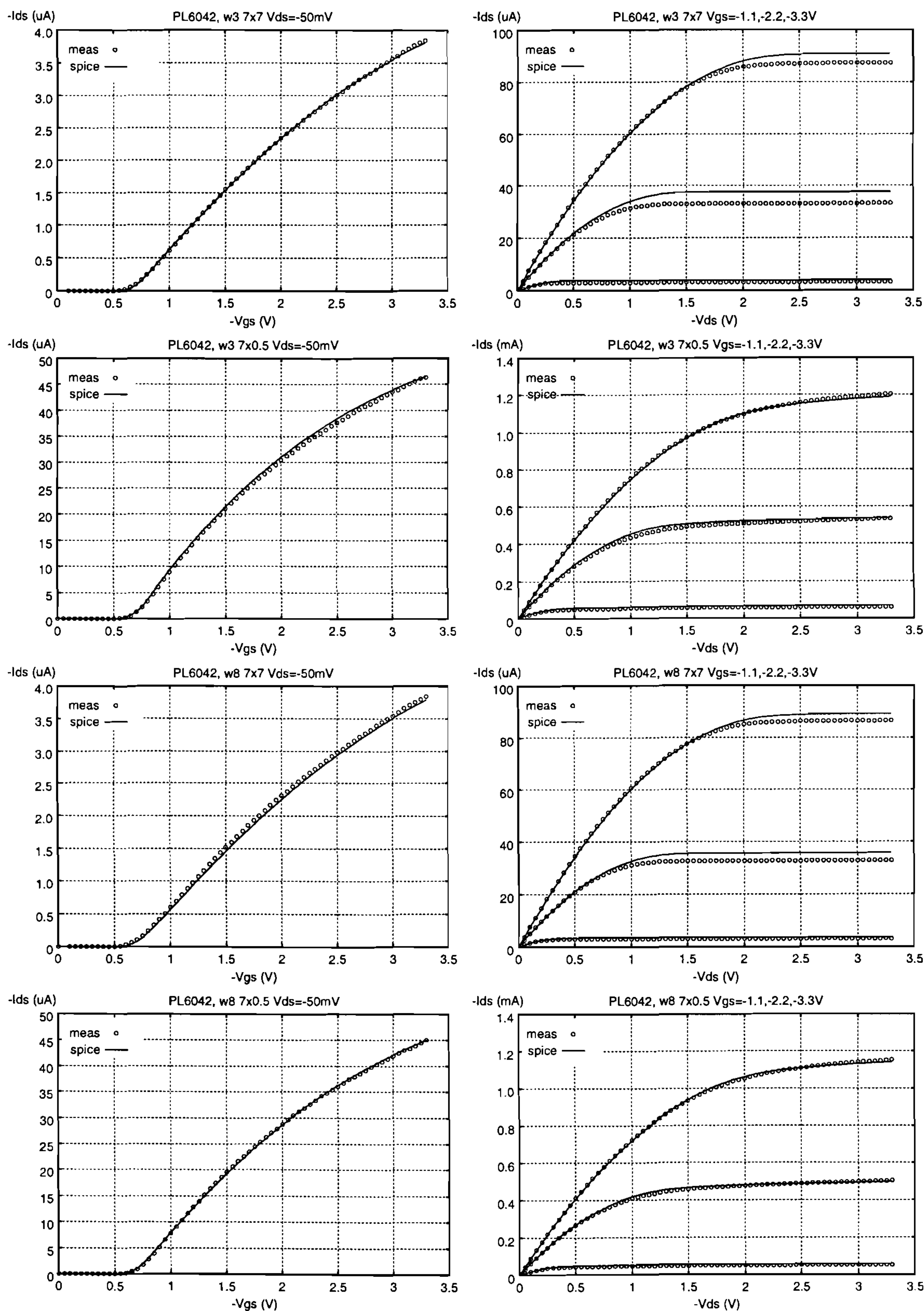


Figure 14: Measured and simulated pMOS id-vg and id-vd curves

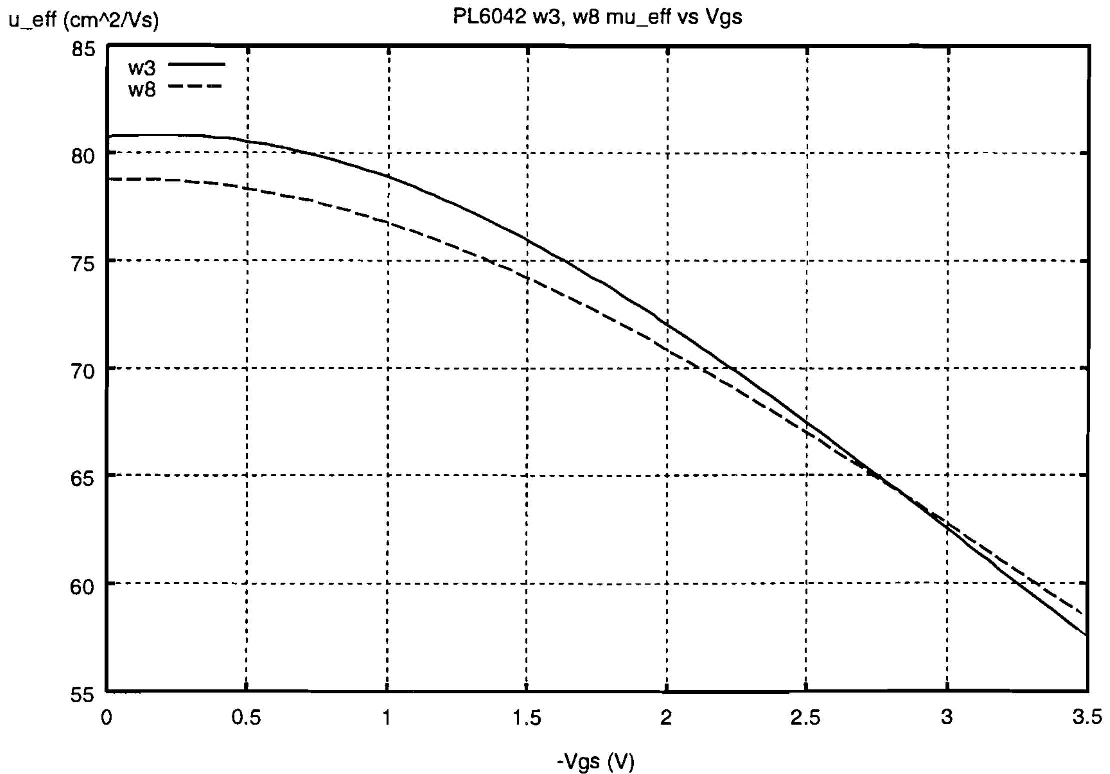


Figure 15: Effective mobility as function of gate voltage

4.5 Conclusions concerning DC characterization

The measurements and simulations presented in this chapter show that the BSIM3v3 SPICE model is capable of modeling a large number of new MOSFET concepts and different process technologies.

The biggest problem in extracting the BSIM3v3 SPICE parameters is the quality of the extraction routines. Often parameters had to be adapted by hand to obtain good simulation results. Also the used extraction routines do not extract all parameters, for example the width dependency of the threshold voltage is not extracted. A new version of the extraction routines will be able to extract more parameters and thus be able to model the MOSFET even better. Another problem is that, before starting an extraction, certain parameters must be known, which can not always be determined very precisely. These are the junction depth XJ (typically between 150 nm and 200 nm) and also the gate oxide thickness. Due to gate depletion there is a difference in the physical and effective electrical oxide thickness. Although BSIM3v3 has a parameter to model this effect (NGATE), it is difficult to use this parameter because its value is also hard to determine precisely. Without knowing the exact values of these parameters, the BSIM3v3 model is capable of modeling the DC behavior very good.

The SPICE models obtained with the current version of the extraction routines are certainly good enough to be used in the noise analysis, which was one of the goals of the DC parameter extraction.

The presented macro-model for halo MOSFETs proved to be able to model these MOSFETs very good. This model can be useful in the noise analysis, when the noise of the halo part would dominate over the noise from the channel. This is investigated in the next chapter.

The disadvantage of such a model is that the SPICE parameters have to be obtained by hand, by means of a trial and error method. This is a time consuming process and it is difficult to obtain the best possible set of parameters.

Because this work does not specifically deal with the investigation of the use of new MOSFET concepts, but rather with the modeling of these special MOSFETs, it is hard to say which concepts are better than others. As can be seen from the presented data, the new concepts have a large influence on the threshold voltage and the junction capacitance. But it is obvious that, without taking special precautions, the classical MOSFET can not be scaled down to sub-micron scale without suffering from short-channel effects. So a well balanced compromise between the possible new concepts will have to be found for each new technology.

5 Noise analysis

Noise measurements can be used as a diagnostic tool to give an indication of the quality of the production process. By adding noise measurements to the standard characterization process it is possible to attain additional information, that would not be known otherwise.

A noise measurement can for example give information about the presence of traps in the channel, the presence of series resistance and the overall quality of the MOSFETs by comparing the Hooge-parameter from one technology to the other.

In this chapter the noise analysis of the different MOSFETs will be explained. First a short introduction on noise is given followed by a more detailed explanation of some existing 1/f noise models. Then the measurement setup is discussed, followed by the actual measurement results and analysis.

5.1 Noise theory

The word "noise" represents all phenomena that relate to spontaneous, natural and complete random fluctuation in mainly electrical components, circuits and systems. Noise is always present and can never be eliminated completely. It is only possible to try to minimize noise. This can be necessary because noise can limit system performance. Because noise is a stochastic signal, it is described in terms of correlation function, variance and spectral intensity.

Different kinds of noise in electrical components are for example Nyquist noise, Generation-Recombination (GR) noise, 1/f or flicker noise and noise related to temperature fluctuations.

The quantity, that is used most to describe the noise, is the Power Spectral Density (PSD). The PSD is a function of the frequency and is defined as:

$$S_v(f) = \overline{\{V(t)\}^2_{f,\Delta f=1Hz}} \tag{4}$$

This means that the PSD at a certain frequency equals the mean squared value of a band filtered signal at that frequency. The PSD can be formed from either a voltage signal ($S_v(f)$ with dimension V^2/Hz) or a current signal ($S_i(f)$ with dimension A^2/Hz).

From the PSD the root-mean-square amplitude of a noise signal, in a certain bandwidth can be calculated via:

$$v_{rms} = \sqrt{\int_{f1}^{f2} S_v(f)\ df} \tag{5}$$

Also the PSD can be used to calculate the variance of a noise signal:

$$\sigma^2 = \int_0^\infty S(f)\ df \tag{6}$$

Modern dynamic signal analyzers can calculate the PSD by applying a Fast Fourier Transform (FFT) on the measured time signal. By changing the measured time interval and time resolution, different parts of the frequency spectrum can be measured accurately.

5.2 Noise sources

Several different noise sources are responsible for noise encountered in semiconductors. In this section a short overview will be given of the different noise sources.

Always present, and unavoidable, is the thermal noise (Nyquist noise), due to the random movement of the electrons. The PSD of thermal noise is:

$$S_v(f) = 4kTR \tag{7}$$

As can be seen, this noise has no frequency dependence, and is therefore often called "white noise". When studying low frequency noise in MOSFETs thermal noise is much smaller than 1/f noise, so this noise source can then be disregarded.

The next noise source is Generation-Recombination (GR) noise. This noise source originates from fluctuations in the conductivity, due to fluctuations of the number of free electrons, which in its turn is caused by generation-recombination mechanisms present in semiconductors. The PSD of this noise source has the following form:

$$S_v(f) \sim \frac{\tau}{1 + (2\pi f \tau)^2} \tag{8}$$

This PSD has a Lorentzian shape: at lower frequencies the PSD is flat, and at a certain frequency (corresponding with the reciprocal time constant of the GR process) the PSD decreases with slope 2. Often several GR-processes can be active at the same time, all with their own amplitude and time constant.

A noise source very similar to GR-noise (actually a special case of GR-noise) is Random Telegraph Signal (RTS) noise, or burst noise. This noise source shows the same PSD as GR-noise, and is caused by trapping of electrons in a single trap. Later on some examples of the time-domain signal and PSD of this noise will be given.

Finally there is 1/f noise. This noise source is called "1/f" because the PSD of this noise source is proportional to 1/f (slope -1). This is the noise source that dominates the low-frequency noise present in MOSFETs. In the next section a more detailed explanation of this noise source will be given.

An example of a typical 1/f noise signal (in the time-domain) is shown in figure 16. The PSD that belongs to such a noise signal is shown in figure 17.

Figure 18 shows the typical noise signal of a MOSFET containing RTS noise. It can be seen that the normal 1/f noise is modulated by a random digital-like signal. That is why this kind of noise is often called Random Telegraph Signal noise or burst noise. The PSD of such a noise signal is shown in figure 19. This PSD shows that there are in this case two GR-spectra (Lorentzian shape) superimposed on a 1/f spectrum. These two GR-spectra make the determination of the 1/f component difficult. Because these GR-spectra can occur at almost any place on top of the 1/f spectrum it is sometimes impossible to recognize the 1/f spectrum. The amplitude of the 1/f noise component can then only be estimated.

Especially in small area MOSFETs and in the subthreshold regime RTS noise can be very large due to the fact that only a small number of electrons are present in the channel. As a rule of thumb the relation $\Delta I/I = 1/N$ can be used, so a change of 1 percent in drain current would indicate that 100 electrons are present in the channel. Deviations from this relation can

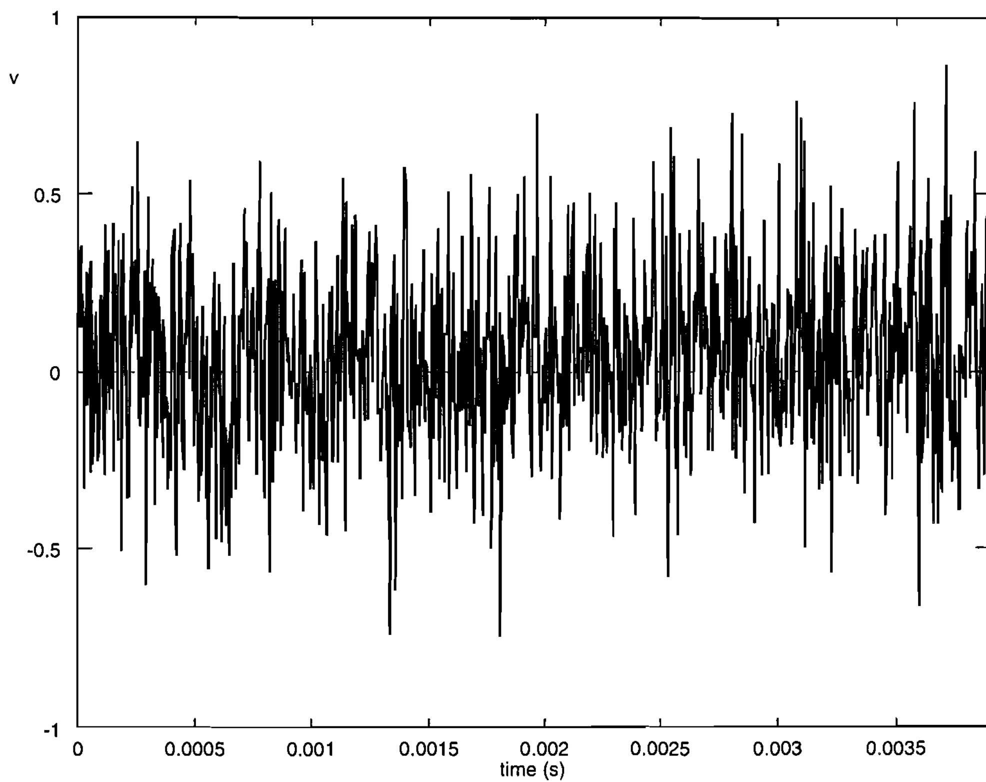


Figure 16: 1/f noise

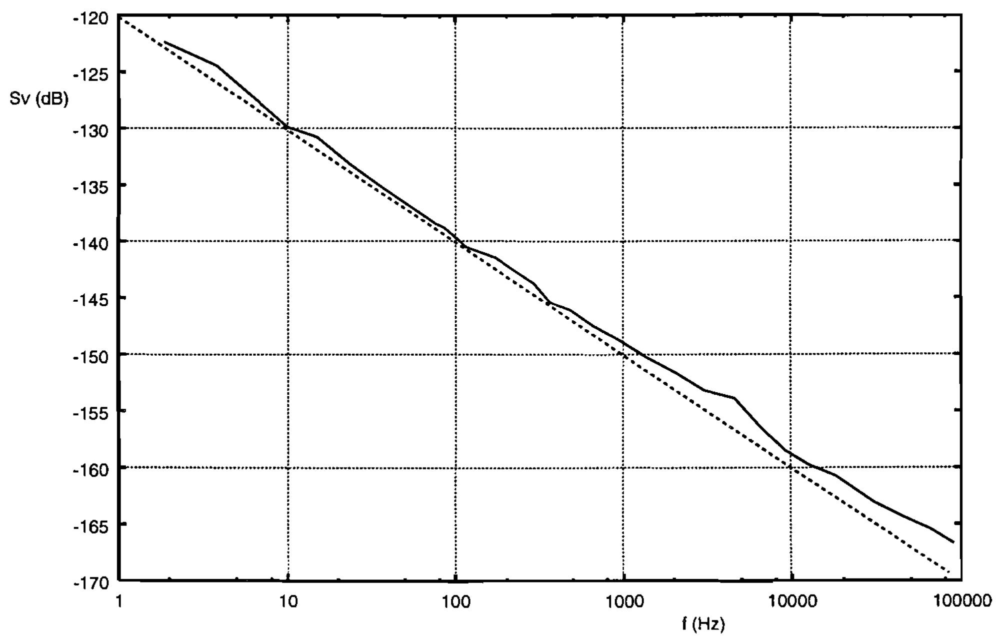


Figure 17: PSD of 1/f noise

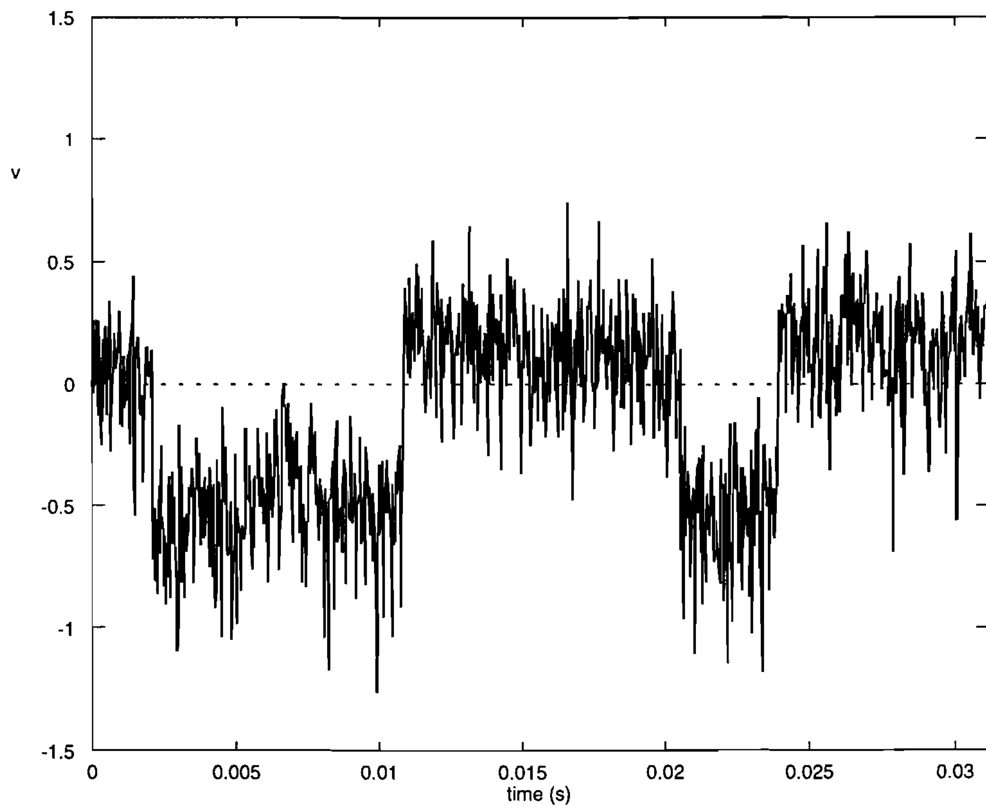


Figure 18: 1/f noise modulated by RTS noise

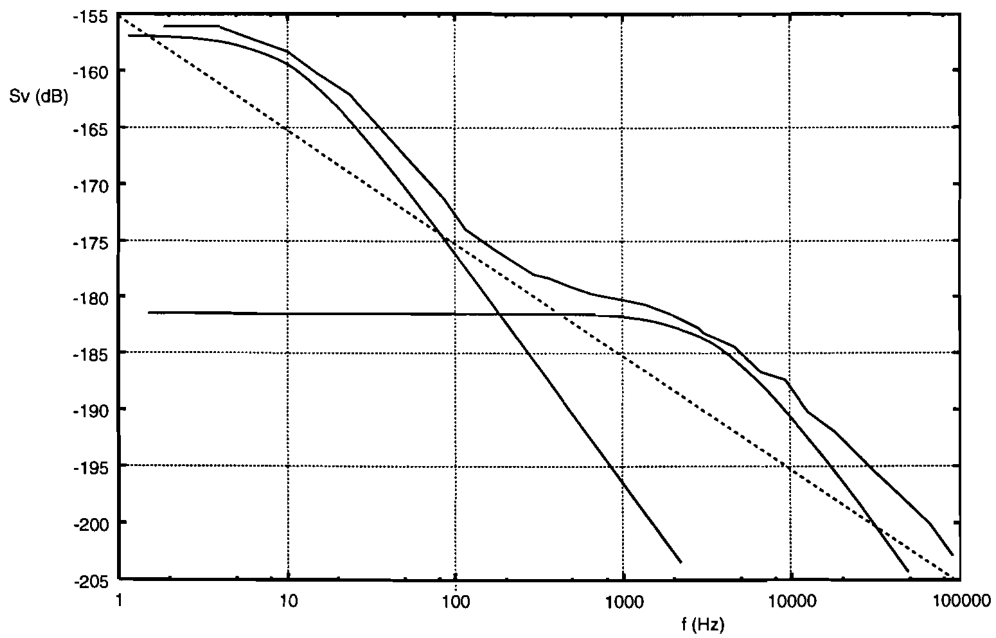


Figure 19: PSD of 1/f noise modulated by RTS noise

occur due to a more or less strategic trap position [12]. Figure 20 and figure 21 show examples of extreme RTS signals that can make the measurement of the 1/f noise component almost impossible. The first figure shows an RTS signal with such a large amplitude, that the low noise amplifiers will be overloaded. The second figure shows a measured RTS signal, which has such a large time constant that the low noise AC amplifier cannot amplify it correctly. As can be seen from these figures, the investigation of RTS noise is a study on its own, and will not be dealt with in this work.

5.3 1/f noise models

For the past 40 years a lot of research has been done to determine the origin of 1/f noise. Still there is no generally accepted explanation for the physical origin of 1/f noise. Different models have been proposed to explain the 1/f behavior of this noise. Two widely used models are the mobility fluctuation ($\Delta\mu$) model and the number fluctuation (ΔN) model. Also unified models that combine the $\Delta\mu$ and ΔN model have been proposed [13].

In the next sections an introduction will be given into the ideas behind these models, the method of calculating the noise and the final current noise expressions.

5.3.1 ΔN and $\Delta\mu$ model

The ΔN and $\Delta\mu$ model each consider the dominant noise to be coming from only one effect, respectively fluctuations in the number of electrons (holes) and fluctuations in the mobility. Fluctuations in the current are fluctuations in the conductivity σ, and since $\sigma = nq\mu$ both n and μ can be the cause of these fluctuations. Many experiments have been performed in the past to collect data both in favor of the ΔN and $\Delta\mu$ model. From these data it can be concluded that mobility fluctuations are always present in semiconductors and that superimposed on mobility noise there can be other types of noise, like number fluctuation noise, generated at the surface of a semiconductor [14]. It seemed that in nMOS devices the ΔN model was dominant, and in pMOS devices the $\Delta\mu$ model. This can be explained by the fact that pMOS devices used to be bulk-operated devices, which means that the current flows in the bulk of the semiconductor, far away from the surface and no number fluctuations could occur. In nMOS devices the current flows directly under the gate oxide, and therefore number fluctuations can be dominant.

But nowadays pMOS devices are also often surface-operated devices, due to the use of p+ poly gates, and as will be shown later on the measured pMOS devices also show number fluctuations noise.

The ΔN model states that the 1/f noise is caused by fluctuations in the number of electrons (holes), due to trapping of electrons at interface and oxide traps. The 1/f spectrum is formed by adding the GR-spectra from all traps. This requires that traps are distributed uniformly. The generation of the 1/f spectrum is depicted in figure 22. Consequence of this theory is that 1/f noise only has a 1/f spectrum in the frequency range between the slowest and fastest trap.

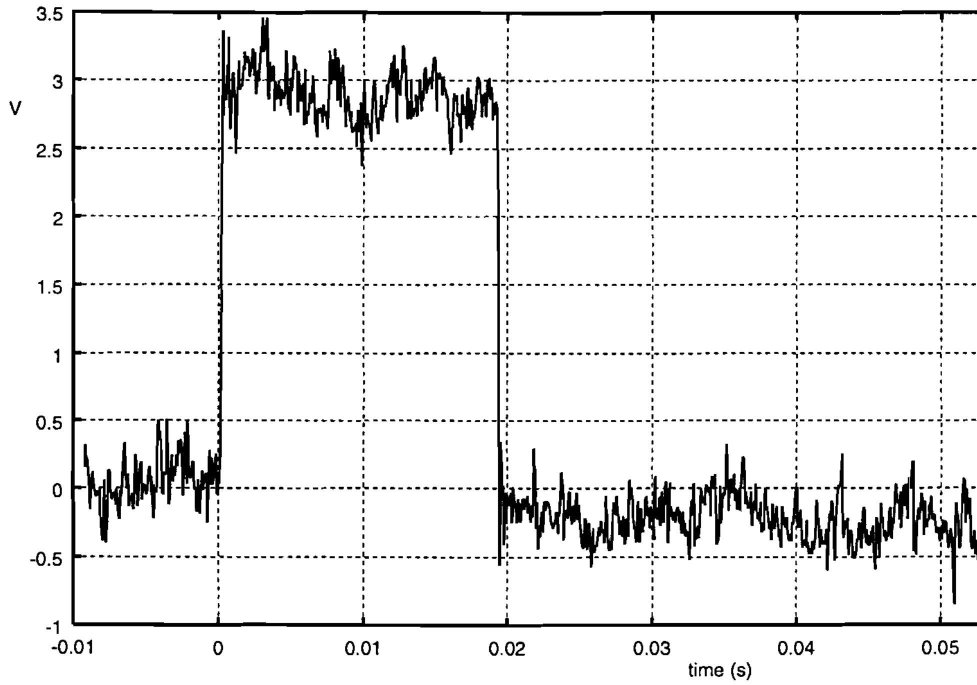


Figure 20: Time signal of extreme RTS noise

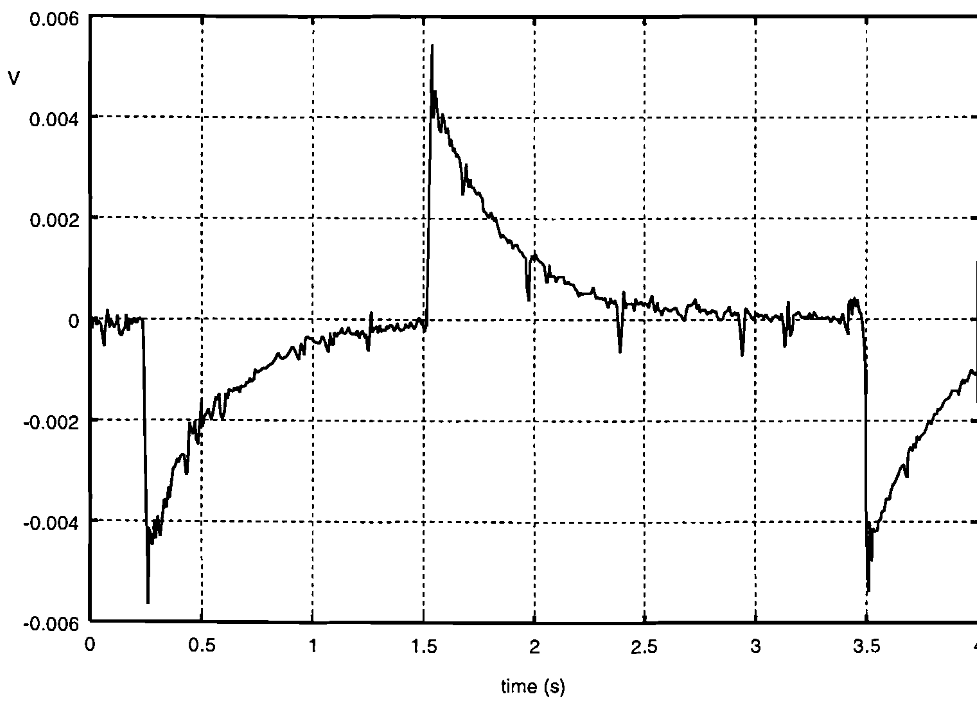


Figure 21: Time signal of very slow RTS noise

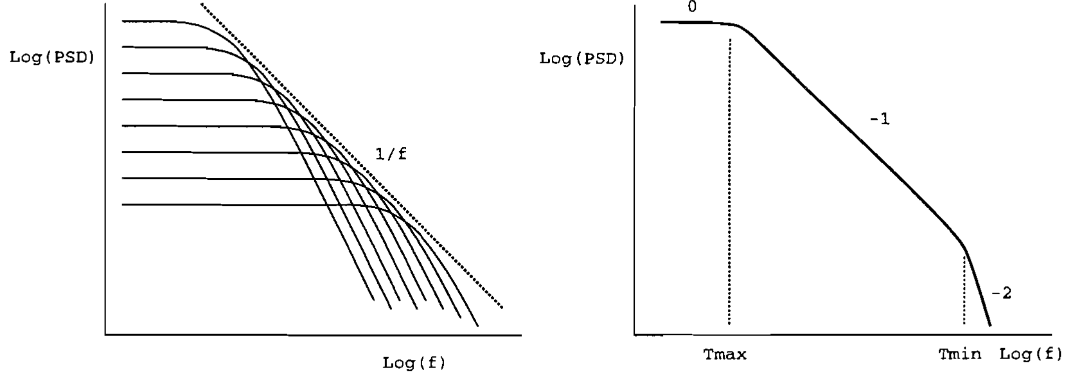


Figure 22: Generation of 1/f spectrum

The $\Delta\mu$ model states that the noise is caused by fluctuations in mobility, due to crystal lattice vibrations. This model does not explain the 1/f nature of the noise spectrum but started with an empirical relation [15]:

$$\frac{S_R}{R^2} = \frac{S_I}{I^2} = \frac{\alpha}{fN} \tag{9}$$

In this relation α, often called the Hooge parameter, is closely related to the quality of the bulk semiconductor material. Values between 4 10^{-7} for bulk-operated p-MOSFETs and 3 10^{-5} for surface-operated devices have been observed [16]. The surprising result is that equation 9 holds for all kinds of homogeneous semiconductors. The parameter α can depend on the mobility via [17]:

$$\alpha_{meas} = \left(\frac{\mu_{eff}}{\mu_0}\right)^2 \alpha_{latt} \tag{10}$$

In this expression α_{meas} is the measured α from expression (9), μ_{eff} is the effective mobility, μ_0 is the mobility when only lattice scattering would be present, and α_{latt} is the Hooge parameter related to material with only lattice scattering present. When assuming $\Delta\mu$ fluctuations, α is independent of the biasing of the MOSFET, in case of constant mobility. Mobility degradation causes a decrease of the apparent α for increasing gate bias. Expression (9) can also be used to model noise from ΔN fluctuations. In that case α is inversely proportional to the gate overdrive voltage ($V_g^* = V_{gs} - V_{th}$) [18].

Since expression (9) is only valid for true homogeneous samples, a more complex expression is needed to model noise in a MOSFET. The noise in a MOSFET can be calculated by considering the MOSFET channel as a piece of semiconductor in which the number of free charge carriers $n(x)$ depend on the place in the channel. This leads to the following expression for the drain-source current noise in the linear regime [18]:

$$S_{Ids}(f) = \frac{\alpha}{f} \frac{q\mu I_{ds} V_{ds}}{L^2} \tag{11}$$

In the saturation regime the current noise PSD becomes:

$$S_{Ids}(f) = \frac{\alpha}{f}\frac{2I_{sat}^2}{N} \tag{12}$$

with

$$I_{sat} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2 \;\; and \;\; N = \frac{C_{ox}WL(V_{gs} - V_{th})}{q}$$

In expression (11) and (12) only 1/f noise is taken into account. Because this study only deals with the low-frequency noise of the MOSFET the Nyquist noise is negligible with respect to the 1/f noise. The GR noise is very unpredictable, because the location and presence of traps is not known. When performing noise measurements, the GR noise can be easily recognized, and the amplitude of the 1/f noise can be estimated by looking at the plot of the PSD versus the frequency.

With the help of these expressions the dominant noise model can be determined. The most simple way to do this, is to plot α versus the gate overdrive voltage V_g^* on a log-log scale. The $\Delta\mu$ model predicts that α is independent of V_g^*, not taking into account the mobility degradation. The ΔN model predicts that α is inversely proportional to V_g^*. But as can be seen later on, α can be a more complex function of V_g^*. Then a unified model can be used to explain the behavior of α. Such models incorporate both the number fluctuation model and the surface mobility fluctuation model. The latter is attributed to fluctuations in the scattering effect due to fluctuating oxide charges. This implies that the mobility fluctuation is correlated to the number fluctuation. In the next sections some other 1/f noise models will be discussed.

Because in other noise models also a parameter α is being used, the Hooge parameter α will further on be denoted by α_H.

5.3.2 The Reimbold subthreshold ΔN model

The 1/f model presented by Reimbold [19] is a ΔN model with some additions for modeling the noise in the subthreshold region. The model starts with the assumption that the 1/f noise is caused by fluctuations in the number of electrons, but distinguishes between fluctuations in the number of electrons and fluctuations in the number of occupied traps:

$$\frac{S_{Id}}{I_d^2} = \frac{S_N}{(WLN)^2} = \frac{S_{Nt}}{(WLN)^2}\left(\frac{\delta N}{\delta N_t}\right)^2 \tag{13}$$

N_t is the number of occupied traps per unit area, N is the number of electrons per unit area present in the channel and W and L are the width and length of the transistor.

The ratio between the fluctuations in the number of electrons δN and the number of occupied traps δN_t is given by:

$$R = \left|\frac{\delta N}{\delta N_t}\right| = \frac{\beta Q_n}{Cox + Cd + Cit + \beta Q_n} \tag{14}$$

with $\beta = (q/kT)$, $Q_n = qN$ the channel charge per unit area and Cox, Cd and Cit respectively the gate oxide capacitance, the depletion capacitance and the interface capacitance per unit area.

It has been shown that the ratio R strongly varies with bias from weak inversion (typically $R \approx 10^{-10}$) to strong inversion ($R = 1$).

Substituting expression (14) and $\beta Q_n = q^2N/kT$ into expression (13) gives:

$$\frac{S_{Id}}{I_d^2} = \frac{S_{Nt}}{(WL)^2} \frac{q^4}{(kT)^2} \left(\frac{1}{Cox + Cd + Cit + \beta Q_n} \right)^2 \tag{15}$$

The spectral density of the fluctuations of the number of occupied traps is given by:

$$S_{Nt} = \frac{N_t kTWL\lambda}{f} \tag{16}$$

with N_t the volume oxide trap density in $CV^{-1}m^{-3}$ and λ the tunnel penetration depth. Substituting this expression in the previous one leads to the expression for the relative current power spectral density, which is valid from weak to strong inversion in the linear regime (i.e. $V_{ds} \ll V_{gs}$):

$$\frac{S_{Id}}{I_d^2} = \frac{q^4\lambda}{fkTWL} \frac{Nt}{(C_{ox} + Cd + Cit + \beta Q_n)^2} \tag{17}$$

In weak inversion $|\beta Q_n| \ll (Cox + Cd + Cit)$, so

$$\frac{S_{Id}}{I_d^2} = \frac{q^4\lambda}{fkTWL} \frac{Nt}{(C_{ox} + Cd + Cit)^2} \tag{18}$$

In the saturation regime Qn is a function of the position along the channel and has to be substituted with an expression for $Q_n(x)$. Because in weak inversion $\beta Q_n \ll (Cox+Cd+Cit)$, expression (18) is valid in both the linear and the saturation regime.

Later on the validity of this model will be checked with the measured noise spectra.

5.3.3 The $\Delta N - \Delta\mu$ model

This model, presented by [13], uses both the number fluctuation theory and the surface mobility fluctuations theory. Several groups use this unified theory to obtain noise expression, for example Hung et al. [20] and Ghibaudo et al. [21]. In this section the approach described by Ghibaudo et al. will be presented. The next section will describe the approach followed by Hung et al., which leads to the BSIM3v3 noise model.

Ghibaudo et al. uses a noise expression which is said to be valid in all operating regimes and from weak to strong inversion [21]. The used noise mechanisms consist of both number fluctuations and correlated surface mobility fluctuations. Correlated surface mobility fluctuations are caused by fluctuations in scattering due to fluctuations in trapped charges. In this model fluctuations in the drain current are related to fluctuations in flat-band voltage, which modulates, via the transconductance g_m, the current, as shown by Christensson et al. [22]. Fluctuations in flat-band voltage originate from the fluctuating charge in the gate oxide.

Fluctuations in the drain current can be expressed as:

$$\delta I_d = \delta V_{fb} \frac{\partial I_d}{\partial V_{fb}} + \delta \mu_{eff} \frac{\partial I_d}{\partial \mu_{eff}} \tag{19}$$

To evaluate $\delta\mu$ Matthiessen's rule is used:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_0} + \alpha Q_{ss} \tag{20}$$

with Q_{ss} the interface charge per unit area and α the scattering parameter in Vs/C. From the previous expression follows that $\delta\mu_{eff} = -\alpha\mu_{eff}^2 \delta Q_{ss}$.

When assuming no influence from velocity saturation effects, the following two approximation can be made:

$$\begin{aligned} \partial I_d / \partial \mu_{eff} &\approx I_d / \mu_{eff} \\ \partial I_d / \partial V_{fb} &\approx -g_m \end{aligned}$$

These expressions may not be valid for short channel devices. When using these two substitutions and substituting $\delta Q_{ss} = -C_{ox}\delta V_{fb}$ equation (19) becomes:

$$\frac{S_{Id}}{I_d^2} = \left(1 + \alpha\mu_{eff} C_{ox} \frac{I_d}{g_m}\right)^2 \frac{g_m^2}{I_d^2} S_{Vfb} \tag{21}$$

The scattering parameter α is also used in the BSIM3v3 noise model, but is then expressed in Vs instead of Vs/C. To avoid misunderstandings, only one parameter will be used to indicate the scattering parameter, namely α_S, expressed in Vs, so $\alpha_S = \alpha\ q$.

The expression for the fluctuations in the flat-band voltage is taken from [22]:

$$SV_{fb} = \frac{q^2 kT \lambda N_t}{WL C_{ox}{}^2 f} \tag{22}$$

with λ the tunnel penetration depth ($\lambda \approx 0.1nm$) and N_t the volume oxide trap density in $CV^{-1}m^{-3}$.

In the subthreshold region the number fluctuation noise dominates, and [21]

$$\frac{Id}{g_m} = \frac{kT}{q} \frac{C_{ox} + Cd + Cit}{C_{ox}} \tag{23}$$

Combining these equations gives:

$$\frac{S_{Id}}{I_d^2} = \frac{q^4 \lambda}{fkTWL} \frac{Nt}{(C_{ox} + Cd + Cit)^2} \tag{24}$$

This is exactly the same result as presented by Reimbold and is also the same as in the BSIM3v3 noise model.

In the linear regime both number fluctuations and the correlated surface mobility fluctuations are active. Substituting S_{Vfb} and $g_m/I_d = C_{ox}/qN$, with N the number of carriers per unit area, in equation (21) gives:

$$S_{Id} = \frac{kT\lambda I_d^2}{fWL}\left(\frac{1}{N} + \alpha_S\mu\right)^2 N_t \tag{25}$$

By substitution of g_m/I_d in equation (21) by experimentally obtained values, the 1/f noise is calculated in all operating regimes.

5.3.4 The BSIM3v3 noise model

This model was first presented in [20]. Like the $\Delta N - \Delta\mu$ model it incorporates both the number fluctuation theory and the correlated surface mobility fluctuation theory. This unified model is also implemented in the BSIM3v3 model [23], but with some differences. As will be shown later on, the SPICE implementation of this model contains some constants, that are actually technology dependent parameters.

First the manual derivations of the noise equations will be given (only for the weak inversion and linear regime). Later on the SPICE implementation of this model is presented. The derivation start with the following expression for the drain current in the linear regime:

$$I_d = W\mu qNE_x \tag{26}$$

Assuming that both the mobility and the electron density can change and, like Reimbold did, that the fluctuations in the number of free electrons do not have to correspond with the fluctuations in the number of occupied traps, gives:

$$\frac{\delta I_d}{I_d} = \frac{\delta\mu}{\mu} + \frac{\delta\Delta N}{\Delta N} = \left(\frac{1}{\mu}\frac{\delta\mu}{\delta\Delta N_t} + \frac{1}{\Delta N}\frac{\delta\Delta N}{\delta\Delta N_t}\right)\delta\Delta N_t \tag{27}$$

With $\Delta N = NW\Delta x$ and $\Delta N_t = N_tW\Delta x$. N and N_t are densities per unit area. ΔN and ΔN_t are numbers of electrons in a small strip with width W and length Δx. Like Reimbold did, the ratio between the fluctuations in the number of free electrons to the fluctuations in the number of occupied traps can be expressed as:

$$R = \left|\frac{\delta\Delta N}{\delta\Delta N_t}\right| = \frac{\frac{q^2N}{kT}}{C_{ox} + C_d + C_{it} + \frac{q^2N}{kT}} = \frac{N}{N + N^*} \tag{28}$$

with

$$N^* = \frac{kT}{q^2}(C_{ox} + C_d + C_{it}) \quad \text{per unit area} \tag{29}$$

and N the number of carriers per unit area.

To evaluate $\delta\mu/\delta N_t$ Matthiessen's rule is used:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_0} + \frac{1}{\mu_{ox}} = \frac{1}{\mu_0} + \alpha_S N_t \tag{30}$$

The parameter α_S is the coulombic scattering coefficient in $[Vs]$.

Matthiessen's rule leads to:

$$\frac{\delta \mu_{eff}}{\delta \Delta N_t} = -\frac{\alpha_S \mu_{eff}^2}{W \Delta x} \tag{31}$$

Substituting this result leads to the following relative drain current fluctuation:

$$\frac{\delta I_d}{I_d} = -\left(\frac{R}{N} + \alpha_S \mu\right) \frac{\delta \Delta N_t}{W \Delta x} \tag{32}$$

and the power spectral density of the local current fluctuations:

$$\frac{S_{\Delta Id}}{I_d^2} = \left(\frac{R}{N} + \alpha_S \mu\right)^2 \frac{S_{\Delta N_t}}{(W \Delta x)^2} \tag{33}$$

With

$$S_{\Delta N_t} = N_t \frac{kTW \Delta x}{\gamma f} \tag{34}$$

and

$$S_{id} = \frac{1}{L^2} \int_0^L S_{\Delta Id} \Delta x dx \tag{35}$$

and assuming that in the linear regime the x dependencies are negligible, does this result in:

$$S_{id} = \frac{kT I_d^2}{\gamma f W L} \left(\frac{R}{N} + \alpha_S \mu_{eff}\right)^2 N_t \tag{36}$$

In weak inversion the ΔN influence dominates, and the $\alpha_S \mu_{eff}$ can be left out. Since $N \ll N^*$, R/N becomes equal to $1/N^*$. This results in (with $\lambda = 1/\gamma$):

$$\frac{S_{Id}}{I_d^2} = \frac{kT}{\gamma f W L} \frac{N_t}{N^{*2}} = \frac{q^4 \lambda}{f k T W L} \frac{Nt}{(C_{ox} + Cd + Cit)^2} \tag{37}$$

which is the same as the expressions obtained by Reimbold and reformulated by Ghibaudo et al.

5.3.5 SPICE implementation and noise parameter extraction

To obtain a more flexible model, the trap density N_t is not taken constant, and the x-dependencies are taken into account. To do this, three new parameters, A in $[CV^{-1}m^{-3}]$, B in $[CV^{-1}m^{-1}]$ and C in $[CV^{-1}m]$ are introduced:

$$N_t(1 + \alpha_S \mu_{eff} N R^{-1})^2 = A + BN + CN^2 \tag{38}$$

Next, equation (35) is solved for the different operating regimes, resulting in three drain current noise equations for the linear region, saturation region and the subthreshold region. The expression for the linear regime is:

$$S_i(f) = \frac{v_{tm}q^2 I_{ds}\mu_{eff}}{fL_{eff}^2 C_{ox}10^8}[N_{oia}log(\frac{N_0 + 2\ 10^{14}}{N_l + 2\ 10^{14}}) + N_{oib}(N_0 - N_l) + 0.5N_{oic}(N_0^2 - N_l^2)] \quad (39)$$

with v_{tm} equal to kT/q, L_{eff} the effective channel length, N_{oia}, N_{oib} and N_{oic} the three BSIM3v3 noise parameters, N_0 the the charge density at the source side and N_l the charge density at the drain side. For the saturation regime the current noise expression is the same as for the linear regime, added with the following extra term:

$$S_i(f) = eq.(39) + \frac{v_{tm}I_{ds}^2 \Delta L_{clm}}{fL_{eff}^2 W_{eff}10^8}\frac{N_{oia} + N_{oib}N_l + N_{oic}N_l^2}{(N_l + 2\ 10^{14})^2} \quad (40)$$

with ΔL_{clm} a measure for the channel length reduction in saturation and W_{eff} the effective channel width. For the subthreshold region the noise expression is:

$$S_i(f) = \frac{S_{limit}\ S_{wi}}{S_{limit} + S_{wi}} \quad (41)$$

with S_{limit} the current noise calculated at $V_{gs} = V_{th} + 100mV$ and S_{wi} given by:

$$S_{wi} = \frac{N_{oia}v_{tm}I_{ds}^2}{W_{eff}L_{eff}f4\ 10^{36}} \quad (42)$$

These expressions and further definition of parameters can be found in the BSIM3v3 manual [10].

In the BSIM3v3 model, the parameter N^* is taken constant ($N^* = 2\ 10^{14}\ m^{-2}$), whereas this parameter is strongly dependent on the oxide thickness. This results in an inaccurate modeling of noise in the subthreshold region. Also the noise expressions are presented in a slightly different way, due to which the BSIM3v3 noise parameters, NOIA, NOIB and NOIC, have a different value than the original three parameters, A, B and C, as can be seen in equations (43) and (44).

To extract to BSIM3v3 noise parameters, the following procedure is used:

First of all, only two parameters are actually used. The third parameter can than be calculated from the other two parameters.

To extract the parameter N_t, noise measurements in the subthreshold region are necessary, because, according to the models, this parameter entirely determines the noise in the subthreshold region. When plotting the relative current noise PSD (S_I/I^2) as function of the frequency, a plateau value should appear. With this plateau value and equation (18), (24) or (37) the value of N_t can be calculated. The value of $C_{ox} + C_d + C_{it}$ can be calculated with equation (23) from experimentally obtained data.

The second parameter, α_S, is obtained by fitting the calculated noise from equation (36) with the measured noise in the linear range.

Now the parameters A,B and C can be calculated:

$$A = N_t \quad B = 2N_t\alpha_S\mu_{eff} \quad C = N_t\alpha_S^2\mu_{eff}^2 = B^2/4A \tag{43}$$

The BSIM3v3 SPICE noise parameters can be calculated with:

$$NOIA = Aq/100 \quad NOIB = Bq/100 \quad NOIC = Cq/100 \tag{44}$$

5.3.6 Summary on noise models

In this section an overview will be given of the presented noise models. Also some plots are given to shows the influence of the various noise mechanisms.

The noise model presented by McWhorter assumes that only number fluctuations are dominant. Hooge's empirical relation assumes noise to be a bulk phenomenon, later on lattice scattering fluctuations were considered as the 1/f noise source. These models do not explain the noise behavior in the subthreshold region. Reimbold made an addition to the number fluctuation model to include the subthreshold region. The approach followed by Hung et al. and Ghibaudo et al. results in the same noise expressions. In both approaches noise is assumed to arise from number fluctuations and correlated surface mobility fluctuations. These two models are said to be valid in all operating regimes, from weak to strong inversion, and from the linear to the saturation regime. Not included in these models is the bulk mobility fluctuation, although experiments have been performed to show that this kind of noise is always present in all semiconductors. In the past this noise mechanism was often dominant in pMOS devices, because these devices were bulk operated MOSFETs, due to the use of an n-poly gate. Bulk operated pMOS devices were usually less noisy than surface operated devices. This indicates that noise produced at the surface of a MOSFET is larger than noise from bulk mobility fluctuations. But nowadays pMOS devices are often produced with a p-poly gate, which makes these devices surface operated, just like nMOS devices.

It is most likely that there is not one noise mechanism that causes the 1/f noise, but that there are several mechanisms active at the same time, and that, depending on the bias condition, one mechanism is dominant.

In weak inversion both $\Delta N - \Delta\mu$ models assume that noise stems from number fluctuations, and thus result in the same noise expression. The difference in noise simulation between expression (17) presented by Reimbold and expression (21)presented by Ghibaudo et al. is shown in figure 23. The noise calculations have been performed with experimental data from the PL7009 wafer 8 on a device with $W/L = 10/5.0\ \mu m$ at Vds=-50mV. The two noise parameters are chosen the following values: $N_t = 1.7\ 10^{41}\ CV^{-1}m^{-3}$ and $\alpha_S = 5.7\ 10^{-15}\ Vs$ Both expressions predict the same plateau level, but at higher gate voltage correlated surface mobility fluctuations can increase the noise. Noise measurements on p-MOSFETs have indeed shown that this increase in noise does occur, so it is likely that the influence of correlated surface mobility fluctuations is present, and that the Reimbold noise model is only valid in the subthreshold region for these p-MOSFETs. But when looking only to noise simulations in the linear regime, also Hooge's empirical relation can be used. This expression also predicts a slope -1 for the relative current noise in the linear regime, when assuming $\Delta\mu$ fluctuations.

In the linear regime the results from the $\Delta N - \Delta\mu$ models are the same, when R=1. The model from Reimbold differs in the linear regime, because only number fluctuations are assumed, and

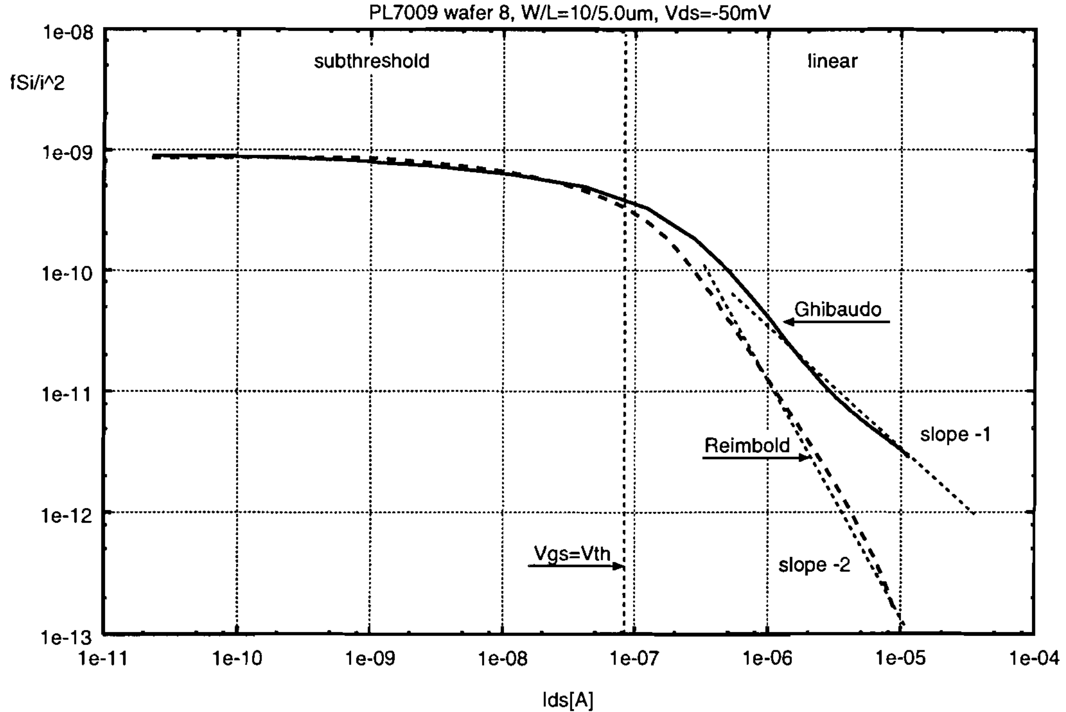


Figure 23: Relative pMOS current noise from weak to strong inversion

no correlated surface mobility fluctuations. In all cases the noise can be described by the use of one or two parameters (α_S and N_t). Figure 24 shows the influence of the different noise mechanisms as function of the bias condition. To obtain this plot measured bias data is used from a PL7009 wafer 8 device with $W/L = 10/5.0$ μm and Vds=-50mV, and equation (36) is used to calculate the current noise (with R=1). $N_t = 1\ 10^{41}\ CV^{-1}m^{-3}$ and $\alpha_S = 6\ 10^{-15}\ Vs$. These values are very close to the values, that will be extracted for this wafer. The total noise plotted in this figure corresponds with the noise as presented by equation (36), ie. the summation of the delta-N part, the correlation part and the delta-μ,surface part. Also plotted in this figure is the drain current noise as predicted by empirical relation (9), with α_H = 1.0 10^{-5}. This noise stems from bulk mobility fluctuations only. The plot shows clearly the influence of the two noise mechanisms. The number fluctuation model causes a current noise that is independent of the gate voltage except the small deviation from a horizontal line due to mobility degradation. The surface mobility fluctuation model causes a current noise that depends quadratically on the gate voltage. Then there is the correlation part that, when using only two parameters to describe the noise, can not be scaled independently from the ΔN or $\delta\mu_{surface}$ curves. This correlation part shows exactly the same dependence on the gate voltage as the bulk mobility fluctuation model with a slope +1. The total noise is obtained by adding up the three individual contributions.

In figure 25 the influence of the noise mechanisms on α_H is shown. In this case α_H is calculated with empirical relation (9). Number fluctuations cause an α_H value that is inversely proportional to the gate voltage, and the correlation part causes a constant α_H value. The surface mobility fluctuations are responsible for an increasing value of α_H at higher gate voltages. As will be shown later on, the α_H curve corresponds very good with the measured alpha.

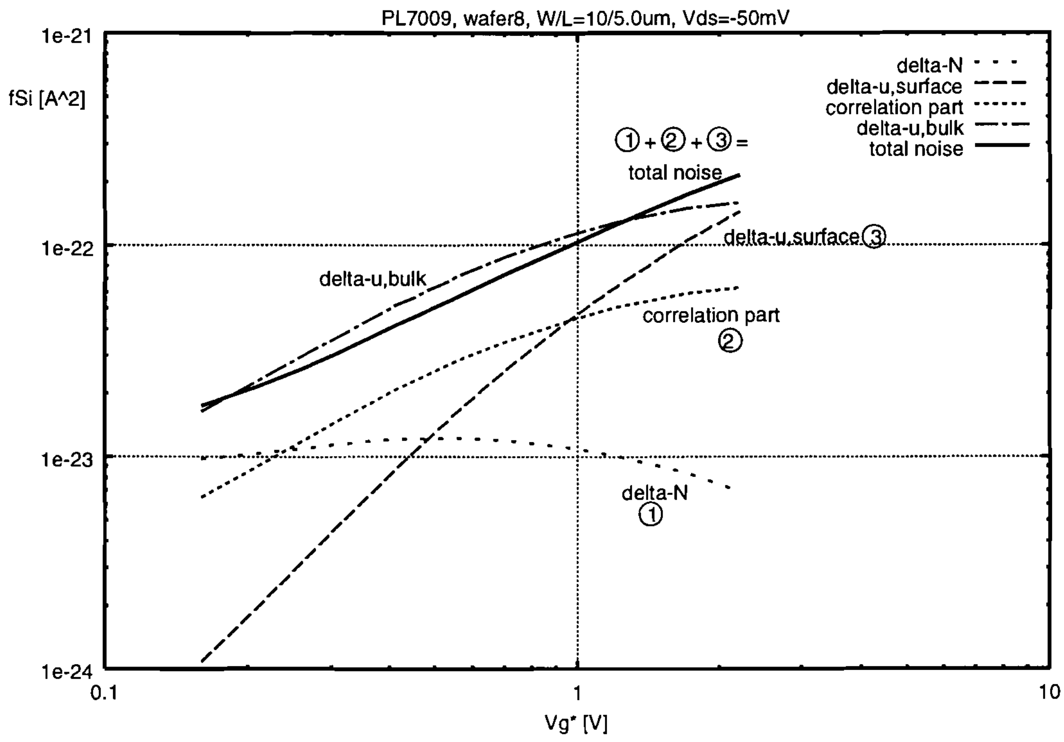


Figure 24: Current noise in the linear regime

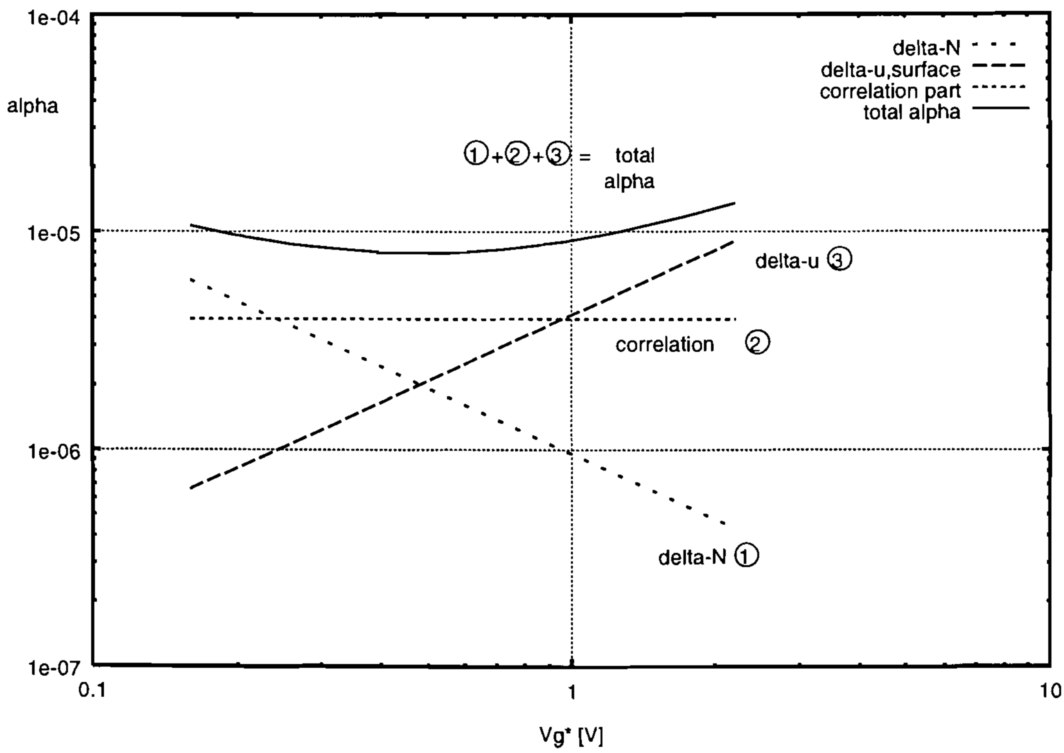


Figure 25: Alpha in the linear regime

5.3.7 Model shortcomings

The two oldest models, the bulk mobility fluctuation model and the number fluctuation model, can often be used to simulate noise in the linear and saturation regime. But these two models can not explain the noise in the subthreshold regime. The predicted relative current noise scales for the straightforward bulk mobility fluctuation model with $1/N$ and for the McWhorter model with $1/N^2$. In the subthreshold region N becomes very small, so the current noise would become very large. Often measurements show that the noise does not increase when N becomes lower, but a certain plateau level is reached. To explain this plateau, changes have to be made to the original models. For the number fluctuation model these modifications have been made by several groups.

The model presented by Reimbold is also a number fluctuations model and contains the additions necessary to make this model applicable to the subthreshold region. This model is often not capable of simulating the noise in strong inversion correctly, especially for p-MOSFETs.

The models presented Hung et al. and Ghibaudo et al. are capable of simulating the noise in all operating regimes. But in the calculations, made to arrive at the final noise expression, some approximations have been performed, that may not be valid for all bias conditions. This makes the physical background of this models more difficult to understand.

Since the BSIM3v3 noise model uses separate expressions for the different operating regimes, discontinuities occur in the noise simulations, when switching from one operating regime to another. The noise expression presented by Ghibaudo et al. is a continuous expressing, valid in all operating regimes. When using this expression, the continuity of the noise simulation depends on the expression used for the drain current and transconductance. In [24] a drain current expression is presented that, when using expression (21) presented by Ghibaudo et al., results in a noise expression with an infinite order of continuity through all operating regimes.

Since this work is not concerned with finding the physical background of noise, it is hard to say which model represents physical realty the best. It is difficult to understand how, for example in the subthreshold region, a 1/f noise spectrum can arise from number fluctuations, when only a very small number of electrons are present in the channel.

5.4 Noise measurement setup

The measurement setup, used to measure the drain-source voltage noise is shown in figure 26. This setup consists of the following elements:

- Bias-box: this box is being used to put the MOSFET in a certain bias condition. The battery voltage can be selected (from 1.5 V, 3.0 V, 4.5 V etc.). The gate voltage is selected by means of a potentiometer and the drain voltage can be adjusted in steps by selecting different resistors (330, 1k, 3k3, 10k etc).
- Ultra Low Noise voltage amplifier (Brookdeal 5004). Amplification +60 dB, equivalent noise resistance 40 Ω, above 1 kHz.
- Precision ac-voltage amplifier (Brookdeal 9452). Frequency range 1 Hz to 1 MHz, amplification 30,40,...,100 dB.
- HP 35665A Dynamic signal analyzer containing software that automatically measures the power spectral density of the noise from 1 Hz to 100 kHz.

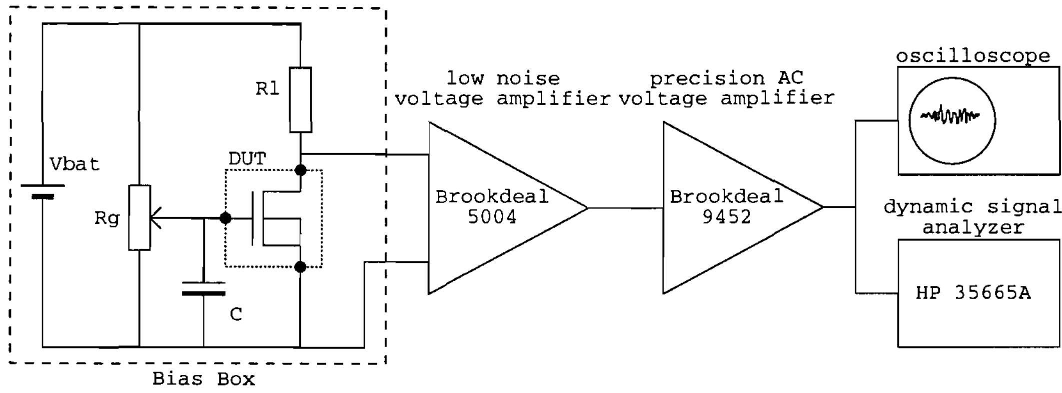


Figure 26: Drain-Source voltage noise measurement setup

- Oscilloscope to check the presence of any unwanted signals (for example 50 Hz crosstalk signals).

The Device Under Test (DUT) can either be a packaged MOSFET in a Dual In-Line (DIL) package, or it can be a MOSFET on a wafer. When performing measurements on wafer an extra probe-station is needed.

The bias-box can also be adjusted to perform current noise measurements. Instead of using a Brookdeal 5004, a Brookdeal 5002 low-noise current amplifier is being used. Also the selectable drain resistor is replaced by a potentiometer, which is decoupled for ac-signals, so that the true MOSFET current noise can be measured. This measurement setup is shown in figure 27.

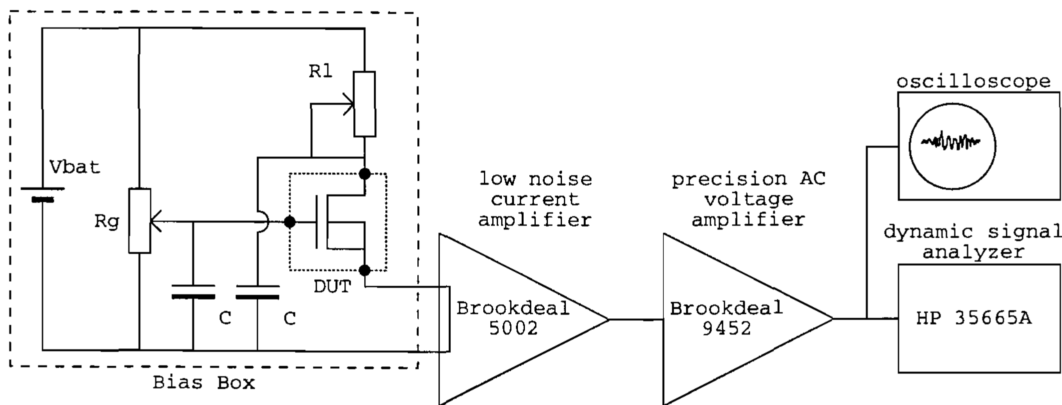


Figure 27: Drain current noise measurement setup

When performing a voltage noise measurement, the noise from the external drain resistor, which is parallel to the channel conductance, is also measured. By means of the noise model depicted in figure 28 this effect can be taken into account. In this model the following noise current sources have been used: I_{most}, representing all current noise from the MOSFET, and I_{Rl}, representing the thermal noise from resistor R_l. From this model the following expression can be derived:

$$S_v = (S_{i,most} + S_{irl})\ (R_l\ //\ R_{most})^2 \tag{45}$$

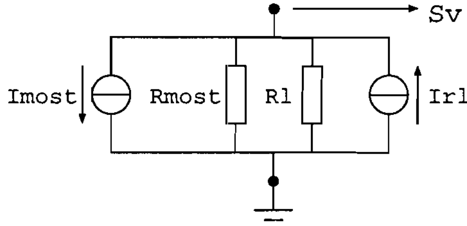


Figure 28: Noise model including the external drain resistor

Since S_{irl} only consists of Nyquist noise, which is much lower than the 1/f noise from the MOSFET, it will be neglected. The noise in the drain current can now be calculated:

$$S_{i,most} = \frac{S_v}{(R_l \; // \; R_{most})^2} \tag{46}$$

with R_{most} being the total MOSFET drain resistance (including the series resistances of the source and drain).

5.5 SPICE noise simulation circuit

In this section a short explanation of the SPICE simulation circuit, that is used to simulate the noise, will be given. A special bias and test circuit has been designed, to simulate the drain-source voltage noise of one single MOSFET, and to allow this voltage noise to be transformed directly into drain current noise.

When simulating the noise behavior in SPICE, a circuit is needed, which contains a small-signal voltage source, to which the noise will be related. This voltage source can be set to zero volt, because it is not needed as a source, but only as a reference point. To measure the noise at a certain bias condition (certain gate and drain voltage), without using external resistors, a special circuit is needed, because the drain voltage source can not be connected directly to the drain of the MOSFET. This would short-circuit the drain voltage noise to ground level. This special circuit consists of two identical MOSFETs: the first is biased at the given gate and drain voltage, and is used to measure the drain current, and the second MOSFET is biased with a current controlled current source, that will force the same bias condition on this MOSFET. The total circuit is shown in figure 29.

The voltage noise can now be obtained with the .NOISE statement, in combination with a .PRINT NOISE ONOISE statement. This voltage noise can be converted to current noise with the help of equation (46), with R_l infinite, and Rmost obtained from the SPICE operating point simulation. This simulation circuit can be used to simulate the noise in all operating regimes.

5.6 The influence of series resistance 1/f noise

In this section the influence of 1/f noise in the series resistances on the total MOST channel noise is examined. This is performed before the analysis of the noise measurements because it is useful to know whether the series resistances will play an important part in the total noise, or not. This possible noise source is not taken into account in the existing $\Delta N - \Delta\mu$ models. It is also important to know in which regime of operation the influence is the largest. In well

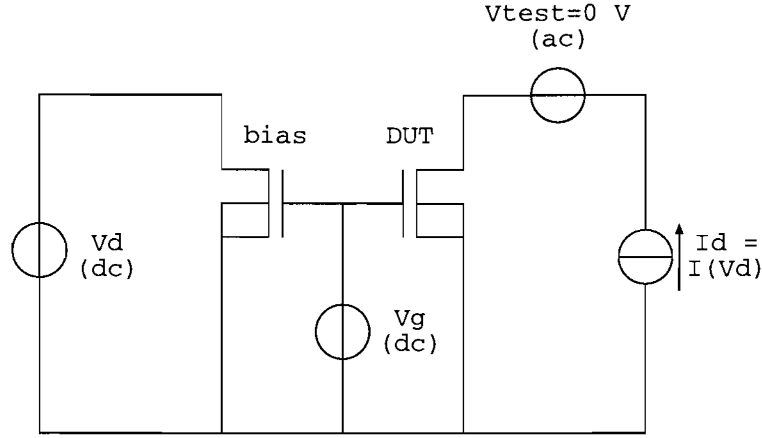


Figure 29: SPICE noise simulation circuit

processed MOSFETs, this noise is negligible, but to study the effect of this noise on the total MOSFET noise, it is assumed that the 1/f noise originating from the series resistances can exceed the 1/f noise originating from the channel.

Figure 30 shows the noise model that is used for the calculations [25]. The total MOSFET

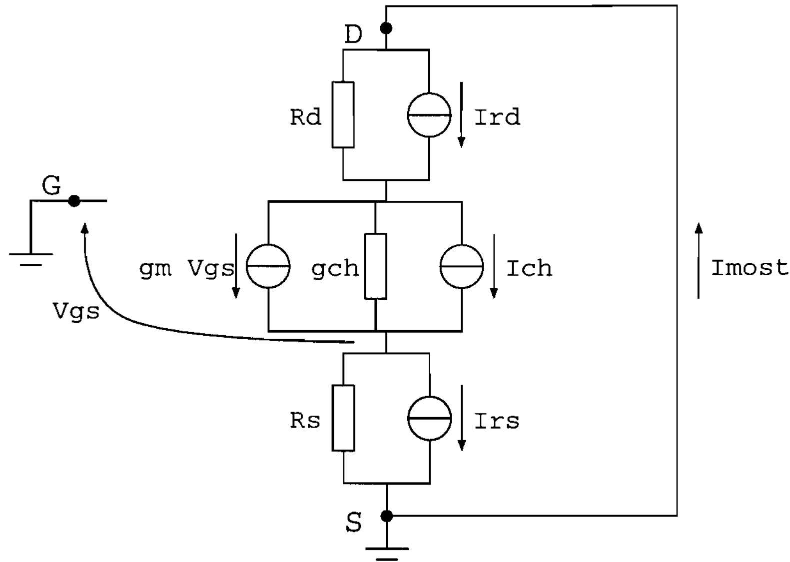


Figure 30: Equivalent circuit with noisy series resistances

current can be written as:

$$i_{most} = \frac{i_{ch} + g_m R_s i_{rs} + g_{ch}(i_{rd} R_d + i_{rs} R_s)}{1 + g_m R_s + g_{ch}(R_d + R_s)} \tag{47}$$

R_s and R_d are the internal source and drain resistances, g_m is the transconductance and g_{ch} is the channel conductance. i_{ch}, i_{rs} and i_{rd} are noise current sources. Rearranging this current gives:

$$i_{most} = \frac{i_{ch} + i_{rs}(g_m R_s + g_{ch} R_s) + i_{rd} g_{ch} R_d}{1 + g_m R_s + g_{ch}(R_d + R_s)} \tag{48}$$

Converting this current into the power spectral density gives:

$$S_{i_{most}} = \frac{S_{ich} + S_{irs}(g_m R_s + g_{ch} R_s)^2 + S_{ird}(g_{ch} R_d)^2}{(1 + g_m R_s + g_{ch}(R_d + R_s))^2} \tag{49}$$

This expression is different by the term $2S_{irs}g_m g_{ch} R_s^2$ from the one presented in [25]. This is due to overlooking the correlation term in the power spectral density expression.

The noise from the series resistances can be written as:

$$S_{irs} = S_{ird} = K\ I_{ds}^2 \tag{50}$$

The parameter K is a measure for the amplitude of the 1/f noise from the series resistances and is inversely proportional to the width of the channel. Note that the Nyquist noise is not taken into account. Using equation (11) and (12), the 1/f noise from the channel can be written as:

$$S_{i_{ch}} = \frac{\alpha_H}{f} \frac{q\mu I_{ds} V_{ds}}{L^2} \quad (Linear) \tag{51}$$

$$S_{i_{ch}} = \frac{\alpha_H}{f} \frac{q\mu I_{ds,sat} V_g^*}{L^2} \quad (Saturation) \tag{52}$$

In these expressions the internal drain-source and gate-source voltages are used. Those values can be calculated from the external voltages as follows:

$$V_{ds,int} = V_{ds,ext} - (R_s + R_d) I_{ds}$$

$$V_{g,int}^* = V_{gs,ext} - V_{th} - R_s I_{ds}$$

The simulation is done with data from the PL5004 wafer 3, at constant Vgs = 1.2 V, and variable Vds. The parameters used in the noise calculation have the following values:

Rs = 32 Ω

K = 1 10^{-8}

α_H = 1 10^{-5} at $V_g^* = 1V$

The parameters K and α_H are chosen so that the 1/f noise from the series resistances can exceed the 1/f noise from the channel.

In figure 31 the contributions of the channel noise, the series resistance noise and the total noise have been plotted separately.

The separate noise contributions in this figure are corrected for all influences of series resistances, so:

$$"S_{i,ch}" = \frac{S_{ich}}{(1 + g_m R_s + g_{ch}(R_d + R_s))^2}$$

$$"S_{i,rs}" = \frac{S_{irs}(g_m R_s + g_{ch} R_s)^2 + S_{ird}(g_{ch} R_d)^2}{(1 + g_m R_s + g_{ch}(R_d + R_s))^2}$$

From this figure it can be concluded that the influence of the 1/f noise in the series resistance is most dominant in the linear regime of the MOSFET. Also can be seen that the influence of the series resistance noise becomes less for longer channels.

When the 1/f noise from the series resistances is not dominant, these series resistances still have an influence on the measured channel noise. Figure 32 show the different influences of noiseless and noisy series resistances. It can be seen that noiseless series resistances reduce the

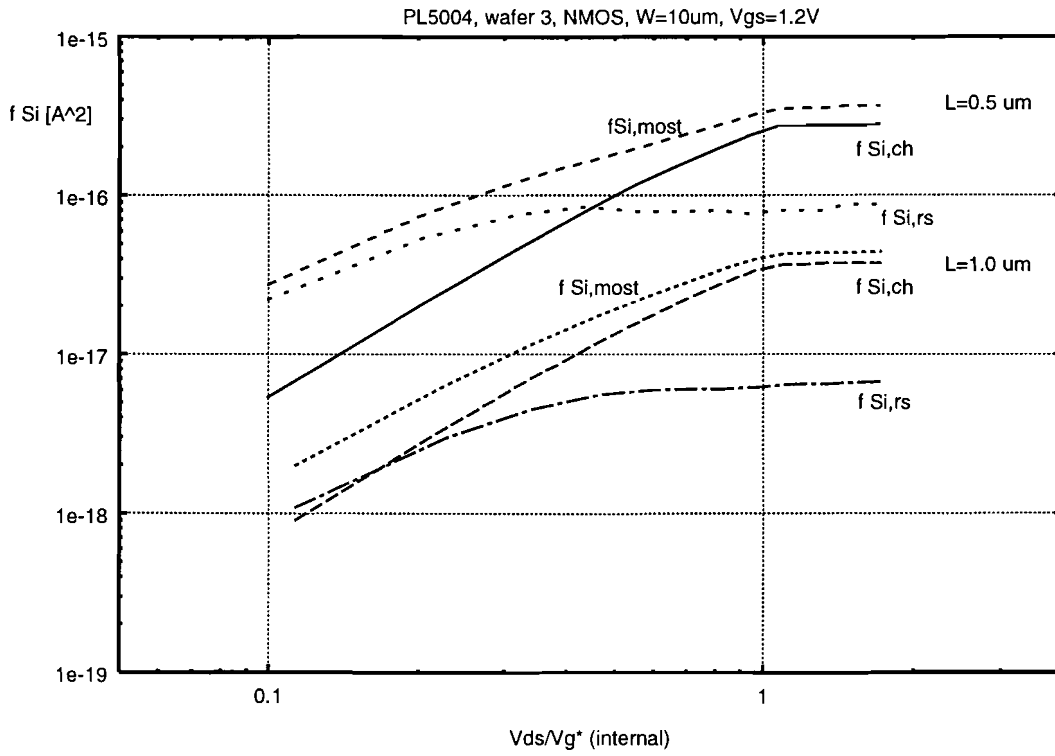


Figure 31: Calculated noise contributions from channel and series resistance

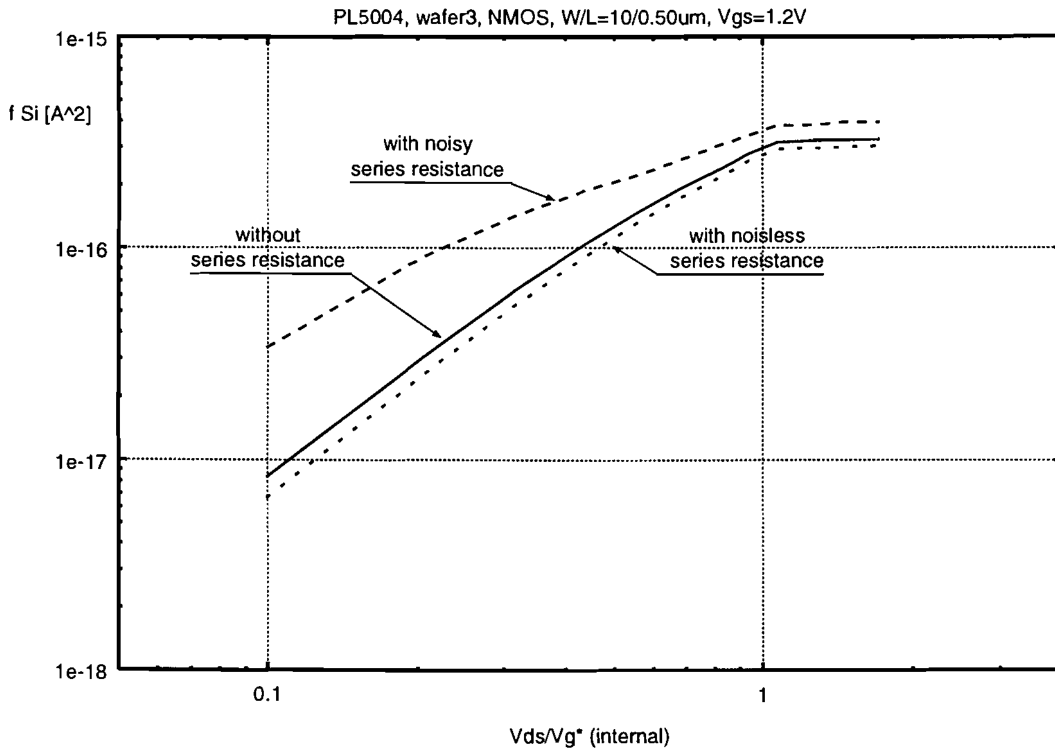


Figure 32: Influence of noisy and noiseless series resistance

total noise by a small amount, because these resistors only reduce the internal bias condition. As seen before, the resistors with 1/f noise will increase the total noise density, especially in the linear regime.

To show the influence of the 1/f series resistance noise in the linear regime, an experiment has been performed with simulation data from the PL7009 wafer 8, with Vds = -50 mV. The same parameters have been used as in the previous experiment, only this time the noise is assumed to originate from mobility fluctuations (because of the used pMOS devices). The results are shown in figure 33. In figure 34 the corresponding apparent α_H have been plotted. This value is calculated using the empirical relation (9), and contains the influences from the series resistance noise. These plots shows that the influence from the series resistance noise

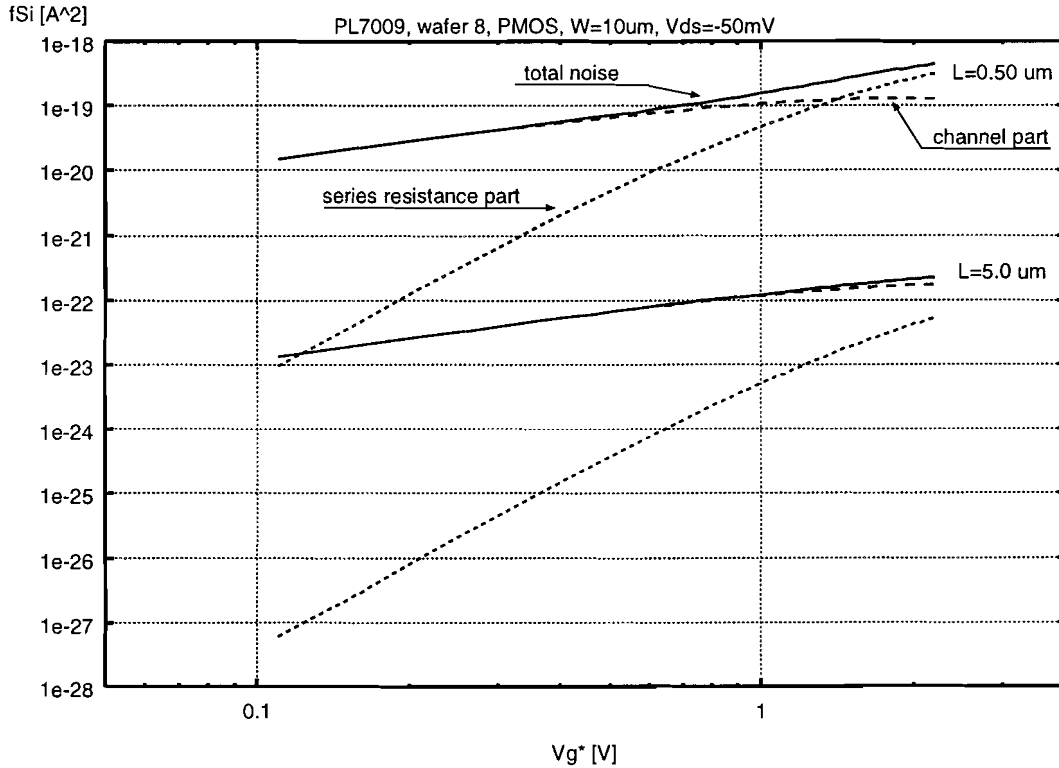


Figure 33: Influence of series resistance noise on linear current noise

can become dominant at higher gate voltages, and at short channel lengths. The influence of the 1/f noise from the series resistances on the linear drain current noise and the influence of correlated surface mobility fluctuations on this current noise show the same trend, for one particular channel length. The difference between these noise sources is the way in which they scale with the transistor dimensions. The influence of the 1/f noise from series resistances on the total absolute MOSFET noise, scales with approximately W/L^4. This can be seen from equation (49):

$$S_{i_{most}} \sim S_{irs}(g_{ch}R_s)^2 \sim KI_{ds}^2(g_{ch}R_s)^2 \sim \frac{1}{W}\frac{W^2}{L^2}\frac{W^2}{L^2}\frac{1}{W^2} \sim \frac{W}{L^4}$$

In the above approximation the term with g_{ch} has been used, but this approximation also holds when using the term with g_m. The influence from correlated surface mobility noise scales just like the normal channel noise: W/L^3.

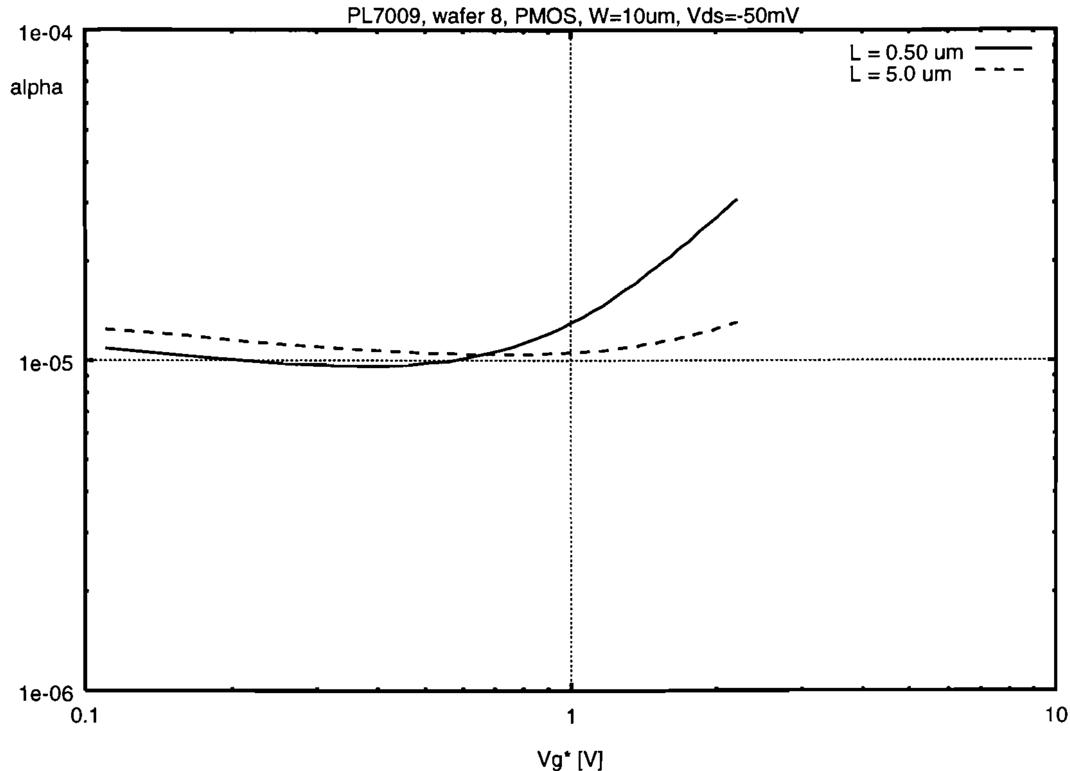


Figure 34: Influence of series resistance noise on apparent α_H

5.7 Noise measurements

The noise measurements have been performed on a number of wafers from all three technologies (PL5004, PL7009 and PL6042). At first the measurements were performed on packaged devices (from the PL5004), to make the measurements more easy to perform. But due to problems associated with the packaging later measurements were performed on wafer.

To check the scalability of the noise models, most measurements have been performed on L-arrays. Later on also some measurements have been done on transistors with different widths.

Because noise measurements are very time consuming, not all operating regimes on all wafers have been measured. The first measurements on the PL5004 n-MOSFETs were mainly intended to investigate the possible influence of the halo implant. This is done by measuring a few bias-point in the linear regime, and then calculate the Hooge-parameter α_H. Measurements on PL7009 p-MOSFETs, and especially on wafer 8, have been done in more detail, to investigate the validity of the different noise models. Finally some extra measurements have been performed on PL6042 p-MOSFETs to investigate the difference in noise between a poly-gate and an amorphous-gate.

5.7.1 PL5004, 0.50 μm NMOS devices

From the PL5004, wafer 3 and 7 have been used for noise measurements. Wafer 7 has the most extreme halo implant, and the influence on the DC behavior is the largest. Wafer 3 is the reference wafer. On both wafers L-arrays have been measured, with lengths varying from 0.50 μm to 10.0 μm. The width was always 10 μm.

The noise has been measured at several bias conditions in the linear regime (Vds = 50 mV). From the measurement results, the α_H values have been calculated using equation (51). At first, the 1/f noise contribution from the series resistances is assumed negligible, and only the noiseless series resistances have been taken into account. The results of the measurements have been plotted in figure 35. Included in this figure are measurements from devices with channel lengths 0.5, 1.0, 2.0, 5.0 and 10.0 μm. Also plotted in this figure is a theoretical alpha curve,

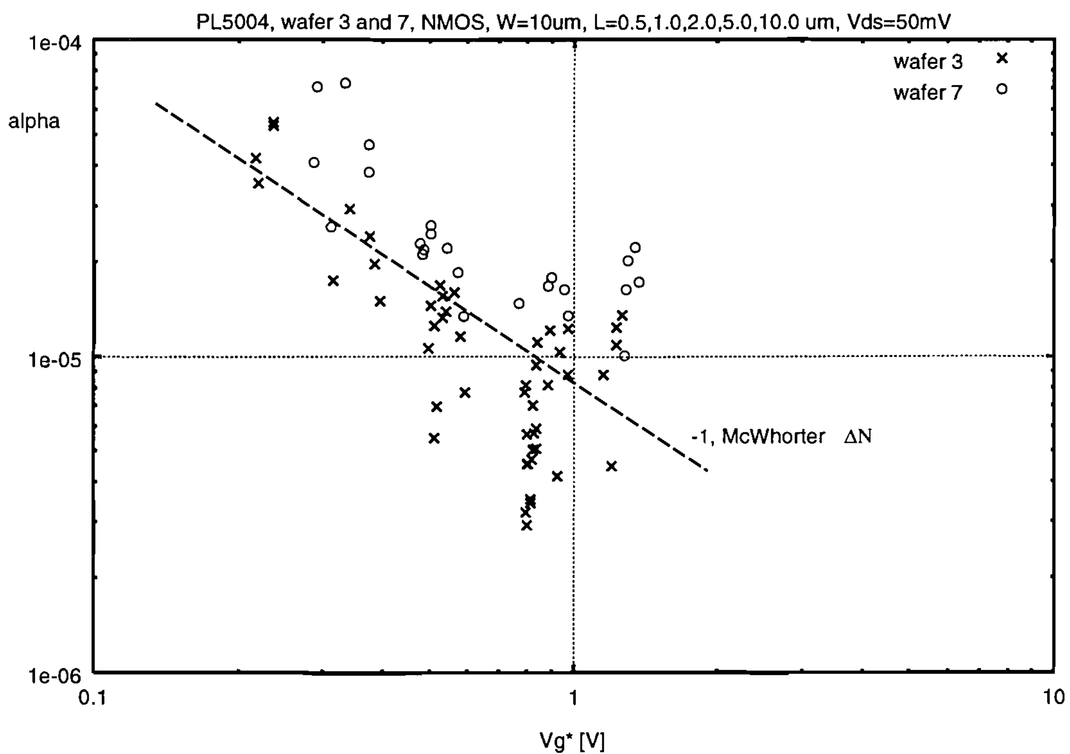


Figure 35: Alpha values versus gate overdrive voltage

when assuming that only the ΔN model is active. It can be seen that alpha is more or less inversely proportional to the gate overdrive voltage. Only at higher gate voltage do the alpha values show more divergence. The increase of alpha with respect to the theoretical curve, at higher gate voltage, could be explained by a noise contribution from the series resistance. This effect could also be explained by using a more complex noise model, with, for example, correlated surface mobility fluctuations. There are not enough measurement results to indicate which of these two effects is likely to cause this increase. Later measurements on other devices will show that the increase in noise can be modeled with more complex noise models, and that the noise contribution from the series resistance is not likely to be the cause of this effect.

What can be seen from the figure, is that the noise in the MOSFET with halo implant is about a factor 2 larger than the noise of the reference device.

5.7.2 PL7009, 0.25 μm PMOS devices

The noise measurements on the PL7009 have been concentrated on three wafers: 8, 11 and 23. Wafer 8 can be seen as a reference condition, with a normal poly gate and only a halo implant. This wafer is also the one with almost no threshold voltage roll-off (see figure 12). Wafer 11 has an amorphous gate and contains an LDD after spacer etch. Wafer 23 also has an amorphous gate, but is an HDD only device.

First, noise measurements have been performed in the linear regime (Vds = -50 mV), on devices with three lengths, 0.25 μm, 0.50 μm and 2.0 μm, to obtain the α_H values. The results of these measurements are shown in figure 36. This plot shows clearly that there is a

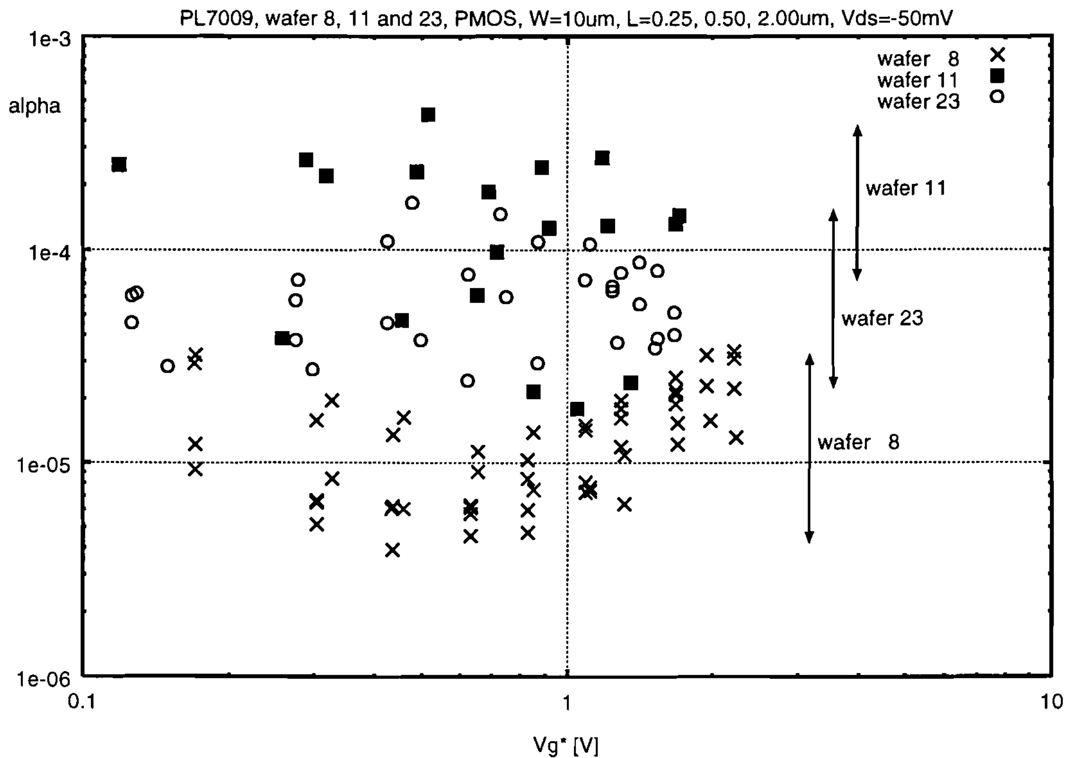


Figure 36: Alpha values versus gate overdrive voltage

big difference in alpha values from the different wafers. This difference is likely to be caused by the different concepts, used to produce these MOSFETs. But because these wafers differ not only in one concept, but contain many differences, it is hard to say which concept causes the most increase in noise. Probably, not only one novel concept will cause the increase, but rather a combination of different concepts. The one thing that wafer 11 and 23 have in common, is that they both have an amorphous gate, whereas wafer 8 has got a poly gate. To investigate if this difference could be the cause of the increase in noise level, extra measurements have been performed on the PL6042. In the next section this investigation will be described.

To check if any channel length dependence of α_H is present also a plot of the α_H values from wafer 8 is given, in which the different channel lengths are denoted separately. This plot can be seen in figure 37. It can be seen that, for all channel lengths, the apparent α_H values increase for higher gate voltage. There is still divergence in the experimental results, but this can not be attributed to a channel length influence on α_H. If the increasing α_H values would be caused by the influence of 1/f noise from series resistances, then a channel length dependence of this

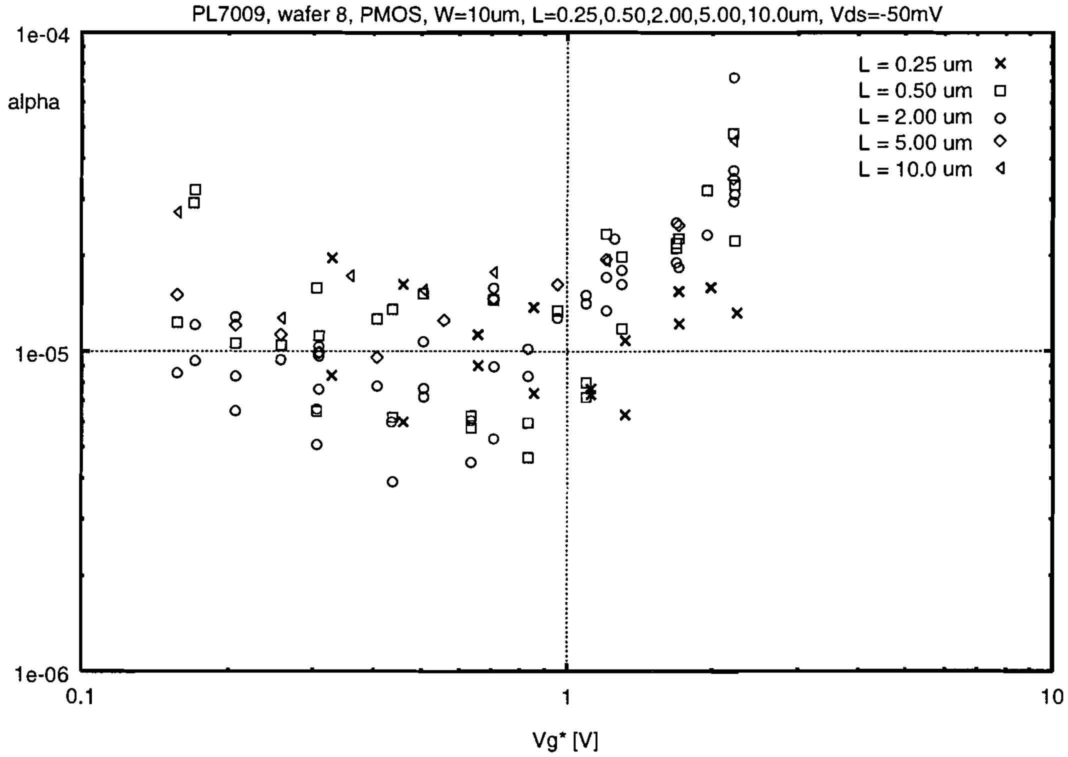


Figure 37: Alpha values versus gate overdrive voltage

increase should be visible. The increase could also be explained by using a $\Delta N - \Delta\mu$ noise model, as can be seen in figure 25. Then the increase would scale just like the noise from the channel, and no channel length influence would be visible. To check which noise model can best be used to simulate the noise behavior, extra noise measurements have been performed in the subthreshold and saturation regime. The noise parameters will be extracted for pMOS devices from PL7009 wafer 8 and the noise will be simulated with the different noise models.

First, the noise is again measured in the linear regime, to check the scaling of the noise with the geometry, and to see if an influence from the series resistances can be noticed. Theory states that the normal drain current noise should scale with W/L^3, and from equation (49) follows that the influence from the series resistance 1/f noise should scale approximately with W/L^4, so the influence must be larger for shorter channel lengths. Figure 38 shows the drain current noise in the linear regime for four channel lengths and the theoretical W/L^3 scaling. It can be seen that the measured noise scales just like the theoretical W/L^3 scaling lines, so it is likely that the noise really stems from the channel of the transistor. In this plot no influence from series resistance noise can be noted. In the next part of this section the parameter extraction will be performed, in order to simulate the noise with the different noise expressions and models. It will be assumed that all the noise stems from the channel of the device.

The noise parameter extraction starts with noise measurements in the subthreshold region (Vds = -1.5 V). The results from these measurements can be used to obtain a value for the trap density N_t. With this value, and with an appropriate value for α_S, the noise expressions of Ghibaudo and BSIM3v3 can be used to model the noise in all operating regimes.

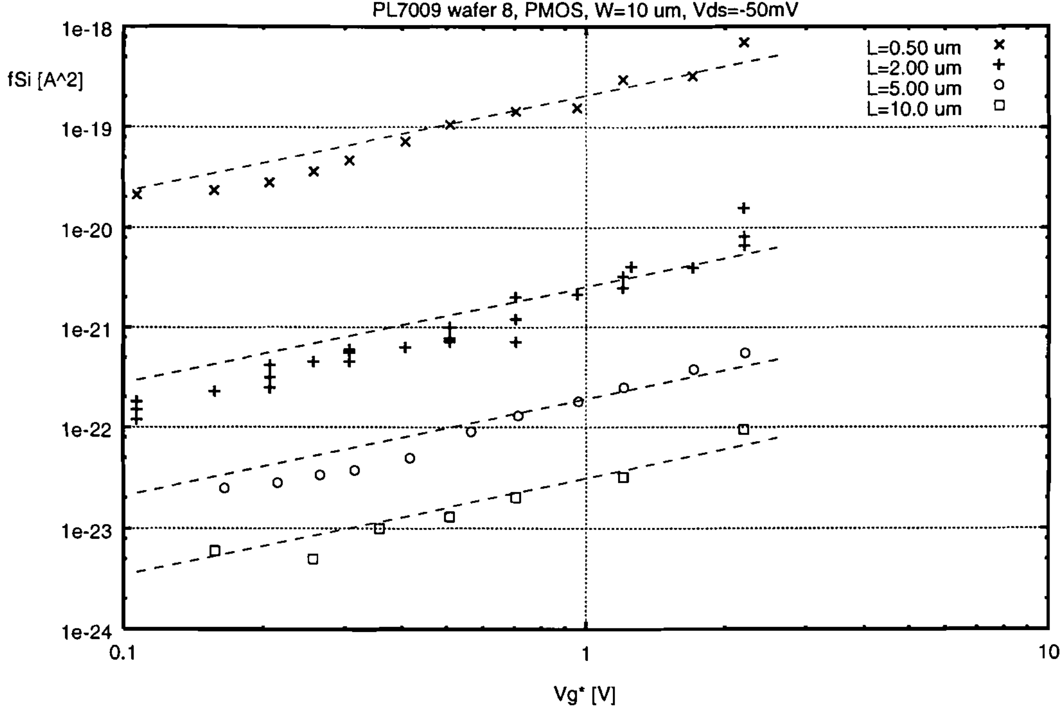


Figure 38: Linear drain current noise and true W/L^3 scaling

The measured plateau values are:

Width [μm]	Length [μm]	Plateau level (fSi/i^2)
10	0.50	$8\ 10^{-9}$
10	2.0	$2\ 10^{-9}$
10	5.0	$8\ 10^{-10}$

Although this is a 0.25 μm technology, the smallest measured device is a device with channel length 0.50 μm. This is because the subthreshold noise measurements of the 0.25 μm device were dominated by RTS noise, and determination of the 1/f noise component was not possible.

Since the measured plateau levels scale with 1/(WL), as theory predicts, it is most likely that these levels really stem from noise in the transistor, and are not caused by some other parasitic effect (like restrictions of the measurement setup). The trap density can be calculated by using equation (23) and (24). Parameters used in this calculation are:

$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = 6.9\ 10^{-3}\ F/m^2$

and obtained from SPICE simulations:

$\frac{I_d}{g_m} = 0.03\ V \quad \Rightarrow \quad C_{ox} + C_d + C_{it} = 8.19\ 10^{-3} F/m^2$

This leads to the following trap density and BSIM3v3 noise parameter:

$N_t = 1.7\ 10^{41}\ CV^{-1}m^{-3}\ =\ 2.7\ 10^{16}\ eV^{-1}cm^{-3} \quad \Rightarrow \quad NOIA = 2.7\ 10^{20}$

To obtain the value for the surface scattering α_S, the measurements from the linear regime have been used. With the help of SPICE noise simulations, and by changing the NOIB parameter by hand (NOIC is calculated from NOIA and NOIB), the best fit has been searched for.

The following values have been obtained:

$NOIA = 2.7\ 10^{20}$, $NOIB = 2.5\ 10^{4}$, $NOIC = 5.8\ 10^{-13}$

With these three parameters the noise can be simulated with the BSIM3v3 noise model, by using a standard SPICE simulator. From these values the noise parameter α_S can be calculated, and N_t was already known:

$\alpha_S = 5.7\ 10^{-15}\ Vs$ and $N_t = 1.7\ 10^{41}\ CV^{-1}m^{-3}$

With these two parameters the noise expression from Ghibaudo et al. can be used to calculate the noise.

In order to compare these two modelings with the mobility fluctuations model, also an α_H value is extracted from the measurements:

$\alpha_H = 1\ 10^{-5}$

Now the empirical relation from Hooge can be used to calculate the noise.

Figure 39 shows the result from the noise simulation in the linear regime. The circles represent

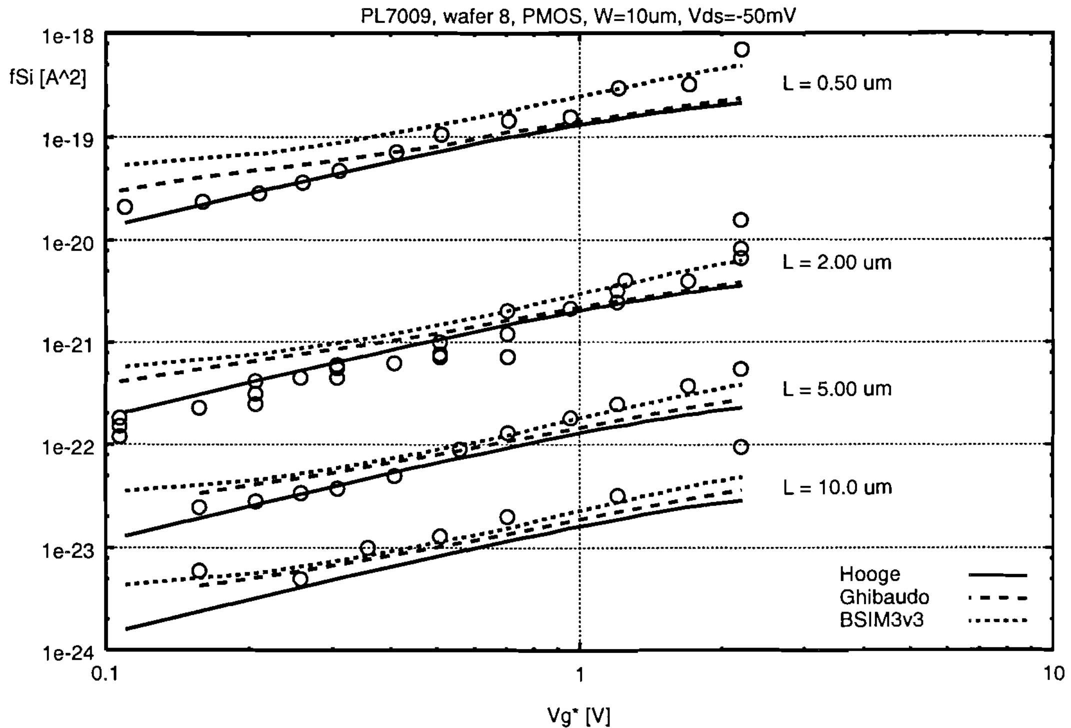


Figure 39: Measured and simulated drain current noise

the measured noise, the solid line the calculated noise from Hooge's empirical relation (9), the dashed line the calculated noise from expression (21) and the dotted line the noise simulation from SPICE. It can be seen that all models result in a good simulation of the noise in the linear regime. There are small deviations, but in noise measurement accuracies, these are not significant.

Figure 40 shows noise measurements and simulations in the saturation regime. Also in this figure have the noise expressions from Hooge, Ghibaudo and BSIM3v3 been used. Again all models result in a good noise simulation, although the divergence between the models is

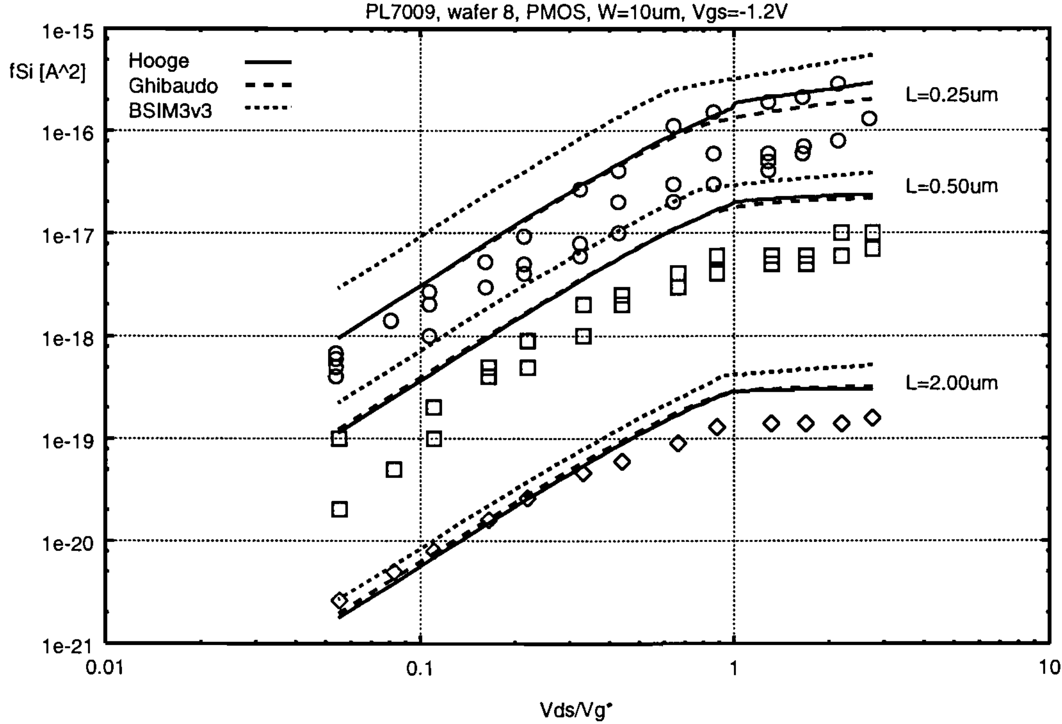


Figure 40: Measured and simulated drain current noise

somewhat larger. Especially the noise simulation from the BSIM3v3 model deviates from the other 2 simulations. To obtain the SPICE simulated noise curve without any discontinuities, the SPICE parameter EM has been changed. This parameter, which represents the saturation electric field, is embedded in the expression for ΔL_{clm}, and can be used to change the level of the plateau, observed in the saturation regime. The default value is 4.1 $10^7 V/m$, but with this value the simulated noise curve shows a discontinuity, when switching from the linear to the saturation regime. The new parameter value is 2.5 $10^7 V/m$.

The noise simulations of the current noise in the saturation regime show that the modeling in this regime is less accurate than in the subthreshold and linear regime. This is mainly because of the fact that the two noise parameters have been extracted from measurements in the subthreshold and linear regime, and are not specifically optimized for the saturation regime.

Figure 41 shows noise measurements and simulations in the subthreshold regime. In this plot only the noise calculations with the expression from Ghibaudo et al. and the empirical relation from Hooge are given. The subthreshold BSIM3v3 noise simulation will be described later. As Hooge's empirical relation is not valid in the subthreshold region, the noise calculation has only be performed for the non-subthreshold region, in this case the saturation region. In this saturation region the noise simulation shows good agreement with the experimental data. The noise calculation with the expression presented by Ghibaudo et al. shows very good agreement with the measured noise, for all bias conditions.

Figure 42 shows the relative measured and BSIM3v3 simulated current noise in the subthreshold region, for one device with W/L = 10/0.50 μm and Vds = -1.5 V. It is clear to see that the SPICE simulation is inaccurate, when simulating noise in the subthreshold region. The cause of this error has been mentioned before: the parameter N^* has a fixed value of 2.0 10^{14} m^{-2}

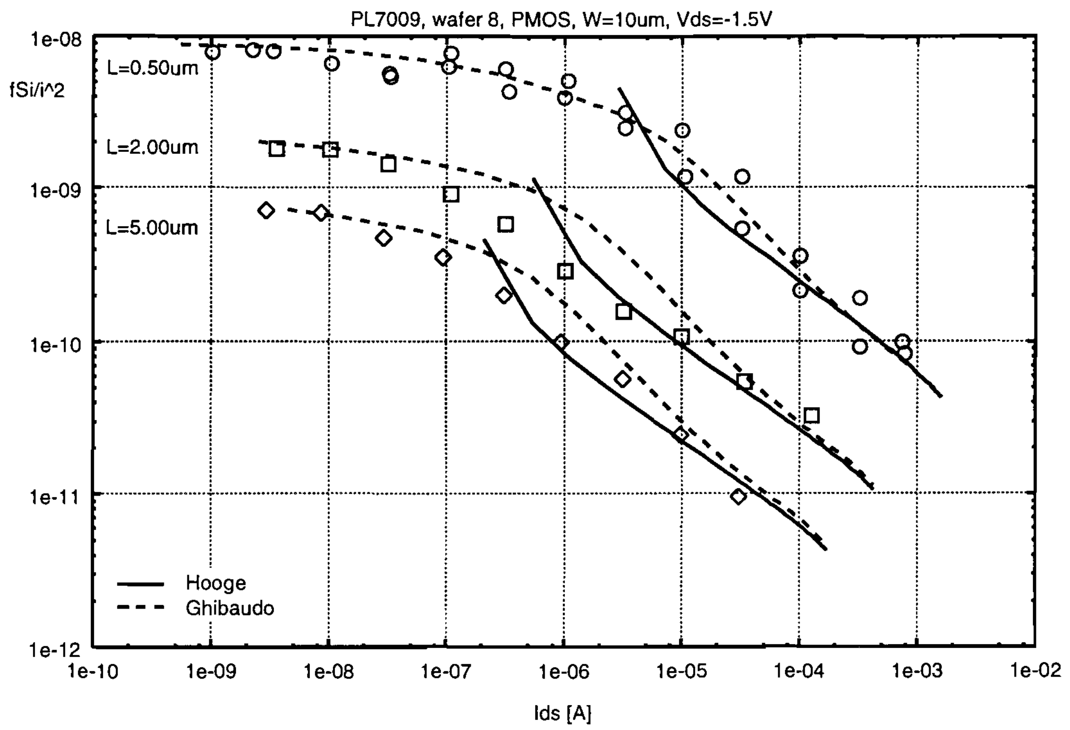


Figure 41: Measured and simulated drain current noise

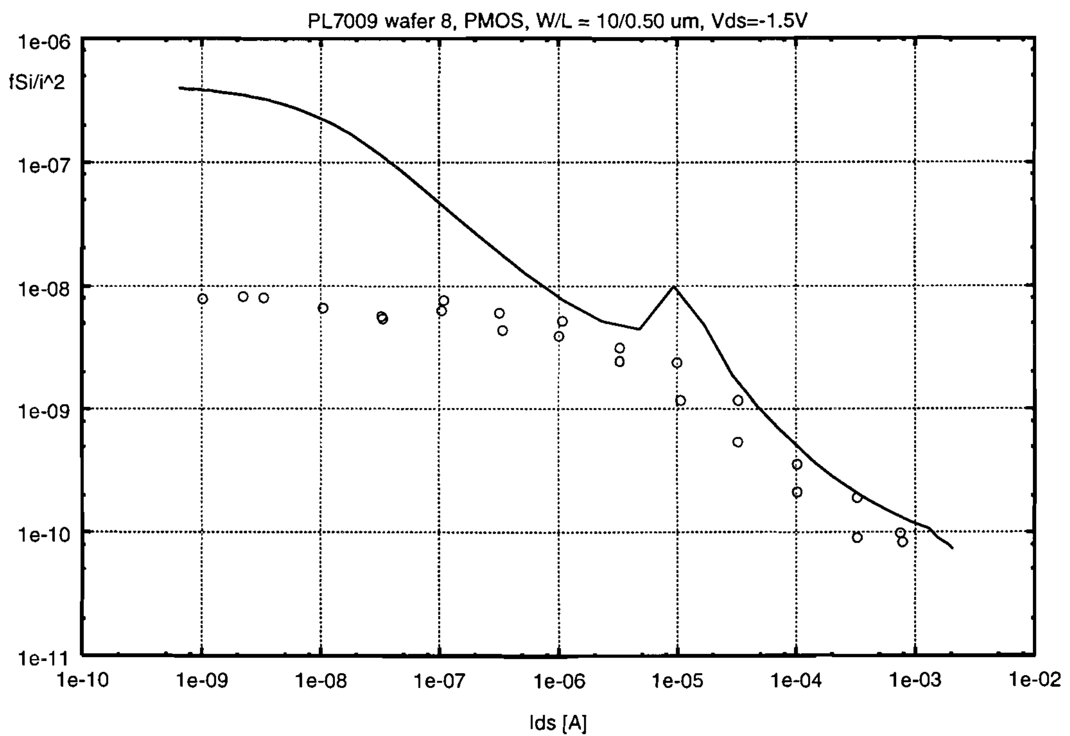


Figure 42: Measured and BSIM3v3 simulated relative drain current noise

in the SPICE implementation of the BSIM3v3 noise model. For the measured devices this should be (equation (29)) 1.3 10^{15} m^{-2}. Since this parameter is squared in the expression for the plateau value, this leads to a calculated difference of a factor 42. This factor is the same as the difference between the measured and simulated noise plateau level, so this error of SPICE is accounted for. Due to the fixed value of N^* the SPICE BSIM3v3 noise simulations are only valid for MOSFET technologies with an gate-oxide thickness of about 30nm. Also a discontinuity is present in the noise simulation at the transition from the subthreshold region to the saturation regime. This is because the BSIM3v3 noise model is not a continuous model for all operating regimes, but uses instead three separate noise expressions (for subthreshold, linear and saturation). Probably the switching between the different noise expressions is not implemented very well.

5.7.3 PL6042, 0.35 μm PMOS devices

The noise measurements on the PL6042 have been performed on two wafers: wafer 3, with an amorphous gate and wafer 8, with a poly gate. Apart from the gate material these wafers received the same processing. These measurements have been performed to study the influence of the gate material on the noise behavior. First, measurements have been performed in the linear regime, on transistors with width 7 μm and lengths 0.5 μm, 1.0 μm and 2.0 μm. From the measured current noise in the linear regime, the α_H values have been calculated. The results are shown in figure 43. This figure shows that α_H for an amorphous gate can be up to

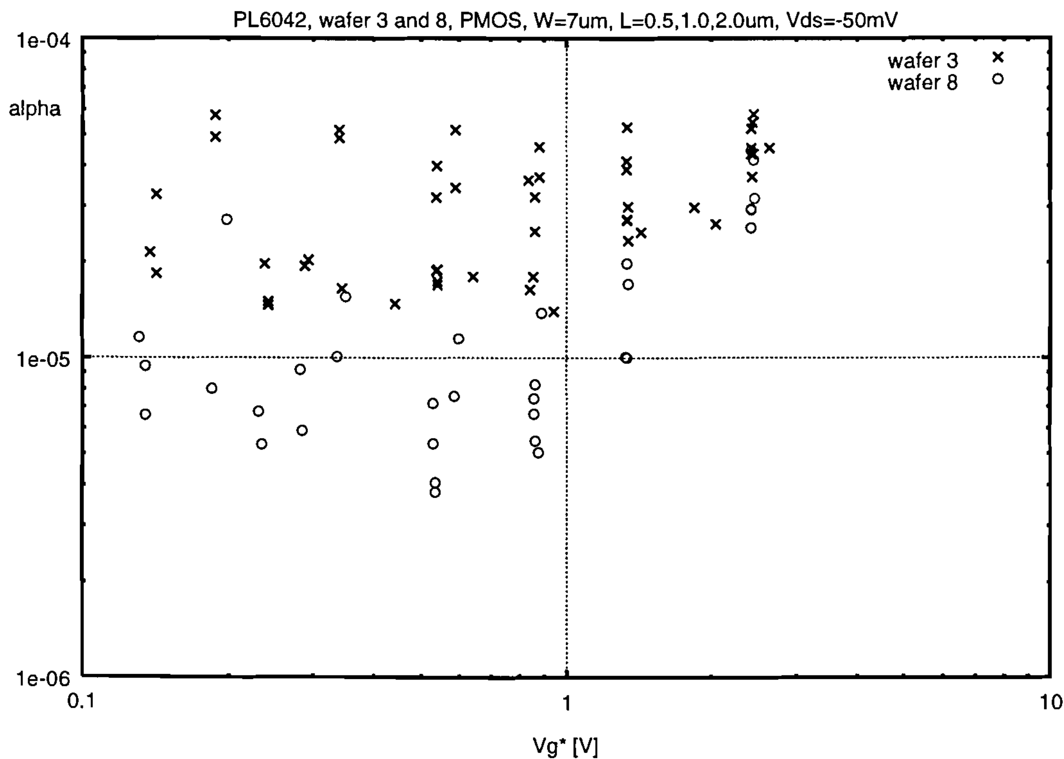


Figure 43: Alpha versus gate overdrive voltage

a factor 5 higher than for a poly gate, depending on the bias condition. At lower gate voltages the difference is larger than at higher gate voltages.

In order to relate this increase in noise for an amorphous gate to the parameters N_t and α_S, the noise has been modeled with SPICE. First subthreshold noise measurements have been performed, to obtain the value of N_t. Measurements on a device with width 7 μm and length 0.5 μm produced for both wafer 3 and wafer 8 a relative current noise plateau level of approximately 1 10^{-8}. This leads to the following trap densities:

$$\text{Wafer 3}: N_t = 2.7\ 10^{16}\ eV^{-1}cm^{-3}$$

$$\text{Wafer 8}: N_t = 2.0\ 10^{16}\ eV^{-1}cm^{-3}$$

The difference in N_t values is not due to a different plateau value but due to a difference in C_d+C_{it} values, obtained with expression (23) and SPICE simulations. Since these measurements produced not very accurate results, extra measurements have been performed to obtain more information about the difference in N_t for the two wafers. This information can be obtained by means of a charge pumping measurement [26]. This measurement can give an accurate value for the interface state density (D_{it}), expressed in numbers per unit area. Figure 44 shows the measured charge pumping characteristics for wafer 3 and 8. The (absolute) maximum of the

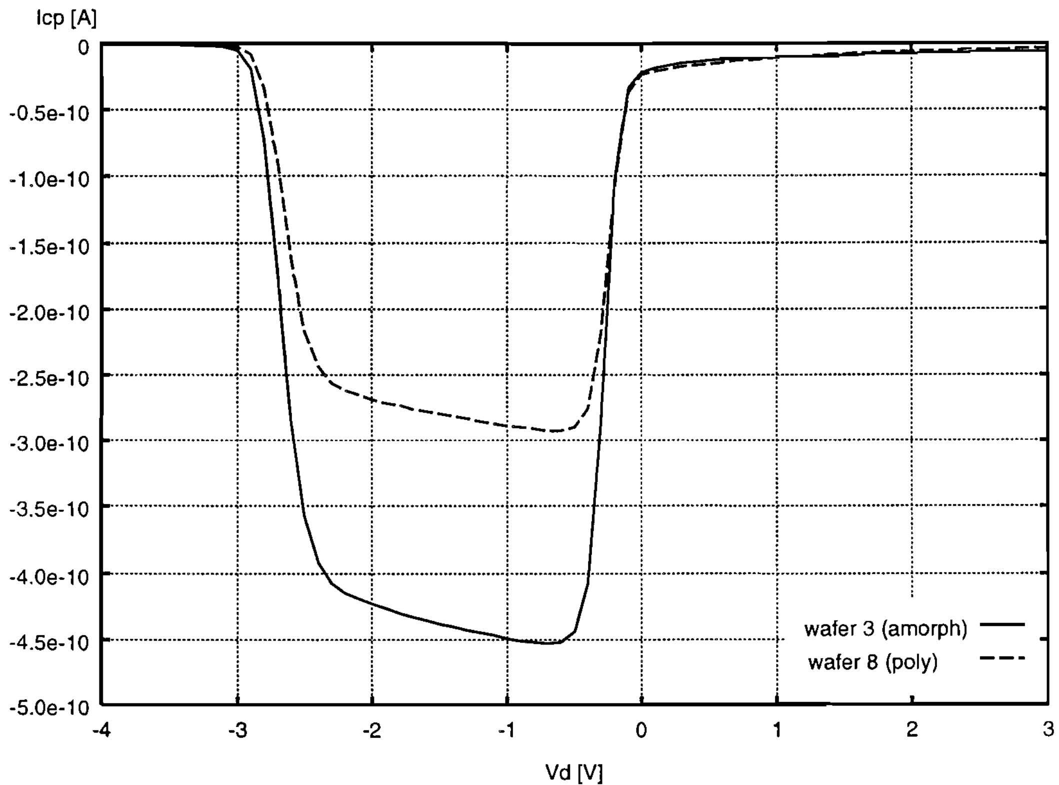


Figure 44: Charge pumping measurement results

charge pumping current is a measure for the interface state density. It can already be seen that the interface state density for wafer 3 is larger than for wafer 8. The calculation method, used for obtaining the values for D_{it}, can be found in [26]. The N_t value, used in the noise models, is expressed in numbers per unit volume, while D_{it} is expressed in numbers per unit area. The parameter that can be used to relate these two values is the oxide thickness (t_{ox}), although this will not result in an quantitative accurate value. More important than the exact value is the measured difference in the interface state density, between wafer 3 and 8. The charge pumping measurement resulted in the following values (with $t_{ox} = 7nm$):

Wafer 3 : $D_{it} = 1.6\ 10^{10}\ \#/cm^2 \Rightarrow N_t = 2.3\ 10^{16}\ eV^{-1}cm^{-3}\ (NOIA = 2.3\ 10^{20})$

Wafer 8 : $D_{it} = 1.1\ 10^{10}\ \#/cm^2 \Rightarrow N_t = 1.5\ 10^{16}\ eV^{-1}cm^{-3}\ (NOIA = 1.5\ 10^{20})$

So N_t for an amorphous gate is about 50 percent larger than for a poly gate. The trap densities obtained from the charge pumping measurement are close to the values obtained from the subthreshold noise measurements. The NOIA values are only added as an indication for likely values, and do not have to be the best parameter values for the SPICE noise simulation. The difference of 50 percent however will be maintained.

Starting with the calculated NOIA values, SPICE noise simulations have been performed, and good values for the two parameters NOIA and NOIB have been found. The third parameter, NOIC, is again calculated out of NOIA and NOIB. The resulting parameters are:

Wafer 3 : $NOIA = 2.0\ 10^{20}$, $NOIB = 3.0\ 10^4$, $NOIC = 1.1\ 10^{-12}$

Wafer 8 : $NOIA = 1.3\ 10^{20}$, $NOIB = 1.8\ 10^4$, $NOIC = 6.2\ 10^{-13}$

The measured subthreshold noise and calculated noise with the equation (21) presented by Ghibaudo et al. are shown in figure 45 and 46. The measured noise in the linear regime, together with the simulated noise from SPICE can be seen in the figures 47 and 48. In these last two figures also the calculated noise has been plotted when using the mobility fluctuations model, with $\alpha_H = 3\ 10^{-5}$ for wafer 3 and $\alpha_H = 1\ 10^{-5}$ for wafer 8. It can be seen that the $\Delta\mu$ model sometimes gives better simulation results than the SPICE noise model. At higher gate voltages the SPICE noise model is often better capable of simulating the noise correctly.

The SPICE noise parameters correspond with the following N_t and α_S values:

Wafer 3 : $N_t = 2.0\ 10^{16}\ eV^{-1}cm^{-3}$ and $\alpha_S = 9.4\ 10^{-15}\ Vs$

Wafer 8 : $N_t = 1.3\ 10^{16}\ eV^{-1}cm^{-3}$ and $\alpha_S = 8.7\ 10^{-15}\ Vs$

From these measurements and simulations can be concluded that, for an amorphous gate, the trap density is about 50 percent higher, than for a poly gate, and that also the surface scattering is somewhat larger.

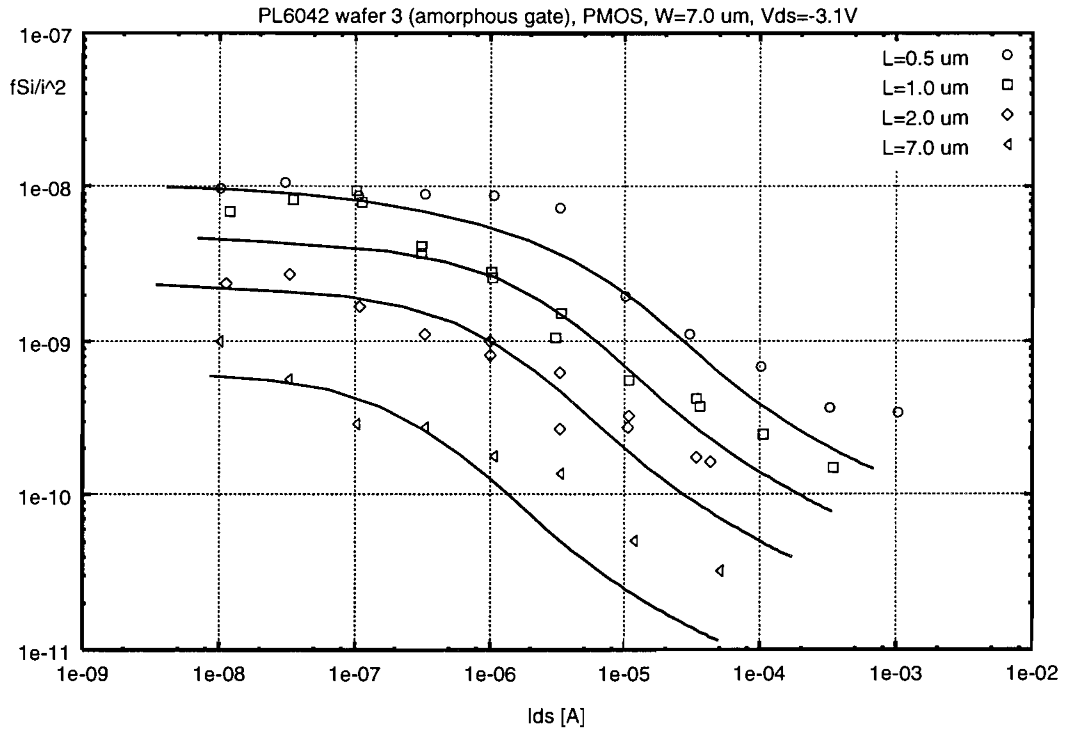


Figure 45: Measured and Ghibaudo calculated subthreshold drain current noise

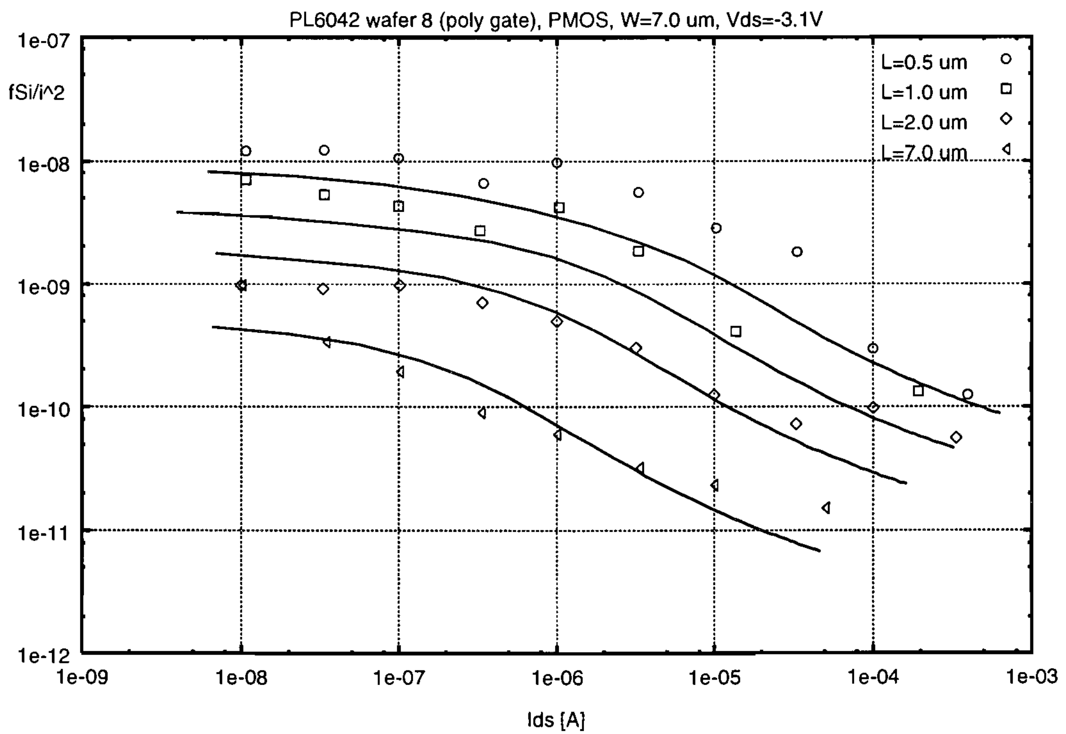


Figure 46: Measured and Ghibaudo calculated subthreshold drain current noise

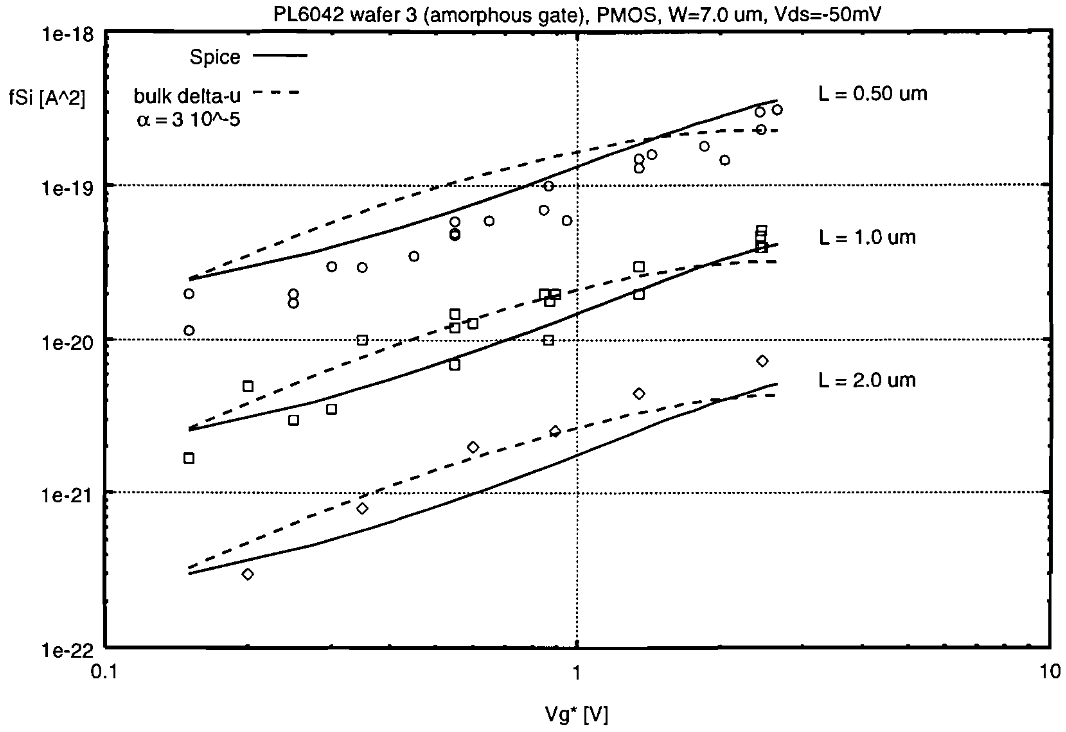


Figure 47: Measured and SPICE simulated linear drain current noise

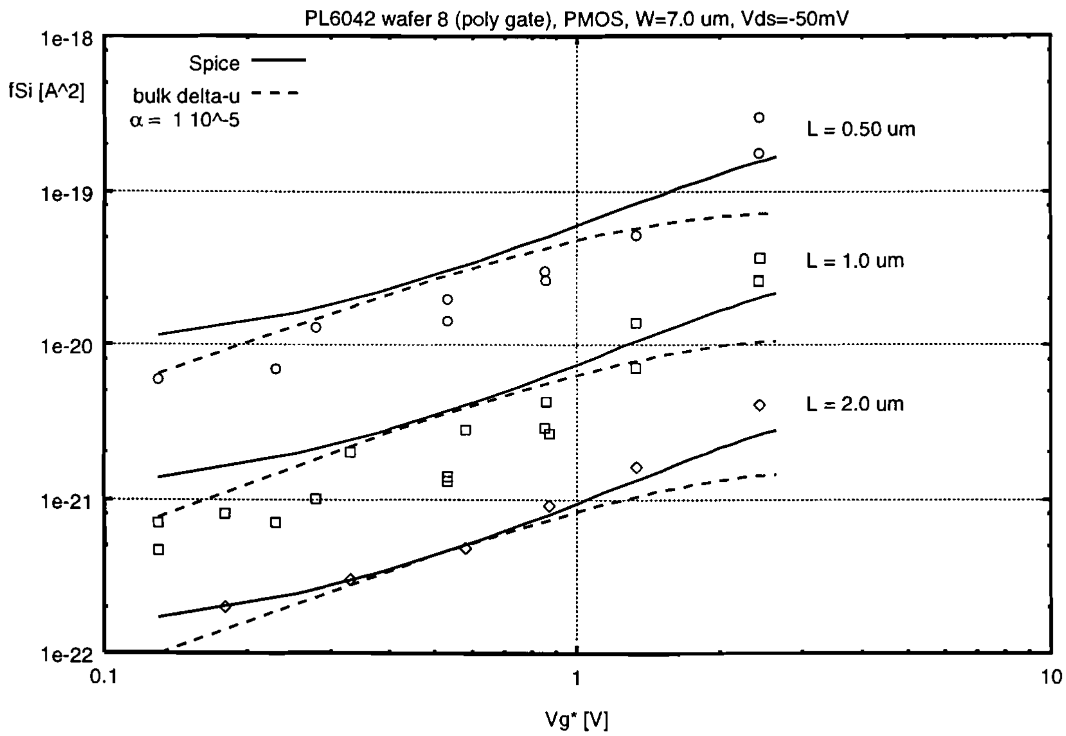


Figure 48: Measured and SPICE simulated linear drain current noise

5.8 Conclusions concerning noise analysis

The noise models assuming number fluctuations and correlated surface mobility fluctuations, have proven to be capable of modeling the observed noise very well, in all operating regimes. The model presented by Reimbold, based on only number fluctuations, does only model the subthreshold behavior well for the measured pMOS devices. Actually all these models result in the same noise expression for the subthreshold region, which makes it likely that in this region the noise, caused by number fluctuations, is dominant.

The $\Delta\mu$ and ΔN model are incapable of modeling the noise in the subthreshold region, and can also not model the deviations of α_H from the theoretical curves. Still the $\Delta\mu$ model results in good simulations in the linear and saturation regime. Also the usage of models, which include 1/f noise in the series resistances, can not explain the observed noise behavior. Although these two models can not explain all measured noise curves, the parameter α_H can still be used to indicate the overall quality of the MOSFET with respect to the noise behavior. Also, the plot of the apparent α_H versus the gate overdrive voltage, can show deviations from the straightforward $\Delta\mu$ and ΔN models, which indicates that a more complex noise model is needed.

The noise measurements on the PL5004 have shown that the use of a halo implant does not increase the noise very much. Only a slight increase was observed, which was not large enough to use a special halo noise model, to model the observed noise.

The noise measurements on the PL7009 have shown that other novel MOSFET concepts can increase the noise very much, easily by a factor 10. The observed noise on wafer 8 was successfully modeled with the $\Delta N - \Delta\mu$ models. Because the three measured wafers from the PL7009 did not differ in only one concept, it is hard to say which novel concept is responsible for the increase in noise. To investigate one difference, namely the gate material, additional noise measurements have been performed on the PL6042. These measurements have shown that the use of an amorphous gate material increases the noise by a factor 5, but this effect alone can not be responsible for the observed difference in noise on the wafers from PL7009. Probably other concepts, or the combination of several concepts, will also cause extra noise.

It has also been shown that the SPICE BSIM3v3 noise simulation can give inaccurate simulation results in the subthreshold region. This is due to the fact that a technology depended parameter has been assumed constant in the SPICE noise model, which limits the applicability of this model to only certain CMOS technologies, or oxide thicknesses.

6 Conclusions

Most detailed conclusions, concerning the DC characterization, noise modeling and noise analysis, have already been presented in sections 4.5, 5.3.6 and 5.8. In this section only the general conclusions will be given:

Conclusions concerning the DC characterization:

- Some novel concepts give very good results, with respect to the DC behavior of the MOSFET. The p-MOSFETs from PL7009 wafer 8, for example, which have been given a halo implantation, have almost no threshold voltage roll-off. This proves that, when several concepts with the right processing properties are combined, it is possible to produce small (0.25 μm) MOSFETS, operating at a low supply voltage (1.2 V).
- The BSIM3v3 model is capable of modeling MOSFETs that have been produced using the presented novel MOSFET concepts, even if these concepts are not explicitly included in the BSIM3v3 model.
- The BSIM3v3 parameter extraction performed with the extraction and optimization routines from the ICCAP software program, can best be performed per parameter, instead of first extracting all parameter automatically, and then optimizing them. In this way non physical parameter values can be avoided.
- The modeling of the halo MOSFETs by means of a three-transistor model gives good results, however the parameter extraction for the special halo transistors must be performed manually, which is a time consuming procedure.

Conclusions concerning the noise analysis:

- The use of novel MOSFET concepts can lead to a large increase in noise. One new concept, the use of amorphous gate material instead of poly, resulted in an increase of α_H by a factor 5.
- The modeling approach used by Reimbold, Ghibaudo and BSIM3v3 all result in the same noise expression for the subthreshold region. All measured subthreshold noise showed a plateau value, that can be modeled very well with this expression. Noise measurements in the subthreshold regions have shown to be very important in the noise parameter extraction, because in this region the dominant noise is directly related to the trap density. In the other operating regions, the noise expression presented by Ghibaudo and BSIM3v3 produced very good noise simulations. Both models are based on the same noise mechanisms, namely number fluctuations in combination with correlated surface mobility fluctuations.
- A simple noise parameter extraction method has been presented, that results in very good noise simulations. Only a few noise curves in the subthreshold region, and the linear region are needed. It was also shown that with the use of only two parameters, the noise can be modeled very well, in all operating regimes.

7 Future work

Because this work was not concentrated on finding the physical cause of the noise, but more on modeling the noise, it is hard to say if the presented unified noise models correspond with physical reality. Although it must be said that the measured noise from several wafers could be modeled very well with these models, but this can also be said of the ΔN and $\Delta\mu$ model. In this work only measurements of a few technologies have been presented. Also the unified models have only been used to model p-MOSFETs. More noise measurements on other MOSFET technologies are needed to check if these models correspond with physical reality.

Because the large difference in noise behavior of several processing concepts could not be totally accounted for, more measurements are needed. To check the influence of other novel concepts on the noise behavior, measurements are needed on splits, which only differ in one processing concept.

It will always be necessary to measure several device geometries (different lengths and widths) of the same wafer. But due to the smaller device sizes the influence of RTS noise becomes more dominant, and can even make the determination of the 1/f noise component impossible. But, on the other hand, it may be possible to use the relative amplitude of the RTS noise to give information about the quality of the device.

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