Designing an 8 bit, 100 MHz, low power, folding analog to digital convertor

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"DESIGNING AN 8 BIT, 100 MHz, LOW POWER, FOLDING ANALOG TO DIGITAL CONVERTOR"

by
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Eindhoven, August 1997

Report of graduation work,
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Dr. Ir. D.M.W. Leenaerts
Ir. G.G. Persoon

PREFACE

This report has been written in the context of my graduation at the Eindhoven University of Technology (TUE). This project has taken place at the TUE and at Philips Research Laboratories in Eindhoven. I especially want to thank Prof. dr. ir. R.J. van de Plassche for giving me the opportunity to graduate under his supervision. I also would like to thank ir. G.G. Persoon and dr. ir. D.M.W. Leenaerts for their useful comments. At Philips Research I want to thank ir. A.G.W. Venes and ir. T. Wagemans for their support. Finally, I would like to thank everybody who has supported me during my graduation report.

Eindhoven, August 1997
Roland van Wegberg

ABSTRACT

Todays consumer electronic products, like for instance mobile phones, usually require the use of high speed data convertors. Subsequently, the use of low power convertors in such products which can be supplied by battery becomes increasingly important. The Analog to Digital Convertor (ADC) discussed in this research report is considered to be an example of such a product. In order to meet the demand for low power, this ADC has been implemented in an advanced bipolar IC-process in which no substrate is used. The former leads to very low parasitic capacitances around the transistors, providing the ideal circumstances for designing low power circuits.

In this research, the design as well as the lay-out of the ADC have been realized. In order to make implementation of the ADC in a digital signal processing system mentioned above, possible, the corresponding static and dynamic specifications which an ADC needs to meet have been analysed and discussed in this research report.

Furthermore, attention has been payed to the architecture of the ADC which has been based on the folding and interpolation technique. Applying this technique has resulted in using less comparators since they are used in a more efficient way compared to for instance a full-flash convertor. Hence, fewer comparators use less power consumption and take in less chip area. The folding and interpolation technique used in this ADC has been discussed in this research report, including the demands for a correct functioning of the ADC. The interpolation has been performed by using a interpolating resistance ladder, presenting the interconnection between the analog preprocessing part and the digital part of the ADC. By using charge control the resistor value has been determined, resulting in an optimum between clock feedthrough noise at the output of the interpolation resistor network and power dissipation of the analog preprocessing part.

Simulations of the ADC have turned out that the design specifications mentioned above have been met adequatly except for the power dissipation of the ADC which turned out to be a factor 2 to 3 higher than the initial design specifications of 6 - 9 mWatt.

The corresponding lay-out realization of the ADC started by searching for a compact lay-out for the comparators. In addition, the transistors which create the sample and hold circuit have been placed closely together to prevent additional interconnection capacitances being added to the sample and hold circuit in order to attain the designed BER (bit error rate).

The total chip area of the ADC is 4 mm * 4 mm due to the limited numbers of metal layers that could be used during this research and the corresponding design rules of those metal layers.

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LIST OF SYMBOLS

ΔA	amplitude duration
A/D	analog to Digital
ADC	Analog to Digital Convertor
A_{input}	analog input voltage
BER	Bit Error Rate
B_m	m_{th} bit value
DNL	Differential Non-Linearity
D_{out}	digital output data
f_{-3dB}	- 3dB bandwidth
f_{cl}	clock signal frequency
f_{in}	input signal frequency
f_T	transistor cut-off frequency
g_m	mutual transconductance
Ic	collector current
INL	Integral Non-Linearity
k	Boltzmann's constant
LSB	Least Significant Bit
MSB	Most Significant Bit
MSS	Meta-Stable State
n	number of bits
q	electron charge
q_e	quantization error
Q_F	forward charge-control variable
Qm	quantization level m
Q_{VC}	collector stored junction charge
Q_{VE}	emitter stored junction charge
R_{ref}	reference source value
S/N	Signal-to-Noise ratio
T	temperature
Δt	time deviation
t_d	half period time of clock signal
Δt_{max}	maximum sampling time uncertainty
Va	analog voltage
Vbe	base-emitter voltage
Vcb	base-collector voltage
β	transistor current gain
τ_{BF}	base transit time
τ_F	forward charge-control time constant

CHAPTER 1 INTRODUCTION

Todays consumer electronic products, like for instance mobile phones, require high speed data convertors. Therefore, using low power convertors in such products becomes increasingly important in vue of consumer demands and the necessity for manufacturers to meet those demands adequately. The Analog to Digital Convertor (ADC) which presents the subject of research in this report can be considered as an example of such products mentioned above. This ADC has been made in an advanced bipolor IC-process in which no substrate has been used. The former leads to very low parasitic capacitances around the transistors, providing the ideal circumstances for designing low power circuits.

In this report the following subjects will be described. In chapter 2 "SPECIFICATIONS OF AN ANALOG TO DIGITAL CONVERTOR" attention will be payed to some static and dynamic specifications of the ADC. Chapter 3 "INITIAL DESIGN SPECIFICATIONS" will present the initial design specifications which the ADC has to meet. Chapter 4 "THE SPIRIT PROCESS" will discuss the SPIRIT process. This process, which has been developed by Philips Research, can be described as an advanced bipolar process, making very low power circuit design possible. This can be achieved due to the absence of the substrate. Subsequently, a coupling between the substrate and the active region of the transistors is not present. The former presents an ideal condition for successfully implementing a high-speed low power Analog to Digital Convertor. Furthermore, the folding and interpolation technique will be described in chapter 5 "FOLDING AND INTERPOLATION PRINCIPLE". This technique is considered to be an important technique used in an ADC. In chapter 6 "FINE PART" the design of the fine part of the Analog to Digital Convertor will be discussed. In this chapter, attention will be payed to the charge control of the master comparator. This model will be used to determine the resistor value of the interpolation network. Furthermore, the meta-stable state will be discussed in this chapter. Chapter 7 "COARSE PART" will pay attention to the design of the coarse part of the Analog to Digital Convertor. After discussing various parts of the Analog to Digital Convertor in the previous chapters, chapter 8 "THE TOTAL ANALOG TO DIGITAL CONVERTOR" will present the total ADC. In this chapter, the output buffer, diverted from the Fairchild μA702 op-amp for obtaining a cmos compatible output, will be described. In addition, chapter 9 "LAY-OUT" will present the lay-out of the ADC. This report will be concluded with a discussion of the main conclusions based on the research results (chapter 10 "CONCLUSIONS AND RECOMMENDATIONS"). In addition, some recommendations resulting from these research results and conclusions, will be presented.

CHAPTER 2 SPECIFICATIONS OF AN ANALOG TO DIGITAL CONVERTOR

2.1 Introduction

This chapter presents an introduction to the static and dynamic specifications which an Analog to Digital Convertor (ADC) needs to meet for applicability in a digital signal processing system like personal communication products. Therefore in section 2.2 the ADC function will be illustrated. In additional sections the sampling time uncertainty as well as the sampling clock time uncertainty will be discussed (section 2.3 and section 2.4). Section 2.5 will illustrate the signal to noise ratio. Section 2.6 will discuss the Bit Error Rate. Finally in section 2.6 and 2.7 the INL and DNL will be illustrated.

2.2 A/D Convertor function

The basic Analog to Digital Convertor is presented as a black box in figure 2.1.

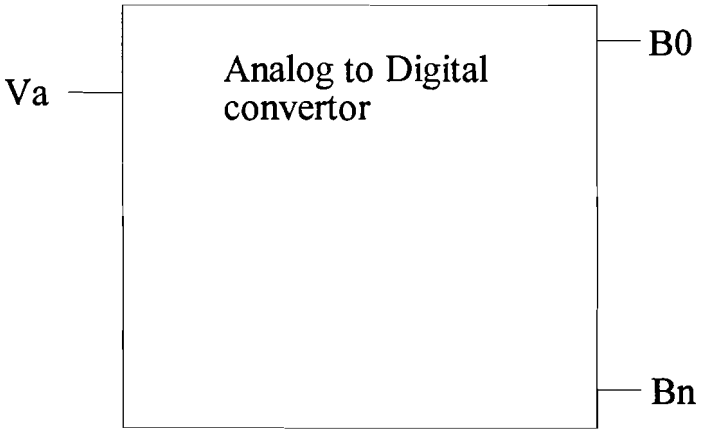


figure 2.1: Block schematic of an Analog to Digital Convertor

The input signal is supplied to the Analog to Digital Convertor and after a certain amount of time the conversion will be established. After the conversion has been established the convertor provides a digital code at its output. This digital output can be written as a function of the input signal. This leads to the following equation:

$$\frac{V_a}{ref} = D_{out} + q_e = \sum_{m=0}^{n-1} B_m 2^m + q_e$$

In this equation D_{out} represents the digitalized value of the analog input signal V_a, whereas q_e represents the quantization error. This error represents the difference between V_a/R_{ref} and the digital signal D_{out} on the condition that n is a finite number. R_{ref} is a reference value, which can be a reference voltage, current or charge.

2.3 Sampling time uncertainty

When sampling an analog signal, additional errors can occur in the output signal caused by sampling time uncertainty. This error occurs when samples are not taken at equal times t, but at times t + Δt (see figure 2.2). Figure 2.2 shows that a Δt time uncertainty introduces an amplitude error ΔA. ΔA has to be smaller than 1 LSB to avoid a significant loss in quantization resolution of the convertor. If the input signal is a sine wave and the input frequency of the convertor is half the sampling frequency, the sampling time uncertainty will introduce the largest error at the zero-crossing of the sine wave. The maximum sampling time uncertainty has been derived in [10]:

$$\Delta t_{max} = \frac{2^{-n}}{\pi * f_{in}}$$

with f_{in} representing the input signal frequency and n the resolution of the convertor. Calculating this for a 8 bit convertor at a clock frequency of 100 MHz, the sampling time uncertainty becomes 25 ps.

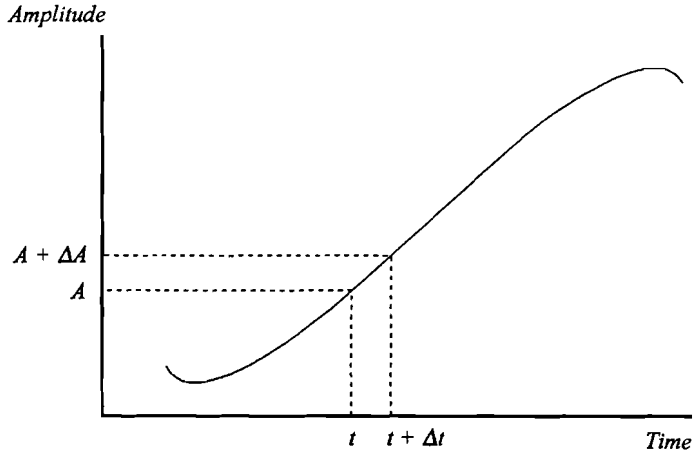


figure 2.2: Sampling time uncertainty

2.4 Sampling clock time uncertainty

By supplying a clock signal to the convertor, information about the pulse-to-pulse time uncertainty can be obtained. Therefore the clock generator is modelled in a way which makes calculations possible. The model for calculating this clock time uncertainty is shown in figure 2.3 with e_n representing the (rms) noise generated by the squaring circuit. Mostly e_n is thermal noise and can be expressed as:

$$e_n^2 = 4kTR_n\Delta f$$

with R_n as the equivalent noise resistance at the input of the squaring circuit.

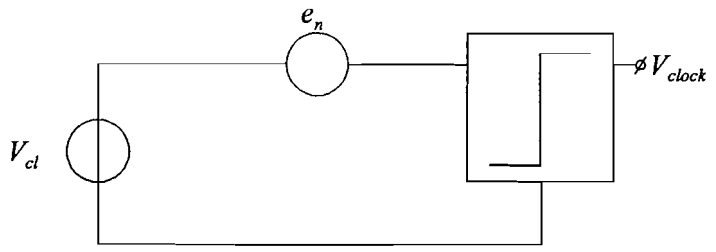


figure 2.3: Clock time uncertainty model

The squaring circuit, with a bandwidth f_b, is supplied by an ideal sine wave $V_{cl} = A \sin \omega t$ with $\omega = 2\pi f_{cl}$. The noise bandwidth Δf is equal to the bandwidth of the squaring circuit. This wide-band noise results in a pulse-to-pulse time uncertainty which depends on the noise amplitude and the slope of the sin wave input signal. The equation for the pulse-to-pulse time uncertainty has been calculated in [10] and results in:

$$\Delta t_{cl} = \sqrt{\frac{2\pi kTR_n f_b}{\pi f_{cl} A}}$$

with $k = 1.38\ 10^{-23}$ J/K and temperature T in Kelvin.

The pulse-to-pulse time uncertainty Δt_{cl} has to be smaller than the maximum sampling time uncertainty Δt_{max} calculated in section 2.3. This puts a very stringent demand on the equivalent noise resistance R_n.

2.5 Signal to noise ratio

Signal to noise ratio is a very important dynamic specification of an Analog to Digital Convertor in digital signal processing systems. It depends on the resolution of the convertor, and thus on the number of quantization levels $2^n - 1$. The theoretical signal to noise ratio for a sine wave has been calculated in [10] and results in:

$$\frac{S}{N} = 6.02*n + 1.76\ dB$$

For an ideal 8 bit convertor the S/N = 49.92 dB. This number can never be met because of the sample time uncertainty and non-linearity in an Analog to Digital convertor.

2.6 Bit Error Rate

In Analog to Digital Convertors many decisions are being made during the conversion time. If a wrong decision is made, the internal code will be converted in a wrong output code. This wrong output can be a meta-stable condition of a comparator. A meta-stable condition of a comparator is an output code level that does not confirm the logic "1" or "0". The meta-stable condition will be further explained in section 6.3.

The number of errors made during the conversion time of a convertor can be presented as the Bit Error Rate (BER). The comparators of the Analog to Digital Convertor need to be designed for a BER between 10^{-10} and 10^{-15} for a high quality convertor.

2.7 INL

The integral non-linearity (INL) can be defined as the deviation of the output code of an Analog to Digital Convertor from a straight line drawn through zero and full scale (see figure 2.4). The output codes for calculating the INL has to be corrected for a possible zero offset. In practical circuits such as input amplifiers, output buffers and comparators, this offset is caused by the finite matching of components.

Monoticity of the convertor is guaranteed if the INL is equal or smaller then ½ LSB [10].

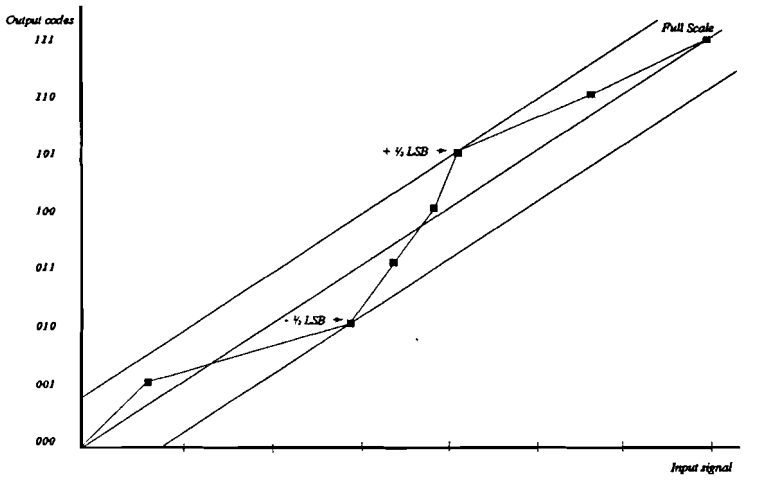


figure 2.4: Integral non-linearity of an Analog to Digital Convertor

2.8 DNL

The differential non-linearity (DNL) describes the difference between two adjacent digital output codes compared to 1 LSB of the Analog to Digital Convertor generated by two adjacent analog signal values. This leads to the following equation:

$$DNL = A_{input}(Q_m + 1) - A_{input}(Q_m) - 1\,LSB$$

with Q_{m+1} and Q_m being two adjacent quantization levels and $A_{input}(Q_m)$ being the analog input voltage corresponding to the quantization level q_n.

From this equation it can easily be understood that if every transition to its neighbour is 1 LSB the DNL will be zero.

CHAPTER 3 INITIAL DESIGN SPECIFICATIONS

This chapter presents the specifications which the Analog to Digital Convertor needs to meet. The specifications were determined at the beginning of the research project [1]. These specifications are illustrated in table 3.1.

table 3.1: Design specifications of an ADC

Initial Design Specifications	
Technology	SPIRIT
Resolution	8 bit + overflow/underflow outputs
Signal to Noise Ratio (SNR)	> 50 dB
Maximum Analog Bandwidth	50 MHz
Conversion Rate	100 MHz
Analog input signal voltage range	1 V_{pp}
Power Consumption	6 - 9 mWatt
Supply Voltage	3 Volt

The specifications presented above have been obtained from a new standard in mobile telecommunication.

These specifications were very preliminary because not all the process parameters were known at the beginning of this research project (like for instance the parasitic capacitances around the transistor). At the time they became available, the demand of the power consumption turned out to be unrealistic because of the large capacitances being a very high load to the transistors. Therefore the power consumption of the ADC will now become a factor 4 larger.

SPIRIT is an advanced bipolar IC process having a high f_T at low current values, which indicates that very fast circuits can be designed with low power consumption. The SPIRIT process will be further discussed in chapter 4 "*THE SPIRIT PROCESS*".

CHAPTER 4 THE SPIRIT PROCESS

4.1 Introduction

SPIRIT, an advanced bipolar process, has been developed by Philips Research. The process makes very low power circuit design possible, which is a major advantage of this process. The low power circuit design can be achieved due to the absence of the substrate which implies that there is no coupling between the substrate and the active region of the transistors. Due to the absence of parasitic capacitances this presents an ideal condition for implementing a high speed low power Analog to Digital Convertor.

In this chapter the SPIRIT process will be discussed, consisting of a discussion of the resistors and NPN transistors in section 4.2. In addition the capacitance which can be used in the design will be discussed in section 4.3.

4.2 Resistors and NPN transistors

The different types of resistors have already been discussed in [1]. Therefore they will not be discussed in this section. The same goes for the NPN transistors which are being used for the design of the ADC.

Figure 4.1 presents a NPN transistor with additional parasitic capacitors. These capacitors are listed in table 4.1.

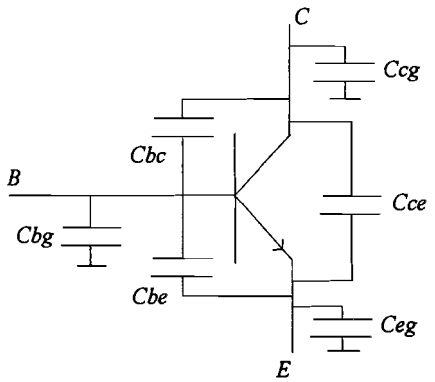


figure 4.1: NPN transistor with additional parasitic capacitors

table 4.1: List of parasitic capacitors

Parasitic Capacitors	Value
C_{BC}	2.0200E-16
C_{CE}	4.8700E-16
C_{BE}	1.3000E-15
C_{CG}	4.7000E-16
C_{BG}	1.0700E-15
C_{EG}	5.6000E-16

Simulations aimed at obtaining information for the design of the various circuits of an ADC are performed on the NPN transistor. An important characteristic for the design of a circuit is the cutt-off frequency f_T versus collector current I_C characteristic shown in figure 4.2. This characteristic has been simulated for several V_{cb} voltages. Furthermore, the V_{be} versus collector current I_C characteristic is also important for it supplies information about the bias adjustments. The V_{be} versus I_C characteristic is illustrated in figure 4.3.

Due to the emitter resistor of the transistor [1], which is the serie resistance between the external emitter terminal and the internal emitter region, the calculated gain of the differential amplifiers will not be met. This resistor introduces additional emitter degeneration (see section 7.3) in the amplifier circuit.

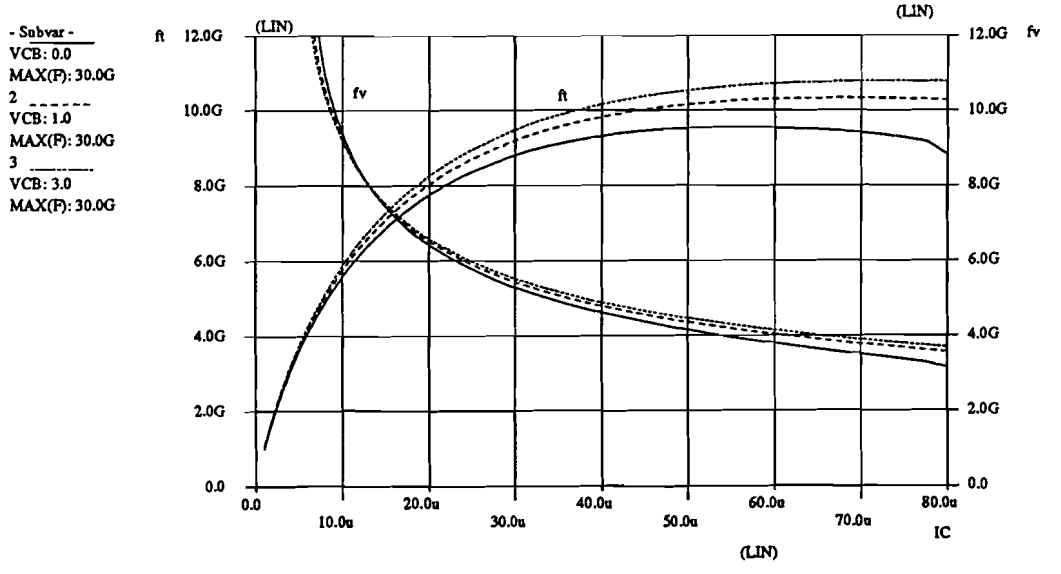


figure 4.2: f_T versus I_C characteristic

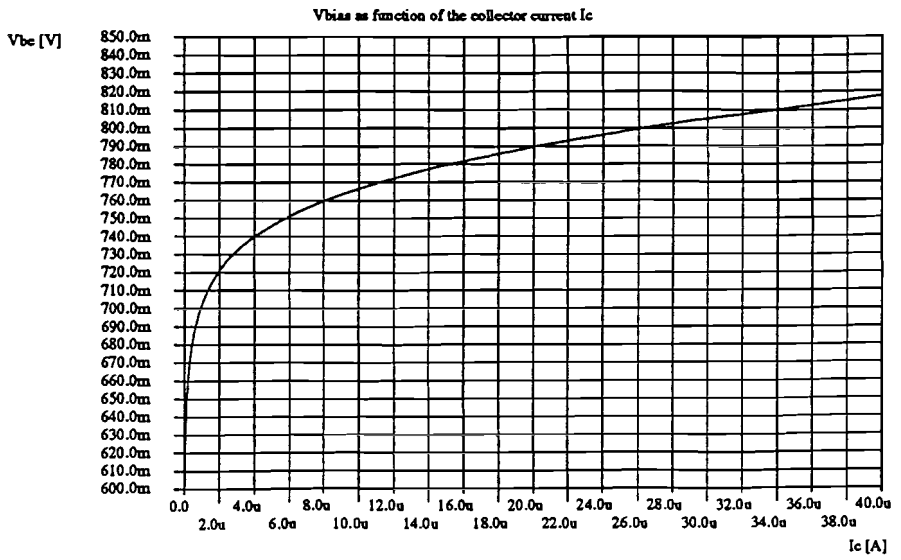


figure 4.3: V_{be} versus I_C characteristic

4.3 Capacitors

Two types of capacitors can be used in the SPIRIT process.

1) $C_{IN\text{-}INS}$. The typical value of the capacitor is 3.15 fF. IN and INS are two kinds of metal that can be used in the SPIRIT process.

2) mnos The typical value of the mnos capacitor is 57.5 fF for a capacitor of dimensions 5 * 5 μm.

Only the mnos capacitor is used in the design of the Analog to Digital Convertor due to its higher typical value.

CHAPTER 5 FOLDING AND INTERPOLATION PRINCIPLE

5.1 Introduction

A high-speed Analog to Digital Convertor can be designed as a full-flash convertor. This convertor consists of an array of $2^n - 1$ comparators followed by the encoding logic which generates the output code of the convertor. The factor n represents the number of bits.

The comparator is connected with one input to the input signal and with the other input to a reference ladder. A major disadvantage of this architecture is the large power consumption and the large chip area taken in on the die.

Another way of designing a high-speed Analog to Digital Convertor is by using the folding and interpolation technique. The result of applying this technique is the use of less comparators because they are used in a very efficient way. Hence, fewer comparators use less power consumption and take in less chip area. No sample-to-hold amplifier is required for this convertor. The architecture of a folding and interpolation high-speed ADC is presented in figure 5.1.

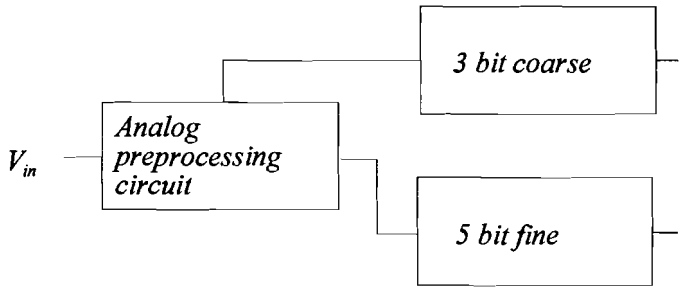


figure 5.1: Architecture of an ADC

The folding and interpolation principle will be described in section 5.2. In section 5.3 the analog preprocessing will be discussed, presenting the condition to be met in order to obtain a correct functioning ADC.

5.2 Folding and interpolation principle

The input signal is supplied to the analog preprocessing circuit (see figure 5.1). This analog preprocessing circuit consists of input amplifiers and folding circuits.

In this design a folding factor of 8 has been chosen resulting in an 8 times folded input signal (see figure 5.2) which can be represented by a 3 bit coarse part. Subsequently, a folding factor of 8 results in a partition in 5 bit fine and 3 bit coarse (see figure 5.1).

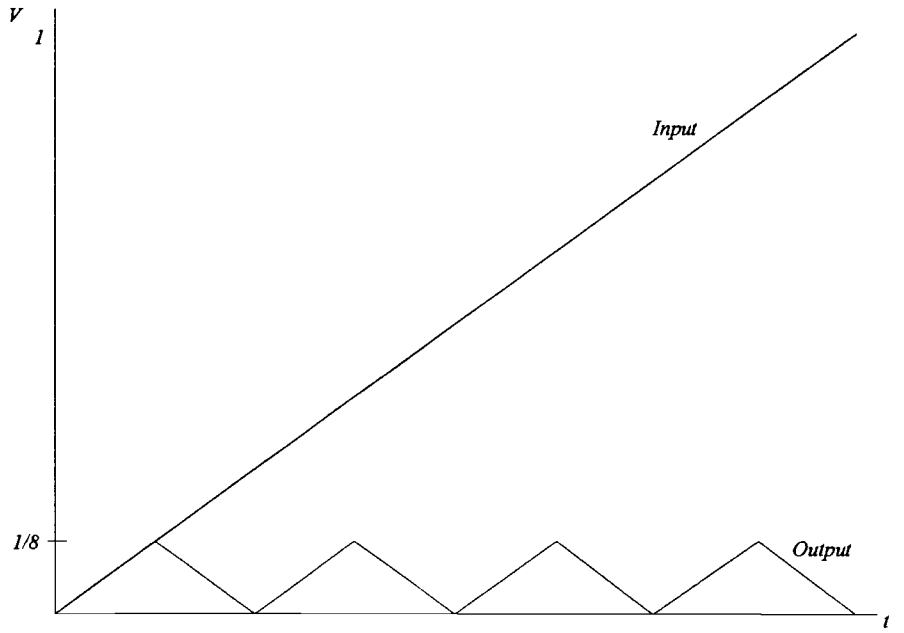


figure 5.2: An 8 times folded input signal

The fine part of the preprocessing circuit has 36 input differential amplifiers. In order to obtain a three times folded signal, three output signals of the input differential amplifiers are connected to the 3-fold circuit with the middle signal inverted. This results in twelve 3-fold output signals which are connected to the 9-fold circuit (see figure 5.3), generating a nine folded signal.

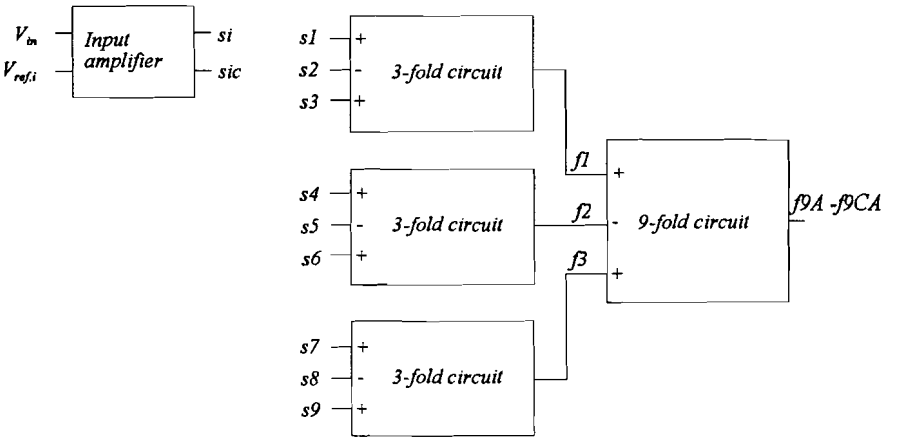


figure 5.3: Folding circuit of the ADC

The output signal is folded nine times (see figure 5.4) in order to generate the circular code used as the internal code of the Analog to Digital Convertor. The major advantage of this code is the possibility of a "0" to "1" detection performed by the EXOR function which can be used to drive the rom table (see section 6.1) in order to generate the binary output code of the convertor. The circular code is shown in table 5.1.

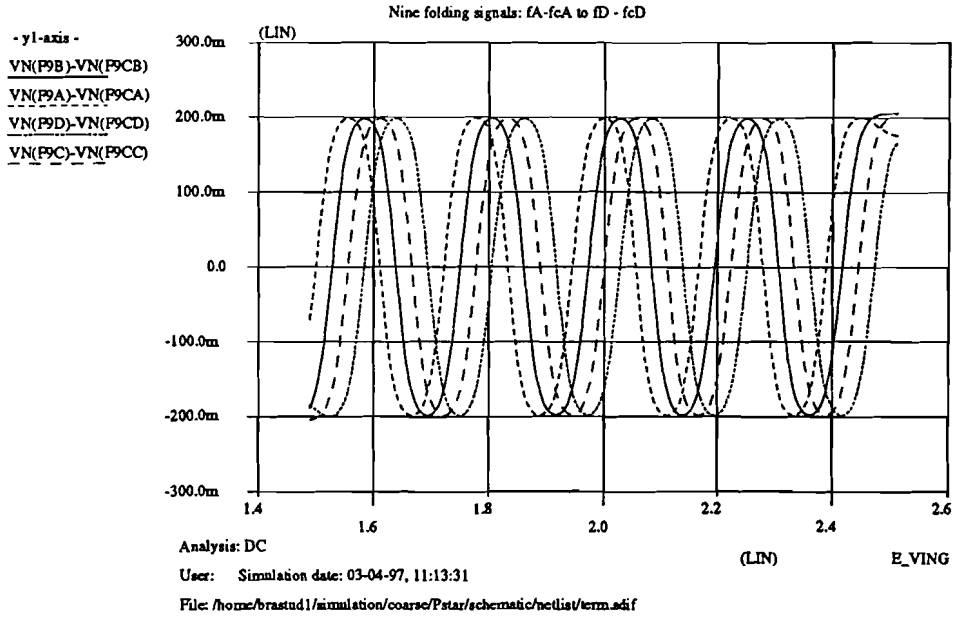


figure 5.4: Output signals of the 9-fold circuits

table 5.1: Circular code used in the ADC illustrated for 3 bit

Binary code	Circular code
000	0000
001	0001
010	0011
011	0111
100	1111
101	1110
110	1100
111	1000

Interpolating between the nine folded signals with a resistor network of 8 resistors results in the 32 zero-crossings for the comparators which are of the master-slave type. The interpolation resistor network is shown in figure 5.5. In figure 5.6 the corresponding output signals of the interpolation resistor network are illustrated. In figure 5.5 additional resistors are added for impedance adjustments, so all interpolated signals have equal signal delay.

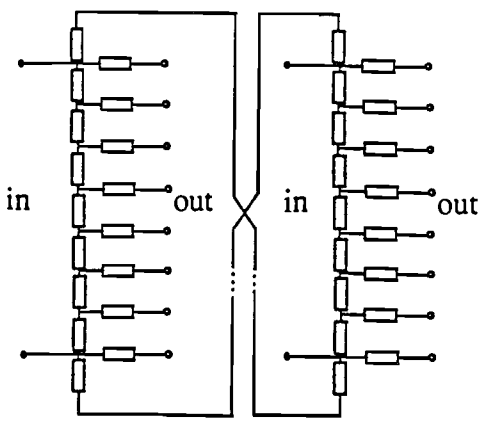


figure 5.5: Interpolation resistor network

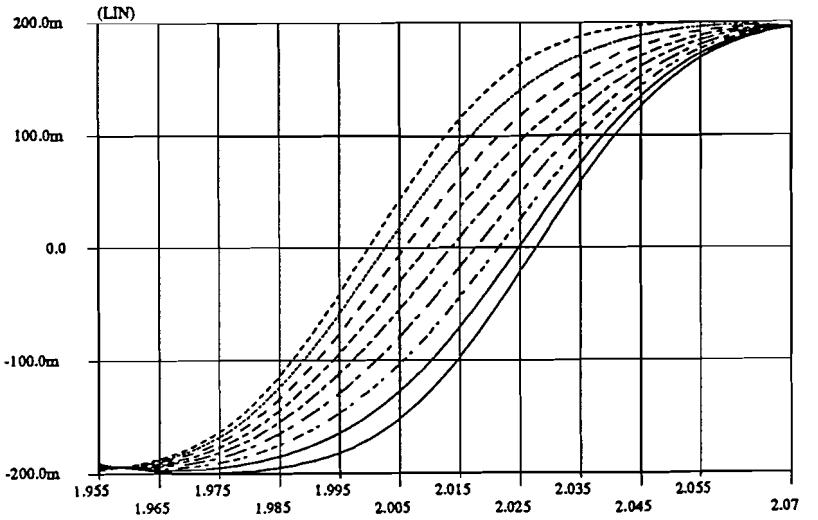


figure 5.6: Output signals of the interpolation resistor network

5.3 Preprocessing part

The preprocessing part has been designed in [1]. From this design only the simulated specifications will be presented here (see table 5.2).

table 5.2: Simulation results of the preprocessing part of the ADC

Preprocessing part of the ADC	
System architecture ADC	Cascaded folding with 8 times interpolation
Resolution	8 bit
Input voltage range	8/9 Volt
Bandwidth preprocessing part	500 MHz
Maximum analog input signal frequency	50 MHz
Maximum gain at zero-crossings	8
Maximum output voltage swing	400 mVolt
INL	$< \pm 0.3$ LSB
Max. distortion component at f = 50 MHz	- 55 dB
Power supply voltage	3 Volt
Tot. power dissipation preprocessing part	5950.55 µWatt

The preprocessing part is illustrated in figure 5.1. The linking of the fine part with the coarse part is of crucial importance in vue of a correct functioning of the Analog to Digital Convertor. For this reason, this subject will be discussed here.

If a ramp signal is being used as an input signal for the ADC (see figure 5.7) the coarse part will start with the output code "000". The fine part will have an increasing output code from "00000" (see A in figure 5.7) to "11111" (see B in figure 5.7). A reference step higher, as the input signal still increases, the coarse part has an output code of "001". At the same time the fine part has to have a code transition from "11111" to "00000". This can be achieved by using the signal as labelled F9D7 for the synchronization between the coarse part and the fine part which will be described in chapter 7 "*COARSE PART*". This signal is also used for obtaining the MSB-2 bit. By using the signal F9D7 (indicated by B in figure 5.7) the MSB transition will occur at an input voltage of 1.94 Volt (see C in figure 5.7).

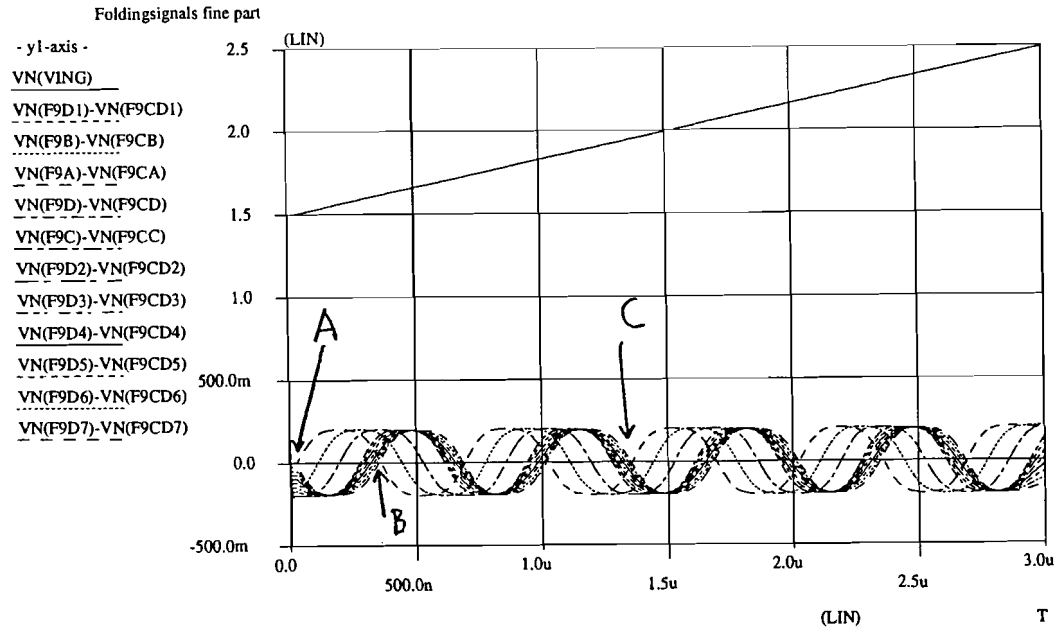


figure 5.7: Output signals of the preprocessing part

CHAPTER 6 FINE PART

6.1 Introduction

In this chapter the fine part of the Analog to Digital Convertor is discussed. The fine part of the ADC is presented in figure 6.1. This figure illustrates that the fine part embraces the following parts:

- comparator;
- EXOR-comb;
- rom table;
- rom-amplifiers;
- EXOR;
- latch;
- buffer.

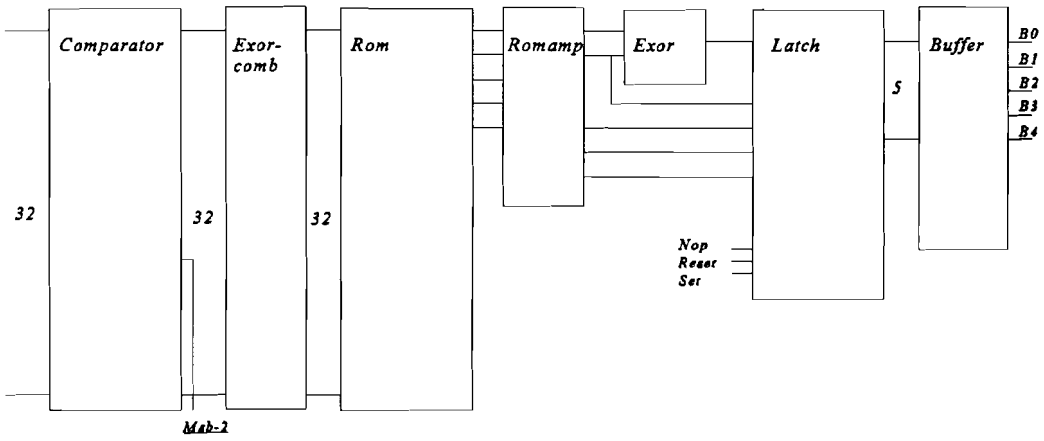


figure 6.1: Block schedule fine part of the ADC

The comparator block is used in order to digitalize the folding signals of the preprocessing part, whereas the EXOR-comb block is used to detect the "0" to "1" decision of the comparator outputs. Furthermore, the output of the EXOR-comb block is used to drive the rom table which delivers the binary output code of the fine part. In this rom table error correction is implemented for the LSB bit. Because of using this error correction the LSB bit needs to be reconstructed from the LSB and LSB+1 signals. The romamp block amplifies the differential output signals of the rom table. Finally, the latch block is used in order to enable the binary output code at the same time at the output.

The buffer will be discussed in chapter 8 "*THE TOTAL ANALOG TO DIGITAL CONVERTOR*". The circuits mentioned above will be discussed after deriving the theory for the charge control of a transistor (section 6.2) and the theory for calculating the meta-stable states of a comparator (section 6.3). The meta-stable state is the condition of the output of the comparator after the half-sample time, which can not be used as a logic signal level. The theory of the meta-stable state will be used for designing the comparator by transient analysis in section 6.4.5. The charge control of a transistor will be used to calculate the value of the interpolation resistor connected to the comparator.

In section 6.4 the design of the comparator will be discussed. Section 6.5 will discuss the EXOR-comb circuit whereas section 6.6 will describe the rom table. The EXOR-comb circuit detects the "0" to "1" transition of the comparators which are encoded to the output code of the fine part by the rom table. The rom table embraces a correction function for decision errors made by the comparators. The rom-amplifier which amplifies the signal from the rom table will be discussed in section 6.7. Finally, in section 6.8 the latches which make the output code of the fine part valid at the same time will be described.

6.2 Charge Control

6.2.1 Introduction

For the connection of the comparators to the interpolating resistance ladder and therefore the determination of the resistance value the charge control model is used. By using this model one can calculate the base current peak that arises every time the comparator is switched by the clock signal. In order to limit this base current peak a differential pre-amplifier can be placed between the comparator and the interpolating resistance ladder. However, the differential pre-amplifier has a bandpass transfer character, which implies that the base current peak will still occur at the interpolating resistance ladder. The comparator, being a low-low clocked comparator, is presented in figure 6.2.

The base current peak is normally called clock feedthrough noise. This clock feedthrough noise is the main cause of conversion errors made in Analog to Digital Convertors.

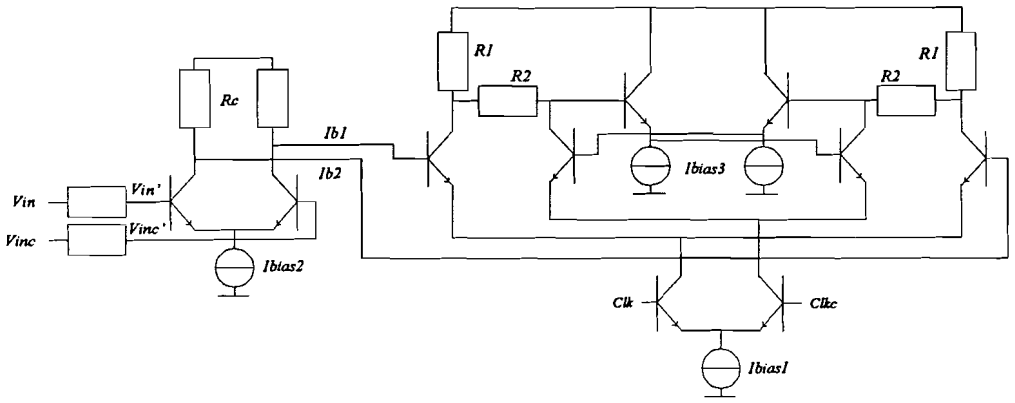


figure 6.2: Circuit diagram of the comparator

6.2.2 Analysis of charge control

The comparator presented in figure 6.2 has a major drawback in case it is placed behind the interpolating resistors. It generates clock feedthrough noise, which arises from base current spikes caused by the on and off turns of the emitter current by the clock signal.

The clock feedthrough noise leads to errors in the Analog to Digital Convertor and is therefore the main reason for degradation of the resolution of the convertor. It is also mixed with the analog input signal and causes distortion. For this reason another comparator is normally used (see figure 6.3). However, in this case this comparator could not be used because counting the Vbe voltages, one can conclude that the supply voltage of 3 Volt is too small. Hence, this comparator might be used after modification like [4, 12, 13]. Since this modification has not taken place during this research project, the comparator shown in figure 6.2 will therefore be used after all.

This clock feedthrough noise will now be analysed by charge control. Therefore the base current of the track circuit of the comparator will be analysed, assuming that the base currents are equal.

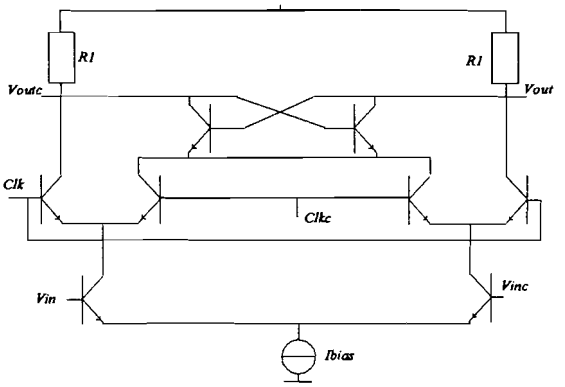


figure 6.3: Circuit diagram of the high-high clocked comparator

The emitter current has been derived in [9] and is presented in figure 6.4.

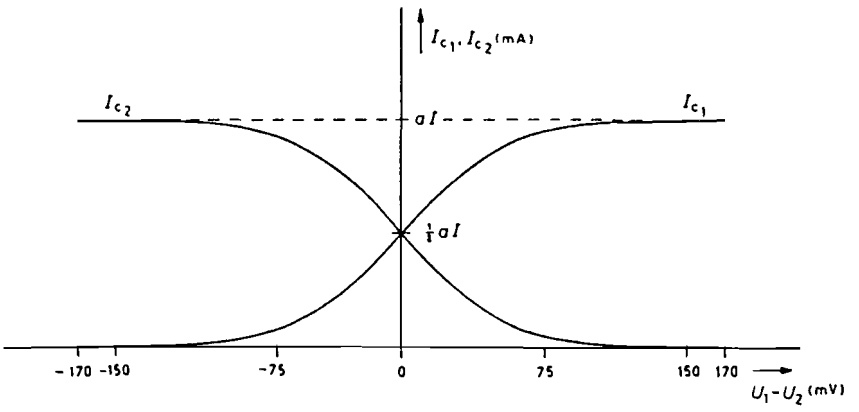


figure 6.4: Emitter current of a differential pair

This figure can be translated into the following equation:

$$I_c = \frac{1}{2} I_{bias1} [1 \pm \tanh(\frac{q\Delta V_{c1}}{2kT})]$$

Assuming that both base currents are equal only I_{b1} is derived. In this case the collector current can be described as:

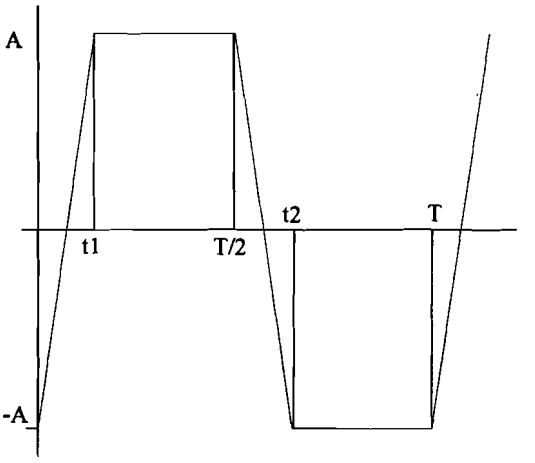
$$I_c = \frac{1}{4} I_{bias1} [1 + \tanh(\frac{q \Delta V_{cl}}{2kT})]$$

with $\Delta V_{cl} = V_{clk} - V_{clkc}$. The used clock signal is equal to the signal illustrated in figure 6.5.

Hence, only a value of t between 0 and t1 and between T/2 and t2 is interesting in this case, because during that time the charge changes in the elements of the charge model (see figure 6.6). Taking this into account, Ic can be written as:

$$I_c = \frac{1}{4} I_{bias1} [1 + \tanh(\alpha t)]$$

with α being positive if the edge of the clock signal increases and α being negative if the edge of the clock signal decreases.



$$\Delta vcl = \begin{cases} \alpha t & \text{for } 0 < t < t1 \\ A & \text{for } t1 < t < T/2 \\ -\alpha t & \text{for } T/2 < t < t2 \\ -A & \text{for } t1 < t < T/2 \end{cases}$$

figure 6.5: Clock signal of the ADC

If the transistor operates in the forward active region and cutt-off region, the charge control model [7] can be illustrated as (see figure 6.6):

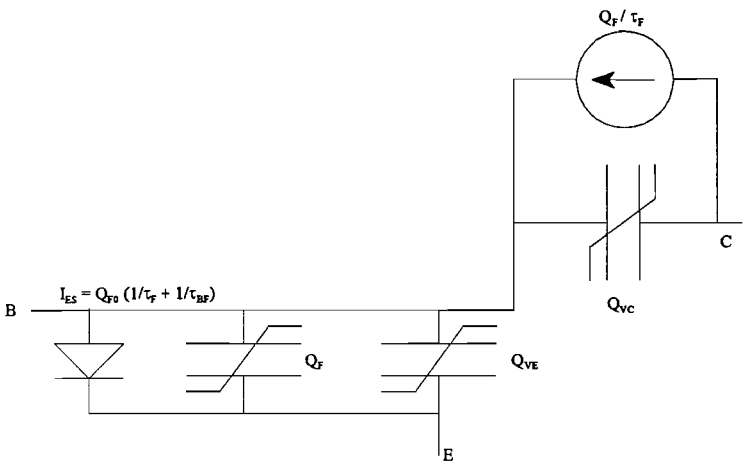


figure 6.6: Charge control representation of a NPN transistor

with the following equations for the collector and the base current:

$$i_c(t) = \frac{Q_F}{\tau_F} - \frac{dQ_{VC}}{dt}$$

$$i_b(t) = \frac{Q_F}{\tau_{BF}} + \frac{dQ_F}{dt} + \frac{d(Q_{VE} + Q_{VC})}{dt}$$

The current dQve/dt can be disregarded because of the base-emitter voltage varying only slightly under forward bias. In addition dQvc/dt can also be ignored considering the fact that the collector voltage is assumed to be constant. For the same reasons the parasitic capacitances around the transistors can be disregarded. Under these conditions and assuming that ic ~ ie, the base current spike can easily be derived. This leads to:

$$i_e(t) = \frac{Q_F}{\tau_F} = \frac{1}{4} I_{bias1}[1 + \tanh(\alpha t)] \qquad (6.1)$$

$$i_b(t) = \frac{Q_F}{\tau_{BF}} + \frac{dQ_F}{dt} \qquad (6.2)$$

with $\tau_{BF} = \beta \tau_F$.

Substituting equation (6.1) into equation (6.2) leads to:

$$i_b(t) = \frac{i_c(t)}{\beta} + \frac{\alpha I_{bias1} \tau_F}{4}[1 - \tanh^2(\alpha t)]$$

After deriving the equation for the base current spike, it appears to exist of two terms. The first term is proportional to the collector current. The second term appears as a current spike. The magnitude of this spike is dependent on the slew-rate of the emitter current and therefore on the clock frequency.

The base current spike analysed here is fed back to the differential pre-amplifier. This base current spike is transformed to high frequency ringing noise due to the inverse transfer characteristic of the pre-amplifier. The small-signal equivalent circuit [2] is shown in figure 6.7. Once again only one side of the pre-amplifier has been analysed due to the symmetry of the circuit mentioned before.

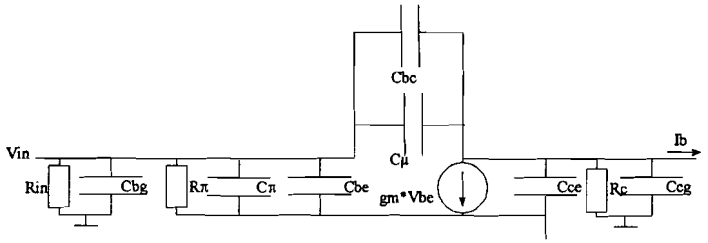


figure 6.7: Small-signal equivalent circuit

The value of the capacitances Cbe, Cce, Cbc, Cbg and Ccg will be explained in chapter 4 "*THE SPIRIT PROCESS*". The other elements of the small-signal equivalent circuit are discussed in appendix 1.

Figure 6.8 shows the small-signal equivalent circuit for practical analysis of the inverse transfer characteristic. All elements that do not effect the inverse transfer characteristic have been removed.

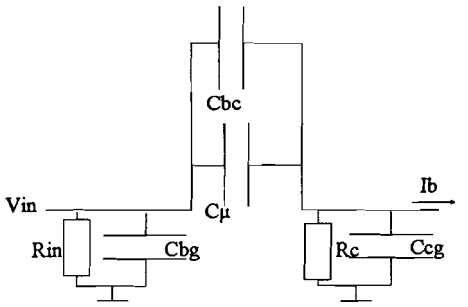


figure 6.8: Practical equivalent circuit

Using Kirchhoff's current law, the inverse transfer characteristic can be derived, leading to the following equation:

$$\frac{V_{in}}{I_{bl}} = \frac{s(C_{\mu} + C_{bc})}{\frac{1}{R_{in}R_c} + s\left(\frac{C_{\mu} + Cbc + Ccg}{R_{in}} + \frac{C_{bg} + C_{\mu} + C_{bc}}{R_c}\right) + s^2(C_{bg}C_{cg} + (C_{bg} + C_{cg})(C_{\mu} + C_{bc}))}$$

This inverse transfer characteristic has been simulated with PSTAR. The simulation results are illustrated in figure 6.9.

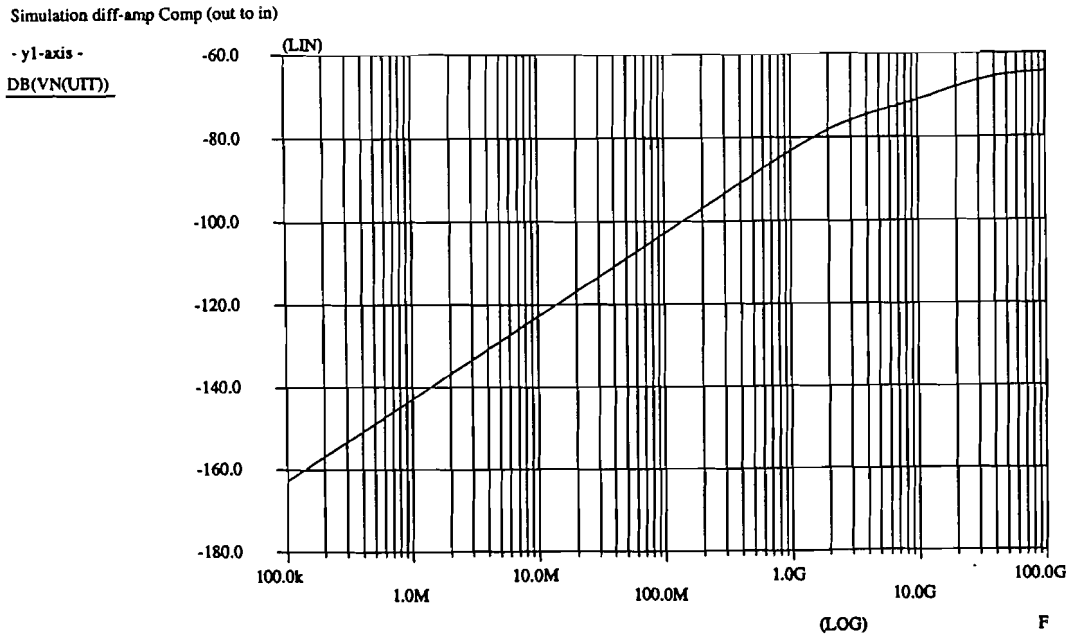


figure 6.9: Inverse transfer characteristic of differential pair

Simulations are used in order to obtain the resistor value of the interpolation resistor network, resulting in a resistor value of 2.5 kΩ.

This resistor value is an optimum between clock feedthrough noise at the output of the interpolation resistor network and power dissipation of the nine fold block [1]. Simulations are executed by supplying the comparator (see figure 6.2), which has the same current settings and resistor values as the master comparator of section 6.4.2, with a differential voltage of 10 μVolt at its inputs Vin and Vinc. At Vin' and Vinc' the clock feedthrough noise is measured and is presented in figure 6.10. The clock signal with a frequency of 100 MHz is supplied to clk whereas the inverted clock signal is supplied to clkc. In figure 6.10 the clock signal clk goes high at t = 345 ns which means that α is positive as presented before. At t = 350 ns the clock signal clk goes low which means α is negative.

In this section in which the base current spike has been calculated the base-emitter voltage has been assumed to vary only slightly under forward bias. This assumption is true if the clock frequency is high enough. If the clock frequency is not high enough the base-emitter voltage will rise to the base voltage with the RC-time of the resistance R_π and $C_\pi + C_{bc}$ shown in the small-signal equivalent circuit (see the equations in appendix 1). This is a very non-linear process. The elements R_π and C_π depend on I_c and V_{be} and consequently the value of the elements will change and therefore the RC-time will change.

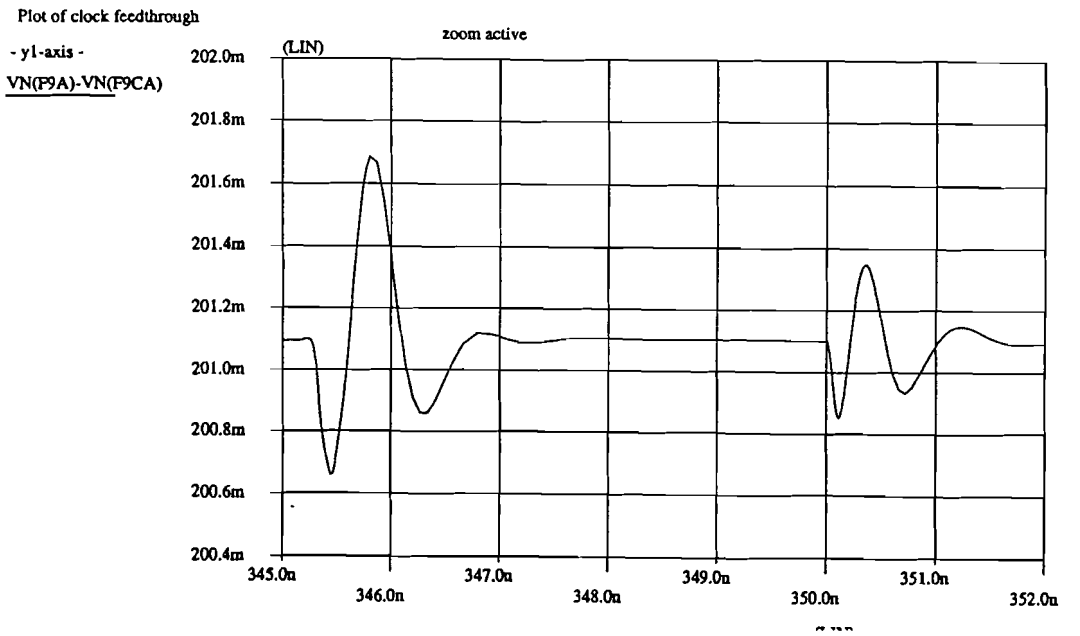


figure 6.10: Clock feedthrough noise at interpolation resistors

6.3 Failure rate of comparators caused by meta-stability

6.3.1 Introduction

When a comparator is used for making a decision, either a digital "0" or a digital "1", it is possible for the input signal to be that small, that by the end of the half-sample time no decision has been made. If the comparator has made no decision the comparator is in its meta-stable region which means that it is in a Meta-Stable State (MSS) (see figure 6.11 with Vm as the meta-stable voltage at the middle of the meta-stable region).

Since the meta-stable state provides neither a digital "0" nor a digital "1", one can conclude that the comparator makes a decision error. This error is passed on to the digital circuitry following the comparator in the Analog to Digital Convertor. As a result the ADC will reveal an incorrect output code, presuming no error correction system is placed behind the comparators.

Taking the former into account, the aim is to find a criterion that is useful during the design of the comparator, determining the number of Meta-Stable States. Circuit noise (see appendix 2 for an overview of sources of noise in a transistor) has no influence on the number of MSS of the comparator.

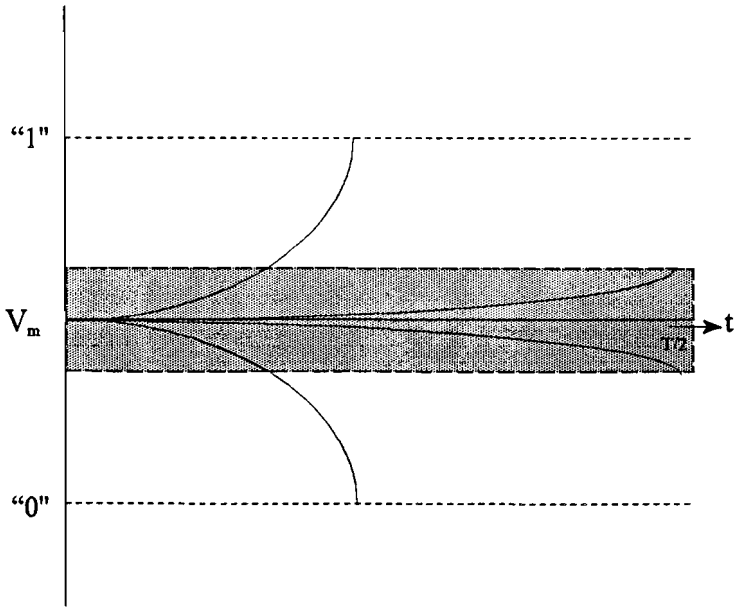


figure 6.11: Comparator output

6.3.2 Small-signal behavior of a comparator

A comparator can be modelled, approximately, by two stages with amplification -A followed by an RC-filter with time constant $\tau = RC$ and the output of the second RC-filter being fedback to the input of the first amplifier (figure 6.12).

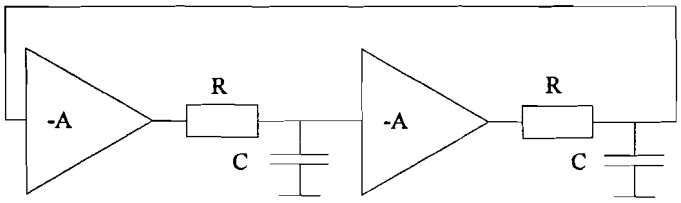


figure 6.12: First order model of a comparator

The feedback theory can now be used to determine the meta-stable condition [15]. This results in the following equation:

$$1 - A^2 = 0 \qquad with\ A = \frac{A_0}{1 + s\tau}$$

The solutions of the differential equations describing the system (see appendix 3) are:

$$v_1 = \lambda_1 \exp(\frac{A_0 - 1}{\tau}t) + \lambda_2 \exp(\frac{-A_0 - 1}{\tau}t) \qquad (6.3)$$

and

$$v_2 = -\lambda_1 \exp(\frac{A_0 - 1}{\tau}t) + \lambda_2 \exp(\frac{-A_0 - 1}{\tau}t) \qquad (6.4)$$

with λ_1 and λ_2 being integration constants. V_1 and V_2 are the output voltages of respectively amplifier 1 and amplifier 2.

At t = 0 $V_1 = V_{01}$ and $V_2 = V_{02}$ are chosen, leading to the calculation of the integration constants. This results in:

$$\lambda_1 = \frac{V_{01} - V_{02}}{2}, \quad \lambda_2 = \frac{V_{01} + V_{02}}{2}$$

By looking again at the equations (6.3) and (6.4) mentioned before one can conclude that after a time

$$t > \frac{A_0 - 1}{\tau}$$

the second term of both equations can be neglected. If also $V_{01} - V_{02} = 2\delta V_0$ is introduced, representing the input signal, the dominant output voltages can be translated into the following expressions:

$$v_1 = \frac{\delta V_0}{2}\exp(\frac{A_0 - 1}{\tau}t) \tag{6.5}$$

and

$$v_2 = \frac{-\delta V_0}{2}\exp(\frac{A_0 - 1}{\tau}t) \tag{6.6}$$

The difference $V_1 - V_2$, the final state of V_1 and V_2, is equal to the logical swing of the comparator.

6.3.3 The failure rate for meta-stable states

The dominant output voltage derived in section 6.3.2 can now be related to the probability P of a meta-stable state occuring [10, 14, 15] after the sampling time td:

$$P(t > t_d) = \exp(-\frac{A_0 - 1}{\tau}t_d)$$

6.3.4 Designing the comparator

As stated in section 6.3.1 the aim is to find a criterion which is useful during the design of the comparator. This criterion can be found in the factor:

$$\frac{A_0 - 1}{\tau}$$

This factor indicates the probability that a meta-stable state will occur (see also section 6.3.3). In order to design the comparator to this factor a transient analysis can be performed. Therefore, deriving an expression for the determination of this factor based on a transient analysis is necessary.

The output differential signal can be obtained by substracting equation (6.5) from equation (6.6), which results in the following expression:

$$V_{out} = V_1 - V_2 = \delta V_0 \exp(\frac{A_0 - 1}{\tau} t) \tag{6.7}$$

The derivation of equation (6.7) to t leads to the next equation:

$$\frac{\partial V_{out}}{\partial t} = V_{out} (\frac{A_0 - 1}{\tau}) \tag{6.8}$$

Rewriting equation (6.8) the criterion necessary for designing a comparator by transient analysis as stated before can be obtained:

$$\frac{A_0 - 1}{\tau} = \frac{1}{V_{out}} \frac{\partial V_{out}}{\partial t}$$

The criterion derived above will be applied in section 6.3.5.

6.3.5 Design by transient analysis

In this section the theory derived in section 6.3.4 will be applied to a comparator. The clock signal with a frequency of 100 MHz is put at input Clk whereas the inverted clock signal is put at input Clkc in order to perform the transient analysis mentioned before. The inputs Vin and Vinc are supplied with a DC-voltage source in serie with an AC-source.

This AC-source is a sine generator with an amplitude of 10 μVolt. The output signal as well as the factor $(A_0 - 1)/\tau$ are presented in figure 6.13. Based on this figure one can conclude that the factor $(A_0 - 1)/\tau = 11.10^9\ s^{-1}$.

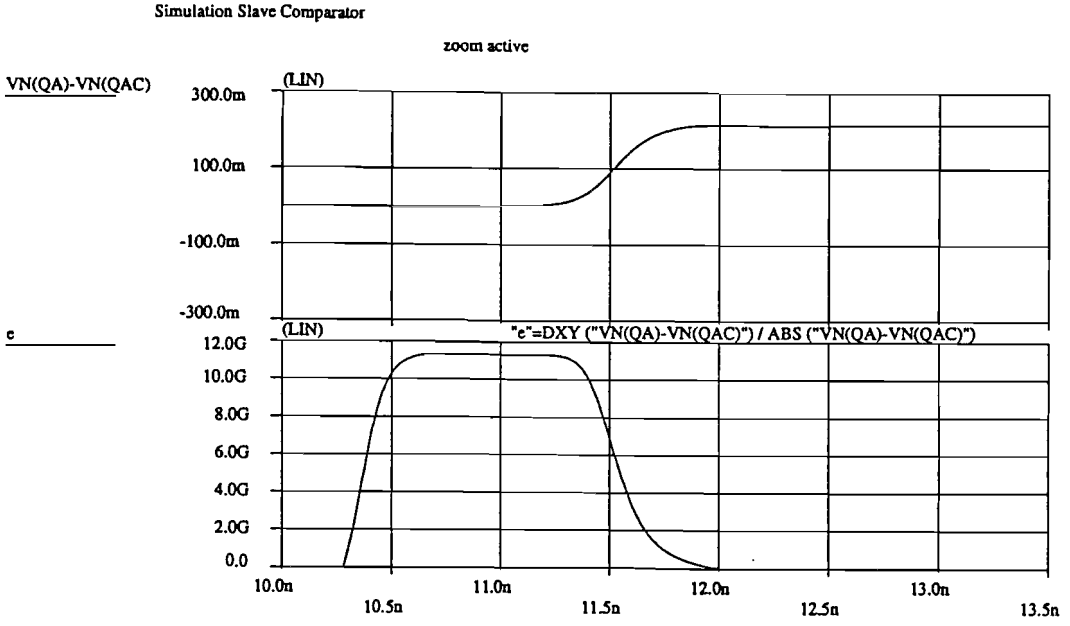


figure 6.13: Transient analysis of a comparator

Knowing the factor $(A_0 - 1)/\tau$ the probability of a meta-stable state occuring can be calculated. This results in the following equation based on the equation presented in section 6.3.3:

$$P(t > t_d) = \exp(-\frac{A_0 - 1}{\tau} t_d) = 1.3 * 10^{-24}$$

with td = 5 ns being the half period time of the clock signal of 100 MHz.

6.4 Comparator

6.4.1 Introduction

The comparator used in the Analog to Digital Convertor is of the master-slave type in order to obtain a higher sensitivity and therefore a reduction of the bit error rate. The master comparator drives the slave comparator. In this way the digitalized folding signals are kept constant during one clock period.

In this section 6.4 the master-slave comparator will be discussed. Therefore the master comparator will be discussed in section 6.4.2 whereas the slave comparator will be described in section 6.4.3. Finally, the master-slave comparator will be discussed in section 6.4.4.

6.4.2 Master comparator

6.4.2.1 Introduction

The master comparator is presented in figure 6.14 which illustrates a split-up in the collector load resistor. The improvement accomplished due to this modification is the reduction of the failure rate as described in [10, 14] due to the increase of the gain A_0 during the hold mode of the comparator.

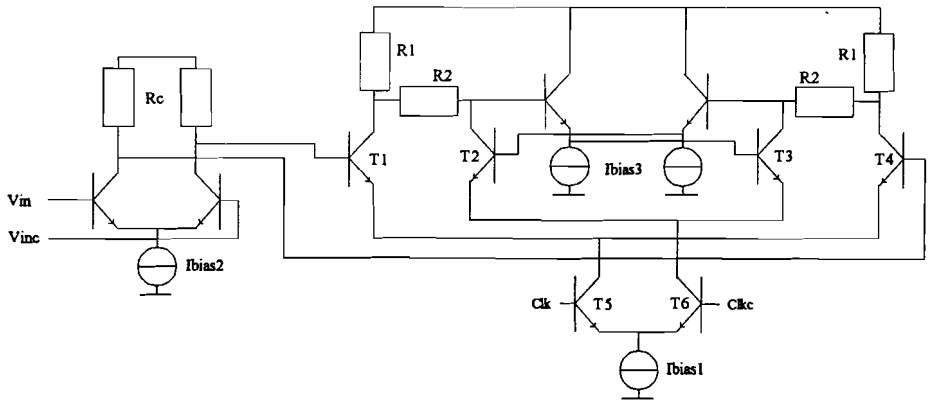


figure 6.14: Master comparator with split-up collector resistors

The master comparator has a differential input Vi = Vin - Vinc and a differential output Vo = Vout - Voutc. The output signal of the master comparator is a differential signal of 250 mVolt.

In the sample mode the input signal is amplified by the transistors T1 and T4 and the load resistors R1. In this mode the clock signal clk is high whereas the inverted clock signal clkc is low. The amplification in this phase can be described as:

$$A \quad g_{m_{T_1,T_4}} * R_1$$

Due to the split-up of the collector resistors a large signal bandwidth can be obtained.

The circuit is in the hold mode as soon as the signal clk goes high and subsequently the signal clkc goes low. In this mode the circuit makes a decision depending on the input signal during the sample mode, resulting in an output signal being either a digital "0" or "1".

The decision is made by a positively fedback circuit formed by transistor T2 and T3 and the collector resistors R1 and R2. Adding the resistor R2 to R1 will increase the gain of the decision amplifier during the hold mode.

The sample and hold modes are controlled by the transistor couple T5 and T6. These transistors are controlled by the signals clk and clkc and therefore operate as switch. The current function has already been illustrated in figure 6.4, section 6.2.2.

6.4.2.2 Design

The current Ibias1 is set by simulation at a value of 12.4 μA whereas the current Ibias3 is set by simulation at a value of 8 μA. These values are chosen to obtain by simulation an optimum in speed, power dissipation and ringing due to the emitter-follower. The ringing is caused by the output impedance of the emitter-follower [2] which behaves inductively. This has a major impact on the circuit behavior when driving capacitive loads such as the equivalent input capacitance of the transistor. The current of the differential amplifier is set by simulation at 8 μA for a f_{-3dB} bandwidth of 1.04 GHz with the master comparator attached.

After setting the currents one can calculate the resistor values. A current Ibias1 = 12.4 μA leads to a total resistor value of 20.138 kΩ for an output swing of 250 mVolt as stated before. The f-3dB bandwidth in the sample mode is 1.45 GHz. In [14] the smallest bit error rate was found for ratios of R1/R2 between 2/5 and 2/3. In this design a ratio of 0.45 has been chosen which implies that R1 = 6.25 kΩ and R2 = 13.888 kΩ. The value of the resistor in the current source can be calculated by using figure 4.3 in chapter 4 "*THE SPIRIT PROCESS*". The Vbe of a transistor at a current of 12 μA is 0.772 Volt. For a transistor at a current of 8 μA the Vbe voltage is 0.76 Volt. With a Vbias1 of 0.85 Volt this results in a resistor value of 6.416 kΩ for Ibias1 source and a resistor value of 11.25 kΩ for Ibias2 source and Ibias3 source.

The resistor Rcm in the differential amplifier is 59.375 kΩ for a DC-shift of 0.475 Volt. The resistor Rc in the differential amplifier is 31.25 kΩ for a voltage swing of 250 mVolt at a current of 8 μA. The power consumption of the master comparator is 0.109 mWatt.

The master comparator is simulated as described in section 6.3.5. The factor $(A_0 - 1)/\tau = 9.10^9\ s^{-1}$ is presented in figure 6.15 and subsequently $P = 2.9\ 10^{-20}$.

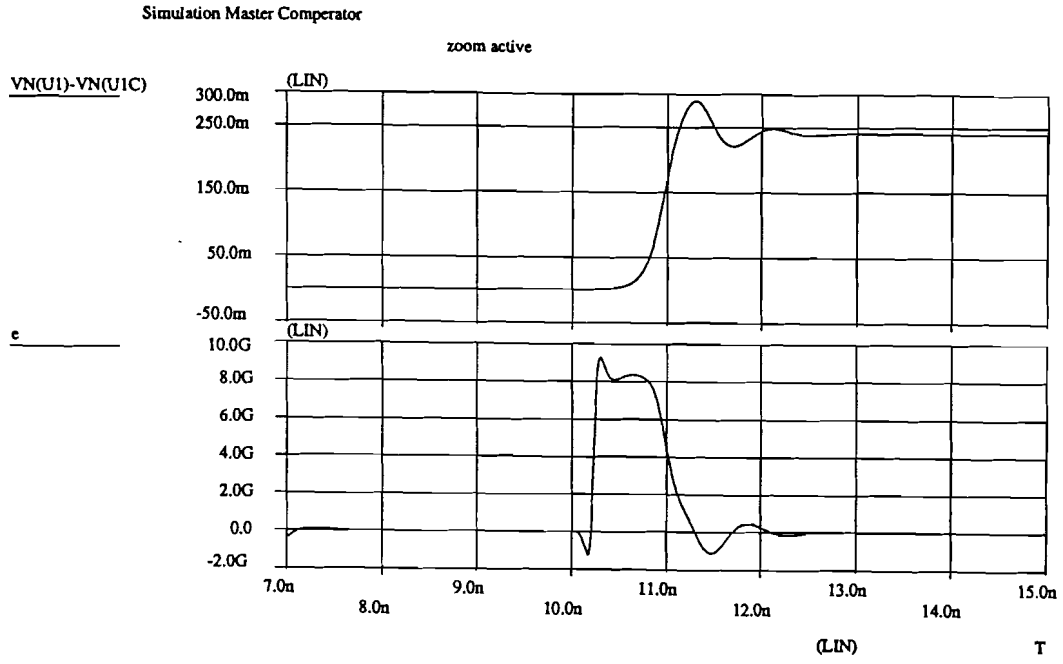


figure 6.15: Transient analysis of the master comparator

The elements of the master comparator are summarized in table 6.1. This table also shows the simulation results.

table 6.1: Calculated and simulated parameters of the master comparator

Parameter	Value differential amplifier	Value comparator
Transistor	n10L24pm, m = 1	
Bandwidth	1.04 GHz	1.45 GHz
Power consumption	0.109 mWatt	
$(A_0 - 1)/\tau$		$9.10^9\ s^{-1}$
Rcm		59.375 kΩ

Parameter	Value differential amplifier	Value comparator
Rc		31.25 kΩ
R1	6.25 kΩ	
R2	13.888 kΩ	
Rbias	11.25 kΩ	6.416 kΩ / 11.25 kΩ
DC-output	2.4 Volt	2.115 Volt

6.4.3 Slave comparator

6.4.3.1 Introduction

The slave comparator which has a differential input Vi = Vin - Vinc and a differential output Vo = Vout - Voutc is presented in figure 6.16. The input and output voltage of the slave comparator are both differential signals with an amplitude of 250 mVolt.

Figure 6.16 illustrates that additional transistors have been added creating a current output at the slave comparator. Interconnecting the current output of the slave comparator in the right way will result in a wired-EXOR function which is being used for detecting a "0" to "1" transition for driving the rom table. The interconnection of the wired-EXOR function will be discussed in section 6.5.

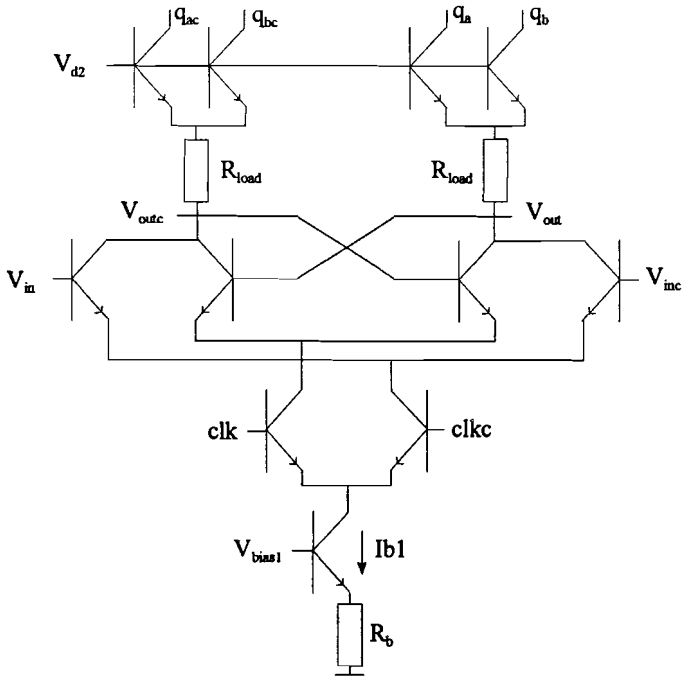


figure 6.16: Slave comparator

6.4.3.2 Design

The current of the slave comparator is set by simulation at 18 μA which results in $(A_0 - 1)/\tau = 5.10^9\ s^{-1}$. The f_{-3dB} bandwidth is 1.16 GHz. Calculating R_{load} for a voltage swing of approximately 250 mVolt results in $R_{load} = 10\ k\Omega$.

The resistor Rb can be calculated using figure 4.3 chapter 4 "*THE SPIRIT PROCESS*". The Vbe voltage of the transistor at a current of 18 μA is 0.786 Volt resulting in Rb = 3.555 kΩ at a Vbias1 = 0.85 Volt for a Vbc of 200 mVolt in conduction. The voltage Vd2 = 2.85 Volt. The power consumption of the slave comparator is 0.054 mWatt.

The results of simulating the slave comparator and the calculated resistor values are summarized in table 6.2.

table 6.2: Calculated and simulated parameters of the slave comparator

Parameter	Value
Transistor	n10L24pm, m = 1
Bandwidth	1.16 GHz
Power consumption	0.054 mWatt
$(A_0 - 1)/\tau$	$5.10^9\ s^{-1}$
Rload	10 kΩ
Rb	3.555 kΩ
Vd2	2.85 Volt

6.4.4 Master-slave comparator

The master-slave comparator digitalizes the folding signals of the preprocessing part [1], keeping it constant during one clock period. The master-slave comparator can be constructed by interconnecting the circuits presented in figure 6.14 and figure 6.16. The total power consumption will become 0.163 mWatt. In the fine part 32 of these master-slave comparators are being used, resulting in a total power consumption of 5.216 mWatt.

The total master-slave comparator is presented in appendix 6.

6.5 The wired-EXOR function

6.5.1 Introduction

By creating a current output at the slave comparator (see section 6.4.3.1) a wired-EXOR function can be created. If the master-slave comparator makes a decision the current will flow into the output qa,qb or qac,qbc. By connecting these currents in a certain way the EXOR function can be obtained.

Figure 6.17 illustrates the interconnections of qa with qbc and of qac with qb of the slave comparators output current.

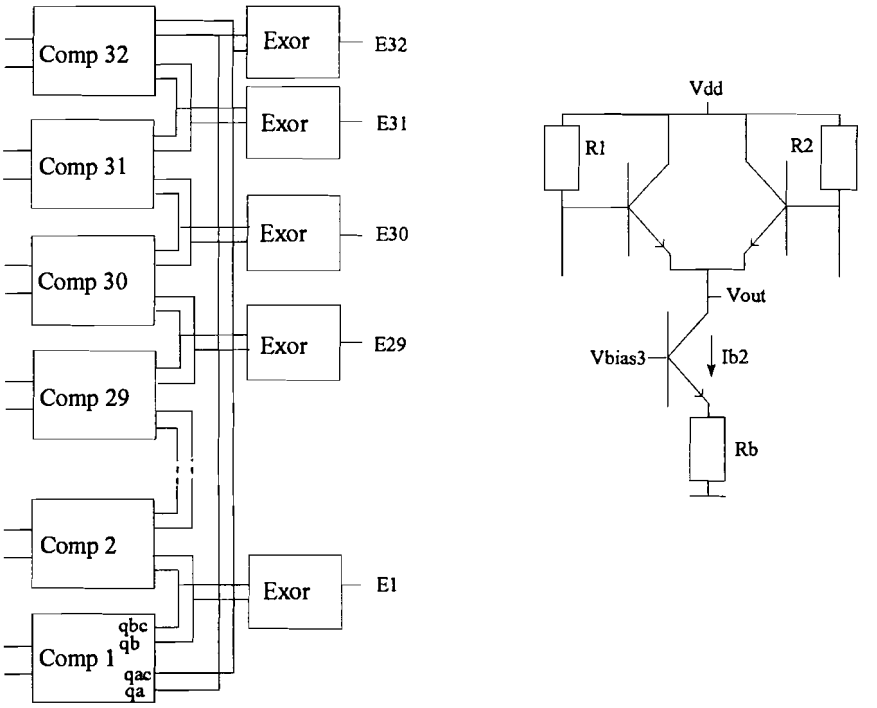


figure 6.17: Interconnection of slave comparators for creating the wired-EXOR function

The following explanation applies to the upper half part of the circular code illustrated in table 5.1, section 5.2. However, an equal explanation can be given for the lower part of the circular code.

Suppose the master-slave comparator, for instance comp 30, makes the decision of a digital "1" due to its input signal. The former implies that all master-slave comparators from comp 1 to comp 29 have a digital "1" as output signal. Suppose the output of the master-slave comparator is a "1". This means that the biasing current Ib1 of the slave comparator flows half through qa and half through qb whereas no current flows through qac and qbc.

The combination of the currents of comp 29 and comp 30, as mentioned before, results in a "low" output voltage E29 = Vdd - ½Ib1*R1 - $Vbe_{(1/2Ib2)}$ due to the fact that equal currents flow through R1 and R2 of the circuit shown in figure 6.17. Master-slave comparator comp 31 reveals an output code of "0" implying that the biasing current flows half through qac and half through qbc. Due to the combination of the currents mentioned before the biasing current Ib1 flows through R1 whereas no current flows through R2.

The former implies that the current Ib2, shown in figure 6.17, flows through the right transistor. E30 therefore becomes Vdd - $Vbe_{(Ib2)}$, the "high" voltage output.

The output voltage E32 is inverted because if the master-slave comparator comp1 would give an output of "1" and comp 32 would still be "0", the output voltage of E32 would be "high". By inverting the current combination E32 will have a "high" output if comp 1 and comp 32 have an output of "1".

6.5.2 Design

The current Ib2 of the wired-EXOR function is set by simulation at 24 μA. The resistors can now be calculated, starting with Rb. The Vbe voltage of the transistor is 0.796 Volt at a current of 24 μA. Using a transistor as diode the voltage lowers another Vbe, resulting in a voltage of 0.408 Volt over the resistor at a Vbias3 of 2 Volt. Therefore the resistor Rb is 17 kΩ. The resistors R1 and R2 have a value of 19.444 kΩ which will result in a voltage of 350 mVolt over the resistors at a current of 18 μA of the combined currents of the slave comparator if a "0" to "1" transition is detected. The collector voltage of the transistors which are attached to the slave comparator to create a current output becomes 2.65 Volt. By supplying these transistors with a voltage of Vd2 = 2.85 Volt the basis-collector voltage is only 200 mVolt in conduction which is allowed.

The "high" output voltage is 2.204 Volt and the "low" output voltage is 2.05 Volt. The power dissipation is 0.072 mWatt.

The parameters calculated before as well as the simulation results are summarized in table 6.3.

table 6.3: Calculated and simulated parameters of the wired-EXOR function

Parameter	Value
Transistor	n10L24pm, m = 1
Power dissipation	0.072 mWatt
R1, R2	19.444 kΩ
Rb	17 kΩ

Parameter	Value
tr	1.0 ns
tf	0.8 ns
td, ts	0.37 ns

6.6 Rom table

6.6.1 Introduction

By using the EXOR function (see section 6.5) a 1 out of 32 output signal is generated. This 1 out of 32 code can be transformed into a 5 bit binary code by using the rom table as illustrated in figure 6.18. A major drawback of the rom table is the fact that the input signal has to be a 1 out of 32 code which implies that only one input of the rom table can be active at the same time.

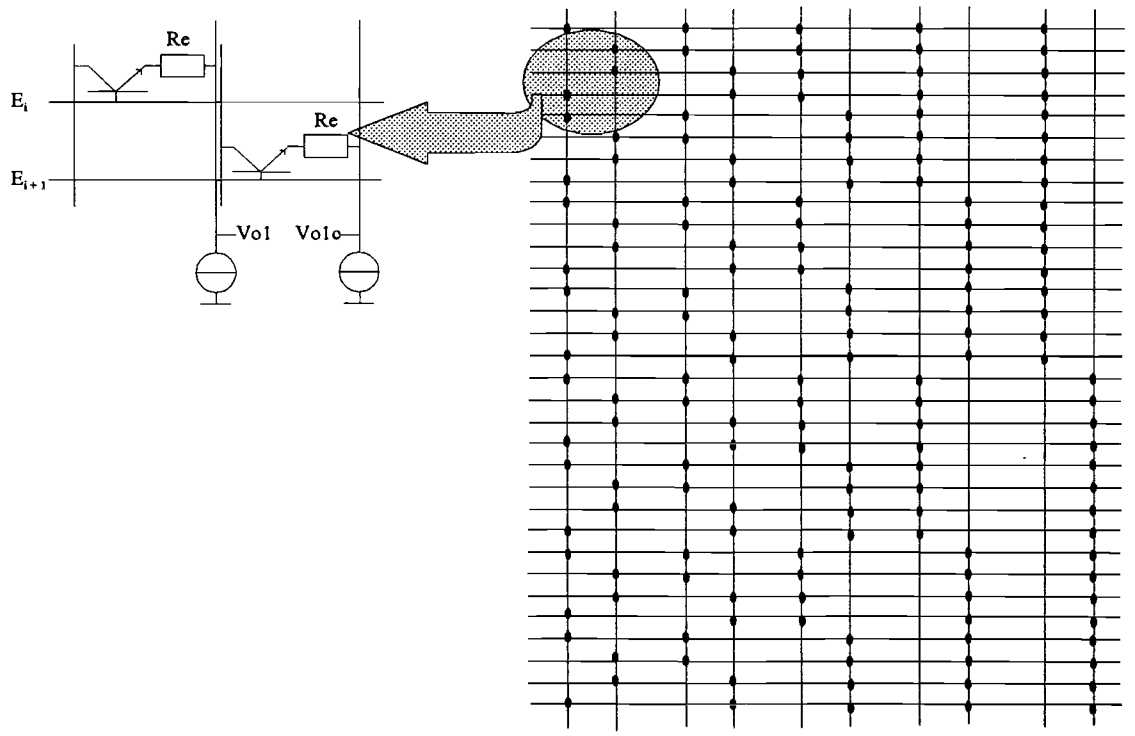


figure 6.18: Rom table

An error correction is necessary considering the fact that the master comparator can make a decision error due to meta-stable states. Therefore a special rom table has been implemented which incorporates the error correction for the LSB bit.

By using the EXOR function the LSB bit can be regained. The upper 4 bits have a normal binary coding scheme. If the master-slave comparator makes a decision error the wired-EXOR output will generate an output code as illustrated in figure 6.19.

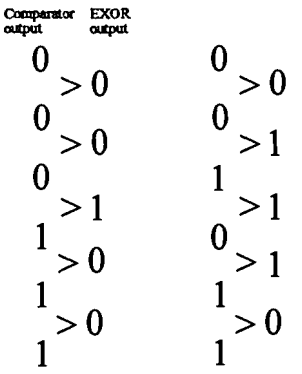


figure 6.19: EXOR output due to MSS

6.6.2 Error correction

If a master-slave comparator makes a decision error the correct 5 bit output code should still be generated. Therefore the rom table presented in figure 6.18 has been implemented. The error correction can be illustrated by figure 6.21 in case an error occurs and by figure 6.20 in case no error occurs.

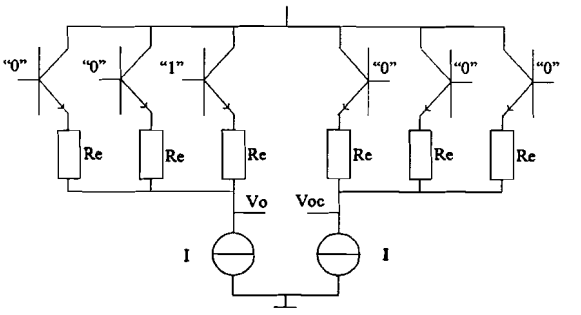


figure 6.20: No error situation

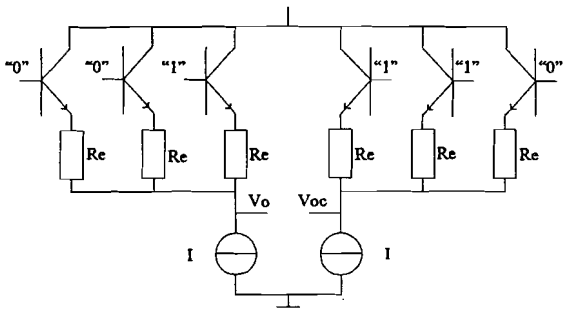


figure 6.21: Error due to MSS

In figure 6.20 and figure 6.21 emitter resistors are presented in the rom table. These resistors are used to enlarge the differential output voltage if the master-slave comparator makes a decision error. A major drawback of the emitter resistor is the fact that the differential output voltage V_{sw} will be smaller in case no error occurs. For that reason differential amplifiers are placed behind the rom table. The rom-amplifiers will be discussed in section 6.7.

A "no fault" situation of the master-slave comparator results in the following differential output voltage of the rom table:

$$V_o - V_{oc} = V_{sw} - V_T \ln(\frac{n}{2}) - R_e I(1 - \frac{2}{n}) \tag{6.9}$$

with n being the number of inputs (n = 32).

However, in case an error does occur the differential output voltage of the rom table can be described as:

$$V_o - V_{oc} = -(V_T \ln(2) + \frac{R_e I}{2}) \tag{6.10}$$

The value of the emitter resistor R_e of the rom table can be calculated for an equal differential output voltage in case a failure does occur or does not occur. This can be calculated by putting equation(6.9) on a par with equation (6.10).

6.6.3 Design

The current I of the rom table is set by simulation at a value of 32 μA. The output swing V_{sw} would have been 250 mVolt if no emitter resistor had been used. R_e can now be calculated (see section 6.6.2) resulting in R_e = 2.235 kΩ. The power dissipation of the rom table is 0.96 mWatt.

The simulation results are presented in table 6.4.

table 6.4: Simulation results of the rom table

Parameter	Value
Transistor	n10L24pm, m = 1
Power dissipation	0.96 mWatt
R_e	2.235 kΩ
t_r	0.8 ns
t_f	0.8 ns
t_d, t_s	0.1 ns

6.7 Rom-amplifiers

6.7.1 Introduction

The differential amplifier is very often used in IC-design. Such a circuit has the advantage of directly coupling two or more stages without interstage coupling capacitors. The differential input characteristic is required in many types of analog circuits. The basic form of the differential pair is shown in figure 6.22. The resistor Rcm is used for a DC-shift of the output signal. The amplifier, which is illustrated in figure 6.22, has a differential input Vi = Vin - Vinc and a differential output Vo = Vout - Voutc.

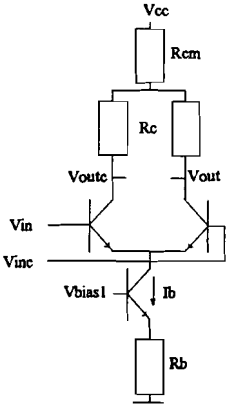


figure 6.22: Basic differential pair

The equations for the differential output and gain are:

$$V_o = I_b R_c \tanh(\frac{V_i}{2V_T})$$

$$G = g_m R_c$$

In figure 6.23 the differential output is illustrated.

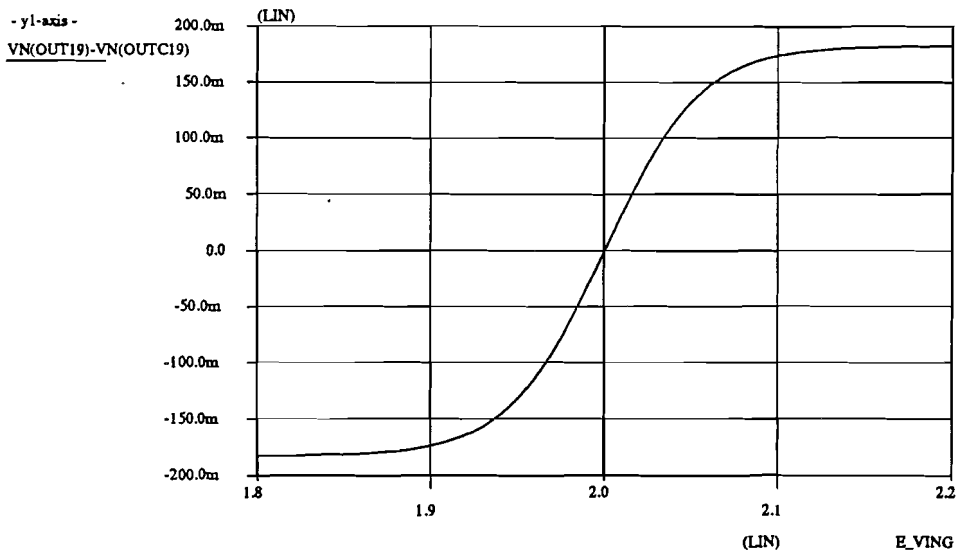


figure 6.23: Differential output

In this section the rom-amplifiers will be discussed. These amplifiers amplify the differential signal from the rom table (see figure 6.18). In section 6.7.2 the design of romamp 1 is discussed, followed by a description of romamp2 and romamp 3 in section 6.7.3 and section 6.7.4. Since the discussion for romamp 2 can also be applied to romamp3, the latter will be discussed only briefly. Designing the rom-amplifiers requires equal signal delays [10] for all five signals (see figure 6.1), which is met by equal bandwidth for the rom-amplifiers. Three rom-amplifiers are necessary because all three have different loads attached (see figure 6.1).

6.7.2 Romamp 1

The current Ib (see figure 6.22) is set by simulation at a value of 34 μA enabling a f_{3dB} bandwidth of 1.2 GHz (see figure 6.24) with the EXOR circuit attached to the romamp1. The simulation is performed with a single input signal of 1 mVolt. This bandwidth is almost equal to the f_{3dB} bandwidth of the comparators in track mode. So the signal of the rom table will not be slew-limited by the differential amplifier. A value equal to this bandwidth can be met. However, in that case the increase in power consumption will be larger than the increase in bandwidth. Therefore, one can conclude that it is useless to meet the demand of equal bandwidth in order to obtain low power design.

Figure 4.3 in chapter 4 "*THE SPIRIT PROCESS*" illustrates that the Vbe of the transistor is 0.81 Volt at a current of 34 μA. With a Vbias1 = 0.85 Volt this results in a resistor value of 1.176 kΩ for resistor Rb. The voltage over Rb is 40 mVolt. Due to the sensitivity [1] to variations of the voltage V_{bias1} a voltage of 200 mVolt - 300 mVolt would be more appropiate. However, this can not be realized, due to the maximum allowable forward voltage V_{bc} of 200 mVolt.

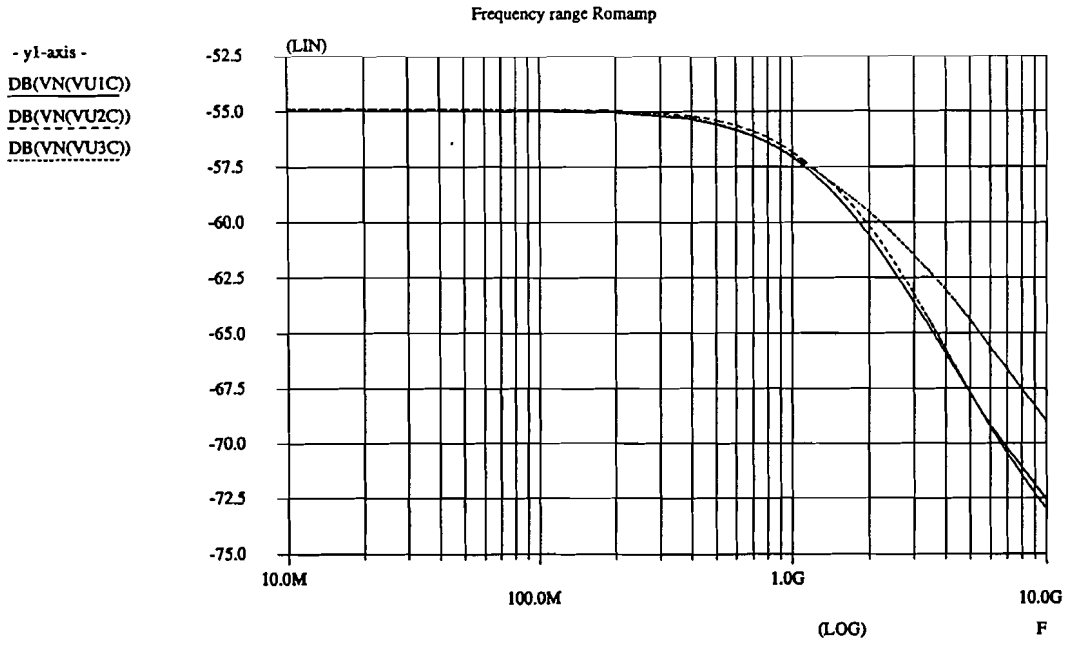


figure 6.24: Frequency range of rom-amplifiers

Resistor Rcm is used for a DC-shift of the output signal (see figure 6.22). For a DC-value at the output of 2.70 Volt a resistor Rcm = 8.8 kΩ has to be used. The resistor Rc can be calculate for a gain of 10 and an output voltage swing of 250 mVolt. Using the former equations results in Rc = 7.353 kΩ. The power consumption of this differential amplifier is 0.102 mWatt.

The parameters derived above are simulated and summarized in table 6.5.

table 6.5: Derived and simulated parameters of Romamp 1

Parameter	Value
Transistor	n10L24pm, m = 1
Bandwidth	1.2 GHz
Power consumption	0.102 mWatt
Gain	3.68
Rcm	8.8 kΩ
Rc	7.353 kΩ
Rb	1.176 kΩ
DC-output	2.70 Volt

6.7.3 Romamp 2

For romamp2 the current Ib (see figure 6.22) is set by simulation at a value of 36 μA in order to obtain a f_{-3dB} bandwidth of 1.2 GHz with the EXOR circuit and master-slave latch attached, equal to the bandwidth of romamp 1 for equal signal delay as stated in section 6.7.2. Figure 4.3 in chapter 4 "*THE SPIRIT PROCESS*" illustrates that the Vbe = 0.812 Volt of the transistor at a current of 36 μA. With a Vbias1 = 0.85 Volt this results in a resistor value of 1.028 kΩ for resistor Rb. Resistor Rcm is used for a DC-shift of the output signal. In order to obtain a DC-value at the output of 2.85 Volt a resistor Rcm = 4.17 kΩ has to be used. The resistors Rc can be calculated for a gain of 10 and an output voltage swing of 250 mVolt. Using the equations as shown before, this results in Rc = 6.944 kΩ. The power consumption of this differential amplifier is 0.108 mWatt.

The parameters derived above are simulated and summarized in table 6.6.

table 6.6 Derived and simulated parameters of Romamp 2

Parameter	Value
Transistor	n10L24pm, m = 1
Bandwidth	1.2 GHz
Power consumption	0.108 mWatt
Gain	3.68

Parameter	Value
Rcm	4.17 kΩ
Rc	6.944 kΩ
Rb	1.028 kΩ
DC-output	2.85 Volt

6.7.4 Romamp 3

Finally, for romamp3, the current Ib (see figure 6.22) is set by simulation at a value of 34 μA in order to obtain a f_{3dB} bandwidth of 1.2 GHz with the master-slave latch attached, equal to romamp 1 and romamp 2. The Vbe of the transistor is 0.81 Volt at a current of 34 μA. With a Vbias1 = 0.85 Volt Rb = 1.176 kΩ can be calculated. Resistor Rcm is used for a DC-shift of the output signal of 0.15 Volt. This results in a resistor Rcm = 4.4 kΩ. The resistors Rc can be calculated for a gain of 10 and an output voltage swing of 250 mVolt. Using again the equations as described in section 6.7.1, resistor Rc results in a value of 7.353 kΩ. The power consumption of this differential amplifier is 0.102 mWatt.

The parameters derived above are simulated and summarized in table 6.7.

table 6.7: Derived and simulated parameters of Romamp 3

Parameter	Value
Transistor	n10L24pm, m = 1
Bandwidth	1.2 GHz
Power consumption	0.102 mWatt
Gain	3.68
Rcm	4.4 kΩ
Rc	7.353 kΩ
Rb	1.176 kΩ
DC-output	2.85 Volt

6.8 EXOR LSB

6.8.1 Introduction

In the rom table (see section 6.6) error correction is implemented for the LSB bit. Therefore the LSB bit needs to be reconstructed which can be done by using the signals LSB and LSB+1 of the rom table.

Table 6.8 shows the definition of the EXOR function in terms of a truth table. Such a truth table contains a listing of all possible input signal combinations and the corresponding output signal value. Based on the truth table one can conclude that the EXOR function is true when its inputs differ in value.

table 6.8: Truth table of the EXOR function

a b	a⊕b
00	0
01	1
10	1
11	0

6.8.2 Design

The currents of the EXOR LSB circuit are set by simulation at 12 μA and 4 μA for the emitter followers (see appendix 6). Obtaining a voltage output swing of 250 mVolt results in a resistor value R_{load} of 20.888 kΩ. The resistors Rb1 and Rb2 for establishing the current sources are 6.5 kΩ and 65 kΩ. The power dissipation is 0.06 mWatt.

The results of simulating the EXOR LSB are summarized in table 6.9.

table 6.9: Simulation results of the EXOR LSB

Parameter	Value (Vin1 -> out)	Value (Vin2 -> out)
Transistor	n10L24pm, m = 1	
Power dissipation	0.06 mWatt	
t_r	1.06 ns	0.81 ns

Parameter	Value (Vin1 -> out)	Value (Vin2 -> out)
t_f	0.96 ns	0.96 ns
t_d, t_s	0.2 ns	0.11 ns
Rload	20.888 kΩ	
Rb1	6.5 kΩ	
Rb2	65 kΩ	

6.9 Latch

6.9.1 Master latch

6.9.1.1 Introduction

The master latch is presented in figure 6.25.

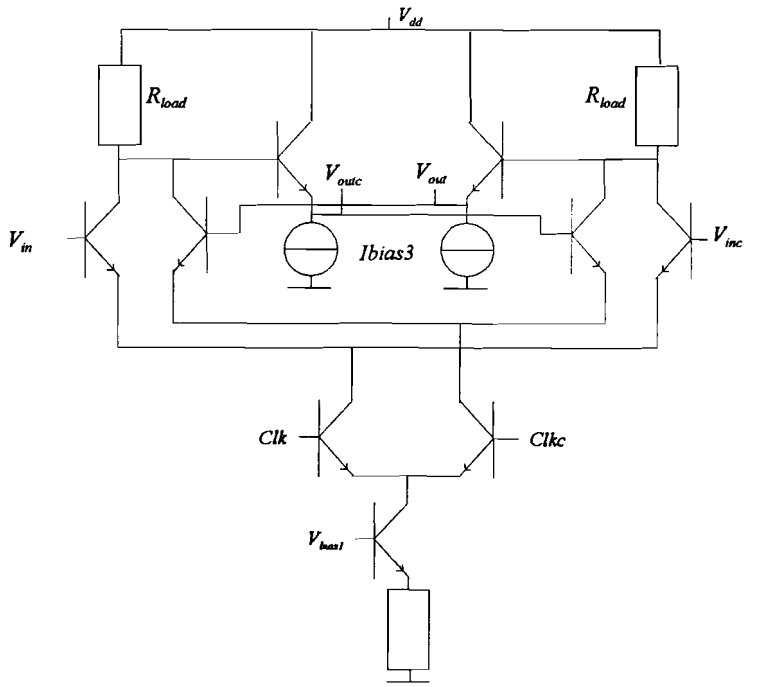


figure 6.25: Master latch

The master latch has two emitter-followers in the hold circuit which are biased by the current source Ibias3. Due to the emitter-follower the influence of the miller capacitance is reduced.

This miller capacitance has a bandwidth limiting effect on the hold circuit and subsequently a limited influence on the factor $(A_0 - 1)/\tau$.

The master latch has a differential input Vi = Vin - Vinc and a differential output Vo = Vout - Voutc. The output voltage of the master latch is 250 mVolt.

For the functioning of this circuit reference is made to section 6.4.2.1 in which the functioning of this circuit has been described.

6.9.1.2 Design

The current of the master latch is set by simulation at 18 μA whereas the current of the emitter-follower is set by simulation at 12 μA.

These current settings leads to a $(A_0 - 1)/\tau$ of 10.10^9 s^{-1} and a f_{-3dB} bandwidth of 1.56 GHz with the slave latch attached.

After setting the currents the resistor values can be calculated. These values and the simulation results are summarized in table 6.10.

table 6.10: Calculated and simulated parameters of the master latch

Parameter	Value
Transistor	n10L24pm, m = 1
Bandwidth	1.56 GHz
Power consumption	0.126 mWatt
$(A_0 - 1)/\tau$	10.10^9 s^{-1}
Rload	13.888 kΩ
Rb	5.333 kΩ
Rbias3	6.5 kΩ

6.9.2 Slave latch

The slave latch used in the ADC is equal to the slave comparator used for the Sync-MSB signal in chapter 7 "*COARSE PART*". Therefore reference is made to the next chapter for calculation and simulation results of the slave latch.

6.9.3 Master-slave latch

The master-slave latch keeps the output binary code valid for one clock period. It is constructed by interconnecting the circuits shown in figure 6.25 and figure 7.2. The total power dissipation of the master-slave latch is 0.18 mWatt.

In the fine part a 5 bit binary output code is generated which results in a power dissipation of 0.9 mWatt.

6.10 Total fine part

The fine part has been described in this chapter. In this section some overall specifications will be listed. The total power dissipation of the total fine part is 9.91 mWatt. The power dissipation of the divers circuits are listed in table 6.11.

table 6.11: Total power dissipation of the fine part

Circuit	Power dissipation
Master-slave comparator	5.216 mWatt
wired-EXOR	2.3 mWatt
Rom table	0.96 mWatt
Rom-amplifier	0.52 mWatt
Master-slave latch	0.9 mWatt
Total	9.91 mWatt

The total fine part has been simulated to determine information about the maximum clock frequency which can be applied to the fine part. This information is obtained by deriving the delay of the fine part meaning the delay between a code transition at the slave comparator and the corresponding code transition at the input of the master latch. The total delay is 2.3 ns, corresponding with a maximum clock frequency of 217 MHz.

Furthermore, the fine part has been simulated in order to obtain information about the output codes. These simulation results are presented in appendix 5.

CHAPTER 7 COARSE PART

7.1 Introduction

In this chapter the coarse part of the Analog to Digital Convertor is discussed. The coarse part of the ADC is illustrated in figure 7.1 and embraces the following parts:

- comparator;
- EXOR;
- bitsync;
- overflow;
- latches;
- differential amplifier;
- buffer.

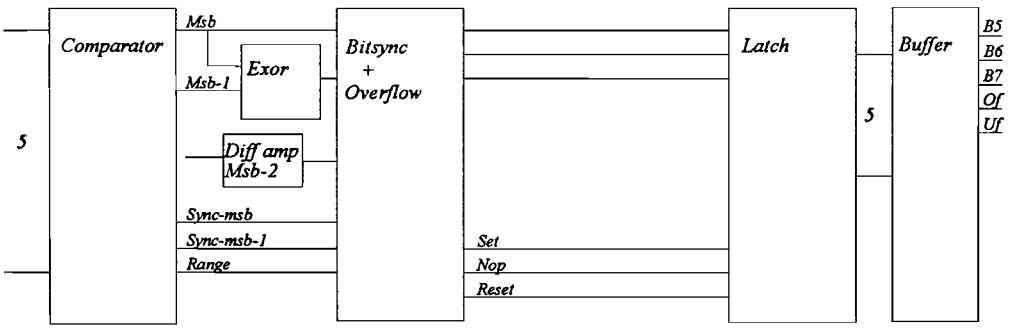


figure 7.1: Coarse part of the Analog to Digital Convertor

The comparator block is used in order to digitalize the coarse folding signals of the preprocessing part. The EXOR block is used for reconstructing the MSB-1 from the signals MSB and MSB-1 necessary for the bitsync block. Furthermore, the bitsync block is used to synchronize the coarse part of the ADC with the fine part which is obtained by deriving the MSB-2 signal of the fine part. The overflow block is used to set and reset the output latches in case the input signal exceeds its input range. Finally, the latch block is used in order to enable the binary output code and the overflow and underflow signals at the same time at the output.

The buffer will be discussed in chapter 8 "*THE TOTAL ANALOG TO DIGITAL CONVERTOR*". The bitsync, overflow and differential amplifier will be discussed in this chapter. The remaining circuits mentioned above will be discussed in section 7.2. Section 7.3 will discuss the differential amplifier. In section 7.4 the bitsync circuit will be described. Finally, the overflow circuit will be discussed in section 7.5.

7.2 Comparator, Latch and EXOR

7.2.1 Introduction

In this section the comparator, latch and EXOR circuit of the coarse part will be discussed. In section 7.2.2 the comparator will be described. Section 7.2.3 will discuss the latch and finally, in section 7.2.3, the EXOR function will be discussed.

7.2.2 Comparator

7.2.2.1 Introduction

The comparator used in the coarse part of the ADC is of the master-slave type. By using this comparator a reduction of the failure rate can be obtained (see [10, 14]). The master comparator digitalizes the folding signals of the coarse part of the preprocessing block.

In this section 7.2.2 the master-slave comparator will be discussed. In section 7.2.2.2 the master comparator will be described whereas in section 7.2.2.3 the slave comparator will be discussed. Finally, the total master-slave comparator will be presented and discussed in section 7.2.3.

7.2.2.2 Master comparator

The master comparator is equal to the master comparator of the fine part (see chapter 6 "*FINE PART*"). Therefore only the calculation and simulation results are presented in this context (see table 7.1):

table 7.1: Calculation and simulation parameters of the master comparator

Parameter	Value differential amplifier	Value comparator
Transistor	n10L24pm, m = 1	
Bandwidth	1.04 GHz	1.45 GHz

Parameter	Value differential amplifier	Value comparator
Power consumption	0.109 mWatt	
$(A_0 - 1)/\tau$		$9.10^9 s^{-1}$
Rcm		59.375 kΩ
Rc		31.25 kΩ
R1	6.25 kΩ	
R2	13.888 kΩ	
Rbias	11.25 kΩ	6.416 kΩ / 11.25 kΩ
DC-output	2.4 Volt	2.115 Volt

7.2.2.3 Slave comparator

7.2.2.3.1 Introduction

The slave comparator is presented in figure 7.2.

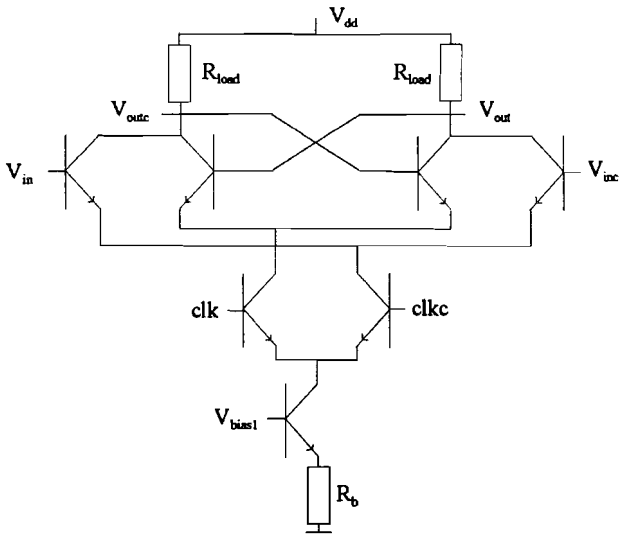


figure 7.2: Slave comparator

The circuit in figure 7.2 is the most simple and basic comparator that can be found. The functioning of the slave comparator has already been described in section 6.4.2.1. The slave comparator has a differential input Vi = Vin - Vinc and a differential output Vo = Vout - Voutc. The input and output voltages of the slave comparator are differential signals with an amplitude of 250 mVolt.

In the next section, section 7.2.2.3.2, the design of the slave comparator will be described.

7.2.2.3.2 Design

The current in the current source is set by simulation at 18 μA. Based on the value of the current and using figure 4.3 in chapter 4 "*THE SPIRIT PROCESS*" the resistor value Rb being 3.555 kΩ can be calculated. For a voltage swing of 250 mVolt the resistor Rload is 13.888 kΩ.

The power consumption of the slave comparator is 0.054 mWatt.

The simulations of the slave comparator have already been described in section 6.3.5 with the factor $(A_0 - 1)/\tau = 6.10^9\ s^{-1}$ and the f_{-3dB} bandwidth being 1.2 GHz.

The slave comparator, which has been described before, will be used for the synchronization signal for the MSB bit: Sync-MSB-1 (see figure 7.2). For the other signals MSB, MSB-1, Sync-MSB-1 and Range an additional common mode resistor Rcm is used for a DC-shift of 250 mVolt placed in the supply lead of figure 7.2. The value of Rcm is 13.888 kΩ.

The simulation results of the slave comparator are presented in table 7.2. In table 7.2 the resistor values are also summarized.

table 7.2: Calculation and simulation results of the slave comparator

Parameter	Value Sync-MSB-1	Value
Transistor	n10L24pm, m = 1	
Bandwidth	1.2 GHz	
Power consumption	0.054 mWatt	
$(A_0 - 1)/\tau$	$6.10^9\ s^{-1}$	
Rcm		13.888 kΩ
Rload	13.888 kΩ	
Rb	3.555 kΩ	

7.2.2.4 Master-slave comparator

The master-slave comparator digitalizes the signals of the coarse part of the preprocessing block [1]. The master-slave comparator is constructed by interconnecting the circuits presented in figure 6.14 and figure 7.2.

The power dissipation of the master-slave comparator is 0.163 mWatt, resulting in a total power dissipation (see figure 7.2) of 0.82 mWatt for the 3 bit binary output code including the overflow and underflow signals of the coarse part.

7.2.3 Master-Slave Latch

The master-slave latch used in the coarse part is equal to the master-slave latch used in the fine part. Therefore reference is made to chapter 6, section 6.9 in which the simulation results of the master-slave latch have been described. The total power dissipation of the master-slave latch is 0.9 mWatt.

7.2.4 EXOR MSB-1

7.2.4.1 Introduction

The bitsync circuit needs a MSB-1 signal shown in figure 7.3.

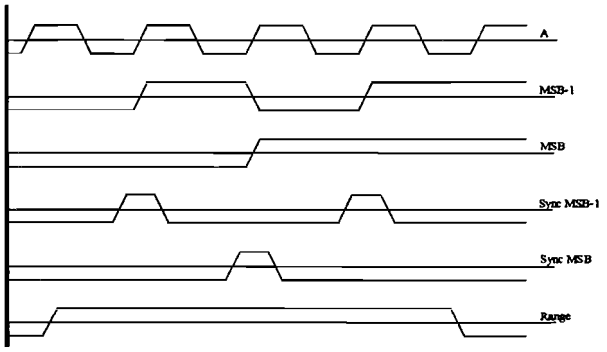


figure 7.3: Needed MSB-1 signal

However, the signal shown in figure 7.4 is generated by the preprocessing part [1].

This signal generation is chosen because as soon as a MSB code transition occurs, MSB-1 also has a code transition, being a heavy load on the preprocessing part. This is solved by generating a MSB-1 signal (see figure 7.4).

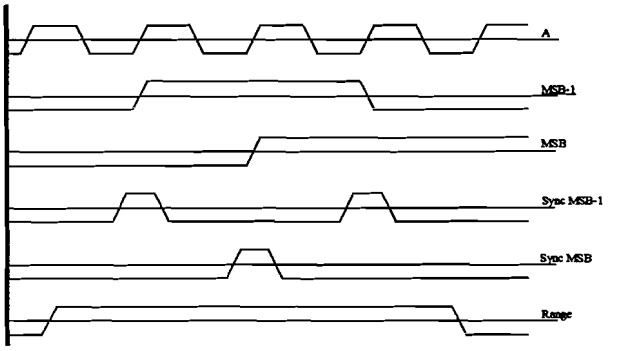


figure 7.4: Generated MSB-1 signal

Having a MSB-1 signal as illustrated in figure 7.4 implies the need to reconstruct the original MSB-1 signal necessary for the bitsync circuit. This can be realized by using the EXOR function on the signals MSB and MSB-1. So after all, the desired MSB-1 signal can be obtained.

The truth table of the EXOR function has already been presented in table 6.8.

7.2.4.2 Design

The design of the EXOR MSB-1 is described in chapter 6, section 6.8. This section also presents the corresponding simulation results (see table 6.10).

7.3 Differential amplifier for MSB-2 signal

7.3.1 Introduction

The differential amplifier for amplifying and inverting the MSB-2 signal is presented in figure 7.5. This amplifier has a differential input Vi = Vin - Vinc and a differential output Vo = Vout - Voutc. Considering the fact that the input signal is already a differential signal of 250 mVolt originated from the fine part, emitter degeneration is used in order to decrease the gain of this stage. The emitter resistor introduces local feedback and subsequently enlarges the linear range of the differential amplifier.

The equations for the differential output and gain are:

$$V_o = I_b R_c \tanh\left(\frac{V_i - \frac{R_E}{R_c} V_o}{2V_T}\right)$$

$$G = \frac{I_b R_c}{2V_T + I_b R_E} \approx \frac{R_c}{R_E} \quad if\ 2V_T \ll I_b R_E$$

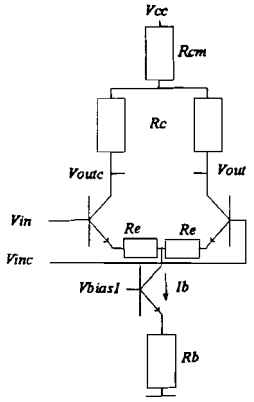


figure 7.5: Differential amplifier with emitter degeneration

7.3.2 Design

The current Ib is set by simulation at a value of 34 μA in order to obtain a f_{-3dB} bandwidth of 1.4 GHz with the bitsync and overflow circuit attached to the differential amplifier. This bandwidth is almost equal to the f_{-3dB} bandwidth of the comparators in track mode.

So the signal from the fine part will not be slew-limited by the differential amplifier. A value equal to this bandwidth can be met. However, in that case the increase in power consumption will be larger than the increase in bandwidth. Therefore, one can conclude that it is useless to meet the demand of equal bandwidth in order to obtain low power design. Using figure 4.3 in chapter 4 "*THE SPIRIT PROCESS*", one can see that the Vbe of the transistor is 0.81 Volt at a current of 34 μA. With a Vbias1 = 0.85 Volt this results in a resistor value of 1.176 kΩ for resistor Rb. Resistor Rcm is used for a DC-shift of the output signal. In order to obtain a DC-value at the output of 2.47 Volt a resistor Rcm of 11.765 kΩ has to be used. The resistors Rc and R_E can also be calculated for a gain of 1.5 and an output voltage swing of 250 mVolt.

Using the equations shown before, this results in Rc = 7.353 kΩ and R_E = 2/3*Rc = 4.9 kΩ.

The power consumption of this differential amplifier is 0.102 mWatt.

The parameters derived above have been simulated, the corresponding results being listed in table 7.3.

table 7.3: Derived and simulated parameters of Diff amp MSB-2

Parameter	Value
Transistor	n10L24pm, m = 1
Bandwidth	1.4 GHz
Power consumption	0.102 mWatt
Gain	1.48
Rcm	11.765 kΩ
Rc	7.353 kΩ
R_E	4.9 kΩ
Rb	1.176 kΩ
DC-output	2.47 Volt

7.4 Bitsync

7.4.1 Introduction

The main purpose of the bitsync is to synchronize the coarse part of the Analog to Digital Convertor with the fine part. This goal can be reached by deriving the MSB-2 signal of the fine part of the ADC. In this way the signals of the coarse part, the MSB and MSB-1 signal of the ADC, can be synchronized with the fine part. For synchronization the signals sMSB and sMSB-1, which represent the synchronizing signals of the MSB and MSB-1 signals, are also being used. The signals mentioned before are all differential signals. Hence, only one signal is illustrated in figure 7.6.

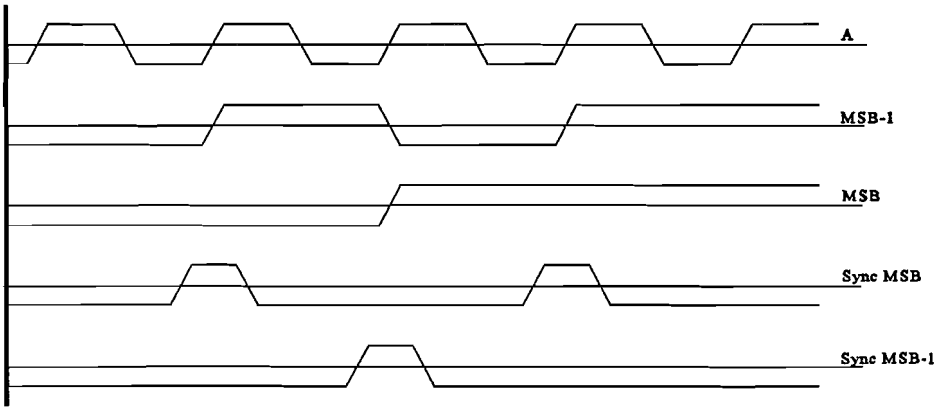


figure 7.6: Input signals bitsync circuit

Figure 7.6 illustrates the possibility to synchronize the MSB signal by combining sMSB and A. If the sMSB signal is "0" the MSB signal originated from the comparator will be used. Combining the signals can be illustrated in the following digital circuit (see figure 7.7):

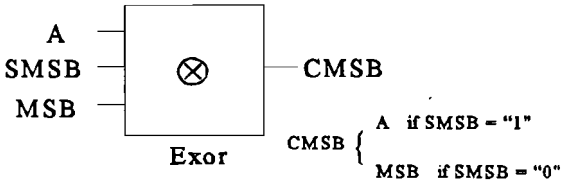
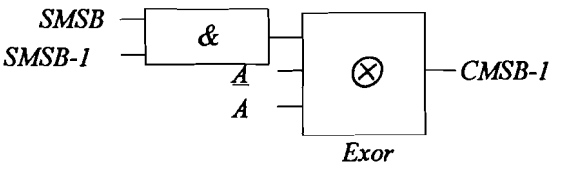


figure 7.7: Synchronization circuit MSB

The MSB-1 signal can be synchronized with the MSB-2 signal by using the following digital circuit (figure 7.8).



$$CMSB\text{-}1 \begin{cases} A & \text{if } SMSB\text{-}1 = \text{"}1\text{"} \\ \underline{A} & \text{if } SMSB = \text{"}1\text{"} \\ MSB\text{-}1 & \text{if } \underline{SMSB}*\underline{SMSB\text{-}1} = \text{"}1\text{"} \end{cases}$$

figure 7.8: Synchronization circuit MSB-1

The AND circuit used in the synchronization circuit for the MSB-1 signal has the following functionality:

sMSB sMSB-1	AND-out
0 0	1
0 1	0
1 0	0
1 1	0

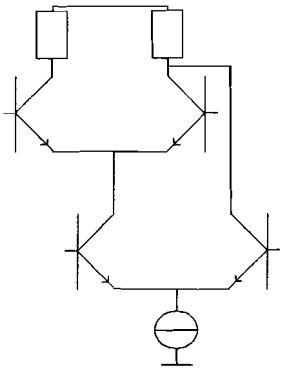


figure 7.9: Functionality description of the AND circuit

7.4.2 Design

Considering the fact that the design of the bitsync is considered to be very comprehensive, it will not be discussed in this section. Therefore, only the simulation results of the bitsync will be presented here (see table 7.4 for the MSB signal and table 7.5 for the MSB-1 signal). The output voltage swing is 250 mVolt. Additional resistors have been added in order to obtain the DC-shift of 0.275 Volt, resulting in a DC-output voltage of 2.725 Volt. The power dissipation of the bitsync is 0.47 mWatt.

table 7.4: Simulation results of the bitsync for the MSB signal

Parameter	Value for SMSB = "1"
t_r	1.15 ns

Parameter	Value for SMSB = "1"
t_f	1.0 ns
td, ts	0.3 ns

table 7.5: Simulation results of the bitsync for the MSB-1 signal

Parameter	Value for SMSB = "1"	Value for SMSB-1 = "1"
t_r	1.2 ns	1.2 ns
t_f	1.14 ns	1.14 ns
td, ts	0.29 ns	0.29 ns

7.5 Overflow

7.5.1 Introduction

The main purpose of the overflow circuit is to set and reset the output latches in case the input signal exceeds its range. Hence, if the input signal for instance drops below the input range, the output of the ADC will become 00000000. However, if the inputsignal for instance exceeds the input range the output of the ADC will become 11111111.

The range of the convertor is defined by the range signal illustrated in figure 7.10. This figure also illustrates the MSB signal, which points out whether an overflow or underflow occurs. Furthermore, synchronization with the fine part of the ADC is necessary. Therefore signal A is being used. The signals mentioned above are all illustrated in figure 7.10.

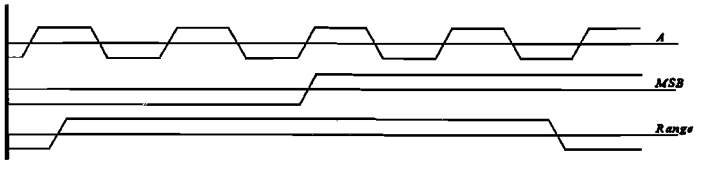


figure 7.10: Input signals overflow circuit

Based on figure 7.10 one can conclude that an underflow will occur if A, MSB and Range are "0" whereas an overflow will occur if A and MSB are "1" and Range is "0". This leads to the following equations:

$$RESET = \overline{A * MSB * Range}$$

$$SET = A * MSB * \overline{Range}$$

Both equations can be realized with a digital AND function. This leads to figure 7.11.
Nop will normaly be "1" if there is no underflow or overflow (i.e. under normal operation conditions).

The three signals Set, Nop and Reset are supplied to the output latches. Based on these signals the signals Of and Uf, shown in figure 7.1, can also be derived by supplying them to the two output latches by using differential amplifiers.

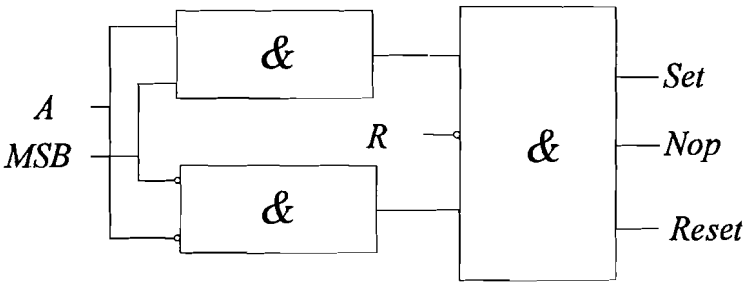


figure 7.11: Digital block representation of the overflow circuit

7.5.2 Design

In addition to the design of the bitsync (see section 7.4.2) the design of the overflow circuit is also considered to be a very comprehensive one. Therefore, once again, only the simulation results will be discussed in this section (see table 7.6). The output voltage swing is 250 mVolt whereas the power dissipation of the overflow circuit is 0.88 mWatt.

table 7.6: Simulation results of the overflow circuit

Parameter	Value for NOP -> SET	Value for NOP -> RESET
t_r	1.95 ns	1.94 ns
t_f	1.70 ns	1.69 ns
td, ts	0.50 ns	0.50 ns

7.6 Total coarse part

The course part has been described in this chapter. The total power dissipation of the total course part is 3.17 mWatt. The total power dissipation of the divers circuits are listed in table 7.7.

table 7.7: Total power dissipation of the coarse part

Circuit	Power dissipation
Master-slave comparator	0.82 mWatt
Bitsync	0.47 mWatt
Overflow	0.88 mWatt
Diff MSB-2	0.102 mWatt
Master-slave latch	0.9 mWatt
Total	3.17 mWatt

CHAPTER 8 THE TOTAL ANALOG TO DIGITAL CONVERTOR

8.1 Introduction

The Analog to Digital Convertor is presented in figure 8.1.

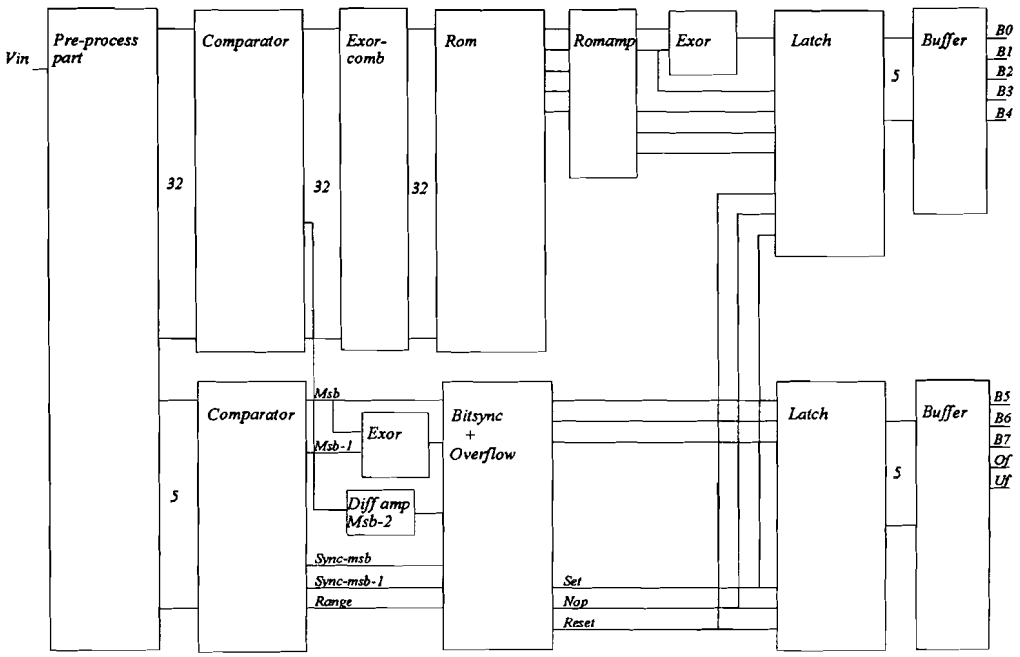


figure 8.1: Total ADC

This figure illustrates the following parts:

- Preprocessing block, designed by [1]. The results of this design are summarized in section 5.2 of chapter 5 "*FOLDING AND INTERPOLATION PRINCIPLE*".
- Fine part, discussed in chapter 6 "*FINE PART*".
- Coarse part, discussed in chapter 7 "*COARSE PART*".

The total power dissipation of the ADC is presented in table 8.1.

table 8.1: Total power dissipation

Part	Power dissipation
Preprocessing	5950.55 μWatt
Fine	9.91 mWatt
Coarse	3.17 mWatt
Total power dissipation ADC	19.03 mWatt

After designing the total Analog to Digital Convertor one has to check whether the initial design specifications presented in chapter 3 "*INITIAL DESIGN SPECIFICATIONS*" have been met. Considering these specifications one can conclude that they have been met adequately (see section 5.3) except for the power dissipation (see table 8.1).

8.2 Buffer

8.2.1 Introduction

The output buffer (see figure 8.2) is placed behind the master-slave latch and has a cmos compatible output voltage which is defined as Vdd for the "high" output level and Vdd - IR_{load} for the "low" output level. A major disadvantage of this output buffer is the need for a constant current, which follows from Vdd - IR, in order to obtain the "low" output level. The Analog to Digital Convertor is supplied with a voltage Vdd of 3 Volts which results in an output voltage of 3 Volt for the "high" output level and 0.6 Volt for the "low" output level.

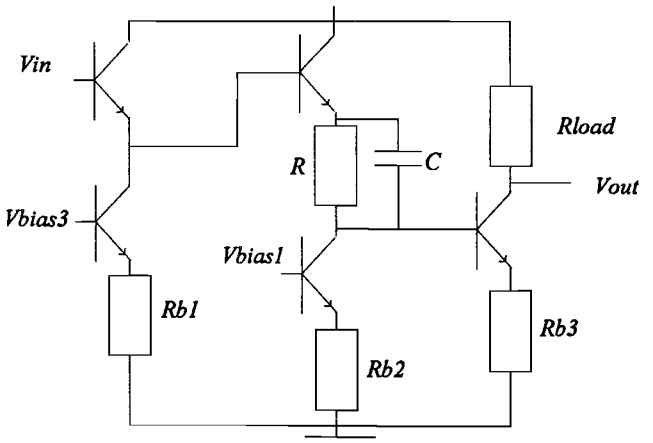


figure 8.2: The output buffer

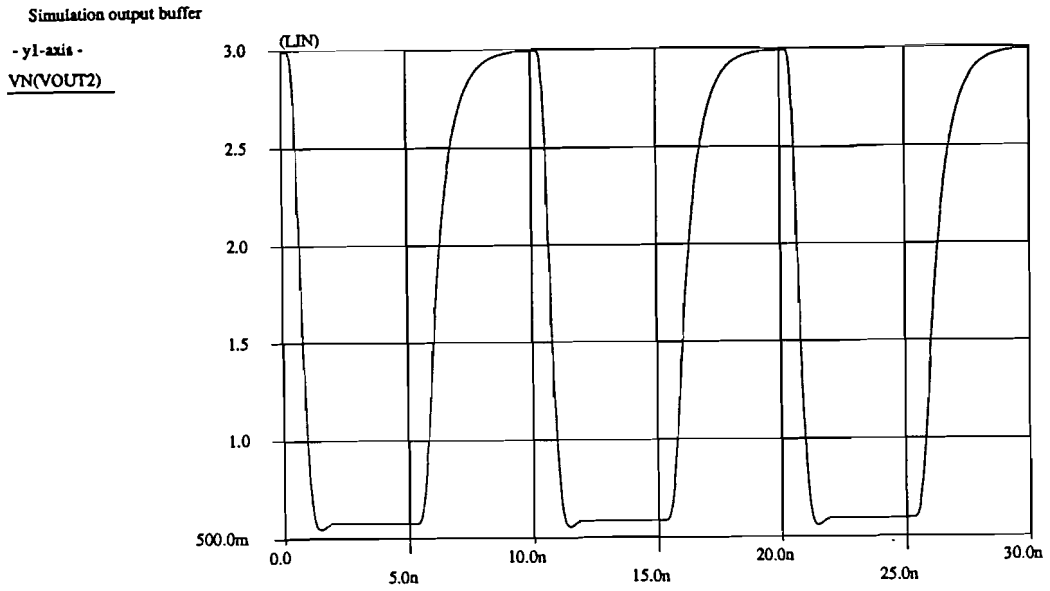


figure 8.3: Output voltage swing of the output buffer

Frequency compensation (lead compensation) has been used to improve the transient response of the output buffer. The circuit presented in figure 8.2 is diverted of a Fairchild μA702 op-amp.

The main design specification which has to be met is the following: the output buffer has to have a t_r and t_f of 2 ns at a capacitive load of 5 pF.

8.2.2 Design

In order to meet the requirement of a t_r and t_f of 2 ns at a capacitive load of 5 pF at the output, the resistor has to have a value of 115 Ω. This value has been obtained by simulation by switching on and off a current source parallelled to the RC network. From this value of the resistor the current necessary for obtaining a "low" output level of 0.6 Volt can be calculated. The current needed is 20.8 mA, which implies that 500 transistors have to be parallelled since the maximum current of one transistor is approximately 40 μA.

The other stages that drive the common-emitter amplifier have been designed to maintain the specification, mentioned above, which has resulted in the following values of the parts of the output buffer (see table 8.2):

table 8.2: List of parts of the output buffer

Part	Value
Rload	115 Ω
R	240 Ω
C	75 pF
Rb1	14.775 kΩ
Rb2	16 Ω
Rb3	2.95 Ω
Power dissipation	68.64 mWatt

CHAPTER 9 LAY-OUT

9.1 Introduction

In this chapter the layout of the Analog to Digital Convertor is described. In section 9.2 the metal layers which can be used in this context will be discussed. Section 9.3 will describe the interconnection capacitances. Finally, section 9.4 will present the dimensions of the designed circuits.

9.2 Metal layers

The ADC will be implemented in the SPIRIT process which uses one metal layer IN for the lay-out and the interconnection of the circuits. The width of metal IN is 1.5 μm whereas the height of metal IN is 0.5μm. Due to the dimensions of metal layer IN the sheet resistance $R_{\square}$ = 60.6 mΩ per square ($\rho = 3.03\ 10^{-2}\ \Omega$ μm for a AlTiW alloy) can be calculated. A second metal layer INS can be used which has a width of 3 μm. The height of metal INS is also 3 μm which leads to the sheet resistance $R_{\square}$ = 9.0 mΩ per square ($\rho = 2.7\ 10^{-2}\ \Omega$ μm for a Al). A major disadvantage of using this metal layer is the design rule which states, that the spacing of INS to INS has to be at least 9 μm. The interconnection between IN and INS is obtained by using vias which have a dimension of 9 μm * 9 μm.

9.3 Interconnection capacitances

The interconnection capacitance from metal IN to ground is between 35 aF/μm and 50 aF/μm.

The interconnection capacitance between metal IN and metal IN is measured for different width w1 and w2 of the wires and different spaces w1,2 between the wires. The measured capacitances are listed in table 9.1.

table 9.1: Interconnection capacitances between metal IN and metal IN

w1 (μm)	w2 (μm)	w1,2 (μm)	Capacitance (aF/μm)
1.0	1.0	1.0	80
1.0	1.0	4.0	36
1.0	1.0	10.0	23
1.0	49.0	1.0	96
1.0	49.0	4.0	50

w1 (µm)	w2 (µm)	w1,2 (µm)	Capacitance (aF/µm)
1.0	49.0	10.0	36
1.0	49.0	20.0	29

The interconnection capacitance between metal IN (width w1) and metal INS (widht w2) is also measured. The measured capacitances are listed in table 9.2.

table 9.2: Interconnect capacitances between metal IN and metal INS

w1 (µm)	w2 (µm)	w1,2 (µm)	Capacitance (aF/µm)
15	15	5	68
1.5	15	5	46

In case of a crossing between metal IN and metal INS in the lay-out, an additional capacitance will occur. This capacitance can be calculated as:

$$C = \epsilon_0 \epsilon_r \frac{A}{d} \quad with \ \epsilon_0 = 8.85 * 10^{-11}$$

resulting in C = 0.45 fF. The dielectric constant ϵ_r for Silicium oxide is 3.9.

9.4 Lay-out realization

The lay-out realization starts by searching for a compact lay-out for the slave comparator as described in chapter 7, section 7.2.2.3 (see appendix 6). The transistors which create the sample and hold circuit have been placed closely together. In this way no additional interconnection capacitances, which would have a major impact on the factor $(A_0 - 1)/\tau$ of the slave latch, can be added to the sample and hold circuit. This compact lay-out is used to design all circuits illustrated in appendix 6.

The lay-out of the circuits is realized in such a way that stacking equal circuits automatically leads to the connection of Vdd, Vss and the biasing voltages. The former leads to the most compact lay-out. Taking into account the sheet resistance of the metal layers (see section 9.2), the width of the metal layers is adapted to the current through the metal layer. Free space in the lay-out is being used for placing decoupling capacitors for Vdd.

Due to the design rules for vias and metal layer INS crossings of metal layer IN (see appendix 6) are made by using low ohmic resistors [1].

The lay-out realization of the divers circuits is presented in appendix 6. The total chip area of the Analog to Digital Convertor is 4 mm * 4 mm.

The floorplan of the ADC is presented in figure 9.1.

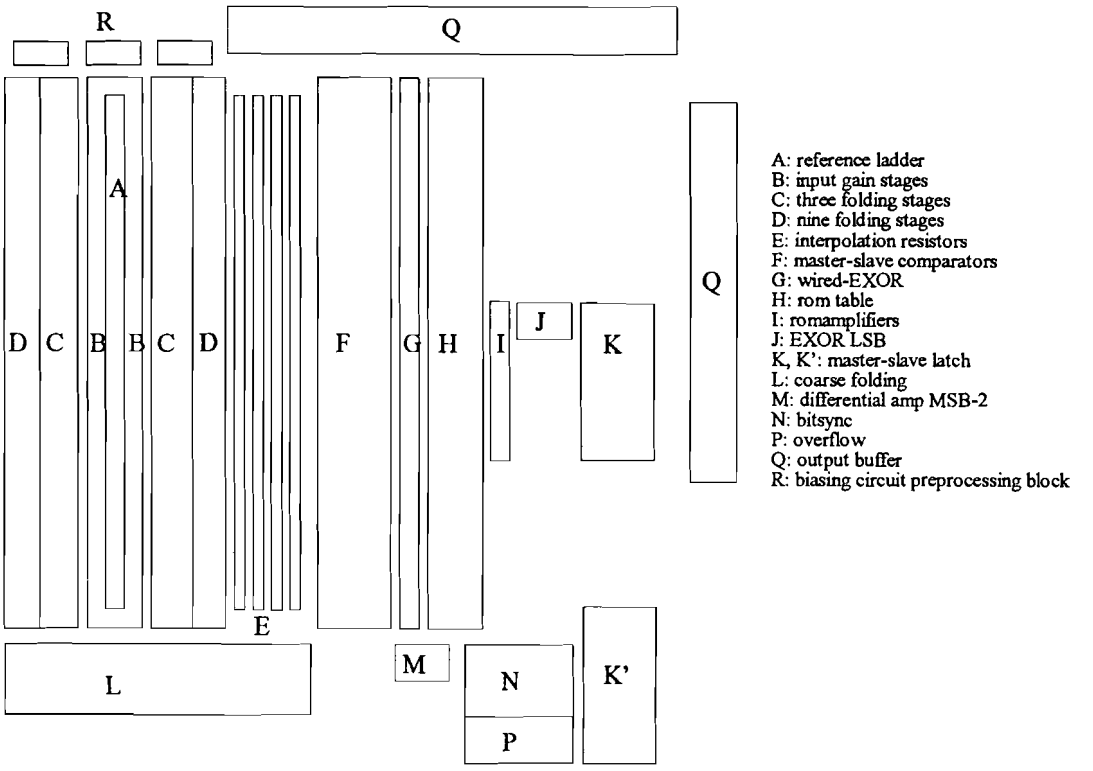


figure 9.1: Floorplan of the Analog to Digital Convertor

CHAPTER 10 CONCLUSIONS AND RECOMMENDATIONS

The preprocessing part has been designed by [1]. A summary of the simulated specifications of the preprocessing part is presented in table 10.1.

table 10.1: Simulated specifications of the preprocessing part

Preprocessing part of the ADC	
System architecture ADC	Cascaded folding with 8 times interpolation
Resolution	8 bit
Input voltage range	8/9 Volt
Bandwidth preprocessing part	500 MHz
Maximum analog input signal frequency	50 MHz
Maximum gain at zero-crossings	8
Maximum output voltage swing	400 mVolt
INL	$< \pm 0.3$ LSB
Max. distortion component at f = 50 MHz	- 55 dB

The power dissipation of the total Analog to Digital Convertor is presented in table 10.2.

table 10.2: Power dissipation of the ADC

Part	Power dissipation
Preprocessing	5950.55 µWatt
Fine	9.91 mWatt
Coarse	3.17 mWatt
Total power dissipation ADC	19.03 mWatt

After presenting the simulated results of the ADC one can conclude that the design specifications have been met adequately except for the power dissipation which is a factor 2 to 3 higher than the initial design specifications presented in chapter 3 "*INITIAL DESIGN SPECIFICATIONS*".

The clock feedthrough noise of the master comparator has been analysed by charge control. By using the charge control model the resistor value of the interpolation network can be obtained which is an optimum between clock feedthrough noise and power dissipation of the nine fold block [1]. Using this analysis one can conclude that clock feedthrough noise leads to less errors in the ADC and therefore has less influence on the degradation of the resolution of the convertor.

The fine part has been simulated in order to obtain information about the output codes. Based on the results (presented in appendix 5) one can conclude that the fine part generates the correct output codes for a ramp signal at the input of the ADC.

The lay-out realization has started by searching for a compact lay-out for the slave comparator. The transistors which create the sample and hold circuit have been placed closely together to prevent additional interconnection capacitance being added. The former leads to the conclusion that the failure rate does not increase.

The total chip area of the Analog to Digital Convertor is 4 mm * 4 mm due to the limited numbers of metal layers that could be used and the design rules of these metal layers. By adding an additional metal layer to the present metal layers, with the design rules equal to IN, the total chip area of the ADC could be reduced. Therefore adding at least one additional metal layer to the current metal layers is strongly recommended.

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APPENDICES

Appendix 1 BIPOLAR TRANSISTOR FORMULAS

Formulas which belong to the small-signal representation of a transistor (see figure 1).

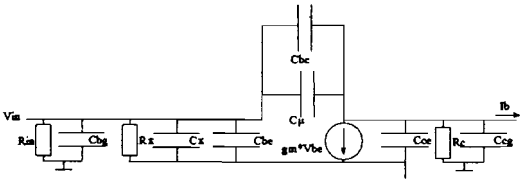


figure 1: Small-signal equivalent circuit

The transconductance is defined as:

$$g_m = \frac{\partial I_c}{\partial V_{be}} = \frac{qI_c}{kT}$$

The small-signal input resistance is given by:

$$R_\pi = \frac{\beta}{g_m}$$

The capacitance C_π contains the base-charging capacitance Cb and the emitter-base depletion layer capacitance Cje. C_π is given as:

$$C_\pi = C_b + C_{je}$$

with Cb:

$$C_b = \tau_F * g_m$$

and Cje:

$$C_{je} = \frac{C_{je0}}{\sqrt{(1 - \frac{V_{be}}{\psi_0})}}$$

The collector-base capacitance for small bias voltages is given by:

$$C_{\mu} = \frac{C_{\mu_0}}{\sqrt{(1 + \frac{V_{bc}}{\psi_0})}}$$

The transition frequency can be defined as the frequency at which the current gain of the transistor becomes 1. The transition frequency can be presented as:

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_{\pi} + C_{\mu}}$$

Appendix 2 NOISE IN BIPOLAR TRANSISTORS

1 Introduction

This appendix deals with noise in bipolar transistors. Noise is a phenomenon that coheres with spontanious random fluctuation in the small currents and voltages in the transistor [1, 2].

In section 2 I shall describe some sources of noise which occure in bipolar transistor. After that I shall present. In section 3 the small-signal circuit of the bipolar transistor with the noise sources of section 2 will be presented.

2 Sources of noise

2.1 Thermal noise

Thermal noise is due to the random thermal motion of electrons. The equation for thermal noise for a resistor can be derived by using the Langevin methode [5]. This equation is:

$$S_V = 4kTR \tag{1}$$

The former equation (1) shows that thermal noise is directly proportional to the temperature T. This indicates that thermal noise will approach zero as T approuches zero.

Equation (1) can also be written as a rms noise voltage, resulting in equation (2).

$$\overline{v^2} = 4kTR\Delta f$$

Equation (1) is valid as long as the electron drift velocity, due to a electrical field (voltage devided by the lenght of the resistor) applied to the resistor, is smaller than the thermal velocity of the electrons, presented as:

$$v_{th} = \sqrt{\frac{kT}{m}}$$

2.2 Shot noise

Shot noise is associated with a direct-current flow as in a vacuum diode. One can derive the equation for shot noise by looking at electrons traveling from cathode to anode with a constant velocity due to the applied field. The electrons start stochasticaly in time at the cathode. By applying the Carson-Campbell theorem [5] one can derive the following equation:

$$\overline{i^2} = 2qI\Delta f$$

2.3 Flicker noise

This type of noise is found in several active devices as well as in metals. The origin of flicker noise can be ascribed to fluctuations in the mobility of carriers, according to the Hooge-model [5]. The equation for flicker noise is:

$$\overline{i^2} = \frac{\alpha}{fN}\Delta f$$

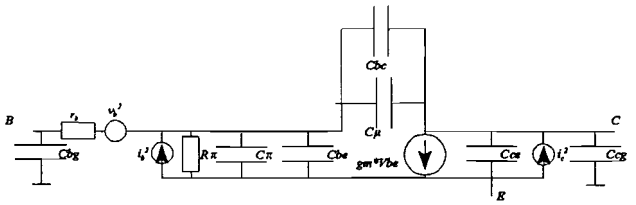
with $\alpha \approx$ 1e-3 and N the total number of carriers.

3 Small-signal circuit with noise sources

A bipolar transistor in the forward-active region can be modelled as illustrated in figure 2. This figure shows the small-signal equivalent circuit including the noise sources. In such a transistor the electrons diffuse from the emitter into the base region and drift across the base region to the collector-base junction. There they are swept across the collector-base depletion region by the existing local field. The moment of arrival of the electrons is a purely random process and thereforee afflicted with shot noise. The shot noise is modelled as source i_c^2 in figure 2.

Transistor base resistor r_b has thermal noise because it is a physical resistor. This noise source is shown in figure 2 as source v_b^2. The resistor R_π has no thermal noise because it is no physical resistor but only used for modelling purposes.

Current I_b is due to recombination in the base and in the base-emitter depletion region. I_b is also due to carrier injection from the base into the emitter. These are all random processes and thereforee afflicted with shot noise. The base current is also afflicted with flicker noise, found experimentally. These two sources of noise are combined in the source i_b^2 in figure 2.



$$v_b^2 = 4kTr_b \Delta f$$

$$i_c^2 = 2qI_c \Delta f$$

$$i_b^2 = 2qI_c \Delta f + \alpha\Delta f/fN$$

figure 2: Small-signal equivalent circuit including noise sources

Appendix 3 SMALL-SIGNAL ANALYSIS OF A COMPARATOR

The small-signal circuit of a comparator is shown in figure 3.

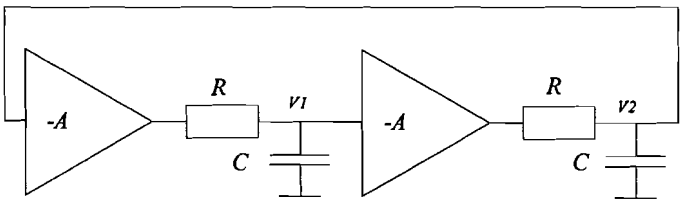


figure 3: Small-signal model of a comparator

If the feedback theory is used, the meta-stable condition can be determined. Applying the feedback theory results in:

$$1 - A^2 = 0 \tag{1}$$

with

$$A = \frac{A_0}{1 + s\tau}$$

Substituting A, as presented in the former equation, into equation (1), results in:

$$\frac{A_0^2}{1 + 2s\tau + s^2\tau^2} = 1 \tag{2}$$

Equation (2) can be rewritten as:

$$s^2\tau^2 + 2s\tau - (A_0^2 - 1) = 0 \tag{3}$$

For solving equation (3) equation (3) is written as a differential equation by replacing s by d/dt.

Equation (4) then results in:

$$\frac{d}{dt}\tau^2 + 2\frac{d}{dt}\tau - (A_0^2 - 1) = 0 \tag{4}$$

Substituting $v = \exp(\lambda t)$ in equation (4) results in:

$$\lambda_{1,2} = \frac{-1 \pm A_0}{\tau}$$

Finally, the solutions of the differential equations are:

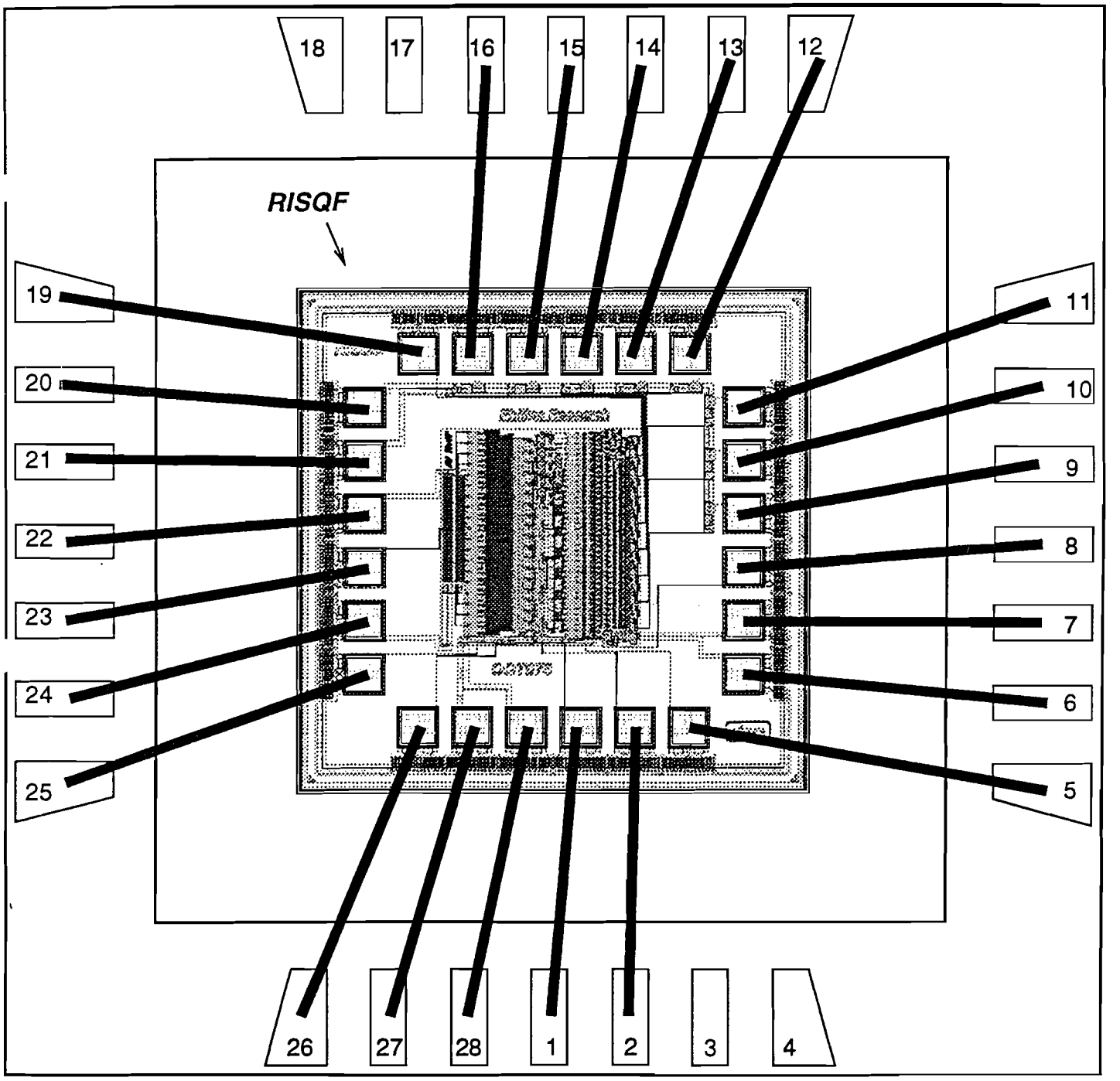
$$v_1 = C_1 \exp(\frac{A_0 - 1}{\tau} t) + C_2 \exp(\frac{-A_0 - 1}{\tau} t)$$

and

$$v_2 = -C_1 \exp(\frac{A_0 - 1}{\tau} t) + C_2 \exp(\frac{-A_0 - 1}{\tau} t)$$

with C_1 and C_2 being integration constants. V1 and V2 are the output voltages of amplifier 1 respectively amplifier 2 illustrated in figure 3.

Appendix 4 WIRING DIAGRAM OF THE ANALOG TO DIGITAL CONVERTOR

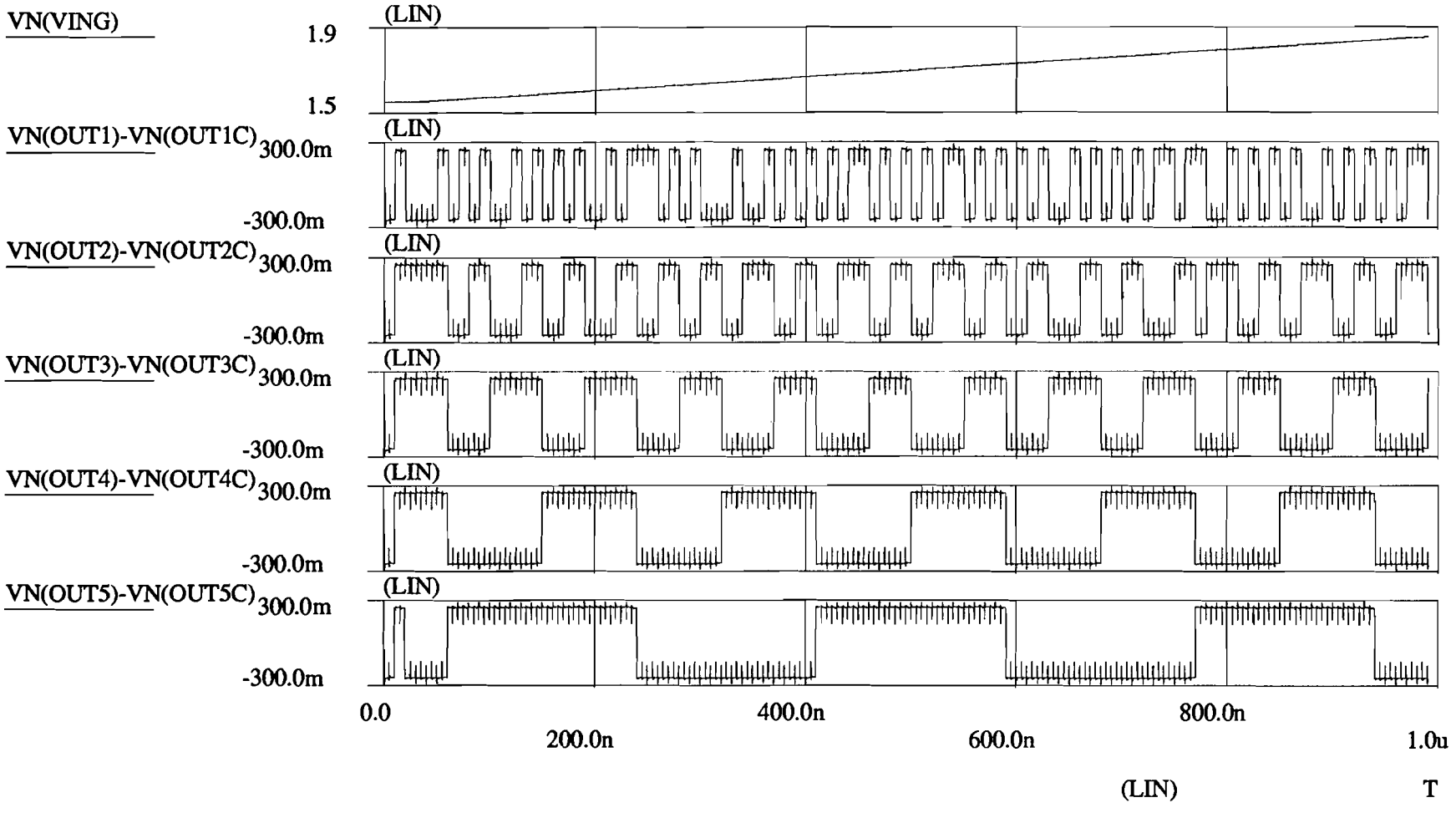


PIN LIST OF A/D CONVERTOR IN SPIRIT PROCESS - CERAMIC PLCC28		
1	VBIAS1	Bias input voltage, 0.85 Volt
2	VBIAS2	Bias input voltage, 1.0 Volt
3	VBIAS3	Bias input voltage, 2.0 Volt
4	CLKCIN	Clockc input
5	VDD2D	Digital VDD2, 2.85 Volt
6	VDDD	Digital VDD, 3.0 Volt
7	VSSD	Digital VSS
8	CLKIN	Clock input
9	B0	Digital output bus, LSB
10	B1	
11	B2	
12	B3	
13	B4	
14	B5	
15	B6	
16	B7	Digital output bus, MSB
17	OFL	Overflow signal
18	UFL	Underflow signal
19	N.C	
20	VSSB	Digital output buffers VSS
21	VDDB	Digital output buffers VDD, 3 Volt
22	REFLOW	Reference ladder, low voltage, default 1.5 Volt
23	REFMID	Reference ladder, middle voltage
24	REFHI	Reference ladder, high voltage, default 2.5 Volt
25	IN	Input Voltage
26	N.C.	

PIN LIST OF A/D CONVERTOR IN SPIRIT PROCESS - CERAMIC PLCC28		
27	VSSA	Analog Vss
28	VCCA	Analog Vcc

Appendix 5 SIMULATION RESULTS FINE PART

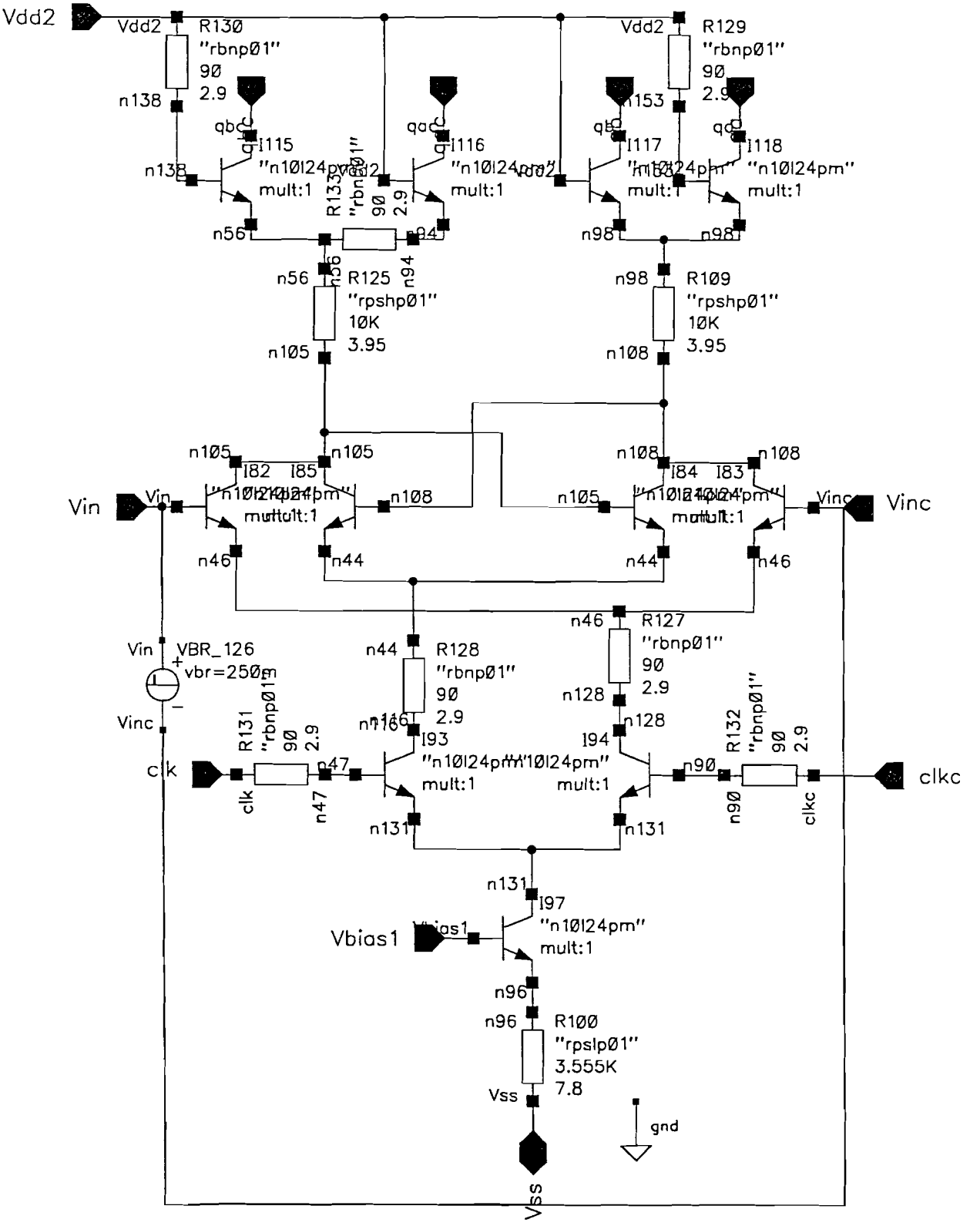
Simulation A/D convertor



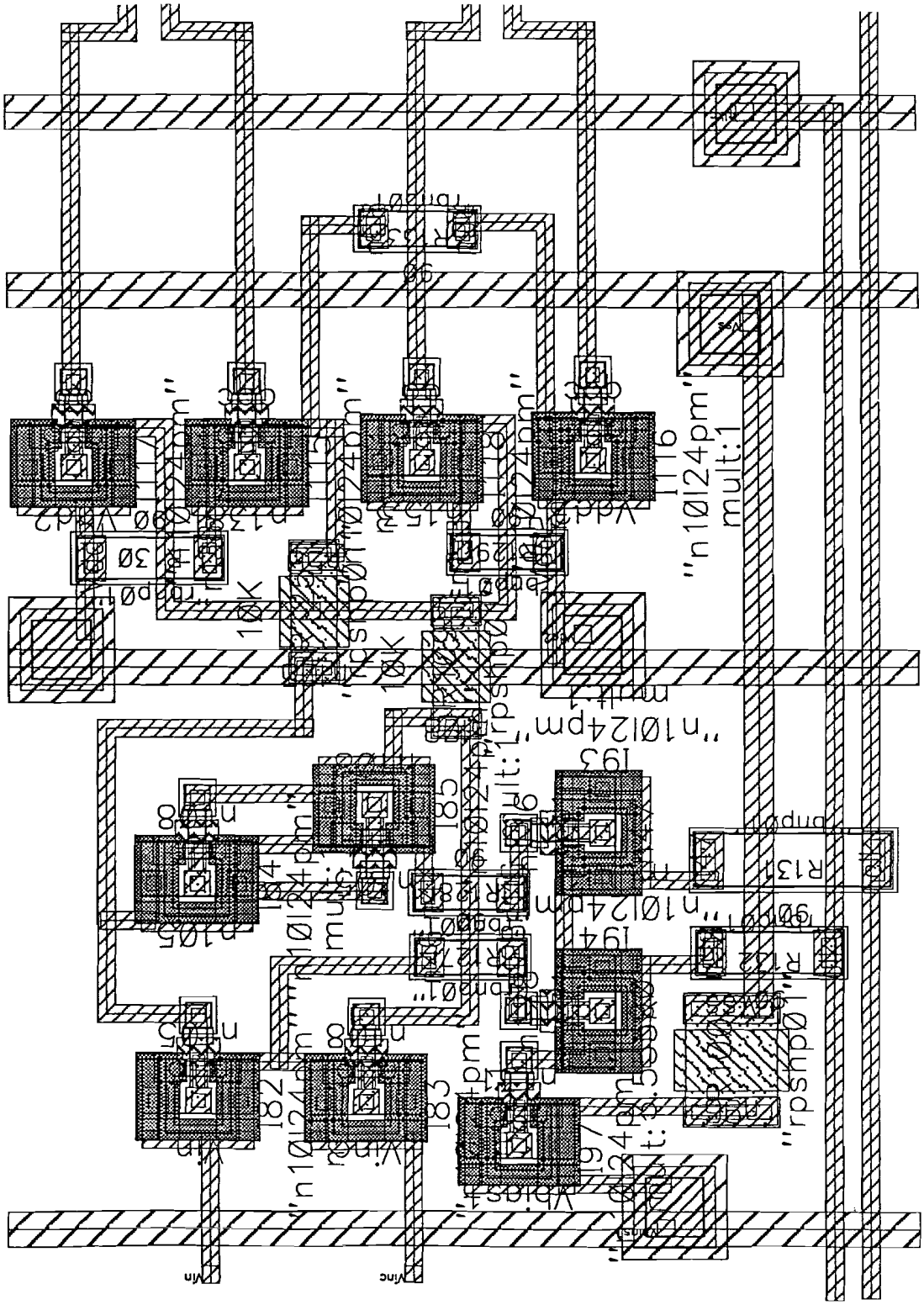
Appendix 6 SCHEMATIC AND LAYOUT OF THE SUB-CIRCUITS OF THE ADC

compsl: slave comparator fine part
compsl1: slave comparator fine part
compsmsb2: slave comparator msb-2 signal fine part
compslc: slave comparator coarse part
compslsmsb: slave comparator smsb signal in coarse part
compma: master comparator
diffmsb2: differential amplifier msb-2 signal
romamp1: rom table differential amplifier
romamp2: rom table differential amplifier
romamp3: rom table differential amplifier
latchsl: slave latch
latchma: master latch
exorla: EXOR function fine part
EXOR: EXOR circuit
overfl: overflow circuit
bitsync: bitsync circuit coarse part
compa: master-slave comparator fine part
compa1: master-slave comparator fine part
compamsb2: master-slave comparator msb-2 signal fine part
comcoarse1: master-slave comparator coarse part
compcoarse2: master-slave comparator smsb signal coarse part
romtab: decode table fine part
latch: master-slave latch
romtot: total rom table differential amplifiers
comptot: total comparator fine part
comptotc: total comparator coarse part
latchtot: total latch fine part
latchtotc: total latch coarse part
uitbuf: output buffer
clock: clock driver
ovunfl: total coarse part
adc: total layout of the ADC

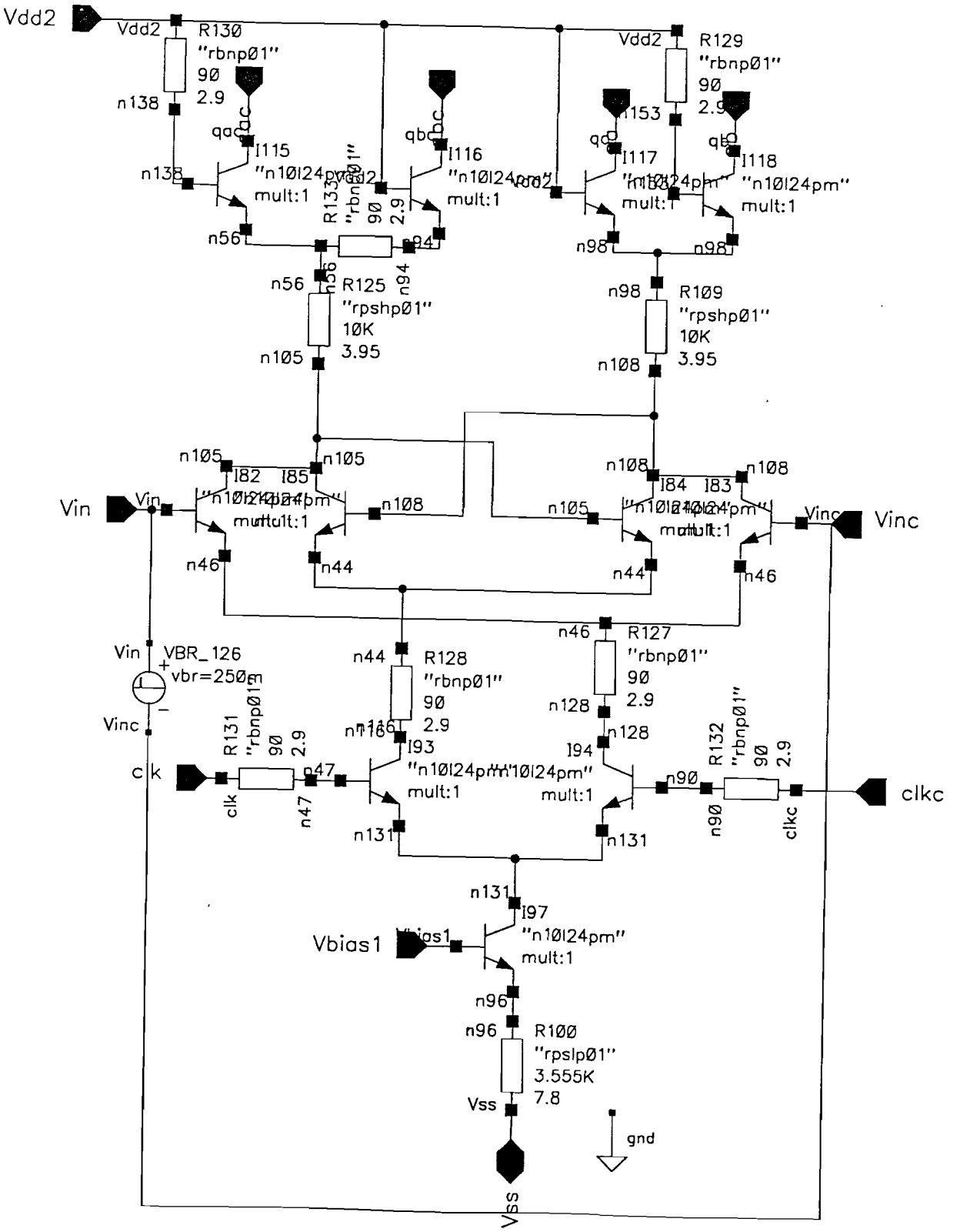
Schematic compsl: slave comparator fine part



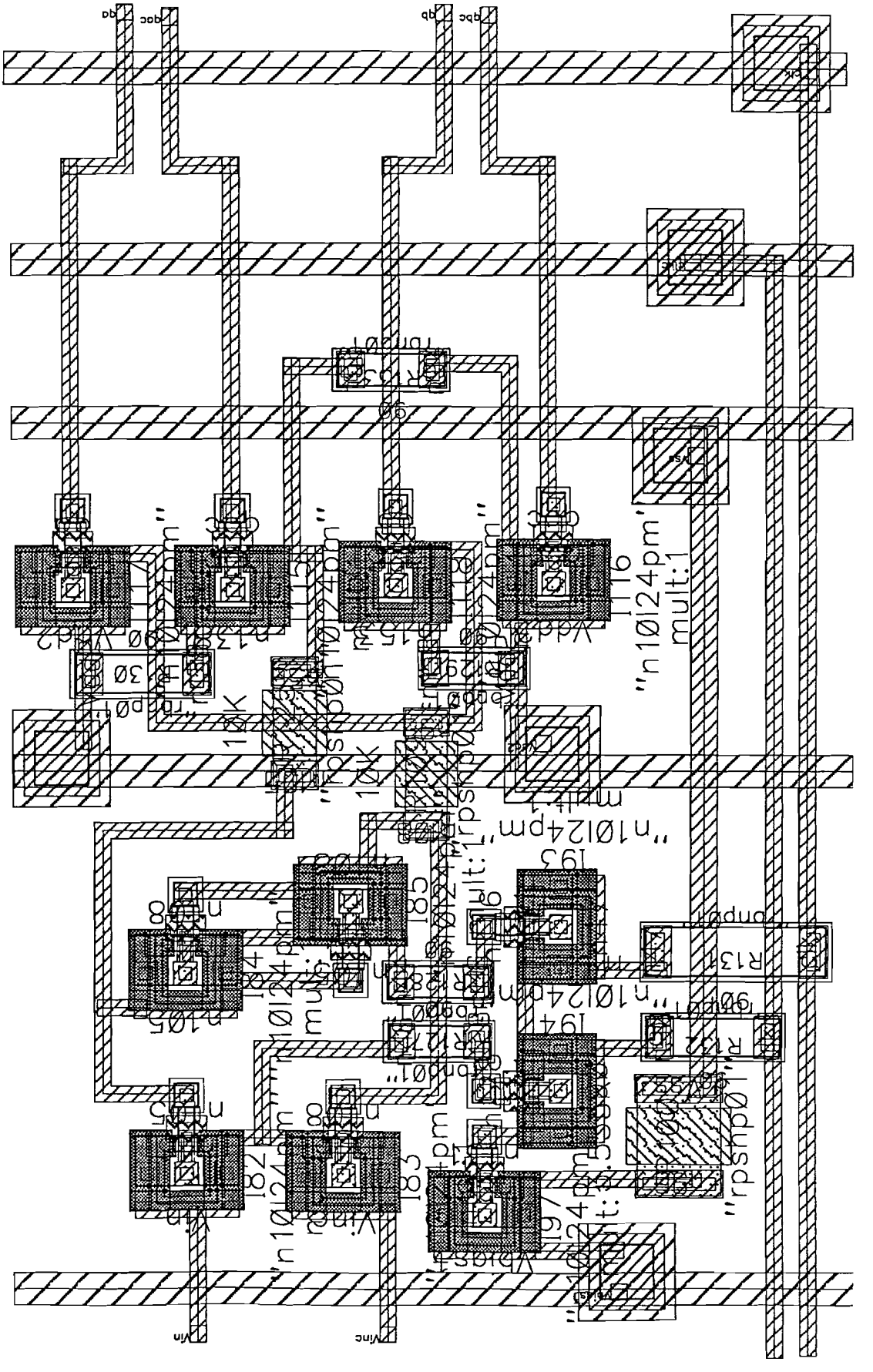
Lay-out compsl: slave comparator fine part



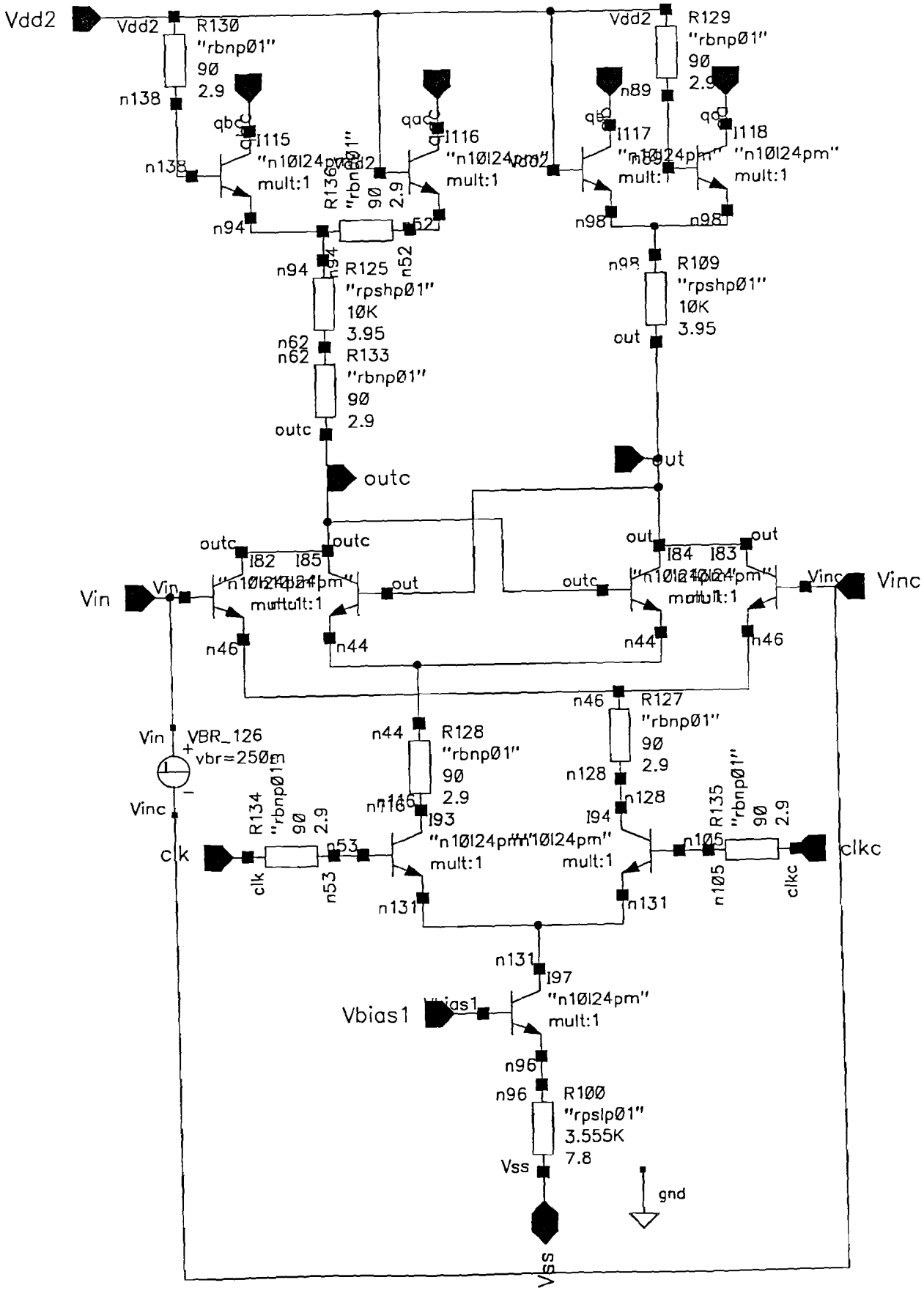
Schematic compsl1: slave comparator fine part



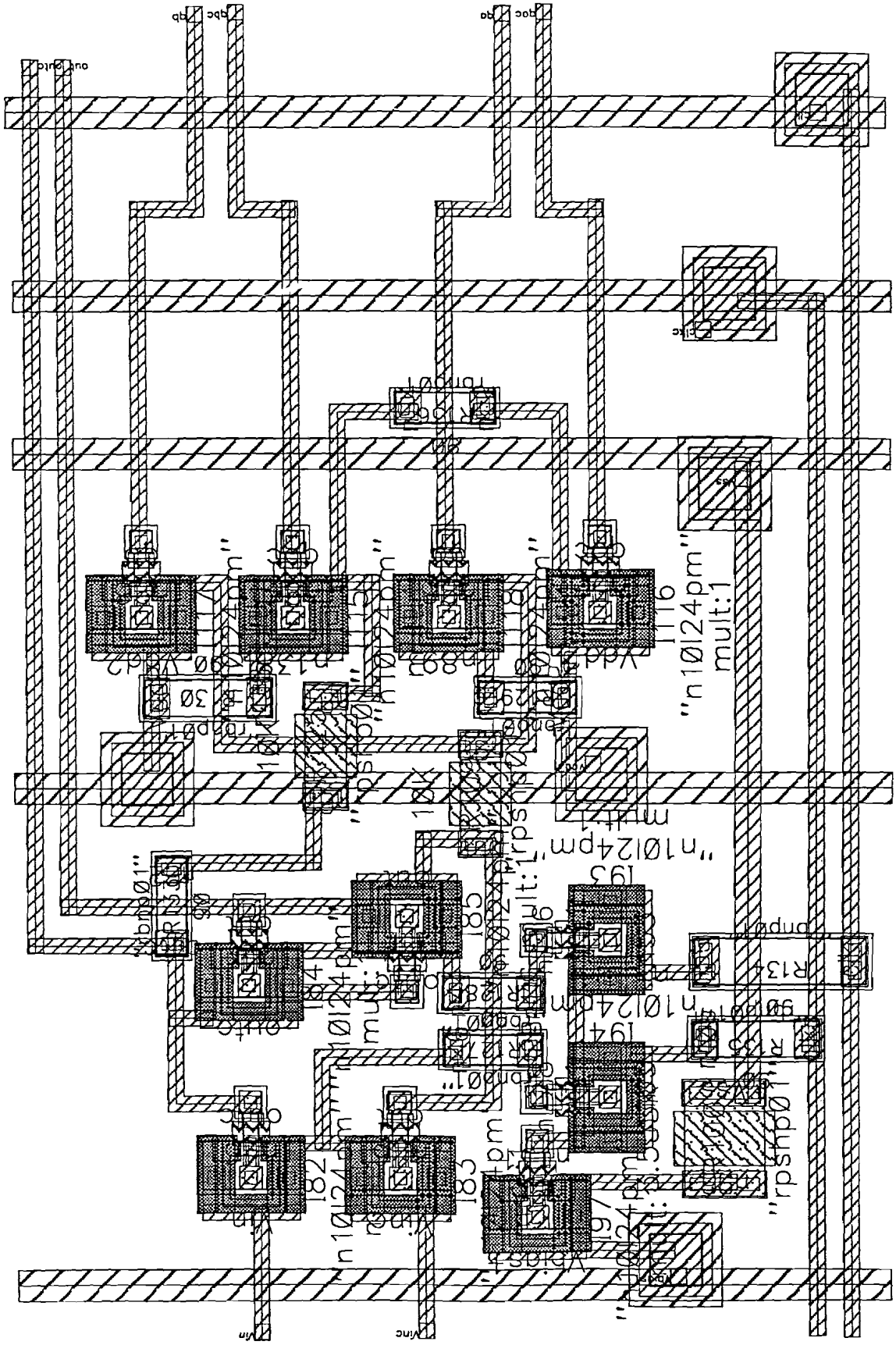
Lay-out compsl1: slave comparator fine part



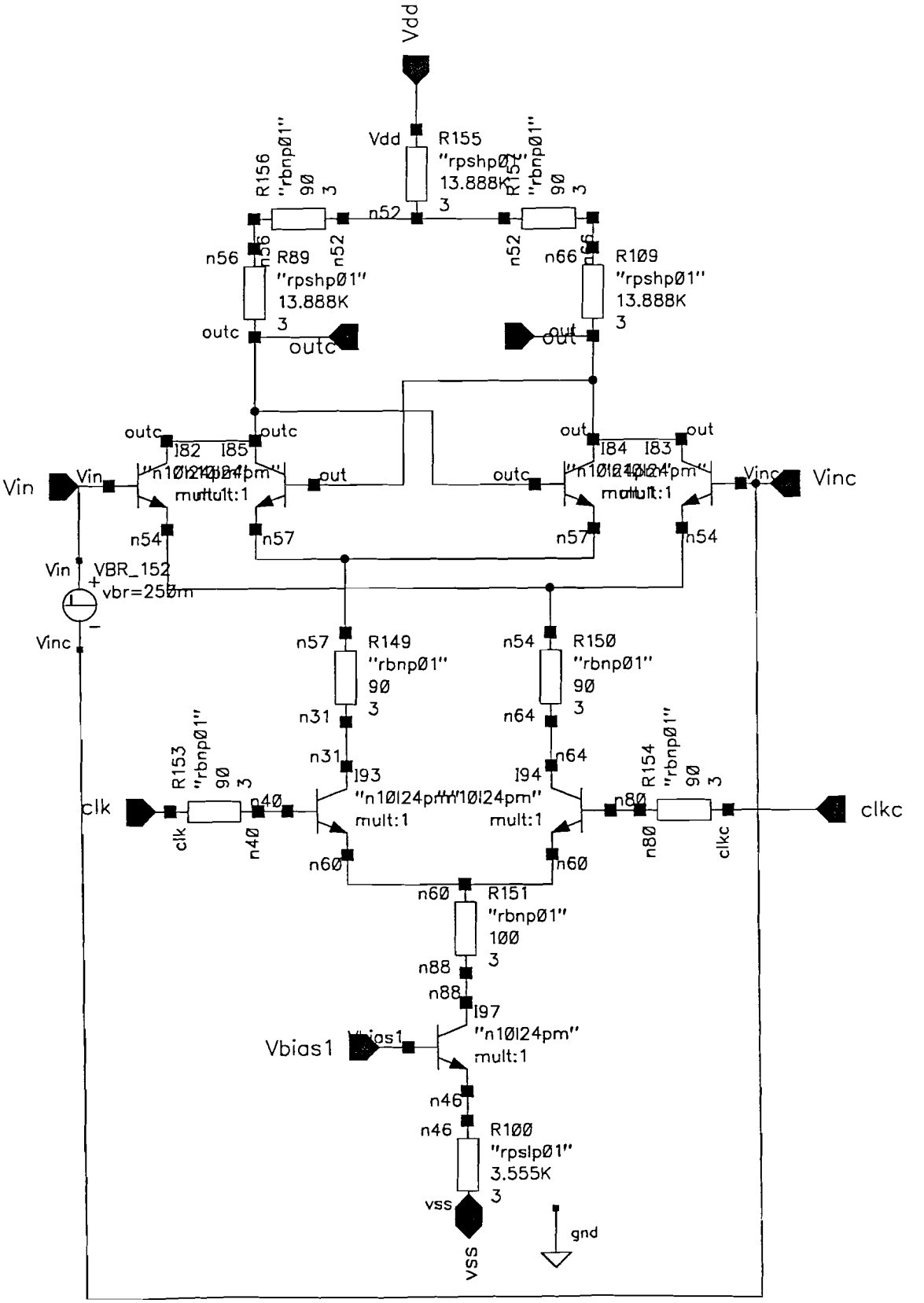
Schematic compsmsb2: slave comparator msb-2 signal fine part



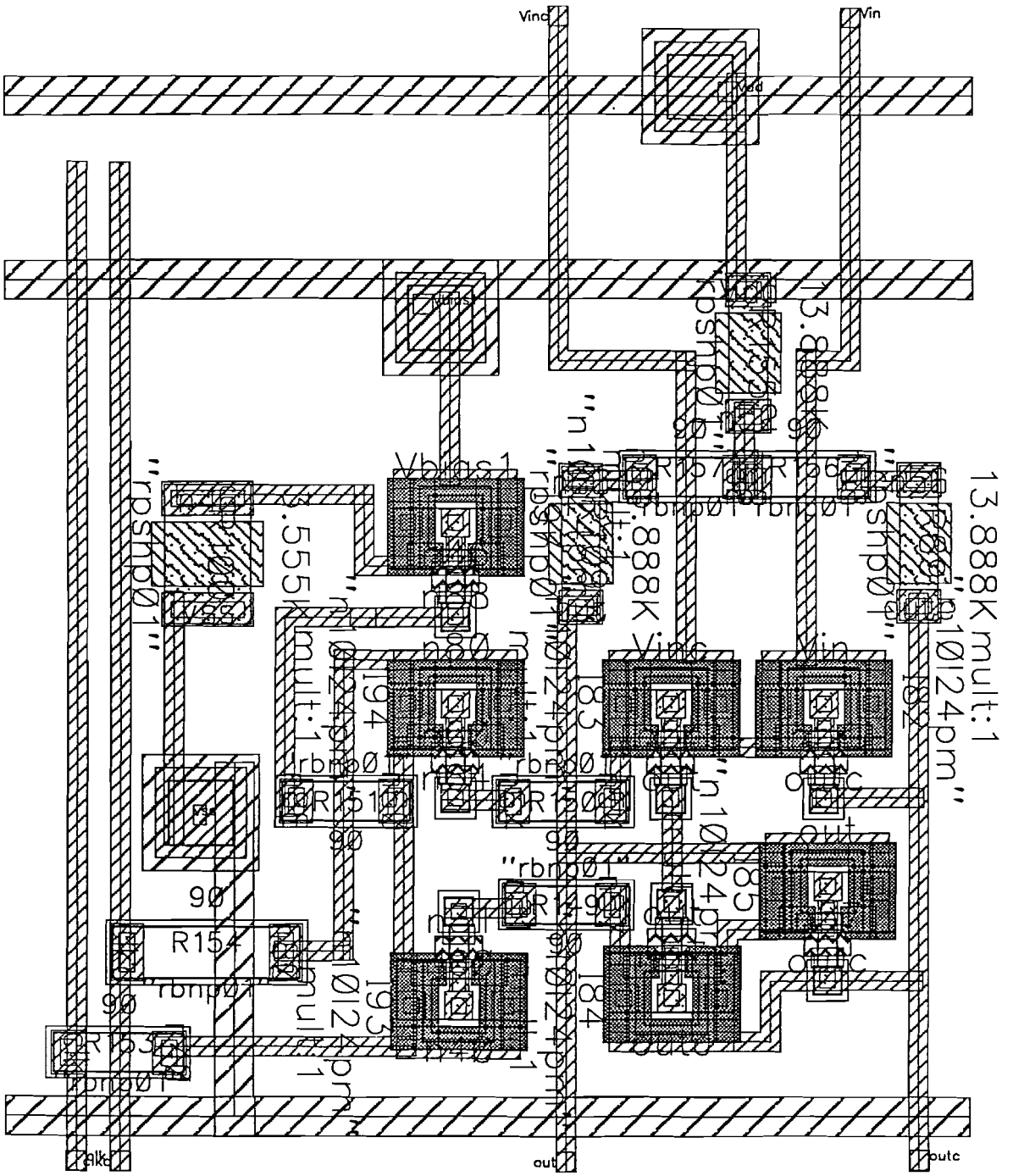
Lay-out compsmsb2: slave comparator msb-2 signal fine part



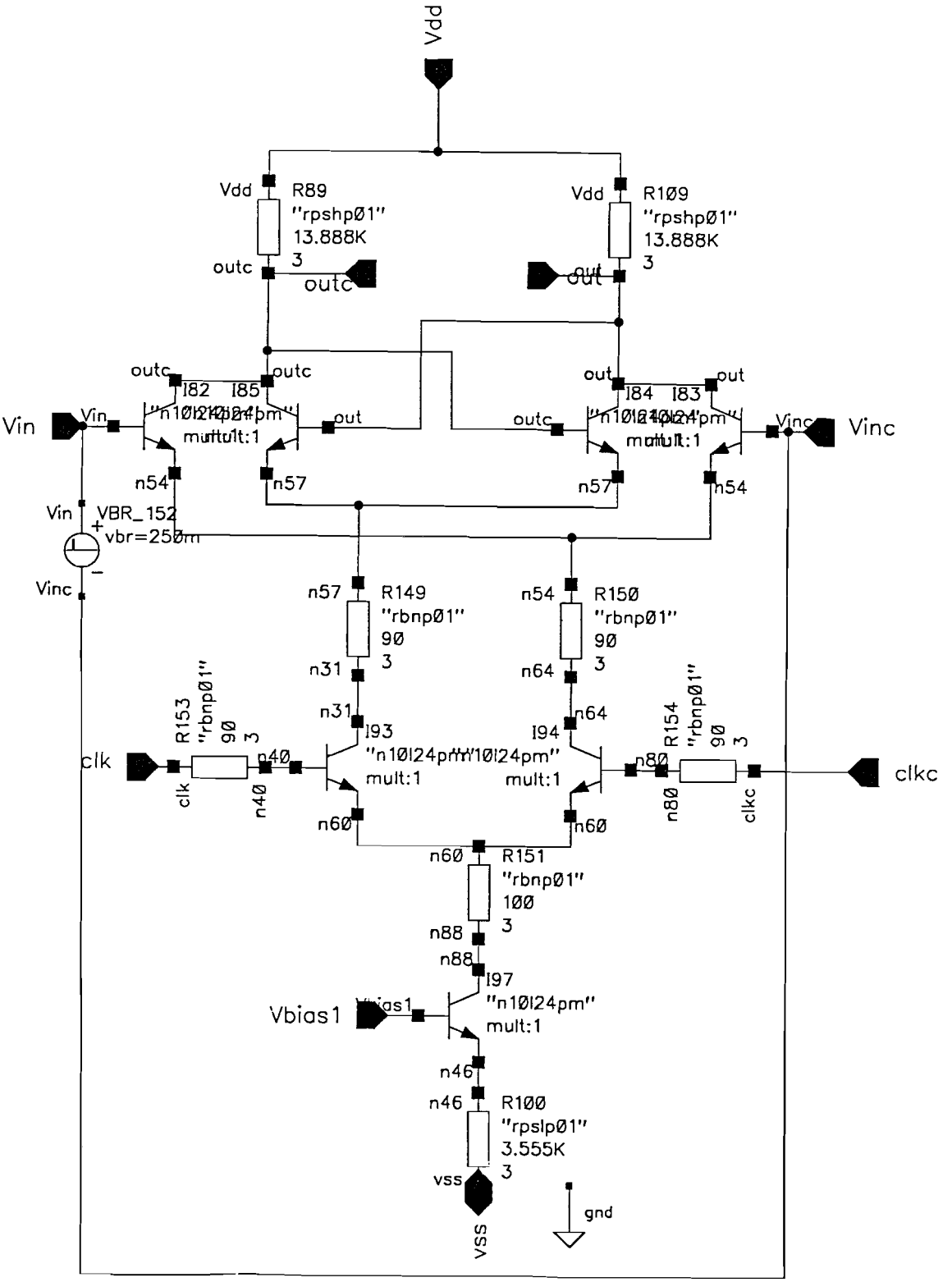
Schematic compslc: slave comparator coarse part



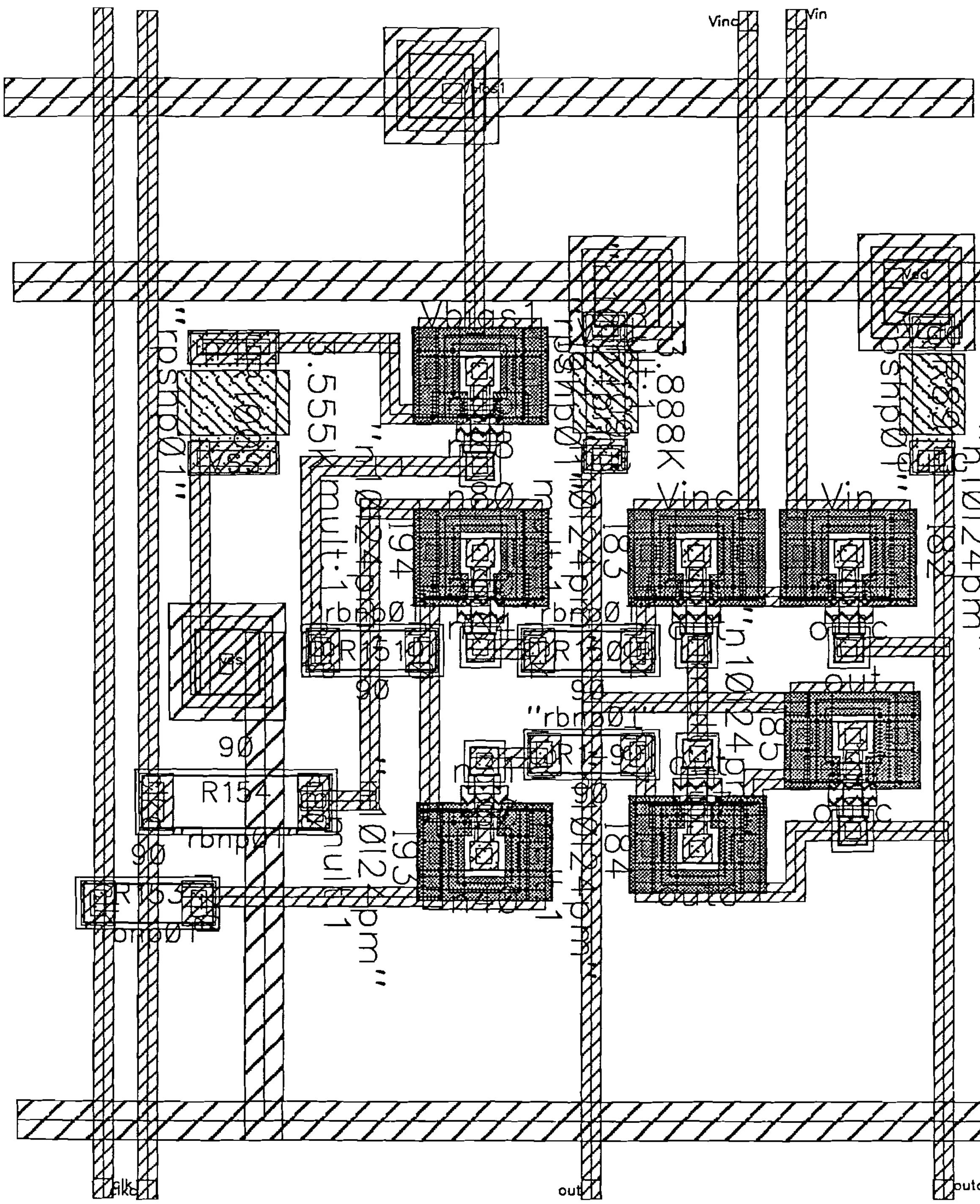
Lay-out compslc: slave comparator coarse part



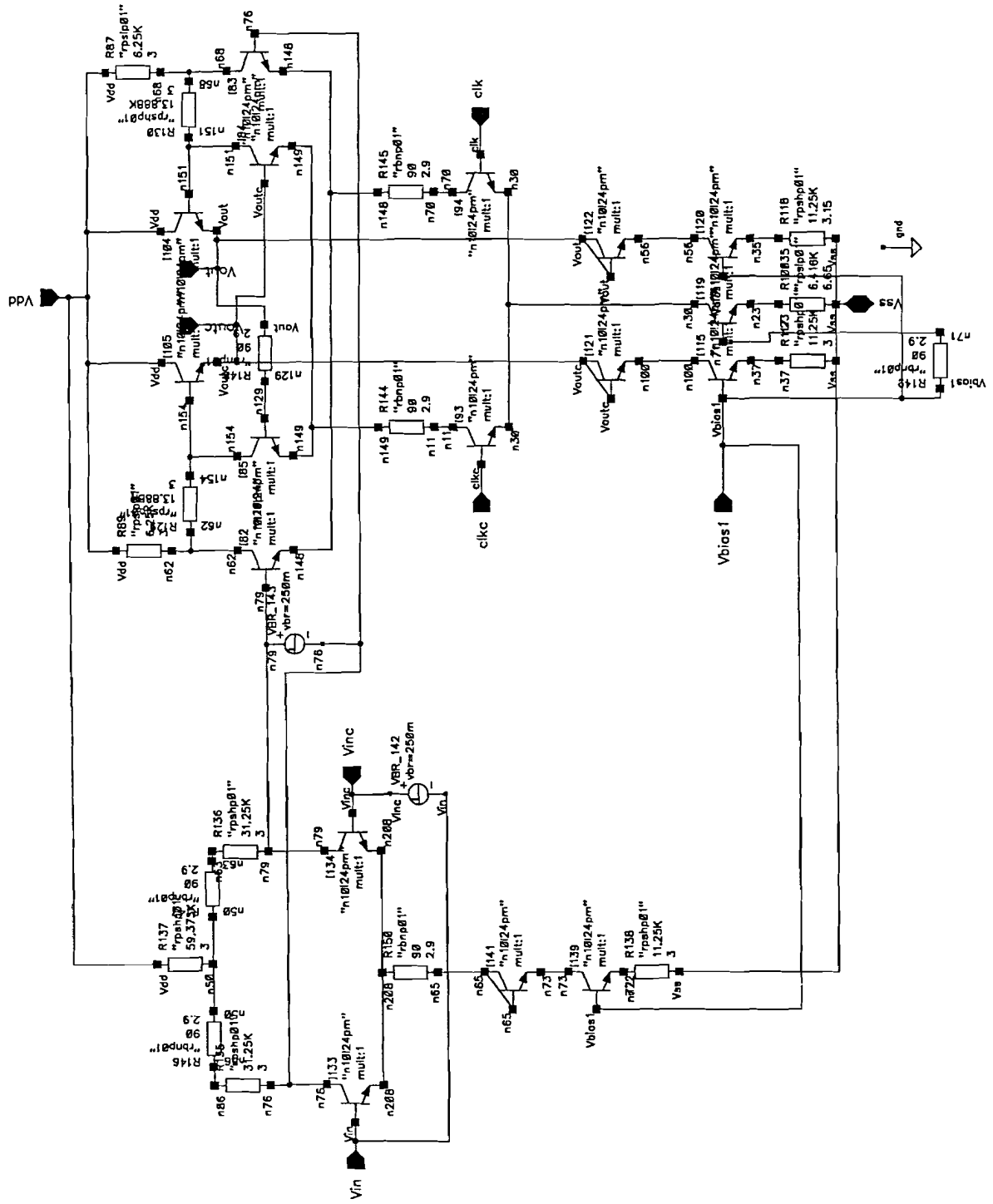
Schematic compslsmsb: slave comparator smsb signal in coarse part



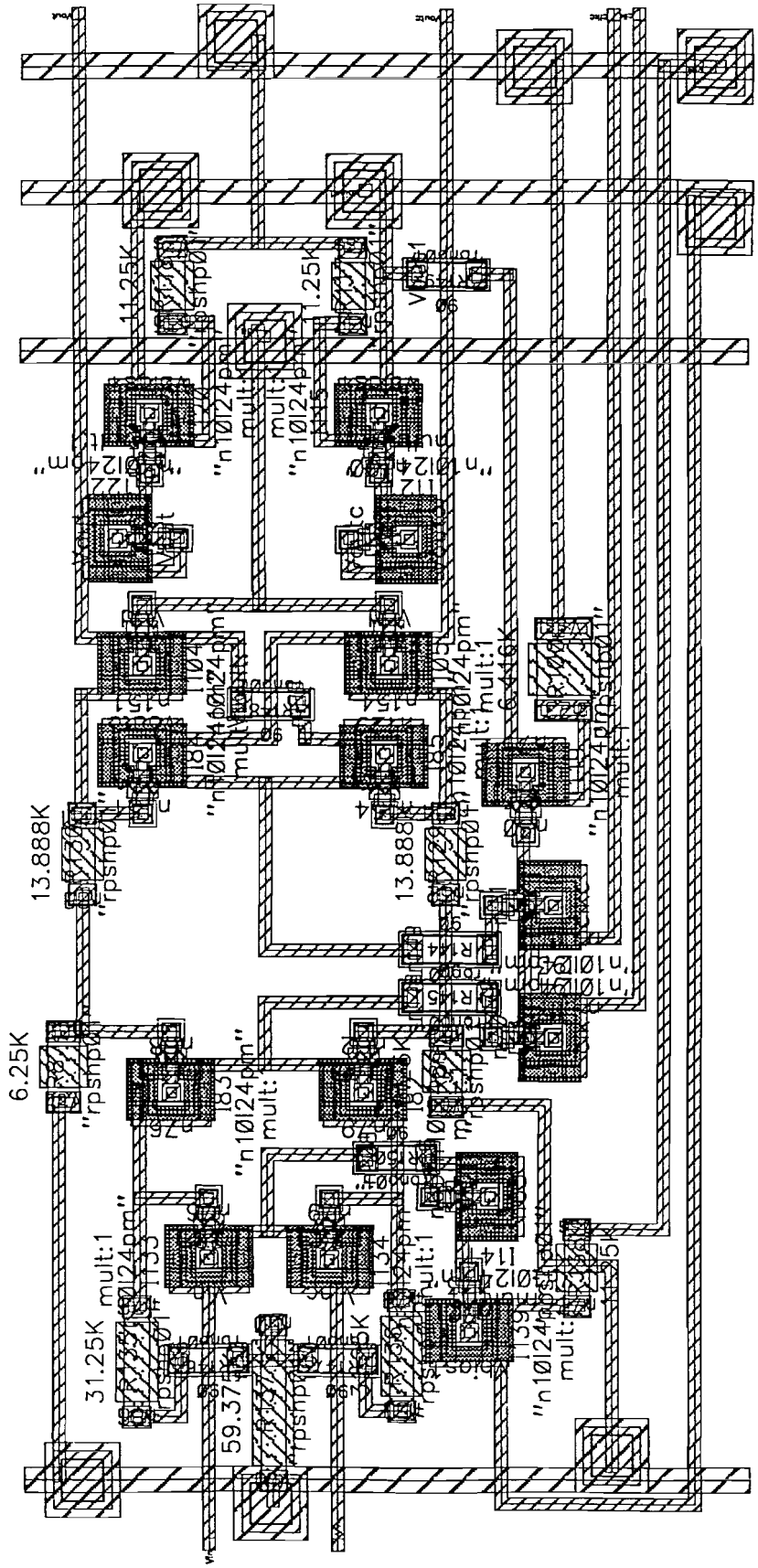
Lay-out compslsmsb: slave comparator smsb signal in coarse part



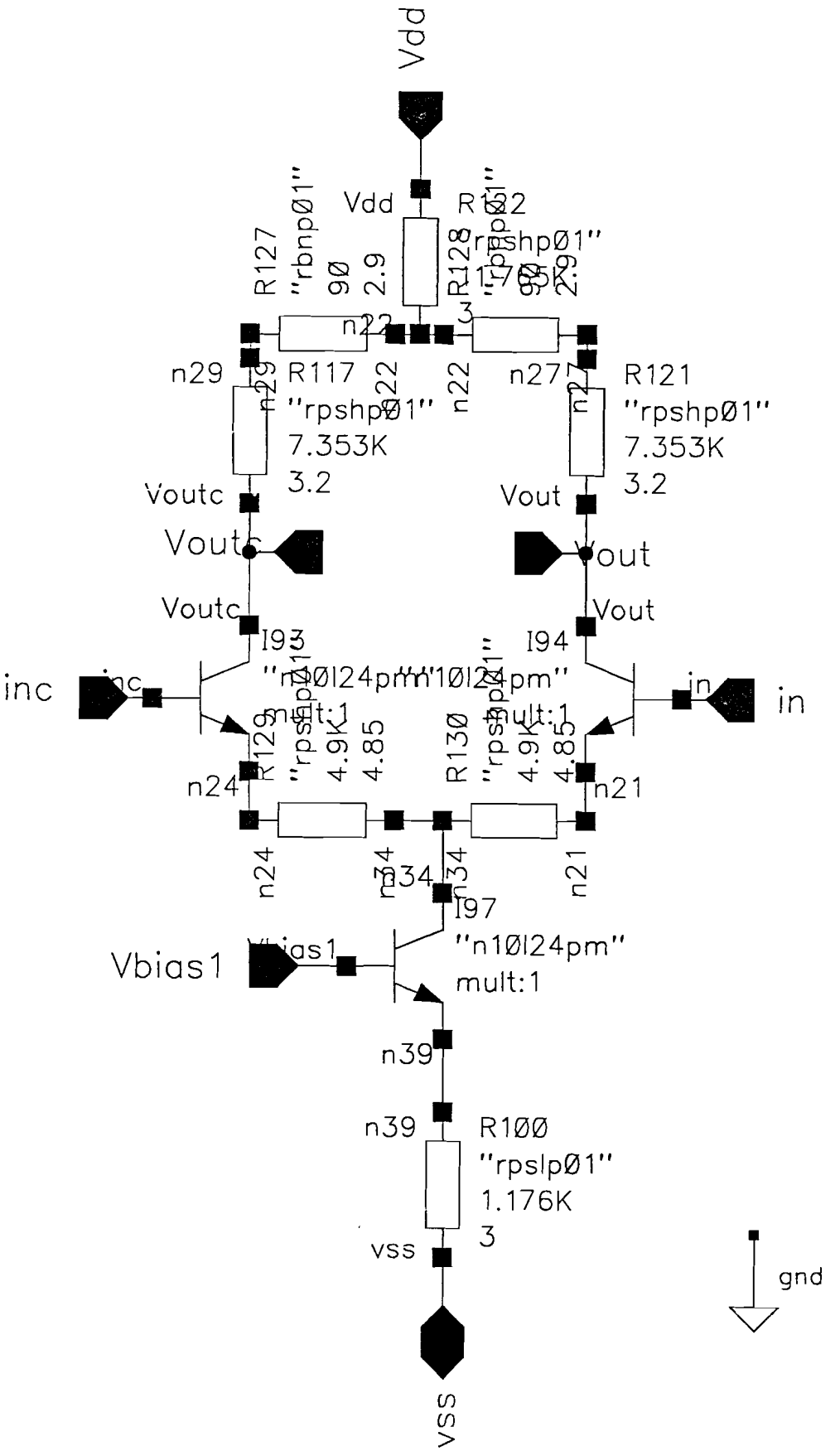
Schematic compma: master comparator



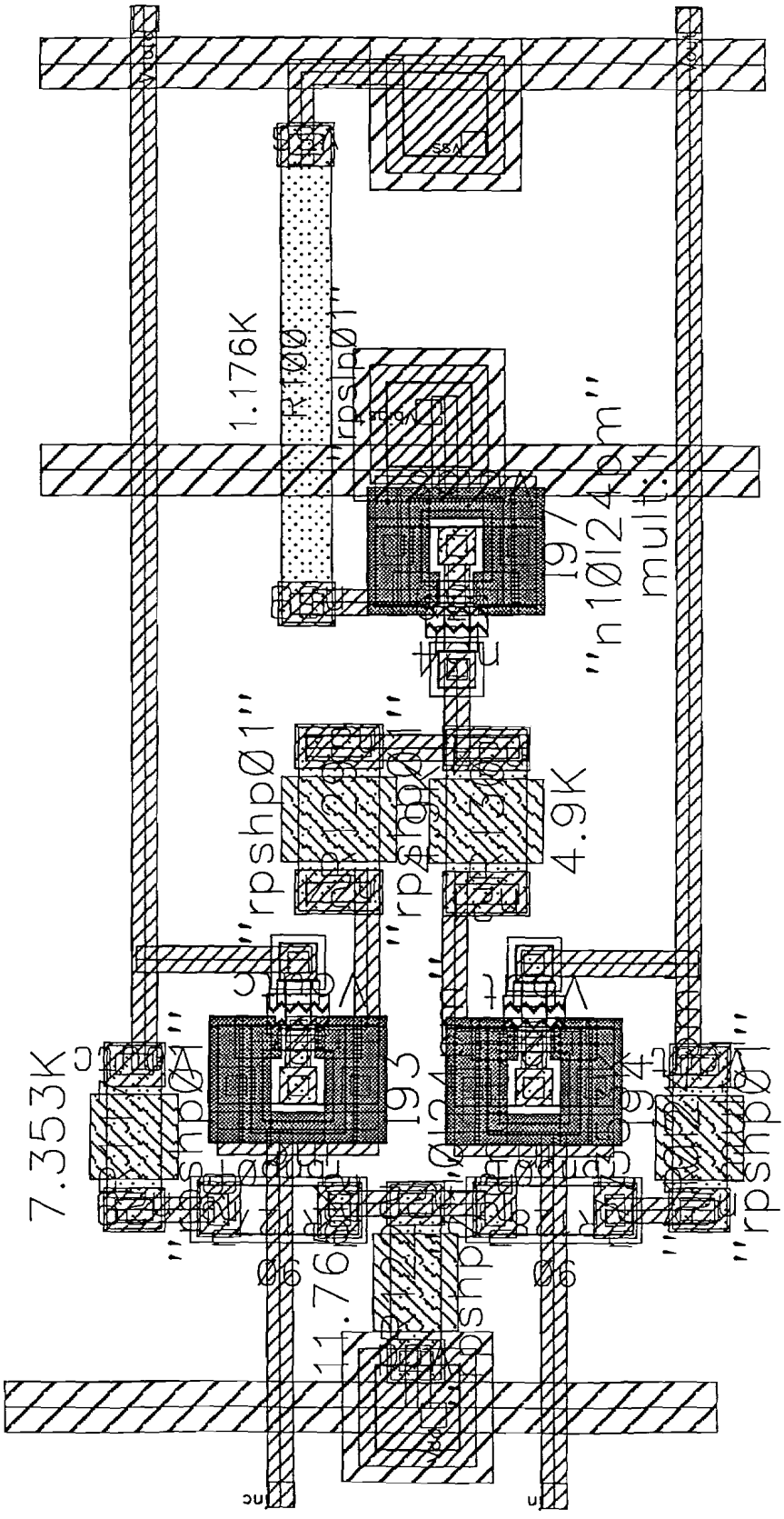
Lay-out compma: master comparator



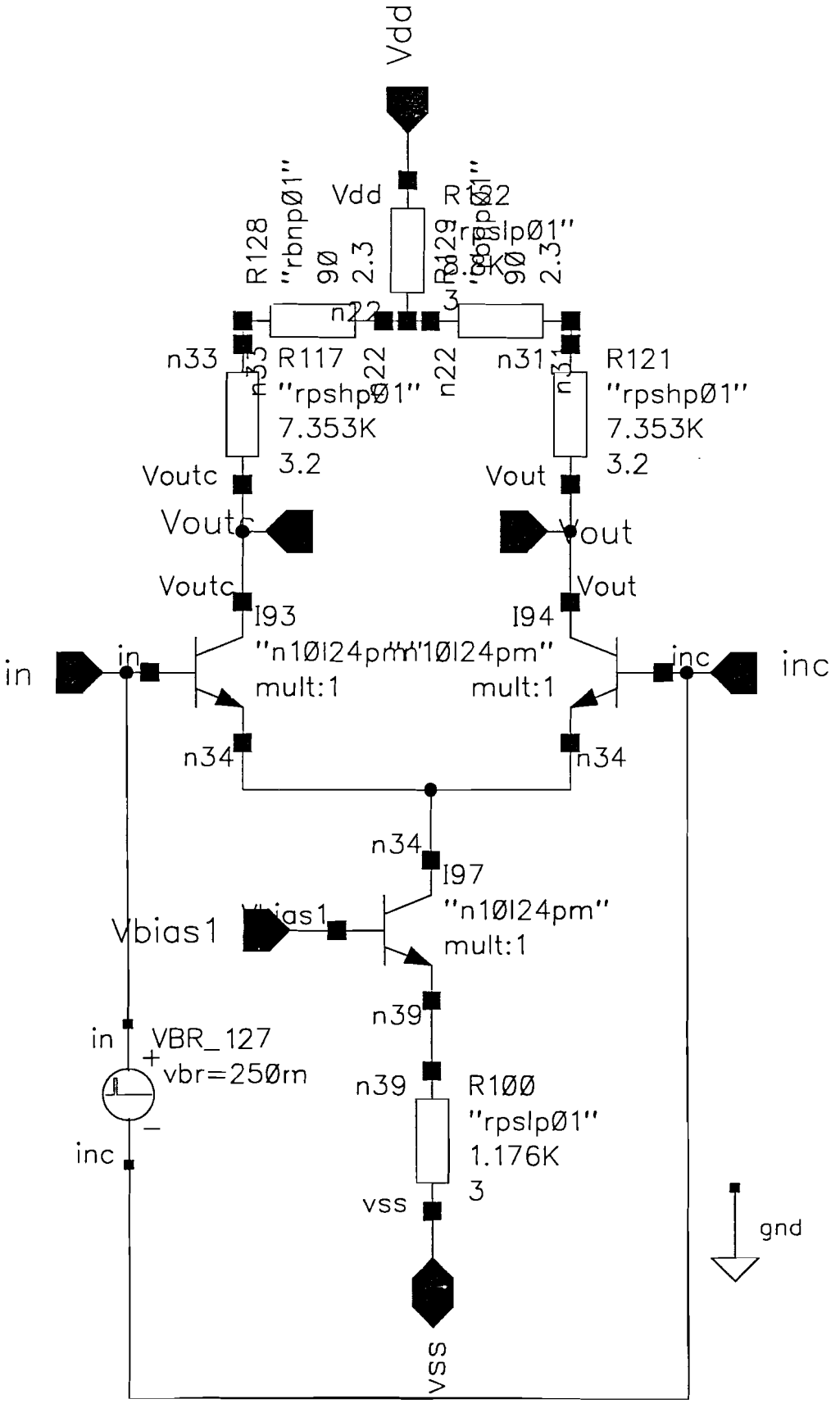
Schematic diffmsb2: differential amplifier msb-2 signal



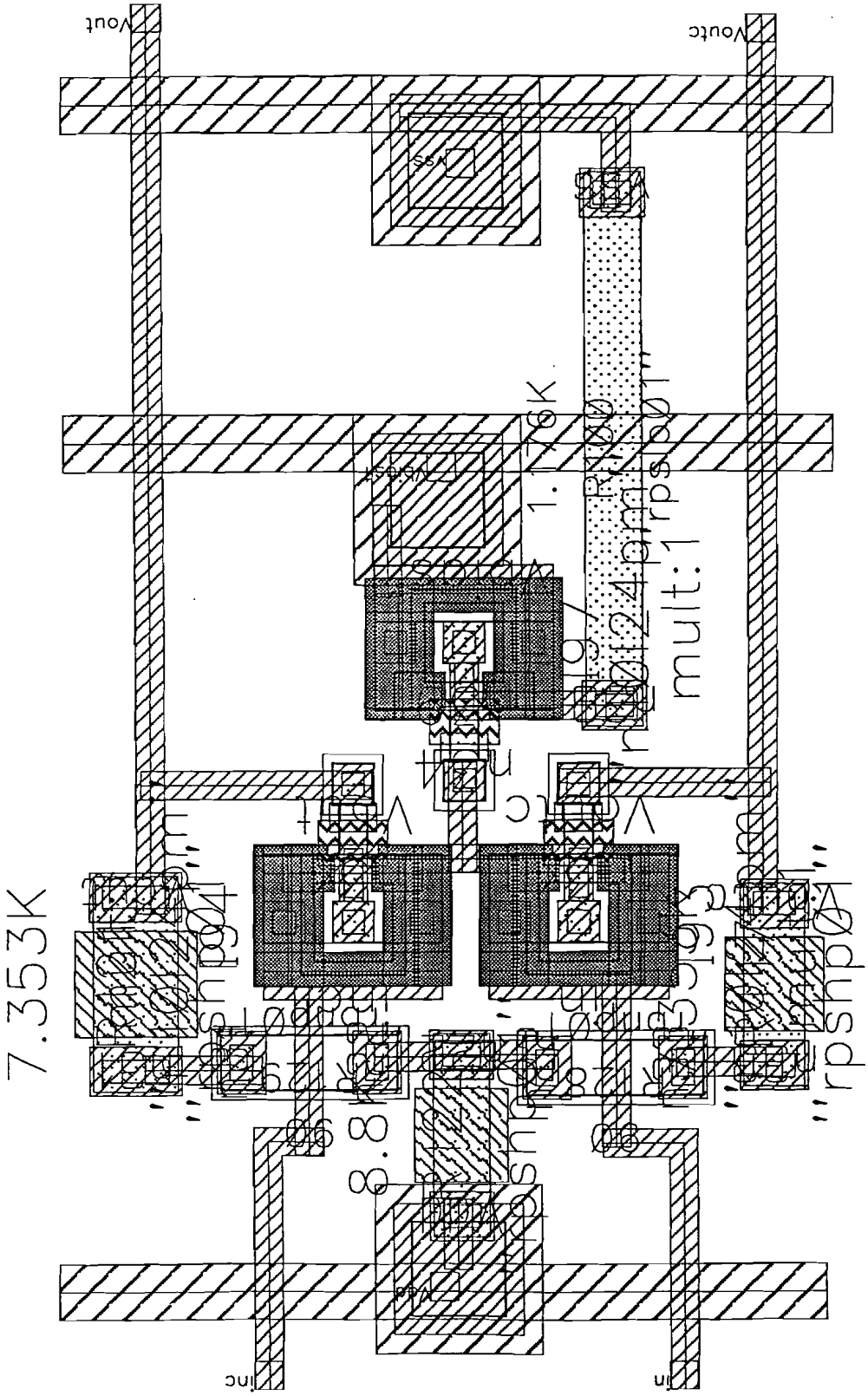
Lay-out diffmsb2: differential amplifier msb-2 signal



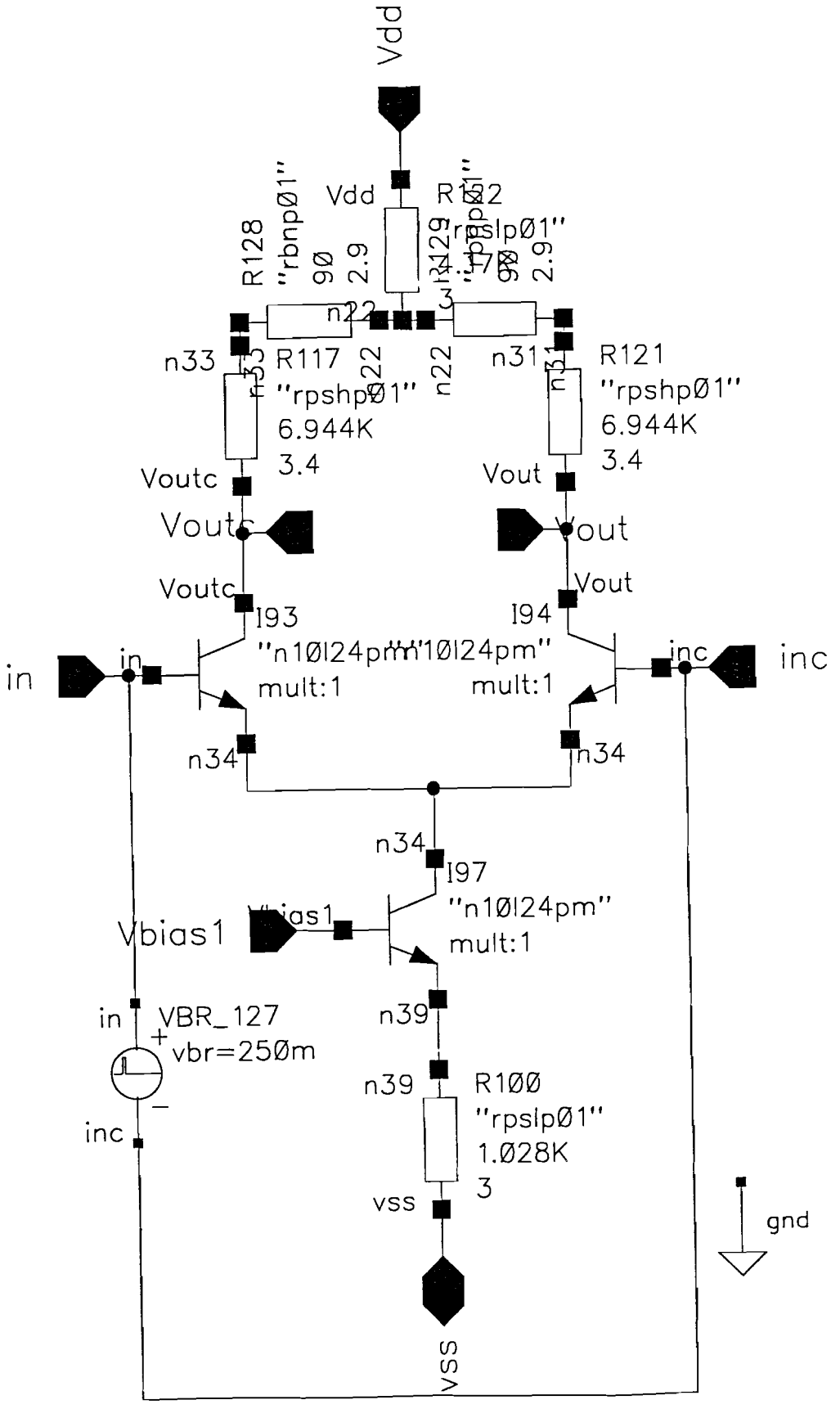
Schematic romamp1: rom table differential amplifier



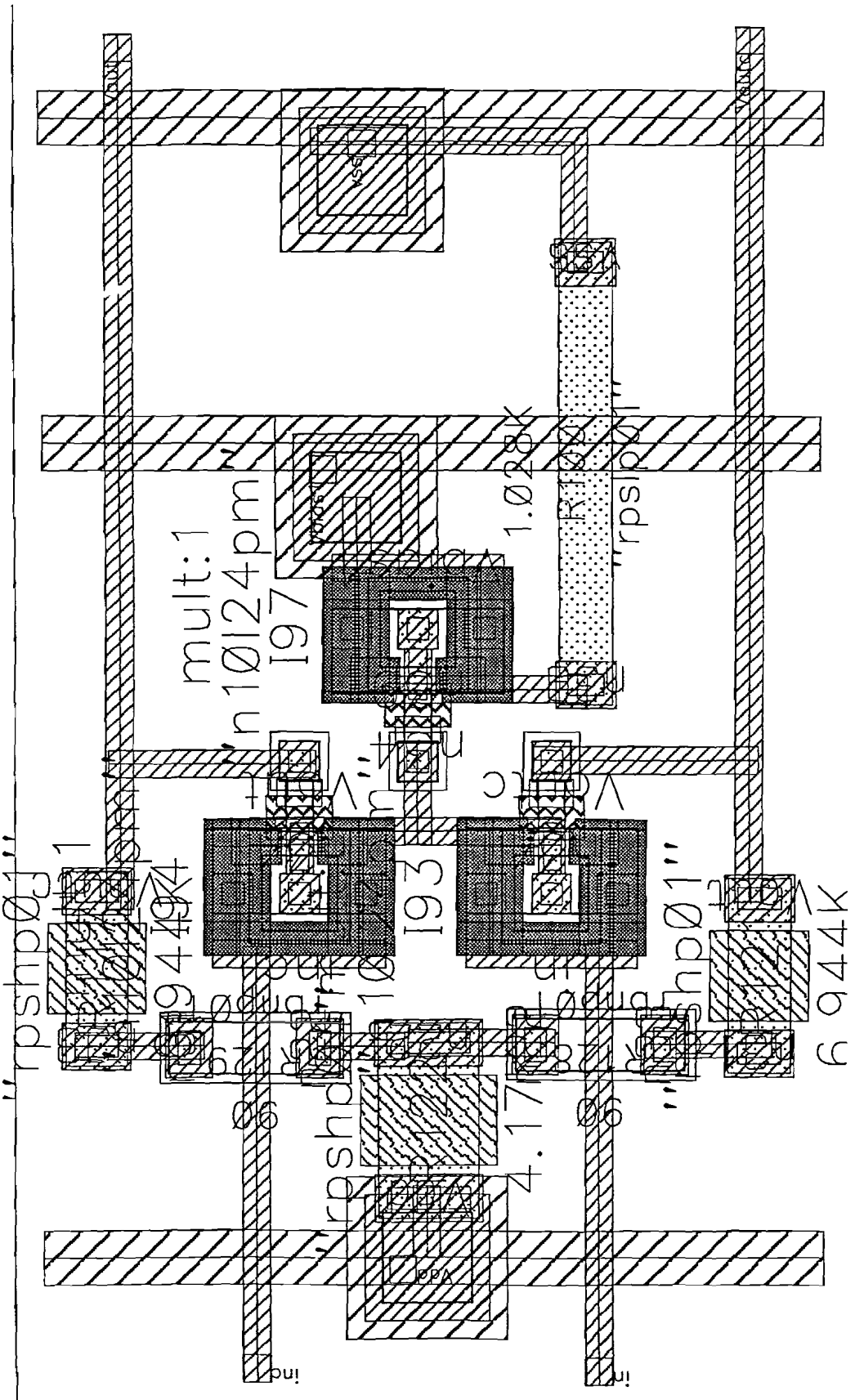
Lay-out romamp1: rom table differential amplifier



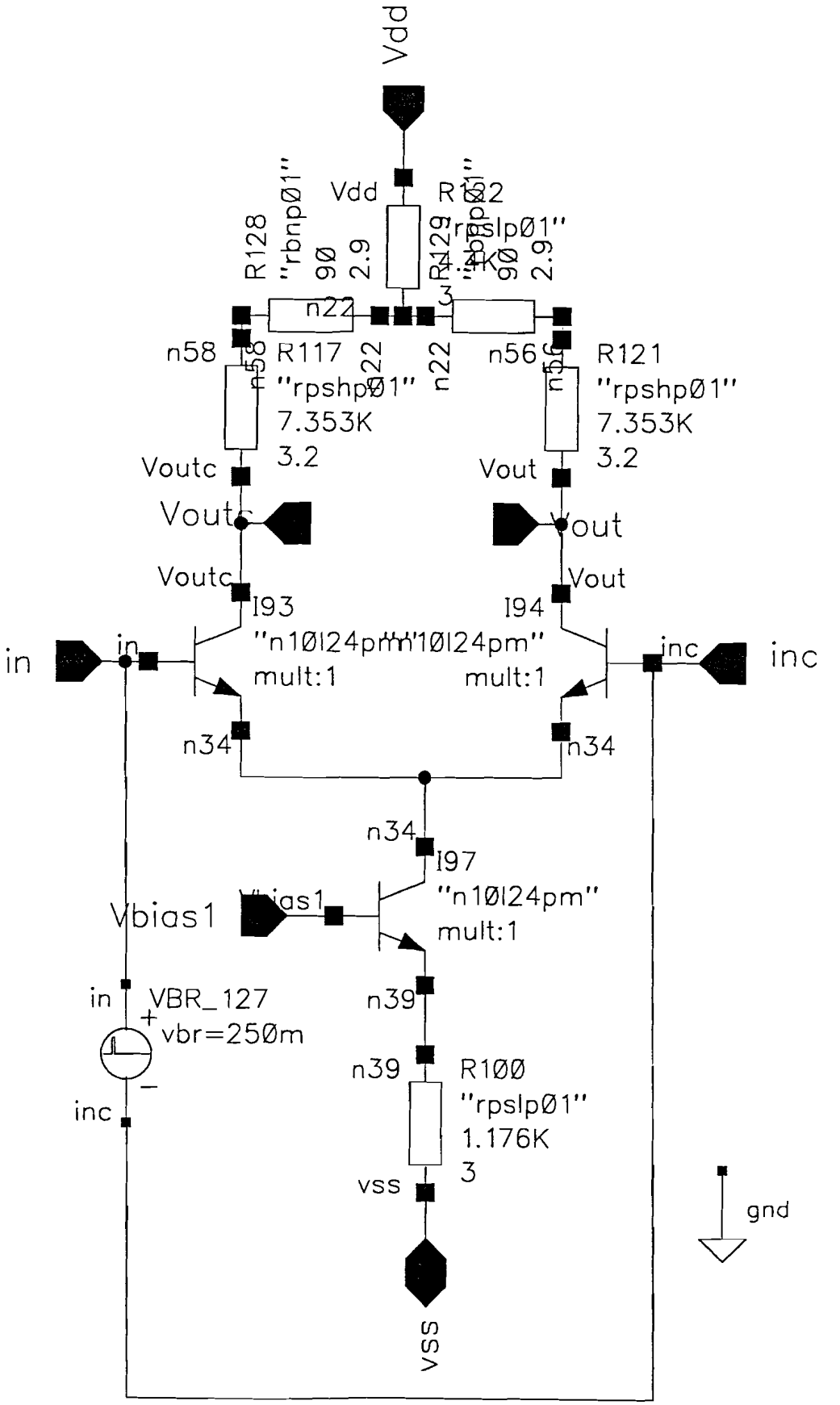
Schematic romamp2: rom table differential amplifier



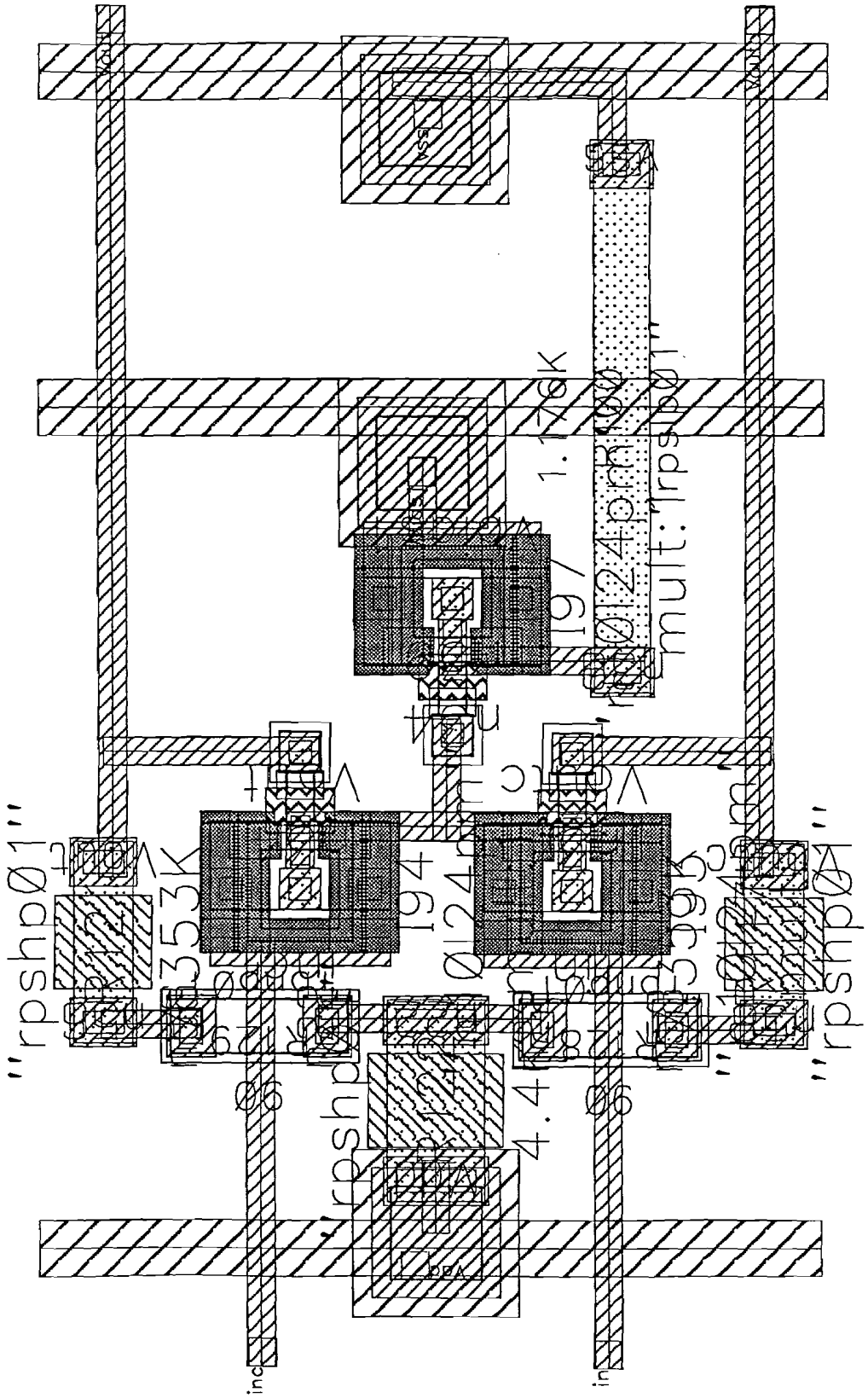
Lay-out romamp2: rom table differential amplifier



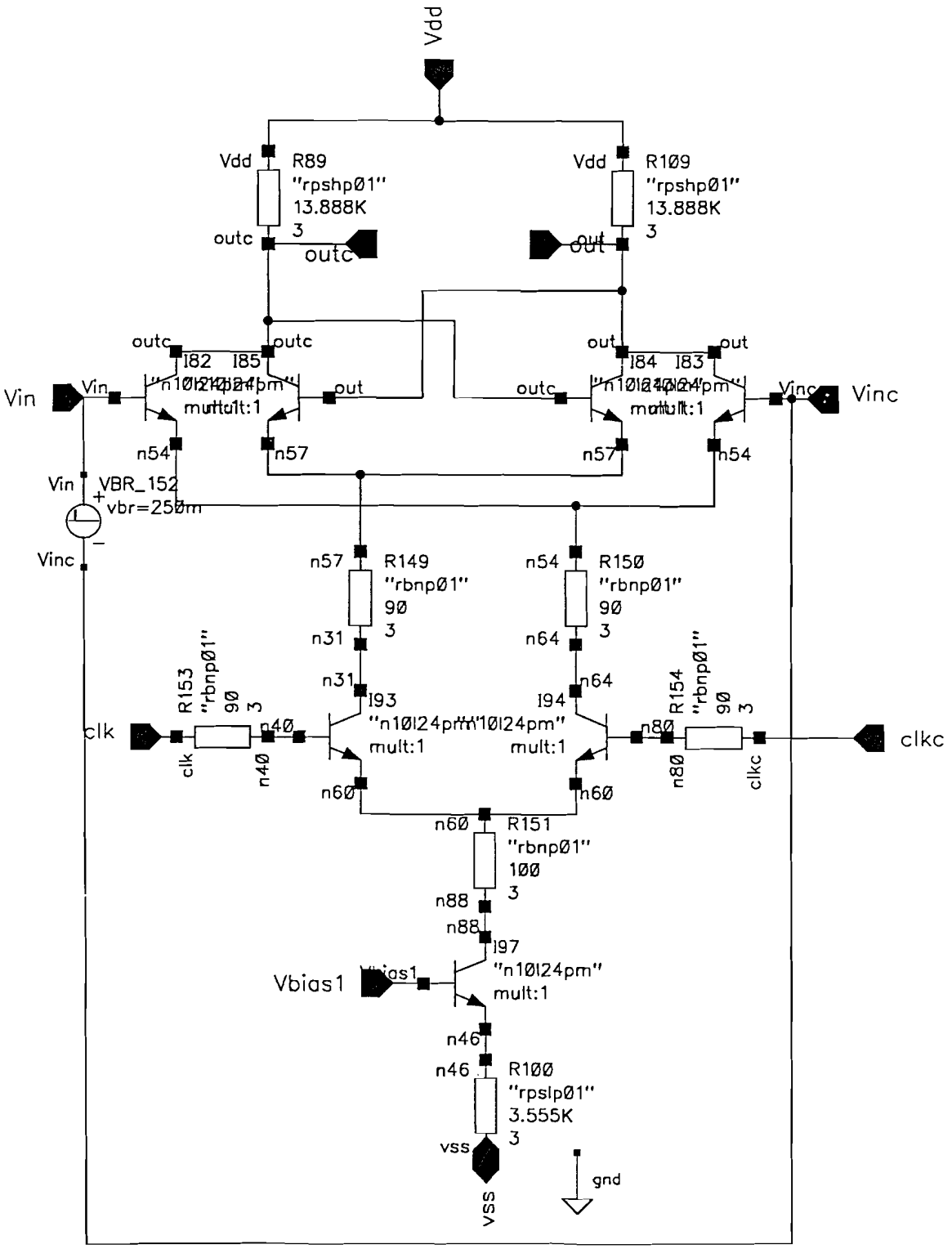
Schematic romamp3: rom table differential amplifier



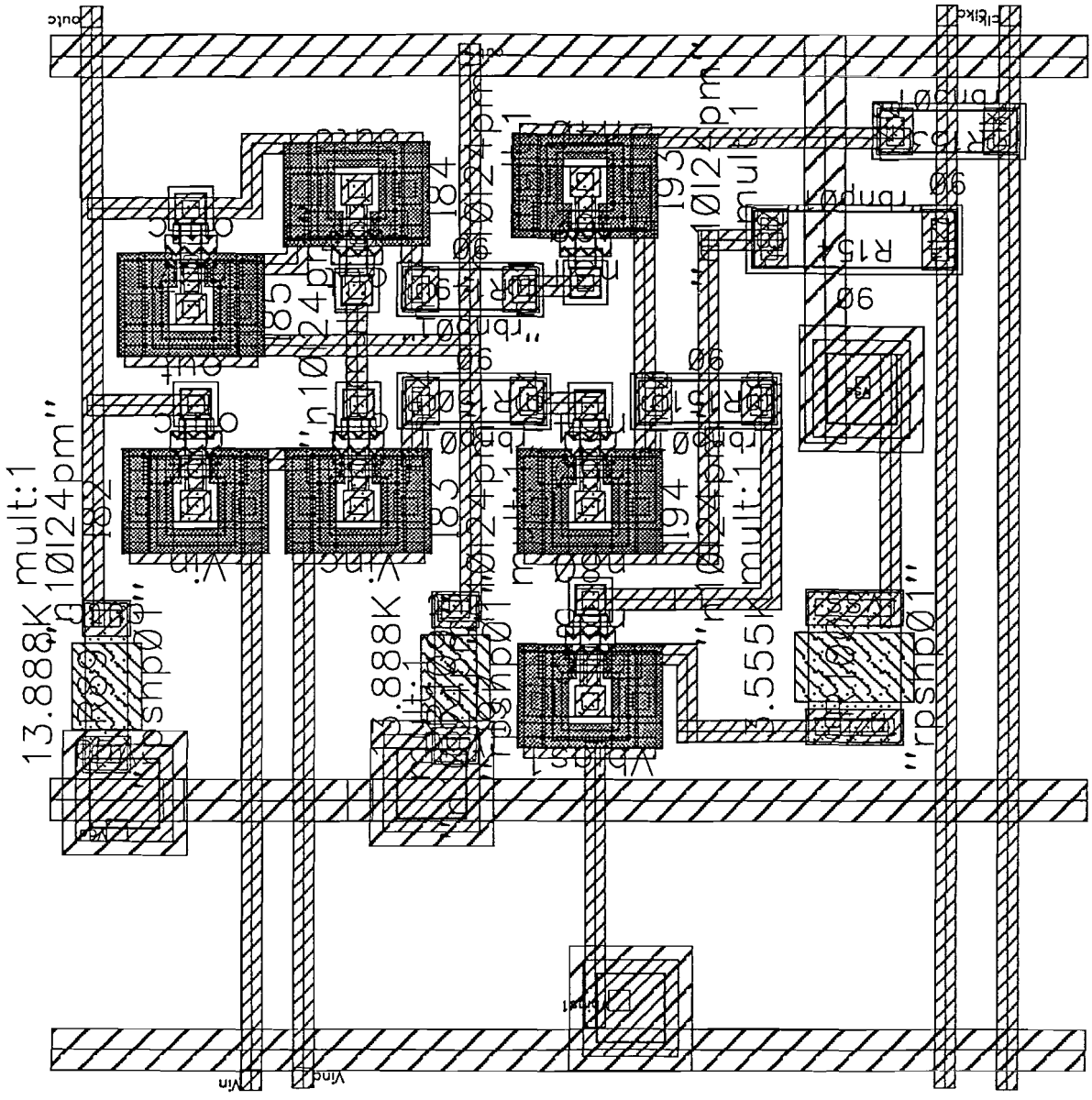
Lay-out romamp3: rom table differential amplifier



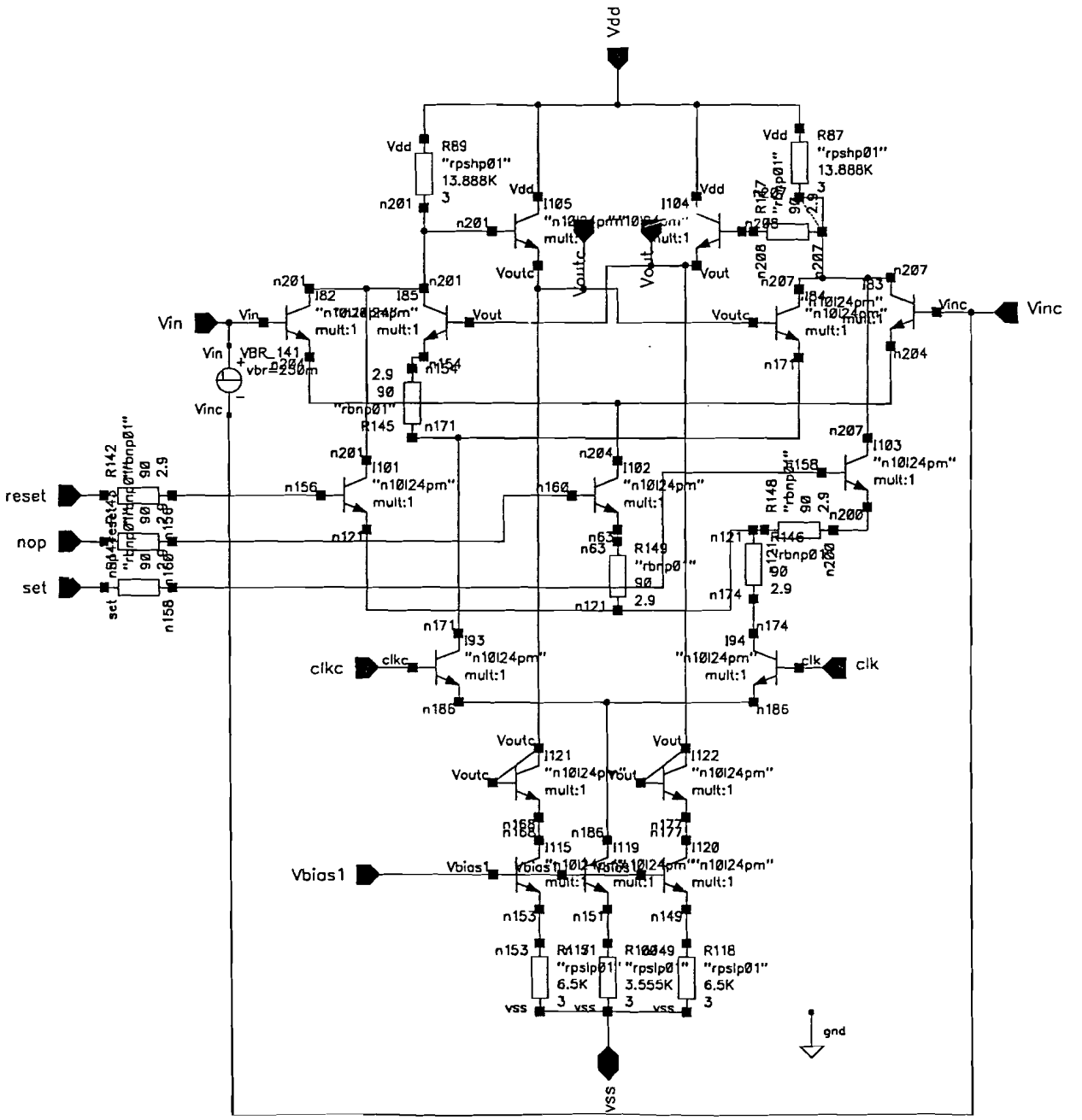
Schematic latchsl: slave latch



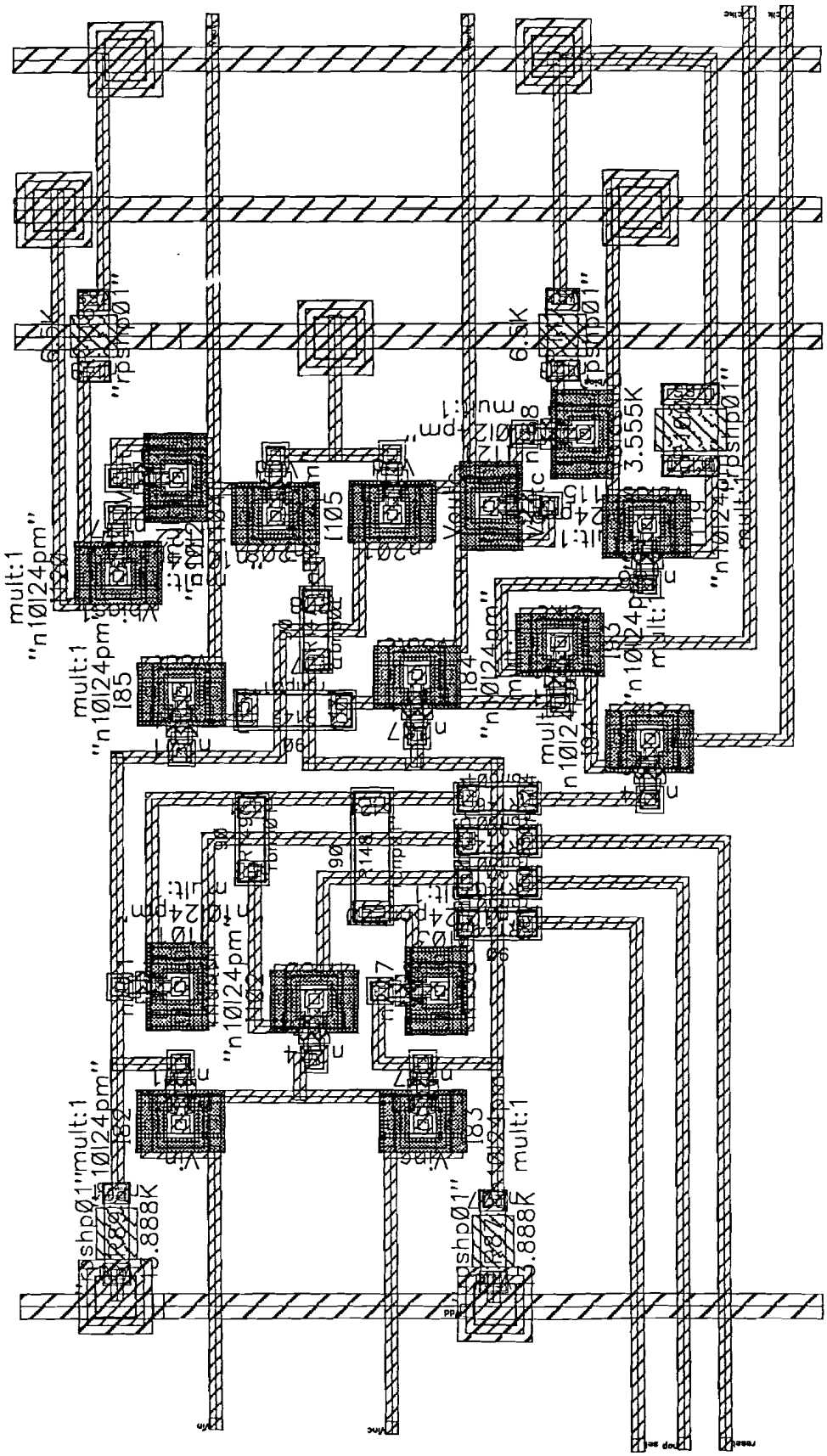
Lay-out latchsl: slave latch



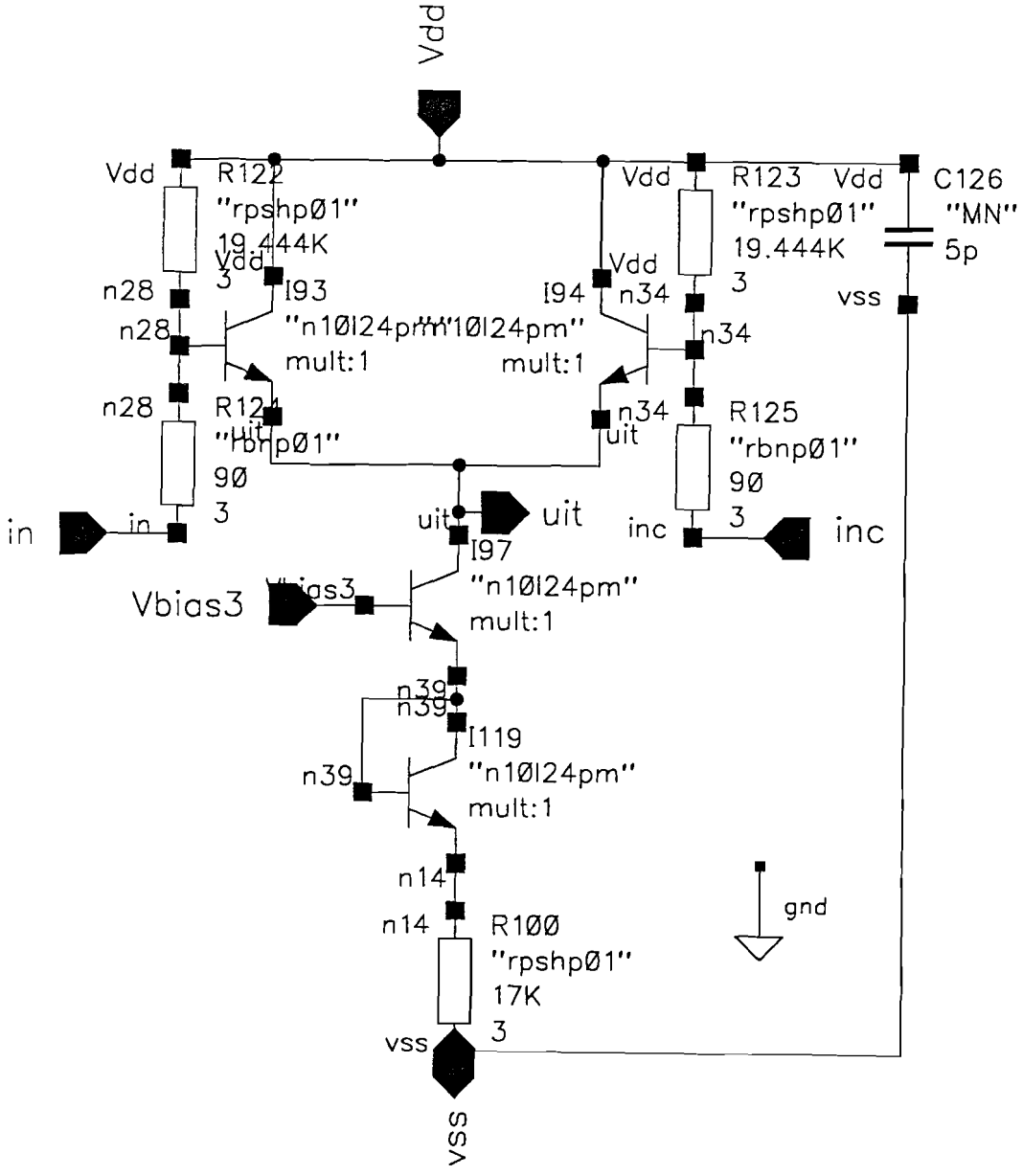
Schematic latchma: master latch



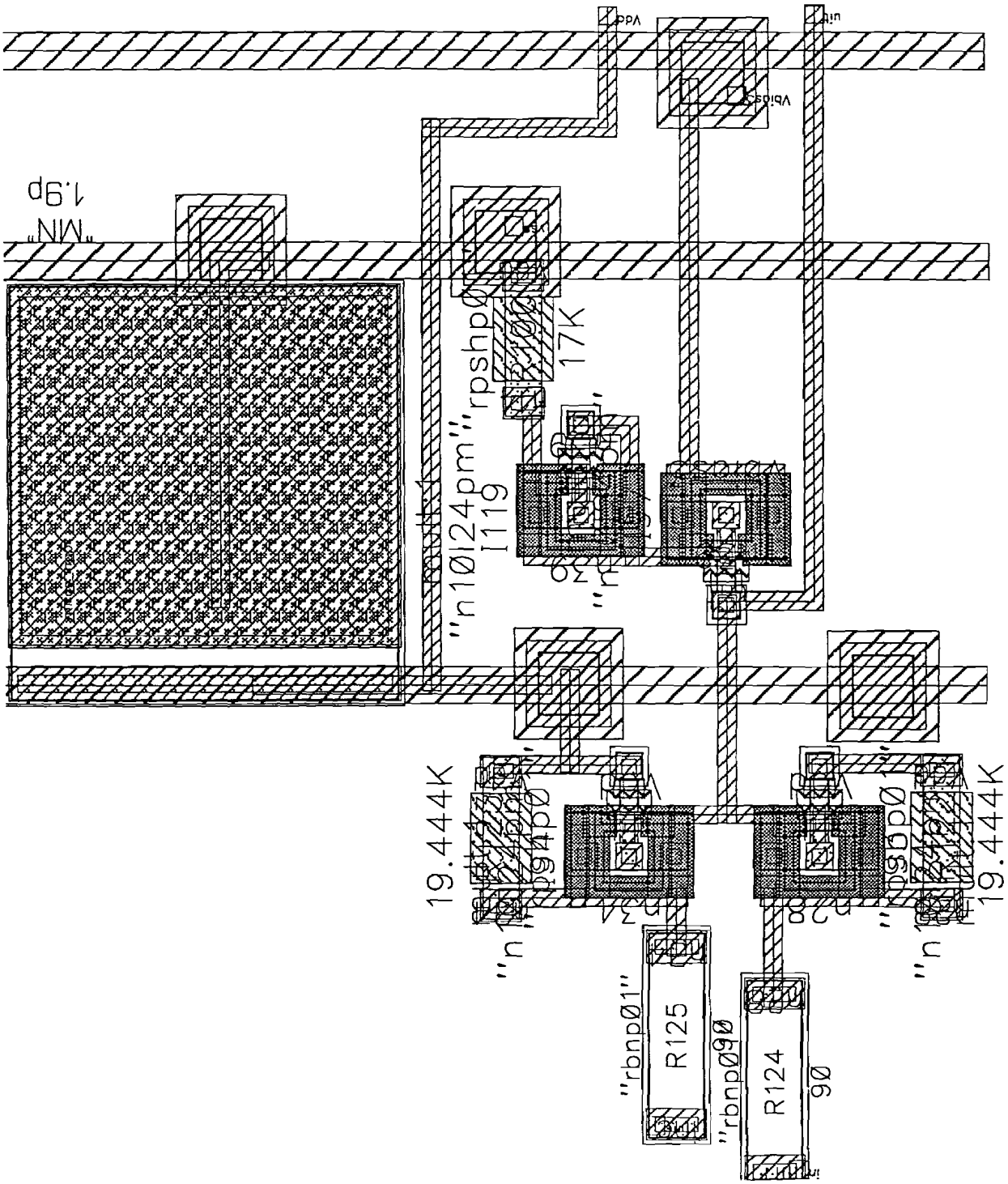
Lay-out latchma: master latch



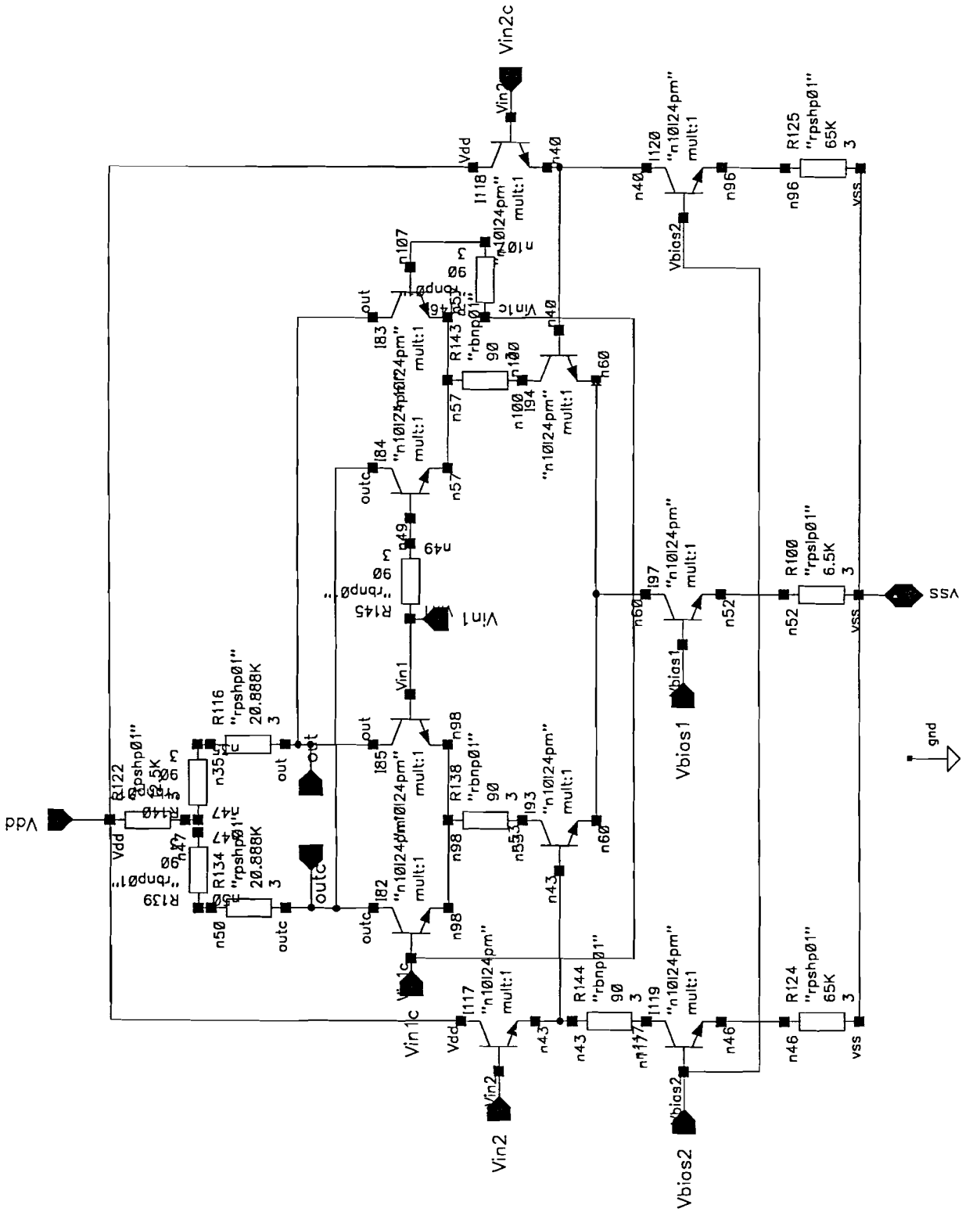
Schematic exorla: EXOR function fine part



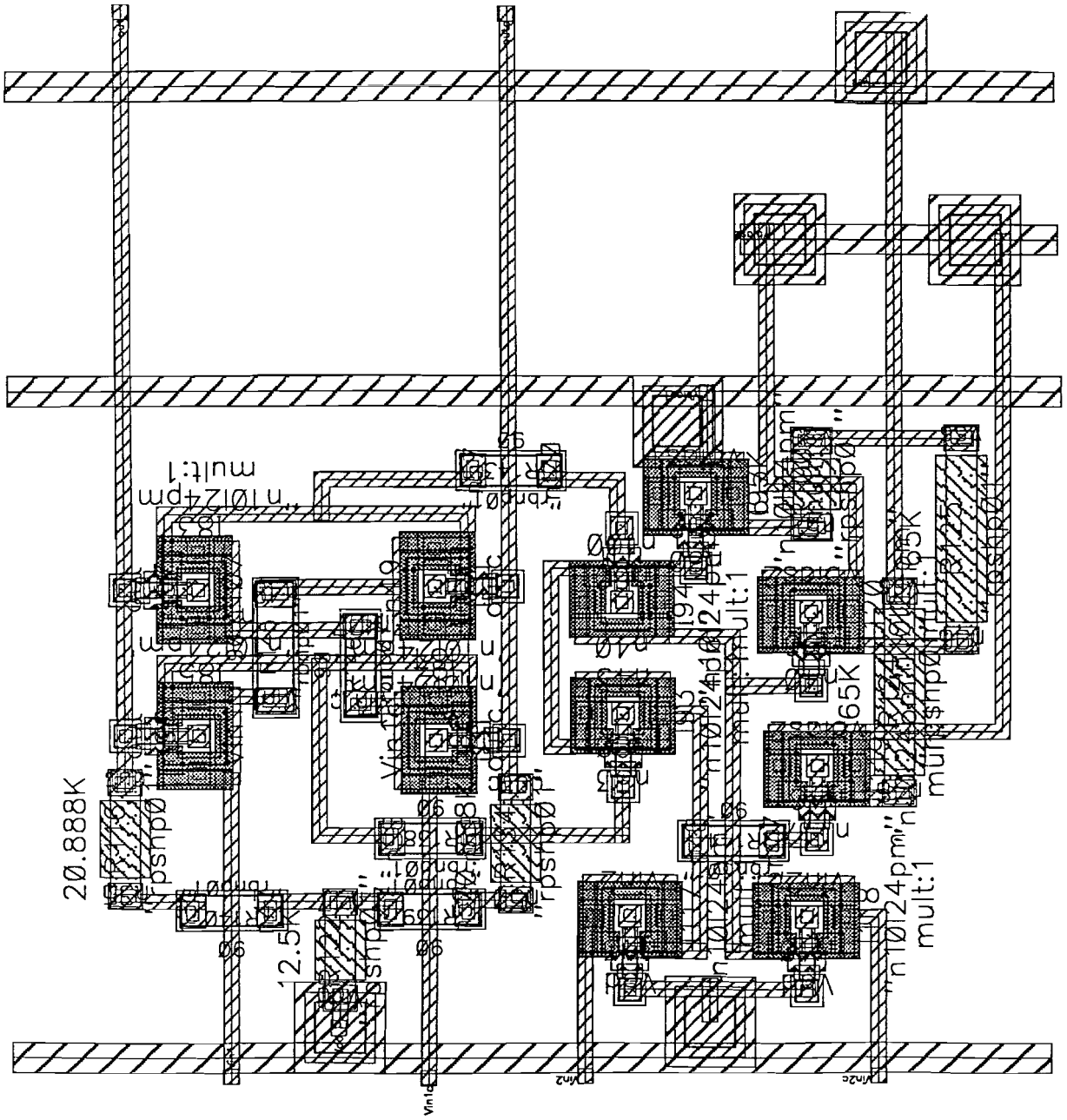
Lay-out exorla: EXOR function fine part



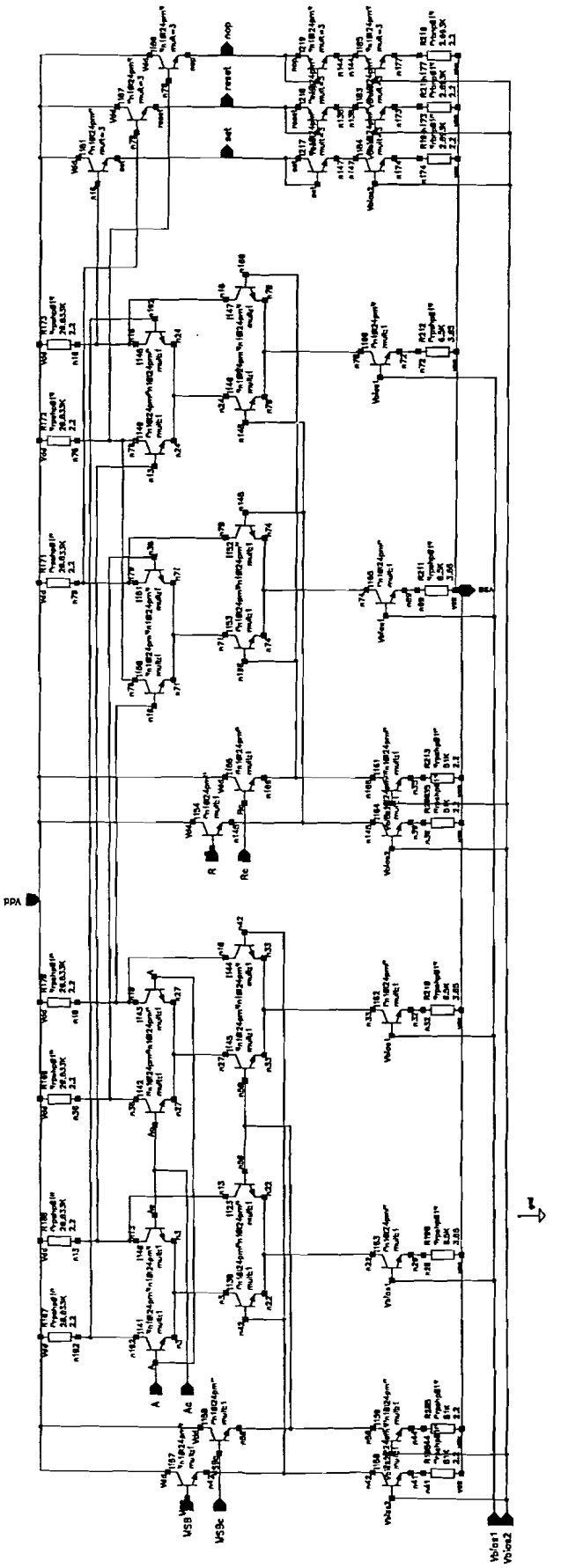
Schematic EXOR: EXOR circuit



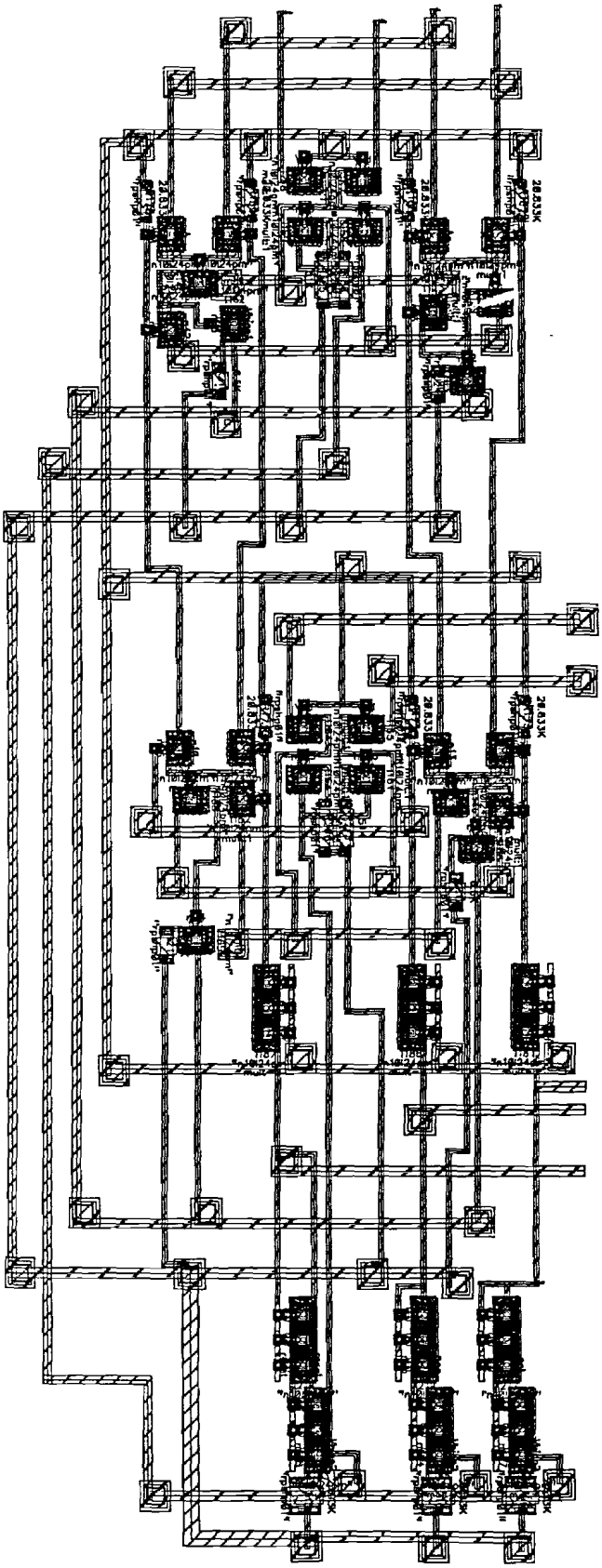
Lay-out EXOR: EXOR circuit



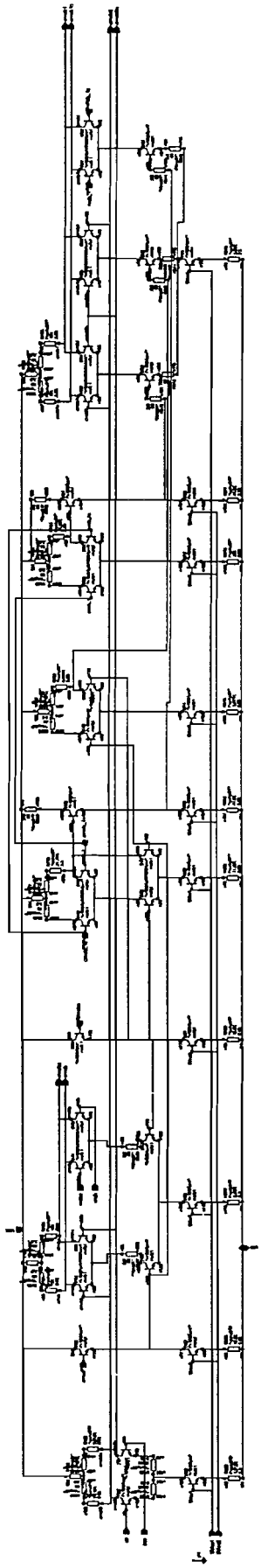
Schematic overfl: overflow circuit



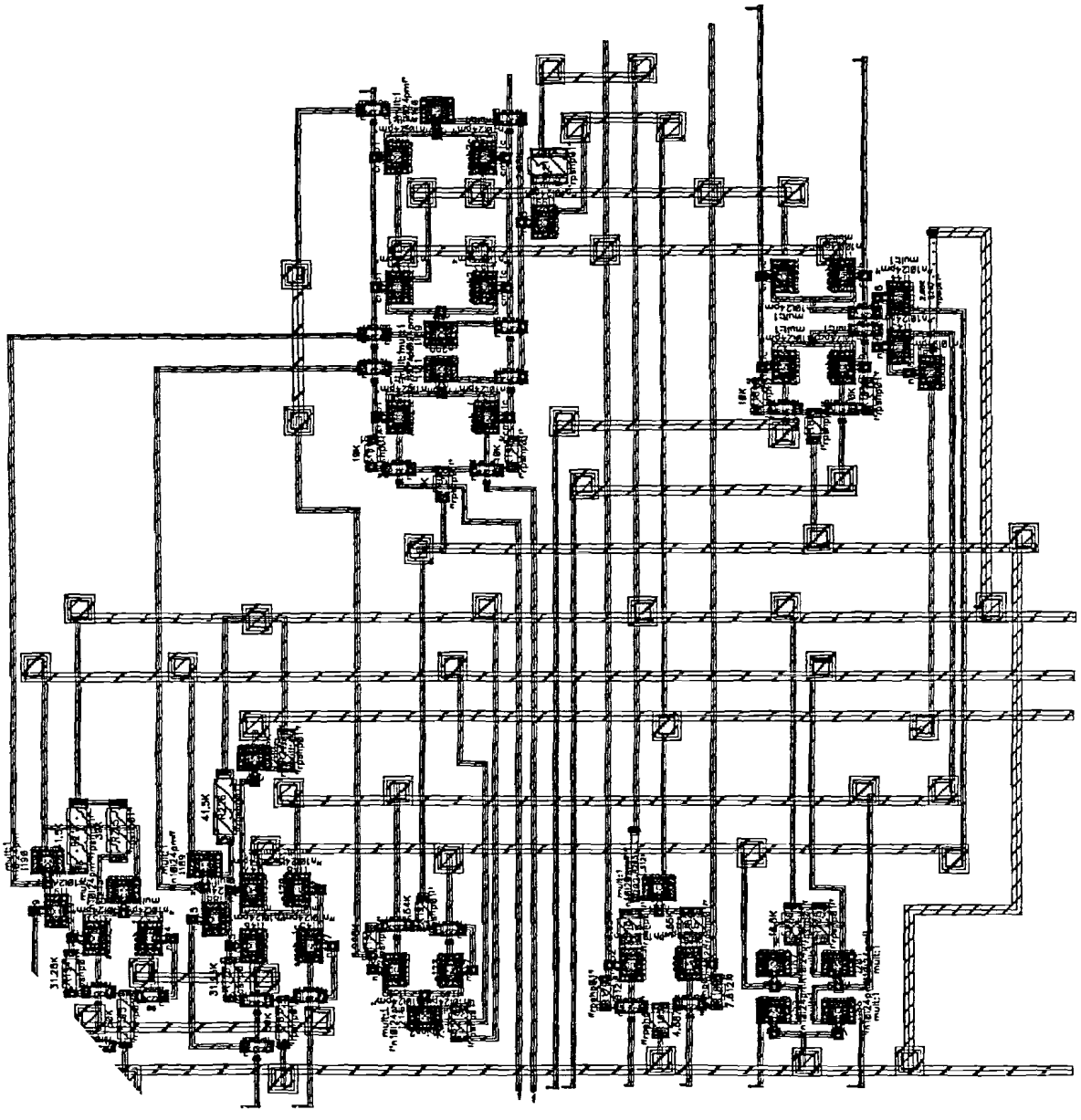
Lay-out overfl: overflow circuit



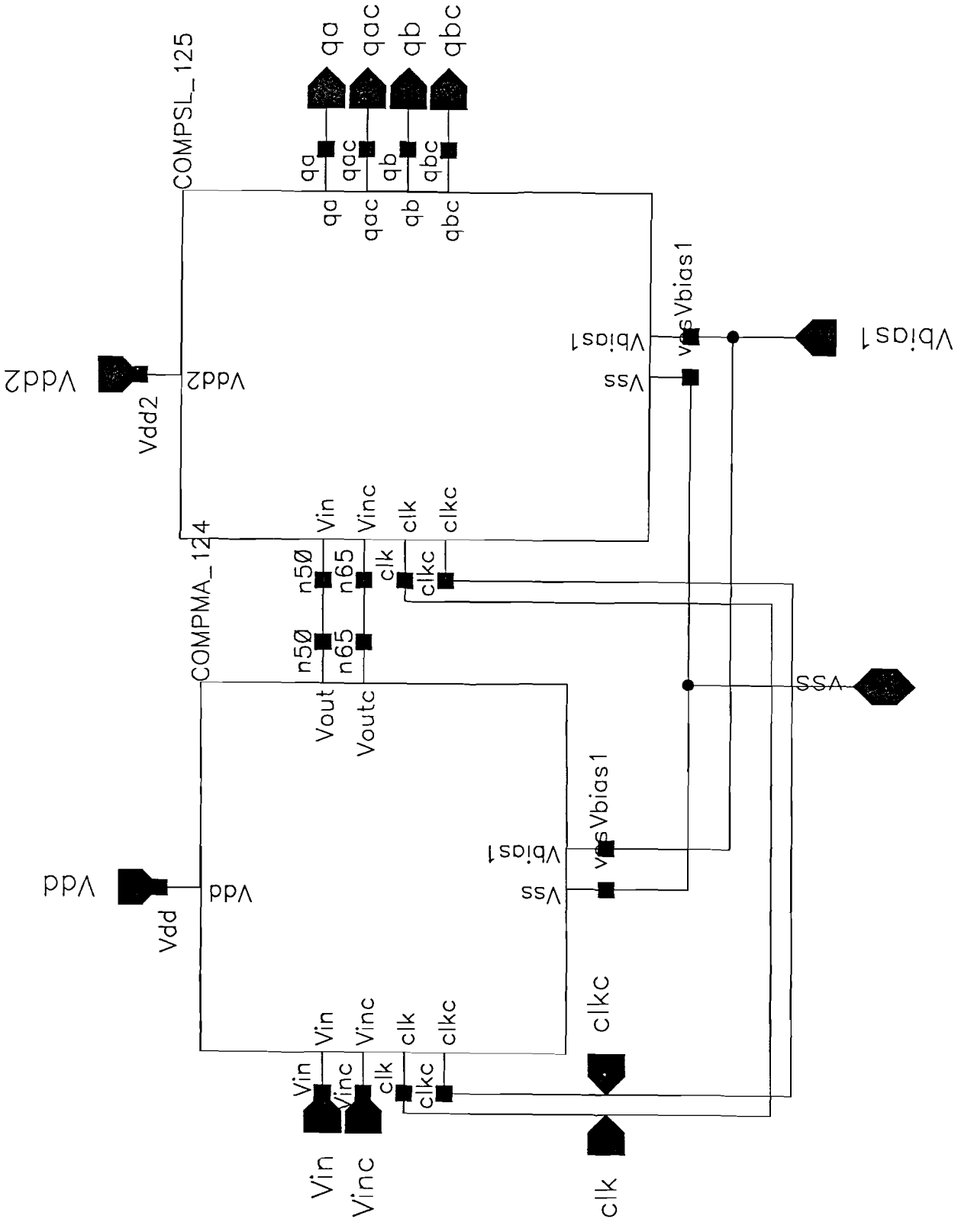
Schematic bitsync: bitsync circuit coarse part



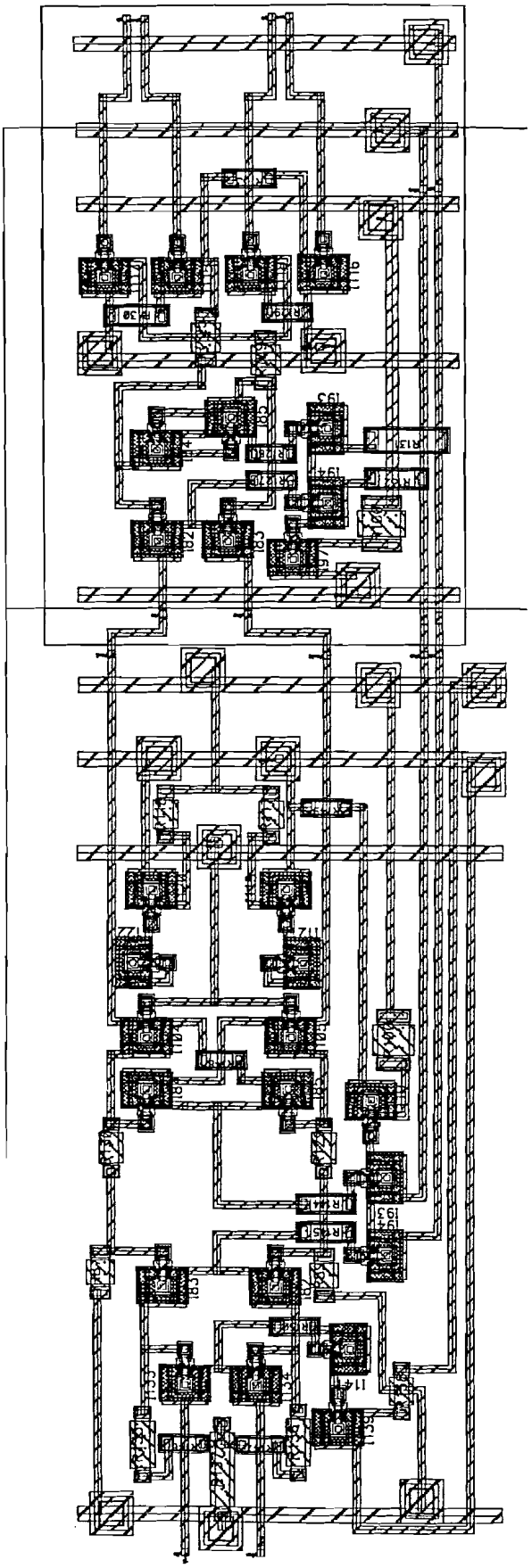
Lay-out bitsync: bitsync circuit coarse part



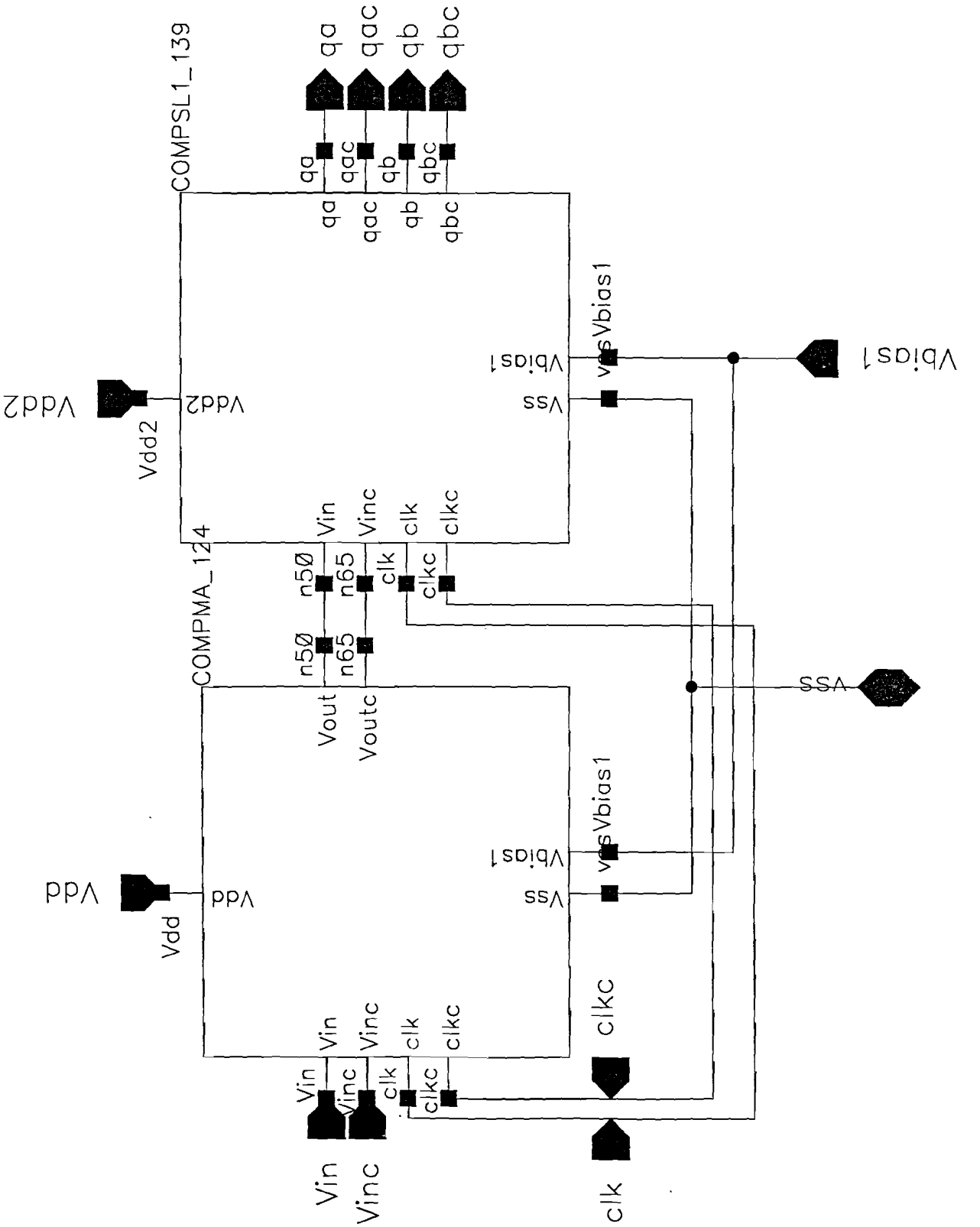
Schematic compa: master-slave comparator fine part



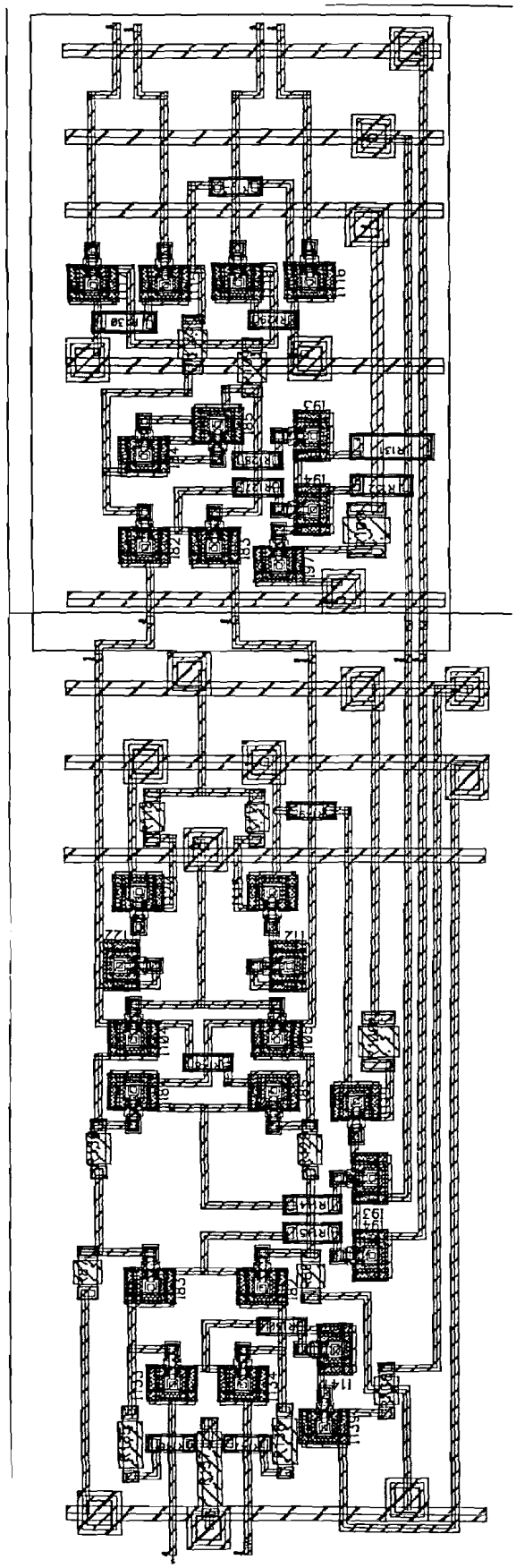
Lay-out compa: master-slave comparator fine part



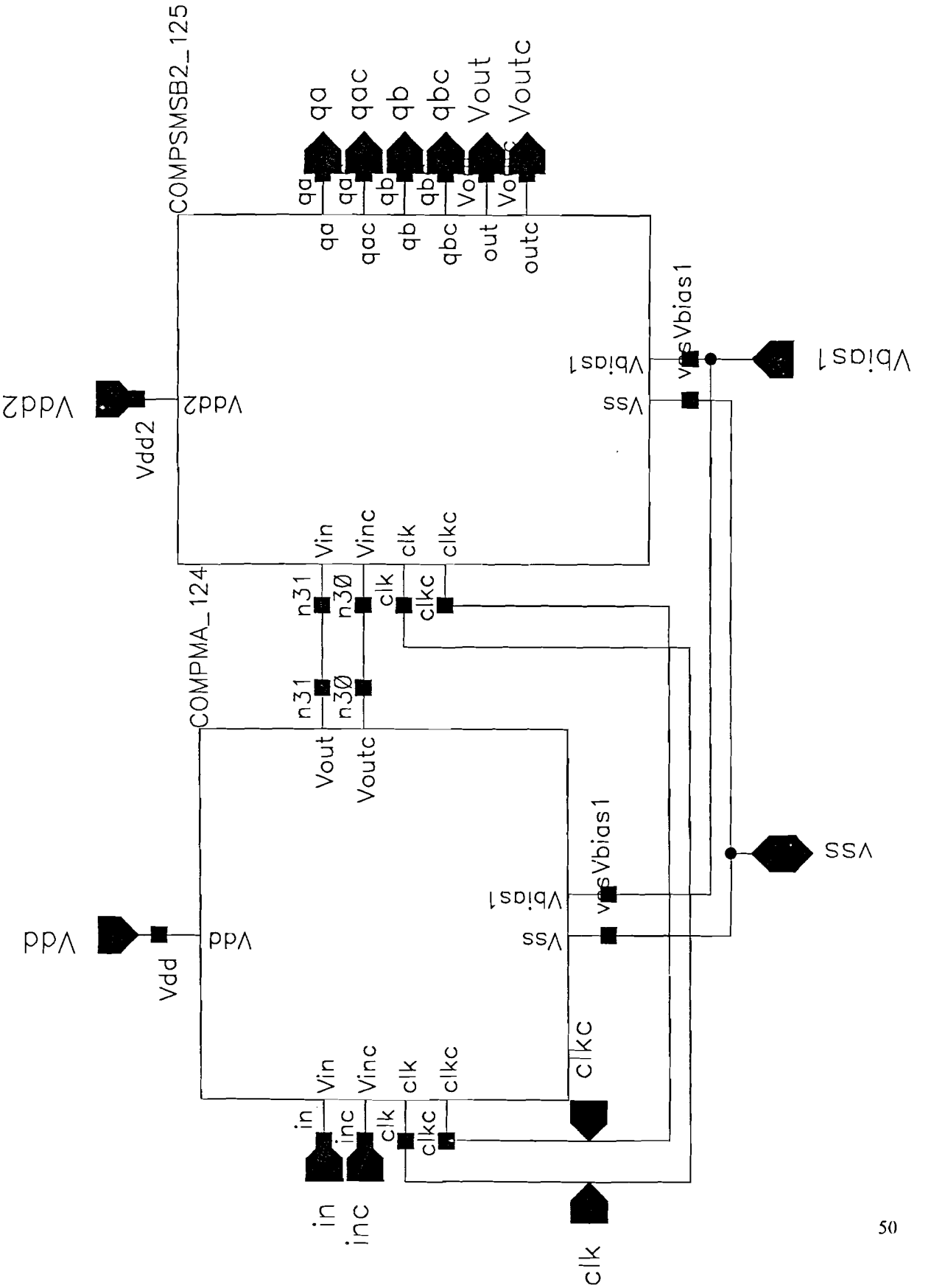
Schematic compa1: master-slave comparator fine part



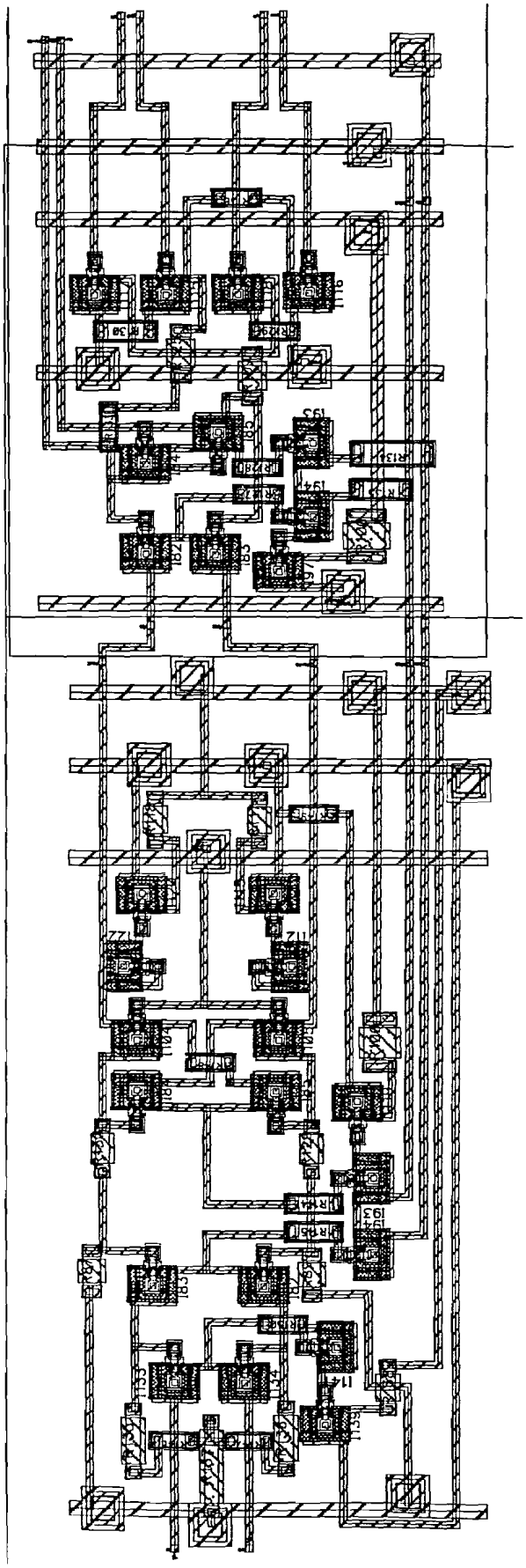
Lay-out compa1: master-slave comparator fine part



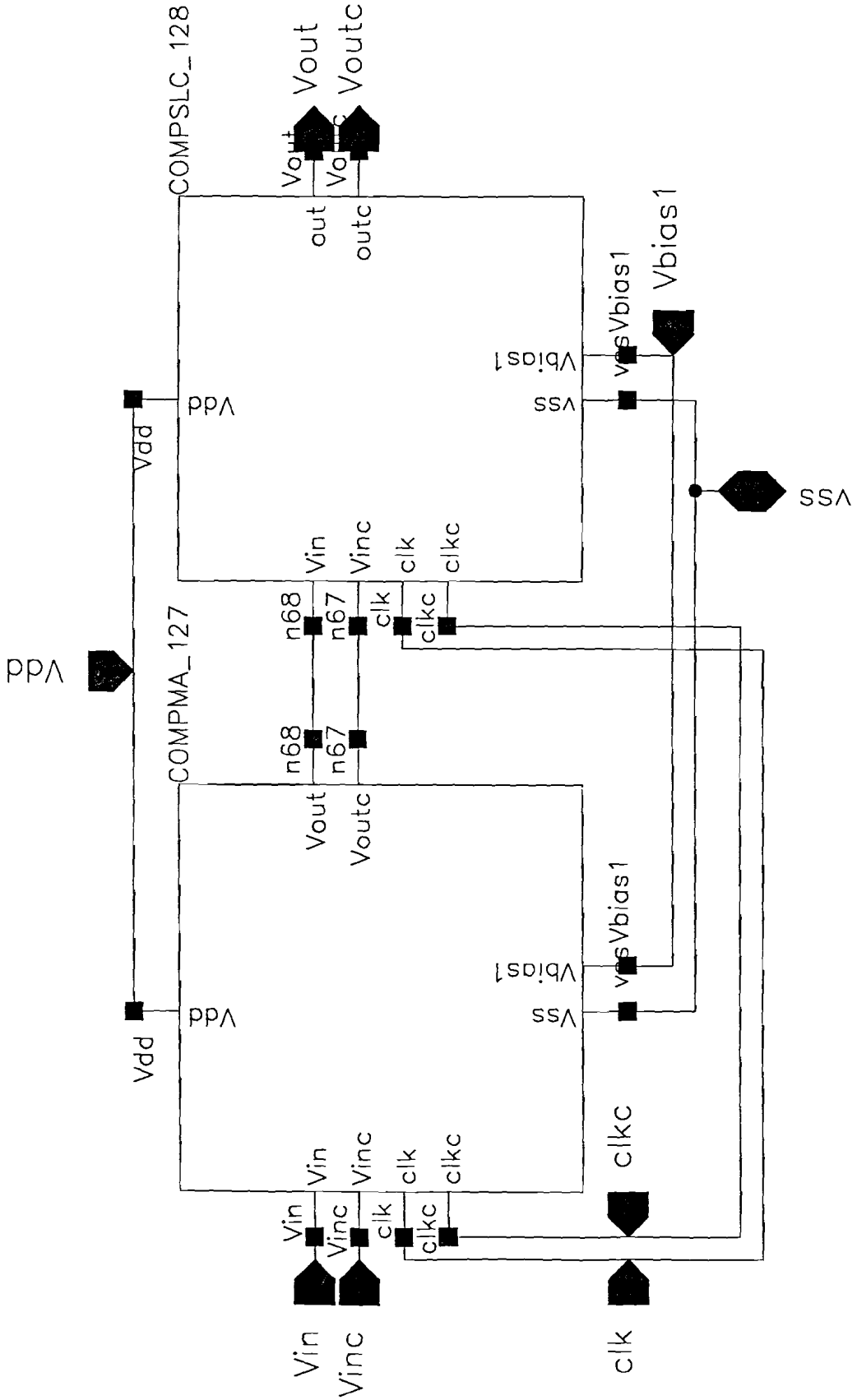
Schematic compamsb2: master-slave comparator msb-2 signal fine part



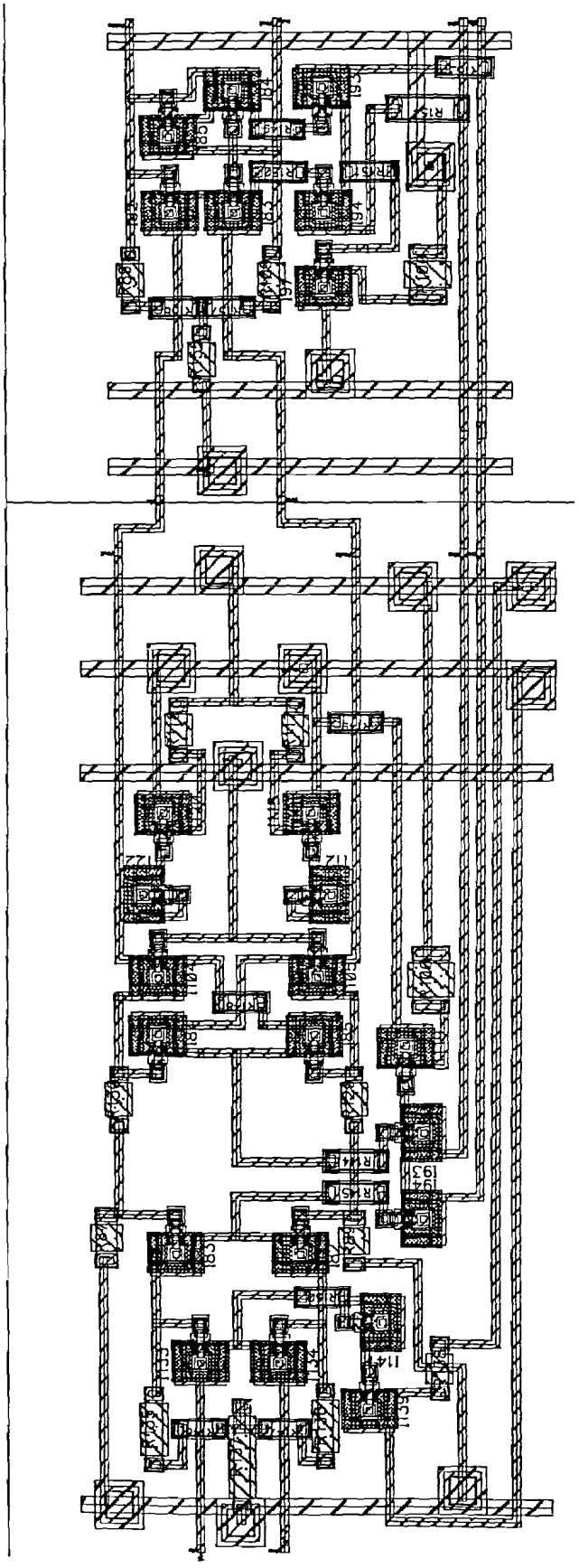
Lay-out compamsb2: master-slave comparator msb-2 signal fine part



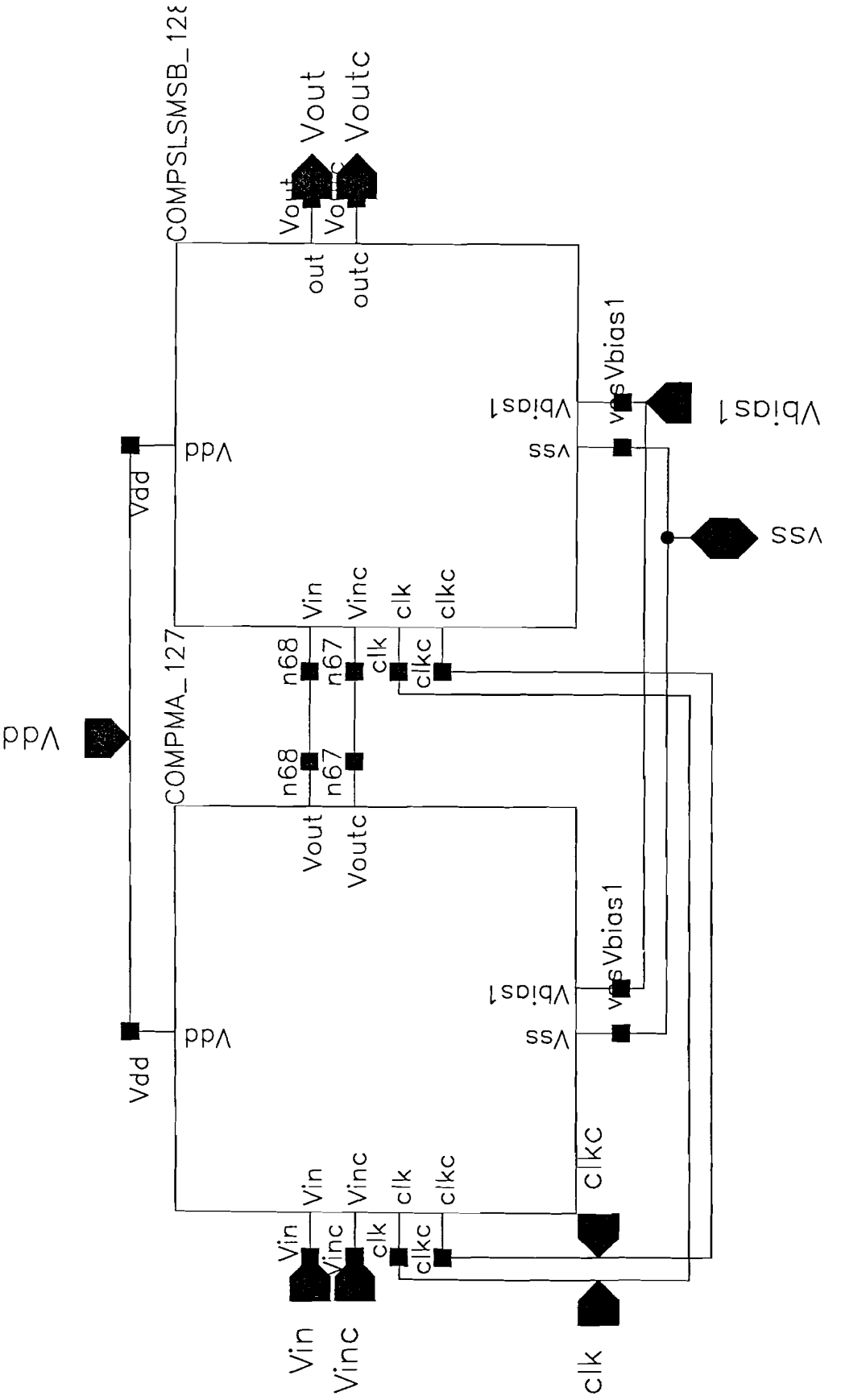
Schematic comcoarse1: master-slave comparator coarse part



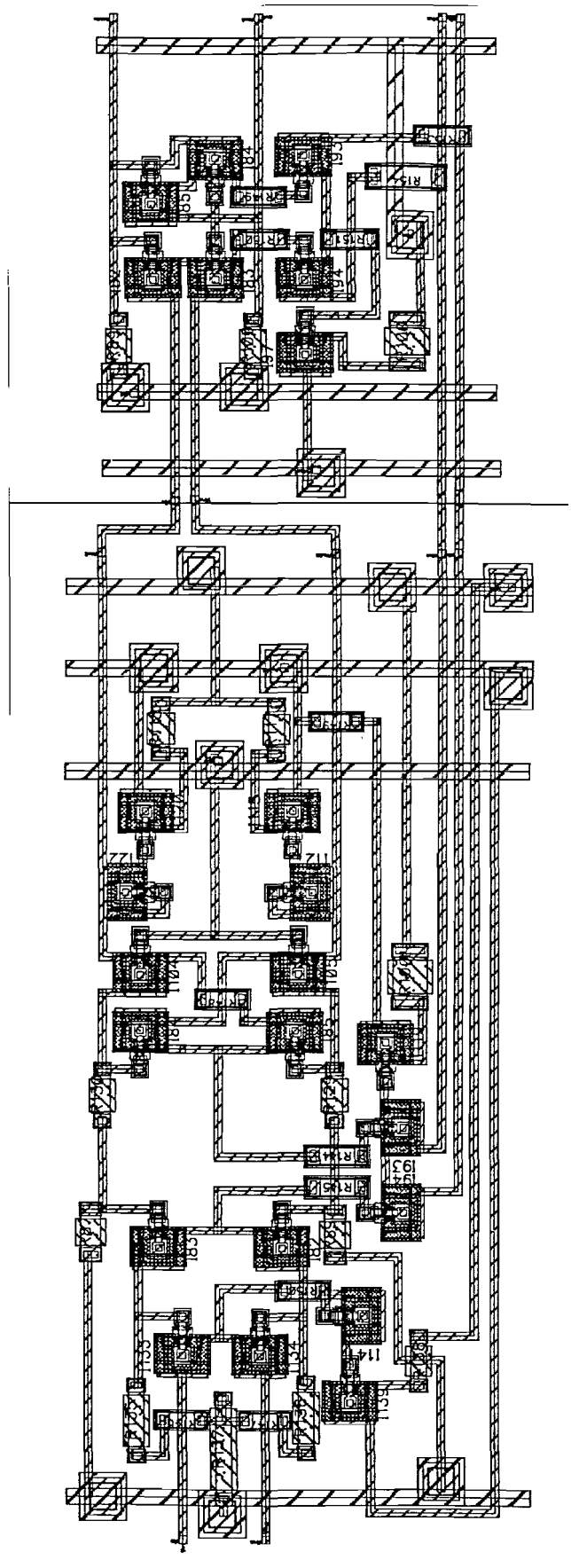
Lay-out comcoarse1: master-slave comparator coarse part



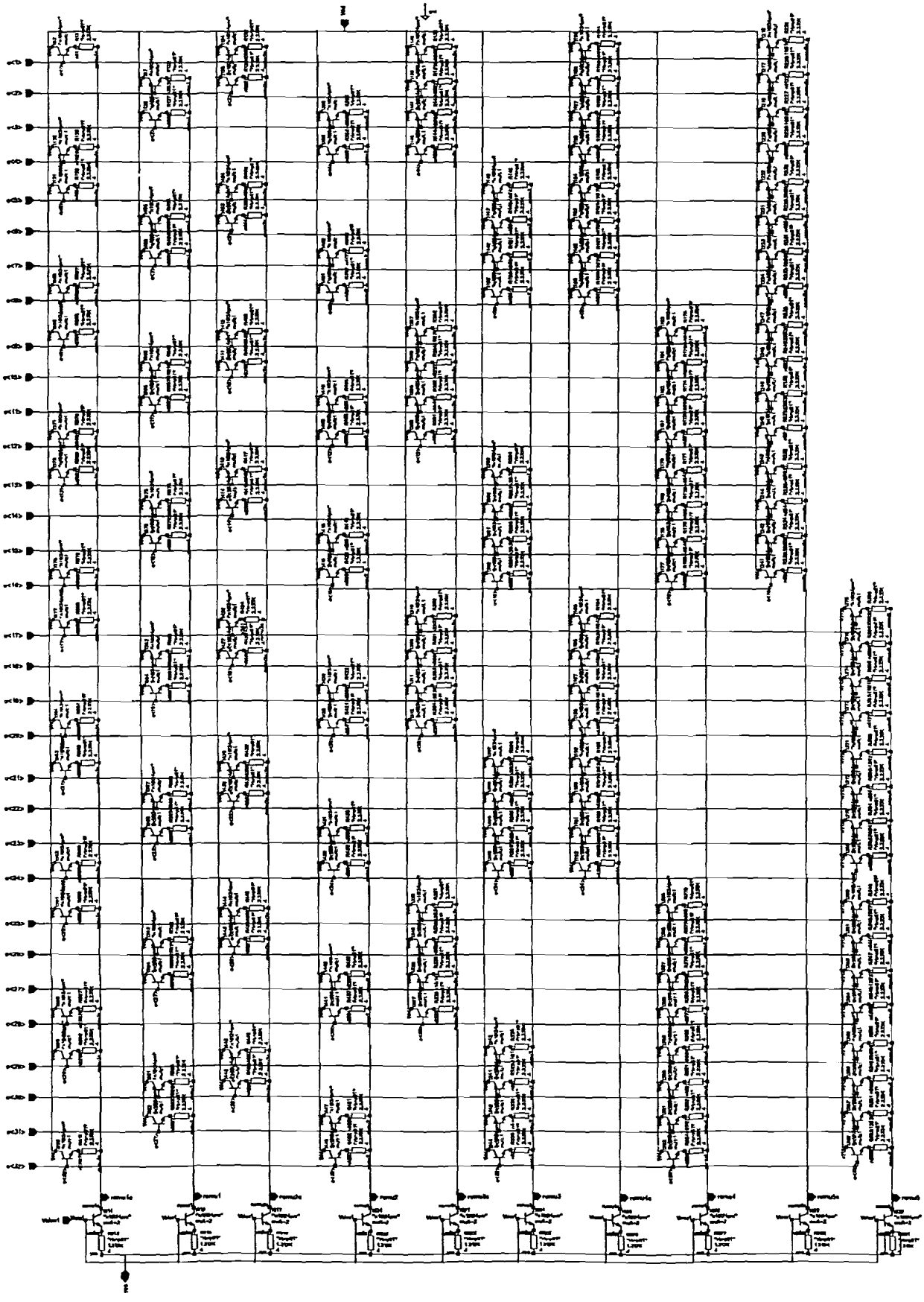
Schematic compcoarse2: master-slave comparator smsb signal coarse part



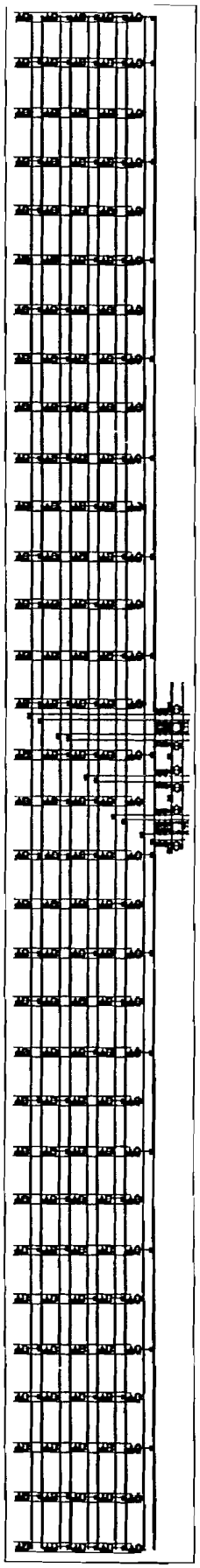
Lay-out compcoarse2: master-slave comparator smsb signal coarse part



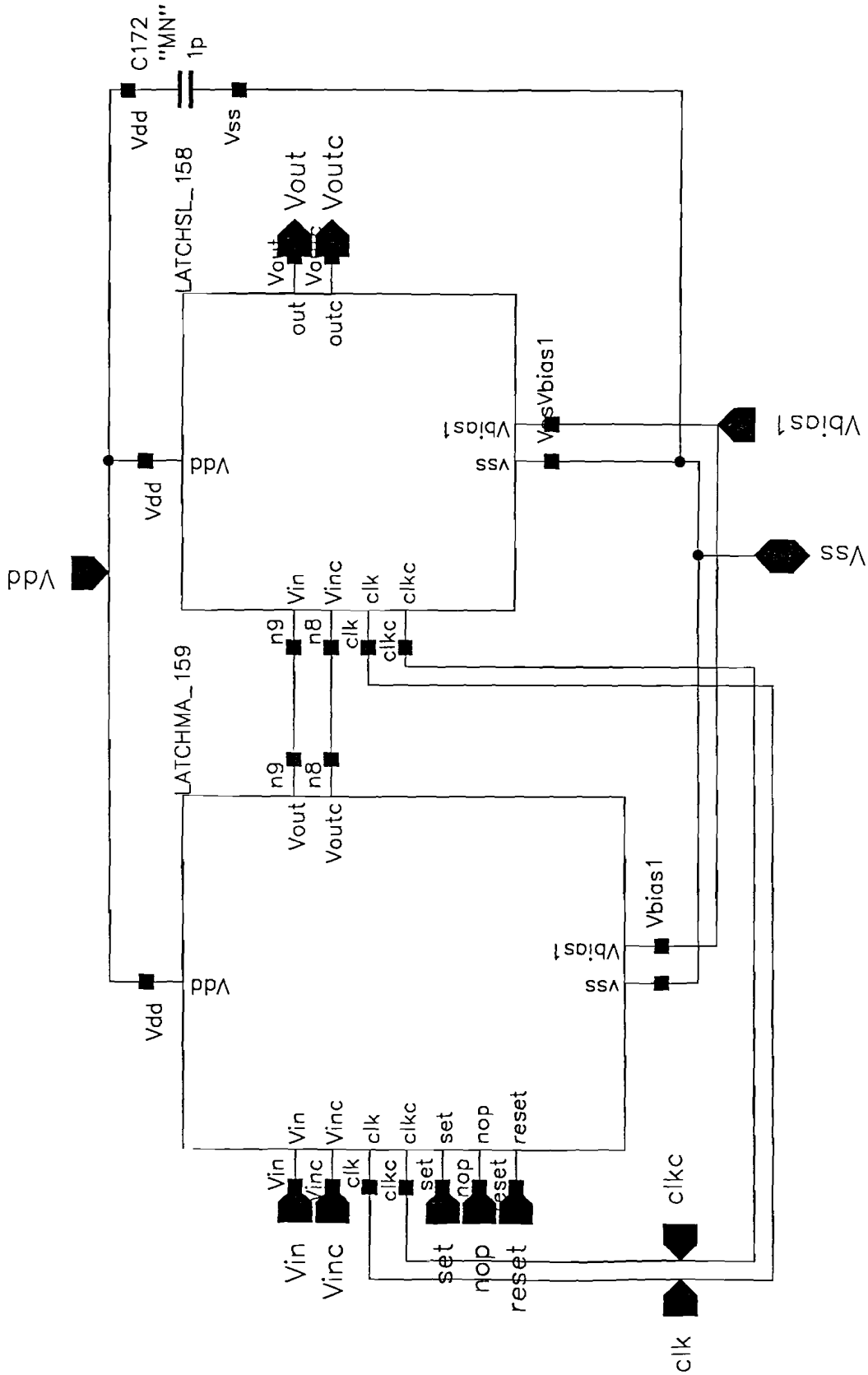
Schematic romtab: decode table fine part



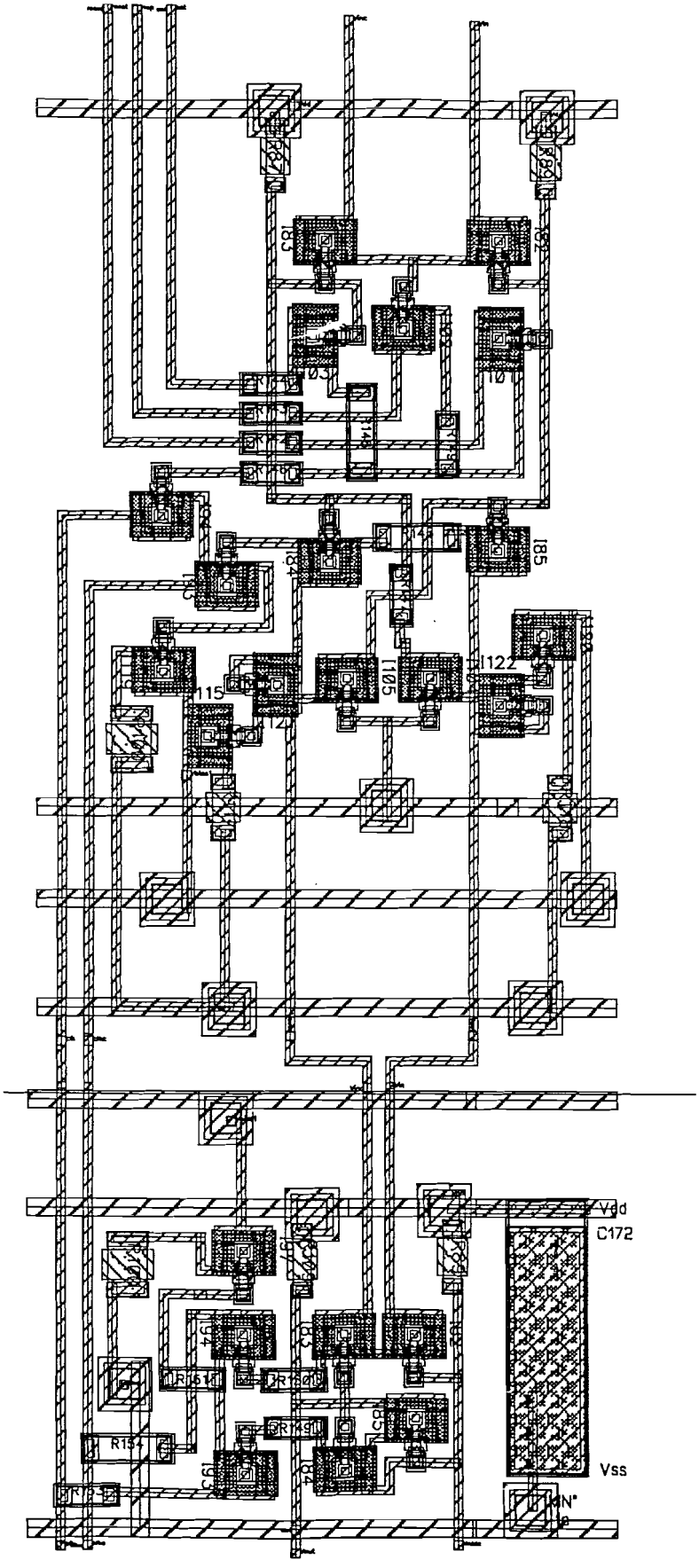
Lay-out romtab: decode table fine part



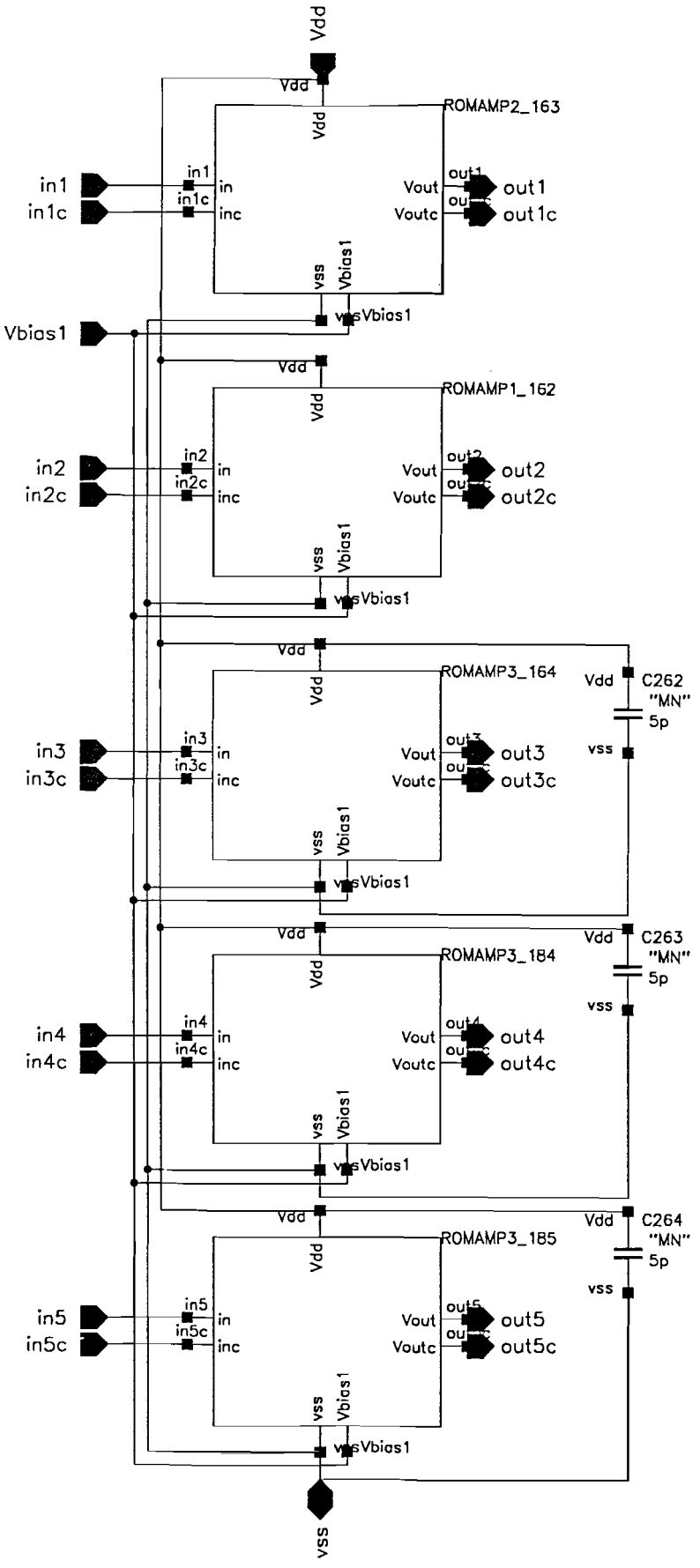
Schematic latch: master-slave latch



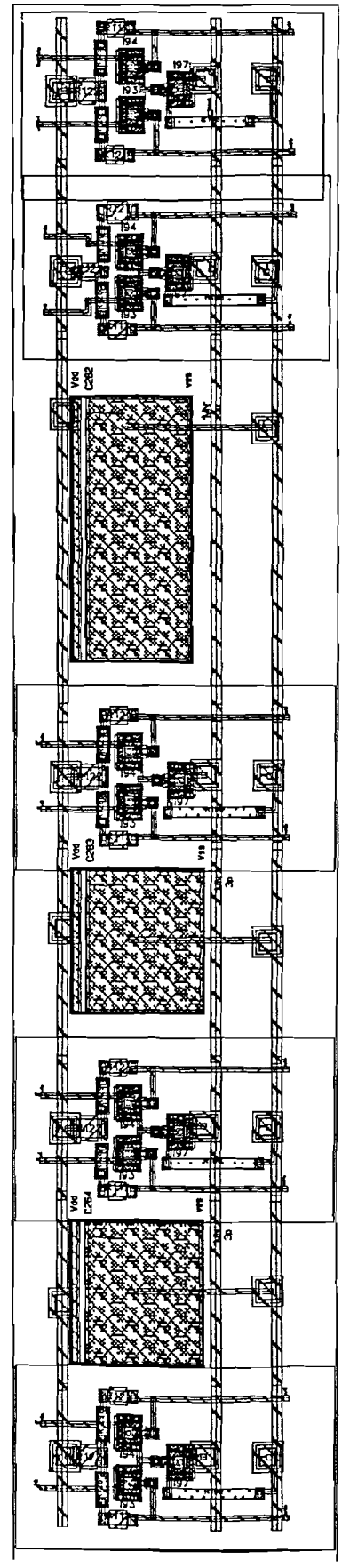
Lay-out latch: master-slave latch



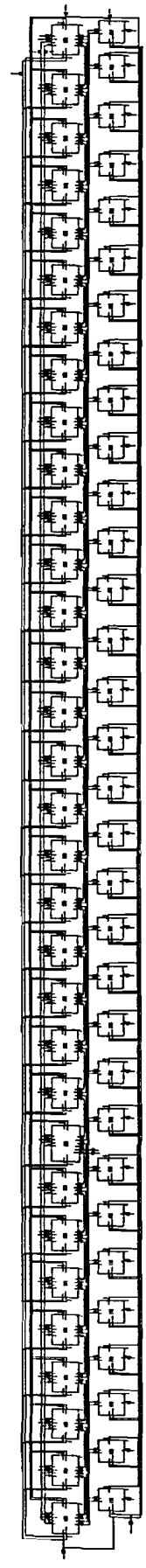
Schematic romtot: total rom table differential amplifiers



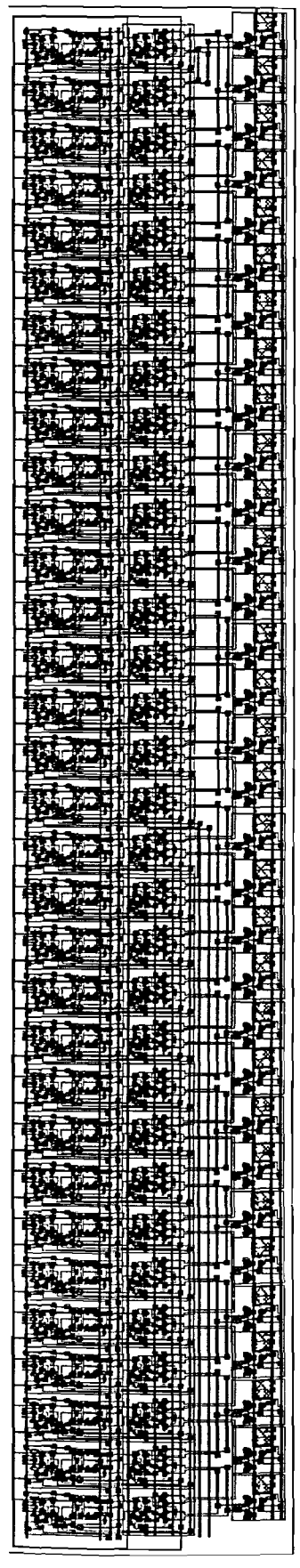
Lay-out romtot: total rom table differential amplifiers



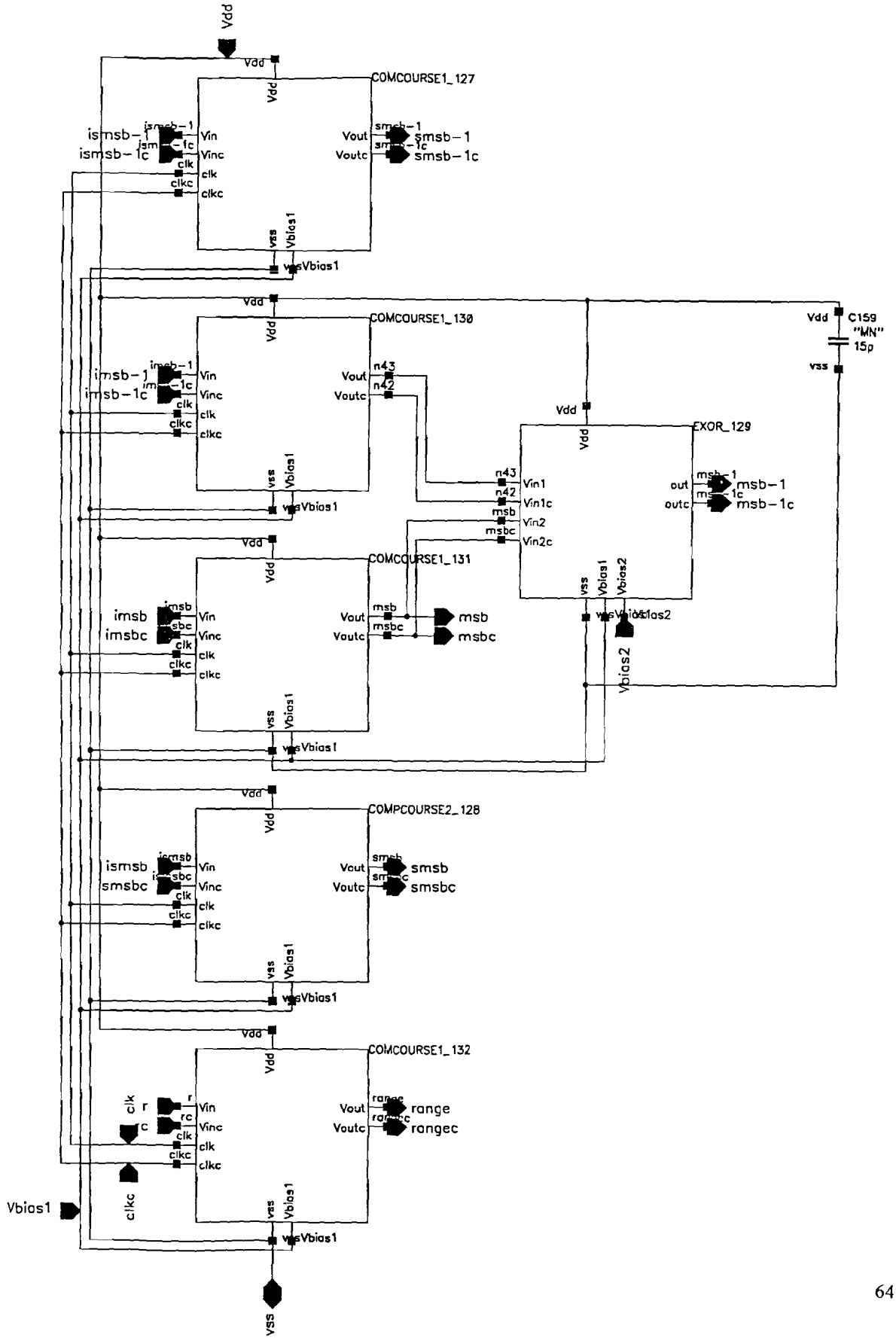
Schematic comptot: total comparator fine part



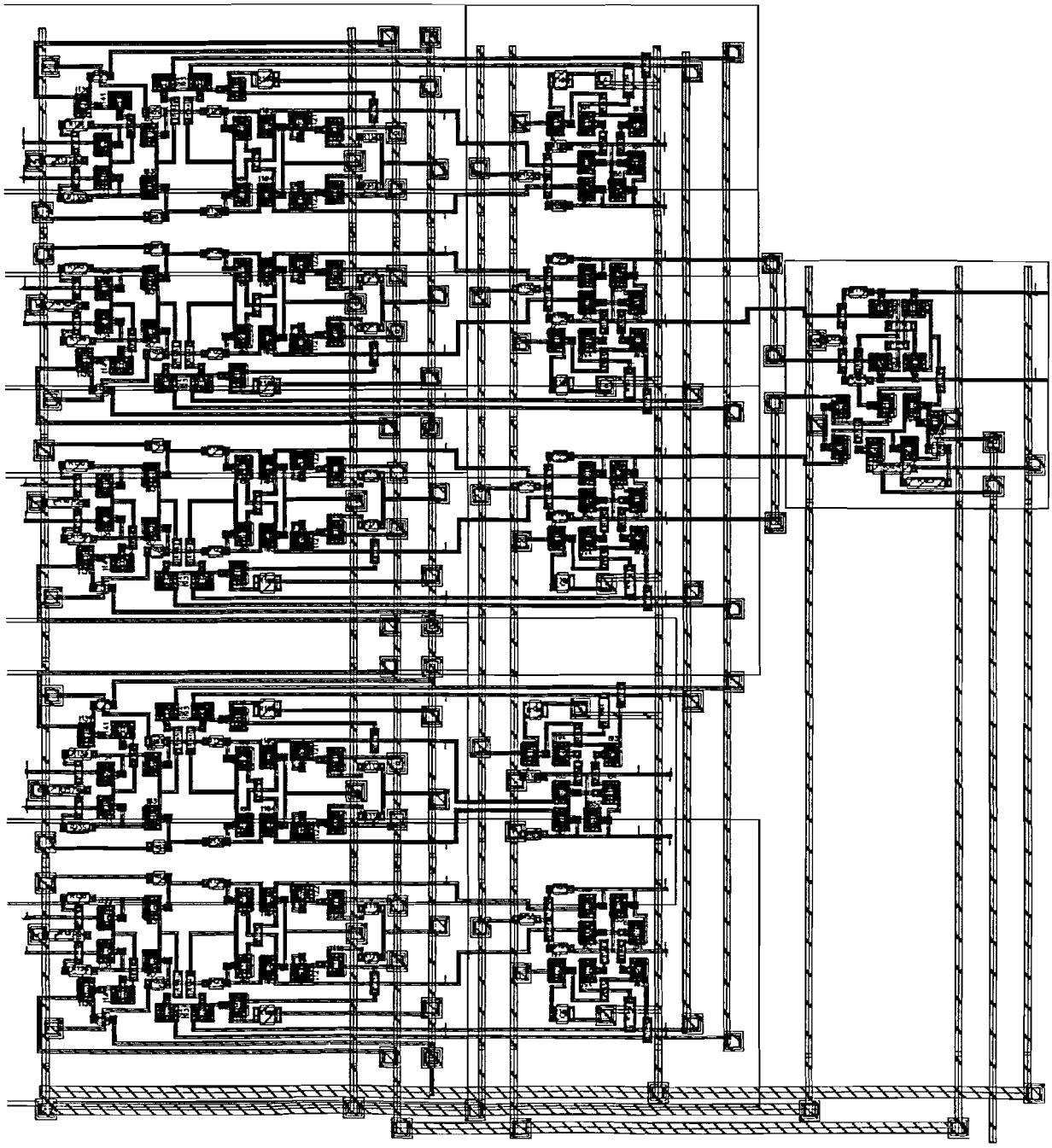
Lay-out comptot: total comparator fine part



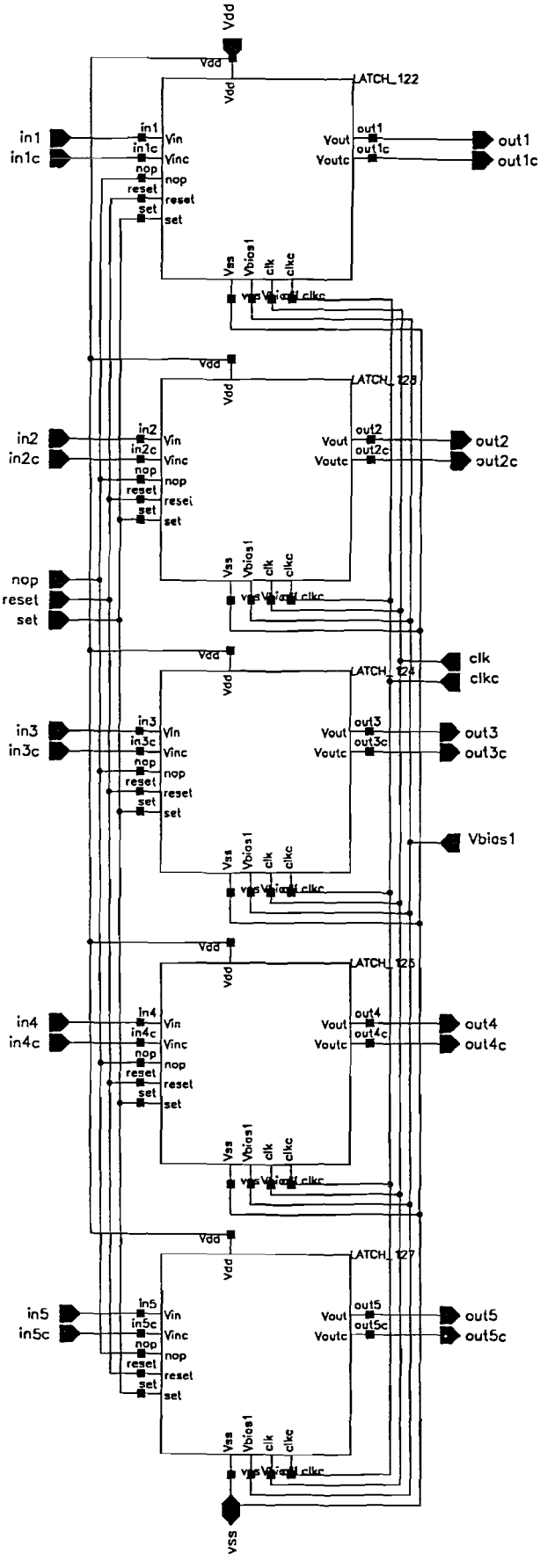
Schematic comptotc: total comparator coarse part



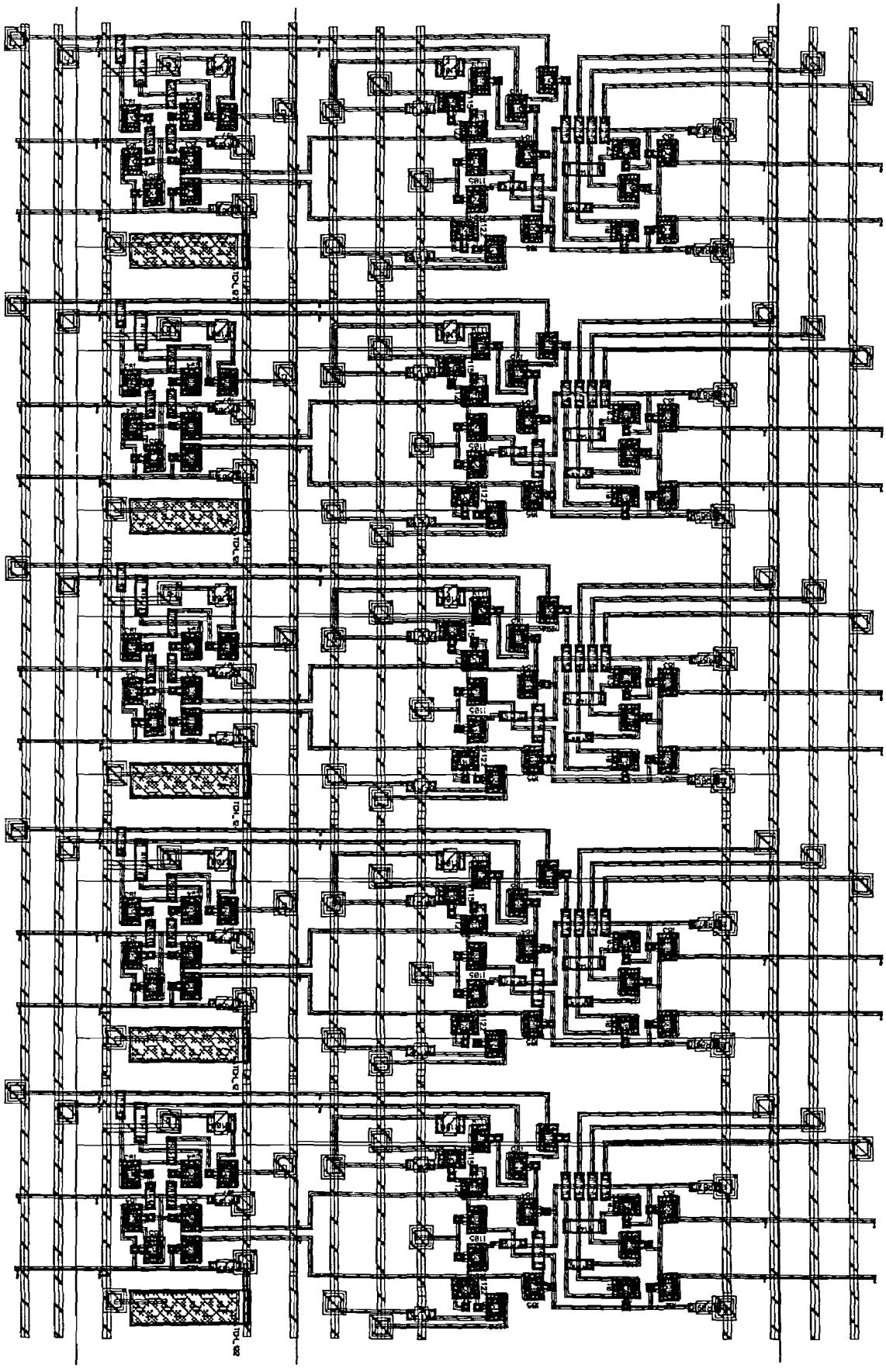
Lay-out comptotc: total comparator coarse part



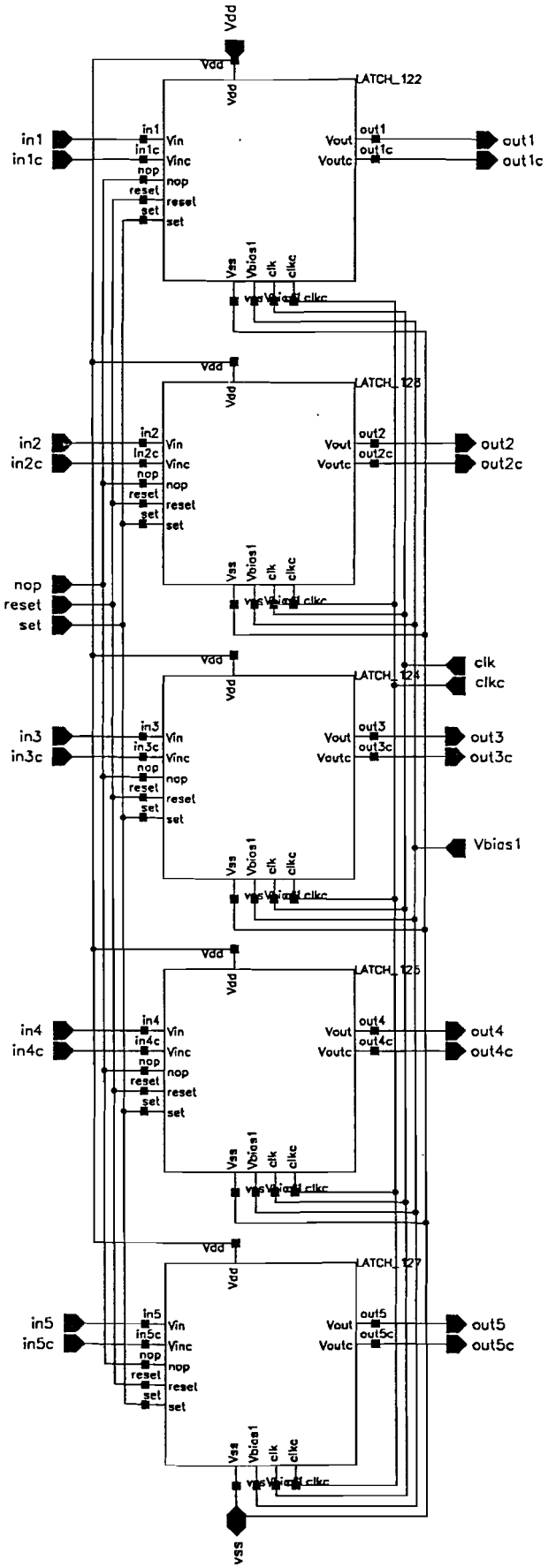
Schematic latchtot: total latch fine part



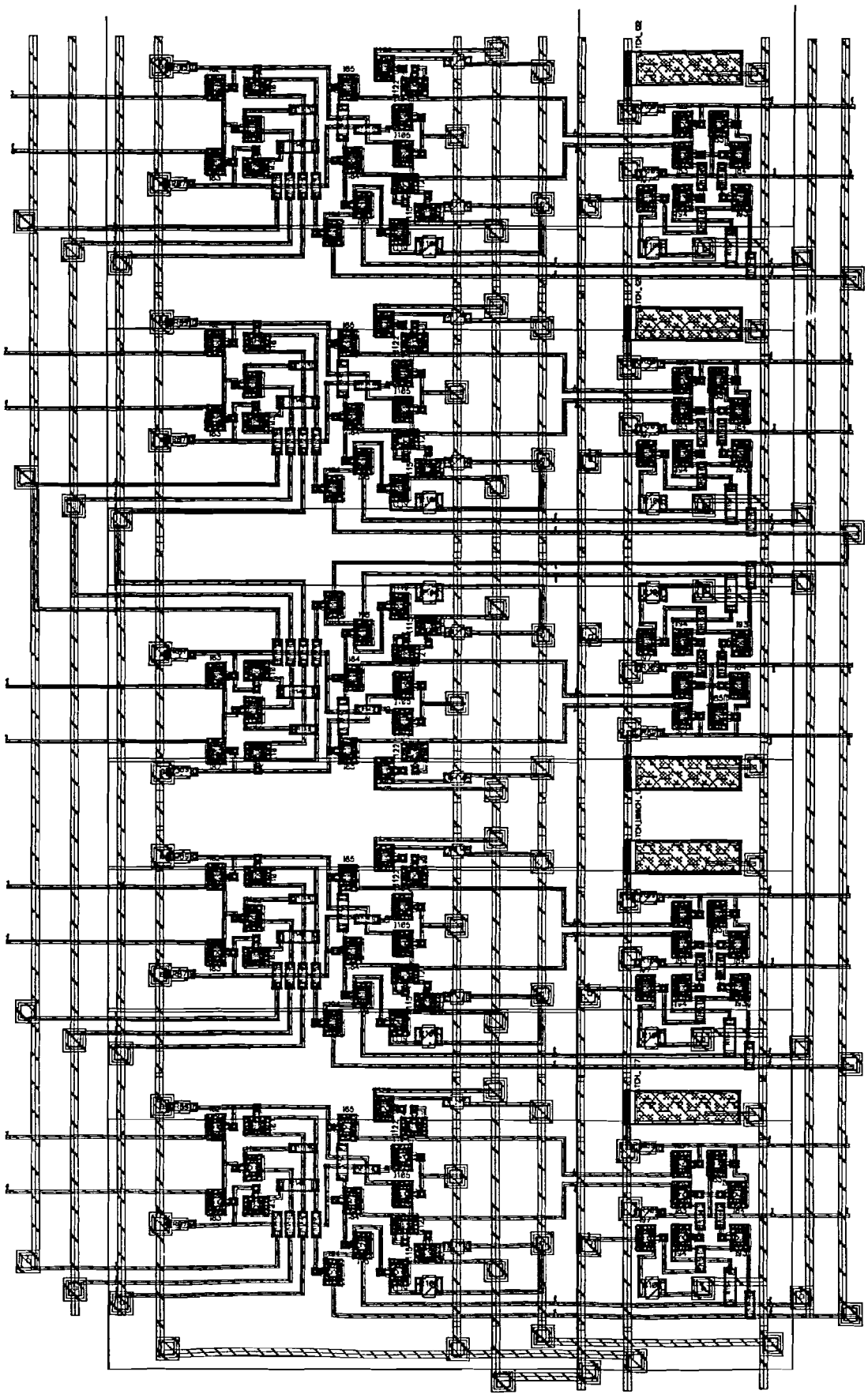
Lay-out latchtot: total latch fine part



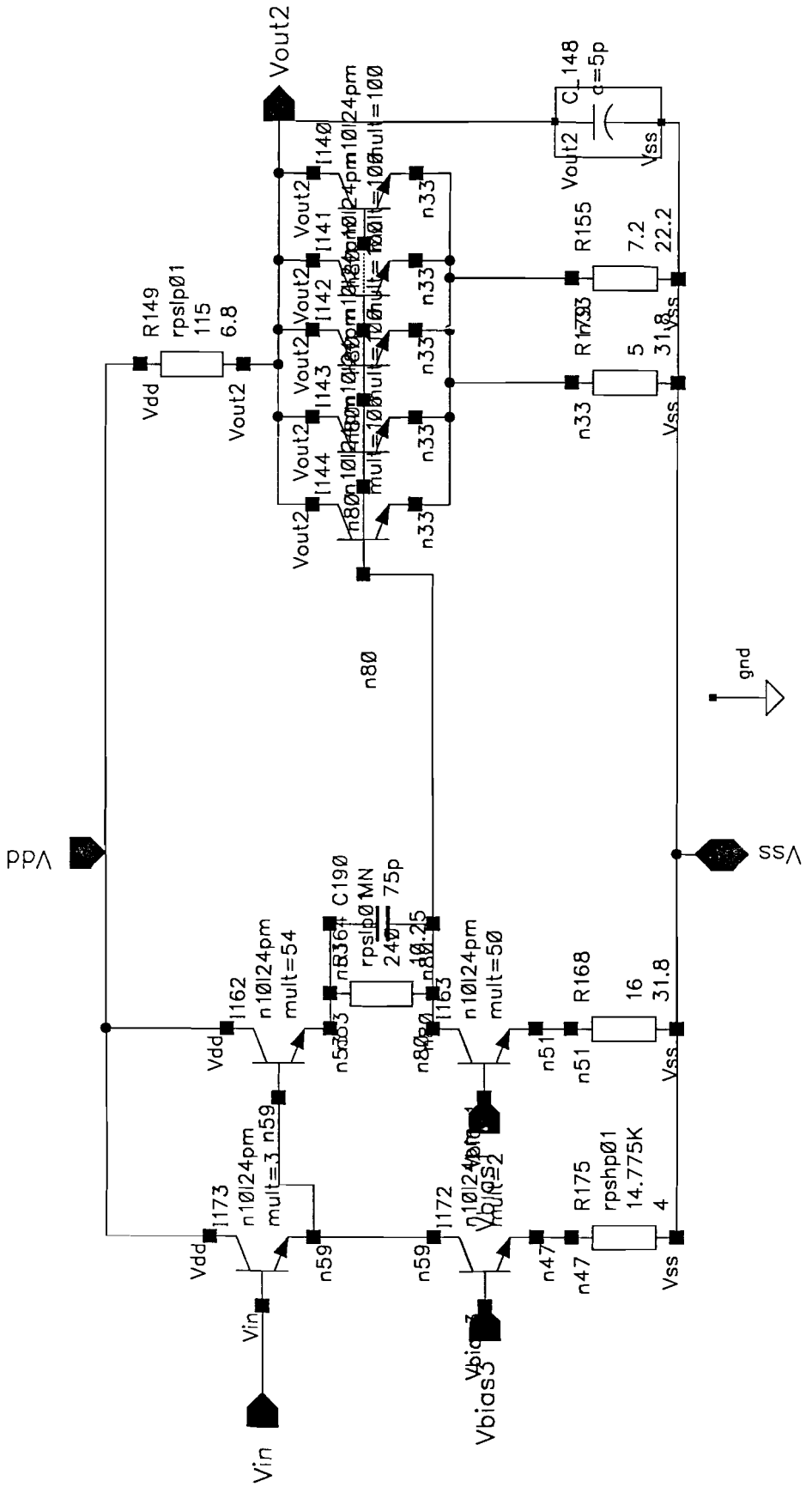
Schematic latchtotc: total latch coarse part



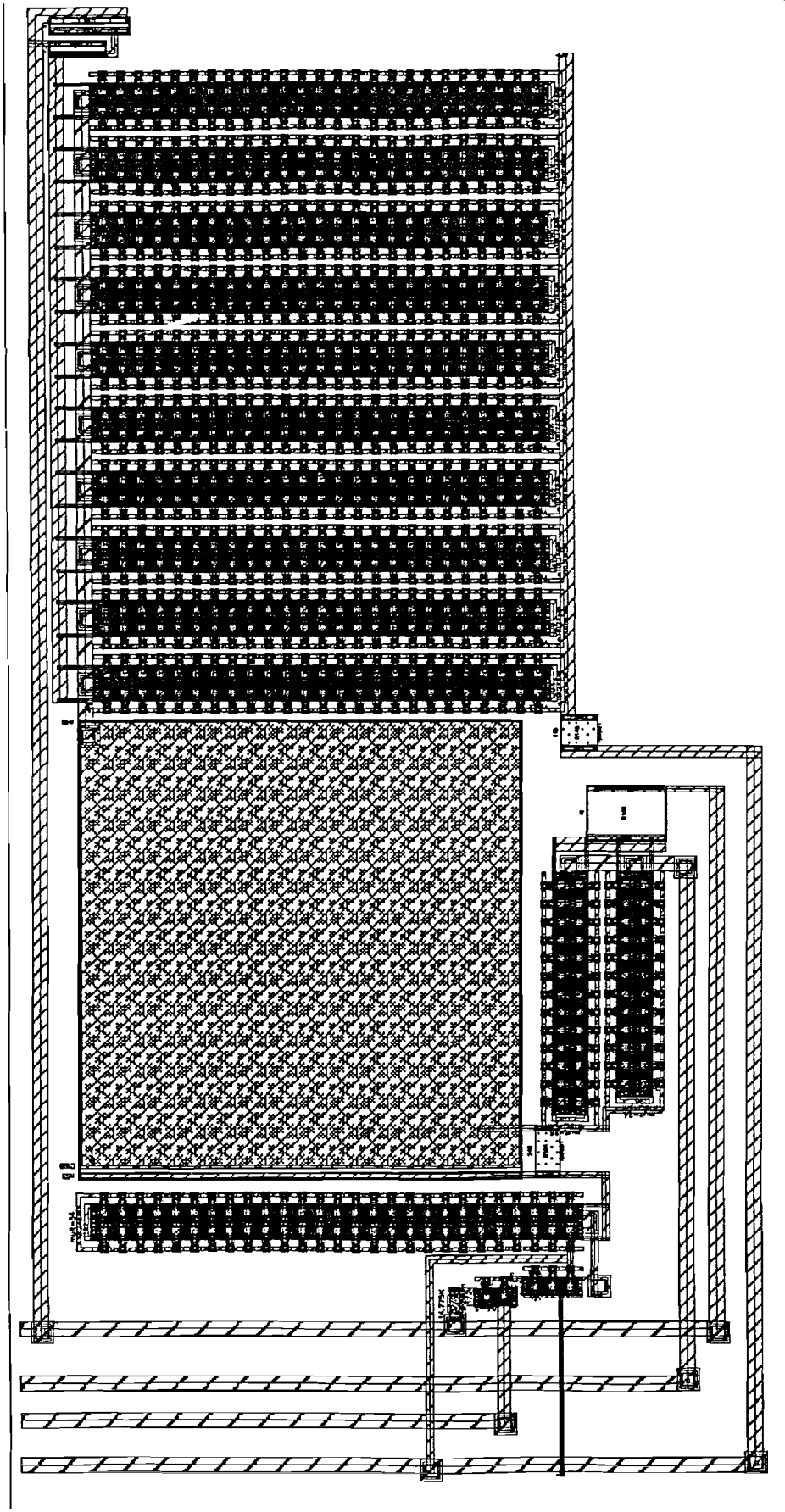
Lay-out latchtotc: total latch coarse part



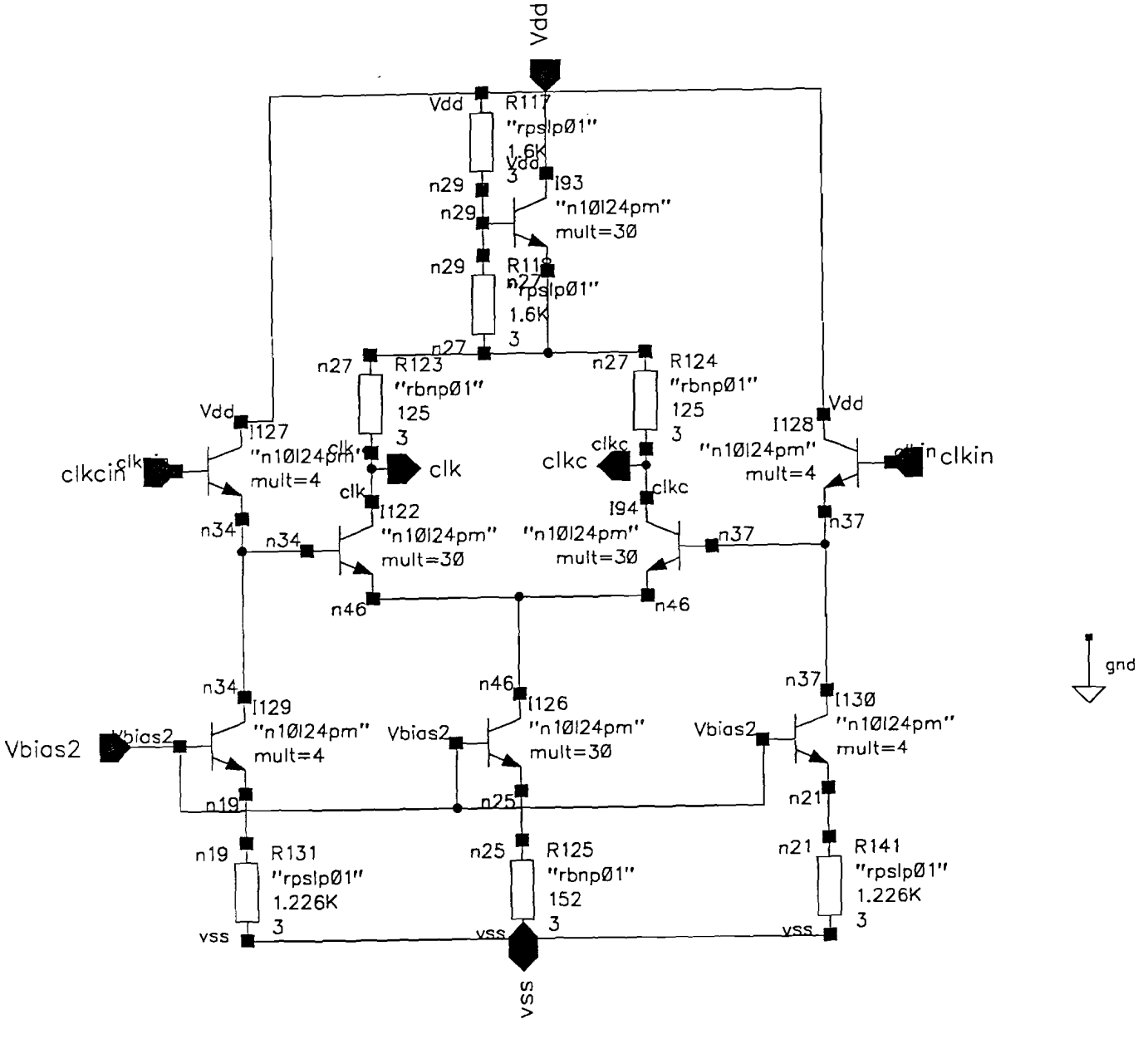
Schematic uitbuf: output buffer



Lay-out uitbuf: output buffer



Schematic clock: clock driver



Schematic ovunfl: total coarse part