Characterization and application of a mismatch detector for adaptive antenna impedance matching

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Characterization and application of a mismatch detector for adaptive antenna impedance matching

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Abstract

Mobile phone antenna mismatch caused by body effect of the phone's user affects the output power efficiency of the mobile phone power amplifier module, adaptive antenna impedance matching is an attractive way to compensate the antenna mismatch due to the body effect. Characterization of the mismatch detector which detects the phase of the reflection coefficient is presented, the phase detector provides both in-phase and quadrature information; at 900MHz, 10dBm input power, a dynamic range of 142° with an accuracy of ±4° is achieved. By applying this phase detector together with a limiter, a counter and a series-LC network which consists of an inductor and a 4-bit binary weighted switched-capacitor array, an adaptive matching network which effectively compensates the reactive antenna impedance mismatch can be realized. From simulation this adaptive matching network compensates an inductive mismatch of j83Ω (reflection coefficient $|\Gamma|$=0.6) to j8Ω ($|\Gamma|$=0.13). The switched-capacitor used for demonstrating the concept of adaptive matching has been modelled and characterized. The simulation results of the switched-capacitor model match with the characterization results, the simulated S12 of the switched-capacitor model and the measured S12 of the switched-capacitor have same magnitude and 4° phase difference, this model can be used for further simulation of the demonstration network.

Contents

List of Figures

List of Tables

1 Introduction

This chapter is intended to give some general information about the project. First the motivation of this project is shown and the project tasks are listed, then the organization of this thesis is given.

1.1 Motivation

Nowadays, consumers of mobile phones not only need long talking and stand-by time but also would like to have more features and functionalities such as camera, TV, MP3, GPS, etc. integrated into their mobile phones. This requires high power efficiency of the mobile phone's RF front-end which essentially includes a Power Amplifier Module (PAM), because the PAM dominates the total phone power consumption when active and together with the antenna it determines the quality of the mobile phone's wireless link. By improving power efficiency of the PAM, the mobile phone's battery can be more efficiently used, thus more energy headroom for integration of new functionalities.

The output impedance of a PAM is designed to match with the mobile phone's antenna impedance which has a nominal value of 50Ω, and the power efficiency of a PAM is strongly dependent on the actual antenna impedance [1]. Unfortunately, the antenna impedance is very sensitive to its vicinal environment, especially the body of the mobile phone's user [2].

Some investigations about the body loss have shown that the user of a mobile phone can seriously degrade the performance of the mobile phone. From the experimental results it has been found that the resonance frequency of the antenna drops due to the body effect. [3] In addition, differences in the body effect have been observed among users and variances in the body effect have been noted when a mobile phone is held in different ways by its user [4].

In order to improve the power efficiency of a PAM under mismatch due to body effect, adaptive antenna impedance matching is currently being developed at Philips Semiconductors and this Master's thesis project is related to the development of adaptive antenna impedance matching. The use of adaptive matching is attractive because it dynamically compensates antenna impedance variations caused by the body effect, consequently it improves the power efficiency of a mobile phone which providing more headroom for integration of more functions into mobile phones.

The adaptive antenna matching system consists of three functional blocks: the detection circuit, the control circuit and the matching network. Figure 1.1 illustrates the basic configuration of the adaptive matching system. A mismatch detector is developed at Philips Semiconductors, the performance of the mismatch detector directly affects the performance of the adaptive matching loop, it must be extensively characterized, and this is the first subject of this thesis project. The second subject of the project is to study the adaptive matching algorithm. The matching network in Figure 1.1 includes essentially a switched-capacitor array and it will apply the

emerging RF-MEMS[1] technology. Before the RF-MEMS technology is available it is desired to implement the adaptive matching loop with discrete components to show the operation of the concept, the applied switched-capacitor network needs to be modelled and characterized, this is the third subject of this project.

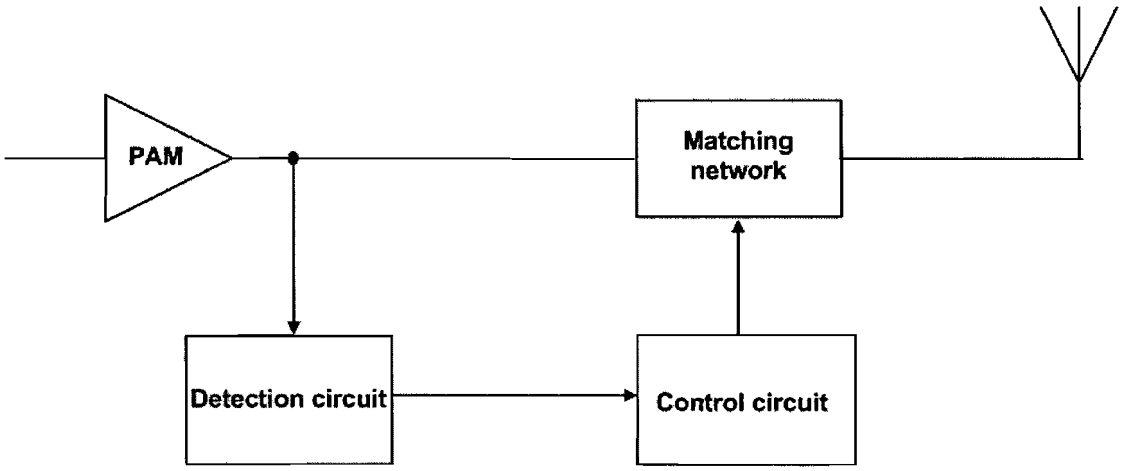

Figure 1.1: Basic configuration of an adaptive antenna matching system.

In summary, the subjects of this project are listed as below:

- Characterization of the mismatch detector.
- Study of the adaptive matching algorithm.
- Modelling and characterization of the switched capacitor network.

1.2 Organization of the thesis

This thesis is organized as follows. After this introduction, the concept of antenna impedance mismatch detection is described in chapter 2. Following that, the behavioural model of the mismatch detection concept is presented in chapter 3. Before the circuit of the mismatch detector was designed, specifications for the circuit were set and these are listed in chapter 4. After that, the circuit of the mismatch detector is presented in chapter 5. The mismatch detection circuit has been characterized and the measurement results are shown in chapter 6. An effective algorithm which compensates the antenna impedance variation is shown in chapter 7. In chapter 8, modelling and characterization of the switched-capacitor used in the adaptive matching is given. Finally, the conclusions and recommendations for future work are shown in chapter 9 and 10.

[1] Radio Frequency MicroElectroMechanical System.

2 The concept of antenna mismatch detection

Adaptive antenna impedance matching continuously needs information about actual matching condition at the antenna, essentially a detector must be included to provide such information. The principle of mismatch detection and the concept of mismatch detector are shown in this chapter.

2.1 The reflection-coefficient detection

In a mobile phone, the equivalent output impedance of a PAM is designed to match with the impedance of the antenna which has a nominal value of 50Ω, the power from the PAM is fully transmitted to the antenna and radiated if the output impedance of the PAM matches with the antenna impedance. When the antenna impedance departs from its nominal value of 50Ω due to the body effect, only part of the power from the PAM is transmitted to the antenna and radiated, the other part of that is reflected. The reflection coefficient Γ is defined as ratio of the reflected (v_r) and incident voltage wave (v_i)

$$\Gamma = \frac{v_r}{v_i} = |\Gamma| \cdot e^{j\varphi(\Gamma)} \tag{2.1}$$

Γ is complex and $0 \le |\Gamma| \le 1$, $0^\circ \le \varphi(\Gamma) < 360^\circ$, where $|\Gamma|$ and $\varphi(\Gamma)$ denote the magnitude and phase of the reflection coefficient, respectively. If $|\Gamma| = 0$ this means there is no reflection at all, in other words, the output impedance of the PAM matches with the antenna impedance; if $|\Gamma| = 1$ this means that all of the power is reflected. By detecting the magnitude and phase of the reflection coefficient, the information about mismatch at the antenna is determined. The concept of reflection-coefficient detector is presented in the next section.

2.2 The concept of reflection-coefficient detector

The block diagram of the reflection-coefficient detector is shown in Figure 2.1. A directional coupler senses the incident (v_i) and reflected (v_r) wave, and their magnitudes are detected by two envelope detectors; the phase of the reflection coefficient, that is, the phase difference between v_r and v_i, is detected by a phase detector. These three major parts of the reflection coefficient detector are introduced in the following sections.

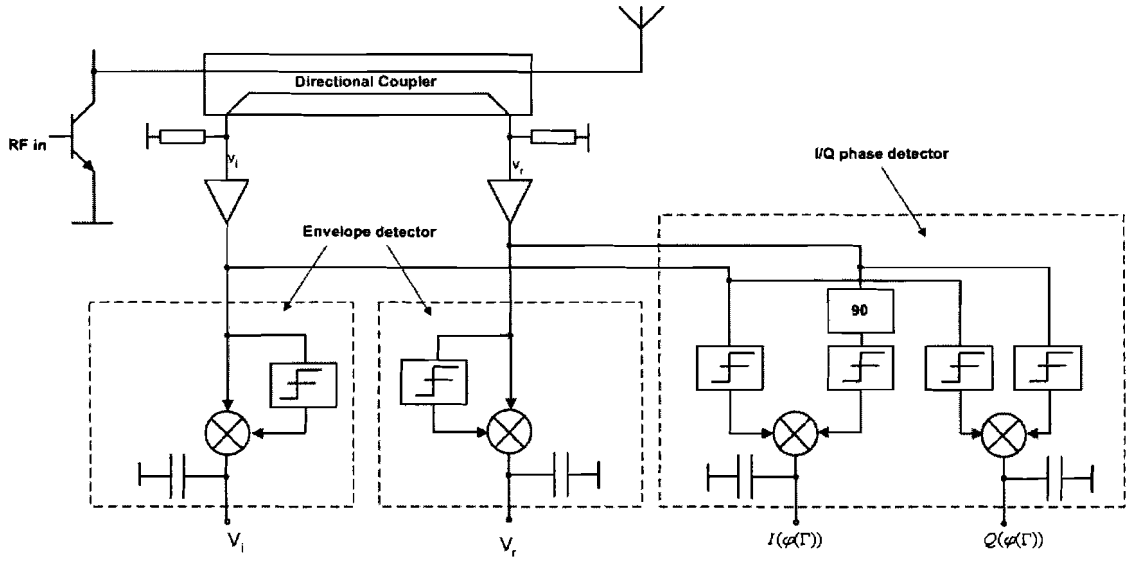

Figure 2.1: Block diagram of the reflection-coefficient detector.

2.2.1 Sensing incident and reflected wave

Sensing incident and reflected wave is accomplished by a directional coupler, which is a passive microwave component used for power division. It is a four-port component and is illustrated in Figure 2.2. Power supplied to the input port is coupled to the coupled port while the remainder of the input power is delivered to the through port, in an ideal directional coupler, no power is delivered to the isolated port.

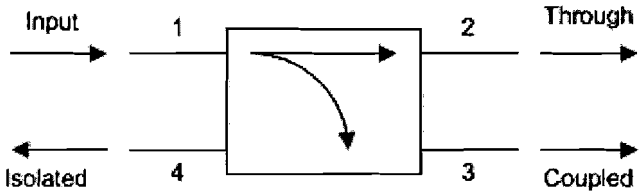

Figure 2.2: Port definition of a directional coupler.

The following three quantities are generally used to characterize a directional coupler:

$$\text{Coupling} = 10\log\frac{P_1}{P_3}$$

$$\text{Directivity} = 10\log\frac{P_3}{P_4}$$

$$\text{Isolation} = 10\log\frac{P_1}{P_4}$$

The coupling factor indicates the fraction of the input power which is coupled to the output port. The directivity is a measure of the coupler's ability to isolate forward and backward waves, as is the isolation. High directivity is needed for accurate detection of the reflection coefficient [5].

2.2.2 The concept of magnitude detection

The magnitudes of v_i and v_r are detected by two envelope detectors which are indicated in Figure 2.1. The envelope detector is based on application of a multiplier and a limiter. When a signal multiplies with its corresponding limited signal, the low-frequency component at the output of the multiplier is proportional to the magnitude of the signal. This is shown as below, suppose the input signal of the envelope detector is

$$V_i(t) = V_i \cos \omega_i t$$

and assuming that the limited $V_i(t)$ has an amplitude of ± 1, which is [8],

$$V_l(t) = \sum_{n=1}^{\infty} A_n \cos n\omega_i t, \qquad A_n = \frac{\sin \frac{n\pi}{2}}{\frac{n\pi}{4}}$$

Then the output signal of the envelope detector is

$$\begin{aligned} V_o(t) &= V_i(t) \cdot V_l(t) \\ &= \sum_{n=1}^{\infty} A_n V_i \cos \omega_i t \cos n\omega_i t \qquad (2.2) \\ &= \sum_{n=1}^{\infty} \frac{A_n V_i}{2} \left[\cos(n+1)\omega_i t + \cos(n-1)\omega_i t \right] \end{aligned}$$

The DC term of equation 2.2 is $\frac{2}{\pi} \cdot V_i$, which is proportional to the magnitude of the input signal. By dividing the detected magnitude of the reflected and incident wave, the magnitude of the reflection coefficient can be determined.

2.2.3 The concept of phase detection

The phase detection is accomplished by application of an analogue multiplier, which takes two analogue inputs and produces an output proportional to their product. If signals of identical frequency are applied to the two inputs, the multiplier behaves as a phase detector and produces an output whose DC component is proportional to the phase difference between the two inputs.

The phase detection can be done in two ways, namely by using linear or non-linear multiplication. With linear multiplication, the incident wave v_i and reflected wave v_r sensed by the directional coupler are directly applied to the inputs of the multiplier; whereas with non-linear multiplication, v_i and v_r are first limited by two limiters and then the limited v_i and v_r are applied as the inputs of the multiplier.

With linear multiplication, assuming both v_i and v_r are sinusoidal waves and $v_i(t) = A_i \cos(\omega t + \varphi_i), v_r(t) = A_r \cos(\omega t + \varphi_r)$ then at the output of the multiplier

$$\begin{aligned} v_o(t) &= v_i(t) \cdot v_r(t) \\ &= A_i \cos(\omega t + \varphi_i) \cdot A_r \cos(\omega t + \varphi_r) \\ &= \frac{A_i A_r}{2} \cos(2\omega t + \varphi_i + \varphi_r) + \frac{A_i A_r}{2} \cos(\varphi_i - \varphi_r) \end{aligned} \tag{2.3}$$

the second term of equation 2.3 is a DC term and is proportional to the phase difference between the incident and reflected wave.

With non-linear multiplication, the DC component of the output is linear proportional to the phase difference between the incident and reflected wave, see curve Q in Figure 2.3. From this curve it is clear that the Q output of the phase detector shown in Figure 2.1 is maximal when the phase difference between v_i and v_r is zero, this output is named quadrature output. If one of the sensed signals (v_i or v_r) is first 90° phase shifted, then passes through the limiter and multiplied with the other limited input signal, the output is zero at the zero-crossing of the input phase difference, this output (the I output in Figure 2.1) is named in-phase output, and its characteristic is illustrated with curve I in Figure 2.3.

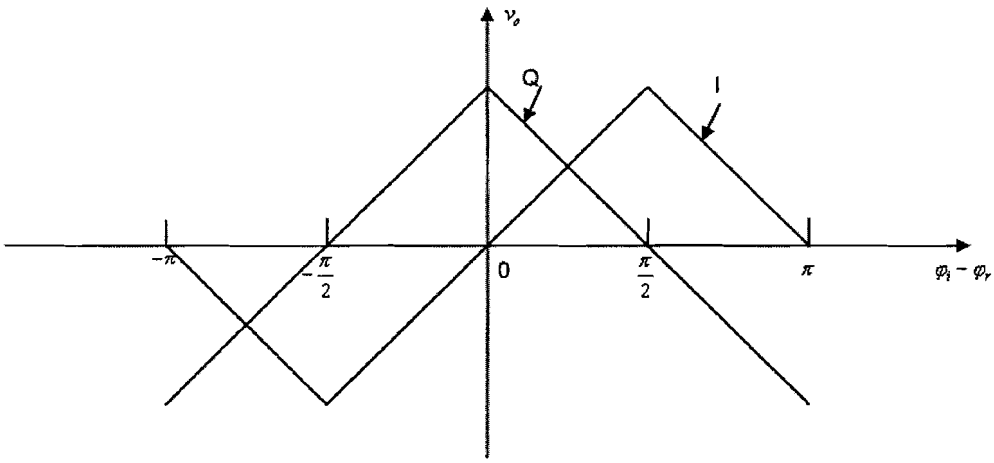

Figure 2.3: Characteristics of in-phase and quadrature outputs of the phase detector

By using a miter, amplitude information of the limiter's input is eliminated while the phase information is remained, therefore the actual waveform shapes of v_i and v_r are unimportant. As a result, the outputs of the I/Q phase detector shown in Figure 2.1 are independent of the amplitudes of the two input signals but only linear proportional to the phase difference between the two inputs. This is an important advantage comparing with linear multiplication with which the output depends both on the phase difference and amplitudes of the two input signals.

2.3 Conclusions

The concept of antenna mismatch detection--the reflection-coefficient detection has been presented in this chapter. And the concept of each block of the reflection-coefficient detector: sensing, magnitude detection and phase detection has been shown separately. The reflection-coefficient detector can detect the antenna mismatch effectively in theory, this is verified with simulations and shown in the next chapter.

3 Behavioural model of the reflection-coefficient detector

In order to verify the concept of reflection-coefficient detector that was presented in the previous chapter, simulations have been run with a behavioural model based on the concept. In this chapter, the behavioural model and its simulation results are shown.

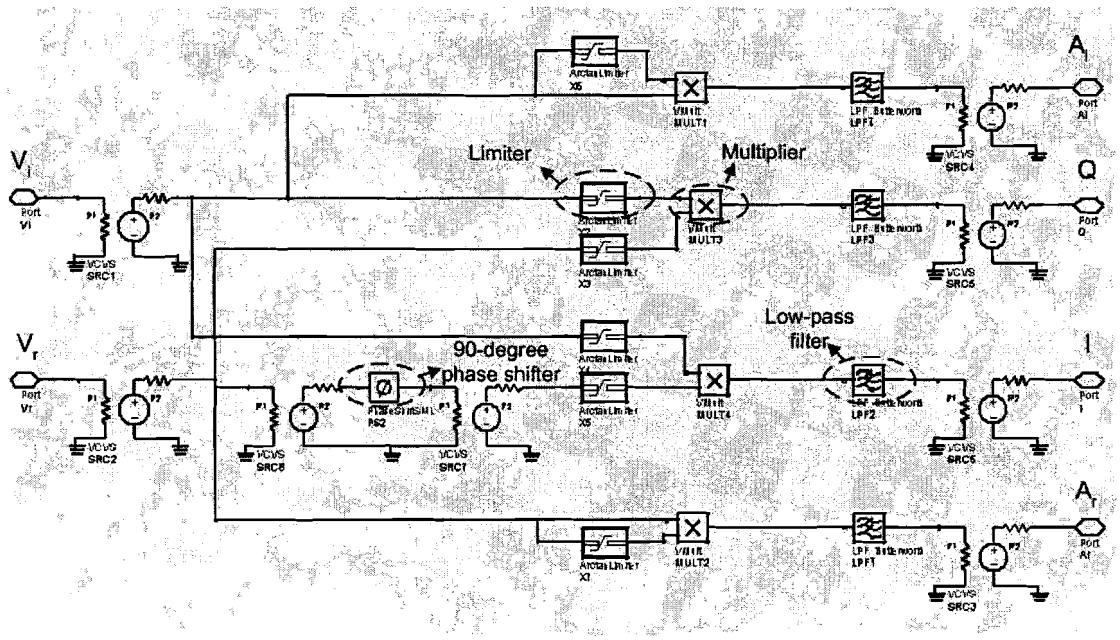

Figure 3.1: The ADS behavioural model of the reflection-coefficient detector.

3.1 The behavioural model

The behavioural model of the reflection-coefficient detector made with ADS[2] is shown in Figure 3.1. The main functional blocks of the model are all indicated in Figure 3.1, the top and bottom branches in the figure are two peak detectors for detection of the magnitude of the incident and reflected wave; the I/Q phase detector is shown in the middle part of the figure. v_i and v_r denote the sensed incident and reflected wave which are as the inputs to the reflection-coefficient detector; at the outputs, A_i and A_r denote the magnitude of the incident and reflected wave; I and Q denote the in-phase and quadrature output of the phase detector. The operation of the reflection coefficient detector has already been explained in the previous chapter, therefore the operation of the behavioural model is omitted here.

[2] Advanced Design System, a computer aided design tool from Agilent Co., is widely applied for high-frequency circuit and system design.

3.2 The simulation setup

The simulation setup, which consists three main functional blocks: the directional coupler, the reflection coefficient detector and the calculator, is shown in Figure 3.2. The incident and reflected wave sensed by the directional coupler are taken as the inputs to the reflection coefficient detector. The information provided by the reflection coefficient detector: the magnitude of the incident and reflected wave, the phase difference between the incident and reflected wave, is sent to a calculator, which is a mathematical calculation block, to calculate the reflection coefficient. The load is configured in such a way that it corresponds to a mismatch which is set at a certain reflection coefficient, and the phase of the reflection coefficient is swept from -180° to 180°.

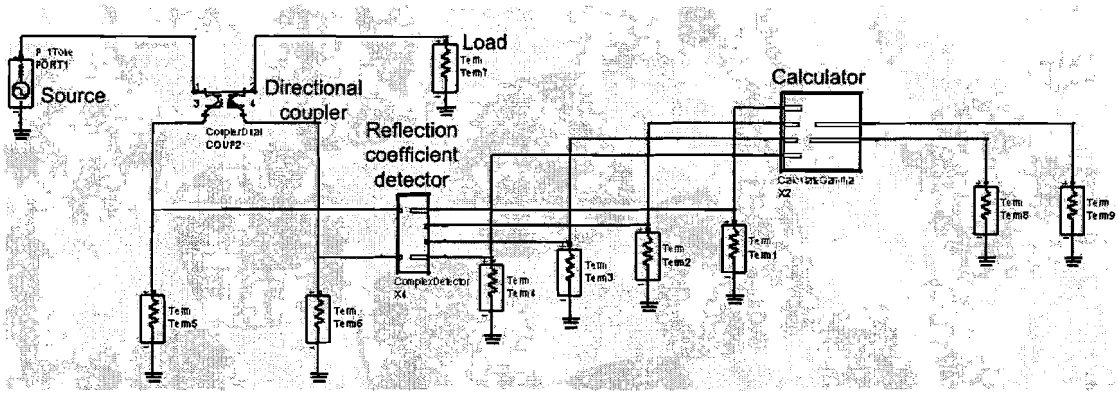

Figure 3.2: The simulation setup for the behavioural model of the reflection-coefficient detector.

3.3 The simulation results

The simulation has been run for detection of the antenna mismatch that is set at a reflection coefficient of 0.6 and the phase of the reflection coefficient is swept from -180° to 180°; the detected magnitude and phase of the reflection coefficient are shown in Figure 3.3 and 3.4.

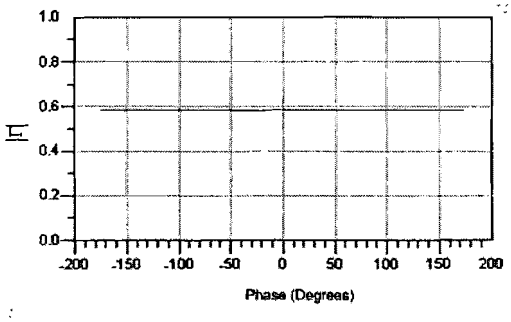

Figure 3.3: The detected magnitude of the reflection coefficient.

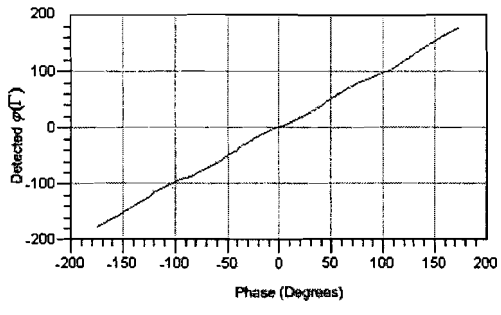

Figure 3.4: The detected phase of the reflection coefficient.

In the figures, the magnitude and phase of the detected reflection coefficient are plotted as function of the swept parameter -- the phase of the reflection coefficient. The detected magnitude of the reflection coefficient is approximately 0.6 from -180° to 180° and the detected phase of the reflection coefficient is correct as well. The

detected reflection coefficient is also plotted in the Smith Chart[7] which is shown in Figure 3.5, the detected reflection coefficient is represented by a circle with radius of 0.58 which corresponds to a reflection coefficient of 0.58.

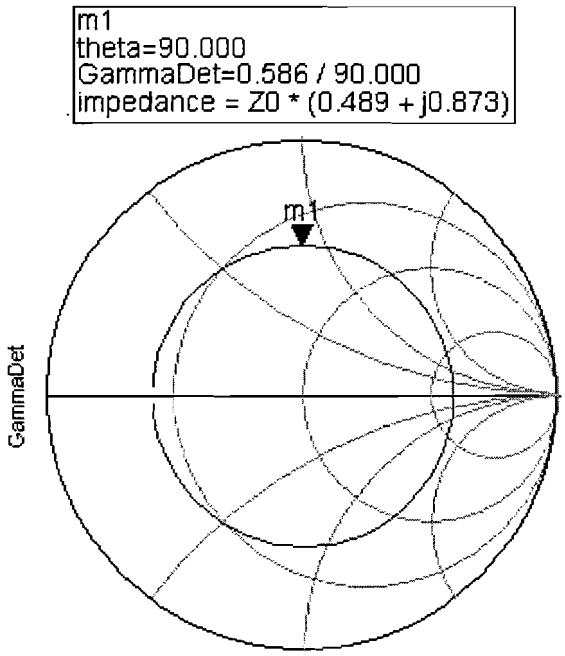

Figure 3.5: The detected reflection coefficient illustrated in the Smith Chart.

3.4 Conclusions

The behavioural model of the reflection-coefficient detector and the simulation results has been presented. The simulation results have shown that the reflection coefficient detector works very well at the concept level, based on this behavioural model, the circuit of the phase-detector part of the reflection-coefficient detector is designed and this is shown in the next chapter.

4 The specifications of the phase detector

Before the phase detector was designed, the specifications of the phase detector were defined in order to meet the requirements of the adaptive antenna impedance matching. The adaptive matching loop can be implemented in several ways, and each of them has different requirements to the phase detector. In this chapter, first the implementation of the adaptive matching loop is briefly introduced; then the specifications of the phase detector are listed.

4.1 The implementation of the adaptive matching loop

The adaptive matching loop can be implemented in two ways: fully analogue or (semi)digital, they are introduced separately below.

4.1.1 The analogue implementation

With the analogue implementation, the impedance of the matching network is continuously changed by the control circuit according to the information detected by the mismatch detector. Therefore, it requires that the phase detector can detect the phase of the reflection coefficient as accurate as possible within a large range.

4.1.2 The (semi)digital implementation

With the (semi)digital implementation, the output of the phase detector is first converted to digital signal and according to this digital signal the control circuit generates different codes to change the impedance of the matching network stepwise instead of continuously. Depending on the analogue to digital converter, the requirements to the phase detector might be less strict than that for the analogue implementation, and this will be further discussed in this chapter.

4.2 The specifications of the phase detector

The specifications of the phase detector were defined according to the analogue implementation of the adaptive matching loop introduced in the previous section, because the analogue implementation has more strict requirements than the digital implementation. The specifications of the phase detector are listed in Table 4.1 to 4.4.

Table 4.1: General specifications of the phase detector.

Parameters	Min.	Typ.	Max.	Unit	Remarks
Supply	3.0	3.5	4.0	V	
Frequency	800	-	2000	MHz	
Dynamic range	20	50	-	Degree	
Max. phase error	-4	-	4	Degree	
Input power	-20	-	10	dBm	

Table 4.2: The specifications of the phase shifter.

Parameters	Min.	Typ.	Max.	Unit	Remarks
Frequency range low-band	800	-	950	MHz	Balanced input
Frequency range high-band	1700	-	1950	MHz	
Phase error	-	±2.5	-	Degree	

Table 4.3: The specifications of the limiter.

Parameters	Min.	Typ.	Max.	Unit	Remarks
Input voltage	-	-	0.4	V	Balanced input
Dynamic range	-	40	-	dB	
Output offset	-	-	1	mV	
Linear gain	-	60	-	dB	

Table 4.4: The specifications of the multiplier.

Parameters	Min.	Typ.	Max.	Unit	Remarks
Input voltage	-	-	0.1	V	Balanced input
Dynamic range	-	40	-	dB	
Output offset	-	-	1	mV	

The phase detector is implemented with differential circuit topology in order to minimize the non-ideality such as offset, but due to process spreading offset can happen in practice. The offset is an important specification because it affects the output accuracy of the phase detector, and depending on the way of implementation, the DC offset has different impact on the accuracy of the detected phase, they are discussed separately below.

In the case of analogue implementation, that is, the outputs of the phase detector are directly applied to the control block of the adaptive loop, the DC offset does affect the output accuracy of the phase detector because the DC offset causes deviation of the phase reference from the defined level.

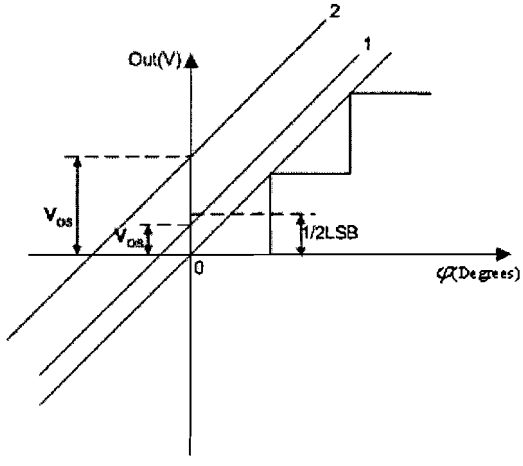

Figure 4.1: The DC offset might cause error for (semi)digital implementation of the adaptive matching loop.

In the case that digital implementation is applied, that is, the output of the phase detector is first converted to a digital signal and then applied to the control circuit, the DC offset might affect the accuracy depending on the level of the LSB (Least Significant Bit) of the analogue to digital (A/D) converter. If ½ LSB is larger than the DC offset, then the DC offset is not a problem since the digital output is still zero (For illustration, see line 1 in Figure 4.1); if ½ LSB is smaller than the offset, the DC offset causes non-zero digital output (see line 2 in Figure 4.1), consequently the control circuit makes wrong decision and incorrect impedance compensation occurs.

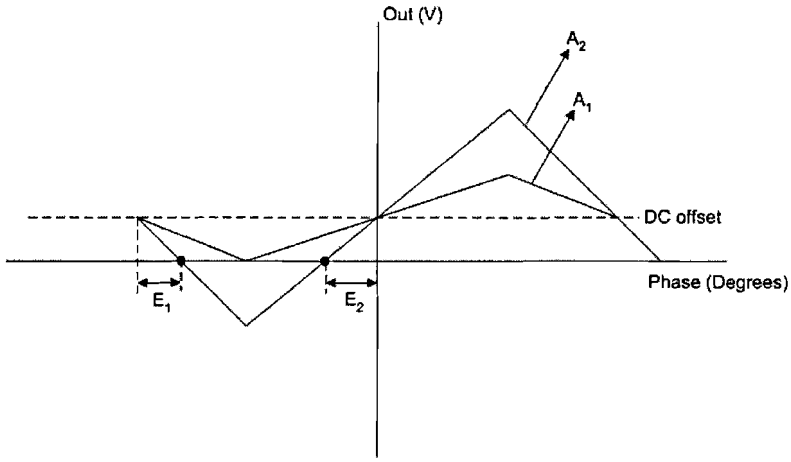

Figure 4.2: DC offset causes the polarity of the phase to be incorrectly detected when one-bit A/D converter (limiter) is used for implementation of the adaptive loop.

The simplest form of digital implementation is to use a one-bit A/D converter, or equivalently, a limiter; as a result, the digital information provided by the limiter actually represents the polarity of the phase angle. Without DC offset, the polarity of the phase angle can be detected correctly. If DC offset exists, considering two conditions which are illustrated in Figure 4.2: For curve A_1, the amplitude of the output is smaller than the DC offset, thus the output of the phase detector is always positive, consequently only half of the phase angle range can be detected correctly. For the condition represented with curve A_2, polarity errors occur in the range E_1 and E_2. Therefore, DC offset is a major limiting factor if the adaptive matching loop is implemented (semi)digitally with a limiter.

5 The circuit of the phase detector

As already shown in the previous chapters, the phase detector mainly consists of three blocks: the 90° phase shifter, the limiter and the multiplier. In this chapter, the circuit of each block is shown and the simulation results are presented. The circuit is designed with the QUBIC4 BiCMOS technology of Philips Semiconductors.

5.1 The adjustable all-pass 90° phase shifter

The all-pass 90° phase shifter provides 90-degree phase shift that is necessary to accomplish the phase detection and its schematic is shown in Figure 5.1, which includes a resistive divider, two second-order all-pass networks and two differential amplifiers [8]. The operation of this circuit is introduced in below.

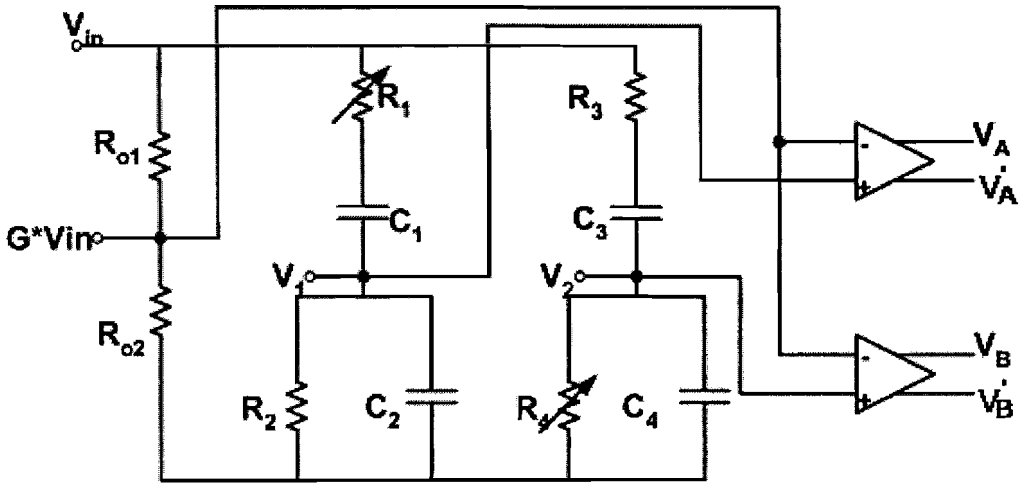

Figure 5.1: The adjustable all-pass 90° phase shifter.

5.1.1 The operation of the phase shifter

This phase shifter splits its input signal (V_{in}) into two different parts, V_A and V_B (in Figure 5.1, $V_A^{'}$ and $V_B^{'}$ are the balanced signals which correspond to V_A and V_B, respectively) with same amplitude but 90° out of phase. At the output, the relative transfer function V_A/V_B can be written as

$$\frac{V_A}{V_B} = \frac{1+Q^2\left(\frac{\omega_0^2}{\omega^2}+\frac{\omega^2}{\omega_0^2}-\frac{1}{r^2}+r^2\right)-jQ\left(\frac{r\omega}{\omega_0}+\frac{r\omega_0}{\omega}-\frac{\omega}{r\omega_0}-\frac{\omega_0}{r\omega}\right)}{1+Q^2\left(\frac{\omega_0^2}{\omega^2}+\frac{\omega^2}{\omega_0^2}-\frac{1}{r^2}+r^2\right)+jQ\left(\frac{r\omega}{\omega_0}+\frac{r\omega_0}{\omega}-\frac{\omega}{r\omega_0}-\frac{\omega_0}{r\omega}\right)} \qquad (5.1)$$

where Q is the "quality factor", r is the "shape ratio" and ω_0 is the "central frequency"[9], all these three parameters are functions of the components in the circuit. From equation 5.1 it can be seen that $|V_A/V_B|$ is equal to one indeed. This

means that the output signals of the phase shifter V_A and V_B have equal amplitude, and it is independent of the operating frequency ω.

From equation 5.1, the phase difference between V_A and V_B is [8]

$$\phi_{r,Q}(\omega) = 2\arctan\left[Q\left(\frac{\omega_0}{r\omega} - \frac{r\omega}{\omega_0}\right)\right] - 2\arctan\left[Q\left(\frac{r\omega_0}{\omega} - \frac{\omega}{r\omega_0}\right)\right]$$

By selecting proper values of the circuit components, 90° phase shift can be achieved within the desired frequency range. The circuit of the phase shifter and the components values can be found in Appendix A.

5.1.2 The adjustable phase shifter

Due to inaccuracy of the circuit components values and process spreading, phase and amplitude errors could exist at the outputs of the phase shifter. Two variable resistors are used to introduce correction of the errors at the outputs. The variable resistor is implemented by using a MOS transistor which operates in its Ohmic region (see Figure 5.2), the equivalent resistance of the MOS transistor can be varied by adjusting its gate voltage. From Figure 5.2, it can be seen that the variable resistance of R_1 is equal to R_{1p} in parallel with the sum of R_{1s} and the equivalent resistance of the MOS transistor T_1. R_p and C form a low-pass network thus eventual high-frequency noise imposed on the control voltage can be filtered out.

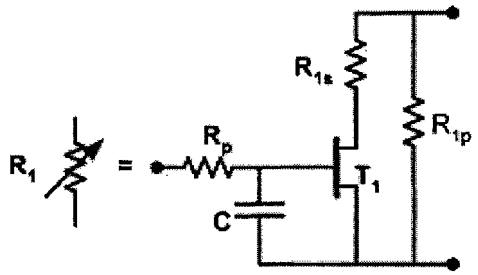

Figure 5.2: The construction of the variable resistor used in the adjustable all-pass 90° phase shifter.

5.1.3 Simulation results

The complete circuit of the all-pass 90° phase shifter is shown in Appendix A. Simulation results of the phase shifter are shown in Figure 5.3 and 5.4.The phase shift generated by the phase shifter is shown in Figure 5.3, it can be seen that the phase shift is approximately 90° over the frequency range from 800MHz to 2GHz (without tuning), and the phase error in this range is within ±4°. By tuning the equivalent variable resistor, the initial specification of ±2.5° phase error can be achieved and the phase shift is able to be tuned to 90° at the desired operating frequency. The amplitude error at the outputs of the phase detector is given in Figure 5.4, the amplitude error is approximately -1dB from 800MHz to 2GHz.

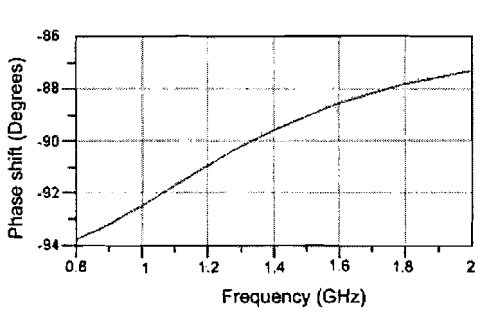

Figure 5.3: The phase shift generated by the phase shifter.

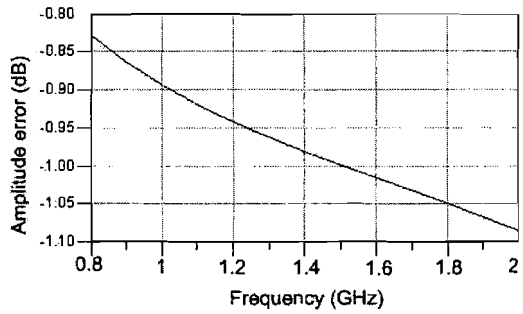

Figure 5.4: The amplitude error at the outputs of the phase shifter.

5.2 The limiter

A limiter is a non-linear circuit with an output saturation characteristic. The ideal limiter transfer function is essentially identical to the output-to-input characteristic of an ideal comparator with a zero reference level. As a result, at the output of a limiter the amplitude variations of the input signal are eliminated whereas the phase information is preserved.

5.2.1 Basic circuit of the limiter

The basic circuit of the limiter is an emitter-coupled pair circuit, the circuit and its output characteristic are shown in Figure 5.5. If the differential input signal is small, the circuit works in its linear range, and it behaves as a linear amplifier. In order to approach the characteristic of an ideal limiter, the linear range of the limiter is desired to be as small as possible, therefore the gain in the linear range should be high and this can be realized by using several such stages in cascade. The limiter used in the phase detector circuit consists of three such emitter-coupled pairs in cascade.

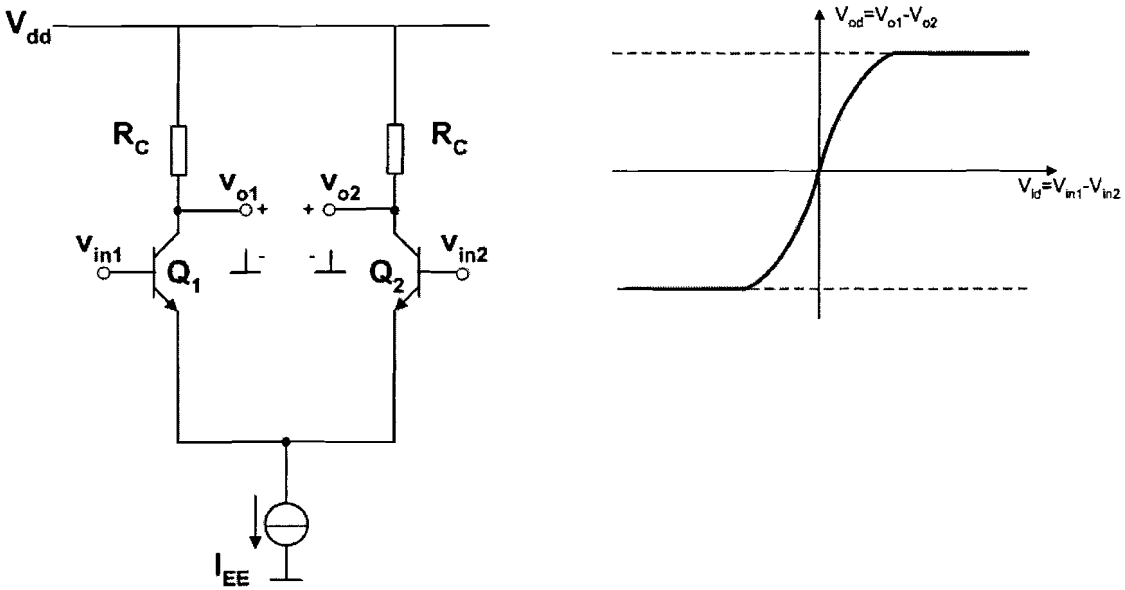

Figure 5.5: The basic circuit of the limiter and its output characteristic.

The output of the differential pair can be derived as [6]

$$V_{od} = V_{o1} - V_{o2} = \alpha_F I_{EE} R_C \tanh(\frac{-V_{id}}{2V_T})$$

where $V_{id}=V_{in1}-V_{in2}$; V_T is the threshold voltage of the bipolar transistors; $\alpha_F=\beta_F/(1+\beta_F)$, with β_F the forward current gain of the bipolar transistors.

5.2.2 Simulation results

The circuit of the differential pair which is as the basic block of the limiter is shown in Appendix B. The linear gain should be high in order to approach the characteristic of an ideal limiter. Simulation has been done to check the gain of the limiter, and the result is shown in Figure 5.6. It can be seen that the gain of one differential pair of the limiter is about 19dB when frequency is smaller than 2GHz. Three such differential pairs are used for the limiter, thus the linear gain of the limiter is 57dB.

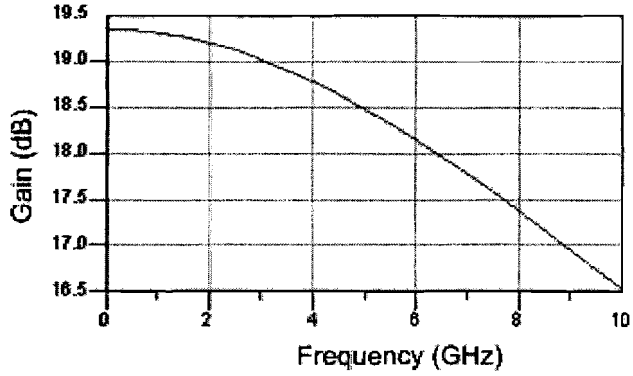

Figure 5.6: The linear gain of the differential pair used in the limiter.

5.3 The multiplier

The multiplier is a circuit which takes two analogue inputs and produces an output proportional to their product. The Gilbert-cell multiplier is introduced first, then the application of Gilbert multiplier as a phase detector is given, finally the simulation results are shown.

5.3.1 The Gilbert multiplier

The Gilbert multiplier [10] [11], shown in Figure 5.7, is the basis for most integrated-circuit balanced multiplier systems. It consists the series connection of an emitter-coupled pair with two cross-coupled, emitter-coupled pairs. In the following analysis, it is assumed that the transistors are identical, that the output resistance of the transistors and that of the biasing current source can be neglected, and the base currents can be neglected.

The differential output current is given by [6]

$$\Delta I = I_{cl} - I_{cr}$$
$$= I_{EE}\left[\tanh(\frac{V_1}{2V_T})\right]\left[\tanh(\frac{V_2}{2V_T})\right] \quad (5.2)$$

where V_T is the threshold voltage of the bipolar transistors. Thus the DC transfer characteristic is the product of the hyperbolic tangent of the two input voltages. The hyperbolic-tangent function may be represented by the infinite series:

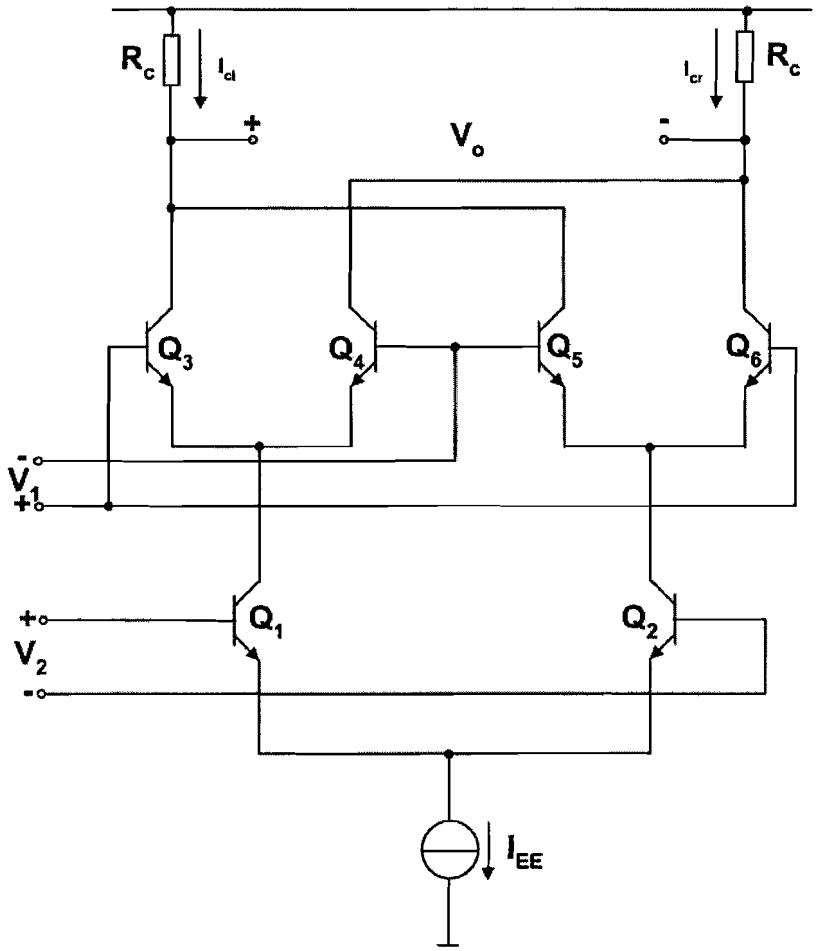

Figure 5.7: The Gilbert multiplier.

$$\tanh x = x - \frac{x^3}{3} \cdots$$

Assuming that x is much less than one, the hyperbolic tangent can then be approximated by

$$\tanh x \approx x$$

Applying this relation to equation 5.2, then

$$\Delta I \approx I_{EE}(\frac{V_1}{2V_T})(\frac{V_2}{2V_T}) \qquad V_1, V_2 << V_T$$

Thus for small-amplitude signals, the circuit performs an analogue multiplication.

If the signals applied to both inputs are large compared to V_T, all six transistors in the circuit behave as switches. This mode of operation is useful for the detection of phase differences between two amplitude-limited signals, this is the phase-detector mode and it will be introduced in the following subsection.

5.3.2 The Gilbert multiplier as a phase detector

If signals of identical frequency ω_0 are applied to the two inputs, the Gilbert multiplier behaves as a phase detector and produces an output whose DC component is proportional to the phase difference between the two inputs.

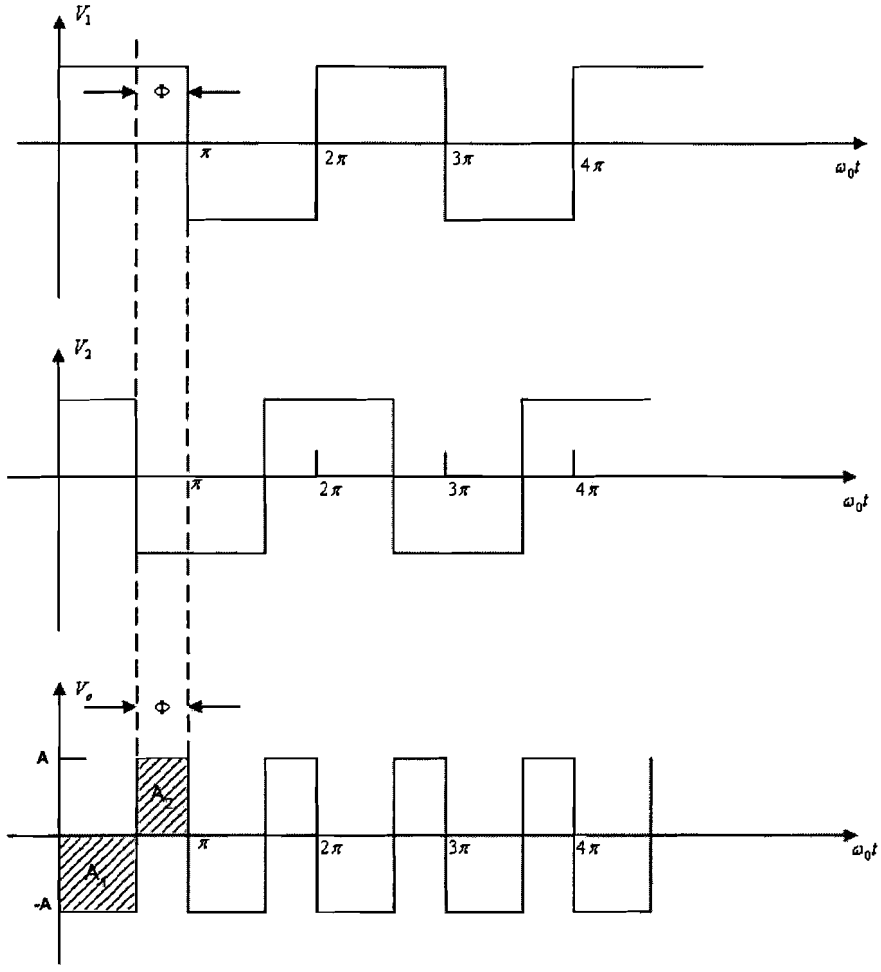

Figure 5.8: The input and output waveforms for a phase detector.

Suppose the two input waveforms V_1 and V_2 in Figure 5.8 are applied to the Gilbert multiplier and assuming that both inputs are large in magnitude so that all the

transistors in the circuit behave as switches. The output waveform that results is shown in the bottom of Figure 5.8 and consists of a DC component and a component at twice the incoming frequency. The DC component of this waveform is given by

$$V_{average} = \frac{1}{2\pi}\int_0^{2\pi} V_o(t)d(\omega_0 t)$$
$$= \frac{-1}{\pi}(A_1 - A_2)$$

where areas A_1 and A_2 are as indicated in Figure 5.8. Then,

$$V_{average} = -\left[A\frac{(\pi-\phi)}{\pi} - \frac{A\phi}{\pi}\right]$$
$$= A\cdot(\frac{2\phi}{\pi} - 1)$$

where $A = I_{EE}R_C$ (see Figure 5.7). This phase relationship is plotted in Figure 5.9.

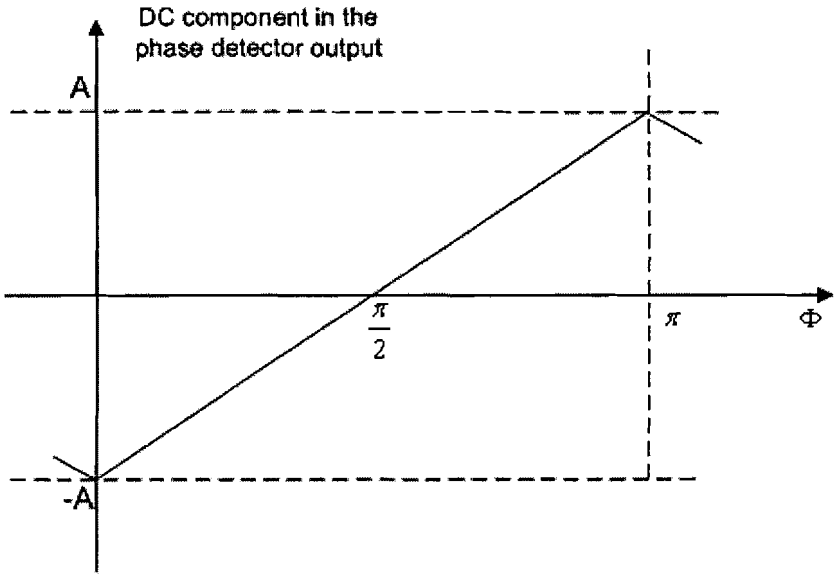

Figure 5.9: The phase detector output.

The above description is assumed that the input waveforms were large in amplitude and were square waves. If the input signal amplitude is large, the actual waveform shape is unimportant since the multiplier simply switches from one state to the other at the zero crossings of the waveform. For the case that the amplitude of one or both of the input signals is comparable to or smaller than V_T, the circuit still acts as a phase detector. However, the output voltage then depends both on the phase difference and on the amplitude of the two input waveforms. Consequently, the accuracy of the detected phase is also dependent on the amplitude of the inputs, this is not desired, therefore a limiter is essential to ensure that the accuracy of the detected phase is only dependent on the amplitude of the inputs.

5.3.3 The simulation results

The circuit of the Gilbert multiplier is given in Appendix C. The simulation of the Gilbert multiplier was run together with the other blocks of the phase detector, and this is presented in the next section.

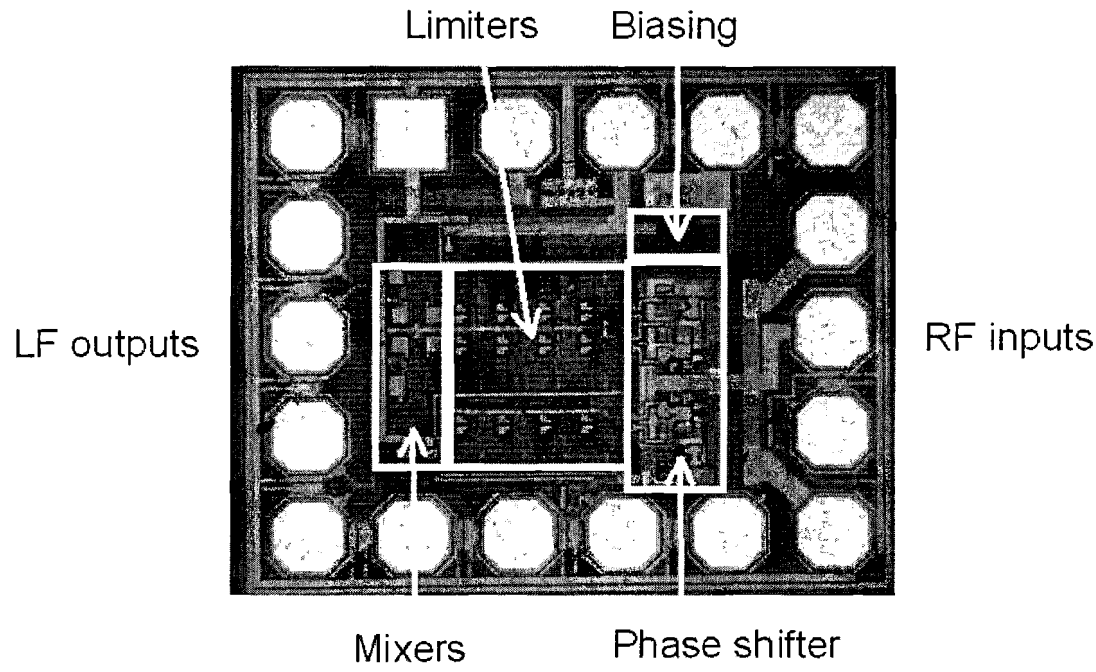

Figure 5.10: Die photograph of the phase detector.

5.4 Simulation results of the phase detector

The complete circuit of the phase detector is shown in Appendix D and the die photograph of the phase detector is given in Figure 5.10. The phase detector has on-chip biasing with single-ended 50Ω inputs and balanced outputs, the active area is 250um x 350um. The simulation setup for circuit of the phase detector is given in Figure 5.11. Different mismatch scenarios have been run with simulation, the results here shown were obtained with the following setup: the magnitude of the reflection coefficient is set at 0.6, the phase of the reflection coefficient is swept from -180° to 180°. The simulated in-phase (I) and quadrature (Q) outputs are shown in Figure 5.12.

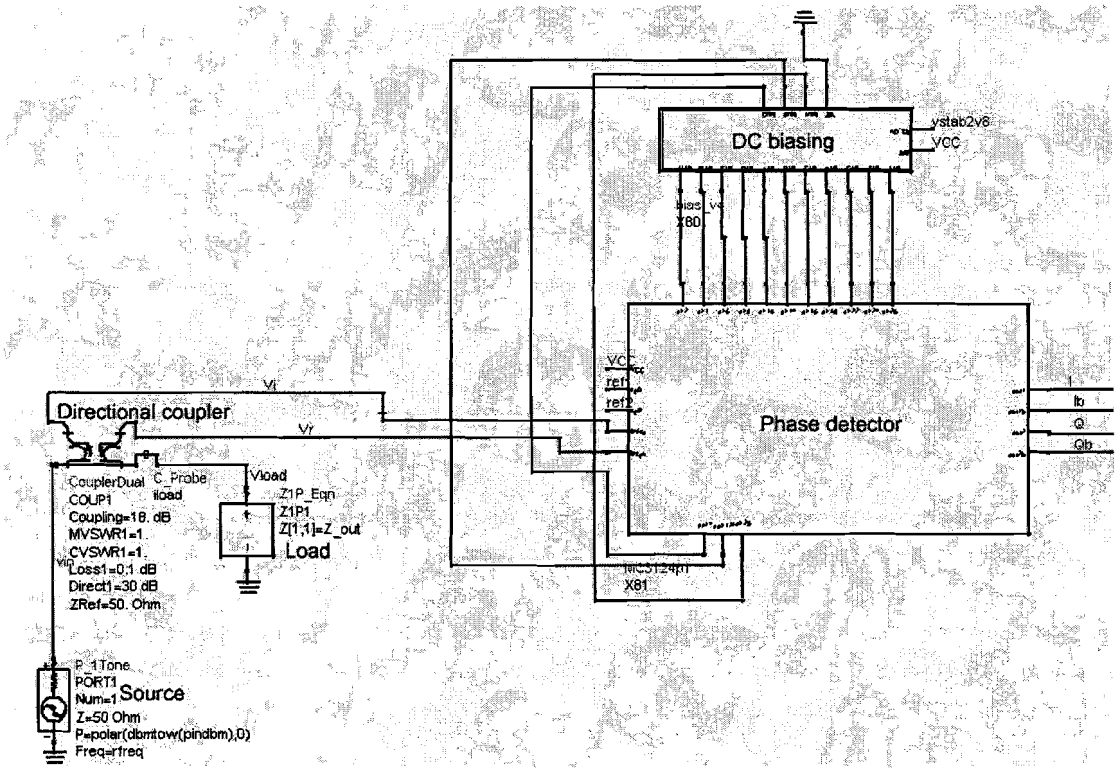

Figure 5.11: The simulation setup for the phase detector circuit.

From simulation, the outputs are triangle waveforms with 90-degree phase difference as expected which are shown in Figure 2.3. Therefore, the phase detector works well and can be used to detect the phase of the reflection coefficient. However, it has been found that when the reflection coefficient is small (approximately from 0 to 0.2), the outputs of the phase detector are not as expected. The reason is that the reflection coefficient is so small that the signal level of the reflected wave detected by the directional coupler is very low, this causes malfunction of the phase detector.

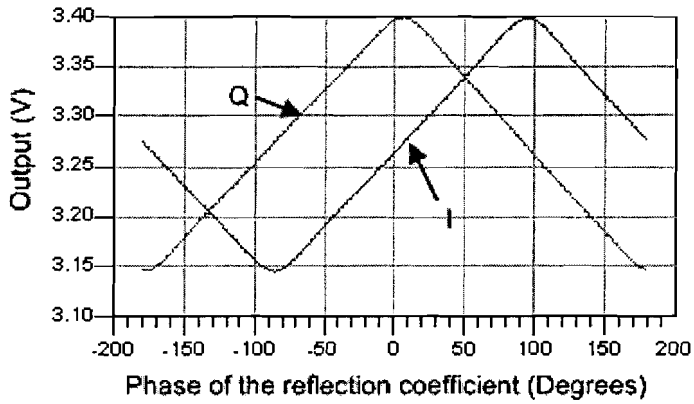

Figure 5.12: The I/Q outputs of phase detector circuit

5.5 Conclusions

The circuits of the main blocks of the phase detector have been presented and the simulation results are shown in this chapter. From simulation, the circuit of the phase detector operates very well, the characteristics of the phase detector outputs are as expected.

From the simulation results, the phase shifter can provide 90° phase shift with phase error smaller than 4° and amplitude error around –1dB from 800MHz to 2GHz without tuning. With tuning the phase shift can be set to 90° at desired operating frequency and the phase error can be improved to ±2.5°. The linear gain of the limiter is 57dB from 800MHz to 2GHz.

When the mismatch is small the phase detector malfunctions due to small magnitude of the reflected voltage wave, from simulation, the phase detector operates if the magnitude of the reflection coefficient is approximately greater than 0.2, at -10dBm input power level. Consequently, it is impossible to compensate the antenna mismatch completely, that is, the reflection coefficient becomes zero; because if it could be, then the phase detector would not work normally any more and the adaptive matching network would be defected.

6 Characterization of the phase detector

The adaptive matching control takes place according to the information provided by the mismatch detector, therefore the accuracy of such information is important for the performance of the complete loop. Key characteristics of the phase detector such as the phase accuracy, dynamic range etc. have been thoroughly examined. In this chapter, the characterization setup is shown in the beginning, then the measured characteristics are presented and discussed.

6.1 The characterization setup

The characterization setup for the phase detector is shown in Figure 6.1. Two reference-locked signal generators generate two signals with small frequency difference (here 100kHz) as the inputs to the phase detector. In phase domain, this can be viewed as that the two input signals run from the same starting point (reference locked), because there is frequency difference between the two inputs, one signal runs faster than the other and by definition the phase of a signal is integration of the signal frequency over time, therefore the phase difference between the two input signals is swept dynamically from 0° to 360°. By using one-period information of the output signal, the characteristics of the phase detector are determined.

This setup has the following advantages: it gives excellent linear phase change; it is easy for measurement of the linearity of the phase detector and the detector sensitivity, which is defined as instantaneous slopes of the outputs. However, the disadvantage of this setup is that it lacks an absolute phase reference. To set the phase reference, the outputs voltages that when no RF signals present at the inputs are taken as the in-phase and quadrature outputs voltages at 0° and ±90°, respectively; all other outputs voltages and phase angles are referenced to there. This can be seen from Figure 2.3, when two hard-limited signals multiply with each other, the output is zero when the phase difference between two input signals is 0° or ±90° for in-phase detector and quadrature detector, respectively. This means that the DC component of the in-phase or quadrature output is zero when the phase difference between the two hard-limited input signals is 0° or ±90°. Therefore, the outputs voltages that when no RF signals present at the inputs are equal to the outputs levels that when the phase difference between the two RF input signals are 0°or ±90°.

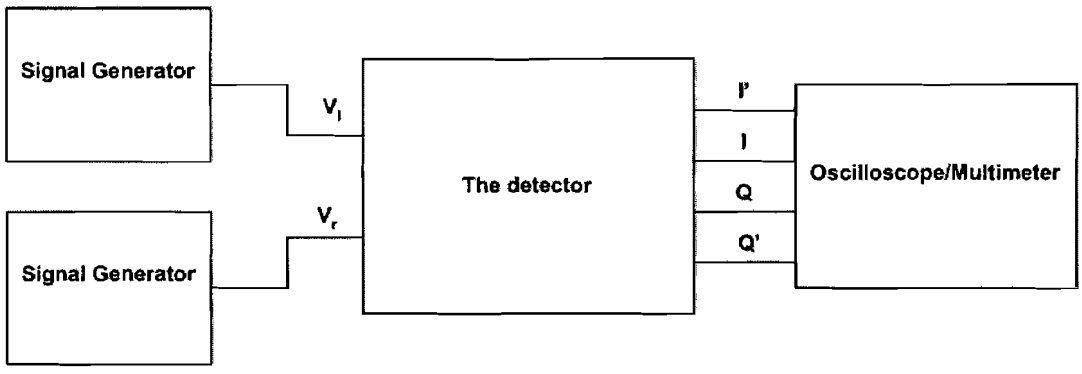

Figure 6.1: Block diagram of the characterization setup for the phase detector

6.2 The DC measurements

The DC measurements have been done in order to check the DC bias conditions, the output reference levels and the power consumption of the phase detector. The measurements have been done with different supply voltages, the DC outputs voltage of the phase detector and the supply current have been measured, the results are shown in Table 6.1.

Table 6.1: The DC measurement results of the phase detector.

V_{sup} (V)	3	3.5	4
I (V)	2.757	3.253	3.750
I' (V)	2.754	3.249	3.746
Offset (mV)	3	4	4
Q (V)	2.752	3.247	3.743
Q' (V)	2.749	3.245	3.741
Offset (mV)	3	2	2
I_{sup} (mA)	16.2	17.2	18.2

Table 6.2: The DC outputs of the phase detector when RF signals present at the inputs.

V_{sup} (V)	3	3.5	4
I (V)	2.761	3.256	3.753
I_b (V)	2.751	3.245	3.743
Offset (mV)	10	9	10
Q (V)	2.753	3.249	3.746
Q_b (V)	2.748	3.244	3.741
Offset (mV)	5	5	5

6.2.1 The DC offset

Ideally, the DC levels of the balanced outputs should equal, i.e.$V_I = V'_I$ and $V_Q = V'_Q$, however, from the DC measurements it has been found that this is not the case, offset exists at the output. This offset is caused by the mismatches in the transistor parameters, the resistors and capacitors of the phase detector. As discussed in chapter 4, the offset has different effects on the accuracy of adaptive matching depending on how the adaptive matching loop is implemented. These results can be used as

reference for setting the specifications of other blocks of the adaptive matching loop in the final design and implementation.

When RF signals are present at the inputs of the phase detector, due to non-idealities such as non-perfect isolation between the two inputs, they do contribute the DC offset at the output in practice. The output DC offset caused by RF signals has also been measured and the results are shown in Table 6.2. It can be seen that the present of RF signals at the phase detector inputs make the offset worse.

6.3 The RF measurements

The RF measurements have been done at different frequencies from 800MHz to 2GHz with input signal levels varying from 10dBm to –20dBm; all the characteristics are shown in the figures of Appendix E.

6.3.1 The determination of accuracy and dynamic range of the phase detector

A very important characteristic of the phase detector is its dynamic range which is defined as the range of angles that can be detected by the phase detector within a certain range of errors (accuracy). Depending on the applied method of adaptive loop implementation, the requirements to the accuracy and dynamic range are different.

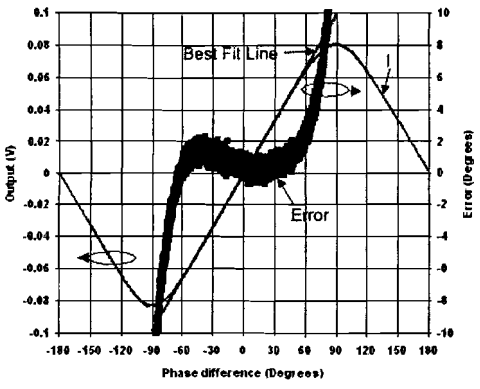

Figure 6.2: In-phase output characteristic at 900MHz, P_{in}=10dBm.

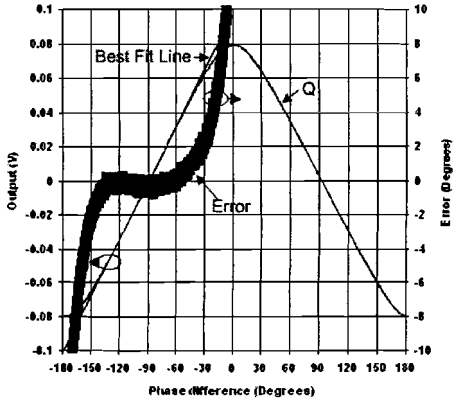

Figure 6.3: Quadrature output characteristic at 900MHz, P_{in}=10dBm.

In order to show how the dynamic range of the phase detector is determined, the output characteristics of the phase detector at 900MHz, input power 10dBm are shown in Figure 6.2 and 6.3. The dynamic range of the phase detector is determined as follows: firstly, the slope of the obtained output characteristic curve around 0° (for I output, -90° for Q output), that is, the detector sensitivity, is found by taking difference of the adjacent output voltages over difference of the adjacent phase angles. Then according to the detector sensitivity a Best Fit Line (BFL) that fits the real characteristic curve can be drawn. The phase detector error is defined as

$$\varepsilon = \frac{V_{BFL} - V_o}{s} \tag{6.1}$$

where ϵ denotes the phase detector error, V_{BFL} denotes the output level corresponding to the BFL, V_o denotes the actual output voltage and s denotes the detector sensitivity.

The characteristics of the I and Q outputs of the phase detector under normal operating condition (the supply voltage V_{sup} = 3.5V) are shown in Figure E.1 through Figure E.12, from which it is clear that the expected characteristics as shown in Figure 2.3 are obtained. The sensitivity of the phase detector is 1.1mV/degree. More detailed discussions about the measured characteristics are given in the next subsection.

6.3.2 Discussions

For analogue implementation of the adaptive matching loop, the accuracy of actual value of the detected phase is important since the analogue outputs of the phase detector are directly applied to the control circuit. From the specifications shown in Table 4.1, chapter 4, the accuracy requirement is ±4°. The dynamic ranges of the phase-detector outputs are determined from Figure E.1 through Figure E.12 of Appendix E, for convenience the numeric results are summarized in Table 6.3 and the graphic results are reorganized in Figure E.13 through E.16, Appendix E.

Table 6.3: Summary of the dynamic ranges of the phase detector.

	I			Q		
P_{in} / f	10dBm	-10dBm	-20dBm	10dBm	-10dBm	-20dBm
900MHz	142°	130°	55°	135°	122°	47°
1800MHz	125°	52°	12°	130°	54°	11°

From Table 6.3, it can be seen that the dynamic range of the phase detector decreases as the operating frequency increases. The decrease is not noticeable if the input signal levels are large, at 10dBm input level the dynamic range decreases from 142° to 125° at the I output and from 135° to 130° at the Q output respectively when the operating frequency is increased from 900MHz to 1800MHz. But at low input levels, the dynamic range decreases dramatically as the operating frequency increases, from 130° to 52° at the I output and from 122° to 54° at the Q output when the input level is equal to -10dBm and the operating frequency is increased from 900MHz to 1800MHz. When the input power is lower than –20dBm, the dynamic ranges at both low band and high band are significantly decreased comparing with that at higher input power levels. In addition, at 1800MHz, -20dBm input power, the dynamic range does not meet the minimal specification 20° (see Table 4.1, chapter 4).

For digital implementation of the adaptive matching loop, the requirements for the accuracy and dynamic range of the phase detector are different to that for the analogue implementation. The ½ LSB level of the A/D converter is a limiting factor for accuracy. If the error ϵ is smaller than ½ LSB, the digital output is still correct; if the error ϵ is greater than ½ LSB, the digital output is wrong. Therefore, the error of the phase detector might cause incorrect adaptive matching to occur depending on the ½ LSB level of the A/D converter.

For the simplest form of digital implementation, using a limiter, the sign of the output is most important but the actual value of the output does not need to be accurate. Therefore, the characteristic of dynamic range does not need to be considered for this kind implementation. From this point of view, it is attractive to apply a limiter instead of multi-bit A/D converter for digital implementation and analogue implementation of the adaptive matching loop.

Another factor should be considered for the case that the adaptive matching loop implemented digitally is the step-level of impedance change of the matching network: the impedance of the matching network is changed in stepwise instead of continuously, therefore, the phase change due to impedance compensation detected by the phase detector is stepwise as well. As a result, it is sufficient that the error of the phase detector is not larger than the step-level of the phase change.

6.4 The dependency on the power supply voltage

For the output characteristic dependency on the supply voltages at 900MHz the results are shown in Figure E.17 and Figure E.18 of Appendix E. Obviously, the output curves have identical characteristics, same detector sensitivity, but the absolute output levels are shifted in accordance with the variation of the supply voltages and this is not indicated in Figure E.17 and Figure E.18. At other operating frequencies, same characteristics as Figure E.17 and E.18 have been obtained, for simplicity, they are not included in Appendix E.

6.5 The phase shift between the I and Q output

The phase shift between the in-phase and quadrature output was measured. This has been done by tuning the equivalent variable resistance of the phase shifter so that the phase shift between the I and Q output at 900MHz is precisely 90°, and with the same tuning voltage the phase shift at high band is measured. From the measurement, the phase shift is 84.6° at 1800MHz, the photo of the measured I/Q phase shift is shown in Figure 6.4.

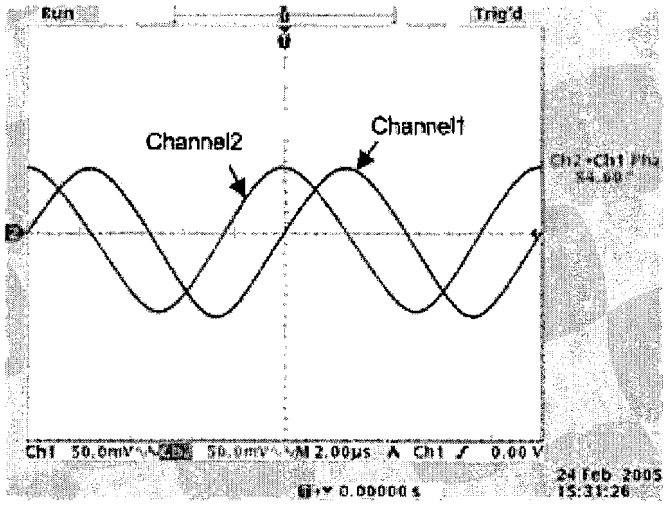

Figure 6.4: The phase shift between I and Q outputs of the phase detector at 1800MHz when the phase shift is tuned to 90° at 900MHz.

The phase shift can be tuned to have an error of ±2.5° within the frequency range from 800MHz to 2GHz.

6.6 Conclusions

The characterization setup for the phase detector and the measured characteristics are presented. The setup is easy to implement and the characteristics of the phase detector can be effectively measured with this setup, the expected characteristic curves have been obtained, and at low frequencies (800~900MHz) the phase detector performs very well, a large dynamic range of 142° is obtained at 900MHz and 10dBm input power.

From the measurement, it has been observed that offset exists at the outputs. Depending on the method of loop implementation, the offset might cause incorrect adaptive matching. With analogue implementation, the actual value of the output of the phase detector is used by the control circuit, therefore, the offset causes error and from the measurement the detector sensitivity is 1.1mV, the offset can cause an error up to 4 degrees. With (semi)digital implementation, whether the offset might cause á significant error is subject to the LSB level of the A/D converter. When a limiter is applied, the offset is a major limiting factor for correctly detecting the polarity of the output of the phase shifter.

For the RF characteristics, with analogue implementation of the adaptive matching loop, the detection error is specified to ±4° for determination of the dynamic range of the phase detector. The dynamic range of the phase detector decreases as the operating frequency increases; this decrease is not obvious if the input signal level is high and the operating frequency is low. However, at low input levels and high frequencies, the dynamic range is significantly decreased as the frequency increases. In other words, the performance of the phase detector is considerably degraded at high frequencies. Furthermore, when the input power lower than –20dBm, at both low band and high band the dynamic ranges are significantly decreased, and at 1800MHz, -20dBm, the dynamic range does not meet the specification.

For digital implementation of the adaptive matching loop, whether the error of the phase detector might cause the control circuit to make wrong decision is dependent on the error and the LSB level of the A/D converter.
For adaptive-loop implementation with a limiter, the dynamic range does not need to be considered because only the polarity of the phase detector needs to be correctly detected. From this point of view, it is attractive to apply a limiter for the loop implementation instead of multi-bit A/D converter and analogue implementation.
Also for digital implementation the step-level of the impedance change of the matching network should be taken into account, the accuracy of the phase detector is acceptable as long as the error of the phase detector is not larger than the step-level of the phase change due to the step-level change of the impedance network.

When the supply voltage varies from the normal operating value, the detector sensitivity is not changed and the output voltage has a shift which is approximately equal to the change of the power supply voltage.

When the phase shift between the I and Q outputs is tuned to 90° at 900MHz, at 1800MHz the phase shift becomes 85° with the same tuning voltage, and the phase shift can be tuned to an accuracy of ±2.5 ° within the frequency range from 800MHz to 2GHz, the performance of the phase shifter is quite good.

In summary, the phase detector meets the defined specifications shown in Table 4.1 provided that the input power is higher than –20dBm, this phase detector can be applied in the adaptive-matching loop for demonstration. The performance of the phase detector should be further improved at high frequencies and lower input level.

7 The adaptive matching algorithm

This chapter shows an algorithm that adaptively compensates the reactive antenna impedance mismatch. Firstly, the algorithm is described; then the implementation of the algorithm is shown; finally the simulation results are presented.

7.1 The algorithm

It is already known that the body-effect detunes the antenna resonance frequencies downwards causing an inductive behaviour of the antenna [12]. Moreover, the variation in the reactive part of the antenna impedance is typically much larger than the change in the resistive part of the antenna impedance. Based on these facts, an effective algorithm is to compensate the reactive part of the antenna impedance mismatch.

An adjustable series-LC network is taken as the matching network to compensate the reactive part of the antenna impedance mismatch, it consists an inductor and a switched-capacitor array. The adaptive matching algorithm is illustrated with a flow chart shown in Figure 7.1. The detector detects the phase of the reflection coefficient

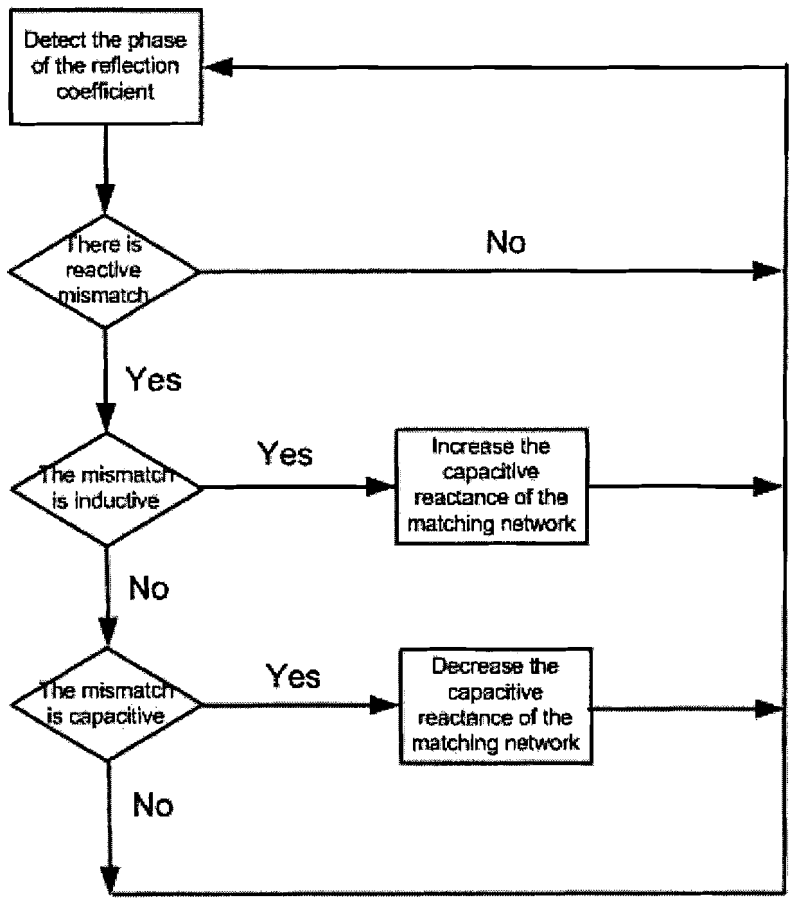

Figure 7.1: The flowchart for the adaptive matching algorithm which compensates the reactive impedance mismatch.

continuously. If it is detected that the mismatch is inductive, then the matching network will be actuated to provide more capacitive reactance; if it is detected that the mismatch is capacitive, then the matching network will be actuated to provide less capacitive reactance. The whole process iterates itself till the reactive mismatch is adapted to zero [13].

Whether the mismatch is capacitive or inductive can be determined by detecting the phase of the reflection coefficient, this can be explained with help of the Smith Chart (see Figure 7.2) and the characteristic of the I-output (see Figure 7.3) of the phase detector: when $0°<\varphi(\Gamma)<180°$, the reactive mismatch is inductive (positive) and the I-output is also positive; when $-180°<\varphi(\Gamma)<0°$, the reactive mismatch is capacitive (negative) and the I-output is negative as well. The sign of the mismatch and that of the I-output is identical, therefore, by knowing the polarity of the I-output, whether the reactive mismatch is inductive or capacitive is determined and the compensation can be done accordingly.

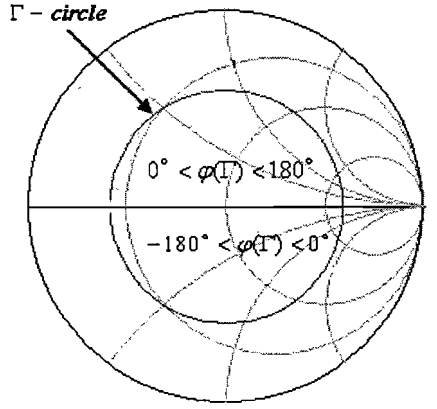

Figure 7.2: Whether the mismatch is inductive or capacitive can be determined by knowing the phase of the reflection coefficient.

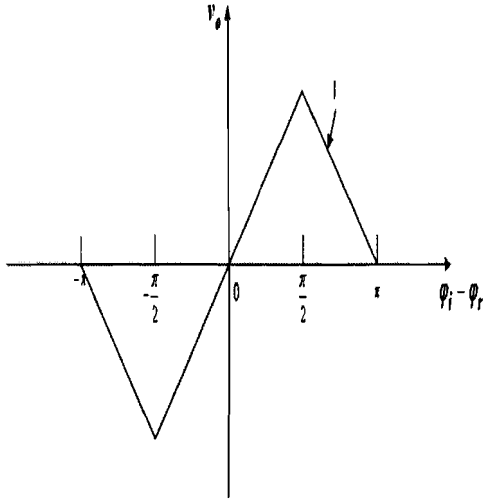

Figure 7.3: The characteristic of the I-output of the phase detector. The sign of the I-output is the same as that of the reactive mismatch.

This algorithm requires only knowing whether the reactive mismatch is inductive or capacitive, in other words, knowing whether the I-output of the phase detector is positive or negative; precise magnitude of the mismatch is not necessary. Thus, only the I-output of the phase detector is needed, this means less chip area, less power consumption and lower cost. In addition, since only the sign of the I-output is needed, this requires the zero-degree level of the phase detector being accurate, large dynamic range is not essential. Therefore, this algorithm can be implemented with the simplest digital implementation which was introduced in the previous chapters, and this is described in the next section.

7.2 The implementation of the algorithm

The complete adaptive matching loop that compensates the reactive antenna impedance variation is shown in Figure 7.4, it consists of the directional coupler, the

phase detector for detection of the phase of the reflection coefficient, a one-bit A/D converter (limiter), an up/down counter, a level shifter and an adjustable series-LC network.

The directional coupler senses the incident (v_i) and reflected wave (v_r) which are taken as the inputs to the phase detector. The phase detector detects the phase of the reflection coefficient, as explained in the previous section, only the I-output is needed. Since only the polarity of the I-output is needed for this algorithm, the magnitude of the I-output is unimportant, a limiter is used to generate positive or negative unit output voltage according to the sign of the phase-detector output. In accordance with the output of the limiter, an up/down counter counts either up or down under the control of an enable signal (EN).

The switches of the switched-capacitor array are ON or OFF following the counter output. The switched-capacitor array consists of 4-bit binary weighted capacitors and it will utilize the emerging RF-MEMS technology which requires high actuating voltage (several tens of Volt), therefore a level shifter is needed to convert the low-voltage counter output to the required high actuating voltage. The actuating voltage needed for the switched-capacitor array used in the demonstration loop is smaller than 5V, and most of the available counter IC has an output voltage of 5V, the level shifter is not needed.

The adaptive mismatch compensation will be applied in standard mobile phones which usually are TDMA-based systems. In such systems, reading the phase information (the limiter output) can be carried out at the rising edge of EN while a power burst is being transmitted, whereas switching activities of the switched-capacitor array can be done outside the power burst at the falling edge of EN. This avoids the distortions caused by switching activities during adaptation [13].

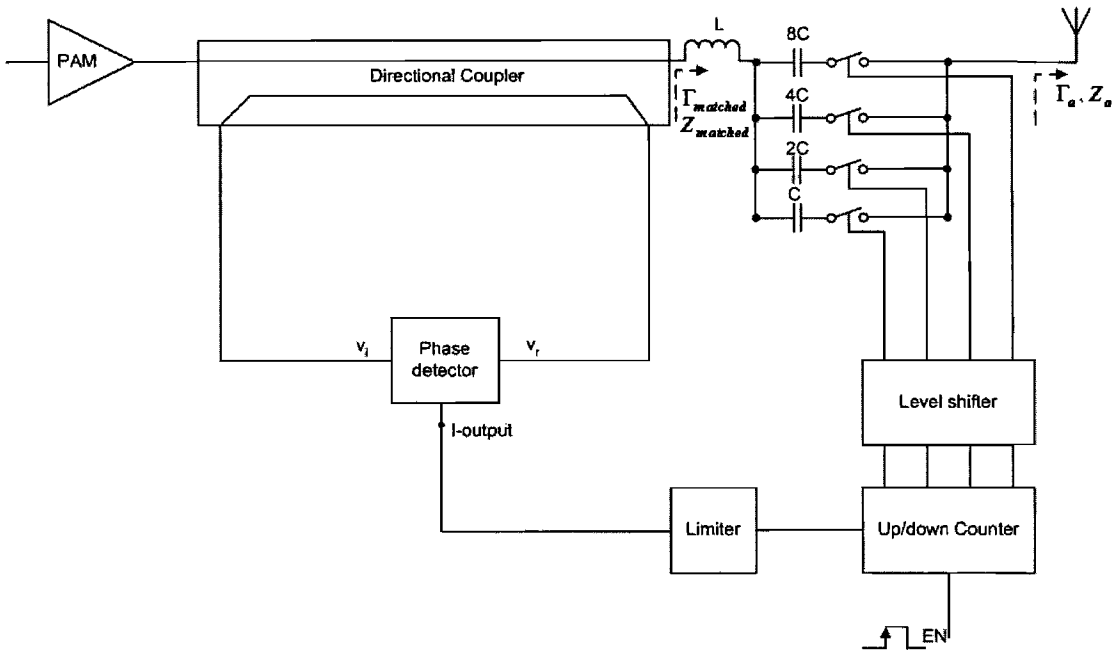

Figure 7.4: The implementation of the adaptive control algorithm which compensates the reactive impedance variation.

7.3 Simulation results

A simulation setup is established to verify the operation of the adaptive matching loop. The mismatch setup is: initially, at the antenna side $|\Gamma_a| = 0.6$ and $\varphi(\Gamma_a) = 45°$, 90° and 135°, respectively (see Figure 7.4, for "Γ_a"); equivalently the corresponding antenna impedance Z_a is: 63+j83Ω, 23+j44Ω and 14+j19Ω, respectively. The simulation were run at 900MHz and 1800MHz.

Figure 7.5 shows the simulated results of the I-output, the initial antenna mismatch conditions are indicated in the figure. It can be seen that after a short period of adaptation the output fluctuates around zero in the steady state, this implies that the reactive mismatch is compensated to about zero. The fluctuation is due to the step-level of the impedance matching network, here the LSB value of the binary 4-bit switched-capacitor array.

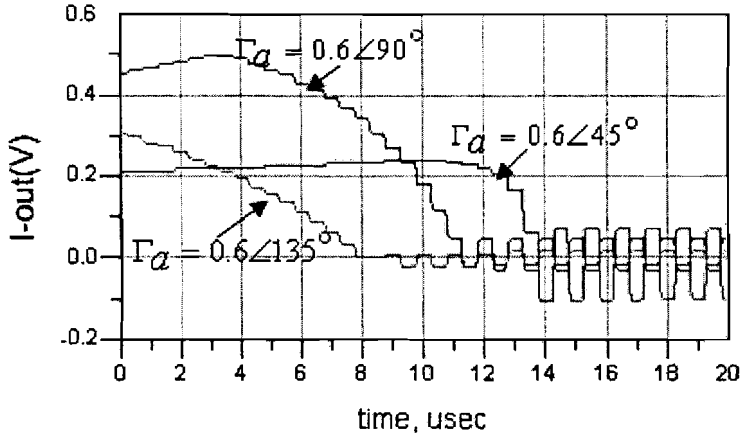

Figure 7.5: Output of the phase detector as a result of adaptive matching for different initial mismatch conditions.

From the simulation, the reactance detected by the directional coupler is compensated to about zero and fluctuates around zero in the steady state, this adaptation process is shown in Figure 7.6. Due to the non-idealities of the directional coupler such as finite directivity and isolation, losses, etc., at the load side the reactance and magnitude of the reflection coefficient are compensated to $Z_{matched}$=j8Ω, $|\Gamma_{matched}|$=0.13 (Γ_a=0.6∠45°); $Z_{matched}$=j3Ω, $|\Gamma_{matched}|$=0.36 (Γ_a=0.6∠90°) and $Z_{matched}$=j1Ω, $|\Gamma_{matched}|$=0.55 (Γ_a=0.6∠135°), see Figure 7.4 for "$\Gamma_{matched}$". The simulation results at 1800MHz are shown in Figure 7.8 and 7.9, the curves are similar to those shown in Figure 7.6 and 7.7, the difference is because that the impedances of the inductor and capacitors are changed due to the frequency variation.

Also, the simulation results under the condition that the mismatch is capacitive are shown in Figure 7.10 and Figure 7.11, the adaptation range is smaller for the capacitive mismatch comparing with inductive mismatch. Because the antenna mismatch behaves mainly inductive due to body effect as mentioned in the beginning of this chapter, it is not necessary to have the same adaptation range for the capacitive mismatch as for the inductive mismatch.

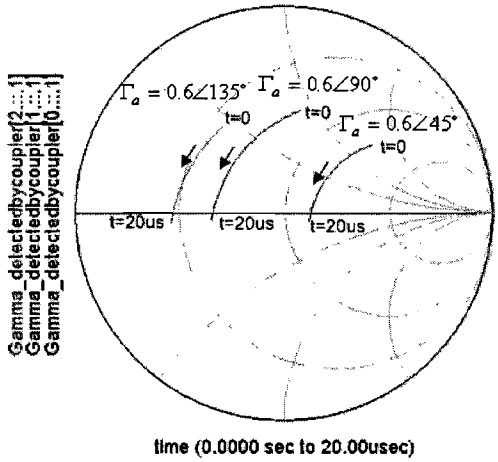

Figure 7.6: The adaptation process by viewing the reflection coefficient detected by the directional coupler, f=900MHz.

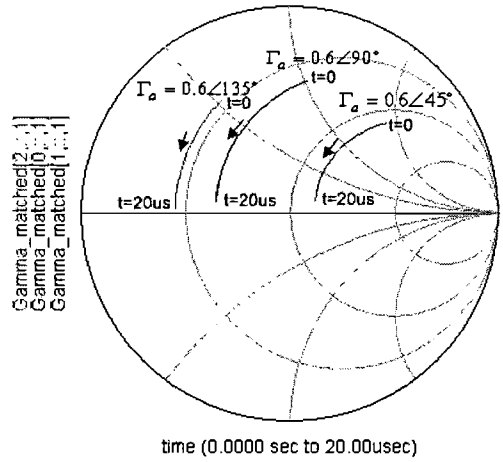

Figure 7.7: The adaptation process by viewing the reflection coefficient at the load side, f=900MHz.

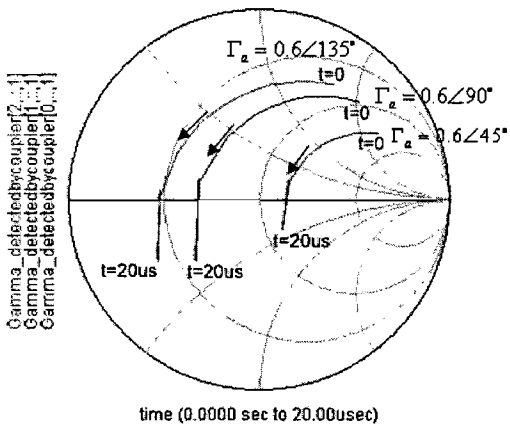

Figure 7.8: The adaptation process by viewing the reflection coefficient detected by the directional coupler, f=1800MHz.

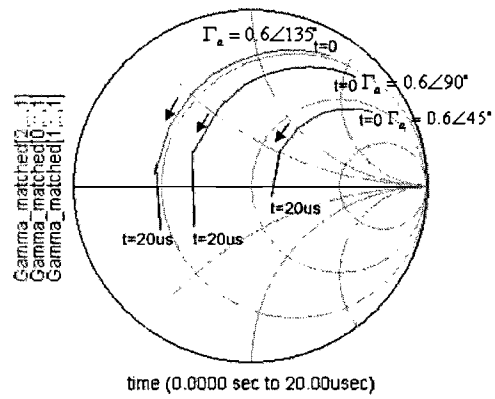

Figure 7.9: The adaptation process by viewing the reflection coefficient at the load side, f=1800MHz.

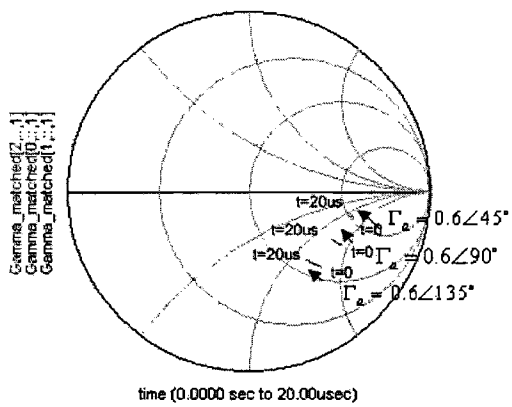

Figure 7.10: The adaptation range is smaller for capacitive mismatch than that for the inductive mismatch, f=900MHz.

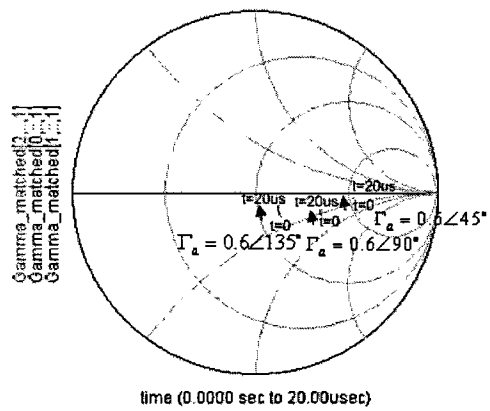

Figure 7.11: The adaptation range is smaller for capacitive mismatch than that for the inductive mismatch, f=1800MHz.

The algorithm compensates the reactive mismatch very well from the results of the simulation, within the adaptation range, the reactive mismatch can be adapted to around zero. But zero reactance does not mean that the antenna mismatch is fully compensated, from the viewpoint of the reflection coefficient, it could still be large after the reactive mismatch is adapted to zero. For example, at 900MHz, $|\Gamma_{matched}|$ is compensated from 0.6 to 0.13 when the initial reflection coefficient at the antenna side is $0.6\angle 45^\circ$ (63+j83Ω); but under the other two initial mismatch conditions, $|\Gamma_{matched}|$ is compensated from 0.6 to 0.36 and 0.55, respectively (see Figure 7.7). This can be explained as follows: In general, the reflection coefficient Γ can be written as

$$\Gamma = \Gamma_r + j\Gamma_i$$

where Γ_r and Γ_i denote the real and imaginary part of the reflection coefficient, respectively. By adapting the reactive mismatch to zero, Γ_i becomes zero, consequently, Γ is completely determined by Γ_r. If $|\Gamma_r|$ is large and because only the reactive mismatch is fully compensated, $|\Gamma|$ is still large. When the reactive mismatch is compensated to zero, $|\Gamma|$ can be written as

$$|\Gamma| = |\Gamma_r| = \frac{R^2 - R_0^2}{(R + R_0)^2}$$

where R is the actual resistance of the antenna and R_0 denotes the nominal resistance (50Ω), and the relationship between $|\Gamma_r|$ and R is plotted in Figure 7.12.

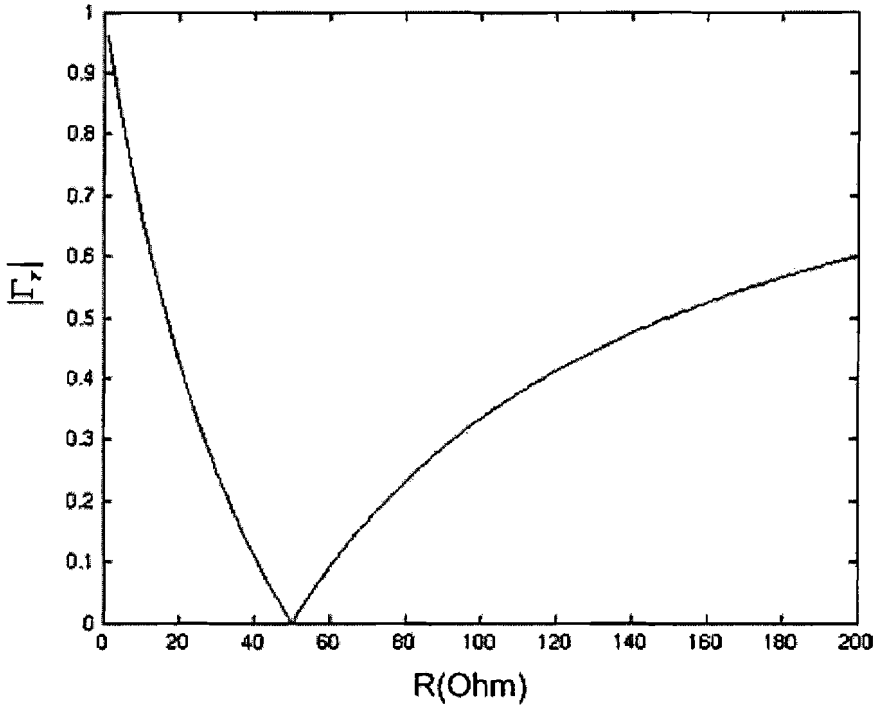

Figure 7.12: : The magnitude of the reflection coefficient as a function of the antenna resistance under the condition that the reactive mismatch is compensated to zero.

From Figure 7.12, it can be seen that the presented algorithm is most effective when the resistive mismatch is small, e.g. if the desired magnitude of reflection coefficient should be around 0.2, then the actual load resistance should be approximately at 35Ω or 75Ω. If the resistive mismatch is dominant, then the reflection coefficient cannot be decreased after adaptation though the reactive mismatch can be adapted to zero by this algorithm. It is also observed from Figure 7.12 that for the same variation of the antenna resistance, the magnitude of the reflection ratio changes faster if the load resistance is smaller than 50Ω.

7.4 Conclusions

The control algorithm that compensates the reactive mismatch and the implementation of the algorithm together with the simulation results have been shown. This algorithm effectively compensates the reactive mismatch to about zero while the resistive mismatch is not changed. Because the reflection coefficient is composed of real and imaginary part, by compensating the reactive mismatch to zero, the imaginary part of the reflection coefficient becomes zero; however, the reflection coefficient could remain large after the adaptation if the real part of the reflection coefficient is dominant. Consequently, this algorithm is most effective if the resistive mismatch is not too large.

This algorithm requires only knowing whether the mismatch is inductive or capacitive, more detailed information about mismatch is not necessary, therefore, this algorithm can be implemented by using the phase detector with one limiter, the simplest digital implementation method. In addition, only the I-output of the phase detector is needed with this algorithm, this means that less hardware is needed and the power consumption is lessened as well.

Since only the polarity of the mismatch needs to be known, this requires that the zero-degree level of the phase detector being accurate, large dynamic range is not necessary.

8 Modelling of the switched-capacitor of the matching network

The matching network of the adaptive antenna matching loop consists of a series-LC network which is composed by a fixed-value inductor and a switched-capacitor array. In order to implement the demonstration loop the switched capacitor needs to be modelled and characterized, therefore the behaviour of the complete demonstration loop can be simulated before real implementation takes place. In this chapter, the switched-capacitor array used for the demonstration loop is introduced first; then the modelling of the switched capacitor is shown, also the simulated and measurement results are presented.

8.1 The switched-capacitor array for the demonstration loop

The switched-capacitor array for the demonstration loop makes use of a quad-band FEM (Front-End Module) evaluation board [14] which consists of four switches made of PHEMT(Pseudomorphic High Electron Mobility Transistors).

The FEM board is a five-port device and its functional schematic is shown in Figure 8.1, the dimensions of the wires are not real, they are just indications. $V_{control2,3,4,5}$ controls the state of the each switch which is connected to one capacitor, two symmetrical-connected such FEM boards compose the switched-capacitor array used in the matching network of the demonstration loop. The behaviour of each switched capacitor on the FEM board is modelled and characterized, this is introduced in the next section.

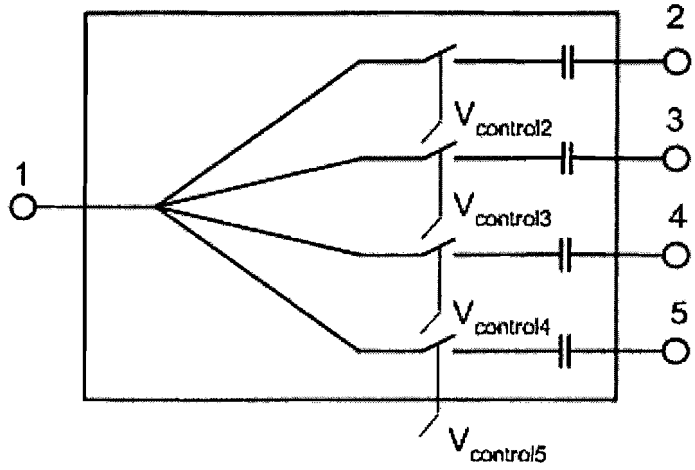

Figure 8.1: Functional schematic of the FEM board, the dimensions of the wires are not real.

8.2 Modelling and characterization of the switched-capacitor

For the demonstration loop, the most important parameter of the switched-capacitor model is the phase shift from port 1 to one of the other four ports, because this adds extra phase shift to the loop, consequently affects the adaptive matching. The paths

from port 1 to port 2 or port 3, 4 and 5 are identical, therefore only one of the paths needs to be modelled and characterized. Two-port S-parameter simulation and measurement have been used, especially the phase of S12 is interesting for the modelling because it represents the phase shift of a signal when it is transmitted from port 1 to port 2.

When modelling the switched-capacitor, the transmission line on the board cannot be ignored, because at high frequencies it causes attenuation and phase shift of the signals. The modelling work has been done in two steps: first the transmission line on the FEM board is modelled; then the transmission line together with the PHEMT and the capacitor are modelled. These two steps are introduced separately below.

8.2.1 Modelling of the transmission line on the FEM board

In order to model the transmission line on the FEM board, a board with the same transmission line (same length, height and width; same material; same trace shape) but without the PHEMT switches is made, and the model of the transmission line together with the parameter values for the transmission line model are shown in Figure 8.2. The two coaxial cable model the two SMA connectors on the board, the three micro strip lines model the transmission line and the two capacitors represents the decoupling capacitors.

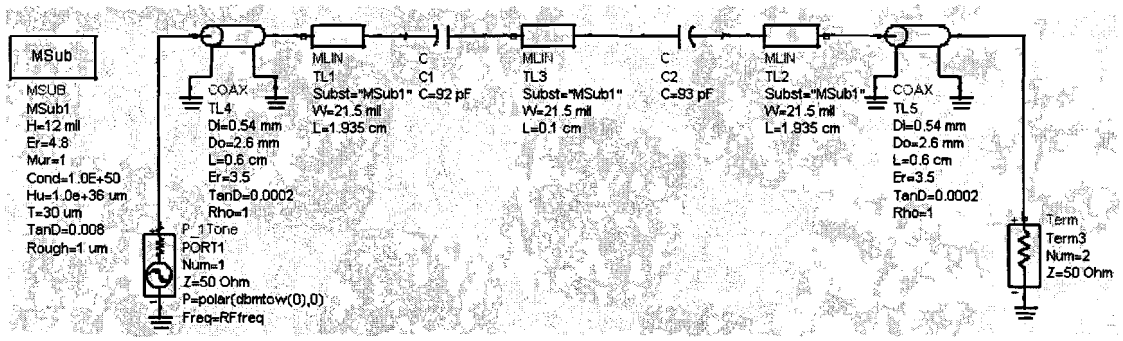

Figure 8.2: Model of the transmission line.

The S-parameter simulation results of the modelled transmission line are shown in Figure 8.3. The S-parameter of the board which is used for modelling of the transmission line is also measured with a network analyser, and the measured S-parameters are shown in Figure 8.4. The simulated and the measured results are similar, the main cause for the small difference between the two results is that it is difficult to model the transition from the SMA connector to the micro strip line in ADS, since the SMA connector and the micro strip line use different materials. Also the nonidealities in the micro strip line contribute to the difference between the simulated and measured results.

8.2.2 Modelling of one switched-capacitor on the FEM board

One switched-capacitor on the FEM board is modelled, the complete model of the FEM board consists four such single-path models and the single-path model is shown in Figure 8.5.

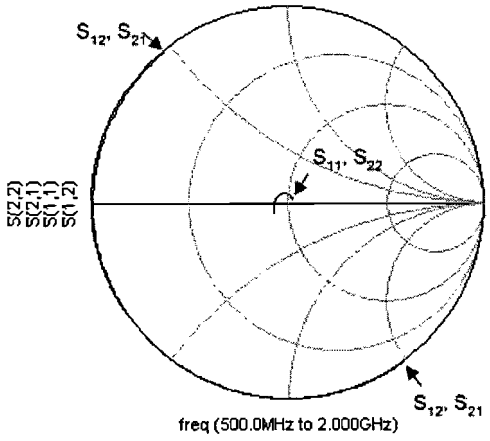

Figure 8.3: Simulated S-parameters for the model of the transmission line. The trajectory of S_{12} and S_{21} coincident with the outermost circle of the Smith chart, the two ends of the trajectory are indicated for clarity.

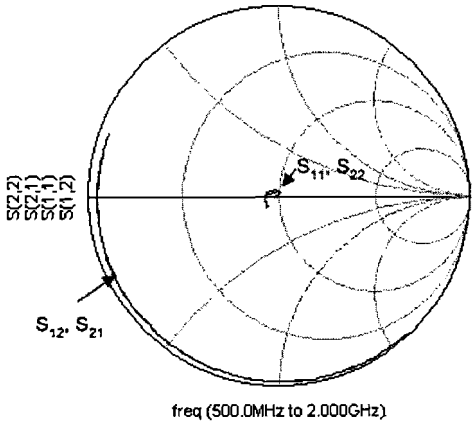

Figure 8.4: Measured S-parameters of the board used for modelling of the transmission line.

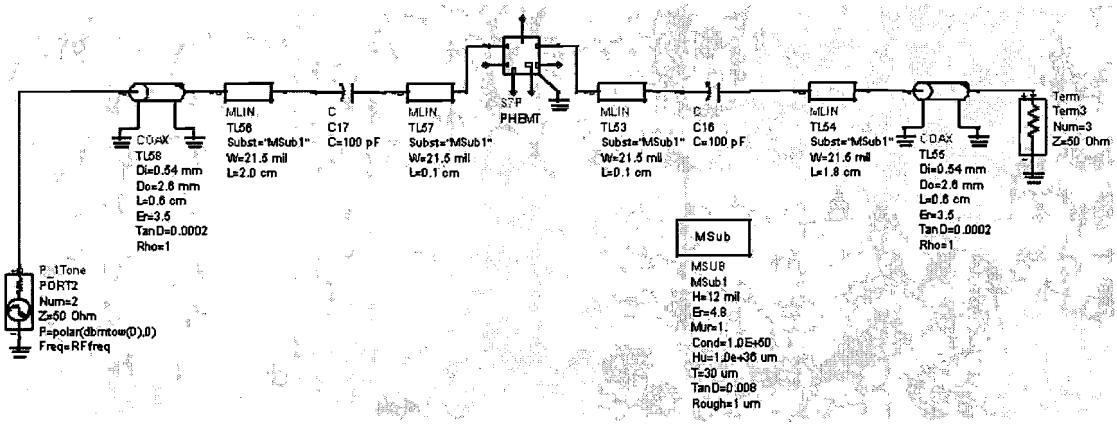

Figure 8.5: Single-path model of the FEM board.

The S-parameter simulation results and the measured S-parameters of a single-path on the FEM board are shown in Figure 8.6 and 8.7, respectively. Again, the two results are similar to each other, especially the modelled and measured S12 at 900MHz have same magnitude and 4° phase difference. This model can be used for further simulation.

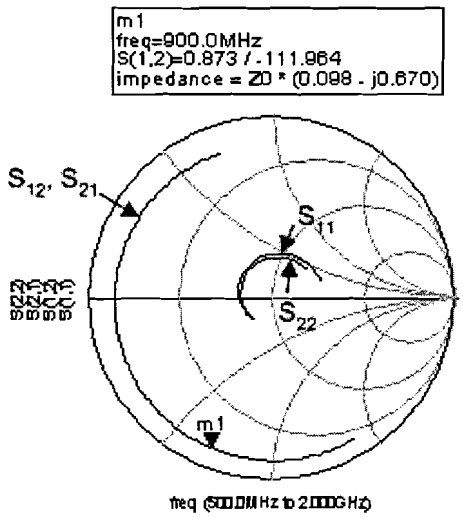

Figure 8.6: Simulated S-parameters for the single-path model of the FEM board.

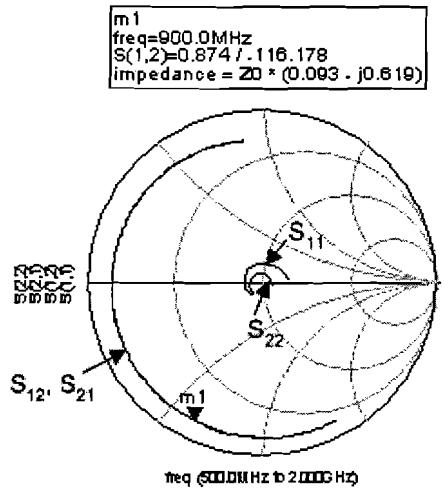

Figure 8.7: Measured S-parameters of the single path on the FEM board.

8.3 Conclusions

Modelling of the switched-capacitor used in the adaptive matching loop for demonstration has been shown. The simulated and measured results are quite similar, the simulated and measured phase of S12 has only a difference of 4 degree, the difference is mainly because that it is difficult to model the transfer from coaxial connector to the micro strip-line with ADS. The model of the switched-capacitor can be used for further simulation.

9 Conclusions

The concept of mismatch detection—reflection-coefficient detection and the circuit of the phase detector for detecting the phase of the reflection coefficient has been shown, also the characterization of the phase detector is presented. An adaptive control algorithm which effectively compensates reactive antenna impedance mismatch is described and the simulation results of the adaptive matching network which implements this algorithm are given. Finally, the modelling and characterization of the switched-capacitor used for the demonstration loop to show the concept of adaptive antenna impedance matching have been introduced.

The phase detector provides both in-phase and quadrature information of the phase of the reflection coefficient, the simulation results have shown that the phase detector works very well and the expected characteristics have been obtained. From the DC measurement results, DC offset exists at the outputs of the phase detector, and it can affect the accuracy of the phase detector depending on how the adaptive matching loop is implemented. If analogue implementation is used, then the DC offset affects the accuracy and because the detector sensitivity is low (1.1mV/degree) the DC offset can cause an error of up to 4 degrees. If (semi)digital implementation is used, then the DC offset might cause error depending on the level of the LSB of the A/D converter. For the simplest form of digital implementation, that is, the A/D converter is an one-bit A/D converter (a limiter), then the DC offset could give wrong polarity of the detected phase.

From the RF measurements, the phase detector performs very well at low frequencies (800MHz-900MHz) but the performance degrades considerably at high frequencies (1800MHz-1900MHz), especially when the input power is low. The performance is evaluated from the viewpoint of accuracy and dynamic range which is defined as the range of phase angles that can be detected within the required accuracy. The dynamic range decreases significantly at high band comparing with that at low band. For analogue implementation, with the specified accuracy of ±4°, the dynamic range is 142° at 900MHz with an input power of 10dBm but 52° at 1800MHz with an input power of –10dBm. With digital implementation, the dynamic range might be larger than that for the analogue implementation depending on the LSB level of the A/D converter. If a limiter is used for the digital implementation, it requires the phase detector be accurate around zero degree and the polarity of the output must be correct, therefore large dynamic range is not necessary but the DC offset is very important in this case.

The presented adaptive-matching algorithm can effectively compensate the reactive antenna mismatch. This algorithm only needs to know whether the mismatch is inductive or capacitive, and this can be easily determined by the polarity of the in-phase output of the phase detector. Therefore, only half of the designed phase-detector is needed, this means less hardware, less cost and less power consumption. The limitation of this control algorithm is that it does not compensate resistive mismatch, if the resistive mismatch is significant, the reflection coefficient is still large though the reactive mismatch is compensated to zero after compensation. The adaptive matching loop based on this algorithm is implemented with the phase detector, a limiter, a counter and a series-LC network which includes an inductor and a 4-bit

switched-capacitor array. From simulation results, an inductive mismatch of $j83\Omega(|\Gamma|=0.6)$ is compensated to $j8\Omega(|\Gamma|=0.13)$ by using this adaptive matching network.

The switched capacitor used for implementation of the demonstration loop is modelled and characterized, the simulation and measurement results matches with each other well, the simulated and measured phase of S12 is 4 degree. The difference is because that it is difficult to model the transfer from the coaxial connector to the micro strip line with ADS. The model can be used for further simulation of the demonstration-loop model.

10 Recommendations

The first recommendation is to finish implementation of the demonstration loop to verify the operation of the adaptive matching loop. The second recommendation is to do research on the limiter used in the phase detector, since the performance at high band and low input power is significantly degraded, the possible reason is that at high band the linear gain is lowered due to parasitic capacitances, therefore for the low-power input signals, at the output they can not reach the desired saturation level, thus the performance is degraded. However, because there is no connection for the limiter on the die of the phase detector, therefore this has not been measured.

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Appendix A: Circuit of the phase shifter

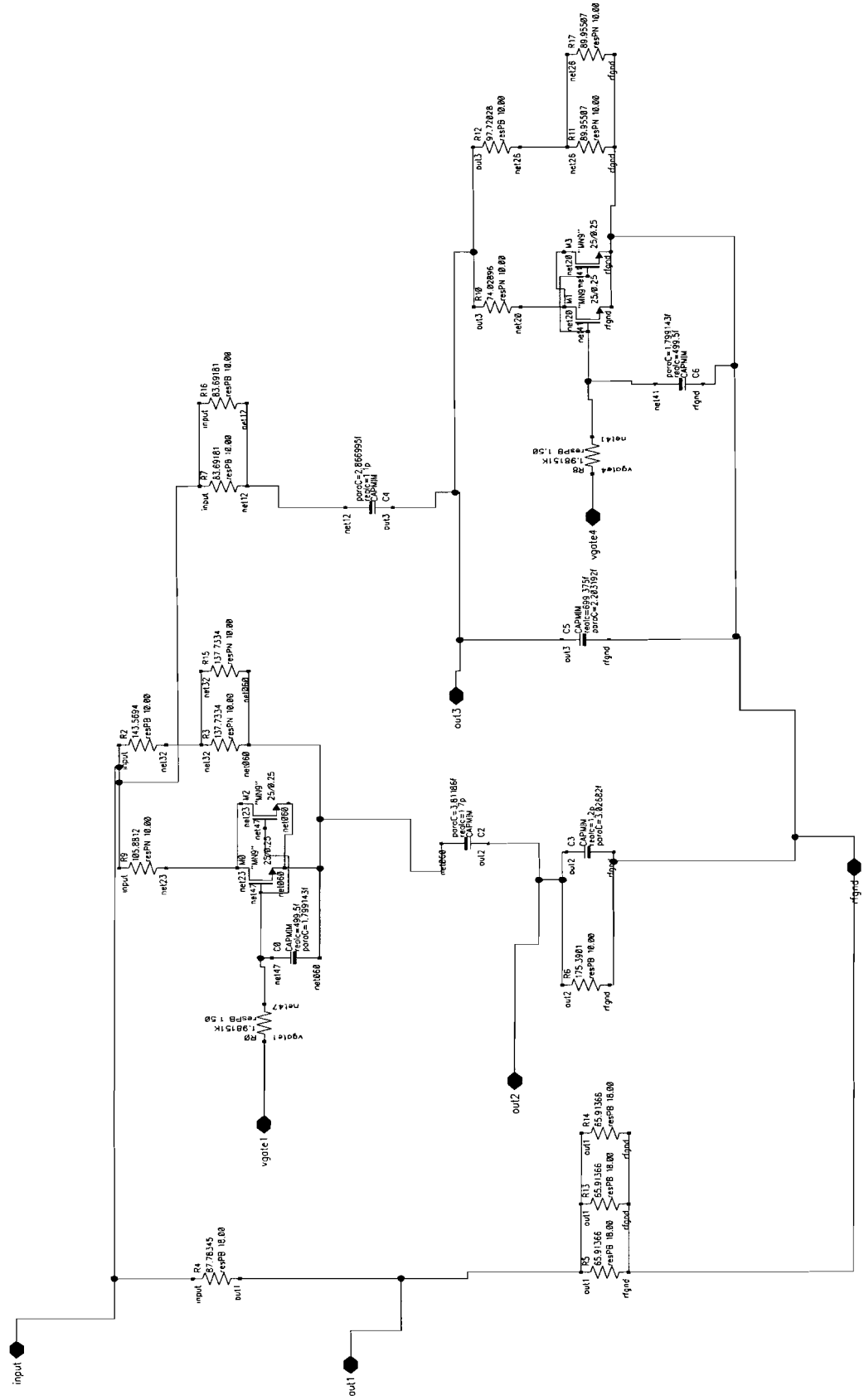

Figure A. 1: The all-pass network of the phase shifter.

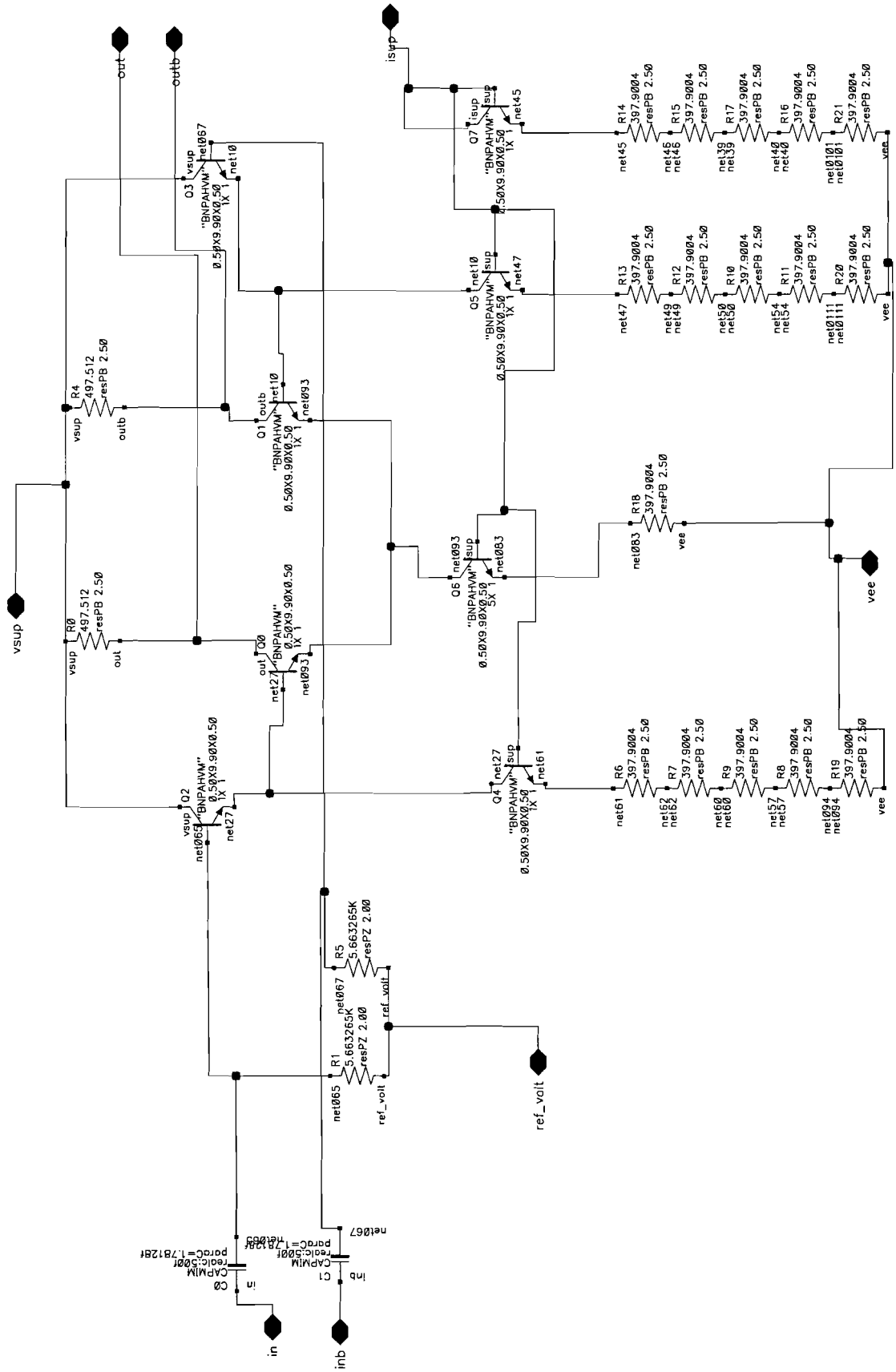

Figure A. 2: The differential amplifier of the phase shifter.

Appendix B: Circuit of the differential pair for the limiter

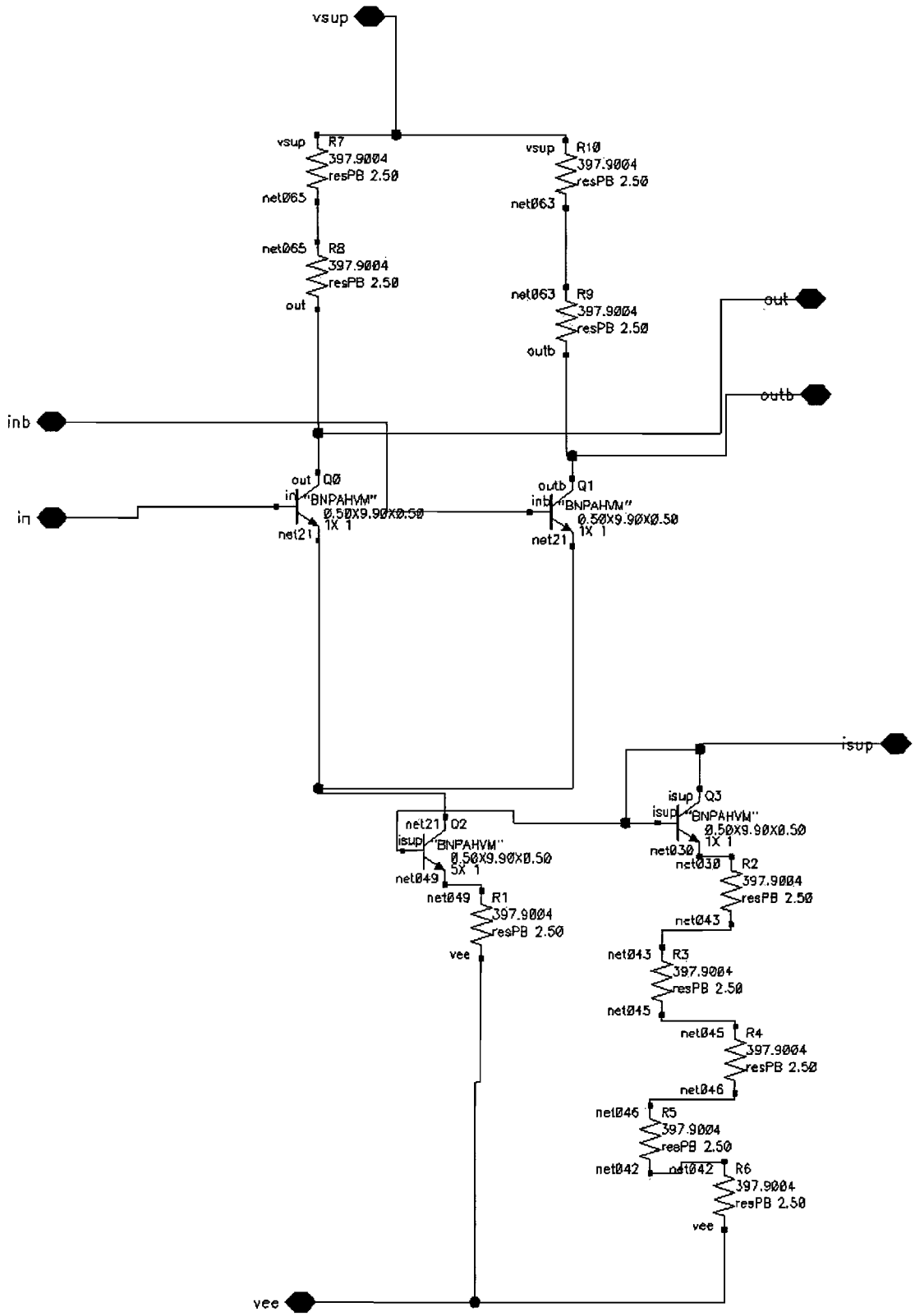

Figure B. 1: The differential pair used in the limiter.

Appendix C: Circuit of the Gilbert multiplier

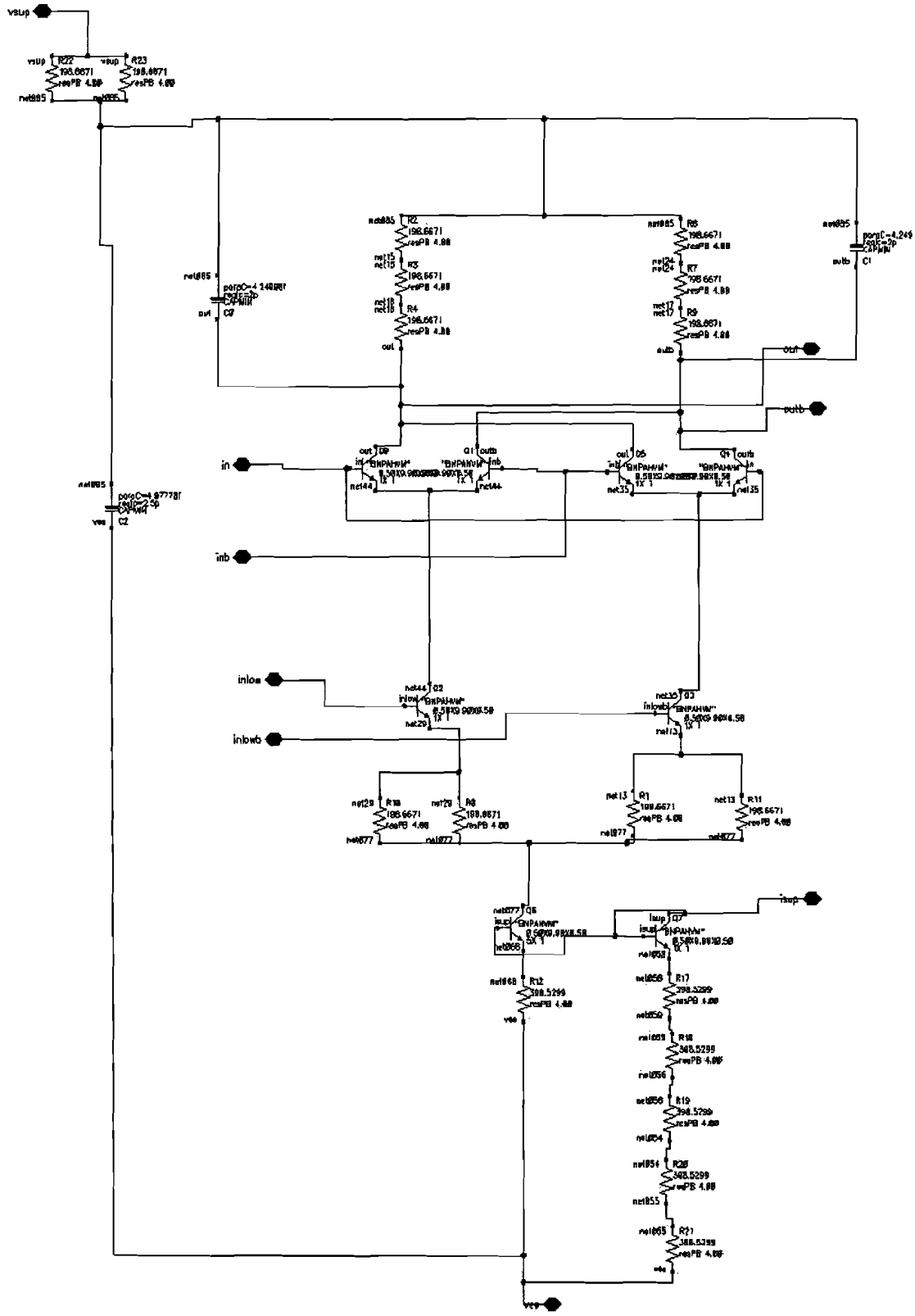

Figure C. 1: The Gilbert multiplier.

Appendix D: Circuit of the phase detector

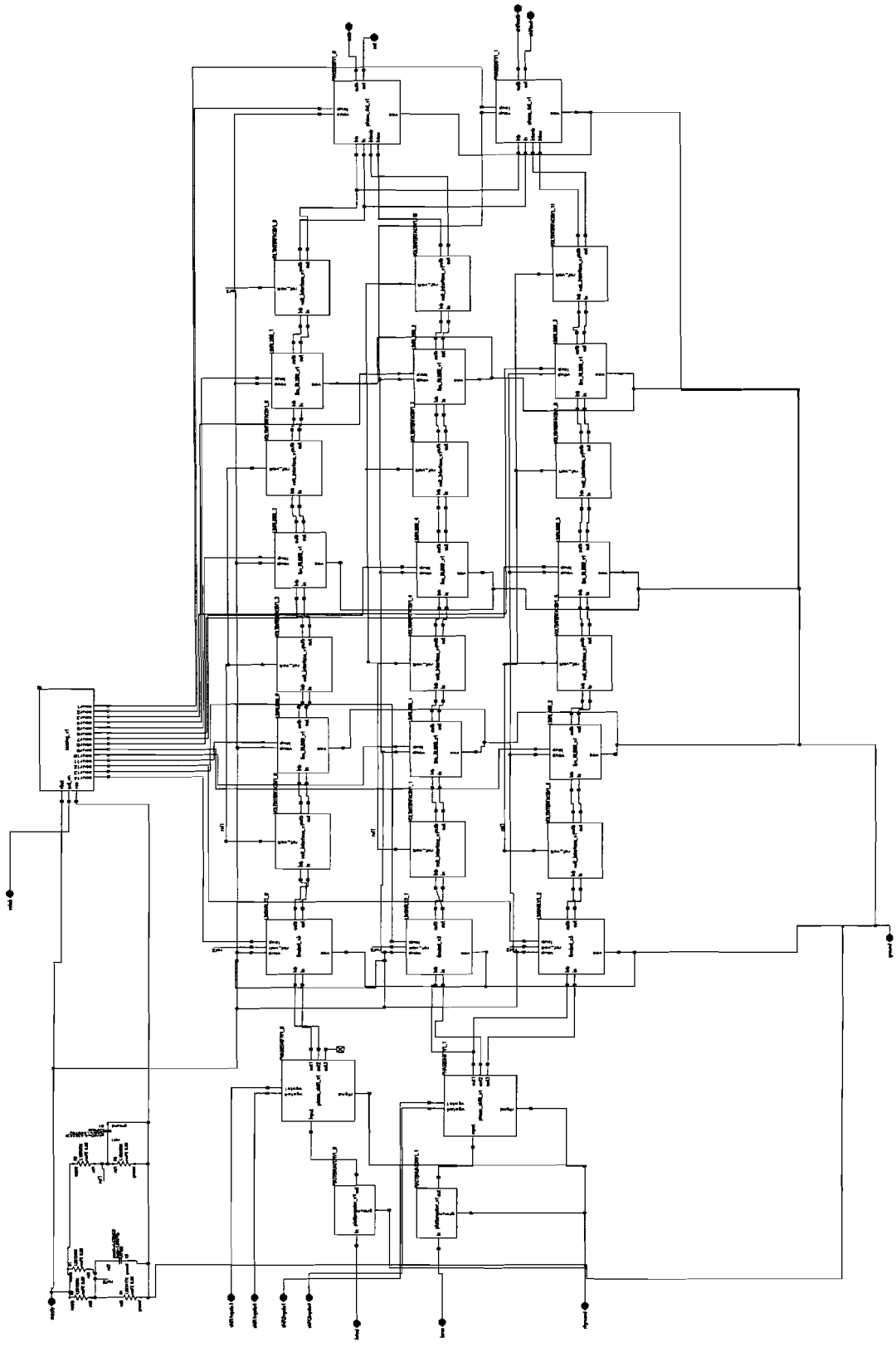

Figure D. 1: Circuit of the phase detector.

Appendix E: Output characteristics of the phase detector

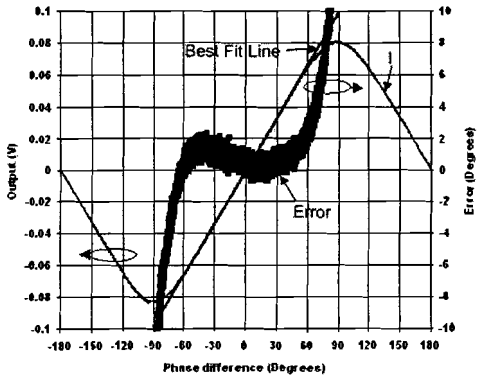

Figure E. 1: In-phase output characteristic at 900MHz, P_{in}=10dBm.

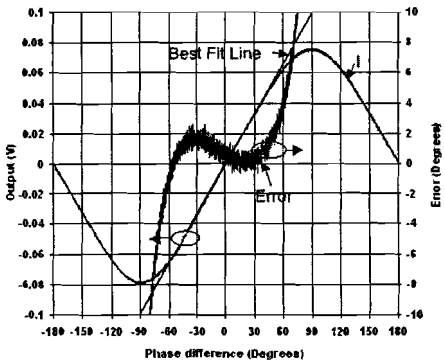

Figure E. 2: In-phase output characteristic at 900MHz, P_{in}=-10dBm.

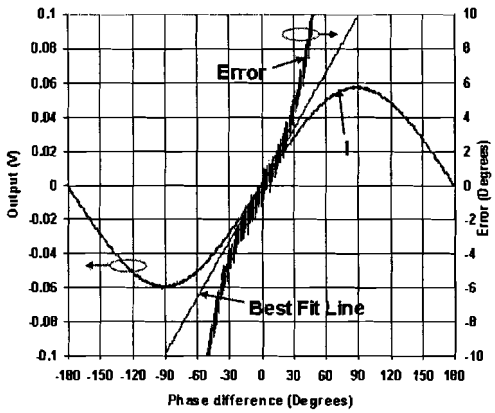

Figure E. 3: In-phase output characteristic at 900MHz, P_{in}=-20dBm.

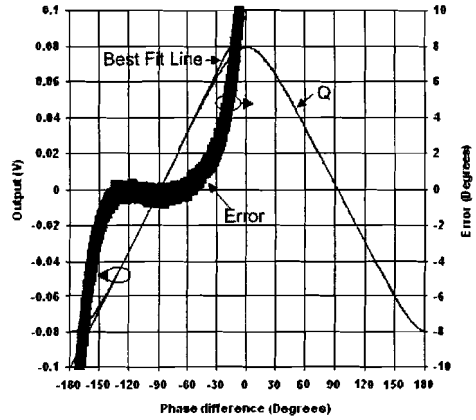

Figure E. 4: Quadrature output characteristic at 900MHz, P_{in}=10dBm.

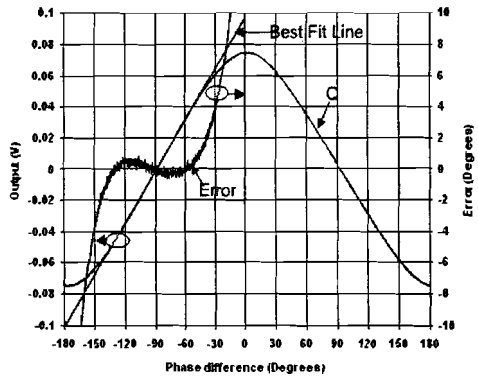

Figure E. 5: Quadrature output characteristic at 900MHz, P_{in}=-10dBm.

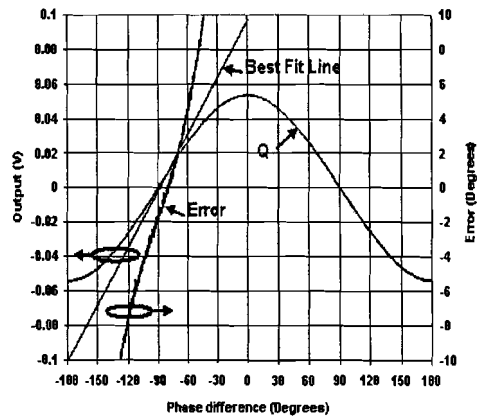

Figure E. 6: Quadrature output characteristic at 900MHz, P_{in}=-20dBm.

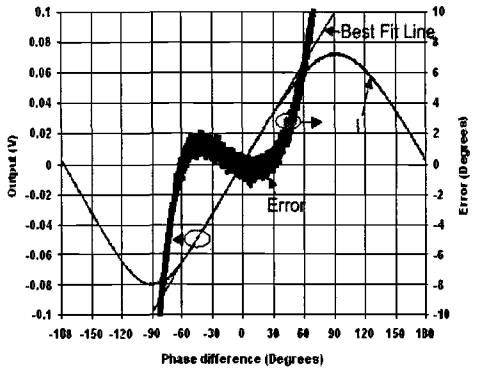

Figure E. 7: In-phase output characteristic at 1800MHz, P_{in}=10dBm.

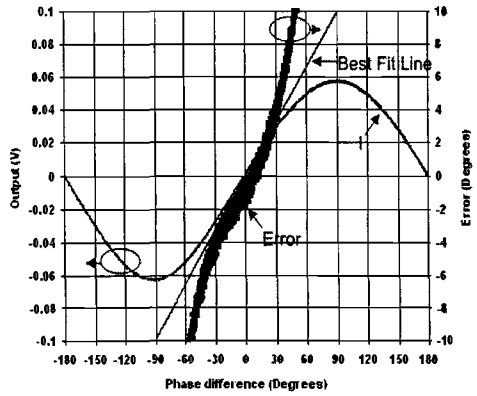

Figure E. 8: In-phase output characteristic at 1800MHz, Pin=-10dBm.

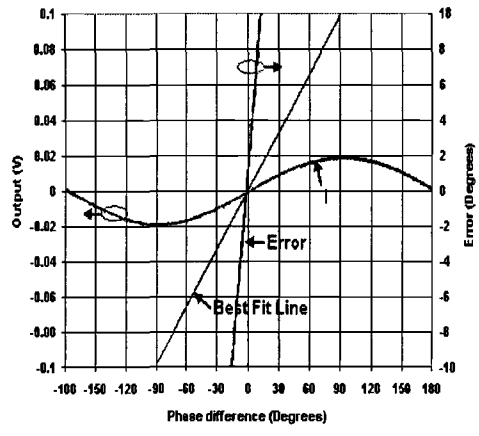

Figure E. 9: In-phase output characteristic at 1800MHz, P_{in}=-20dBm.

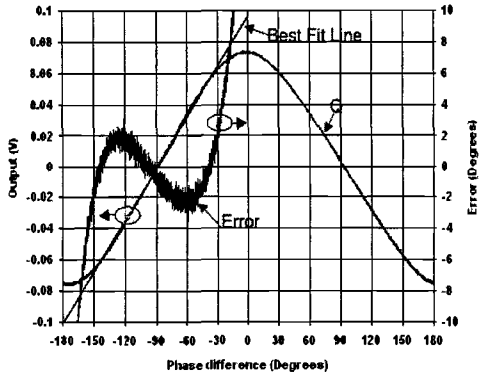

Figure E. 10: Quadrature output characteristic at 1800MHz, P_{in}=10dBm.

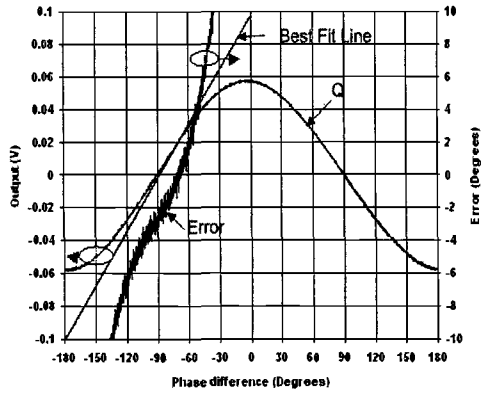

Figure E. 11: Quadrature output characteristic at 1800MHz, P_{in}=-10dBm.

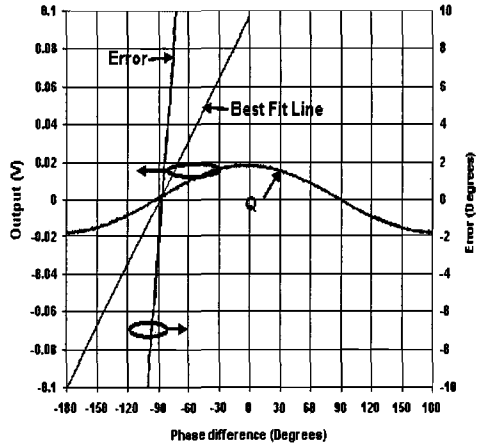

Figure E. 12: Quadrature output characteristic at 1800MHz, P_{in}=-20dBm.

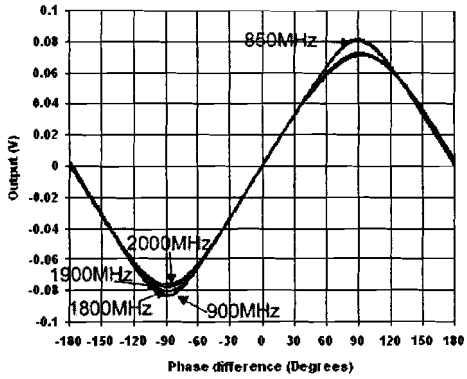

Figure E. 13: In-phase output characteristics at 850, 900, 1800, 1900 and 2000MHz, P_{in} =10dBm.

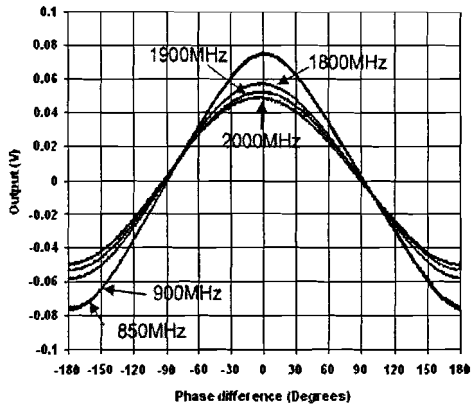

Figure E. 16: Quadrature output characteristics at 850, 900, 1800, 1900 and 2000MHz, P_{in}=-10dBm.

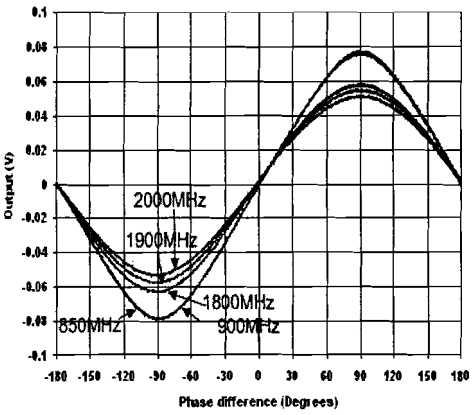

Figure E. 14: In-phase output characteristics at 850, 900, 1800, 1900 and 2000MHz, P_{in}=-10dBm.

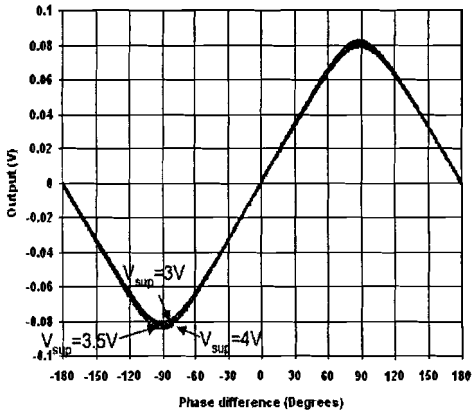

Figure E. 17: In-phase output characteristics at 900MHz with V_{sup} = 3V, 3.5V, 4V.

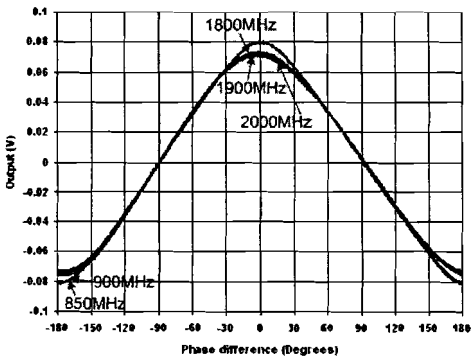

Figure E. 15: Quadrature output characteristics at 850, 900, 1800, 1900MHz, P_{in}=10dBm.

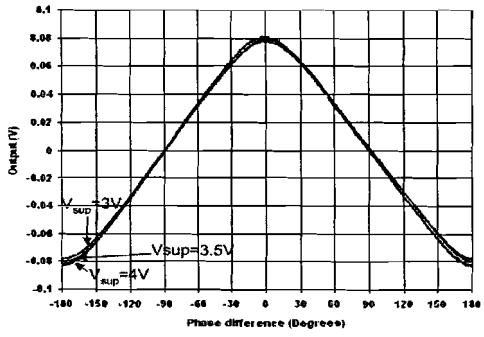

Figure E. 18: Quadrature output characteristics at 900MHz with V_{sup} = 3V, 3.5V, 4V.

Appendix F: Used measurement apparatus

Table F. 1: The used measurement apparatus.

Apparatus	Model no.	Manufacturer	Specifications
Oscilloscope	TDS3054B	Tektronix	500MHz 5GS/s
Spectrum analyser	HP8595A	HP	9kHz~6.5GHz
Signal generator	HP8648A	HP	100kHz~3.2GHz
	R&S SMT03	ROHDE&SCHWARZ	5kHz~3.0GHz
DC power supply	3610A	HP	0-8V, 0-3A 0-15V, 0-2A
	6284A	HP	0-20V, 0-3A
	E3631A	HP	0-6V, 5A 0-±25V, 1A
Network analyser	PNA E8358A	Agilent	300kHz~9GHz
Multimeter	34401A	HP	
	2700	KEITHLEY	