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Integrated cooling in silicon

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Integrated cooling in silicon

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May 14, 2004

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Abstract

In this report two different types of integrated cooling mechanisms will be investigated. The first one is cooling by combined thermo tunneling and thermionic emission in vacuum. The second method is cooling by forced water convection through micro-channels.

The feasibility of the concept for cooling by combined thermionic emission and thermo tunneling to vacuum will be reviewed. In theory, a combination of a strong electric field (>10^6 V/cm) and an image charge potential can significantly lower the work function, which may open the possibility for cooling at room temperature by combined thermionic emission and thermo tunneling. However, due to numerous practical problems, such a cooling device is not possible within the present experimental tolerances.

Integrated micro-channels, processed in silicon, directly underneath an electronic circuit for on-chip cooling with forced water convection has been investigated both theoretically and experimentally. In a 1-cm^2 experimental device 370 W was dissipated without exceeding the critical junction temperature of 120 °C at a flow rate of only 0.1 l/min and a pressure drop of 0.15 bar. The minimum thermal resistance, which is measured, is 0.08 K/W for a power dissipation of 428 W at a flow rate of 1.1 l/min. This more than satisfies the requirements for cooling of next generation CPUs. The experimental results are compared to numerical calculations. For low flow rates there is a very good agreement. For higher rates, the flow is not fully developed and becomes turbulent, which results in an even better performance as predicted by the numerical calculations. There are several opportunities available to improve the cooling performance.

Technology assessment

As integrated circuits become faster and more densely packed with transistors, the power density increases and the heat generated, due to the electrical resistance of the large number of interconnects, becomes a problem. In addition, the area available for heat removal decreases. As a result, thermal management becomes increasingly critical to the electronics industry.

The reliability of semiconductor devices depends on the temperature reached during operation. This interrelation between reliability and temperature is the result of both direct and induced mechanisms. Direct mechanisms are caused by the relationship between the temperature and the rate of diffusion or chemical reactions, which frequently lead to chip failure. These mechanisms are exponentially dependent on the operating temperature and hence, the package reliability. The induced mechanisms are directly related to thermal stresses inherent within the chip and typically result in failure caused by fatigue of the mechanical devices or connections. In addition, many of the physical and chemical processes that can cause chip failure are accelerated by elevated temperature. This all is why heat buildup is becoming one of the major limitations to creating tomorrows more compact and complex microelectronics devices. The increasing integration of electronic systems is leading to challenges for the thermal design of an integrated cooling device directly underneath the electronic circuit, to remove the heat from the circuit and transport it to other places. By separating the heat source from the area where the heat is released to the ambient, the area available for heat removal can be increased, and hot spots in the electrical devices can be prevented.

The possible methods to cool an electronic system vary widely [1]. Because in most systems the space available for the cooling device is limited, not all methods are possible. Consequently, research on cooling concepts is focused on integrated micro cooling devices.

In this report two different types of integrated cooling mechanisms will be investigated. The first one is cooling by combined thermo tunneling and thermionic emission in vacuum. The second method is cooling by forced water convection through micro-channels.

[1] C.S. Nicole, "Alternative cooling techniques," Nat.Lab. Technical Note 2002/224, July 2002.

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PART I

Cooling by combined thermo tunneling and thermionic emission in vacuum

Chapter 1

Introduction

Solid-state coolers, like thermoelectric coolers have many advantages over conventional refrigerators. They have the advantage of not having moving parts, nor any type of fluid. Therefore, they produce minimum of noise and can be made very compact. Furthermore, thermoelectric refrigeration avoids the use of environmentally hazardous chlorofluorocarbons (CFC's) used in most compressor-based refrigeration. However, it has a small efficiency and only a small temperature difference can be maintained in a single stage thermoelectric cooler.

In thermoelectric refrigerators or generators [1], electrons serve as both entropy and charge carriers in solids. In linear approximation, the effectiveness of heat and electric power conversion depends only on a single dimensionless material parameter ZT:

$$ZT = \frac{\Pi^2}{\rho \kappa T}, \tag{1.1}$$

where Π [WA^{-1}] is the Peltier coefficient which is equal to the entropy flow divided by the charge flow carried by the electric current, ρ [Ωm] the electrical resistivity and κ [$WK^{-1}m^{-1}$] the thermal conductivity. It is important to reduce the thermal conductivity and electrical resistivity as much as possible in order to have a better thermoelectric material, as can be seen from equation 1.1. Since electrons serve as both heat and charge carriers in solids, it has been a difficult task to find a good thermoelectric material.

An alternative cooling mechanism is thermionic refrigeration, which is based on the principle of thermionic emission. In thermionic emission, two electrodes are used, an emitter and a collector (or cathode and anode), separated by vacuum with a bias potential applied (Fig. 1). On the emitter side, a heat source is attached, which results in an increased electron temperature. Those electrons that are thermally excited and have enough energy to surmount the barrier (called work function, denoted by Φ, this is the minimum amount of energy an individual electron has to gain to escape from a particular surface) will escape into the vacuum. The emitted electrons travel ballistically toward the anode, arrive at the anode, and give off their heat. On the emitter side, an electron is replaced at the Fermi level to maintain charge neutrality. Thus there is a net transport of heat equivalent to the work function per emitted electron, and the emitter is cooled.

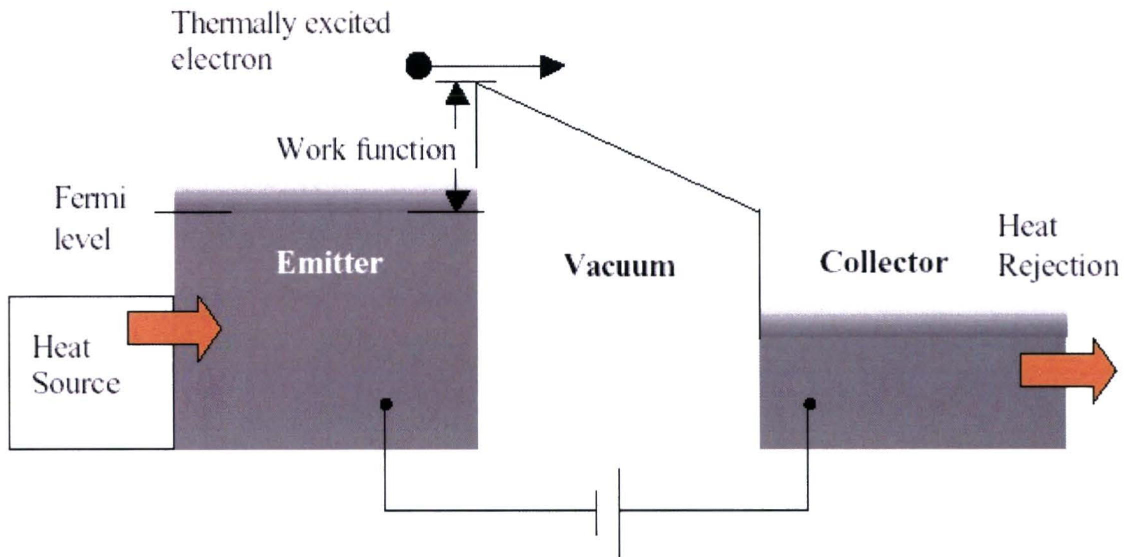


Figure 1. Thermionic emission of electrons.

Thermionic emission across a vacuum gap promises to have a much higher figure of merit (*ZT*, equation 1.1) than a solid thermoelectric because there is no lattice thermal conductivity, there is no ohmic resistivity due to the absence of electron scattering in the vacuum, because they travel ballistically. A result of the absence of heat dissipation in the vacuum is that all the heat is pumped to the hot side of the cooling device (collector). The effective Peltier coefficient is also greater than that of thermoelectric materials. Other advantages of thermionic emission are that the only possible heat backflow through the vacuum is by radiation, which is ~ 0.1 W/cm^2 for black body radiation at room temperature.

Mahan theoretically studied the possibility of vacuum thermionic refrigeration [2]. To make a thermionic cooling device, which can operate at room temperature, an anode with a work function of 0.4 eV is needed. However, it seems unlikely that such low values of work function will be found. As a result of this, room temperature cooling with use of only thermionic emission seems to be not possible. The lowest work functions for materials at room temperature are around 0.7-0.8 eV. This value of work function permits a thermionic refrigerator whose cold temperature is 500 K, but this temperature is too high for most electronic devices. So additional reduction of the barrier of 0.4 eV is necessary for thermionic emission at room temperature.

It is known that the energy barrier near a surface is significantly distorted by a strong applied electric field and by the image charge of the emitting electron itself. The distortion causes the barrier height reduction, which is generally known as the Schottky effect. The Schottky effect reduces the effective barrier height by few tenths of an eV when an electric field in order of 10^6 V/cm is applied. In order to produce such a strong field, a high potential usually needs to be applied between the emitter and the collector. For example, if the emitter-collector separation is 10 μm, the required potential is over 1000 V, which makes the thermionic cooling very inefficient and impractical. In order to make thermionic cooling efficient and competitive, at room temperature, with other cooling methods, the emitter-collector gap must be reduces to 1-10 nm. Such a narrow gap and a

strong electric field also make it possible for electrons to tunnel through the barrier to the collector.

So by combining low work function materials and making controlled nanometer gaps, with vacuum between the emitter and collector and an applied bias voltage, there seems to be a window of opportunity for achieving the low barrier potential condition necessary for room temperature thermionic emission.

Chapter 2

Theory

2.1 Theory of thermionic emission

In a metal or semiconductor at non-zero temperature, free electrons move around in a random manner whose velocity distribution it determined by the temperature. Some electrons have enough kinetic energy to escape from the surface of the solid. The energy necessary for an electron to escape from the surface of solid into the vacuum is called the work function of a material and is denoted by Φ. More electrons are emitted into the vacuum as temperature is increased or the work function is decreased.

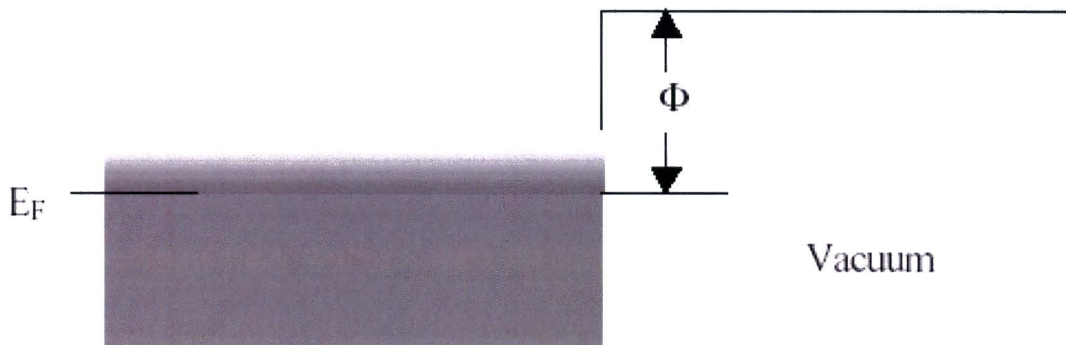


Figure 2. Potential barrier at the metal/semiconductor-vacuum boundary.

The probability that an electron energy level E will be occupied in an ideal electron gas in thermal equilibrium is given by the Fermi-Dirac distribution:

$$f(E)=\frac{1}{1+\exp\left[\frac{(E-E_F)}{k_BT}\right]}, \tag{1.2}$$

where E_F [J] the Fermi energy level, k_B [JK^{-1}] the Boltzmann constant and T [K] the temperature. When the Fermi energy level is set to zero by definition, than the number of electrons incident on unit area in unit time with kinetic energy in x direction in the range E_x, E_x+dE_x is given by:

$$N(E_x)=\frac{mk_BT}{2\pi^2\hbar^3}\ln\left[1+\exp\left(-\frac{E_x}{k_BT}\right)\right], \tag{1.3}$$

where m the mass of an electron and $\hbar$ [Js] the constant of Planck divided by 2π. Electrons whose E_x is greater than the work function of the material will escape into vacuum, so the

total thermionic emission current density is obtained by integrating all electrons having $E_x > q\Phi$:

$$J_R(T) = \frac{mqk_B^2T^2}{2\pi\hbar^3}\exp\left(-\frac{q\Phi}{k_BT}\right), \tag{1.4}$$

with q the charge of the electron.

This well-known result is called the Richardson equation. As seen in this equation, a small variation in work function caused by a change in surface conditions produces a significant change in amount of electron emission. To obtain a reasonable amount of thermionic current (~1 A/cm^2 [2]) at room temperature, a work function of 0.4 eV or less is necessary. However, the work function of clean silicon is 4.7 eV. It is possible to lower the work function by evaporating alkali metals onto the surface. Alkali metal sub-monolayer coverage onto a surface is known to produce work functions lower than that of bulk values of alkali metals (Fig. 3).

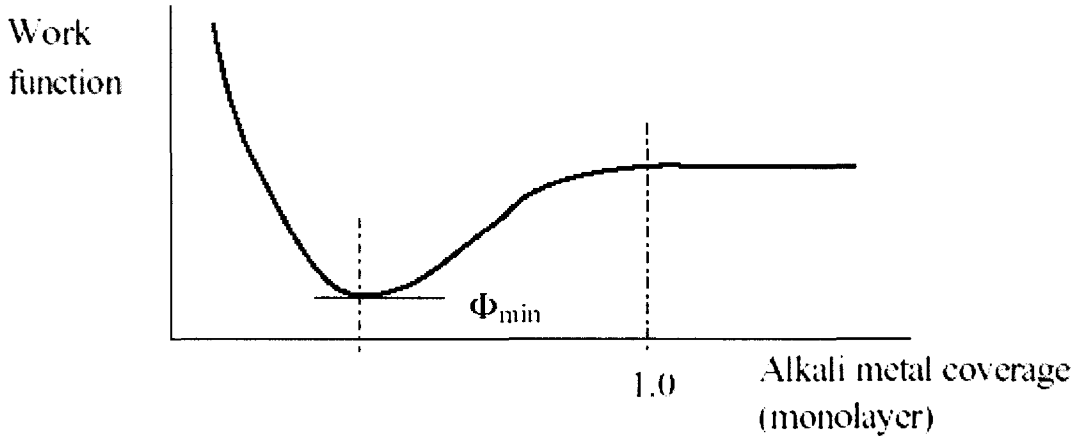


Figure 3. Schematic of work function vs. alkali metal coverage.

Oxygen additives can achieve further lowering of the work function. It is possible to create work functions around the 1 eV [3]. This is already a good start to get a low barrier needed for thermionic emission.

The amount of energy carried by thermionically emitted electrons can be found similarly. The mean kinetic energy of electrons in the transverse directions is ½ k_BT each according to the equipartition theorem. Therefore, the thermal flow density is given by:

$$Q_R(T) = \int_{q\Phi}^{+\infty}(E_x + k_BT)N(E_x)dE_x = J_R(T)\left(\Phi + \frac{2k_BT}{q}\right). \tag{2.5}$$

To collect the thermionically emitted electrons, an electric field is applied between an emitter and a collector. In addition to this linear field, an electron also experiences a force due to its image charge. Accordingly to this image charge, the potential profile of an electron is modified as seen in Fig. 4.

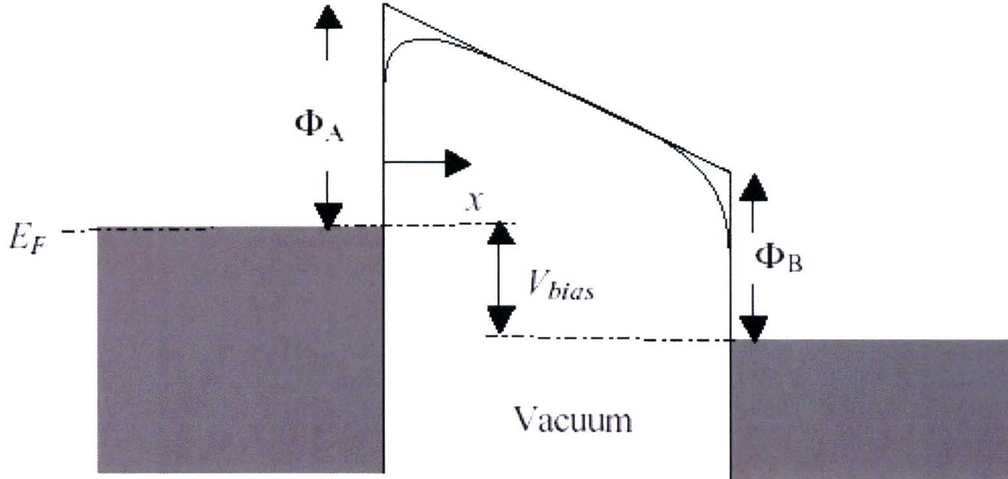


Figure 4. Potential barrier between two electrodes modified by image charges.

The potential of an electron between two conductors is given by [3]:

$$V(x) = \frac{\Phi_A}{q} - \frac{V_{bias} + \Phi_A - \Phi_B}{d} x - \frac{q}{4\pi\varepsilon_0}\left[\frac{1}{4x} + \frac{1}{2}\sum_{n=1}^{\infty}\left(\frac{nd}{n^2d^2 - x^2} - \frac{1}{nd}\right)\right], \tag{1.6}$$

where d is the gap between the electrodes and V_{bias} is the applied bias voltage. The last summation terms are included to account for an infinite number of the image charges reflected on both emitter and collector surfaces. The maximum of the potential barrier is no longer located at $x = 0$, but is located at some distance away from the emitter surface. The maximum height of the barrier is also reduced, which lowers the effective work function and increases the amount of thermionic emission. This increase in current is called the Schottky effect, and is appreciable with fields in order of 10^4 V/cm or greater. Figure 5 shows barrier height reduction due to the Schottky effect as function of emitter-collector separation for various applied bias voltages. The emitter and collector are assumed to have the same work functions in this calculation. As seen from this graph, the barrier height decreases by several tenth eV when the field strength is on the order of 10^6 V/cm range. This electric field corresponds to gaps of a few nanometers to a few tens of nanometer when the applied bias voltage is a few volts.

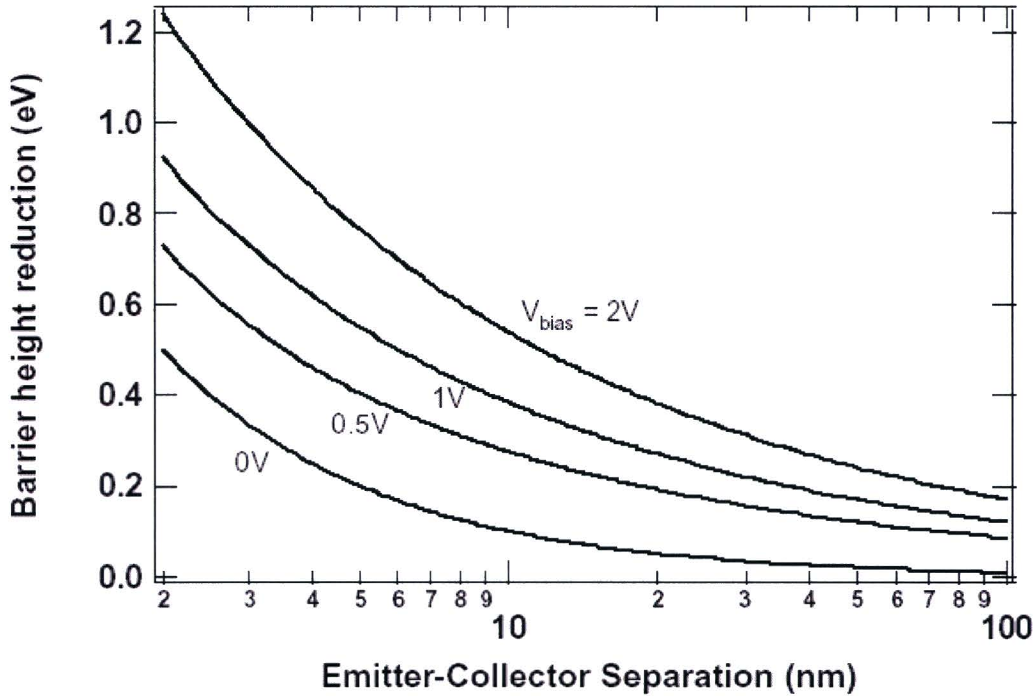


Figure 5. Barrier height reduction due to Schottky effect for various applied voltages, both electrodes are assumed to have the same work function.

With the barrier height reduction as result of the Schottky effect and the work function lowering by covering the surface with a sub-monolayer of an alkali metal with oxygen additives is it possible to create barrier heights around the 0.4 eV, or even lower. With such a lower barrier it is theoretically possible to make a thermionic refrigerator working at room temperature.

2.2 Theory of thermo tunneling

Field emission is another mechanism for extracting electrons from the surface. Such emission occurs when a very strong electric field is applied, reducing the potential barrier width and making it permeable for electrons to tunnel.

The probability that an electron will penetrate a potential barrier of height $V(x)$ (assuming the barrier to be in the x-direction) can be found by the Wentzel-Kramer-Brillouin (WKB) approximation:

$$D(E_x) = \exp\left[-\frac{2}{\hbar}\int_{x_b}^{x_a}\sqrt{2m(V(x)q - E_x)}dx\right], \quad (1.7)$$

where x_a and x_b are the roots of $V(x)q-E_x=0$ (Fig. 6), $V(x)$ defined by equation 1.6 and $E_x=\frac{1}{2}m_e v_x^2$.

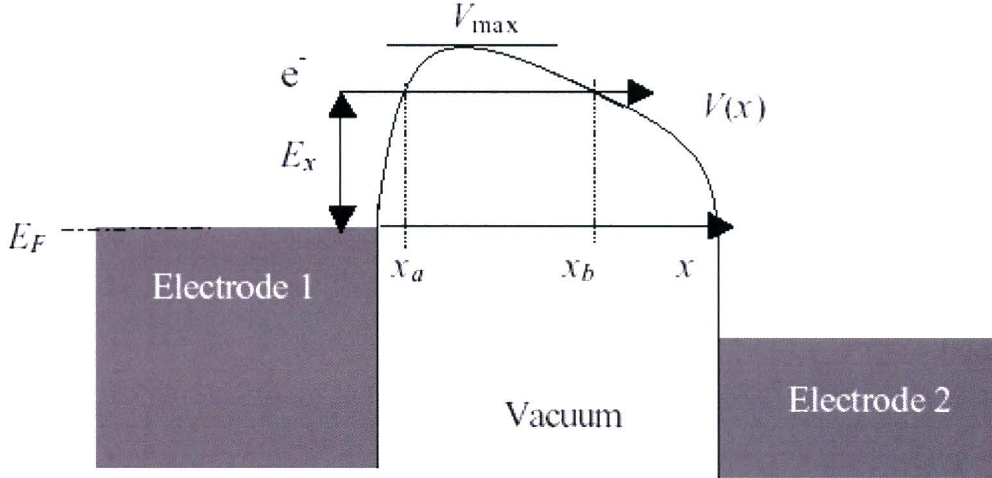


Figure 6. Potential barrier between two electrodes with an electron tunneling through the vacuum.

Assuming that the electrons are at thermal equilibrium, the tunneling current is obtained by:

$$J_{tun} = q\int_{-\infty}^{qV_{max}} D(E_x)N(E_x)dE_x, \tag{1.8}$$

where $N(E_x)$ is the number of electrons incident on unit area in unit time with kinetic energy in x direction in the range E_x, E_x+dE_x, as given by expression 1.3. The amount of energy carried by the tunneling electrons is similarly obtained by:

$$Q_{tun}(T) = \int_{-\infty}^{qV_{max}} (E_x + k_B T)D(E_x)N(E_x)dE_x, \tag{1.9}$$

$k_B T$ is included to account for kinetic energy in transverse directions.

To maintain the charge neutrality of the emitter electrode, the emitted electrons are replaced by electrons at the Fermi level. This is why it is important to prevent that also a lot of electrons below the Fermi level will tunnel. Because when there is a significant amount of emission originating below the Fermi level, the emitter will become hot instead of cold. For this reason, the potential barrier cannot be to low.

Chapter 3

Calculation of expected cooling power by combined thermionic emission and thermo tunneling.

As discussed in the two previous sections, work functions around 1 eV can be obtained by forming sub-monolayer coverage of alkali metals with oxygen additives. Further reduction in the barrier height is possible by application of a strong electric field and because of image charges of emitting electrons as already mentioned. A work function reduction of 0.3 - 0.5 eV is expected for $E = 1 \sim 2 \cdot 10^6$ V/cm or bias voltage of $1 \sim 2$ V across a 10 nm gap. This chapter illustrates calculations performed to estimate current and cooling power densities for emitters with work functions of $0.8 \sim 1.2$ eV.

3.1 Electron energy distribution

At thermal equilibrium, the electrons in a metal or semiconductor have an energy distribution given by the Fermi-Dirac distribution function. The electrons, which have enough energy to surmount or penetrate the potential barrier at the surface, will escape into the vacuum and travel to the collector. The electrons emitted from the surface form a new energy distribution after being filtered by the potential barrier. Therefore, it is important to keep track of the energy distribution of the electrons in order to calculate the energy carried by the electrons.

An example of an electron energy distribution for a conventional thermionic device is shown in Fig. 7. The work function is 2.0 eV, the applied bias is 1.0 V, the distance between electrodes is 0.1 mm and the temperature is 1500 K.

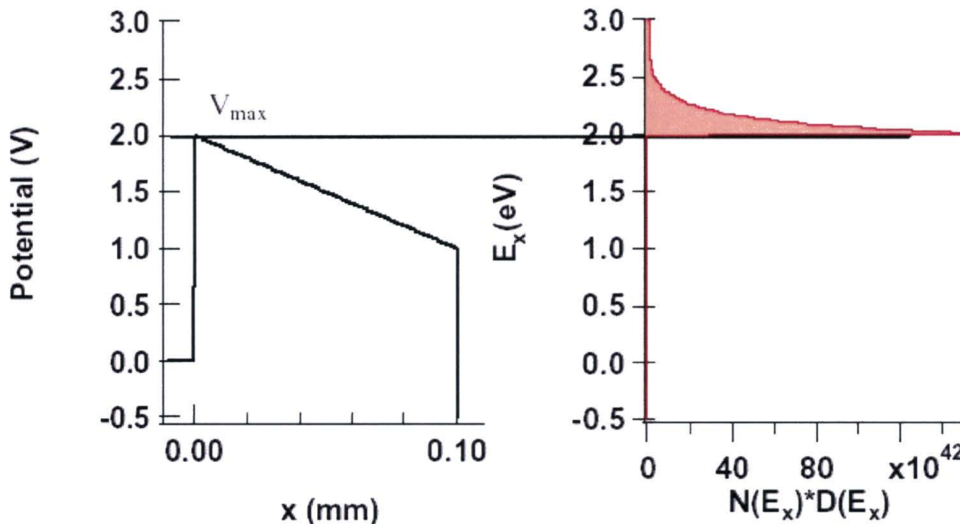


Figure 7. Potential profile and electron energy distribution for conventional thermionic emission. Φ = 2.0 eV, the applied bias is 1.0 V, the distance between electrodes is 0.1 mm and the temperature is 1500 K.

In this example, the vast majority of the electrons that escape into the vacuum have energies greater than the potential barrier height, because the tunneling current is negligible due to the relatively small electric field and large vacuum gap. Because of the high temperature, there are a significant number of electrons populating the high-energy states. For this nearly pure thermionic emission case, the Richardson equation (1.4) can be employed to find the current density. When the temperature is around 300 K (room temperature), almost no electrons populate the high-energy states. This implies that at room temperature there are almost no electrons that are able to escape into the vacuum and there is almost no thermionic current. Consequently the thermionic cooler will not work at a room temperature, when the work function is 2.0 eV.

Figure 8 shows an electron energy distribution for a much smaller gap as proposed for the integrated cooling of IC's. In this example, the gap between emitter and collector is only 60 Å, the bias voltage is 1.6 V, the temperature is 300 K and both electrodes have a work function of 1.0 eV.

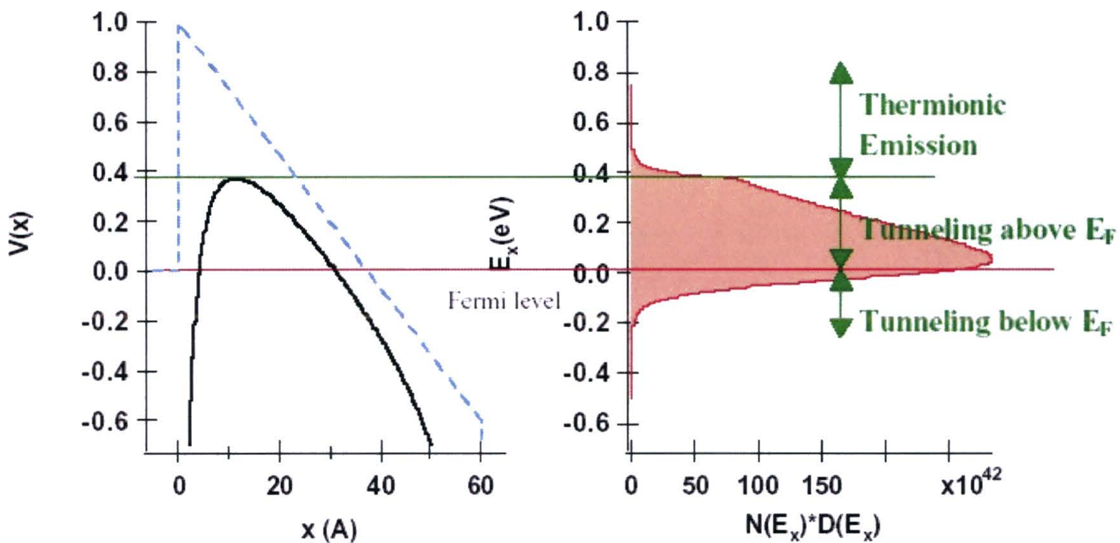


Figure 8. Potential profile and electron distribution for a very narrow electrode separation at 300 K. The applied bias voltage is 1.6 V, the emitter-collector distance is 60 Å and the work function is 1.0 eV for both electrodes. The dominant emission comes from tunneling above the Fermi level. The dashed line is the potential profile without distortion due to the image charge effect.

The barrier height, as calculated with equation 1.6, is significantly reduced, from $\Phi = 1.0$ eV to 0.375 eV, a reduction of 0.625 eV, due to a distortion of the potential profile by a combination of the strong electric field and the image charge effect. The emitted electrons consist of those with enough energy to surmount the barrier and those tunneling through the barrier. In the case of conventional field emission electrons are originating in the neighborhood of the Fermi level. If electrons are origination below the Fermi level. They would cause the emitter heat-up, because they will be replaced by electrons at the Fermi level. In the case of Fig. 8, a large number of tunneling electrons originate above the Fermi level, taking heat away from the emitter. In fact, these hot tunneling electrons constitute the majority of the emission and energy transport in this case.

Figure 9 shows the electron energy distribution with the same conditions as the previous case except with a larger bias voltage (2.8 V). In this case, electrons originating below the Fermi level are dominant, consequently heating up the emitter instead of cooling it.

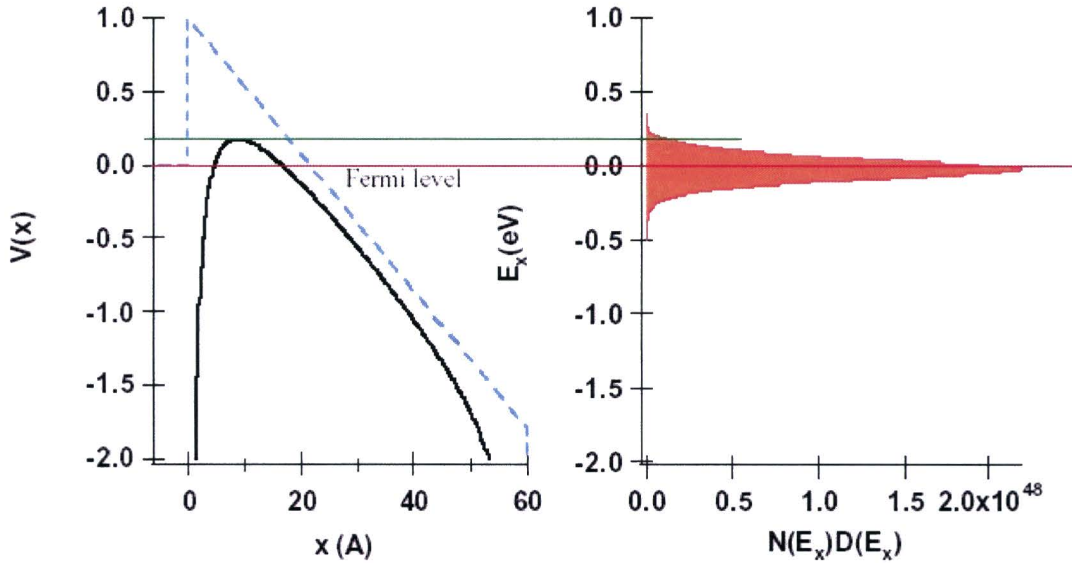


Figure 9. Potential profile and electron energy distribution for a very narrow electrode separation at 300K. The applied bias voltage is 2.8 V, the emitter-collector distance is 60 Å and the work function is 1.0 eV for both electrodes. The dominant emission comes from tunneling below the Fermi level, thus heating the emitter. The dashed line is the potential profile without distortion due to the image charge effect.

There is a range of electric field strength in which electrons originating above the Fermi level are dominant and thereby cool the emitter at room temperature even if the emitter has a work function as high as 1.0 eV. The strength of the electric field is therefore critical, as the emission goes into the heating regime when an excessively strong field is applied.

3.2 Current and cooling power densities

Once the electron energy distribution is obtained, it can be integrated to find the current density across the gap. Integrating the distribution from the barrier maximum to infinity with respect to E_x gives thermionic emission current. Integration below the barrier height gives the tunneling current. Figure 10 shows both types of current as a function of electric field for the case of a narrow electrode gap (100 Å) at room temperature (300K).

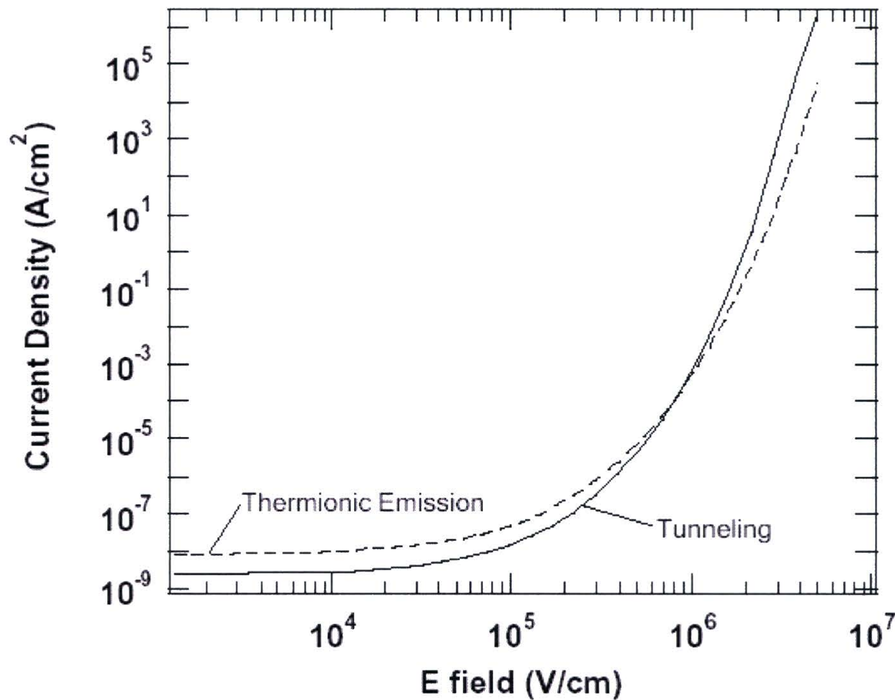
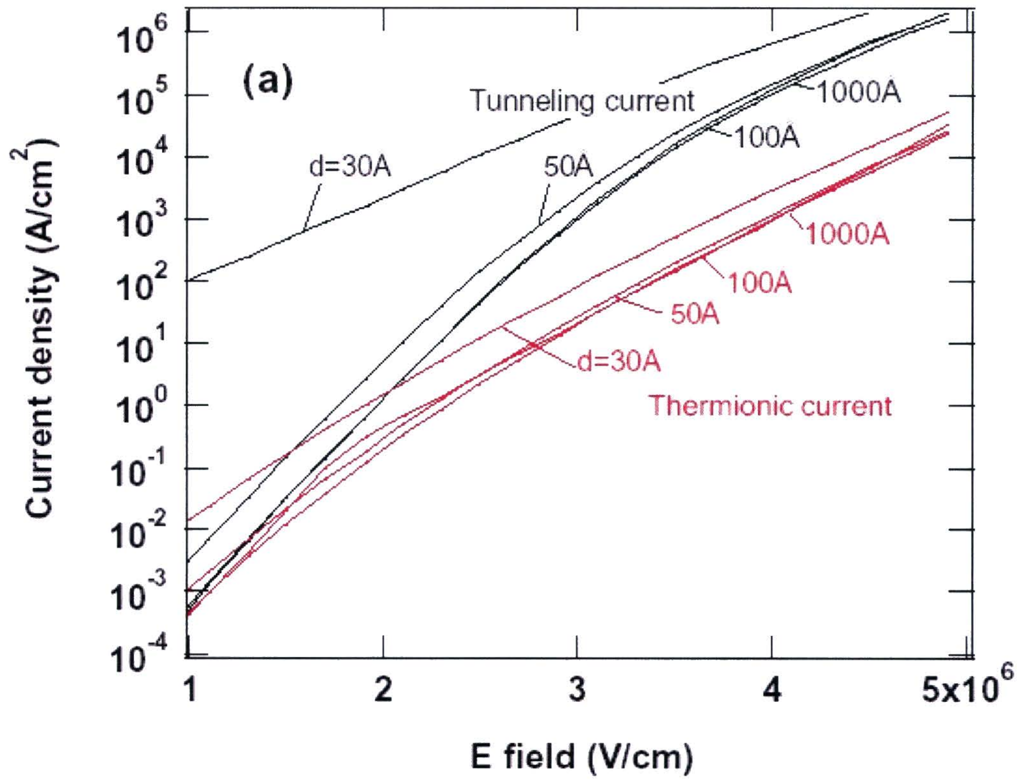


Figure 10. Thermionic and tunneling current density as a function of electric field at 300K. For a work function of Φ = 1.0 eV and the gap between the electrodes is 100 Å.

When the electric field strength is less than 10^5 V/cm, the current is negligible for the purpose of cooling. The tunneling current is smaller than the thermionic current in this range. When the electric field is larger than 10^5 V/cm, both currents start to increase rapidly, and reach a useful level (>1 A/cm^2 [2]) above $\sim 2 \cdot 10^6$ V/cm. In this range of electric field, the tunneling current constitutes the major part of the total current. Therefore, it is necessary to calculate not only the thermionic emission density but also tunneling current density and their energy distributions in order to accurately calculate the thermal flow when the electrode gap is in nanometer range.

As can be seen in Fig. 10, the applied electric field is an important parameter for the current and thus also for the cooling power. Figure 11 shows a) current and b) cooling power densities as a function of the electric field strength for various gaps between emitter and collector with Φ = 1.0 eV and T = 300K. The cooling power is calculated by summing the contributions from thermionic and tunneling emission, as calculated with equations 1.5 and 1.9. For $E > 2 \cdot 10^6$ V/cm, the tunneling current density is one or two orders of magnitude larger than thermionic current density. This situation resembles the normal field emission case. However, as stated previously, tunneling electrons could become a dominant cooling component if they originate above the Fermi level. If the electric field becomes too high ($E > 5 \cdot 10^6$ V/cm), a significant part of the tunneling electrons originates below the Fermi level, which results in heating instead of cooling. This can be seen by the fast decreasing thermal flow density in Fig. 11b.



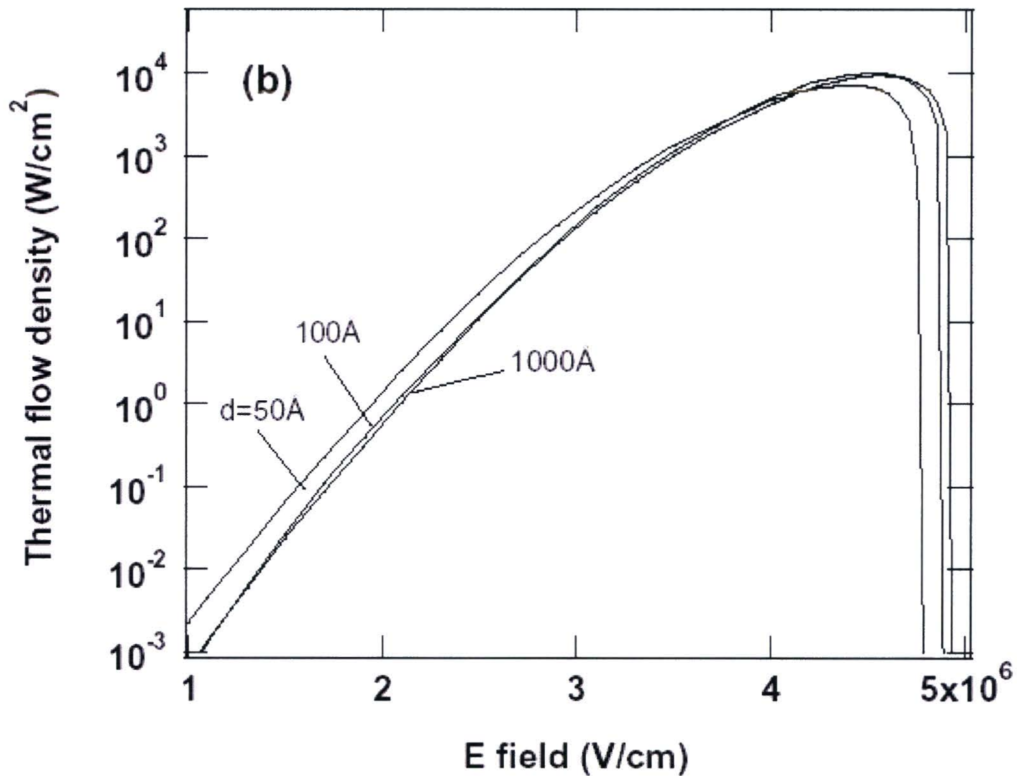


Figure 11. a) Thermionic and tunneling current densities and b) total cooling power densities as a function of electric field for various emitter-collector gaps at 300 K, Φ = 1.0 eV for both electrodes.

Both tunneling and thermionic current densities strongly depend on the electric field and have a weak dependence on the emitter-collector gap above 50 Å. However, below a gap of ~30 Å, a large tunneling current originating around the Fermi level begins to flow, which is detrimental to cooling. Therefore, for the purpose of cooling the emitter-collector gap must be kept above ~40 Å. Cooling power for the case of 30 Å is negative (heating the emitter) throughout this field range, and cannot be shown in this semi-log graph. Maybe the most important thing, which can be seen from Fig. 11b is that a cooling power of almost 10^4 W/cm^2 can be reached at room temperature.

Figure 12 shows current densities and cooling power densities as a function of electric field at different temperatures for the case of emitter-collector gap of 100 Å and Φ = 1.0 eV. Thermionic current has a strong dependence on temperature since the electron population at high energy levels rapidly changes with temperature, whereas the tunneling current has a weaker dependence especially for $E > 2.5 \cdot 10^6$ V/cm.

Cooling power on the order of a few W/cm^2 is expected even at temperatures as low as 200 K. In thermionic cooling, thermal conduction is absent (limited only by radiation), this implies that thermionic/tunneling cooling is capable of sustaining a large temperature difference between the cathode and the collector, because there is vacuum between them.

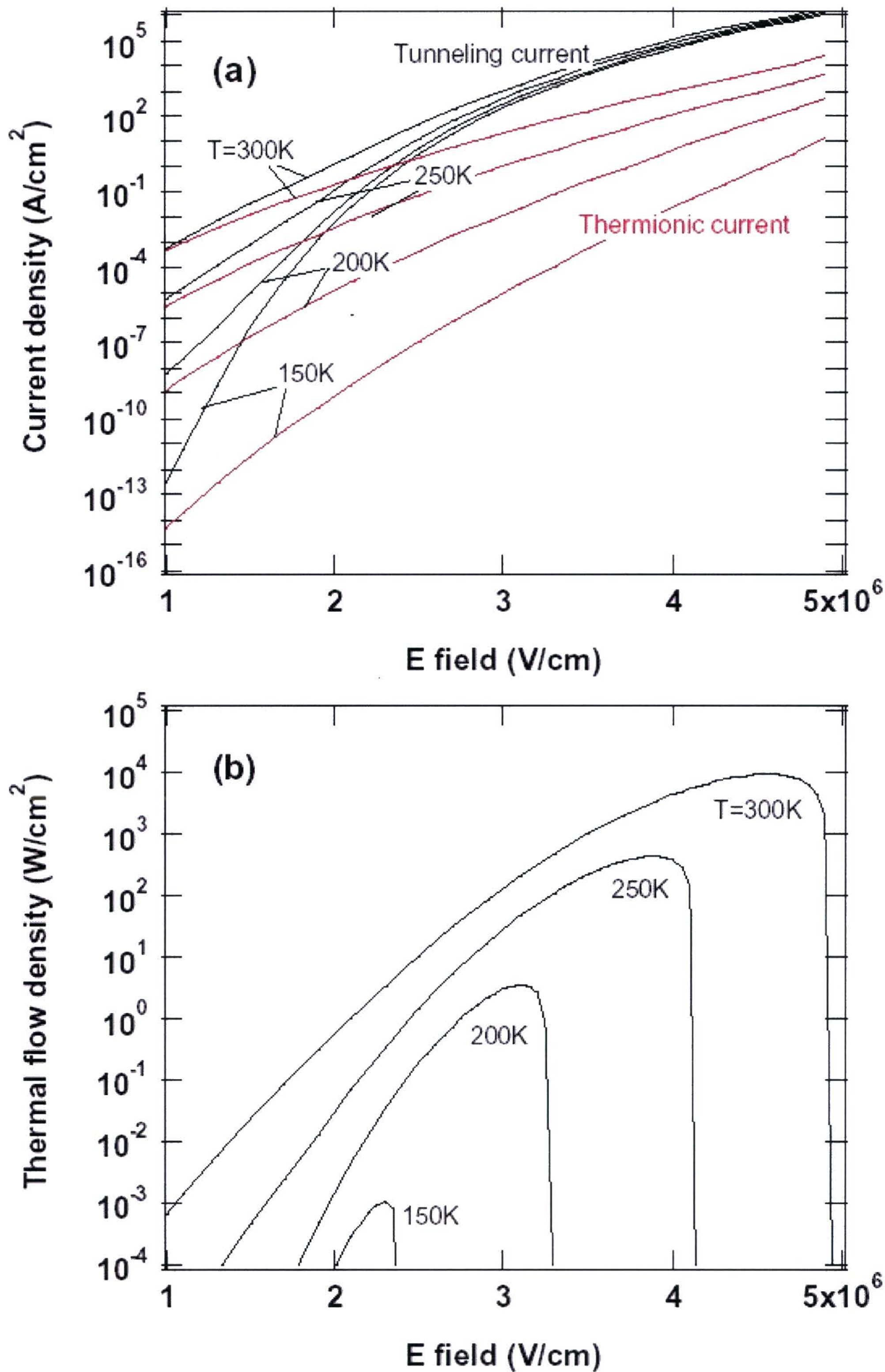


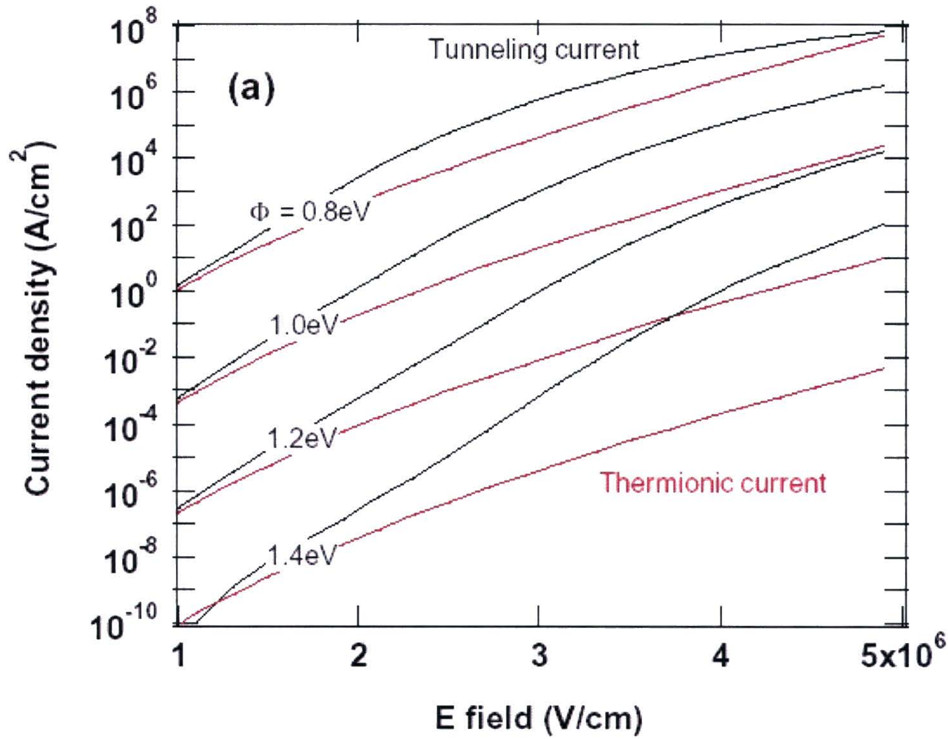
Figure 12. a) Thermionic and tunneling current densities and b) total cooling power densities as a function of electric field for different temperatures. The emitter-collector gap is 100 Å and Φ = 1.0 eV for both electrodes.

Figure 13 shows a) thermionic and tunneling current densities and b) cooling power density as a function of electric field at 300 K with an emitter-collector gap of 100 Å for work functions of 0.8, 1.0, 1.2 and 1.4 eV. Figure 13 shows that for a low work function, a small difference between thermionic and tunneling current densities occurs. Consequently, for emitters with small work functions, emission currents become more thermionic-like and result in more energy carried per electron (larger Peltier coefficient).

As expected, the smaller the work function, the more cooling power is obtained and the smaller the electric field requires to reach the maximum cooling power which improves cooling efficiency. With use of nanometer gap (~6 nm) between emitter and collector, a work function as large as 1.4 eV is expected to produce a cooling power of few tens of W/cm^2 at room temperature.

3.3 Conclusion

In summary, dependences of thermionic and tunneling currents on electric field, emitter-collector vacuum gap, temperature and work function are explored. It is found that for a range of electric field ($1 \sim 5 \cdot 10^6$ V/cm), tunneling current becomes the dominant component of electron emission and provides the major contribution to the thermal flow density. In theory, a combination of a strong electric field ($>10^6$ V/cm) and an image charge potential can significantly lower the work function, which may open a window of possibility for cooling at room temperature by combined thermionic emission and thermo tunneling. It is found from the calculations that an emitter with a work function as large as 1.0 eV is capable of producing a cooling power on the order of 1000 W/cm^2 at room temperature, when an electric field of $3 \sim 4 \cdot 10^6$ V/cm is applied. In addition, refrigeration down to 200 K is possible. However, making such a cooling device is not obvious, this is why the next chapter discusses a practical implementation.



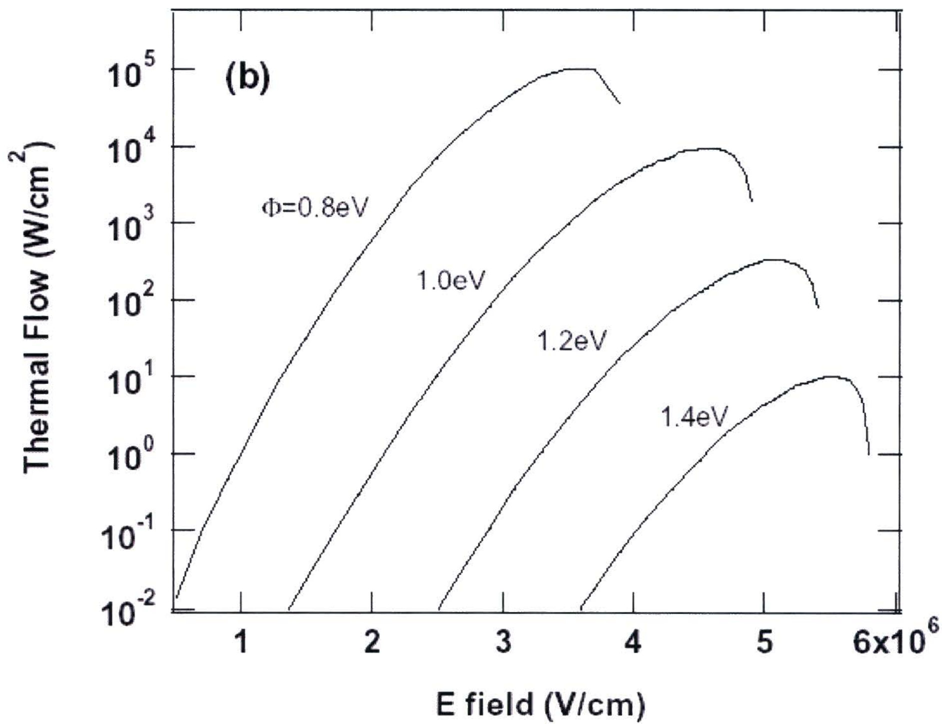


Figure 13. a) Thermionic and tunneling current densities an b) cooling power density as a function of electric field for various work functions at T = 300K.

Chapter 4

Practical implementation: the fabrication of an integrated cooler in silicon

To make an efficient cooling device, based on combined thermionic cooling and thermo tunneling, an emitter and collector separated by several nanometers are needed. The distance between the emitter and collector must be constant within a tolerance of 5 % of the separation [4], over a surface as big as the device that is cooled. The local electric field can become too high if the separation is not constant within the tolerance, which results in heating instead of cooling. This means that the surface roughness may not be more than a few Angstroms. Furthermore, the spacing between the emitter and collector must be vacuum, to prevent a thermal leak over the gap in reverse direction by conduction and convection. An additional complication is that the emitter and collector will bend to each other as a result of the pressure difference between the nanometer gap and the surrounding of the device. To prevent the bending, small spacers between the emitter and collector are necessary. The spacers have to be both a thermal and electrical insulator to prevent heat and current flowing through the spacers. The most efficient way to cool electronics is to integrate the cooling device directly underneath the electric circuit. Silicon is an attractive material for the fabrication of such a cooling device because:

- Electric circuits are most of the time made in silicon.
- Silicon wafers have an extremely flat surface.
- Nanometer lithography is possible on silicon.
- It is possible to grow a layer of several nanometers SiO_2 on top of a wafer to make the spacers. SiO_2 is an electrical and thermal insulator.

Consequently, it is interesting to investigate the possibility to integrate a cooling device in silicon.

The basic technology required for the fabrication of the cooling device is wafer bonding. A cooler can be constructed when two flat silicon wafers with a very thin patterned oxide layer acting as a spacer are wafer-bonded. To lower the work function of the silicon surface half a monolayer of cesium on the surface is required. However, this cannot be deposited prior to vacuum wafer bonding, because of two reasons. For fusion bonding two very clean and hydrophilic surfaces are necessary, so when there is some cesium on the silicon or SiO_2 surface, fusion bonding is hampered. The second reason is that cesium is reactive with oxygen gas in the atmosphere. Consequently it is important that the spacing between the emitter and collector is vacuum before the cesium will be applied on the surface. A suitable technology to apply the Cs might be ion implantation. Cs can be implanted underneath the silicon surface and subsequently to diffuse it to the surface after fusion bonding in vacuum.

The following procedure is proposed to fabricate a device for combined thermionic cooling and thermo tunneling. The most important process steps are shown in Fig. 14. The silicon wafers are heavily doped, to decrease the electrical resistance (lowest resistance: n^{++} 3-6 mΩcm), and are polished to obtain a very flat surface to create a constant emitter-

collector separation. The organic contamination layer on top of the wafer needs to be removed. This is done by cleaning the wafer, for 10 minutes, in concentrated sulphuric acid (H_2SO_4, 96 %) and hydrogen peroxide (H_2O_2, 31 %) mixture at 90 °C (Piranha clean). After the wafer is cleaned a layer of 60 Å SiO_2 is grown by dry oxidation. The wafer is cleaned again with Piranha, to supply the surface with OH-groups. Before the resist is spincoated, the wafer is HMDS (HexaMethylDiSilazane) primered to improve the adhesion between the SiO_2 layer and the resist. On top of this SiO_2 layer a layer of resist (AZ111XF, Micro Chemicals) is spincoated, with a thickness of 1 μm (4000 rpm). After the resist is applied by spin coating, the wafer is put on a hotplate (90 °C, 1 minute) to bake the resist. To pattern the spacers in the resist, the wafer is exposed to ultraviolet light using I-line stepper lithography (Fig. 14 A). Because the ultraviolet light changes the chemical properties of the positive resist, it is possible to remove the resist only on the positions where it was exposed by developing the wafer for 1 minute in developer AZ303 1:4 (Micro Chemicals). Wet etching with buffered HF (20:1, 32.5 nm/min) is used to remove the SiO_2 at the positions where the resist was exposed and developed. Wet etching is proposed since it will not affect the silicon surface (Fig. 14 B). The next step is implanting the cesium underneath the silicon surface. The resist is again used as a mask to prevent the cesium going into the SiO_2 (Fig. 14 C). To be sure the cesium is implanted underneath the silicon surface, an implantation energy of 200 keV is used. After the cesium has been implanted, the resist needs to be removed. This is done by a resist strip in a IPC Barrel (Branson) (60 Minutes of plasma-oxide (800W, 130°C)). Both surfaces have to be clean and hydrophilic before they can be bonded, this is why the wafers first get a Piranha clean. Another heavily doped silicon wafer is bonded on top of the SiO_2 layer using fusion bonding. The bonding is done in vacuum, to be sure the spacing between the emitter and collector is vacuum (Fig. 14 D). After the fusion bonding the two wafers get an anneal at 1000 °C in N_2 to make the binding between the new silicon wafer and the SiO_2 layer stronger and to diffuse the cesium to the surface between the two wafers. The last process step is to grind and polish the upper wafer to a thin layer of silicon. This layer cannot be too thin, because it has to handle a pressure drop of 1 bar.

The critical step in the proposed fabrication procedure is the Cs migration towards the silicon surface after ion implantation and wafer bonding. Some research has been carried out to investigate the feasibility of this concept. To investigate whether if the implanted cesium will diffuse to the surface during annealing, some Rutherford Backscattering Spectrometry (RBS) measurements have been done on silicon wafers implanted with Cs (a 2 MeV He^+ ion beam is used, the detection angle is 77.2° and the sample is channeled). For this purpose, $5 \cdot 10^{15}$ cesium atoms/cm^2 have been implanted with an energy of 200 keV in a silicon wafer. The RBS spectrum direct after implantation is shown in Fig. 15 A. The mean implantation depth of the cesium is 800 Å and the FWHM is 700 Å. The thickness of the amorphous silicon layer formed during ion implantation is 1760 Å. The oxygen signal is a result of a native silicon oxide layer on top of the silicon wafer. The carbon signal is a result of the carbon contamination layer, which is deposited on top of the wafer during the measurement. The dip in the amorphous silicon signal is because of the presence of the cesium at that depth. In order to investigate the Cs migration process towards the surface another part of the implanted wafer is first annealed for one hour at a temperature of 1000 °C before it is measured with RBS. The RBS spectrum of this measurement is shown in Fig. 15 B. The cesium signal is now much smaller ($1.5 \cdot 10^{15}$ cesium atoms/cm^2) and the signal is also shifted to a higher channel. This implies that the

cesium is diffused in the direction of the surface and already 70% of the cesium atoms have reached the surface and have evaporated. The amorphous silicon signal is also much smaller. This is a result of re-crystallization of the silicon atoms during the temperature anneal. The amorphous layer thickness is now 540 Å. Another result of the annealing is the increase of the SiO_2 layer thickness.

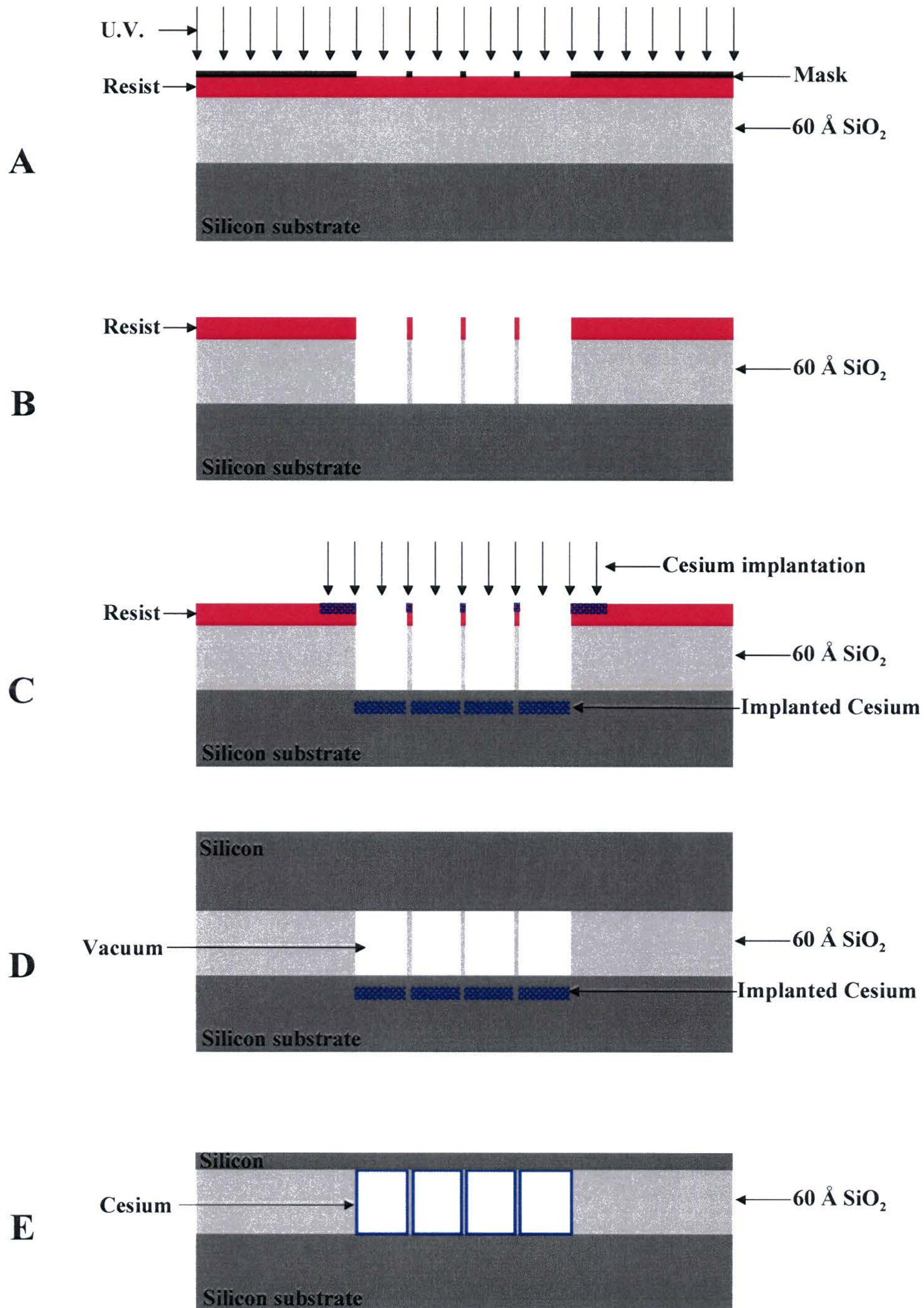


Figure 14. Most important process steps to make an integrated cooling device in silicon, based on thermionic emission and thermo tunneling.

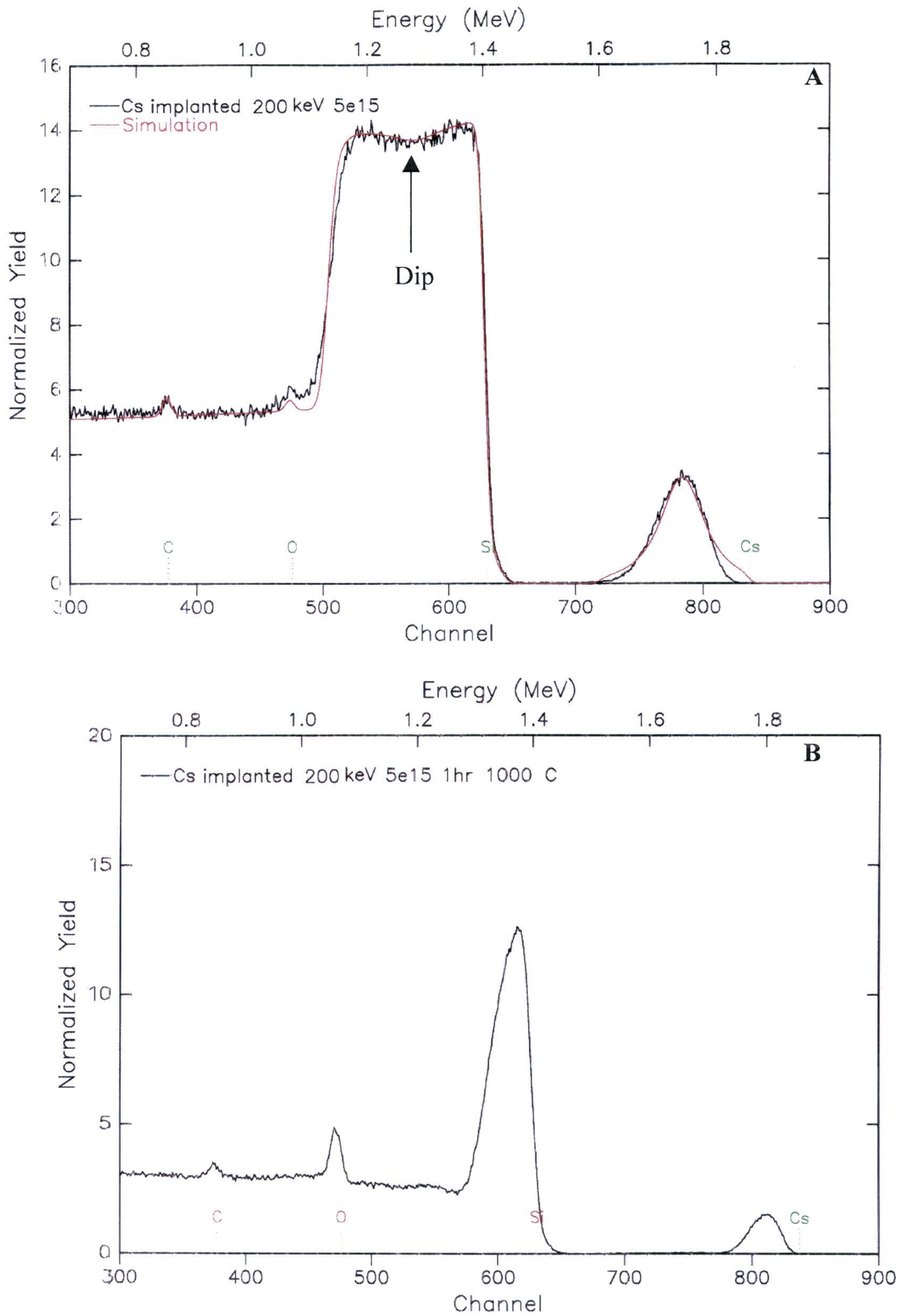


Figure 15. RBS spectra of a silicon wafer implanted with $5 \cdot 10^{15}$ cesium atoms/cm^2 with an energy of 200 keV, before A) and after B) a 1 hour temperature anneal at 1000 °C.

Chapter 5

Discussion

In this section the operation of a practical device based on realistic dimensions and process parameters is discussed. At first we assume that it is possible to lower the work function of silicon from 4.7 eV to 1.0 eV, by covering the surface with half a monolayer of cesium (with oxygen additives) as discussed before. Based on the design rules required for cooling and following the fabrication process described in chapter 4, the spacing between emitter and collector is chosen as d = 60 Å and the bias voltage over the gap V_{Bias} = 1.6 V (Fig. 16)

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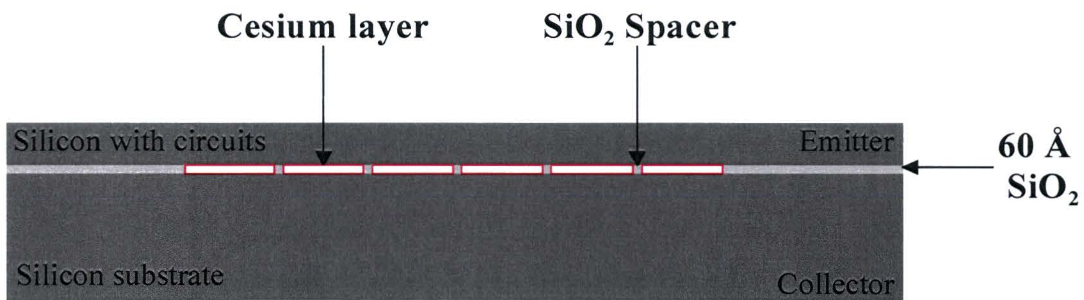

Figure 16. Vacuum gap of 60 Å, made by silicon processing and wafer bonding as discussed before.

Furthermore, it is assumed that the silicon top layer has a thickness of 10 μm, the silicon substrate a thickness of 500 μm and the SiO_2 layer (and also the spacing between emitter and collector) a thickness of 60 Å. The spacers between the emitter and collector are needed to prevent bending of the wafers, because of the vacuum in between. The spacer density can be determined by calculation the deformations due to the applied pressure [5]. There are three deformations due to this pressure:

1. The silicon top layer and substrate bends due to the pressure difference.
2. The spacer height d changes an amount Δd due to the applied pressure.
3. The spacer deforms the silicon top layer and substrate locally (u_0). This deformation will be ignored in the calculation of the spacer density.

The total deformation must be smaller than the tolerance.

The deflection due to bending can be calculated with:

$$\delta = C_\delta p L^4 D^{-1} \quad , \tag{1.10}$$

where C_δ a constant, dependent on the geometry, C_δ =0.00581 in the case of an array of spacers [5], with a distance L between the centers of the spacers (Fig. 17). D is the flexural rigidity of the plate give by:

$$D = \frac{Eh^3}{12(1-\upsilon^2)}, \tag{1.11}$$

where E is Young's modulus (E_{Si} = 170 Gpa and $E_{Siliconoxide}$ = 72 Gpa) and υ the Poisson ratio (υ_{Si} = 0.3 and $\upsilon_{Siliconoxide}$ = 0.2), h is the thickness of the silicon layer.

The change in spacer height (Δd) can be calculated with:

$$\Delta d = \frac{d}{A}\frac{F}{E}, \tag{1.12}$$

where d the spacer height, A the contact area between the silicon and the spacer and F the force acting on an individual spacer.

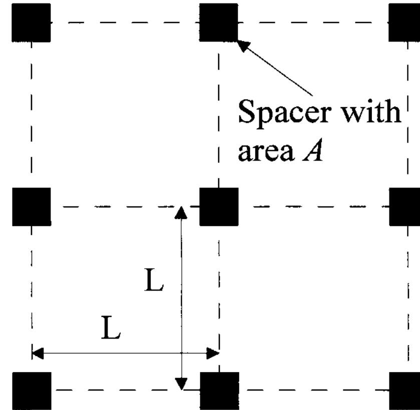

Figure 17: Array of spacers, with contact area A and a distance L between the centers of the spacers.

To estimate the distance between the spacers (L) it will be assumed that deformation due to bending must be smaller than 2 Å. This implies that the distance between the spacers must be smaller than 10 μm (equation 1.10 and 1.11). To estimate the size of the spacers it will be assumed that the change in spacer height (Δd) must be smaller than 1 Å. This results in $A \approx 8$ μm^2 (equation 1.12). The spacer density must be larger than 8 % of the total surface to prevent exceeding the tolerance due to mechanical deformation.

For the calculation of the cooling power using the theory described in chapter 2, we take a spacer density of 8 % of the total surface, and a working temperature of 300 K. The potential barrier for this situation calculated with formula 1.6 is given in Fig. 18, the work function reduction by a combination of the strong electric field and the image charge effect is 0.625 eV.

The applied voltage over the vacuum gap is 1.6 V. In first approximation it is assumed that the resistance of the silicon emitter and collector can be neglected because heavily doped silicon is used. Consequently it is assumed that the voltage over the total device (emitter vacuum and collector) is also 1.6 V by approximation. The thermal cooling power of the device described above can be calculated using the thermionic current (equation 1.4) and the thermo tunneling current (equation 1.8) The sum of the thermionic and tunneling current is $2.25 \bullet 10^2$ A/cm^2 and the cooling power is 35.3 W/cm^2 (equation 1.5 and 1.9). When the resistance of the silicon is assumed to be 3 mΩcm and the total silicon thickness is 510 μm, the voltage drop over the silicon substrate is $V = R \bullet I = 3 \bullet 10^{-3} \bullet 510 \bullet 10^{-4} \bullet 2.25 \bullet 10^2 = 0.03$ V. If we assume that there is also a heat dissipation of 35.3 W/cm^2 in the electric circuit on top of the emitter we obtain stationary situation. As result of the bias voltage and the thermionic and tunneling current, a power of $3.60 \bullet 10^2$ W/cm^2 ($P = I \bullet V$) will be dissipated in the top layer of the silicon substrate, because there is no dissipation in the

vacuum gap. The electrons, which reach the collector, are decelerated in the top layer of the silicon substrate by collisions and will give their energy to the silicon atoms. Consequently, the total heat flux in the silicon substrate is the sum of the cooling power and the joule heating in the top layer of the silicon substrate.

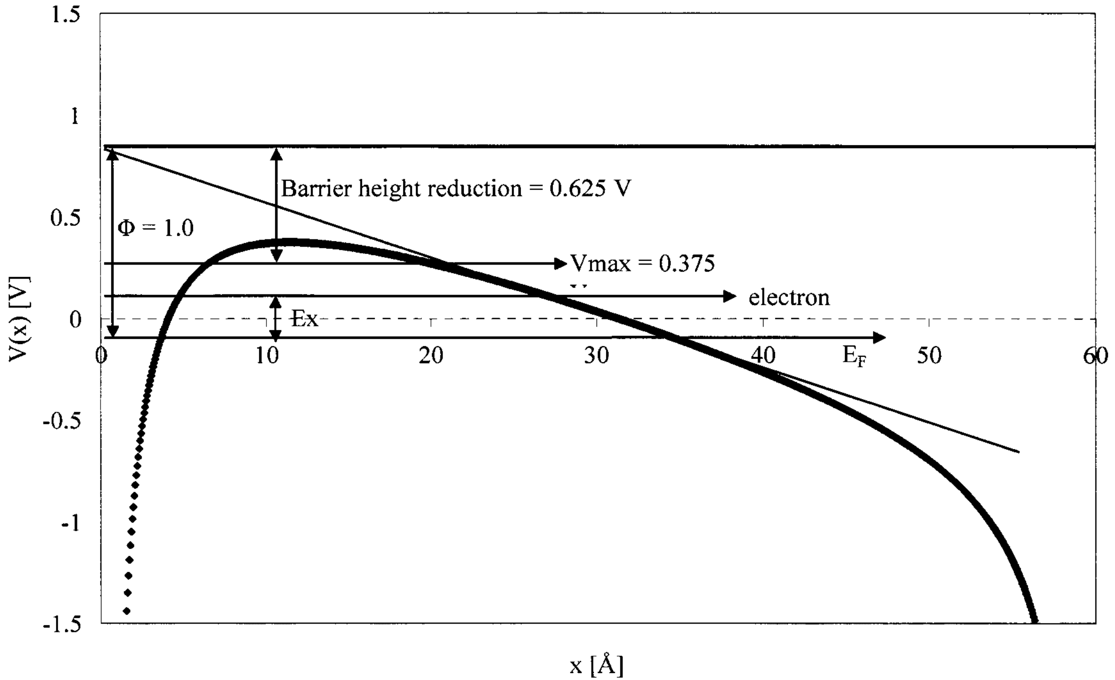

Figure 18. The potential barrier profile V(x) versus x, for Φ = 1.0 eV, emitter-collector separation of 60 Å, V_{Bias} = 1.6 V. The Barrier height reduction is 0.625 eV.

This heat is transported to the bottom of the substrate by conduction. The temperature difference between the top layer and the bottom of the silicon substrate can be calculated with Fourier's law:

$$\vec{q} = -k\vec{\nabla}T\,, \tag{1.13}$$

with q the heat flux, k [$Wm^{-1}K^{-1}$] the thermal conductivity of the material. The top layer of the silicon substrate will reach a temperature of 320 K when the bottom of the substrate is kept at room temperature (300 K). This is no problem, when there is vacuum between the emitter and collector. But because spacers are needed to maintain the gap, a heat leak through the spacers will be present. This heat leak is always in the direction of the emitter, because the principal of the cooling mechanism implies that the temperature of the top layer of the substrate always is higher than the emitter temperature. When the temperature difference over the spacer is 20 K, the spacer thickness is assumed to be 60 Å and the spacer density is 8 % of the total surface, the heat leak through the spacers is $3.77\bullet10^6$ W/cm^2. This implies that the heat flow through the spacers is much higher than the cooling power.

It is possible to decrease this heat leak by decreasing the spacer density. The problem is then that the bending of the silicon and the deformation of the spacers will exceed the tolerance. The heat leak through the spacers is still $4.66 \cdot 10^3$ W/cm^2 when the spacer density is only 0.01 %. A solution is to use thicker oxide spacers located in recesses in the wafer surface as shown in Fig. 19. However, this is quite complicated to make and it is much more difficult to create a gap with a constant distance between emitter and collector. The difference in the expansion coefficient between silicon and SiO_2 makes it more difficult to maintain a constant gap.

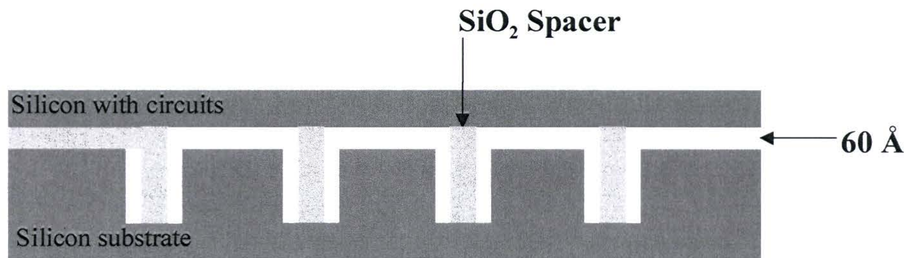

Figure 19. New design for a vacuum gap of 60 Å, now with longer spacers to reduce the heat leak through the spacers.

Chapter 6

Conclusion

In this chapter, the feasibility of the concept for cooling by combined thermionic emission and thermo tunneling to vacuum will be reviewed. In theory, a combination of a strong electric field (>10^6 V/cm) and an image charge potential can significantly lower the work function, which may open a window of possibility for cooling at room temperature by combined thermionic emission and thermo tunneling. The theory described in chapter 2 shows that a material having a work function of 1.0 eV is capable of producing a cooling power in order of 100-1000 W/cm^2 at room temperature. However, making such a cooling device is not obvious and there are some practical problems. The first problem is that the spacing between the emitter and collector must be constant within 5 % of the spacing length. This implies that the roughness of the emitter and collector must be less than a few Angstroms given a required vacuum gap of approximately 60 Å. The surface roughness of most materials is already much larger. However, silicon has one of the flattest surfaces (in the order of some Angstrom), which maybe provides the opportunity to integrate cooling devices in silicon, closely situated to the heat producing electrical circuits. But even if the roughness of silicon is small enough, the constant spacing is still a problem. This is because the spacing between emitter and collector must be vacuum. This results in a pressure drop over the silicon and the result of this pressure drop is bending of the silicon. To prevent this bending, spacers between emitter and collector are needed. These spacers must be electrical and thermal insulators to prevent the electrons going through the spacers instead of going through the vacuum and to prevent a heat leak back to the emitter. Fortunately, SiO_2 is a good electrical and thermal insulator. Its compatibility with IC technology allows to grow a layer of several nanometers SiO_2 on top of a silicon wafer and to make the spacers really small. A spacer density of 8 % of the total surface is needed to prevent the deformations exceeding the tolerance. This density results in a heat leak much larger than the cooling power. Because of this heat leak, the cooling device cannot work at room temperature.

Another topic that has to be addressed is the lowering of the work function. The work function of the silicon surface needs to be decreased to a value around 1 eV. In principle, this can be achieved by covering the surface with cesium as discussed in chapter 2. A number of potential problems have to be investigated: the resulting roughness of the surface, possibly the diffusion of cesium into the SiO_2, or the formation of a conductive layer of cesium on the spacer sidewalls. Because of all these practical problems, a cooling device based on thermo tunneling and thermionic emission is not possible within the present experimental tolerances.

Chapter 7

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PART II

Forced convection through micro-channels

Chapter 1

Introduction

One of the most commonly applied cooling principles is forced convection. In the second part of this thesis, integrated cooling of electronic circuits by a single-phase flow through rectangular micro-channels machined in the backside of a silicon wafer will be discussed.

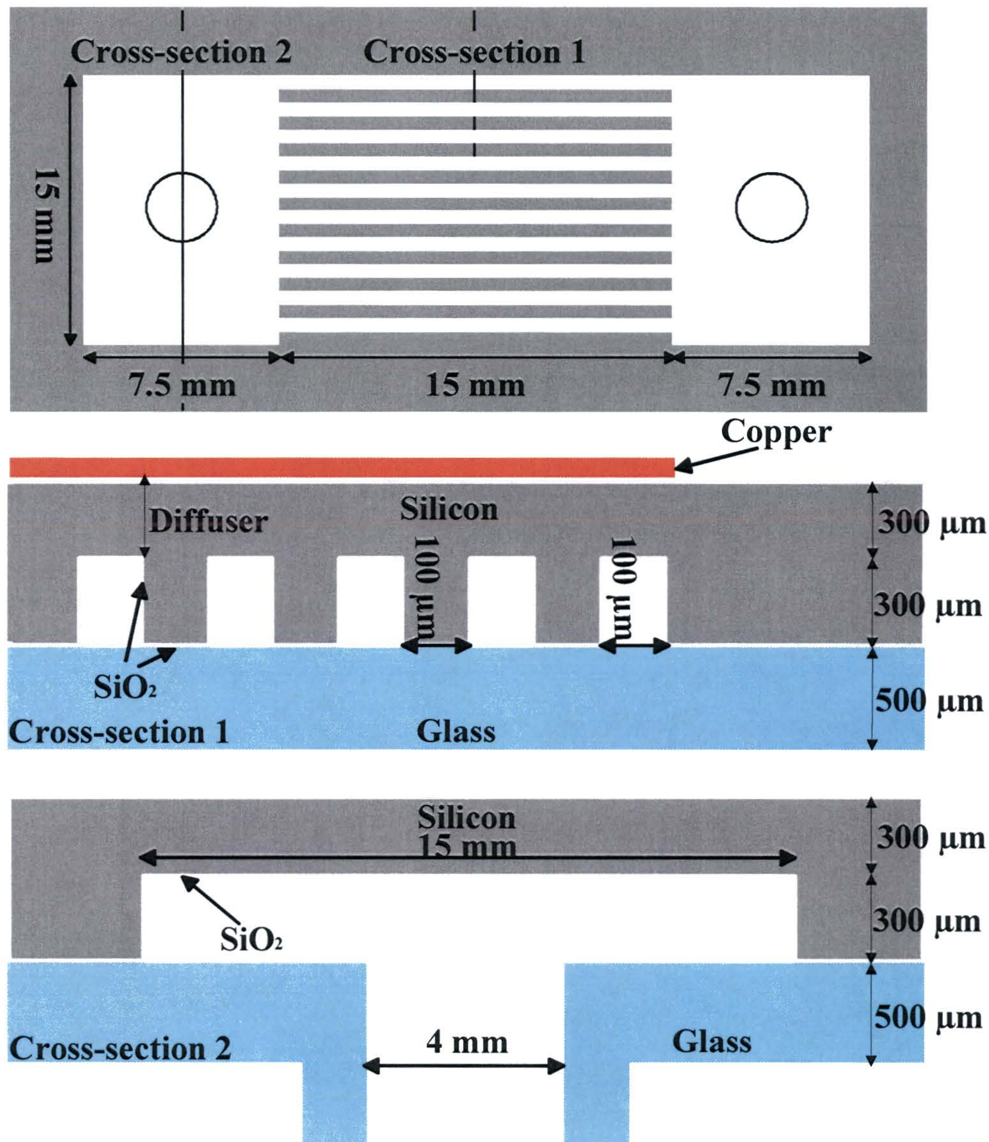


Figure 1. The geometry of the micro-channels in the backside of a silicon wafer. The final device has a total number of 75 channels.

By integration into the silicon wafer, space can be saved and intermediate layers between the integrated circuit (IC) and the micro-channels, which may act as thermal barriers, are eliminated.

The geometry of the fabricated and used micro-channels is shown in Fig 1. Water is selected, as working fluid, because of its good thermal and hydraulic properties. Especially the high heat capacity and relative low viscosity, makes water a suitable cooling medium.

First of all, the theory about active cooling with use of an active flow through micro-channels will be reviewed. With use of this theory the proposed micro-channels are analysed by solving (numerically) the heat transfer problem consisting of a simultaneous determination of the temperature field both in the solid substrate and in the flowing liquid. After the theory is reviewed, the fabrication of integrated micro-channels in silicon will be discussed, together with the sealing steps. Subsequently an experimental setup will be described which was build to measure the cooling capacity of a micro-channel cooling device. The results of the measurements will be discussed and compared with the calculations, followed by a general evaluation and the conclusions.

Chapter 2

Theory

2.1 Heat transfer basics

Heat transfer is energy in transit due to a temperature difference. Whenever a temperature difference exists in a medium or between media, heat transfer will occur. Different modes for heat transfer processes exist. The term conduction is used when a temperature gradient exists in a stationary medium. In this situation, the heat transfer will occur across the medium by atomic or molecular collisions or by collective vibrations such as phonons. The term convection refers to heat transfer in a moving fluid or gas by the collective movement of molecules or diffusion. The third mode of heat transfer is by emission of electromagnetic waves, called radiation. All surfaces of finite temperature emit electromagnetic waves, with an energy depending a.o. on the surface temperature. Hence, in the absence of an intervening medium, there is still heat transfer by radiation between two surfaces at different temperatures.

In order to characterize heat transfer between two objects/places A and B in contact, thermal resistance is introduced as an analogy with electric resistance. It links the temperature difference between A and B with the heat flux P [W]. The thermal resistance [KW^{-1}] can be expressed as:

$$R_{th} = \frac{T_A - T_B}{P}, \tag{2.1}$$

where $T_A > T_B$.

2.1.1 Conduction

Conduction can be seen as the transfer of energy from the more energetic to the less energetic particles of a material due to interactions between the particles. The heat flux vector $\vec{q}$ [Wm^{-2}] is the heat transfer rate per unit area perpendicular to the direction of heat transfer, and is proportional to the temperature gradient:

$$\vec{q} = -k\vec{\nabla}T, \tag{2.2}$$

with k [$Wm^{-1}K^{-1}$] the thermal conductivity of the material. This equation is known as Fourier's law. The minus sign is a consequence of the fact that heat is transferred in the direction of decreasing temperature. The power flux P [W] is defined as:

$$P = \frac{dQ}{dt} = \iint_S \vec{q}.\vec{n}.dS, \tag{2.3}$$

dQ [J] represents the elementary quantity of energy handed over by an arbitrary surface S characterized by the local vector $\vec{n}$ perpendicular to the elementary surface dS.

2.1.2 Convection

The convection heat transfer mode is comprised of two mechanisms. In addition to energy transfer due to diffusion, there is also energy being transferred by the bulk, or macroscopic, motion of the fluid (or gas). The fluid motion is associated with the fact that, at any instant, large numbers of molecules are moving collectively. Such motion, in the presence of a temperature gradient, will give rise to heat transfer. The molecules retain also their random motion, which leads to diffusion in presence of a temperature gradient. The total heat transfer is the superposition of energy transport by the random motion of the molecules and by the bulk motion of the fluid. It is customary to use the term convection when refereeing to this cumulative transport and the term advection when referring to transport due to bulk motion only.

For micro-channel cooling, heat transfer due to convection between a fluid in motion and a boundary surface has to be considered. A consequence of fluid flow is the development of a region in the fluid through which the velocity varies from zero to a finite value u_∞, associated with the bulk flow. This region is known as the hydrodynamic boundary layer. Moreover, if the surface and fluid differ in temperature, there will be also a region of the fluid through which temperature varies from T_S, the temperature of the surface, to T_∞ in the outer flow. This region, called the thermal boundary layer, may be smaller, larger or the same size as the hydrodynamic boundary layer. If $T_S > T_\infty$, convection heat transfer will occur between the surface and the outer flow. The diffusion dominates near the surface, where the fluid velocity is low. In fact, at the interface between the fluid and the surface, the fluid velocity is zero and heat is transferred only by this mechanism. The contribution due to bulk fluid motion originates from the fact that the thermal boundary layer grows as the flow progresses. In effect, the heat that is transported into this layer is swept downstream and is eventually transferred to the fluid outside the boundary layer.

Convection flow can be classified according to the nature of the flow. It is called forced convection when the flow is caused by an external force. In contrast, for free (or natural) convection, the flow is induced by forces, which arise from density differences caused by temperature variations in the fluid. The heat flux due to convection [Wm^{-2}], regardless of the particular nature of the convection, is given by:

$$q = h.(T_s - T_\infty), \tag{2.4}$$

where h [$Wm^{-2}K^{-1}$] the convection heat transfer coefficient. It encompasses all the parameters that influence convection heat transfer. In particular, it depends on conditions in the boundary layer, which are influenced by surface geometry, the nature of the fluid motion and an assortment of fluid thermodynamic and transport properties. Equation 2.4 is known as Newton's law of cooling.

2.1.3 Radiation

Unlike conduction and convection, which requires a medium, radiation is an electromagnetic phenomenon and travels easily through vacuum with the speed of light. All surfaces emit thermal radiation and absorb or reflect incident radiation. The net rate of heat flux from a surface equals the total energy emitted minus the total energy absorbed from the surroundings. A "black" surface (emission at a maximal rate and, correspondingly, absorption of all incident radiation) emits energy at a rate proportional to the fourth power of the absolute temperature of the surface. If a black surface has area A and temperature T, its radiant emission is given by:

$$E_b = \sigma A T^4, \tag{2.5}$$

where σ [$Wm^{-2}K^{-4}$] the Stephan-Boltzmann constant. Real surfaces are non-black and emit radiation at a rate less than maximum. A convenient way to express this is to say that they emit at a fraction ε of the black body rate:

$$E = \varepsilon \sigma A T^4. \tag{2.6}$$

The dimensionless parameter ε is called the emissivity of the surface and varies between zero and unity. Experiments show that ε varies with the temperature and also with surface parameters, texture, colour, degree of oxidation and the presence of coatings. The analysis of radiant interchange between two or more surfaces can be a complex algebraic procedure. A common special case is when body 1 has a temperature T_1 and constant emissivity ε_1, and is completely enclosed by a large surface area, $A_2 >> A_1$, with temperature T_2 and constant emissivity ε_2. The net radiant heat transfer from the small body to the large enclosure is:

$$q_{1\to 2} = \varepsilon_1 \sigma A_1 (T_1^4 - T_2^4), \tag{2.7}$$

which is independent of the size and the emissivity of the enclosure.

2.2 Thermal and fluidic laws for single phase forced convection through micro-channels

2.2.1 Thermal resistances

The maximum temperature allowed in an IC is around 120 °C. Because of this maximum temperature, the heat transfer by radiation to the surrounding can be neglected. This means that the heat generated in the IC is most efficiently transported by conduction and convection. For a micro-channel cooler, in the backside of a silicon wafer, the thermal resistance can be seen as the sum of three terms:

1. The thermal resistance due to conduction through the diffuser, R_{cond}. The diffuser contains silicon and a thin layer of silicon oxide (Fig. 1).
2. The convection resistance, which represents the heat exchange between the micro-channel walls and the fluid, R_{conv}.
3. The capacitive resistance, which represents the increase of the fluid temperature between the channel inlet and outlet, R_{cap}.

2.2.1.1 Conduction thermal resistance, R_{cond}

Two cases have to be distinguished about diffusion resistance:

1. *The heat flux is unidirectional.* The heat flux is only unidirectional when the heat dissipation in the IC is uniform, and the IC has the same size as the micro-cooler. In the simple case of a single layer diffuser, the conduction resistance can be expressed as:

$$R_{cond} = \frac{d}{kA}, \tag{2.8}$$

where d the diffuser layer thickness, k the thermal conductivity and A the diffuser area through which the heat flux goes. It is easy to minimize the importance of this resistance by decreasing the diffuser thickness, only limited by the mechanical constraints of our system. When the diffuser contains several layers, the thermal resistance can be calculated with:

$$R_{cond} = \sum_{i=1}^{n} R_{cond,i} = \sum_{i=1}^{n} \frac{d_i}{k_i A}. \tag{2.9}$$

2. *The heat flux is 2-Dimendional.* This case appears when the IC is smaller than the cooler or when the heat dissipation in the IC is not uniform, and is amplified when the diffuser contains a thermal barrier. In the micro-channel design shown in Fig. 1 the silicon is covered with a thin layer of SiO_2 (100 nm), to make the surface hydrophilic and the prevent the copper diffusing into the silicon. SiO_2 is an insulator, but because this layer is only 100 nm, it is not a big thermal barrier. When the heat dissipation in the IC is not uniform, the presence of the SiO_2 even decreases the maximum temperature. This is because heat is spread in SiO_2 layer, and the heat flows through a larger area than in the one-dimensional case. This is why it is important to make the diffuser layer not to thin when the heat flux is not uniform. By using an optimal diffuser layer hot spots can be prevented.

2.2.1.2 Convection thermal resistance, R_{conv}

Convection represents heat exchange between the channel walls and the fluid. Convection thermal resistance can be expressed as:

$$R_{conv} = \frac{1}{hA_{\mu-ch}}, \tag{2.10}$$

where h [$Wm^{-2}K^{-1}$] the heat transfer coefficient for convection and $A_{\mu-ch}$ the surface of the micro-channels. The heat transfer coefficient for convection depends on numerous parameters such as convection mode (forced or free), cooler geometry, flow characteristics (laminar or turbulent), thermal and hydraulic transient properties etc.

2.2.1.3 Capacitive thermal resistance, R_{cap}

Contrary to the former thermal resistances, which care about temperature differences parallel to the heat flux, this resistance describes the fluid temperature increase between the channel inlet and outlet perpendicular to the heat flux. This

temperature rise is due to the heat quantity absorbed by the fluid while it is flowing through the micro-channels. The capacitive thermal resistance can be calculated with:

$$R_{cap} = \frac{1}{\rho \dot{V} C_p}, \tag{2.11}$$

where ρ [kg m^{-3}] the density of the fluid, $\dot{V}$ [m^{3}s^{-1}] the volumetric flow rate and C_p [J kg^{-1}K^{-1}] the specific heat.

2.2.1.4 Overall thermal resistance, R_{th}

By applying equation 2.1 to micro-channel cooling, the overall thermal resistance can be calculated with:

$$R_{th} = \frac{T_j - T_{in}}{P}, \tag{2.12}$$

where T_j the junction temperature in the IC, T_{in} the fluid inlet temperature and P the dissipated power. Because the micro-channels are made in the backside of a silicon wafer, there is no intermediate layer between the IC and the micro-channels. When the micro-channels are not fabricated in the silicon, there is an extra thermal resistance due to the presence of the intermediate layer.

2.2.2 Convective exchange laws from a thermal and hydraulic point of view

In this part, the flow through the micro-channels will be characterized with use of four dimensionless numbers:

1. The Reynolds number
2. The Prandtl number
3. The Friction coefficient
4. The Nusselt number

2.2.2.1 Reynolds number

The Reynolds number describes the relation between the convective forces and the friction forces in the fluid and is given by:

$$\mathrm{Re} = \frac{\rho v D_h}{\mu}, \tag{2.13}$$

with v the speed of the fluid, μ [Pa s] the dynamic viscosity and D_h the hydraulic diameter of the micro-channel. The hydraulic diameter can be calculated with:

$$D_h = \frac{4s}{p}, \tag{2.14}$$

with s and p respectively the area and the perimeter of the channel.

The Reynolds number defines the transition between laminar and turbulent flows. The transition value is well known for channels and mini-channels ($D_h > 1$ mm), the flow is laminar for $Re < 2300$ and becomes turbulent for Reynolds numbers above this value. However, in the case of micro-channels, the Reynolds number for the transition is not well known. Wang and Peng [1] studied the forced convection of liquid in micro-channels ($D_h \sim 0.3$ mm) experimentally and found that fully developed turbulent convection was initiated at $Re = 1000\text{-}1500$ and the conversion from laminar to turbulent occurred at approximately $Re = 300\text{-}800$.

2.2.2.2 Prandtl number

Flow can be fully developed either thermally and hydraulically. A flow is fully developed thermally (or hydraulically), when the fluid temperature (or velocity) profile, in a channel, no longer depends on its position along the channel. The Prandtl number, *Pr*, gives information about the thermal and hydraulic development of the flow. This dimensionless number only depends on fluid properties and not on the channel geometry.

$$\Pr = \frac{\mu C_p}{k}. \tag{2.15}$$

This number represents the relative importance between the thermal and viscous effects. For instance, consider a fluid element with a characteristic size of l, then the viscous diffusion time τ_υ and the thermal diffusion time τ_κ can be expressed as:

$$\tau_\upsilon = \frac{l^2}{\upsilon}, \tag{2.16}$$

$$\tau_\kappa = \frac{l^2}{\kappa}, \tag{2.17}$$

where υ [m^{2}s^{-1}] the fluid kinematic viscosity and κ [m^{2}s^{-1}] the thermal diffusivity of the fluid. Now follows for the Prandtl number:

$$\Pr = \frac{\mu C_p}{k} = \frac{\rho C_p \upsilon}{\rho C_p \kappa} = \frac{\upsilon}{\kappa} = \frac{\tau_\kappa}{\tau_\upsilon}. \tag{2.18}$$

So, for fluids with a high Prandtl number ($\Pr \gg 1$), the time to reach thermal equilibrium is longer than the time to reach viscous flow equilibrium, consequently heat diffusion processes initially determine the fluid motion. On the contrary, for low Prandtl numbers ($\Pr \ll 1$), thermal effects decrease and hydrodynamic laws lead the fluid motion. The Prandtl number for water is around 7. This implies that the viscous diffusion time and thermal diffusion time have the same order of magnitude.

2.2.2.3 Friction coefficient and pressure losses

Pressure losses between channels input and output can be calculated with:

$$\Delta P = \frac{4\rho C_f L v^2}{2D_h}, \tag{2.19}$$

where C_f the friction coefficient, v the speed in the channel and L the channel length.

2.2.2.4 Nusselt number

The Nusselt number describes the heat transfer between the solid and the fluid and is given by:

$$Nu = \frac{hD_h}{k}. \quad (2.20)$$

For a laminar flow, which is fully developed, both thermally and hydraulically, it is possible to calculate the Nusselt number analytically, if the velocity profile is known and when it is known how to solve the heat equation.

2.3 Analytical model

To compare the results of our experiments with theory, the thermal resistance of the micro-channels is calculated by solving numerically a conjugate heat transfer problem consisting of the simultaneous determination of the temperature fields, in both the substrate and the liquid [2]. For the purpose of this calculation, it is assumed that all the channels have a uniform, rectangular cross-section of width $2W_c$, height H_c, hydraulic diameter D_h and length L. The distance between the centers of adjacent channels is $2W$ and the thickness of the wafer is H (Fig. 2)

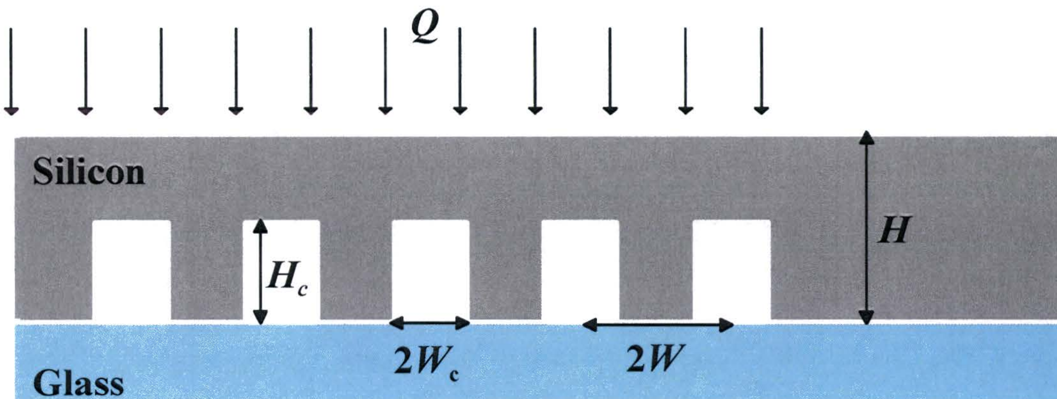


Figure 2. A cross section of the heat exchanger with the dimensions used in the analysis.

Since the cover plate is made out of glass, which thermal conductivity is about two orders of magnitude lower than that of silicon ($k_{glass} \approx 1$, $k_{silicon} \approx 100$), it is assumed that this boundary is thermally insulated. This is a conservative assumption, which will lead to a slight overestimation of the overall thermal resistance. A more precise analysis would require information about the thermal interaction between the glass plate and its environment. The exact nature of this interaction depends on the packaging of the electronic circuits and is not likely to be generic. Further, it is assumed that the channels surfaces are smooth, and that the heat flux Q is uniform. The thermal conductivities of the solid and the fluid are k_s and k_f, respectively.

Taking advantage of symmetry, the computations are based on a unit cell consisting of half a channel and the surrounding silicon. Figure 3 depicts the computational domain, the governing equations, and the boundary conditions. The channels height, H_c, is used as a unit of length and the average fluid velocity, $\bar{U}$, is taken as the unit for the velocity. The convention is adopted that uppercase and lowercase represent, dimensional and non-dimensional quantities, respectively. For this model, the flow is assumed laminar and fully developed (both thermally and hydraulically). In situations in which entrance effects may be important, this model would overestimate the thermal resistance.

2.3.1 Fluid velocity profile

The dimensional average velocity, $\bar{U}$, and the non-dimensional velocity field, $u(x,y)$ are obtained from the classical expressions for fully developed, laminar flow in a rectangular duct with aspect ratio $A = H_c/2W_c = 1/w_c > 1$ [2]:

$$\overline{U} = \frac{H_c^2}{12\mu}\left(-\frac{dP}{dZ}\right)\left[1-\frac{192A}{\pi^5}\sum_{i=1,3,5...}^{\infty}\frac{\tanh\left(\frac{i\pi}{2A}\right)}{i^5}\right], \tag{2.21}$$

and

$$u(x,y) = \frac{\frac{48}{\pi^3}\sum_{i=1,3,5,...}^{\infty}(-1)^{\frac{i-1}{2}}\left[1-\frac{\cosh(i\pi x)}{\cosh(i\pi w_c)}\right]\frac{\cos(i\pi(y-0.5))}{i^3}}{1-\frac{96}{\pi^5 w_c}\sum_{i=1,3,5...}^{\infty}\frac{\tanh(i\pi w_c)}{i^5}}. \tag{2.22}$$

In the above, P is the pressure, μ the dynamic viscosity, and (x,y,z) are Cartesian coordinates. The coordinates (x,y) are depicted in Fig. 3. The coordinate z is aligned in the streamwise direction.

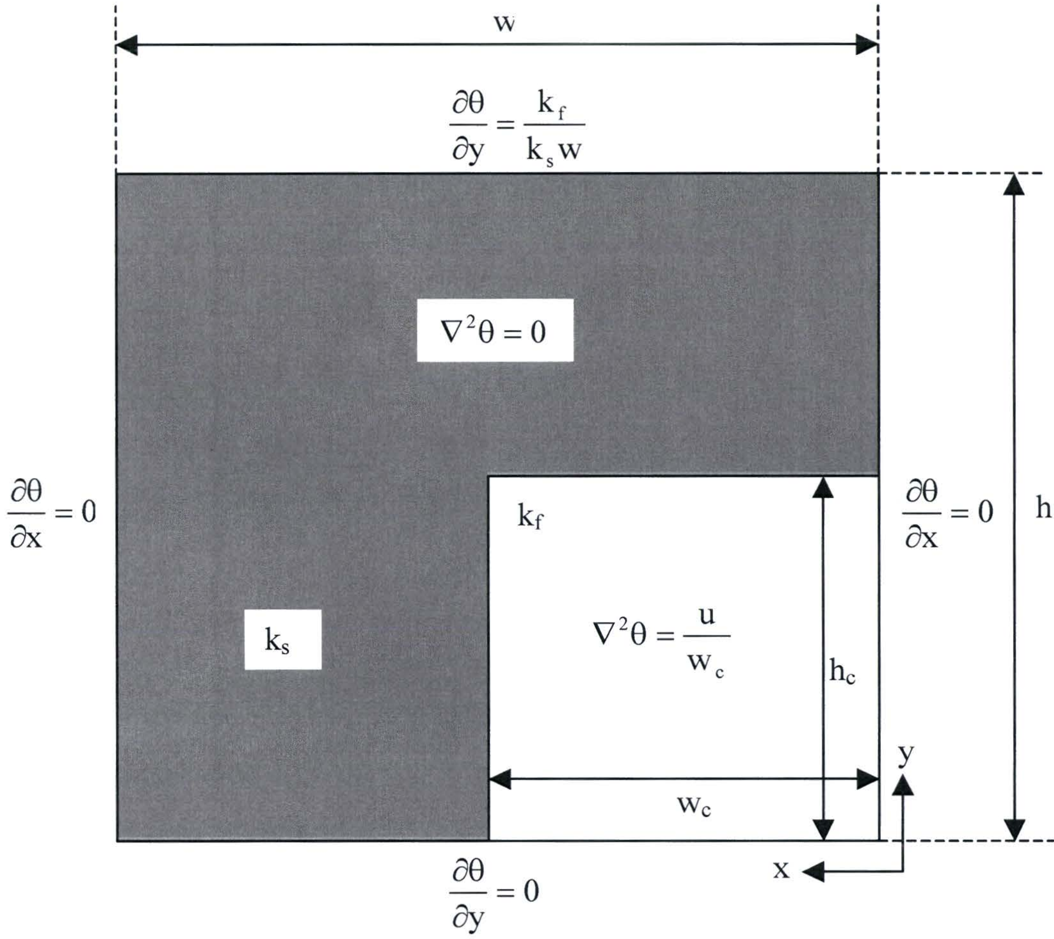


Figure 3. A computational cell obtained utilizing symmetry is shown together with the governing equations and boundary conditions. θ is the non-dimensional temperature, which will be defined further on.

2.3.2 Temperature field

Since the flow is assumed to be thermally developed, the shape of the temperature profile does not change along the channel length. However, the bulk fluid temperature will increase along the channel length because of the heat flux. The fluid bulk temperature, $T_B(z)$, can be expressed as:

$$\frac{dT_B}{dZ} = \frac{Q}{\rho_f C_p \overline{U}} \frac{W}{W_c H_c}, \tag{2.23}$$

where ρ_f and C_p are the fluid density and specific heat respectively and Q the uniform heat flux applied on the wafer top..

Because the thermal resistance between the solid and the liquid is small, it can be assumed that the axial temperature gradient in both is the same. So a non-dimensional temperature θ can be defined as:

$$\theta(x,y) = \frac{k_f}{WQ}\left[T(x,y,z) - T_B(z)\right], \tag{2.24}$$

where $T(x,y,z)$ is the dimensional temperature. The temperature field satisfies the following equations:

- In the fluid

$$\frac{\partial^2\theta^*}{\partial x^2} + \frac{\partial^2\theta^*}{\partial y^2} = \frac{u(x,y)}{w_c}, \tag{2.25}$$

- In the solid

$$\frac{\partial^2\theta^*}{\partial x^2} + \frac{\partial^2\theta^*}{\partial y^2} = 0, \tag{2.26}$$

with the boundary conditions as depicted in Fig. 3. The temperature and flux continuity across the solid-liquid interfaces are:

$$\frac{k_s}{k_f}\left(\frac{\partial\theta^*}{\partial\hat{n}}\right)_{solid} = -\left(\frac{\partial\theta^*}{\partial\hat{n}}\right)_{liquid}, \tag{2.27}$$

where $\hat{n}$ the specified mediums outwardly directed normal vector at the solid liquid interface. The new variable, θ^*, used in equation 2.25, is different from θ. This variable θ^* is introduced because equation 2.25 and the corresponding boundary conditions yield a temperature distribution which is invariant to the addition of a constant. So, uniqueness is achieved by selecting $\theta_B = 0$. Accordingly:

$$\theta(x,y) = \theta^*(x,y) - \theta_c, \tag{2.28}$$

where

$$\theta_c = \frac{1}{w_c}\int_0^{w_c} dx \int_0^1 dy\ u(x,y)\theta^*(x,y). \tag{2.29}$$

Once the temperature profile $\theta(x,y)$ is known, all the relevant heat transfer quantities may be computed. The local Nusselt number (Nu_L) is given by the formula:

$$Nu_L = \frac{H_c}{T_{sf} - T_B}\left(\frac{\partial T}{\partial\hat{n}}\right)_{sf} = \left(\frac{1}{\theta}\frac{\partial\theta}{\partial\hat{n}}\right)_{sf}, \tag{2.30}$$

where the subscript (sf) denotes the solid fluid interface. For design purpose, one is typically interested in the overall thermal resistance,

$$R_{ov} = \frac{\overline{T(h,L)} - T_B(0)}{QW_T L}, \tag{2.31}$$

expressed in units of [KW^{-1}] and based on the temperature difference between the wafer's surface opposite to the exit of the micro channels and the inlet bulk temperature. W_T is the chip width. One may prefer to define the thermal resistance based on the maximal surface temperature rather than the average one. Due to the high thermal conductivity of the silicon, the difference between the two resistance definitions is likely to be small, especially for uniform heat fluxes.

2.3.3 Solution procedure

The differential equations 2.25 and 2.26 are Poisson equations, and they can be solved numerically by using the finite differences method. The first step for solving the Poisson equations numerically is defining a computation grid in the xy-plane. The simplest way of building this grid is to take a regular and uniform grid with a step Δ:

$$\begin{cases} x_i = x_0 + i\Delta \ , \ 0 \le i \le I \\ y_j = y_0 + j\Delta \ , \ 0 \le j \le J \end{cases}, \tag{2.32}$$

with

$$\begin{cases} I = \dfrac{w_c}{\Delta} \\ J = \dfrac{h_c}{\Delta} \end{cases}. \tag{2.33}$$

Using a Taylor development of the second order, the second derivative of the Poisson equation becomes:

$$\begin{cases} \dfrac{\partial^2 \theta^*}{\partial x^2} \approx \dfrac{\theta^*(x+\Delta, y) + \theta^*(x-\Delta, y) - 2\theta^*(x,y)}{\Delta^2} \\ \dfrac{\partial^2 \theta^*}{\partial y^2} \approx \dfrac{\theta^*(x, y+\Delta) + \theta^*(x, y-\Delta) - 2\theta^*(x,y)}{\Delta^2} \end{cases}. \tag{2.34}$$

Adopting the following conventions:

$$\theta^*_{i,j} = \theta^*(x_i, y_j), \tag{2.35}$$

and

$$s_{i,j} = \begin{cases} \dfrac{u(x_i, y_j)}{w_c} & \textit{in the fluid} \\ 0 & \textit{in the solid} \end{cases}, \tag{2.36}$$

the Poisson equation becomes:

$$\frac{1}{\Delta^2}\left(\theta^*_{i+1,j} + \theta^*_{i-1,j} - 2\theta^*_{i,j}\right) + \frac{1}{\Delta^2}\left(\theta^*_{i,j+1} + \theta^*_{i,j-1} - 2\theta^*_{i,j}\right) = s_{i,j}. \tag{2.37}$$

By a transformation from the 2D-matrix, $\theta^*_{i,j}$ to a 1D-vector, $\theta^*_{i(J+1)+j} = \theta^*_{i,j}$, whose length is $(I+1)(J+1)$, and an equivalent transformation for $s_{i,j}$, the former equation can be written as:

$$\theta^*_{k+(J+1)} + \theta^*_{k-(J+1)} + \theta^*_{k+1} + \theta^*_{k-1} - 4\theta^*_k = s_k. \tag{2.38}$$

It should be noticed that this equation is valid only inside the domain (for $1 \le i \le I\text{-}1$ and $1 \le j \le J\text{-}1$), the other points correspond to the boundaries of the domain for which boundary conditions are specified. Once these boundary conditions are well defined, a linear system of $(I\text{-}1)(J\text{-}1)$ equations is obtained.

The Matlab program, which solves the Poisson equations numerically using the finite differences method is presented in the Appendix [A]. In order to estimate the accuracy of computation, the influence of the grid size on the results has been investigated. So, for a flow rate of 0.118 l/min and a pressure drop of 0.2 bar over an array of 75 channels (100x300 μm^2) with a length of 1 cm, calculations have been carried out with different grid sizes (Fig. 4).

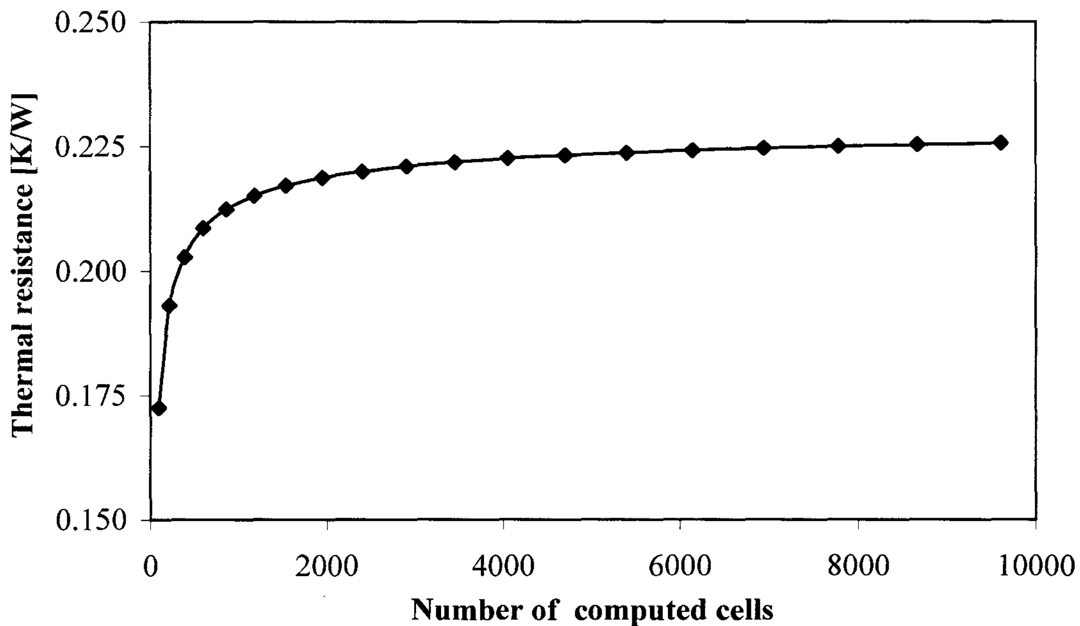


Figure 4. Computed thermal resistance as a function of the number of computed cells.

From Fig. 4 follows that the thermal resistance, determined with use of the Matlab program, approaches a constant value for large numbers of computation cells. The maximum number of computation cells is limited by the computer memory.

The most important assumption underlying the analytical model is that the flow is already fully developed (both thermally and hydraulically). Another limitation is that the fluid properties, like the viscosity, are assumed to be independent of temperature. The advantage of applying the analytical model is mathematical simplicity, which limits the computation time to only a few seconds. The geometry of the channels can be optimized, within the boundary conditions, with use of the Matlab program, so the program can be used as a design tool.

The water velocity profile computed with the numerical program for a flow rate of 0.10 l/min is shown in Fig. 5.

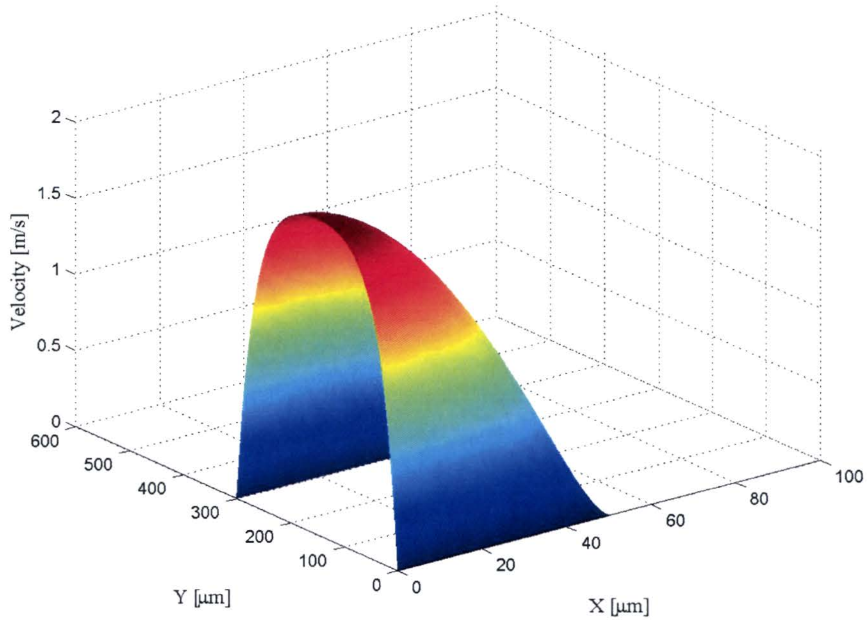


Figure 5. Velocity profile in a micro-channel for a flow rate of 0.10 l/min.

The cross-sectional temperature field at the channel inlet is plotted in Fig. 6 for a flow rate of 0.10 l/min, and a uniform heat flux of 100 W/cm^2. The mean inlet water temperature is taken to be 20 °C.

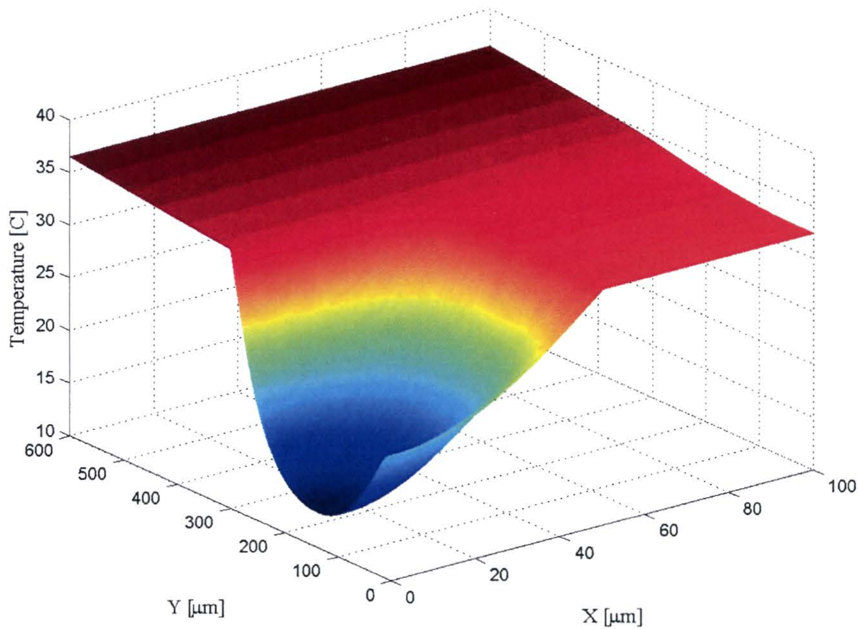


Figure 6. Cross-sectional temperature distribution at the channel inlet, for a flow rate of 0.10 l/m and a uniform heat flux of 100W/cm^2.

The outlet temperature profile (for a channel length of 1cm) is shown in Fig. 7. This profile has exactly the same shape as the inlet temperature profile, it is only shifted to a higher temperature originating from the assumption that the flow is fully developed (both thermally and hydraulically). The boundaries between the solid and the liquid are clearly visible. Due to the high thermal conductivity of silicon, the temperature gradient in the silicon is relatively small and the temperature distribution resembles almost isothermal. It can be noticed that the temperature in the fins varies almost linearly as a function of the fin height.

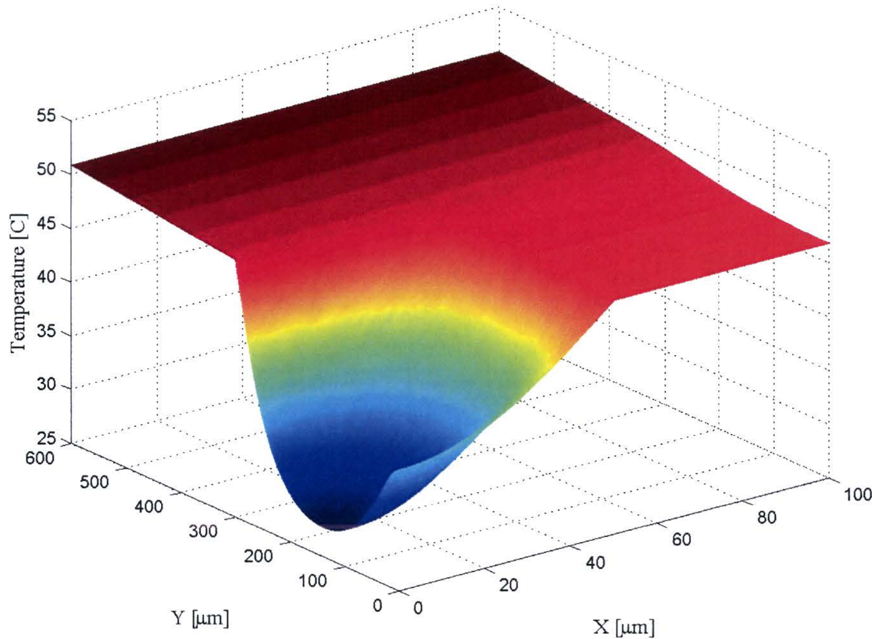


Figure 7. Cross-sectional temperature distribution at the channel outlet, for a flow rate of 0.10 l/m and a uniform heat flux of 100W/cm^2.

The local Nusselt numbers have also been calculated along the solid liquid interface for an equivalent flow rate of 0.10 l/min, and a uniform heat flux of 100 W/cm^2. The local Nusselt numbers are normalized to the maximum value Nu_{max} = 15.0 and are shown in Fig. 8 and Fig. 9.

The Nusselt number reaches its minimal value at the corner of the channel, where the local velocities and the temperature gradients are the smallest. The local Nusselt number reaches a maximum at the base center and along the fin at $Y=Y_c<H_c/2$. Although the velocity profile is symmetric with respect to fin mid height ($Y=H_c/2$), the same is not true for the Nusselt number. Two factors create this asymmetry. The temperature is not constant in the fin, but decreases towards the end of the fin (minimum at Y=0) and because the boundary at Y=0 is insulated.

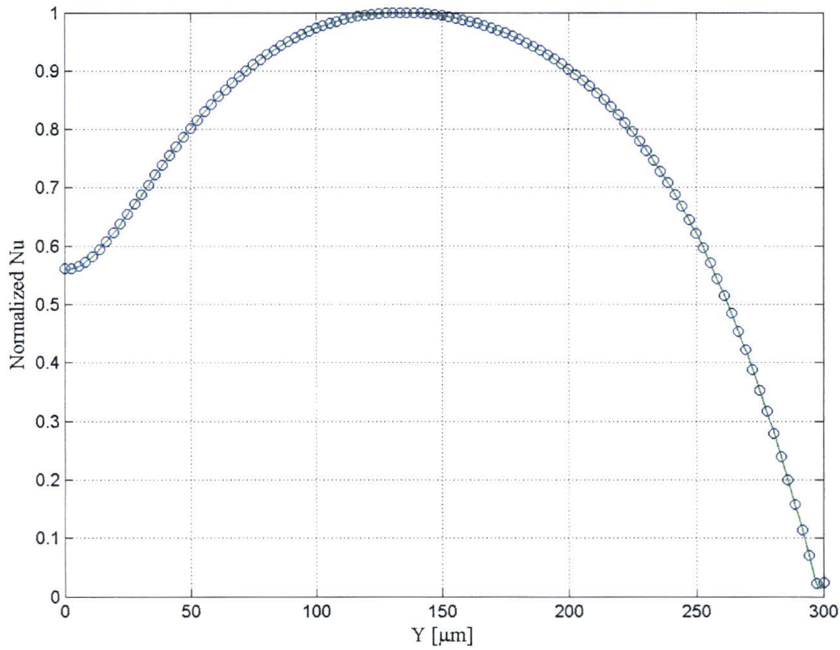


Figure 8. The local Nusselt number as a function of the position along the fin, for a flow rate of 0.10 l/min and a heat flux of 100 W/cm^2. The location Y=300 μm corresponds to the channel corner.

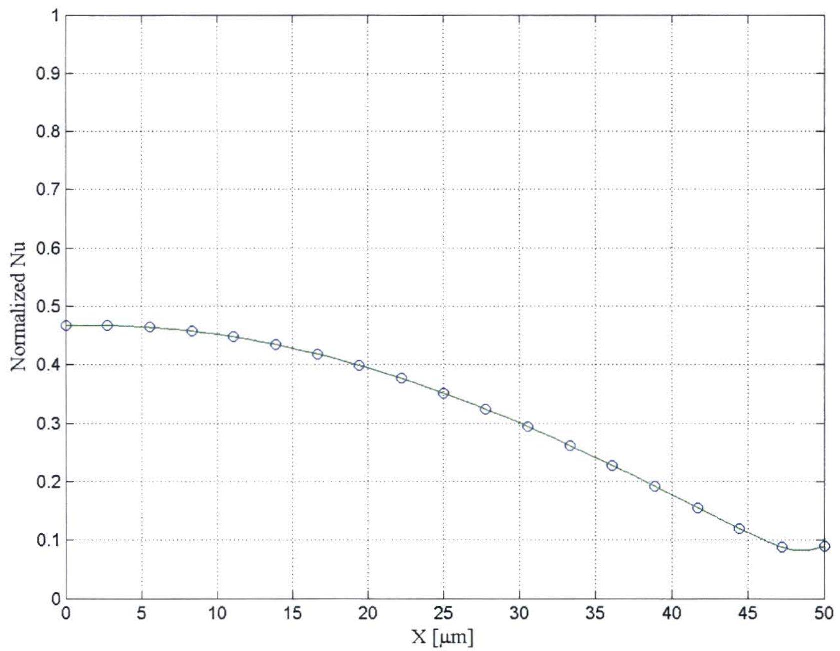


Figure 9. The local Nusselt number as a function of the position along the base, for a flow rate of 0.10 l/min and a heat flux of 100 W/cm^2. The location Y=50 μm corresponds to the channel corner.

Chapter 3

Practical implementation

3.1 Fabrication of micro-channels in Silicon

In this chapter, a survey is given of the micro-channel processing. Micro-channels with a depth of 300 μm and a width of 100 μm have been constructed. The fins also have a width of 100 μm. The channels and fins have a length of 1.5 cm, and the total device exists of an array of 75 channels. The geometry and dimensions are shown in Fig. 1.

The micro-channels are made in a 6-inch silicon monitor wafer (20-30 Ωcm, p-type). First of all, the organic contamination layer on top of the wafer needs to be removed. This is done by cleaning the wafer, for 10 minutes, in concentrated sulphuric acid (H_2SO_4, 96 %) and hydrogen peroxide (H_2O_2, 31 %) mixture at 90 °C (Piranha clean). After the wafer is cleaned, a layer of SiO_2 with a thickness of 1 μm is grown by wet oxidation. The wafer is cleaned again with Piranha, to supply the surface with OH-groups. Before the resist is spincoated, the wafer is TMSDEA primered (TriMethylSilylDeEthylAmine) to improve the adhesion between the SiO_2 layer and the resist. On top of this SiO_2 layer a layer of resist (AZ4533, Micro Chemicals)) is spincoated, with a thickness of 6.35 μm (1500 rpm) (on the backside of the wafer). After the resist is applied by spin coating, the wafer is baked on a hotplate (90 °C, 3 minutes) to remove remaining solvent in the film. To pattern the micro-channels in the resist, the wafer is exposed to ultraviolet light for 90 seconds, using a foil-mask with the micro-channel design (Fig. 10 A). Because the ultraviolet light changes the chemical properties of the positive resist, the exposed resist can be removed, by developing the wafer for 2 minutes in developer AZ400K 1:3 (Micro Chemicals). After development, it is possible that still some resist remains on the wafer (on the places where the resist had to be removed). To remove the remnants of the resist, a descum (1 minute plasma-oxide etch (800 W, 130 °C)), is done in an IPC Barrel (Branson). After a convection bake at 90 °C for 30 minutes the SiO_2 is removed in the places where the resist was exposed and developed. This is done using Reactive Ion Etching in the Applied Materials Precision 5000. Reactive Ion Etching is also used to etch the micro-channels in the silicon. This is done using the Bosch etch procedure [3] on an HRE-STS Advanced Silicon Etcher (See 3.2) (Recipe: Timmed 2, 100 minutes). The resist as well as the SiO_2 layer act as a mask for the silicon etching process (Fig. 10 B). When the micro-channels have been made in silicon, the resist needs to be removed. This is done by a resist strip in the IPC Barrel (60 Minutes of plasma-oxide (800W, 130 °C)). The SiO_2 layer is also removed, because this layer is a thermal barrier, using buffered HF (7:1, 80 nm/min). The wafer is cleaned again in Piranha and to make the wafer surface hydrophilic a thin layer (100 nm) of SiO_2 is grown on the wafer by wet oxidation (8 minutes 1000 °C) (Fig. 10 C). Figure 11 depicts a SEM microphotograph of the micro-channels.

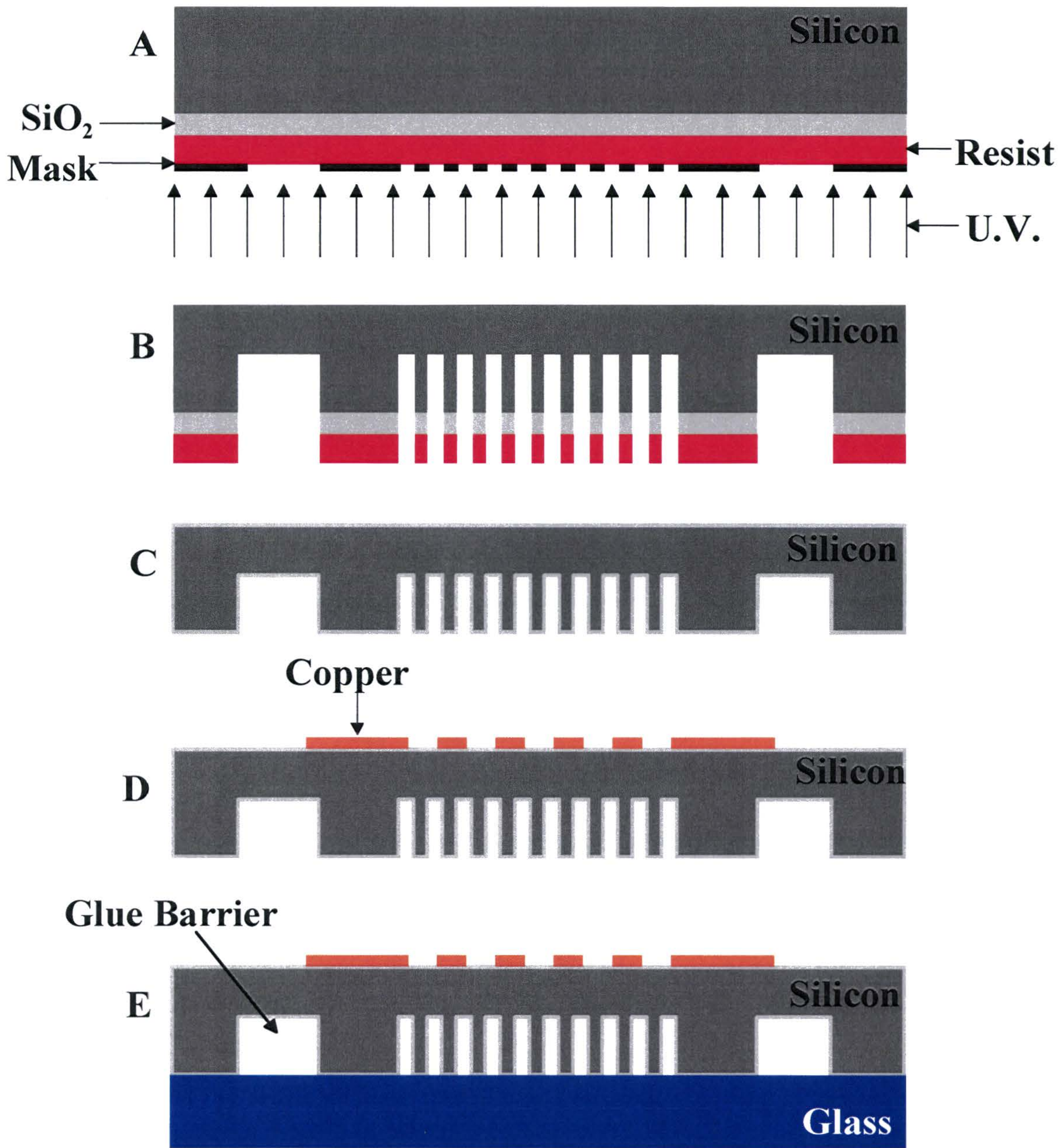


Figure 10. Most important process steps for the fabrication of integrated micro-channels in silicon.

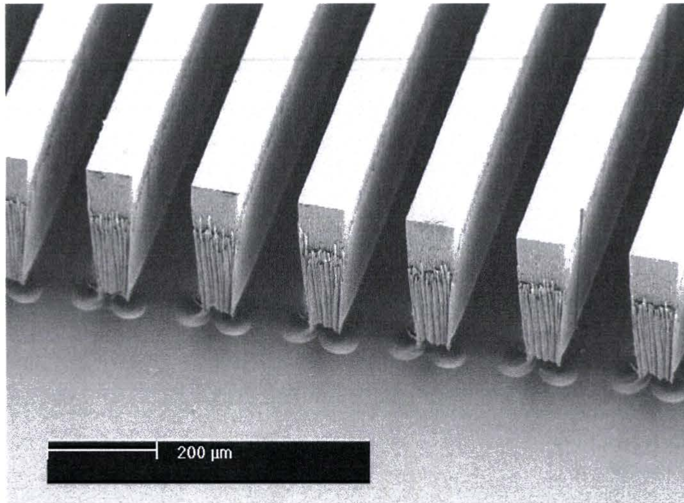


Figure 11. SEM microphotograph of the micro-channels, with a channel and fin width of 100 µm and a depth of 300 µm. The channel width at the bottom of the channel is larger than at the top, because the etching process is not optimised.

To simulate the power generated by a CPU, a meander-shaped copper heater (Fig. 12) is electro-plated on the front side of the wafer to a thickness of approximately 10 µm. Before the heater is electro-plated, a plating base consisting of 20 nm chrome and 200 nm copper is sputtered on the front side of the wafer. The layer of chrome is needed to prevent the copper diffusing into the silicon and it also improves the adhesion between the silicon and the copper layer. Directly before resist is spincoated, the wafer is put for 10 seconds in copper oxide etch (10 gr $Na_2(SO_4)_2$ solved in 1 liter water and 2.5 ml H_2SO_4). On top of the plating base, a layer of resist (AZ4562, Micro Chemicals) is spincoated, with a thickness of 11 µm (1500 rpm). After the resist is applied by spin coating, the wafer is put in a convection oven (90 °C, 30 minutes) to bake the resist. To pattern the meander-shaped heater in the resist, the wafer is exposed to ultraviolet light for 90 seconds, using a foil-mask. The foil mask must be aligned to the front side of the wafer. The resist is developed for 2.5 minutes in AZ400K 1:3 (Micro Chemicals). Directly before the copper is electro-plated, the wafer is baked in a convection oven (30 minutes at 90 °C), put for 15 seconds in the copper oxide etch, and 1 minute in a water bath with one droplet of Triton X100 surfactant (USBiological). A layer of copper is electro-plated in a bath of commercially available plating solution, to a thickness of approximately 11 µm. The resist is removed with acetone, the copper of the plating base is etched in a solution of 900 ml H_2O, 25 ml H_2SO_4 (96 %) and 75 ml H_2O_2 (30 %) and the chrome is removed using a chrome etch solution (Fig. 10 D).

The last step in the process is gluing a glass plate on the wafer to cover the micro-channels. Two holes are lasered in the glass plate, which are needed for the in- and outflow (see Fig.1). The glass plates are cleaned with use of Piranha at 60 °C and they are scrubbed. Both the wafer and the glass plate are primered (mixture of Isopropylalcohol - demiwater - Methacryloxy-propyltrimethoxysilaan, 50:50:1, Johnson Matthey) to improve the adhesion with the glue. The wafer and the glass plate can be

glued using a UV curing adhesive (Diacryl 101; Di-ethoxylated Bisphenol A Dimethacrylate (AKZO) with photo initiator Irgacure 651 (Ciba-Geigy)), a day after they are primered. The glass plate is squeezed on the silicon wafer and with use of the capillary force is the glue applied between them. A glue barrier is etched around the micro-channel device to prevent the glue going inside the micro-channels. The glue is cured using UV-light (Fig. 10 E). The connection tubes are glued on top of the glass plate in the same way. The final device is shown in Fig. 13.

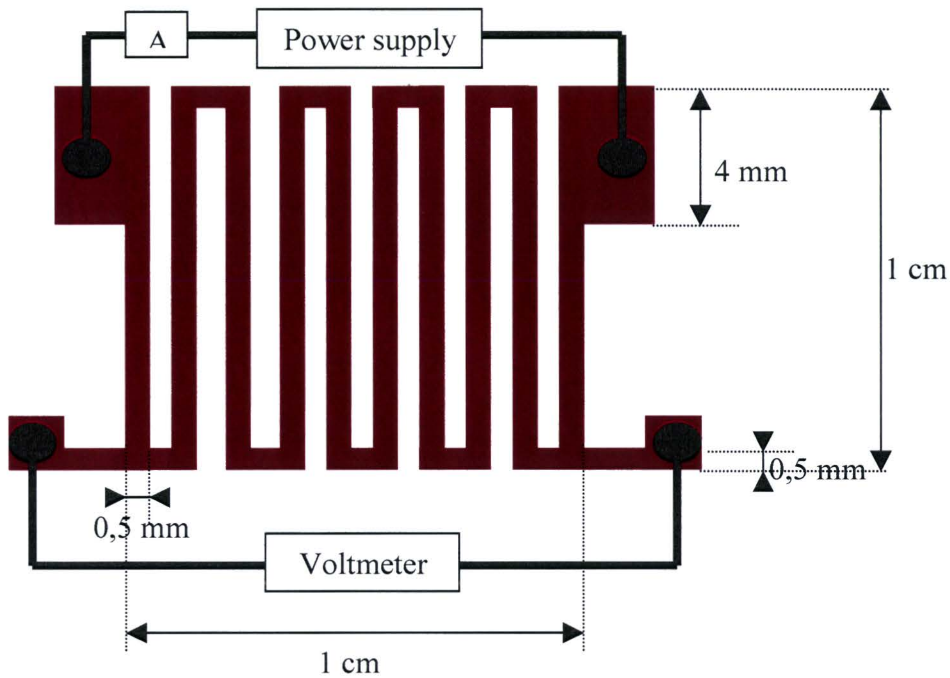


Figure 12. The geometry of the meander-shaped heater, with the electrical connection areas.

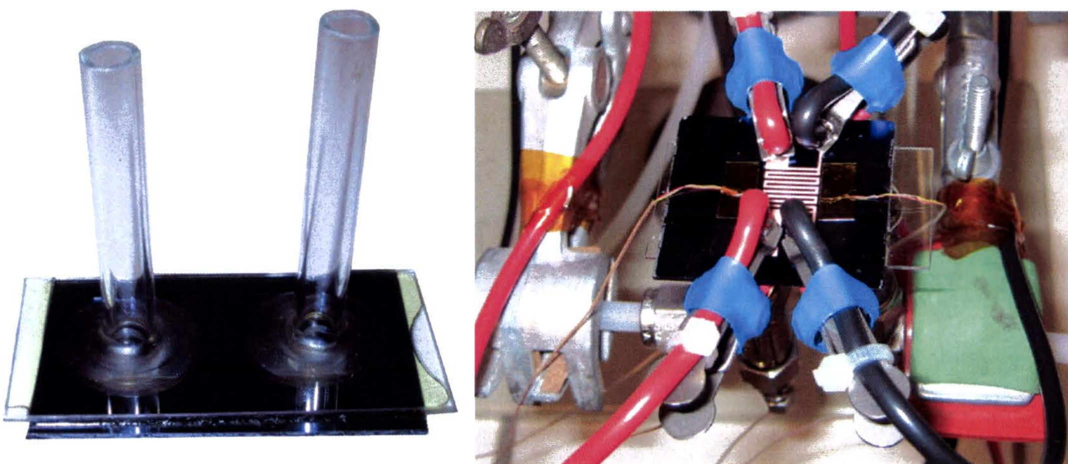


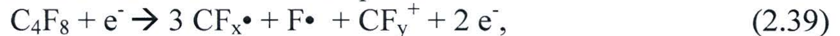
Figure 13. Left: Final device, micro-channels in silicon, covered with a glass plate and with two connection tubes glued on the glass plate. Right: Cooling device connected in the set-up. Clearly visible are the copper heater and the electrical connections.

3.2 Anisotropic dry etching of silicon

The most essential step in the process is the deep etching of the micro-channels in the silicon wafer, therefore this step is discussed in more detail. The STS silicon etch process is based on a patented process developed by Bosch GmbH and uses a variation of the sidewall passivation technique. Rather than continuous sidewall protection being an integral part of the existing anisotropic etching process, in the Bosch-type etch processing the passivation is deliberately segregated by using sequentially alternating etching and deposition steps. First a sidewall passivation monomer is deposited and polymerized, subsequently the polymer and silicon are etched from the bottom of the trench, to allow the etching to proceed directionally. In the cyclic way, the etching and deposition can be balanced to provide an accurate control of the anisotropy. The principle of the Bosch process can be best understood by considering a simple model of a C_4F_8 / SF_6 dry etching process. Consider the relative simple deposition and etch precursors C_4F_8 and SF_6, respectively.

3.2.1 Deposition step

Firstly, the deposition precursor gas is dissociated by the plasma to form ion and radical species. A possible chemical reaction for this process is:



$$C_4F_8 + e^- \rightarrow 3\ CF_x\bullet + F\bullet\ + CF_y^+ + 2\ e^-, \qquad (2.39)$$

which undergo polymerization reactions to result in the deposition of a polymeric layer:

$$n\ CF_x\bullet \rightarrow (CF_2)_n\ (s). \qquad (2.40)$$

Here the suffix (s) is used to emphasize the depostion of the solid-state passivation film. This passivating Teflon-like layer $(CF_2)_n$ is deposited on the surfaces of the silicon and the mask during this first step, as shown schematically in Fig. 14.

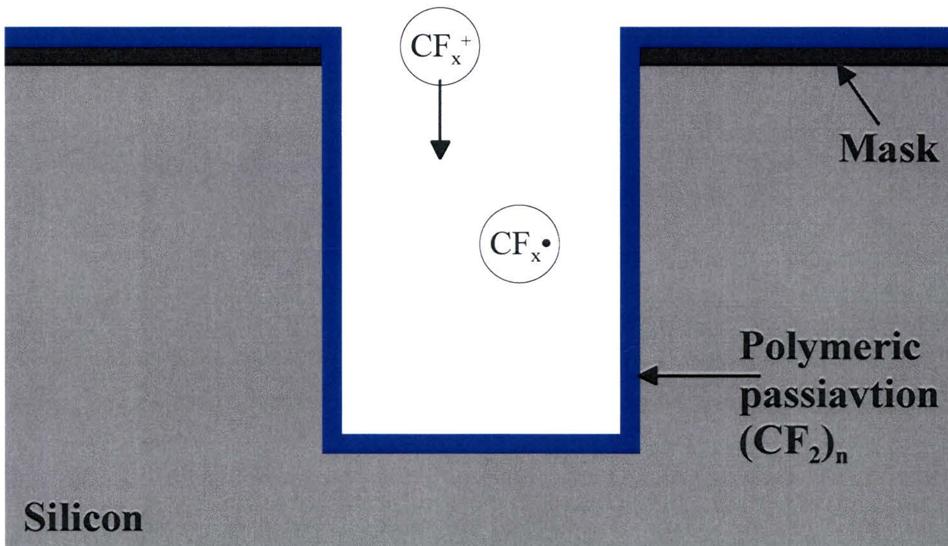
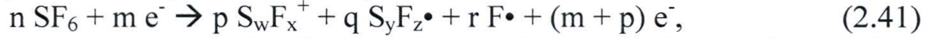


Figure 14. Deposition step.

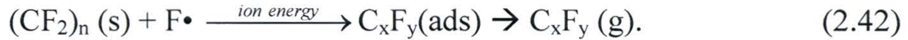
3.2.2 Etch step

The second step is the etching step. The gases are then switched to allow etching. During this subsequent etch step, the SF_6 firstly dissociates:



$$n\,SF_6 + m\,e^- \rightarrow p\,S_wF_x^+ + q\,S_yF_z\bullet + r\,F\bullet + (m+p)\,e^-, \quad (2.41)$$

It illustrates the formation of ion and radical species by electron (e) impact dissociation. Next, the fluorine radicals and ions must remove the surface passivation layer from the bottom while the sidewall passivation is left intact.



$$(CF_2)_n\,(s) + F\bullet \xrightarrow{ion\ energy} C_xF_y(ads) \rightarrow C_xF_y\,(g). \quad (2.42)$$

The ion bombardment plays a critical role. The ions are accelerated in the direction perpendicular to the bottom of the micro-channels, with use of a bias potential. It removes the passivation layer only on the bottom and not on the sidewalls. Now the fluorine radicals can proceed further with the silicon etching by adsorption (ads), followed by product formation and desorption as a gas (g):

$$Si + n\,F\bullet \rightarrow Si\text{-}nF, \quad (2.43)$$

$$Si\text{-}nF \xrightarrow{ion\ energy} SiF_x(ads), \quad (2.44)$$

$$SiF_x(ads) \rightarrow SiF_x\,(g). \quad (2.45)$$

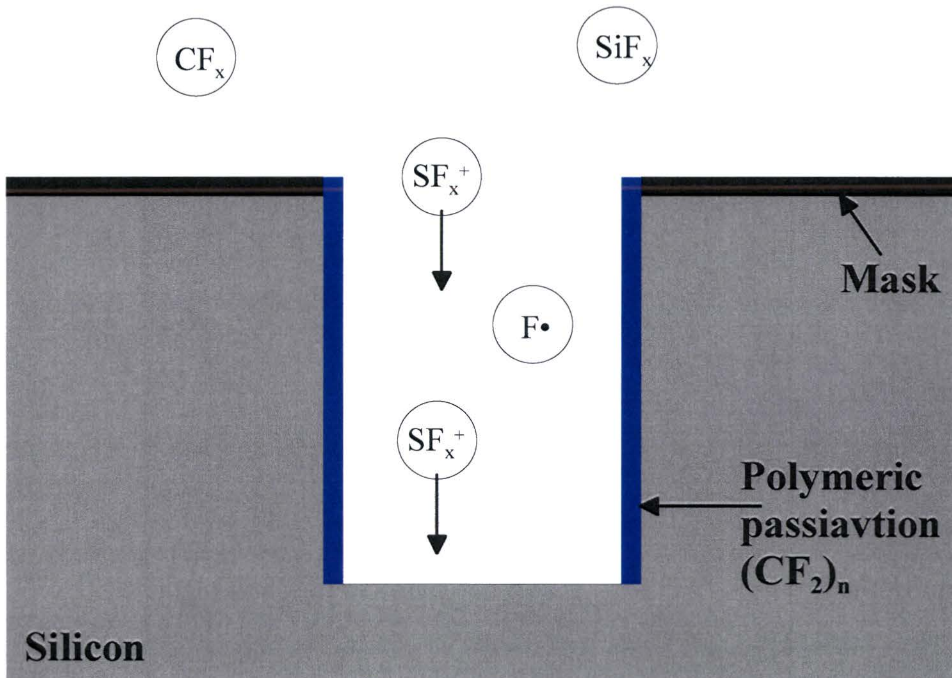


Figure 15. Etch step.

The silicon etching and passivation layer etching (conditioned by ion bombardment) can be broken down into six primary steps as illustrated in Fig. 16. The first step is the production of the reactive species in the gas-phase (1). In a glow discharge the gas dissociates to some degree by impact with energetic particles. This step is vital because most of the gases used to etch thin films do not react spontaneously with the film. In a second step, the reactive species diffuse to the solid (2), where they become

adsorbed (3) and react with the surface (4). Finally, the reaction products leave the surface by desorption (5) and diffusion (6).

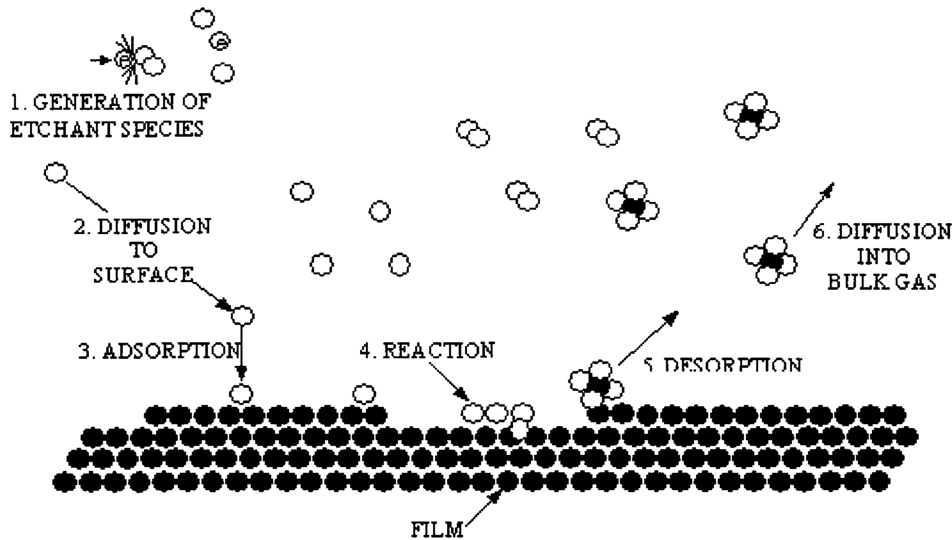


Figure 16. Primary process occurring in a plasma etch process.

The cycle including passivation and etching is repeated until the expected depth is reached. The directionality of the etching is controlled by the ion bombardment through its role of aiding the removal of the surface polymer. The etching is controlled by process time, the flow of the injected gas, the pressure, bias power, coil power and temperature. The wafer temperature during processing is maintained by helium cooling flowing along the backside of the wafer. This process is carried out in a so-called ICP plasma (Inductive Coupled Plasma) and is referred as DRIE (Deep Reactive Ion Etching). As can be seen in Fig. 11, the etching process is not optimised. The channel width at the bottom of the channel is too large, because the passivation step at the end of the process is too short.

3.3 The heater calibration

The heater is almost directly electro-plated on the silicon wafer to prevent an intermediate layer, which act as a thermal barrier, between the micro-channels and the heater in the experimental setup. Only a 20 nm thick layer of chrome and a 100 nm thick layer of SiO_2 is present between the copper heater and the silicon. However, this is only a very small thermal barrier, R_{cond} ~10^{-5} W/K. The dissipated power in the heater is determined by measuring the current through the heater and the voltage over the heater, with a 4-points measurement. As can be seen in Fig. 12, the voltage is not measured over the entire length of the heater, so the applied voltage is not equal to the measured voltage. Some experiments have been done to investigate the relation between the measured and applied voltage. The following relation has been found:

$$V_{applied} = 1.18\, V_{measured}. \qquad (2.46)$$

The resistance of the heater is temperature dependent, this is why the mean heater temperature can be determined by measuring the resistance of the heater. The heater has been calibrated to find the relation between the resistance and the mean heater temperature. The calibration has been done by adjusting the heater temperature in a temperature-controlled oven, and measuring the resistance of the heater with a 4-points measurement at different temperatures. A heater calibration is shown in Fig. 17. The steepness of the calibration curve is characteristic for the used material and the deposition method. The offset depends on the thickness of the copper layer, so other copper heaters have approximately the same ramp, but another offset.

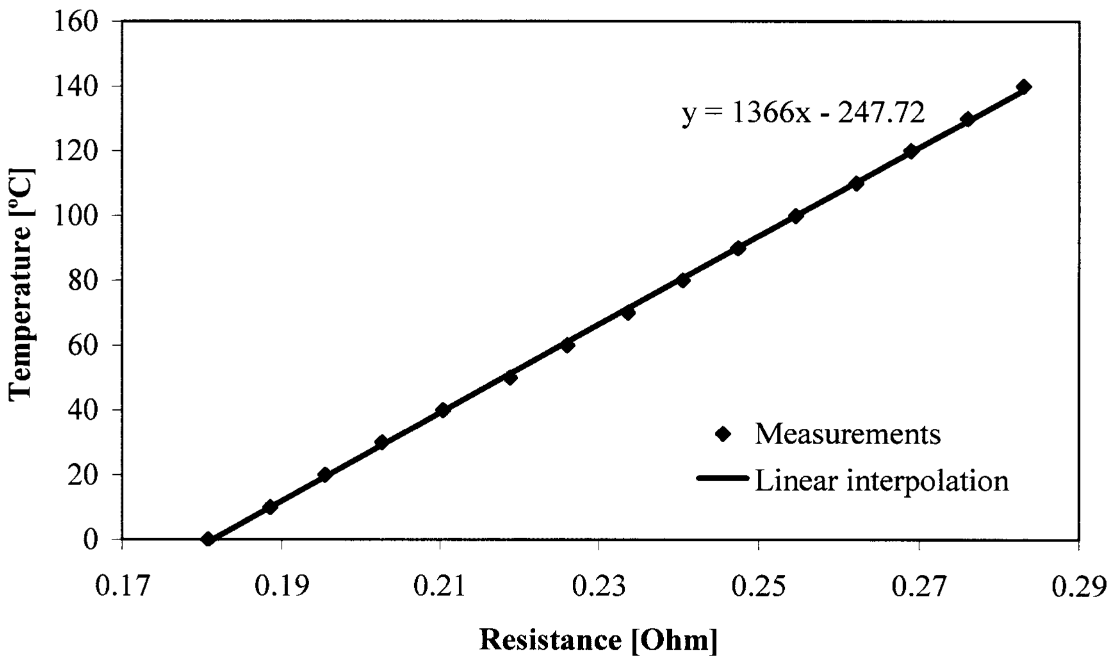


Figure 17. Heater calibration.

3.4 Experimental setup

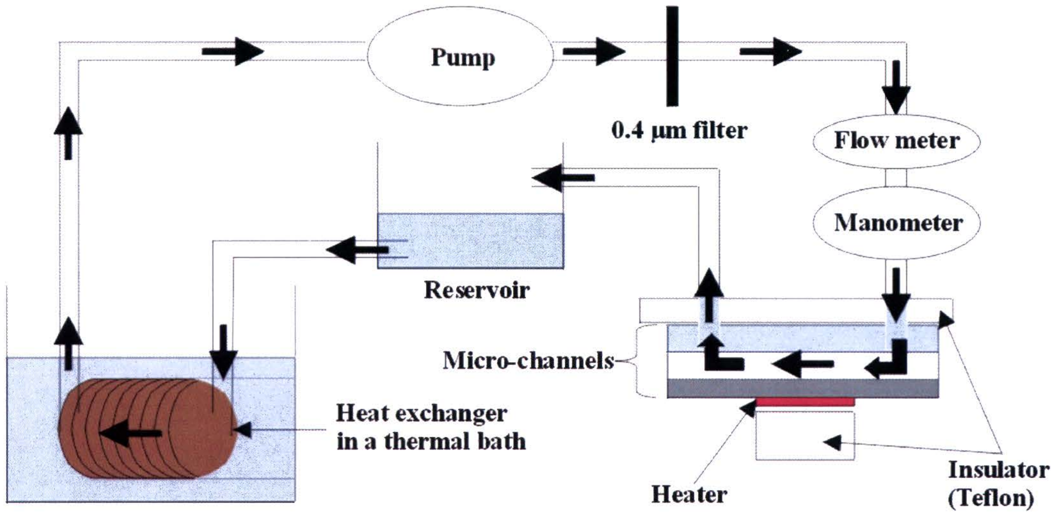


Figure 18. Experimental setup.

The complete experimental setup consists of a closed hydraulic circuit composed of a mechanical pump, a 0.4 µm filter, a flow meter, a manometer, and heat exchanger located in a thermal bath in order to have a constant inlet water temperature (Fig. 18). Temperatures at five different points in the setup are measured using thermocouples (Fig. 19). Two thermocouples are inside the fluid, one near the entrance of the micro-channels (T_{in}) and one at the end (T_{out}), to measure the water inlet and outlet temperature respectively. Two thermocouples are situated on the silicon, near the heater, one on the side of the inlet ($T_{j\text{-}in}$) and one on the side of the outlet ($T_{j\text{-}out}$). The last thermocouple is placed on the glass plate opposite the heater (T_{glass}). All the experiments have been done with demi water.

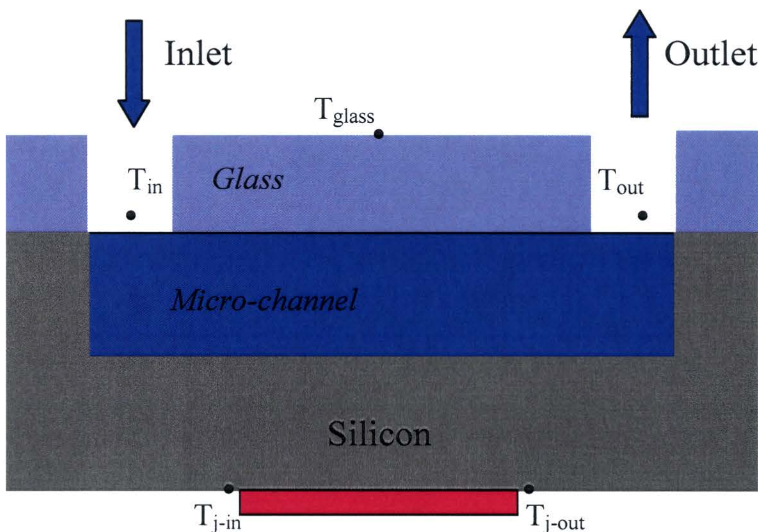


Figure 19. Thermocouples location (Side view).

Chapter 4

Experimental results and comparison with calculations

Several experiments with different flow rates and with different heat dissipations have been carried out and compared with the numerical calculations. The calculations were done by solving numerically the conjugate heat transfer problem consisting of the simultaneous determination of the temperature fields in both the solid substrate and in the water (analytical model, chapter 2.3). The performance of the device is measured by its total thermal resistance (R_{th}), which is defined as:

$$R_{th} = \frac{T_h - T_{in}}{P}, \qquad (2.47)$$

where T_h the mean heater temperature, T_{in} the inlet water temperature and P the dissipated power. The mean heater temperature is determined by a four-point measurement of the resistance of the heater. The error in the dissipated power measurement is less then 2% of the total dissipated power. The error in the measured temperature difference between the mean heater temperature and the inlet temperature is less than 0.5 °C. This results in an error in the total thermal resistance in the order of 0.01 K/W.

The thermal resistance depends on the flow rate through the micro-channels. The thermal resistance, measured and calculated, as a function of the flow rate with P = 100 W is shown in Fig. 20. As can be seen from Fig. 20, the measured thermal resistance for flows in excess of 0.2 l/min is lower than the thermal resistance calculated using the analytical model (by a factor of two for flows around 1 l/min). This can be explained from the fact that the analytical model assumes a fully developed flow (both hydraulically and thermally) at the entrance of the micro-channels. However, this is not the case, in particular not for high flow rates. The analytical model assumes a mean inlet temperature of 20 °C, but the water temperature near the micro-channel wall is assumed to be higher, as can be seen in Fig. 6. However, in the experiments the water temperature at the entrance of the micro-channels is really 20 °C, also near the micro-channels wall, because the flow in not fully developed near the micro-channel entrance. Resulting in a lower experimental thermal resistance then expected according to the analytical model.

Figure 20 also shows that the calculations predict a more or less constant thermal resistance for flow rates above 0.6 l/min. However, the experiments show that the thermal resistance continues to decrease for increasing flow. This is because the calculations assume a laminar flow, while in fact the flow becomes turbulent for flow rates in excess of 0.6 l/min. The onset of turbulence is measured by monitoring the flow rate as a function of the pressure drop as shown in Fig. 21.

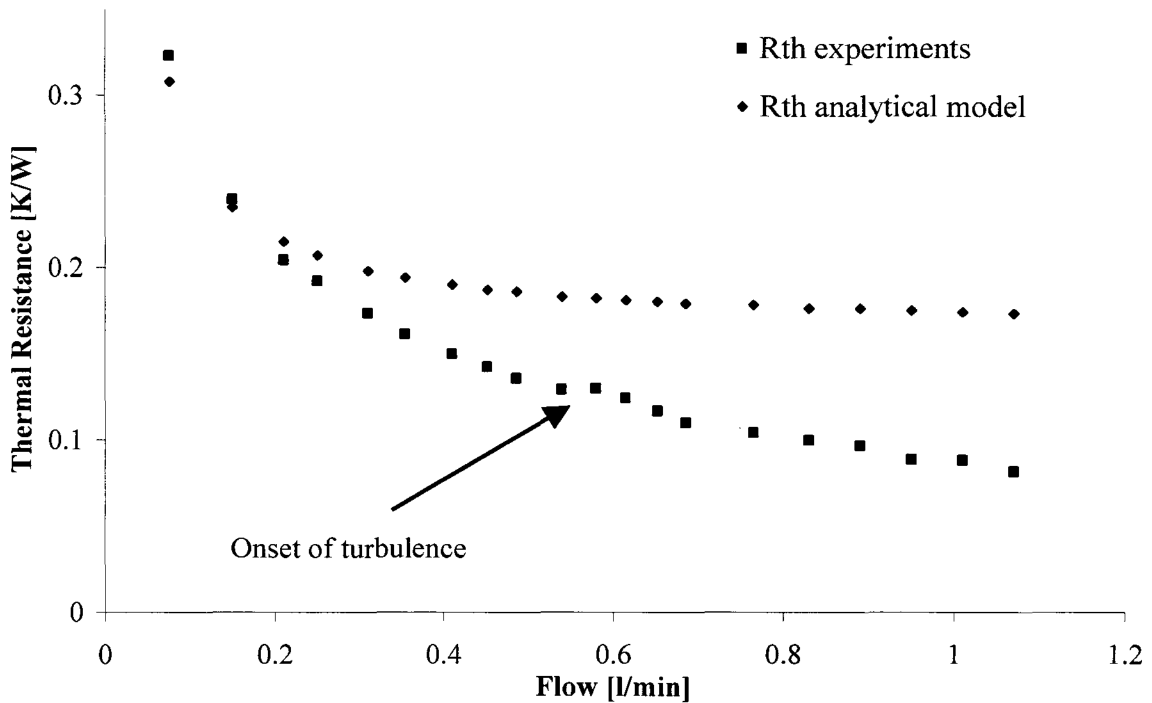


Figure 20: The experimental, calculated and simulated thermal resistance as a function of the flow rate for a dissipated power of 100 W. The error in the measured thermal resistance is in the order of 0.01 K/W.

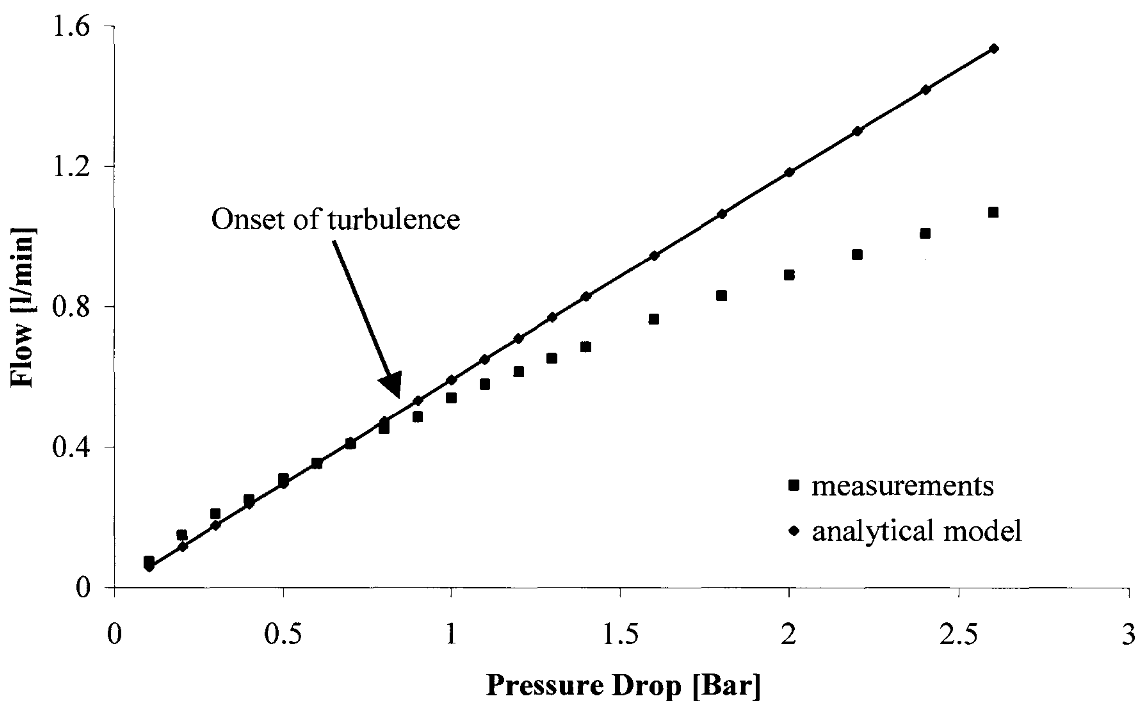


Figure 21. Flow rate as a function of the pressure drop over the micro-channels. The error in the measured thermal resistance is in the order of 0.01 K/W.

The transition between laminar and turbulent for micro-channels occurs for Reynolds numbers (Re) ≈ 200-700 [1]. The Reynolds number corresponding to a flow rate of 0.6 l/min for our device is $Re = 630$, so the measured onset of turbulence is in agreement with literature. Turbulence in the micro-channels is desirable because it increases the heat transfer coefficient for water convection. The disadvantage of turbulence is that a higher pressure drop is needed to generate the same flow rate.

High flow rates require relatively large reservoirs and pressures, which is not practical for the cooling of electronics. For this reason the focus of the next paragraphs will be on modest flow rates of ~ 0.1 l/min. In this range, the flow in the micro-channels will be fully developed already a short distance from the channel entrance (ca. 1 mm) [2,4]. Under this condition the analytical model gives a good approximation of the thermal resistance. Figure 22 shows the measured thermal resistance as a function of dissipated power, at a constant pressure drop of 0.15 bar over the device. For this pressure drop a flow rate of 0.089 l/min and a thermal resistance of $R_{th} = 0.29$ K/W is predicted by the analytical model. However, in reality, the flow rate also depends on the dissipated power, since the water viscosity varies with temperature. The measured flow rate for example at a constant $\Delta p \approx 0.15$ bar at 50 W is 0.084 l/min, and increases to 0.108 l/min at 370 W. Taking the temperature dependence of viscosity into account, the thermal resistance can be calculated as a function of dissipated power using the analytical model. The results of this calculation are depicted in Fig. 22. A small difference remains between the calculated thermal resistance using the analytical model and the measured thermal resistance for power dissipation below 100 W. This can probably be explained by the fact that the heat transport from the heater used during the measurements is not uniform. The heat transport from the heater to the water is so fast that at low power densities the heat does not have the time to spread uniformly. This results in a smaller effective area used for heat exchange and consequently in a higher thermal resistance. For power densities above 100 W/cm^2 the heater apparently operates uniformly.

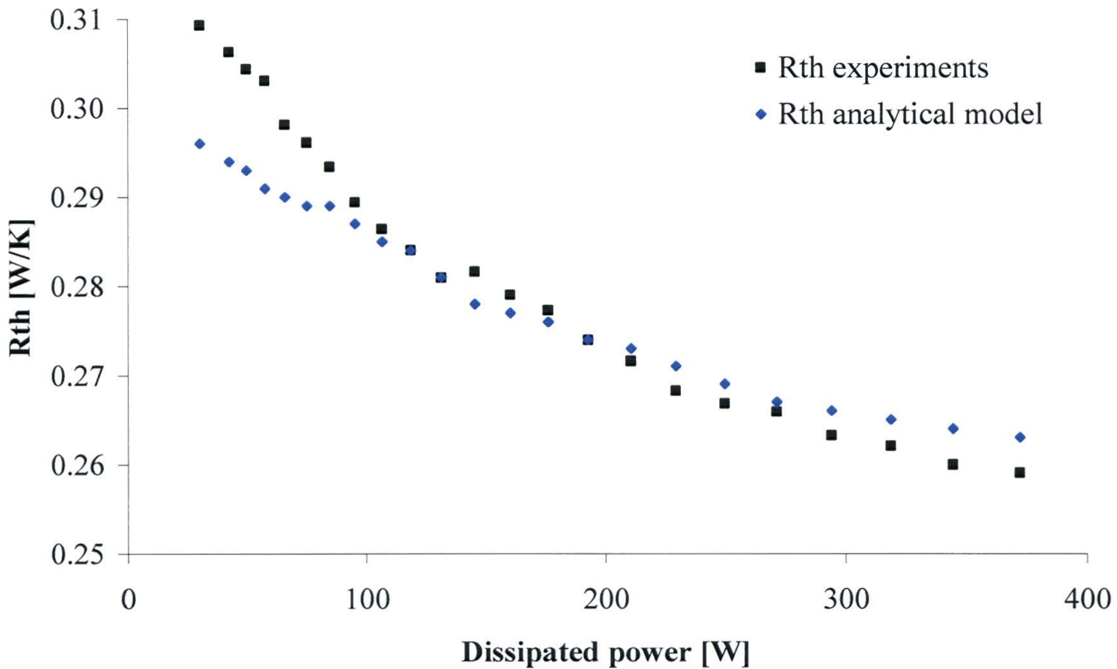


Figure 22. Thermal resistance as a function of the dissipated power at a constant pressure drop $\Delta p \approx 0.15$ bar. The viscosity in the analytical model is determined from the experiments, which results in a non-smooth character of the curve associated with the analytical model. The error in the measured thermal resistance is in the order of 0.01 K/W.

Theoretically the thermal resistance does not depend directly on the dissipated power. There is only an indirect relation through the temperature dependence of the viscosity of water, and the thermal conductivity of water and silicon. This also follows from the measurements. When the thermal resistance is multiplied by the flow through the micro-channels an almost constant value of 0.026 is found. This is the same value as predicted by the analytical model.

Figure 23 shows the mean heater temperature, the inlet water temperature and the outlet water temperature as a function of dissipated power at $\Delta p \approx 0.15$ bar over the micro-channels (same measurements as shown in Fig. 22). The maximum temperature under normal operation conditions in an IC is limited to 120 °C. But instead of measuring the maximum temperature, the mean heater temperature is measured. The temperature gradient over one strip of the heater is linear, assuming that the flow is fully developed (both hydraulically and thermally). This temperature gradient approximately equals the temperature gradient between the inlet water temperature and the outlet water temperature. Under these approximations it is possible to calculate the maximum temperature (Fig. 24).

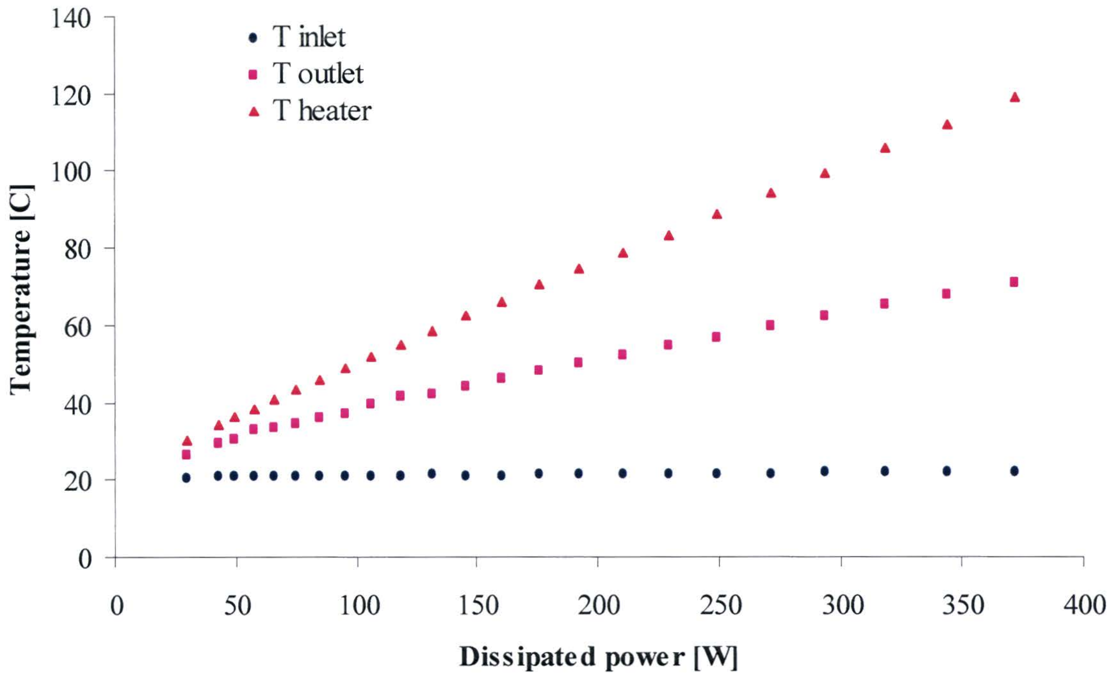


Figure 23: The inlet, outlet and mean heater temperature as a function of the dissipated power at a constant pressure drop $\Delta p \approx 0.15$ bar.

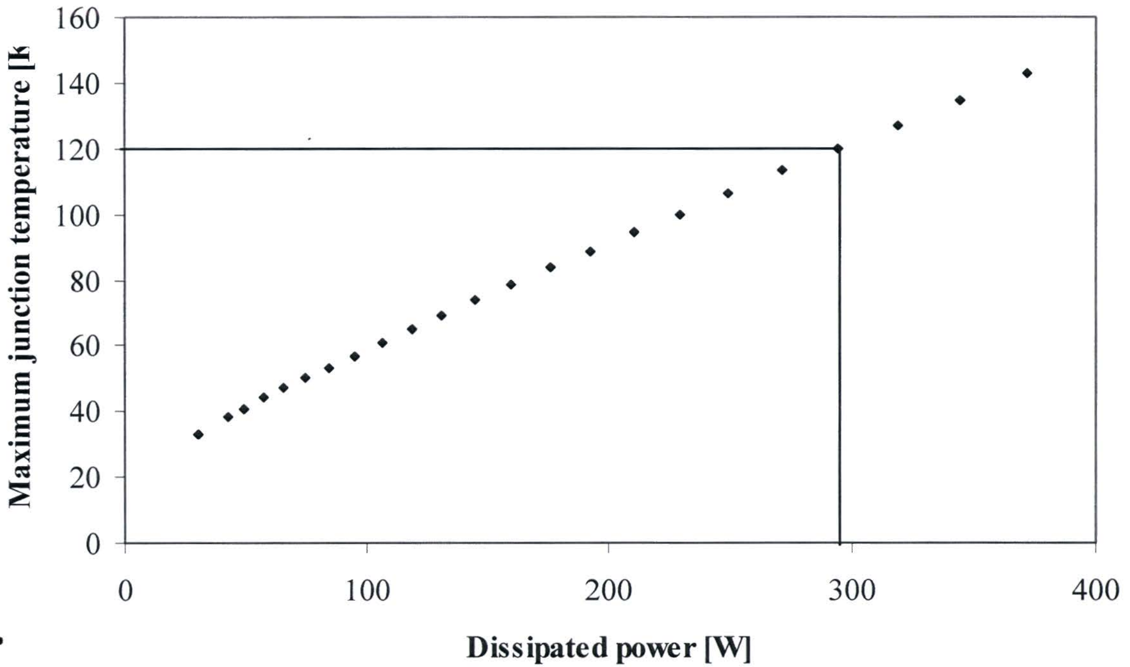


Figure 24. Maximum junction temperature as a function of the dissipated power at a constant pressure drop $\Delta p \approx 0.15$ bar.

Figure 24 depicts that at a flow of 0.1 l/min, the maximum cooling capacity without exceeding a maximum junction temperature of 120 °C is almost 300 W. Using a flow rate of 1.1 l/min a peak dissipation of 428 W is achieved with a mean heater temperature of 55 °C, which corresponds to a thermal resistance of 0.08 K/W.

Because the experimental device is not perfectly insulated, there is also heat transport by natural air convection. The error caused by the natural air convection during these measurements is small. The amount of transported heat by the water can be calculated from:

$$P = \rho \dot{V} C_p \Delta T , \tag{2.48}$$

with ρ the water density, $\dot{V}$ the volumetric flow rate, C_p the specific heat of water and ΔT the water temperature difference between the inlet and outlet (Fig. 23). For example, at a power dissipation of 370 W, the power transported by the water is approximately 365 W. The remaining 5W is transported by natural air convection. This is less than 2 % of the total dissipated power. The natural convection (without insulation) was also measured as a function of the mean heater temperature (Fig. 25). Because there is no active cooling during this measurement, the temperature of the total device is almost uniform. For this reason, the natural air convection as a function of the heater temperature is an overestimation compared with the natural air convection during the other measurements.

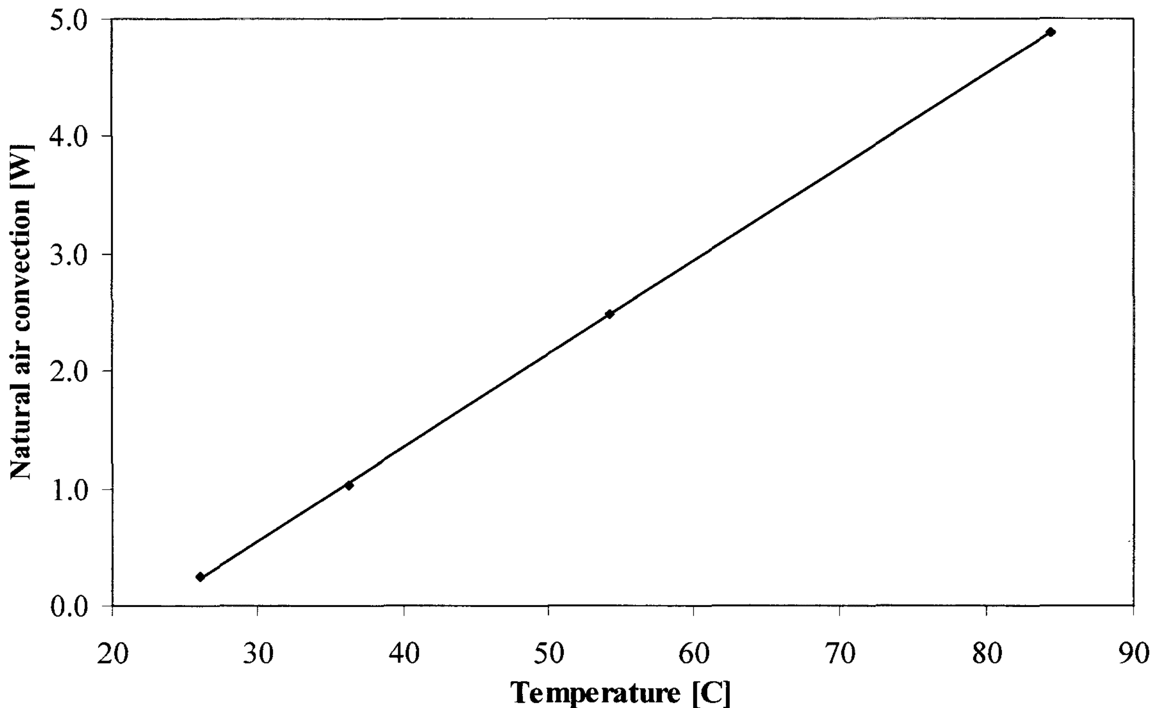


Figure 25. Natural air convection as a function of the mean heater temperature.

In conclusion, on chip cooling using forced water convection through micro-channels is an effective cooling method, especially compared to natural air convection.

Chapter 5

Discussion

The total thermal resistance of the integrated micro-channel cooler is the sum of three contributions, as already discussed in chapter 2.2.1:

1. *The thermal resistance due to conduction* can be calculated using equation 2.9. The thickness of the silicon diffuser layer is 300 μm, and in addition also diffusion occurs through the fins with a height of 300 μm. The average diffusion distance is approximately 450 μm (overestimation). A layer of SiO_2 with a thickness of 100 nm is present between the heater and the silicon, which also acts as a small thermal barrier. An upper limit for the thermal resistance due to conduction, R_{cond}, can then estimated to be 0.03 K/W. Making the silicon layer thinner can decrease R_{cond}, but when it becomes too thin, the device becomes fragile. Additionally decreasing the diffuser layer thickness can also increase the maximum junction temperature when the heat flux is not uniform. R_{cond} is a constant value, which only depends on the geometry of the device and the used materials, but not on the liquid and the flow rate.

2. *Convection resistance* corresponding to the heat exchange between the micro-channel walls and the liquid and can be calculated with use of equation 2.10. This term can be decreased by increasing the micro-channel surface or by making the flow turbulent, which increases the heat transfer coefficient for water convection. Turbulence generally only occurs at relatively high flow rates, which is not desirable. It is also possible to generate turbulence/mixing in micro-channels at low flow rates by adding a small amount of polymer to the water [5], or by making artificial disturbances in de sidewalls. This term depends among other things on the geometry of the device and on the flow characteristics (laminar or turbulent).

3. *Capacitive resistance* representing the increase of the water temperature between the inlet and outlet of the micro-channels, can be determined using equation 2.11 and 2.48:

$$R_{cap} = \frac{1}{\rho \dot{V} C_p} = \frac{\Delta T}{P}. \qquad (2.49)$$

This term can be calculated by measuring the inlet water temperature and outlet water temperature as a function of the dissipated power (Fig. 23). Increasing the flow can decrease this term. However, high flow rates are not desirable from a practical point of view. The minimum capacitive resistance is limited by maximum flow rate. The maximum flow rate depends among other things on the performance of the heat exchanger, which is needed to cool the water down to the desirable inlet water temperature.

The measured total thermal resistance shown in Fig. 20 is the sum of the three terms discussed above. The three contributions are shown in Fig. 26. The thermal resistance due to conduction is a constant value, which is estimated above. The capacitive thermal resistance is calculated with use of the measured inlet and outlet water temperature. The thermal resistance due to convection is the measured total thermal resistance minus the capacitive thermal resistance and the thermal resistance due to conduction. The onset of turbulence is clearly visible, however the convection resistance is not constant for laminar and turbulent flow. The heat transfer coefficient for water convection depends not only on the geometry of the device and the type of flow, but also on other properties as mentioned in 2.2.1.2.

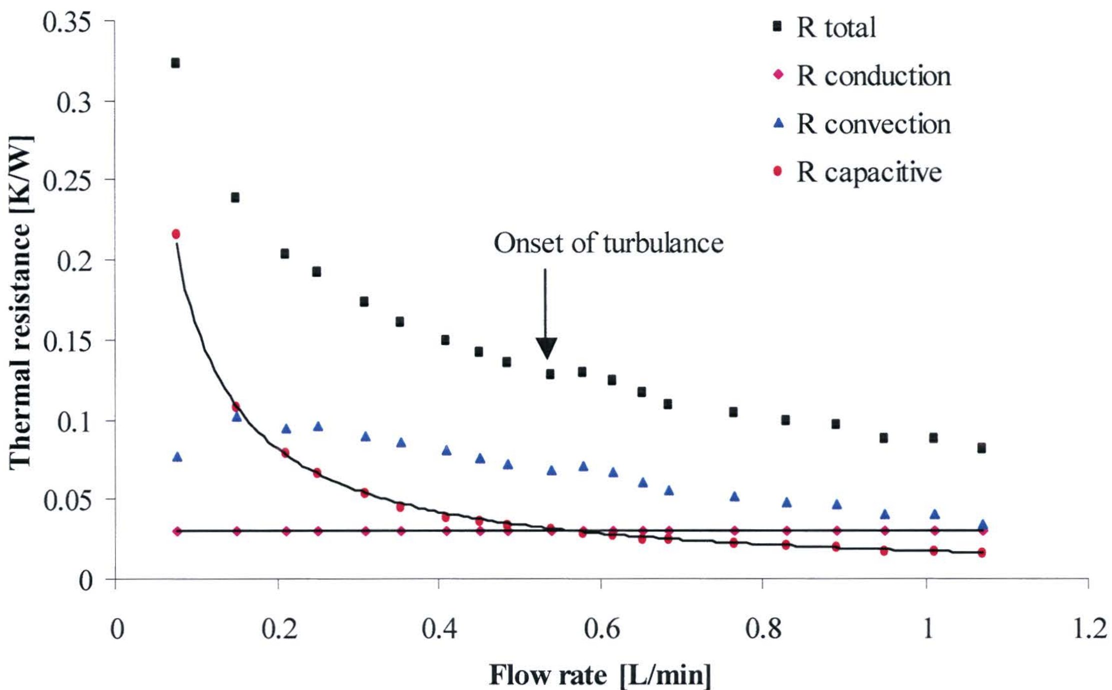


Figure 26. Thermal resistances as a function of the flow rate for a dissipated power of 100 W.

The most obvious way to improve the efficiency of the micro-channel cooling device is to decrease the convection resistance by increasing the heat exchange area ($A_{\mu\text{-}ch}$). The heat exchange area can be increased by decreasing the channel and/or fin width. However, by decreasing the channel a larger pressure drop is required to generate a certain flow rate. The maximum pressure drop and flow rate depend on the overall system configuration and package reliability. For a given maximum pressure drop and flow rate it is possible to optimise the channel width. There is also an optimal fin width. When the fins are too wide, $A_{\mu\text{-}ch}$ is not optimised, but when the fins are too narrow, the temperature drop over the fin height will result in a reduced effective heat exchange area ($A_{\mu\text{-}ch}$).

For a maximum pressure drop of 1 bar, and a maximum flow rate of 0.1 l/min the channel and fin widths are optimised using the analytical model. The optimised channel width is 36 μm with a fin width of 19 μm. The thermal resistance for this geometry is R_{th} = 0.16 K/W. The calculations also indicate that the channel and fin width are not very critical, At a channel and fin width of 50 μm, the thermal resistance is still 0.17 K/W for a pressure drop of 0.6 bar and a flow rate of 0.1 l/min

Note that the array of micro-channels has a total width of 1.5 cm and each channel has a length of 1.5 cm. However, the heater is only 1x1 cm^2, and consequently more than 50 % of the cooling area is not used. If the micro-channels would have the same size as the heater, the flow rate and the pressure drop can be reduced by 33 %. For a cooling device with the same size of the heater, the total thermal resistance for the optimised channel geometry for a pressure drop of 1 bar, and a maximum flow rate of 0.1 l/min, is reduced to R_{th} = 0.12 K/W. This value will decrease to R_{th} = 0.09 K/W if a pressure drop of 2 bar and a maximum flow rate of 0.2 l/min is allowed.

Increasing the fin height will also increase the heat exchange area ($A_{\mu\text{-}ch}$). This results in a thinner silicon diffuser if the thickness of the silicon wafer is constant. Consequently, R_{cond} and R_{conv} will decrease, and the pressure drop needed to generate a certain flow rate will also decrease, but the device becomes more fragile. There are good opportunities to decrease R_{th}, by increasing the fin height, since the device with a silicon diffuser thickness of 300 μm can handle a pressure drop in excess of 4 bar, as can be concluded from our experiments.

An other possibility to increase the heat exchange area ($A_{\mu\text{-}ch}$), is by choosing an other geometry than channels, for example an array of silicon spikes, or crosses. Figure 27 depicts a SEM-microphotograph of a silicon micro-heat-exchanger with an array of crosses. The heat exchange area is increased compared with micro-channels, but a higher pressure drop is needed to generate a certain flow rate when the density of crosses becomes too high. Depending on the design constrains, it must be possible to design an optimal structure. For example, when an high pressure and only a small flow rate is allowed, an optimal design could be a kind of porous material with a very high heat exchange area.

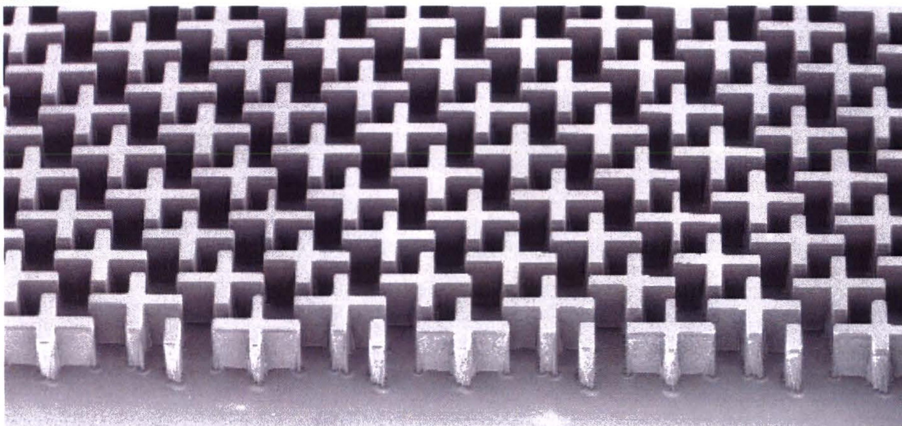


Figure 27: SEM-microphotograph of a silicon micro-heat-exchanger with an array of crosses.

Chapter 6

Conclusion

Integrated micro-channel cooling devices directly underneath the eletronic circuit for on-chip cooling with forced water convection have been studied. A peak dissipation of 428 W at a flow rate of 1.11 l/min resulted in a mean chip temperature of 55 °C, corresponding to a thermal resistance of 0.12 K/W. With a more practical flow rate of 0.1 l/min a peak dissipation of 300 W resulted in a temperature of 120 °C. This by far exceeds the desired cooling power required for the next generation CPUs.

The experimental results are compared to numerical calculations. For low flow rates there is a very good agreement. For higher rates, the flow is not fully developed and becomes turbulent, which results in an even better performance as predicted by the numerical calculations.

Several opportunities are available to improve the cooling performance:

1. The thermal resistance due to conduction can be decreased by decreasing the silicon diffuser layer. Nevertheless, this will make the device more fragile, and when the heat flux is not uniform the maximum junction temperature will increase.
2. The thermal resistance due to convection can be decreased by increasing the area available for heat exchange. The heat exchange area can be increased by decreasing the channel and fin width. However, this will result in a higher pressure drop needed to generate the same flow rate. Another possibility to increase the heat exchange area is by increasing the fin height. This results in a thinner silicon diffuser if the thickness of the silicon wafer is constant. Consequently, R_{cond} and R_{conv} will decrease, and the pressure drop needed to generate a certain flow rate will also decrease.
3. Another way to decrease the convection resistance is by generating turbulence at low flow rates. This can be done by adding a small amount of polymer to the water, or by making artificial disturbances in the sidewalls.
4. The capacitive resistance can be decreased by increasing the flow rate.

For these reasons, the optimal geometry depends on the maximum allowed pressure drop and flow rate, which depends on the design constrains. Further research is needed to optimise the geometry dependence on the design constrains. Not only micro-channels, but also other designs, like an array of crosses, are possible to reduce the total thermal resistance. These measures will result in a significant improved cooling performance.

Chapter 7

Reference

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[5] A. Groisman and V. Steinberg, "Efficient mixing at low Reynolds numbers using polymer additives," *Nature*, vol. 410, pp. 905-907, April 2001.

Chapter 8

Appendix A: Matlab program

```
% _______________________ Micro-channel geometry _______________________

    Wc = 0.00005;               % Half channel width [m]
    Hc = 0.0003;                % Channel height [m]
    L = 0.01;                   % Channel length [m]
    W = 0.000029;               % Half the distance between adjacent channels [m]
    H=0.0006;                   % Chip's height [m]
    Dh = 4*Wc*Hc/(2*Wc+Hc);     % Hydraulic diameter [m]
    A = Hc/(2*Wc);              % Aspect ratio A

% _______________________ Non dimensional parameters _______________________

    hc = 1;                     % Non dimensional wafer's thickness =Hc/Hc
    wc = Wc/Hc;                 % Non dimensional half channel width
    w = W/Hc;                   % Non dimensional half the distance between adjacent
                                % channels
    h = H/Hc                    % Non dimensional chip's height

% _______________________ Fluid properties _______________________

    nu = 0.001002;              % Fluid viscosity [N.s/m2]
    d = 998;                    % Fluid density [kg/m3]
    kf= 0.6;                    % Fluid thermal conductivity [W/(m.K)]
    Cp = 4181.9;                % Fluid specific heat [J/(kg*K)]

% _______________________ Solid properties _______________________

    ks = 150;                   % Silicon thermal conductivity [W/(m*K)]

% _______________________ Flow properties _______________________

    deltaP = 200000;            % Pressure drop [Pa]
    fprintf('pressure drop = %1.2f [bar]\n',deltaP/100000);
    Tin = 20;                   % Inlet temperature [C]

% _______________________ Heat flux _______________________

    Q = 4000000;                % Heat flux [W/m2]
    fprintf('heat flux = %6.2f [W/cm^2]\n',Q/10000);
    Qtot=2*Q*W*L;               % Total heat flow [W]
```

% Velocity profile calculation

% Calculation of the dimensional average velocity Umean

```
i = 1;
U(i) = tanh(pi/(2*A));
sU = U(i);
while (U(i)/sU) > 0.000000000001
        i = i+2;
        U(i) = tanh(i*pi/(2*A))/(i^5);
        sU = sU+U(i);
end
Umean = (Hc^2/(12*nu))*(deltaP/L)*(1-((192*A/pi^5)*sU));
fprintf('mean velocity = %1.2f [m/s]\n',Umean);
```

% Calculation of the flow rate [l/min]

```
Flow = Umean*Hc*2*Wc*1000*60*0.01/(2*W);
fprintf('flow = %1.3f [L/min]\n',Flow);
```

% Non-dimensional velocity profile u(x,y)

```
% Defining the calculation mesh:
p = wc/8;                                % Step of our calculation
x = 0:p:wc;
nx = length(x);
y = 0:p:hc;
ny = length(y);


% Calculation of the first term of the sum
su1x(1:nx) = 1-cosh(pi*x)/cosh(pi*wc);
for j = 1:nx
        for i = 1:ny
                su1(j,i) = su1x(j).*cos(pi*(y(i)-0.5));
        end
end
u1(1:nx,1:ny) = su1(1:nx,1:ny);

% Calculation of the other terms until accuracy=1e-4%
j = 1;
r(1:(nx-2),1:(ny-2)) = abs(su1(2:(nx-1),2:(ny-1))./u1(2:(nx-1),2:(ny-1)));
                                         % From 2 to nx-1 because of the division by 0
r2 = max(r(1:(nx-2),1:(ny-2)));
r3 = transpose(r2);
cont = max(r3);
while cont > 0.00001
        j=j+2;
        su1x(1:nx) = (-1)^((j-1)/2)*(1-cosh(j*pi*x(1:nx))/cosh(j*pi*wc));
        for i = 1:ny
                su1(:,i) = su1x(:).*cos(j*pi*(y(i)-0.5))/j^3;
        end

        u1(1:nx,1:ny) = u1(1:nx,1:ny)+su1(1:nx,1:ny);
        r(1:(nx-2),1:(ny-2)) = abs(su1(2:(nx-1),2:(ny-1))./u1(2:(nx-1),2:(ny-1)));
```

```
        r2 = max(r);
        r3 = transpose(r2);
        cont = max(r3);
end

% Calculation of the sum u(2)
su2 = tanh(pi*wc);
u2 = su2;
j = 1;
while (su2/u2) > 0.00001
        j = j+2;
        su2 = tanh(j*pi*wc)/j^5;
        u2 = u2+su2;
end

% Final calculation of u(x,y), the mean velocity, the maximum velocity, the mean Reynolds
% number and the maximum Reynolds number. Followed by the velocity profile plot.
u(1:nx,1:ny)=(48/pi^3.*u1(1:nx,1:ny)/(1-96/(pi^5*wc)*u2));
velocity(1:nx,1:ny)=u(1:nx,1:ny)*Umean;
m=mean(velocity);
m=mean(transpose(m));
Mean=m;
fprintf('mean velocity = %1.2f [m/s]\n',Mean);
Re=Dh*Mean*d/nu;
fprintf('Re = %4.2f \n',Re);
Max=max(velocity);
Max=max(transpose(Max));
fprintf('maximum velocity = %1.2f [m/s]\n',Max);
ReMax=Dh*Max*d/nu;
fprintf('ReMax = %4.2f \n',ReMax);
I=ones(ny,1);
X=Hc*I*x*1e6;
I=ones(nx,1);
Y=Hc*I*y*1e6;
figure(1);
surf(transpose(X),Y,velocity);
axis([0 W*1e6 0 H*1e6 0 Max]);
shading interp;
title('Velocity profile');
xlabel('\mum');
ylabel('\mum');
zlabel('velocity [m/s]');
grid on;
```

% Axial conduction

```
% ConductionRatio is Qc/Q
ConductionRatio =ks/(L*d*Cp*Umean)*(((W*H)/(Wc*Hc))-1);
fprintf('Conduction Ratio = %1.4f \n',ConductionRatio);
```

% **Poisson equation**

```
%Defining the calculation mesh:
xs = 0:p:w;
nxs = length(xs);
ys = 0:p:h;
nys = length(ys);
```

% Finite differences method

```
m = nys*nxs;
S = zeros(m,1);                     % 2nd term of the equation
A = zeros(m,m);                     % Equations system
```

% PDE in the liquid

```
% equations system
for i = 2:(nx-1)
        for j = 2:(ny-1)
                k = (i-1)*nys+j;
                A(k,k-nys) = 1;
                A(k,k-1) = 1;
                A(k,k) = -4;
                A(k,k+1) = 1;
                A(k,k+nys) = 1;
                S(k) = u(i,j)*p^2/wc;       % Second term
        end
end

% Boundary condition for y = 0, dtheta/dy = 0
for i = 1:(nxs-1)
        k = (i-1)*nys+1;
        A(k,k) = 1;
        A(k,k+1) = -1;                      % (second term=0)
end

% Boundary condition for x = 0, dt/dx = 0
for k = 2:nys
        A(k,k) = 1;
        A(k,k+nys) = -1;                    % (second term=0)
end
```

% PDE in the solid

```
% Equations system (x>wc)
for i = (nx+1):(nxs-1)
        for j = 2:(nys-1)
                k = (i-1)*nys+j;
                A(k,k-nys) = 1;
                A(k,k-1) = 1;
                A(k,k) = -4;
                A(k,k+1) = 1;
```

```
                A(k,k+nys) = 1;          % (second term=0)
        end
end

% Equations system (y>hc)
for i = 2:nx
        for j = (ny+1):(nys-1)
                k = (i-1)*nys+j;
                A(k,k-nys) = 1;
                A(k,k-1) = 1;
                A(k,k) = -4;
                A(k,k+1) = 1;
                 A(k,k+nys) = 1;         % (second term=0)
        end
end

% Boundary condition for y = h, dtheta/dy = kf/(ks*w)
for i = 2:nxs
        k = (i-1)*nys+nys;
        A(k,k) = 1;
        A(k,k-1) = -1;
        S(k) = kf*p/(ks*w);              % Second term
end

% Boundary condition for x = w, dt/dx = 0
for l = 1:nys-1
        k = (nxs-1)*nys+l;
        A(k,k) = 1;
        A(k,k-nys) = -1;                 % (second term=0)
end
```

% Solid/Liquid interface

```
% for x = wc, (ks/kf)*(dt/dx)sol = (dt/dx)fl
for i = 2:ny-1
        k = (nx-1)*nys+i;
        A(k,k) = 1+ks/kf;
        A(k,k-nys) = -1;
        A(k,k+nys) = -ks/kf;             % (second term=0)
end


% for y = hc = 1, (ks/kf)*(dt/dy)sol = (dt/dy)fl
for i = 2:nx
        k = (i-1)*nys+ny;
        A(k,k) = 1+kf/ks;
        A(k,k-1) = -1;
        A(k,k+1) = -ks/kf;               % (second term=0)
end

A1=sparse(A);
```

```
%                              Solve the Poisson Equation

    T = A1\S;
    Theta = zeros(nxs,nys);
    for k = 1:m
            i = floor((k-1)/nys)+1;
            l = k-(i-1)*nys;
            Theta(i,l) = T(k);
    end
```

% Computation of θ_c

```
    for i = 1:nx
            for j = 1:ny
                    ut(i,j) = Theta(i,j)*u(i,j);   % ut = u*theta
            end
    end

    for i = 1:nx-1
            for j = 1:ny-1
                    uti(i,j) = (ut(i,j)+ut(i+1,j)+ut(i+1,j+1)+ut(i,j+1))/4;
            end
    end

    utix = sum(uti);
    tuti = transpose(utix);
    Thetac = sum(tuti)*p^2/wc;                  % Computation of thetaC

%                    Computation of deltaT=T(x,y)-Tb

    DeltaT = zeros(nxs,nys);
    DeltaT(1:nxs,1:nys) = W*Q/kf*(Theta(1:nxs,1:nys)-Thetac);

%               Computation of Tb(z) = fluid bulk temperature

    % Computation of dTb/dz
    dTb = Q*W/(d*Cp*Umean*Wc*Hc);

    % Computation of Tb(z)
    pz = L/20;
    z = 0:pz:L;
    nz = length(z);
    for i = 1:nz
            Tb(i) = dTb*z(i)+Tin;
    end

%         Calculation and plot of the inlet temperature profile T(x,y)

    Temp(1:nxs,1:nys) = Tb(1)+DeltaT(1:nxs,1:nys);
    I = ones(nys,1);
    Xs = Hc*I*xs*1e6;
```

```
I = ones(nxs,1);
Ys = Hc*I*ys*1e6;
figure(2);
surf(transpose(Xs),Ys,Temp);
shading interp;
title('Inlet temperature profile');
xlabel('\mum');
ylabel('\mum');
zlabel('Temperature [C]')
grid on;
```

% Calculation and plot of the outlet temperature profile T(x,y)

```
Temp(1:nxs,1:nys) = Tb(nz)+DeltaT(1:nxs,1:nys);
I = ones(nys,1);
Xs = Hc*I*xs*1e6;
I = ones(nxs,1);
Ys = Hc*I*ys*1e6;
figure(3);
surf(transpose(Xs),Ys,Temp);
shading interp;
title('Outlet temperature profile');
xlabel('\mum');
ylabel('\mum');
zlabel('Temperature [C]')
grid on;

MaxTemp=max(transpose(max(Temp)));
fprintf('Maximum Temperature = %3.3f [C]\n',MaxTemp);
```

% Computation and plot of the local Nusselt numbers

```
% Interface x = wc, Nu = (1/Theta)*dtheta/dx
for i = 1:ny
        dThetax = (Theta(nx,i)-Theta(nx-1,i))/p;
        Nux(i) = (1/(Theta(nx,i)-Thetac))*dThetax;
end
m = max(Nux);
NormNux = Nux/m;
xx = y*Hc*1e6;
xxx = 0:1:Hc*1e6;
yyy = spline(xx,NormNux,xxx);
figure(4);
plot(xx,NormNux,'o',xxx,yyy);
axis([0 H*1e6 0 1]);
title('Normalized Nussel Number on the interfase x=Wc');
xlabel('\mum');
ylabel('Normalized Nu');
grid on;

% Interface y = hc, Nu = (1/Theta)*dtheta/dy
for i = 1:nx
        dThetay = (Theta(i,ny)-Theta(i,ny-1))/p;
        Nuy(i) = (1/(Theta(i,ny)-Thetac))*dThetay;
end
```

```
NormNuy = Nuy/m;
xx = x*Hc*1e6;
xxx = 0:1:Wc*1e6;
yyy = spline(xx,NormNuy,xxx);
figure(5);
plot(xx,NormNuy,'o',xxx,yyy);
axis([0 W*1e6 0 1]);
title('Normalized Nussel Number on the interfase y=Hc');
xlabel('\mum');
ylabel('Normalized Nu');
grid on;
```

```
%                    Computation of the thermal resistance
```

```
% computation on Tj_in
for i = 1:nxs
        Tj_in(i,1) = (W*Q/kf*(Theta(i,nys)-Thetac))+Tb(1);
end
meanTj_in = mean(Tj_in);

% computation of Tj
for i = 1:nxs
        for j = 1:nz
                Tj(i,j) = (W*Q/kf*(Theta(i,nys)-Thetac))+Tb(j);
        end
end
meanTj = mean(transpose(mean(Tj)));      % Mean junction temperature [°C]
R = (meanTj-Tin)/(Qtot);                 % Overall thermal resistance [K/W]
Rc = 10000*(meanTj-Tin)/Q;               % Overall thermal resistance [K.cm2/W]
fprintf('Thermal Resistance = %1.4f [K*cm^2/W]\n',Rc);
```

Chapter 9

Appendix B: Publication

Integrated micro-channel cooling in silicon

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Abstract

Integrated micro-channel cooling directly underneath an electronic circuit for on-chip cooling with forced water convection has been investigated both theoretically and experimentally. In a 1-cm^2 experimental device 370 W was dissipated without exceeding the critical junction temperature of 120 °C at a flow rate of only 0.1 l/min and a pressure drop of 0.15 bar. The minimum thermal resistance, which is measured, is 0.08 K/W for a power dissipation of 428 W at a flow rate of 1.1 l/min. This more than satisfies the requirements for cooling of next generation CPUs.

Introduction

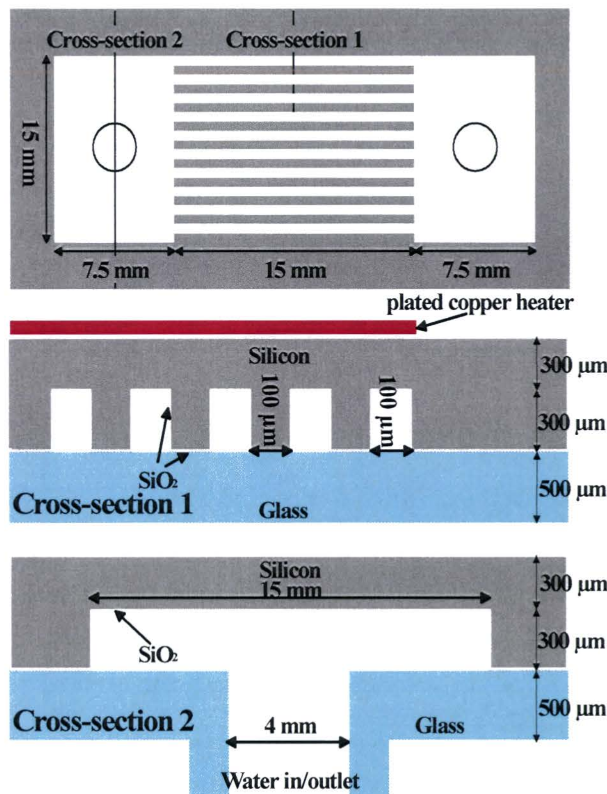

Figure 1: The geometry of the micro-channels in the backside of a silicon wafer. The final device has a total number of 75 channels.

As integrated circuits (ICs) become faster and more densely packed, the power density increases and the heat generated as a by-product becomes a serious problem. In order to ensure optimal performance and lifetime, new solutions for enhanced cooling of components will be required.

A very promising solution is an integrated micro-cooling device directly underneath the electronic circuit, to transport the heat from the circuit to other places. In this way the area available for heat removal can be increased and hot spots in the IC can be prevented.

An efficient way to integrate a micro-cooling device underneath the electronic circuit is by deep Reactive Ion Etching of micro-channels in the backside of the silicon chip. Water flowing through the micro-channels is used to transport the heat away from the silicon IC. By integrating the cooling device in the chip itself, intermediate layers, which act as thermal barriers, are eliminated.

In this paper we present the study of forced convection of demi-water through micro-channels etched in the backside of the IC. The fabrication of silicon microchannels will be reviewed. Next, we will discuss the experimental results and compare them with numerical simulations.

Device design and fabrication

The integrated micro-channel device is made by etching rectangular shaped channels in the backside of a silicon wafer underneath the heat generating circuit. By using the Bosch process [1], channels with arbitrary depth and near perfect vertical sidewalls are obtained. After etching and stripping of resist, a thin layer of SiO_2 (100 nm) is grown by thermal oxidation to make the surface hydrophilic. To simulate the power generated by an electric circuit or CPU, a 10 μm thick meander-shaped copper heater is electro-plated on the front side of the wafer. The size of the heater is 1x1 cm^2. The channels are covered with a glass plate, which is glued to the silicon using a UV curing adhesive. Connection tubes for the liquid are glued on top of the glass plate. A schematic top view and two cross-sections are shown in Fig. 1.

The complete experimental set-up consists of a closed hydraulic circuit composed of a mechanical pump, a flow meter, a manometer, a 0.4 μm filter, thermocouples and a heat exchanger located in a thermal bath in order to have a constant inlet water temperature. Figure 2 shows the device connected in the experimental set-up and Fig. 3 depicts a SEM microphotograph of the micro-channels.

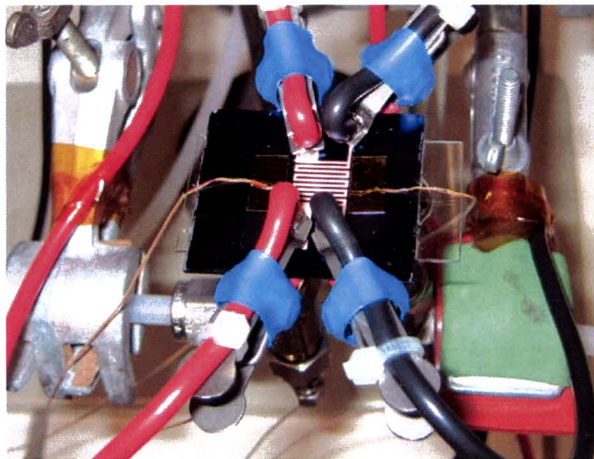

Figure 2: Cooling device connected in the set-up. Clearly visible are the copper heater and the electrical connections.

Experimental results and simulations

Several experiments with different flow rates and with different heat dissipations have been carried out and compared with numerical simulations. The simulations were done using the commercial software package Flotherm [2], as well as by solving numerically a conjugate heat transfer problem consisting of the simultaneous determination of the temperature fields in both the solid substrate and in the water (analytical model) [3]. The performance of the device is measured by its total thermal resistance (R_{th}), which is defined as:

$$R_{th} = \frac{T_h - T_{in}}{P}, \tag{1}$$

where T_h the mean heater temperature, T_{in} the inlet water temperature and P the dissipated power. The mean heater temperature is determined by a four-point measurement of the resistance of the heater.

The thermal resistance depends on the flow rate through the micro-channels. The thermal resistance, both measured and simulated, as a function of the flow rate with $P = 100$ W is shown in Fig. 4.

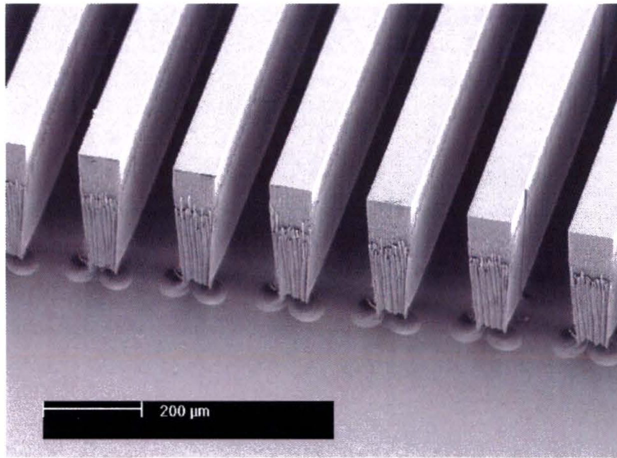

Figure 3: SEM microphotograph of the micro-channels, with a channel and fin width of 100 µm and a depth of 300 µm.

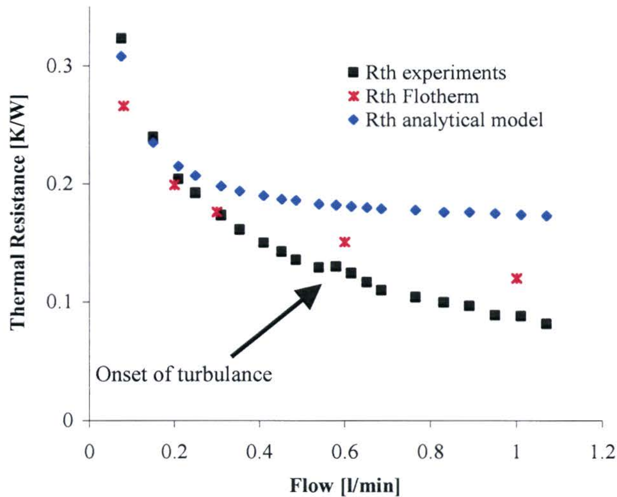

Figure 4: The experimental and simulated thermal resistance as a function of the flow rate for a dissipated power of 100 W.

As can be seen from Fig. 4, the measured thermal resistance for flows in excess of 0.2 l/min is lower than the thermal resistance calculated using the analytical model (by a factor of 2 for flows around 1 l/min). This can be explained from the fact that the analytical model assumes a fully developed flow (both hydraulically and thermally) at the entrance of the micro-channels. However, this is not the case, in particular not for high flow rates, resulting in a lower thermal resistance then expected according to the analytical model. The simulations using Flotherm are in better agreement with the experimental results, because Flotherm does not make this assumption.

Figure 4 also shows that the calculations predict a more or less constant thermal resistance for flow rates above 0.6 l/min. However, the experiments show that the thermal resistance continues to decrease for increasing flow. This is because the simulations assume a laminar flow, while in fact the flow becomes turbulent for flow rates in excess of 0.6 l/min. This can also be seen in Fig. 5.

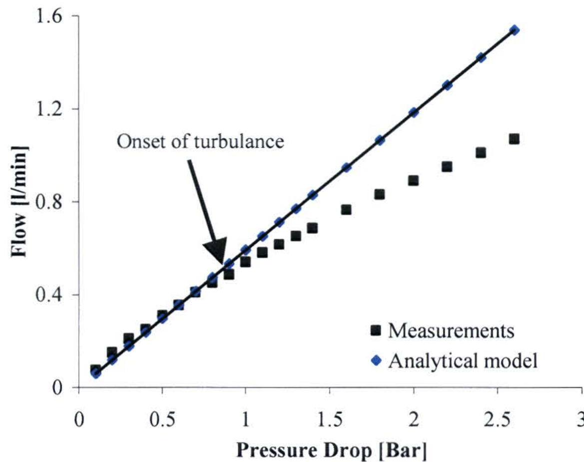

Figure 5: Flow rate as a function of the pressure drop over the micro-channels.

The transition between laminar and turbulent flow for micro-channels occurs for Reynolds numbers (Re) ≈ 200-700 [4]. The Reynolds number corresponding to a flow rate of 0.6 l/min for our device is Re = 630, so this is in agreement with literature. Turbulence in the micro-channels is desirable because it increases the heat transfer coefficient for water convection. The disadvantage of turbulence is that a higher pressure drop is needed to generate the same flow rate.

High flow rates require relatively large reservoirs and pressures, which is not practical for the cooling of electronics. For this reason, the focus of the next part will be on modest flow rates of ~ 0.1 l/min. In this range, the flow in the micro-channels will be fully developed already at a very short distance from the channel entrance (ca. 1 mm) [3,5]. Under this condition the analytical model gives a good approximation of the thermal resistance. Figure 6 shows the measured thermal resistance as a function of dissipated power, at a constant pressure drop of 0.15 bar over the device. For this pressure drop a flow rate of 0.089 l/min and a thermal resistance of $R_{th} = 0.29$ K/W is predicted by the analytical model. Nevertheless in reality, the flow rate also depends on the dissipated power, since the water viscosity varies with temperature. The measured flow rate for example at a constant $\Delta p \approx 0.15$ bar at 50 W is 0.084 l/min, and increases to 0.108 l/min at 370 W. Taking the temperature dependence of viscosity into account, one can calculate the thermal resistance as a function of dissipated power using the analytical model (Fig. 6). There is a small difference between the calculated thermal resistance using the analytical model and the measured thermal resistance for power dissipation below the 100 W. This can be explained by the fact that the heater used during the measurements is not uniform. The heat transport from the heater to the water is so fast that at low power densities the heat does not have the time to spread uniformly. This results in a smaller effective area used for heat exchange and consequently in a higher thermal resistance. For power densities above 100 W/cm^2 the heater operates uniformly.

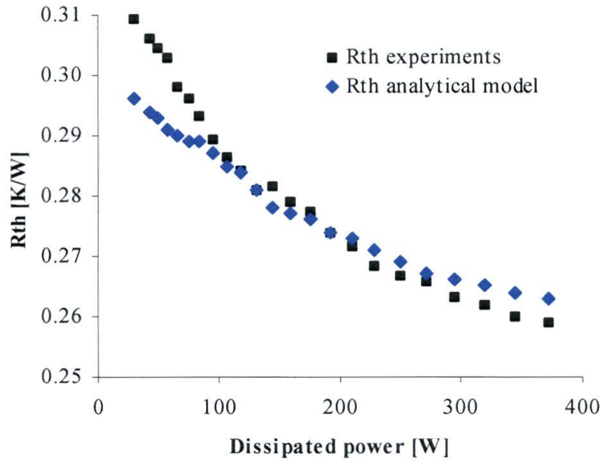

Figure 6: Thermal resistance as a function of the dissipated power, at a constant pressure drop $\Delta p \approx 0.15$ bar.

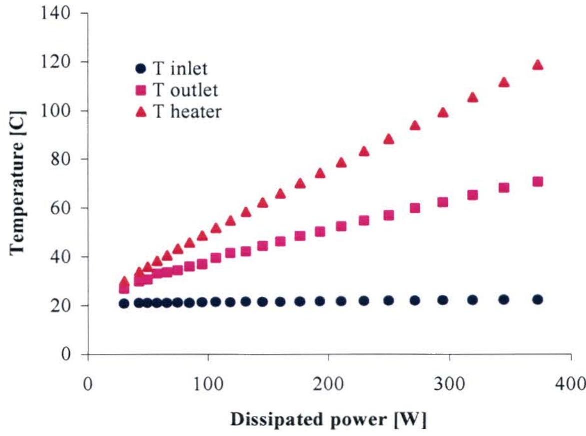

Figure 7: The inlet, outlet and heater temperature as a function of the dissipated power at a constant pressure drop $\Delta p \approx 0.15$ bar.

Figure 7 shows the heater temperature, the inlet water temperature and the outlet water temperature as a function of the dissipated power at $\Delta p \approx 0.15$ bar over the micro-channels (same measurement as shown in Fig. 6).

The maximum junction temperature under normal operation conditions in an IC is limited to 120 °C. This means that at a flow of 0.1 l/min, the maximum cooling capacity of this micro-channel design is in excess of 350 W. Using a flow rate of 1.1 l/min a peak dissipation of 428 W is reached with a heater temperature of 55 °C, which corresponds to a thermal resistance of 0.08 K/W.

The error caused by the natural air convection during these measurements is small. The amount of transported heat by the water can be calculated from:

$$P = \rho \dot{V} C_p \Delta T , \tag{2}$$

with ρ the water density, $\dot{V}$ the volumetric flow rate, C_p the specific heat of water and ΔT the water temperature difference between the inlet and outlet (Fig. 7). For example, at a power dissipation of 370 W, the power transport by the water is approximately 365 W. The remaining 5 W is transported by natural air convection. This is less than 2 % of the total dissipated power. In conclusion, on-chip cooling using forced

water convection through micro-channels is an effective cooling method, especially compared to natural air convection.

Discussion

The total thermal resistance of the device is the sum of three contributions:
1) *Resistance due to conduction* through the silicon R_{cond}:

$$R_{cond} = \frac{d}{kA}, \tag{3}$$

where d the thickness of the silicon layer, k the thermal conductivity of silicon and A the device area. Making the silicon layer thinner can decrease R_{cond}, but when it becomes too thin, the device becomes fragile.
2) *Convection resistance* corresponding to the heat exchange between the micro-channel walls and the water:

$$R_{conv} = \frac{1}{hA_{\mu-ch}}, \tag{4}$$

with h the heat transfer coefficient for water convection and $A_{\mu\text{-ch}}$ the area of the micro-channel walls. This term can be decreased by increasing the micro-channel surface or by making the flow turbulent, which increases the heat transfer coefficient for water convection. Turbulence generally only occurs at relatively high flow rates, which is not desirable. It is also possible to generate turbulence in micro-channels at low flow rates by adding a small amount of polymer to the water [6], or by making artificial disturbances in the sidewalls.
3) *Capacitive resistance* representing the increase of the water temperature between the inlet and outlet of the micro-channel:

$$R_{cap} = \frac{1}{\rho \dot{V} C_p}. \tag{5}$$

Increasing the flow can decrease this term. However, high flow rates are not desirable from a practical point of view. Therefore, the most obvious way to improve the efficiency of the micro-channel cooling device is to increase the heat exchange area ($A_{\mu\text{-ch}}$) by decreasing the channel and/or the fin width. However, by decreasing the channel size a larger pressure drop is required to generate a certain flow rate. The maximum flow rate depends on the reservoir size, and the maximum pressure drop depends on the pump and package reliability. When the maximum flow rate and pressure drop are known, it is possible to optimise the channel width. There is also an optimal fin width. When the fins are too wide, $A_{\mu\text{-ch}}$ is not optimised, but when the fins are too narrow, the temperature drop over the fin height will result in a reduced effective heat exchange area ($A_{\mu\text{-ch}}$).

For a maximum pressure drop of 1 bar, and a maximum flow rate of 0.1 l/min the channel and fin widths are optimised using the analytical model. The optimised channel width is 36 μm with a fin width of 29 μm. The thermal resistance for this geometry is R_{th} = 0.16 K/W. The calculations also indicate that the channel and fin width are not very critical. At a channel and fin width of 50 μm, the thermal resistance is still 0.17 K/W for a pressure drop of 0.6 bar and a flow rate of 0.1 l/min.

Note that the array of micro-channels has a total width of 1.5 cm and each channel has a length of 1.5 cm. However, the heater is only 1x1 cm^2, and consequently, more than 50 % of the area is not used. If the micro-channels would have the same size as the heater, the flow rate and the pressure drop can be reduced by 33 %.

Conclusion

Integrated micro-channel cooling devices directly underneath the electronic circuit for on-chip cooling with forced water convection have been studied. A peak dissipation of 428 W at a flow rate of 1.11 l/min resulted in a chip temperature of 55 °C, corresponding to a thermal resistance of 0.12 K/W. With a more

practical flow rate of 0.1 l/min a peak dissipation in excess of 350 W resulted in a temperature of 118 °C. This by far exceeds the desired cooling power required for next generation CPUs.
The experimental results are compared to numerical simulations and calculations. For low flow rates there is very good agreement. For higher rates the flow is not fully developed and becomes turbulent, which results in even better performance than predicted by the numerical calculations.

The calculations also show that the device can be further optimised. The performance can be improved by making the channels and fins smaller. The flow rate and pressure drop can be reduced by making the cooling device as large as the heater. The thermal resistance at low flow rates can also be reduced when it is possible to generate turbulence at these flow rates. This may be done by adding a small amount of polymer to the water, or by making artificial disturbances in the sidewalls. These measures will result in a significantly improved cooling performance.

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