Design of a sigma-delta modulator for optical detector applications

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ABSTRACT

This work deals with the design of an analogue-to-digital converter for optical detector applications, which is based on a sigma-delta modulator. To reduce chip area and to improve linearity, the output current of a position-sensitive photodetector is directly offered to the sigma-delta modulator. This implementation requires continuous-time discrete-time mixed-mode circuitry. The designed third-order sigma-delta modulator converts its analogue input current to a single-bit digital signal. The system achieves a resolution of 14bit, for a stable input current range of ±90nA, giving a total input reduced noise current spectral density of $0.16\text{pA}/\sqrt{\text{Hz}}$ at 1kHz. This is equivalent to an input reduced noise current spectral density, of a transimpedance amplifier with a 650kΩ feedback resistor. The output signal of the position-sensitive detector is AM modulated, in order to limit DC offsets due to environmental light. The carrier frequency is 1kHz and the modulating signal has a bandwidth of 200Hz, so the signal band of interest reaches from 0.8kHz to 1.2kHz. The sampling frequency is 256kHz.

Keywords: analogue-to-digital converters, current input, optical receivers, position-sensitive detectors, sigma-delta modulation

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LIST OF SYMBOLS AND ABBRIVIATIONS

$a_{1,2,...}$	Integrator gain factor	1
A_{in}	Amplitude sigma-delta modulator input signal	V
A_{th}	Sigma-delta modulator threshold	V
A_0	Operational amplifier DC gain	1
$A(s)$	Operational amplifier gain in the s-domain	1
ADC	Analogue-to-digital converter	
AM	Amplitude modulation	
$b_{1,2,...}$	Feedback gain factor	1
B	Number of quantiser output bits	bit
BW_n	Noise bandwidth	Hz
$C_{1,2,...}$	Capacitor	F
C_c	Comparator input capacitance	F
C_d	Position-sensitive photodetector capacitance	F
C_g	Operational amplifier input capacitance	F
C_l	Equivalent load capacitance	F
C_n	Node capacitance	F
C_{ox}	Oxide capacitance per unit area	F/m^2
CMOS	Complementary MOS	
D	Oversampling ratio	1
DAC	Digital-to-analogue converter	
DC	Direct current	
e_Q	Quantisation error	V
$e[n]$	Discrete-time quantisation error signal	V
$\overline{e^2}$	Quantisation noise power	V^2
$\overline{e_o^2}$	Ditto in the base band after oversampling	V^2
$\overline{e_{on}^2}$	Ditto in the base band after noise-shaping	V^2
$E(z)$	Quantisation error signal in the z-domain	
$E_o(f)$	Noise spectral density after oversampling	$V/\sqrt{Hz}$
$E_{on}(f)$	Ditto after noise-shaping	$V/\sqrt{Hz}$
$E^2(f)$	Quantisation noise power spectral density	V^2/Hz
$E_o^2(f)$	Ditto after oversampling	V^2/Hz
$E_{on}^2(f)$	Ditto after noise-shaping	V^2/Hz
f	Frequency	Hz
f_b	Highest signal frequency	Hz
f_c	AM carrier frequency	Hz
f_m	Modulating frequency	Hz
f_{nyq}	Nyquist frequency	Hz
f_s	Sampling frequency	Hz
g_m	Transconductance MOS transistor	A/V
g_{mb}	Bulk transconductance MOS transistor	A/V
GBW	Gain bandwidth product	Hz
$h_I[n]$	Discrete-time impulse response	1
$H_I(z)$	Transfer function in the z-domain	1
hd	Harmonic distortion component	V
$i_{d,max}$	Maximum sigma-delta modulator input current	A

$i_{d,q/2}$	Reference current value	A
i_n	Noise current	A
i_n^2	Noise current power	A^2
$i_d(t)$	Continuous-time input current sigma-delta modulator	A
$i_d[n]$	Ditto discrete-time	A
$i_{d,sin}[n]$	Ditto sinusoidal	A
$I_d(s)$	Ditto in the s-domain	
$I_d(z)$	Ditto in the z-domain	
I_{bias}	Bias current	A
I_{DS}	Drain-source current nMOS transistor	A
I_{SD}	Source-drain current pMOS transistor	A
Im	Imaginary	
k	Index	
k_b	Boltzmann factor= 1.38×10^{-23}	J/K
K'	Constant for a MOS transistor in saturation	A/V^2
KF_F	$1/f$ noise technology parameter	C^2/m^2
l	Index	
L	Order of the sigma-delta modulator	
	Gate length in MOS transistor calculations	m
M	MOS transistor	
MOS	Metal-oxide-semiconductor	
n	Discrete-time index	
N	Resolution of the sigma-delta modulator	bit
nMOS	n-channel MOS	
P_{diss}	Power dissipation	W
PM	Phase margin	°
pMOS	p-channel MOS	
q	Quantiser step	V
Q_{in}	Quantiser input signal	V
Q_{out}	Quantiser output signal	V
R_o	Operational amplifier output resistance	Ohm
$R(t,t+\tau)$	Auto-correlation function	V^2
Re	Real	
s	Complex frequency for continuous-time signals	
$S(f)$	Spectral density	$A/\sqrt{Hz}$ or $V/\sqrt{Hz}$
$S^2(f)$	Power spectral density	A^2/Hz or V^2/Hz
$S_n(f)$	Noise spectral density	$A/\sqrt{Hz}$ or $V/\sqrt{Hz}$
$S_n^2(f)$	Noise power spectral density	A^2/Hz or V^2/Hz
SNR	Signal-to-noise ratio	dB
$SP_{hd}R$	Signal-to-harmonic distortion ratio	dB
SR	Slew rate	V/s
t	Time	s
T	Unit-delay	s
T_{emp}	Temperature	K
T_s	Sampling period	s
T_ϕ	On-time clock phase	s
v_n	Noise	V
v_n^2	Noise power	V^2

$v_i[n]$	Discrete-time integrator input voltage	V
$V_i(z)$	Ditto in the z-domain	
$v_o[n]$	Discrete-time integrator output voltage	V
$V_o(s)$	Ditto in the s-domain	
$V_o(z)$	Ditto in the z-domain	
$v_{q/2}[n]$	Discrete-time quantiser output voltage	V
$V_{q/2}(z)$	Ditto in the z-domain	
V_{CM}	Common-mode voltage	V
V_{DD}	Highest supply voltage	V
$V_{DS,sat}$	Saturation voltage nMOS transistor	V
$V_{SD,sat}$	Saturation voltage pMOS transistor	V
V_{SS}	Lowest supply voltage	V
V_{GS}	Gate-source voltage nMOS transistor	V
V_{SG}	Source-gate voltage pMOS transistor	V
V_{Q_H}	Highest quantiser level	V
V_{Q_L}	Lowest quantiser level	V
V_T	MOS transistor threshold voltage	V
$w[n]$	Discrete-time integrator output signal	V
W	MOS transistor gate width	m
$x(t)$	Continuous-time sigma-delta modulator input signal	V
$x[n]$	Ditto discrete-time	V
$X(z)$	Ditto in the z-domain	
$y[n]$	Discrete-time sigma-delta modulator output signal	V
$Y(z)$	Ditto in the z-domain	
z	Complex frequency for discrete-time signals	
α	Multiplication factor due to a circuit limitation	1
α_1	Coefficient	
β_1	Coefficient	
γ	White noise constant	V^2/Hz
δ	Relative resolution of the comparator	1
Δ	Difference	
ε	Error due to a circuit limitation	1
ϕ	Clock phase	
θ	Relative angle-frequency	1
κ	Threshold multiplication factor	1
λ	Non-linear quantiser gain	1
λ_{min}	Minimum non-linear quantiser gain	1
μ_0	Carrier mobility	m^2/Vs
π	Angular constant	
σ	Relative stable input range	1
$\sigma()$	Standard deviation	
$\sigma^2()$	Variance	
Σ	Summation	
τ	Time constant	s
Θ	Phase uncertainty	rad
ζ	$1/f$ noise constant	V^2

PREFACE

Design of a sigma-delta modulator for optical detector applications, master thesis by ing. A.G. Mulders. This thesis is to obtain a degree in electrical engineering, from the Department of Electrical Engineering of the Eindhoven University of Technology in The Netherlands. The work was carried out at the Electronics Laboratory of the University of Oulu in Finland, from October 1996 till June 1997, in the scope of the ERASMUS exchange programme.

The aim of this work is to design an analogue-to-digital converter for optical detector applications, which is based on a sigma-delta modulator. The application is shortly introduced in chapter 1. Besides the design itself, the secondary aim is that the Electronics Laboratory of the University of Oulu becomes acquainted with sigma-delta modulation. Therefore the basic sigma-delta modulation theory is extensively discussed in chapter 2. In chapter 3 the actual design begins by selecting a suitable topology, which is translated into a simplified circuit. The specific limitations of this circuit are analysed in chapter 4. Chapter 5 deals with the design of the actual circuit. In chapter 6 the circuit is evaluated with a combination of calculations, high-level simulations and circuit simulations. For the specific digital post-processing, a proposal is given in chapter 7. Finally the design is discussed in chapter 8.

Oulu, June 1997

Addy Mulders

1. INTRODUCTION

At the Electronics Laboratory of the University of Oulu, high-accuracy CMOS position-sensitive photodetectors are being developed [1][2][3]. Some possible applications are displacement measurements and target practice. In Fig. 1 the general configuration of a (simplified) position-sensitive photodetector in a system is shown.

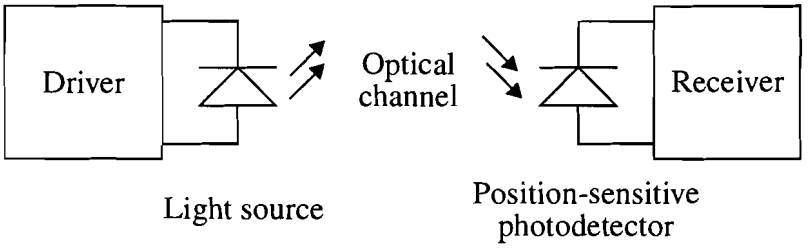

Figure 1. General configuration of a position-sensitive photodetector.

The driver modulates a carrier signal with the signal of interest, by means of AM modulation, to limit DC offsets. These are mainly caused by environmental light falling on the position-sensitive detector, because the optical channel is usually open air. The receiver converts the output signal of the position-sensitive detector to a signal that can be processed and recovers the band of interest by AM demodulation. Highly linear analogue or digital signal processing circuitry, that offers a high resolution is required for the receiver.

In this work a digital variant for the receiver is presented. The analogue output signal of the position-sensitive detector is on-chip converted to a digital signal, in order to avoid signal degradation due to long signal paths and extra processing circuitry. An analogue-to-digital converter, which can convert a very small current with high resolution and high linearity is required. Analogue-to-digital converters based on sigma-delta modulators offer these advantages. Relatively simple systems can be very accurate and robust [4].

An analogue-to-digital converter based on a sigma-delta-modulator consists of two parts, the sigma-delta modulator and its digital post-processing, which are shown in Fig. 2. The system presented in this work is a sigma-delta analogue-to-digital converter, with a proposal for a digital AM demodulation method.

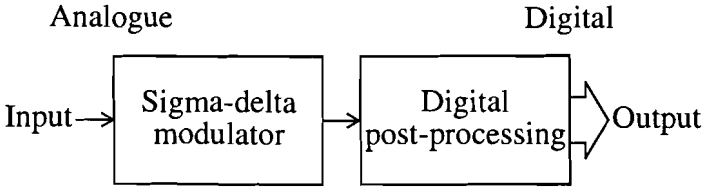

Figure 2. Sigma-delta analogue-to-digital converter.

The analogue input signal is the output current of the position-sensitive detector, which is at a high sampling rate converted to a digital single-bit signal. Digital AM demodulation of this signal recovers the band of interest, also in a digital single-bit format. Digital low-pass filtering eliminates undesired high frequencies, which mainly consist of quantisation noise. The resulting signal is decimated, which results in a multi-bit signal at a lower sampling rate.

The required resolution of the sigma-delta converter is 12bit to 14bit, for a maximum amplitude of the input current of about 100nA. The AM carrier frequency is 1kHz and the modulating signal has a bandwidth of about 200Hz, so the bandwidth of interest reaches from 0.8kHz to 1.2kHz. The clock frequency of the system should not exceed 300kHz, in order to reduce power dissipation for future portable applications. The capacitance of the position-sensitive detector for which the system is designed, is about 50pF. In order to be useful for applications with other types of photodiodes, the capacitance range is taken from 2pF to 50pF.

2. THEORY OF SIGMA-DELTA MODULATION

This chapter deals with the basic theory of sigma-delta modulation. After an overview of sampling and quantisation of analogue signals, resolution enhancement by oversampling and noise-shaping is discussed. These are the processes on which the operation of sigma-delta modulators is based. Finally coding and stability of sigma-delta modulators are analysed. The major differences between theoretical models and real systems are discussed throughout this chapter.

2.1. Analogue and digital signals

An analogue signal is continuous in both time and amplitude, while a digital signal is discrete in both time and amplitude. Converting an analogue signal to a digital signal causes signal degradation. Degradation due to sampling can be avoided, but degradation due to quantisation can only be reduced.

2.1.1. Sampling of an analogue signal

When sampling an analogue signal, samples are taken at equidistant time intervals. The number of samples taken per second determines the sampling rate or sampling frequency f_s. According to the Nyquist criterion, there is no signal degradation if the sampling frequency is at least two times the signal bandwidth [4]. In case the sampling frequency is exactly two times the signal bandwidth, it is called the Nyquist frequency f_{nyq}. The base band ($|f| \leq f_b$) and the side bands, due to the sampling process, will then be separated as shown in Fig. 3. In this case signal recovery is possible.

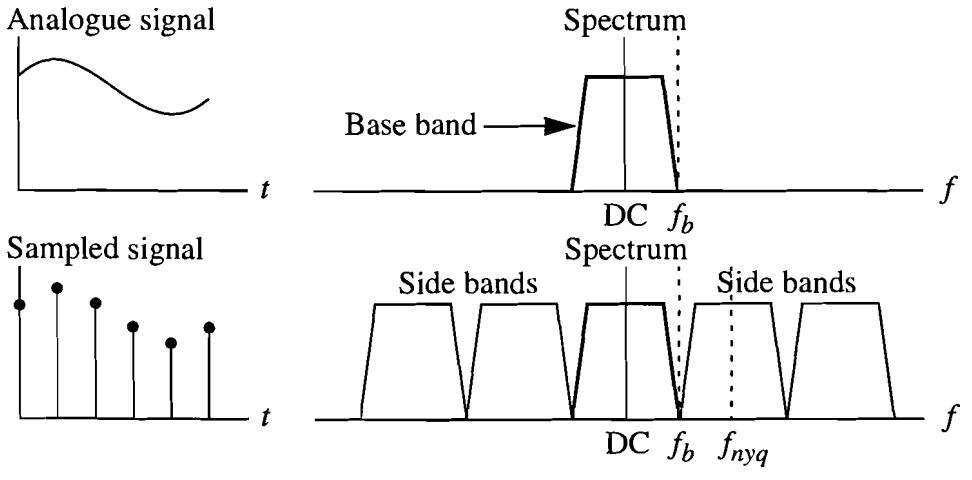

Figure 3. Sampling at the Nyquist frequency.

If the sampling frequency is less than the Nyquist frequency, there is undersampling. In this case the side bands will disturb the base band, so signal recovery is no longer possible. This disturbance is called aliasing [4] and is shown in Fig.4. If on the other hand the sampling frequency exceeds the Nyquist frequency, the sampled signal will contain more samples than necessary for signal recovery. The information contents is the same as in case the signal is sampled at the Nyquist frequency, but the side bands are better separated from the base band. This oversampling is also shown in Fig.4.

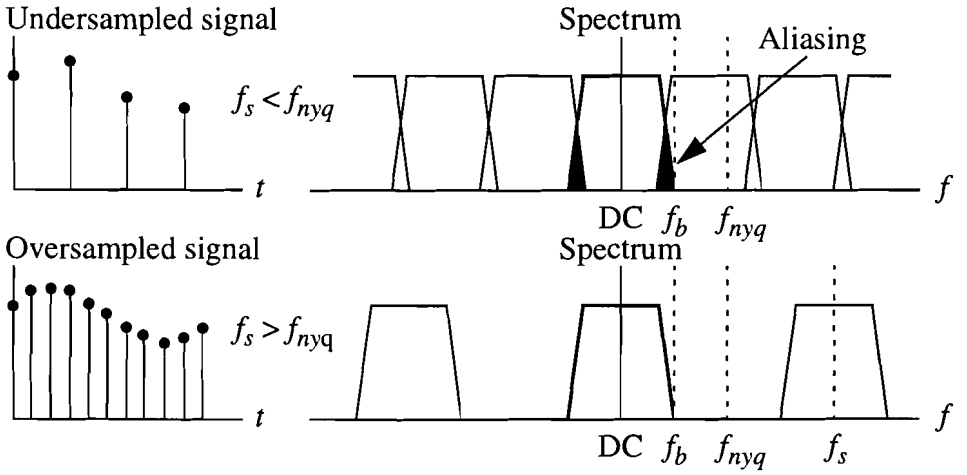

Figure 4. Undersampling and oversampling.

Oversampling is applied in sigma-delta modulators, in order to increase the resolution. The oversampling ratio D is the number of times the sampling frequency is higher than the Nyquist frequency

$$D = \frac{f_s}{f_{nyq}} = \frac{f_s}{2f_b} \tag{1}$$

2.1.2. Quantisation of an analogue signal

If an analogue signal is quantised, its continuous-amplitude value is truncated to a certain discrete-amplitude value. In this way it can be represented by a finite word length. The discrete truncation values are the quantisation levels of the quantiser, which determine its transfer characteristic shown in Fig.5. The input signal of the quantiser Q_{in} is truncated to its nearest quantiser output value Q_{out}. Because of this a quantisation error e_Q is introduced, which varies between plus and minus half the quantisation step q. Therefore the quantiser can be modelled as a unity-gain factor and an additive error source, which is also shown in Fig.5. The error source represents the effect of the quantiser non-linearity. Further on will be discussed that this model is incorrect for calculating stability properties of sigma-delta modulators.

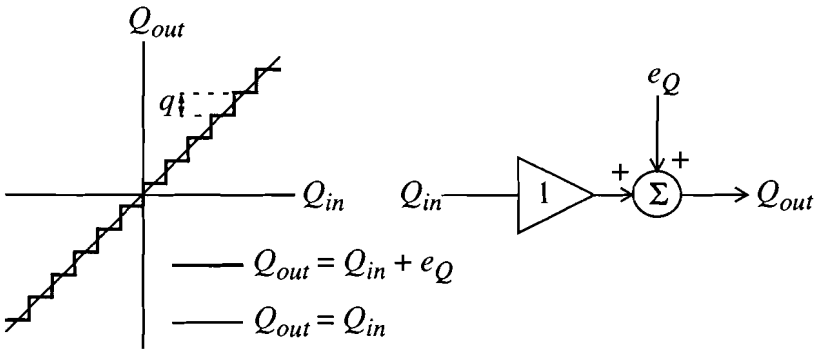

Figure 5. Quantiser transfer characteristic and linear model.

The quantisation error is correlated with the input signal, but if the input signal varies sufficiently fast the quantisation error can be treated as white [4]. The quantisation error is in that case referred to as quantisation noise, which is assumed to be uniformly distributed over the bandwidth $0 \leq f < \infty$. If it is assumed that the probability distribution of its magnitude is uniform, the quantisation noise power can be calculated as

$$\overline{e^2} = \frac{1}{q}\int_{-\frac{q}{2}}^{\frac{q}{2}} e_Q^2 de_Q = \frac{q^2}{12} \tag{2}$$

2.1.3. Sampling and quantisation of an analogue signal

If an analogue signal is both sampled and quantised, the quantisation noise power folds into a bandwidth from DC to half the sampling frequency [4]. In case the sampling frequency equals the Nyquist frequency, the quantisation noise is uniformly distributed over the base band. The quantisation noise power spectral density is in this case

$$E^2(f) = \frac{\overline{e^2}}{f_{nyq}/2} \tag{3}$$

If the maximum output value of the quantiser can be represented by a word of B bits, the maximum analogue sinusoidal input signal has a peak-to-peak value of $2^B q$ and a power of $(2^{B-1}q)^2/2$. The signal-to-noise ratio at the output of the quantiser is in this case given by

$$SNR_Q = 10 \times \log_{10}\left(\frac{3}{2} \times 2^{2B}\right) \approx 1.76 + 6B \quad \text{dB} \tag{4}$$

2.2. Resolution enhancement by oversampling

If the quantisation noise power is uniformly distributed over a bandwidth from DC to half the sampling frequency, it is obvious that increasing the sampling frequency will lower the noise power spectral density and thus the quantisation noise power in the base band. The signal-to-noise ratio is in this case determined by the amount of noise power $\overline{e_o^2}$, which is left in the base band. This process is illustrated in Fig.6.

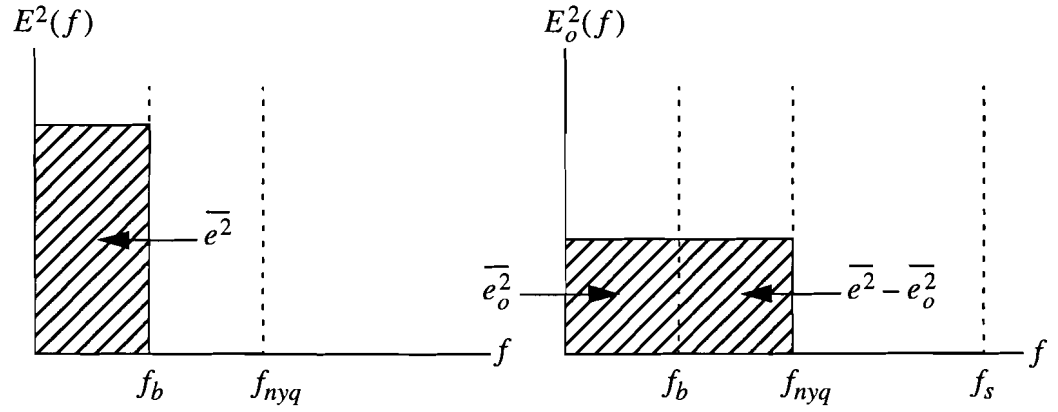

Figure 6. Reduction of quantisation noise power in the base band by oversampling.

The quantisation noise power spectral density is in this case

$$E_o^2(f) = \frac{\overline{e^2}}{f_s/2} \tag{5}$$

The noise power in the base band is thus determined by the oversampling ratio

$$\overline{e_o^2} = \int_0^{f_b} E_o^2(f)df = \frac{2f_b}{f_s}\overline{e^2} = \frac{1}{D}\overline{e^2} \tag{6}$$

If the input signal has a peak-to-peak value of $2^B q$, the signal-to noise-ratio becomes

$$SNR_Q = 10 \times \log_{10}\left(\frac{3}{2} \times 2^{2B} \times D\right) \text{ dB} \tag{7}$$

Compared to equation (4) is the oversampling ratio present in the equation. By increasing the oversampling ratio, the resolution of the sigma-delta modulator increases.

2.3. Resolution enhancement by noise-shaping

A sigma-delta modulator shapes the quantisation noise in such a way, that it is suppressed for low frequencies and amplified for higher frequencies. In Fig.7 the general topology of a sigma-delta modulator is shown [4].

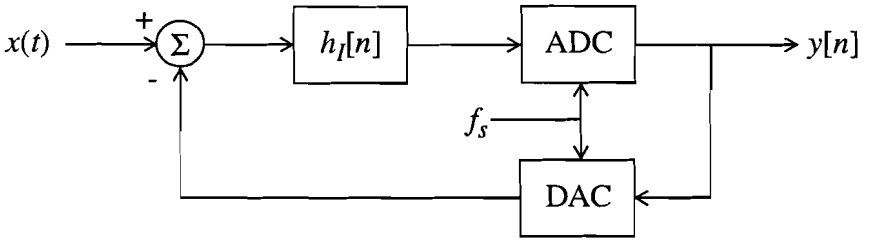

Figure 7. General topology of a sigma-delta modulator.

The analogue input signal $x(t)$ is compared to the encoded binary output signal $y[n]$ and their difference is accumulated by an integrator $h_I[n]$. Note that the binary coded output signal of the integrator, is the output signal of the sigma-delta modulator. If the order of the integrator is increased, the quantisation noise in the base band will be further suppressed. The order of the integrator is also the order of the sigma-delta modulator.

The analogue-to-digital converter and the digital-to-analogue converter together, form the previously discussed quantiser. This combination truncates a continuous-amplitude signal to a discrete-amplitude signal. The analogue-to-digital converter also samples the signal, but this can also be done elsewhere in the system. From this point on a digital signal is defined as a binary coded discrete-time and discrete-amplitude signal, instead of its uncoded version. Note that the digital-to-analogue converter introduces no error, so its analogue output signal contains the same information as its digital input signal. Therefore the digital-to-analogue converter can be left out in sigma-delta modulator models.

Because of the quantiser, a sigma-delta modulator is a non-linear system. In order to make quantisation noise calculations, the linear model of Fig.8 is introduced [4].

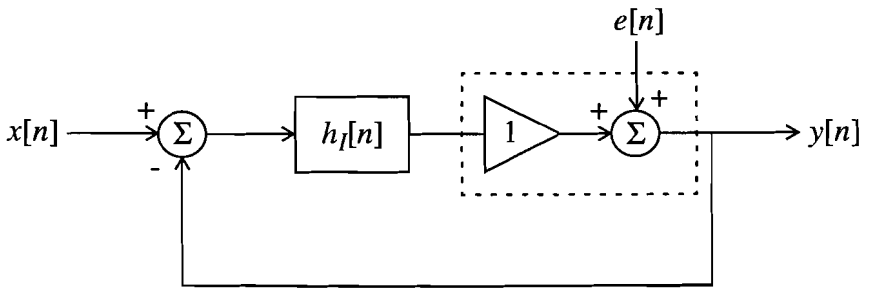

Figure 8. Linear sigma-delta modulator model.

The combination of analogue-to-digital converter and digital-to-analogue converter is replaced by the linear quantiser of Fig.5. Note that the input signal is now discrete-time. The transfer function of this system in the z-domain is

$$Y(z) = \frac{H_I(z)}{1+H_I(z)}X(z) + \frac{1}{1+H_I(z)}E(z) \tag{8}$$

If $H_I(z)$ is an integrator transfer function, the input signal is almost fully transferred and the quantisation noise in the base band is suppressed in a certain degree. The noise-shaping process will be illustrated by analysing the basic Lth-order sigma-delta modulator shown in Fig.9 [4].

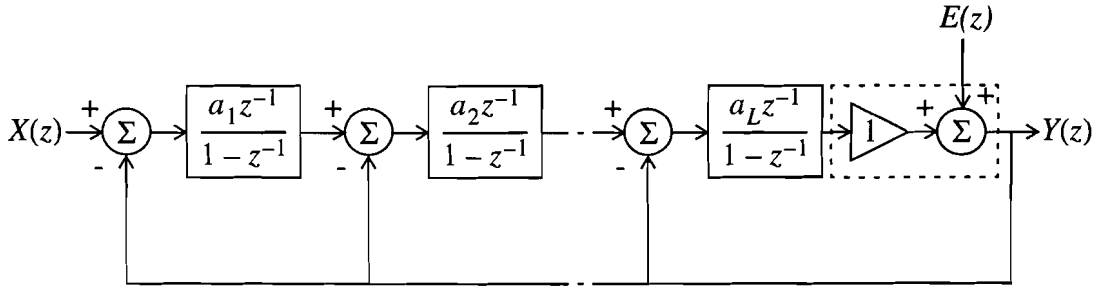

Figure 9. Linear Lth-order sigma-delta modulator model.

Integrators 1 to L, together with the feedback paths, make up the Lth-order integrator. Each integrator has a gain factor, in order to optimise the noise-shaping properties. These gain factors are also for optimising the stability properties of the system, but this will be discussed further on. The transfer function of this system in the z-domain is

$$Y(z) = \frac{a_L \ldots a_1 z^{-L} X(z) + (1-z^{-1})^L E(z)}{(1-z^{-1})^L + a_L z^{-1}(1-z^{-1})^{L-1} + \ldots + a_L \ldots a_1 z^{-L}} \tag{9}$$

With the gain factors of the integrators the transfer function can be optimised towards

$$Y(z) = z^{-L}X(z) + (1-z^{-1})^L E(z) \tag{10}$$

With $z=e^{j\theta}$ and $\theta=2\pi f/f_s$, the modules of the transfer function in the f-domain is

$$|Y(f)| = |X(f)| + \left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^L |E(f)| \tag{11}$$

The power spectral density of the quantisation noise becomes thus

$$E_{on}^2(f) = \left\{\left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^L |E_o(f)|\right\}^2 = \frac{2}{f_s}\left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^{2L}\overline{e^2} \tag{12}$$

If $f_s \gg f_b$ then $\sin(\pi f/f_s) \approx \pi f/f_s$, so the quantisation noise power in the base band is approximated by

$$\overline{e_{on}^2} = \int_0^{f_b} E_{on}^2(f)df \approx \frac{\pi^{2L}}{2L+1}\left(\frac{1}{D}\right)^{2L+1}\overline{e^2} \tag{13}$$

If the input signal has a peak-to-peak value of $2^B q$, the signal-to noise-ratio becomes

$$SNR_Q = 10 \times \log_{10}\left[\frac{3}{2} \times 2^{2B} \times \frac{2L+1}{\pi^{2L}} D^{2L+1}\right] \text{ dB} \tag{14}$$

Compared to equation (7) the oversampling ratio is present in a higher degree, depending on the system order. By increasing the system order, the resolution of the sigma-delta modulator increases.

All these equations are valid for $L \geq 0$, but for $L=0$ the system consists of only the quantiser. Both first-order and second-order quantisation noise spectral densities are shown in Fig. 10, together with the spectral density when no noise-shaping is applied.

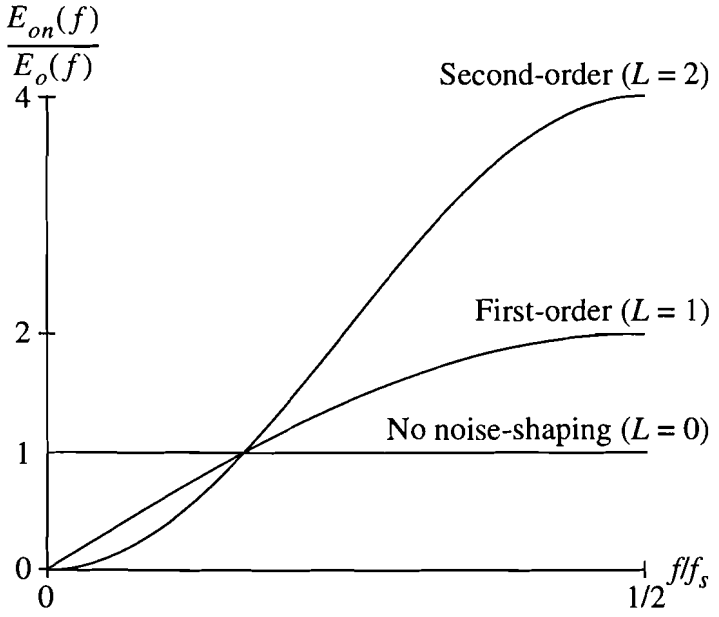

Figure 10. Quantisation noise spectral densities due to and without noise-shaping.

It is obvious that the quantisation noise is suppressed for low frequencies and amplified for higher frequencies. The degree of suppression increases with increasing order of the sigma-delta modulator. From equation (12) it can be derived, that the total quantisation noise power increases with increasing order of the system. After noise-shaping the quantisation noise is often referred to as modulation noise.

According to equation (4), a signal-to-noise ratio increment of 6dB is equivalent to a resolution increment of 1bit. According to equation (14), the signal-to-noise ratio increases with $3(2L+1)$dB for every doubling of the sampling frequency. This implies that the resolution of the sigma-delta modulator increases with $L+1/2$bit. Every extra quantiser bit adds 6dB, which is equivalent to 1bit resolution enhancement. In Fig.11 this relationship is shown for different orders of a sigma-delta modulator, with a single-bit quantiser ($B=1$). Every extra quantiser bit lifts the characteristics 6dB, but the noise-shaping process itself is unaffected.

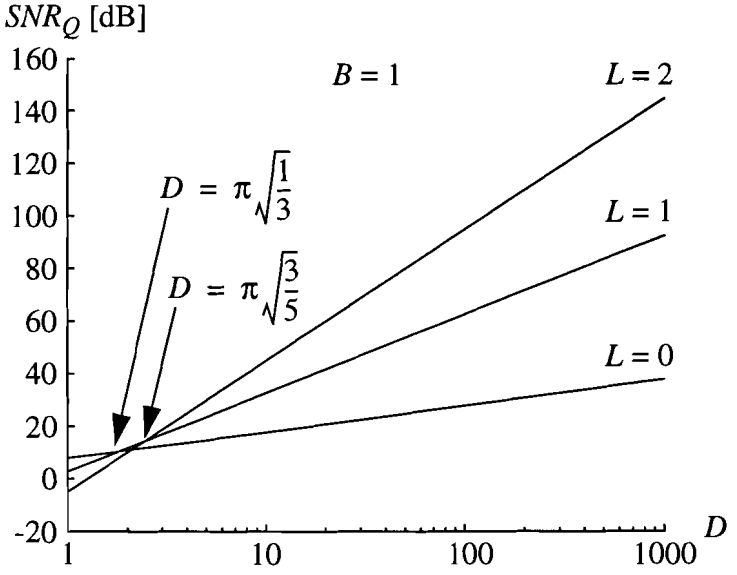

Figure 11. Signal-to-noise ratio as function of oversampling ratio and order.

This figure also shows that the oversampling ratio has to be of a certain value if the order of the system is increased, otherwise the resolution will decrease instead of increase. For a higher order the oversampling ratio has to be (compared to $L-1$)

$$D > \pi\sqrt{\frac{2L-1}{2L+1}} \quad ,L \geq 1 \tag{15}$$

2.4. Coding mechanism and validity of the white noise assumption

The way a sigma-delta modulator converts an analogue to a digital signal, will be illustrated by the first-order single-bit system shown in Fig.12. A first-order single-bit system gives a clear view on the operation of sigma-delta modulators. Again the quantiser is considered to be the combination of the analogue-to-digital converter and the digital-to-analogue converter, but they are separately shown. Because it is a single-bit system, the quantiser has two output or quantisation levels $\pm q/2$.

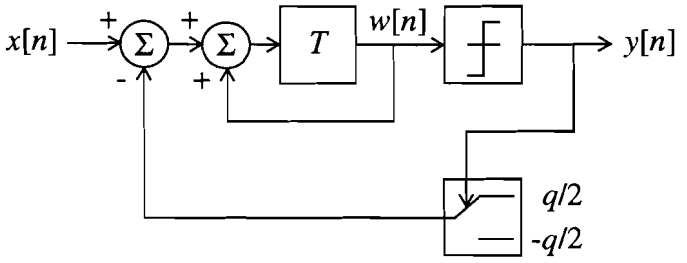

Figure 12. First-order single-bit sigma-delta modulator.

The output signals of the integrator $w[n]$ and the sigma-delta modulator $y[n]$ are

$$w[n] = w[n-1] + x[n-1] - y[n-1]$$
$$y[n] \equiv \begin{cases} q/2 & ,w[n] \geq 0 \\ -q/2 & ,w[n] < 0 \end{cases} \tag{16}$$

Note that not the format of the output signal $y[n]$ is relevant, but the values of the quantisation levels represented by it. The ranges of the sigma-delta modulator input-signal $x[n]$ and the integrator output signal $w[n]$ are

$$\begin{aligned} -q/2 \leq x[n] \leq q/2 \\ -q \leq w[n] \leq q \end{aligned} \tag{17}$$

The range of $x[n]$ equals the output range of the quantiser. If $x[n]$ exceeds this range the system overloads, because it can not correct itself any more. The range of $w[n]$ is only relevant in practice, because the integrator may not overload. This causes loss of information and thus signal degradation.

Equation (16) shows that the difference between the input signal and the output signal of the sigma-delta modulator, the error, is accumulated by the integrator. The system tries to keep the average error zero, so the average increment of the integrator output signal is also zero. Therefore its sign has to change in time and because of that the sign of the sigma-delta modulator output signal also changes. The system tries to minimise the error between its input and output, which gives such a variation in $y[n]$ that the average value of this signal approximates the value of the input signal. This will be illustrated by a numerical example.

Suppose that the quantiser levels in Fig. 12 are $\pm q/2 = \pm 1$ and the input signal has a value of $x[n] = 0.1$. The quantiser output signal will then oscillate between -1 and 1, in such a way that the average value over a certain number of output samples equals 0.1. This is shown in Fig. 13. The output signal of the quantiser has a period of twenty samples, of which nine equal -1 and eleven equal 1. Its average value is 0.1, equal to the input value of the sigma-delta modulator. For converting the value 0.1 the period is relatively small. For converting a more complicated value, for example 0.1234, the period will be larger.

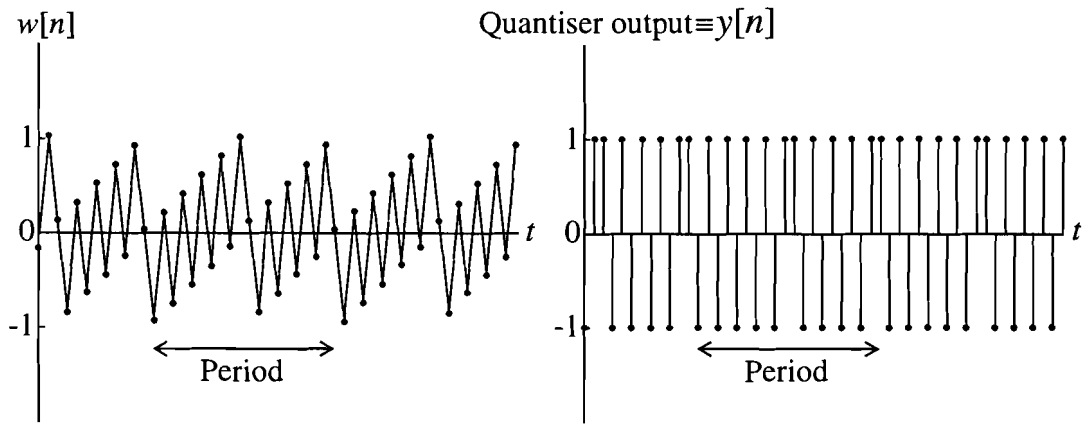

Figure 13. Output signals of the integrator and the quantiser.

When the input signal of the single-bit first-order sigma-delta modulator is zero, its output oscillates between one and minus one, keeping its average value zero. This will be discussed in more detail further on. When a small sinusoidal input signal is applied to the system, its amplitude has to be larger than a certain threshold value A_{th}, in order to appear at the output. This threshold can be determined with [4]

$$\frac{A_{th}}{q/2} = \kappa\left(\frac{\pi}{D}\right)^{L} \quad ,\kappa \leq 1 \tag{18}$$

For a first-order system $\kappa = 1$ and κ decreases for an increasing order of the system. As the worst-case condition κ will be assumed equal to one for every order. If the sigma-delta modulator has to achieve a resolution of N bit, the condition for the oversampling ratio is determined by the threshold value as

$$\frac{A_{th}}{q/2} \leq 2^{-N} \Rightarrow D \geq 2^{N/L}\pi \tag{19}$$

Equation (18) implies that every doubling of the sampling frequency gives an increase in signal-to-noise ratio of $6L$dB, instead of the in section 2.3 calculated $3(2L+1)$dB. This means a resolution improvement of Lbit, instead of $L+1/2$bit, which shows that not only the quantisation noise determines the resolution of the sigma-delta modulator.

To illustrate the noise-shaping process, the quantisation error signal of a single-bit quantiser is in Fig. 14 compared to that of the first-order sigma-delta modulator.

The quantiser truncates the input value of 0.1 to 1, so the quantisation error is always 0.9 and all the quantisation noise power is thus located at DC. Previously has been assumed that when the input signal varies sufficiently fast, the quantisation error can be modelled as an additive white noise source. The quantisation noise has in that case a random character. A DC input signal does not vary, so the white noise assumption is not valid.

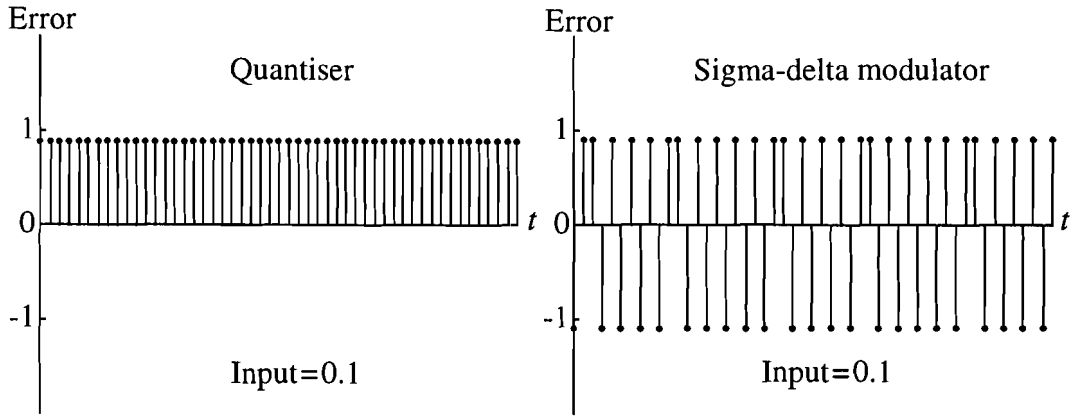

Figure 14. Quantisation error of a single-bit quantiser and of a first-order single-bit sigma-delta modulator, both for an input signal of 0.1.

The output signal of the sigma-delta modulator changes between -1 and 1, so the quantisation error changes between -1.1 and 0.9. Because it is a varying signal the quantisation noise power is located at higher (discrete) frequencies. In this case the input signal of the single-bit quantiser in the system is not a DC signal, even though the input signal of the sigma-delta modulator is. The quantisation error is less correlated with the input signal and thus the quantisation noise spectral density is more white. The higher the order of the sigma-delta modulator is, the more random the quantisation error is and the more valid the white noise assumption [4].

The quantisation noise spectral density depends in case of a DC input signal thus on the order of the sigma-delta modulator and on the value of the input signal. If the frequency components of the error signal are located within the signal band they appear as so called pattern noise [4]. This degrades the signal-to-noise ratio and thus the resolution of the system. If the input signal of a sigma-delta modulator is an AC signal, a relatively fast varying signal, the assumption of a random quantisation error is more valid than in case of a DC input signal. In this case the quantisation noise spectral density looks more like the ones previously determined. However, the quantisation error is always correlated in a certain degree with the input signal of the sigma-delta modulator. Therefore the previous quantisation noise calculations are always an approximation. The real performance has to be verified by computer simulations.

2.5. Stability of sigma-delta modulators

The z-plane poles of a sigma-delta modulator can be derived from its linear transfer function, in order to determine the stability of the system. Only if the poles lay within the z-plane unity-gain circle, the system is stable [4]. Stability is in this case regarded in the context of linear systems, but a sigma-delta modulator is a non-linear system and therefore it is more complicated to determine its stability.

A sigma-delta modulator is stable, if for a bounded input signal its state variables are also bounded. Even if the system is stable during normal operation, its stability can not always be guaranteed in other circumstances [4]. The system must also be able to go to normal operation after non-zero initial state conditions and return to normal operation after an overload. Because there are different factors that can make a sigma-delta modulator unstable, stability can not accurately be determined by calculation. Extensive computer simulations have to determine if stability can be guaranteed under all conditions mentioned. However, for approximating the positions of the poles linear stability calculation techniques are useful.

The quantiser error can not be seen as a random signal any more, because stability analysis require a more deterministic approach. Therefore the quantiser is modelled as a non-linear gain factor λ, which represents its non-linearity. The non-linear quantiser model is shown in Fig. 15.

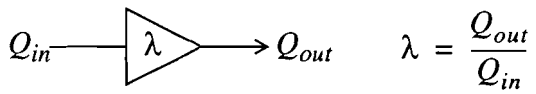

Figure 15. Non-linear model of the quantiser.

By replacing the linear quantiser in the sigma-delta modulator of Fig.8 for the non-linear one, the transfer function of the sigma-delta modulator becomes

$$Y(z) = \frac{\lambda H_I(z)}{1 + \lambda H_I(z)} X(z) \tag{20}$$

The poles of the system can be determined by solving the characteristic equation

$$1 + \lambda H_I(z) = 0 \tag{21}$$

To gain insight in the stability behaviour, the basic Lth-order sigma-delta modulator shown in Fig. 16 is analysed.

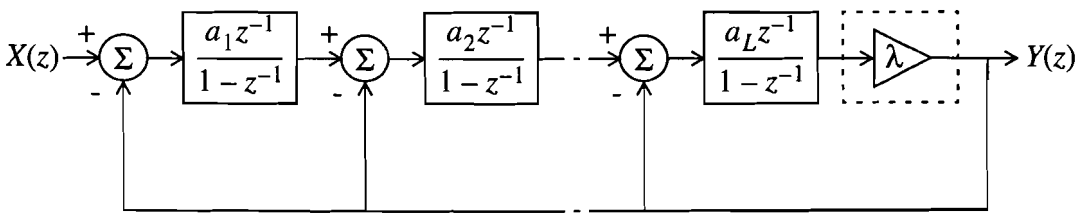

Figure 16. Basic Lth-order sigma-delta modulator.

The transfer-function of this system in the z-domain is

$$Y(z) = \frac{\lambda a_L \ldots a_1 z^{-L}}{(1-z^{-1})^L + \lambda[a_L z^{-1}(1-z^{-1})^{L-1} + \ldots + a_L \ldots a_1 z^{-L}]} X(z) \qquad (22)$$

The poles of the system can be derived from this equation. The position of the poles is in this case not only determined by the gain factors of the integrators, but also by the non-linear gain of the quantiser. Because of the last one the poles can move outside the unity-gain circle during operation, so the system becomes unstable. Further on it will be discussed, that for the operation of the sigma-delta modulator a certain kind of instability is required.

As mentioned in section 2.3, the gain factors of the integrators are not only for optimising the noise-shaping properties of the system, but also for optimising the stability properties. In most cases a compromise between resolution and stability has to be made. Because an unstable sigma-delta modulator is useless, resolution has then to be sacrificed, in order to obtain a stable system.

2.5.1. Stability of single-bit sigma-delta modulators

The gain of a single-bit quantiser is strongly non-linear, so its linearised transfer characteristic is arbitrary. There are infinite possible linear transfer characteristics to choose from. The pole movement of the system can not be calculated exactly, because the gain factor a_L of the integrator preceding the quantiser does not change the behaviour of the system. Only the sign and not the magnitude of the output signal of that integrator, determines the output of the quantiser and thus the behaviour of the system. Although exact modelling is not possible, basic root locus calculation techniques can in some cases give a good approximation about the stability of single-bit sigma-delta modulators. This is shown in Fig. 17.

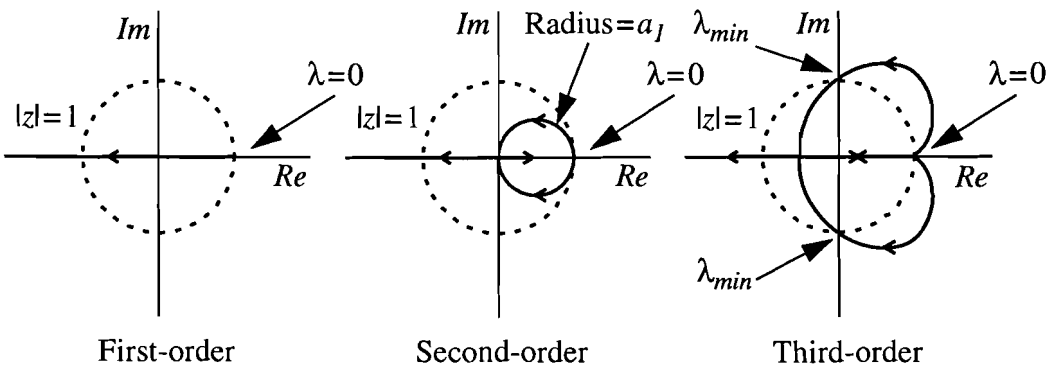

Figure 17. Root locus as a function of the quantiser gain in the z-plane.

A first-order system is always stable for every value of the integrator gain factor. The stable input range is $\pm q/2$, in order not to overload the system. A second-order system is only stable for values of gain factor a_1 of the first integrator, that are smaller than unity. Although computer simulations show that a_1 has to be smaller than 0.8, the approximation is good. The stable input range of the second-order sigma-delta modulator is smaller than $\pm q/2$. This is because the output of the integrator preceding the quantiser increases without limit, when the input signal comes close to $\pm q/2$. The integrator will overload and the sigma-delta modulator does not operate properly, so signal degradation is the consequence.

In both cases rather accurate conditions for the integrator gain factors and the input range can be determined, in order to keep the poles within the unity-gain circle. In the first-order case nothing has to be done to acquire a stable system and in the second-order case only an integrator gain factor has to be properly set and the input range is bounded. This is however not possible for higher-order systems ($L \geq 3$), because for them extra measures have to be taken in order to keep the system stable. One possible method will be given [5]. For higher-order systems, the intersection point of the root locus and the unity-gain circle can be calculated. For the third-order system in Fig. 17 these are marked λ_{min}. This is the minimum value of the quantiser gain, for which the poles stay within the unity-gain circle and thus the system is stable. In order to keep the quantiser gain above this value, measures have to be taken in the form of suitable output limits for the integrator preceding the quantiser.

For a certain value of the quantiser gain, one pole crosses the unity-gain circle at $z=-1$. In this case the input signal of the sigma-delta modulator is zero, so an idle pattern at half the sampling frequency occurs. The in this case between the two reference levels oscillating quantiser output, also has an average value of zero. Applying an input signal to the system disturbs the idle pattern generating another pattern, so the average output value changes. These patterns are limit cycles, which are stable oscillations [5]. In the context of linear systems this is instability, because the system has no stable operating point. However, this kind of instability is needed for the operation of sigma-delta modulators. The previously given stability condition is very suitable for designing purposes, but stability of sigma-delta modulators has to be defined more exactly. This will give a better view on the operation of the system. Limit cycles that are located at higher frequencies are a part of the quantisation error. They do not disturb the signal band, so they can be regarded as quantisation noise. If there are limit cycles present that are not affected by the input signal of the system, the system is unstable. These limit cycles can disturb the signal band and remain present when the value of the input signal is returned to zero.

If for a stable system a pole leaves the unity-gain circle at $z=-1$, the quantiser gain and the limit cycle increase. Because of that the input signal of the quantiser increases, so the gain and the limit cycle decrease. This will bring the pole back within the unity-gain circle. If however a pole leaves the unity-gain circle for $z>0$, the quantiser gain decreases ($\lambda \leq \lambda_{min}$) and the limit cycle increases. Because of that the input signal of the quantiser increases, decreasing the quantiser gain even further. Therefore the pole will not return within the unity-gain circle, resulting in an unstable system.

The shape of the idle pattern depends on the order of the sigma-delta modulator. This means that its spectral components differ for every order. For a first-order system the idle pattern frequency is at $f_s/2$. For a second-order system the idle pattern frequency is at $f_s/4$, which is not according to the root locus of Fig. 17. The quantiser model with only a varying gain is not sufficient to explain the behaviour of sigma-delta modulators accurately, because its phase-uncertainty is not taken into account [6].

2.5.2. Stability of multi-bit sigma-delta modulators

A multi-bit sigma-delta modulator has a multi-bit quantiser, so it has more than two output values. The gain of a single-bit quantiser can vary between zero and infinity, but the gain of a multi-bit quantiser can only vary between one and infinity. A condition is that the multi-bit quantiser is not overloaded. If the value of the input signal is zero the gain is infinity. If an input signal is applied to the system the gain will be close to unity. For stability the range between zero and one is relevant, because for higher-order systems λ_{min} is usually within this range. If this range can be avoided the system is always stable. The root locus of a multi-bit system is comparable to the root locus of a single-bit system. Note that if the input of a multi-bit sigma-delta modulator is zero, its quantiser output oscillates between the two smallest output levels $\pm q/2$, generating an idle-pattern.

If an input signal is applied to the multi-bit sigma-delta modulator, its quantiser can be approximated by the linear model ($\lambda=1$) of Fig. 5 and the poles of the system can be derived from equation (22). The approximation of $\lambda=1$ is only valid if the quantiser does not overload, so that the quantisation error is always between $-q/2$ and $q/2$. The output signal of the integrator preceding the quantiser, denoted as $w[n]$, has then the following range [4]

$$\left(-2^{B-1}-\frac{1}{2}\right)q \le w[n] \le \left(2^{B-1}+\frac{1}{2}\right)q \tag{23}$$

In order to meet this condition, the input range of the sigma-delta modulator is [4]

$$|x[n]| \le \left[\left(2^{B-1}+\frac{1}{2}\right)-\left(2^{L-1}-\frac{1}{2}\right)\right]q \tag{24}$$

This implies that the stable input range of the sigma-delta modulator is smaller than the input range of its quantiser. By determining the appropriate integrator gain factors the poles can be placed within the unity-gain circle. Because the quantiser is not perfectly linear, there is still a little variation in quantiser gain that shifts the poles during operation. The exact variation depends on the number of output bits and on the value of the input signal. This will cause low-level limit cycles [4], but will not lead to an unstable system. Nevertheless, the stability of the system under all circumstances has to be verified by extensive computer simulations.

2.6. Summary

The operation of a sigma-delta modulator is based on oversampling and noise-shaping. Oversampling is required for the correct operation of the system and distributes the quantisation noise over a wide frequency range. Noise-shaping suppresses the quantisation noise for low frequencies. In both cases the quantisation noise in the base band decreases, so the resolution of the system increases.

In modelling the noise-shaping and stability behaviour of the system, certain assumptions have to be made, that make the analysis an approximation. How accurate this approximation is depends on different properties of the system. Because exact modelling is not possible, quantisation noise and stability behaviour have to be verified and optimised by computer simulations. The methods of simulation will be discussed further on. There will be a compromise between stability and resolution.

3. THE TOPOLOGY AND ITS IMPLEMENTATION

In this chapter the topology of the sigma-delta modulator is determined. Hand calculations give a point to start the design from, but extensive computer simulations have to verify and optimise it. The resulting topology is translated into a circuit. It is relevant that the circuit realises exactly the same transfer function as the topology, otherwise the behaviour of the circuit is not in compliance with that of the topology.

3.1. Determining the topology of the sigma-delta modulator

For sigma-delta modulators already exist several topologies, which all have their distinctive features. Because the aim of this work is to design a sigma-delta modulator for a specific application, its topology is selected out of these existing ones rather than developing a new one. Main selection criteria for the topology are the noise-shaping and stability properties, but also the complexity and the sensitivity to circuit limitations are relevant. These criteria depend on the application for which the sigma-delta modulator is designed and therefore the system requirements discussed in chapter 1 are decisive. First the output format of the sigma-delta modulator is determined, so single-bit or multi-bit, and after that the topology and its required parameters. Because calculations only give an approximation of the noise-shaping and stability properties of the system, computer simulations will be used for verification and optimisation.

3.1.1. Single-bit and multi-bit sigma delta modulators

As already implied in chapter 2, there are differences between single-bit and multi-bit sigma-delta modulators in noise-shaping and stability behaviour. Depending on the application an appropriate choice has to be made. Because the single-bit output format has decisive advantages for the application, it is chosen for the design.

For an equal oversampling ratio, a multi-bit sigma-delta modulator achieves a higher resolution than a single-bit one. If there is a sufficient number of output bits even the system order can be decreased. This can be directly concluded from equation (14). Another advantage is that it is less complicated to design a stable multi-bit sigma-delta modulator, because its poles can be calculated more accurately.

The major drawbacks of a multi-bit output format are the more complex circuitry and the higher sensitivity to circuit limitations. A multi-bit analogue-to-digital converter and digital-to-analogue converter are non-linear. The non-linearity of the analogue-to-digital converter is reduced by the feedback action of the system, but the non-linearity of the digital-to-analogue converter is not. Therefore its linearity has to be the same as the linearity of the sigma-delta modulator, even though its number of

output bits may be far less [4]. It is possible to digitally correct the non-linearity of the digital-to-analogue converter [7], but this requires extra circuitry.

A single-bit analogue-to-digital converter and digital-to-analogue converter are always linear, have a relatively high insensitivity to circuit limitations and can be realised with relatively simple circuitry. These are important reasons for preferring a single-bit output format over a multi-bit one. Another advantage of a single-bit sigma-delta modulator is its pulse-density modulated output format. It makes the use of less complicated and less power dissipating digital post-processing circuitry possible, because all required operations can be realised with simple logical operations [4].

3.1.2. The topology

Besides the basic sigma-delta modulator topology discussed in chapter 2, there are several alternatives. The ones most frequently used can be found in [4] and [5]. The major differences are in the noise-shaping and stability properties, but therefore also in the complexity of the circuity required to implement them. Optimising a topology towards resolution or stability, without affecting the other one too much, means usually the use of extra circuitry. Especially if it is for the digital post-processing, the area and power dissipation become decisive.

For this application the basic sigma-delta modulator topology is chosen, because it is relatively uncomplicated to implement. This is mainly because its relatively high insensitivity to circuit limitations and its possibility to accommodate a single-bit output format. The basic Lth-order single-bit sigma-delta modulator topology is shown again in Fig. 18. The structure of integrators 1 to L is separately displayed, together with their transfer function in the z-domain.

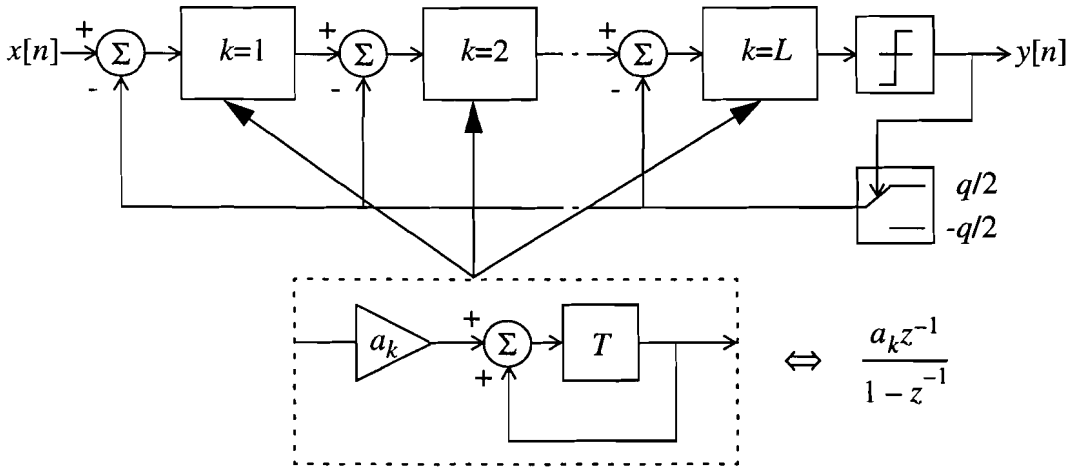

Figure 18. Basic Lth-order single-bit sigma-delta modulator topology.

The system parameters that have to be determined are the oversampling ratio, the system order, the quantisation levels and the integrator gain factors. After high-level computer simulations, the stable input range can be determined as

$$|x[n]| \leq \sigma \frac{q}{2} \quad ,\sigma \leq 1 \tag{25}$$

3.2. Approximation of the required parameters

For now the oversampling ratio, the system order and the integrator gain factors are relevant. In a later stage, when the circuit properties have to be taken into account, also the quantiser levels are relevant. First the parameters for achieving the required resolution are determined by hand calculations and after that verified by computer simulations.

3.2.1. Calculation of the required parameters

To approximate the system parameters, calculations have to be made first. Even though they will not give a final set of parameters, they provide a point to start the design from. In this stage only the required resolution will be taken into account. Stability calculations will be omitted, because for a single-bit system it is difficult to give a stability approximation. This is especially the case for instability due to non-zero initial state conditions and due to overload. For a single-bit system $B=1$ in equation (14). The relationship between the signal-to-noise-ratio and the oversampling ratio for the single-bit case has already been shown in Fig. 11, for several system orders. By taking the specifications from chapter 1 into account, the parameters of the system can be calculated. Note that the bandwidth of interest is 0.8kHz to 1.2kHz, but the topology of the sigma-delta modulator will be optimised for a bandwidth from DC to 1.2kHz.

With equation (4) it can be calculated, that for the required 14bit resolution the signal-noise-ratio has to be $SNR_Q \geq 86$dB. The maximum clock frequency and thus sampling frequency is 300kHz, so $f_s=256$kHz is a good choice. This is the AM carrier frequency of $f_c=1$kHz multiplied by 2^8, which might be useful for digital post-processing. For a maximum signal frequency of $f_b=1.2$kHz, the oversampling ratio is calculated with equation (1) at about $D=100$. According to equation (14) a second-order system ($L=2$) achieves in this case a signal-to-noise ratio of 95dB, which is according to equation (4) equivalent to 15.5bit resolution. Compared to the specification there is a 1.5bit margin to compensate for circuit limitations. The required integrator gain factors are derived from equation (9). Inserting $L=2$, $a_1=0.5$ and $a_2=2$ in this equation, reduces it to the optimal form of equation (10)

$$Y(z) = z^{-2}X(z) + (1-z^{-1})^2 E(z) \tag{26}$$

Without any need for calculating stability properties, a prediction for stability can be made. According to section 2.5.1 a second-order system is always stable for $a_1<0.8$, so this condition is met. The value of a_2 is arbitrary, because it is the gain factor of the integrator preceding the single-bit quantiser.

3.2.2. Verification by computer simulation

The possibility of using a second-order system is advantageous, because it is easy to stabilise. However, it has to be kept in mind that the quantisation noise predictions are an approximation. This is especially the case for single-bit systems, because the linear single-bit quantiser model is inaccurate and the value of the integrator gain factor preceding the quantiser does not change the behaviour of the system. Therefore the selected topology has to be simulated by computer, in order to determine its achievable resolution. High-level computer simulations are performed with the numerical calculation package MATLAB. The method of simulation is discussed in the appendix. In Fig. 19 the simulation model of the second-order sigma-delta modulator is shown.

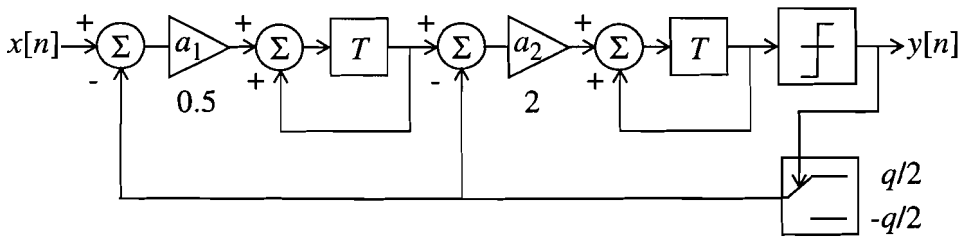

Figure 19. Second-order sigma-delta modulator simulation model.

The exact value of the quantiser levels $\pm q/2$ is in this stage not relevant. They only determine the stable input range, of which the exact value is not relevant either for now. Only the circuit properties, especially the supply voltages, are decisive for the value of the quantiser levels. This will be discussed further on. Note that the quantiser is the combination of analogue-to-digital converter and digital-to-analogue converter.

The simulation results for the signal-to-noise ratio as function of the input signal amplitude, are shown in Fig. 20. The system achieves a maximum signal-to-noise ratio of 79dB, which is equivalent to a resolution of 12.9bit. The stable input range is $|x[n]| \leq 0.8q/2$, which gives $\sigma=0.8$. This is 2.6bit below the calculated resolution and 1.1bit below specification. Simulating the system with other values of a_1 does not give any improvement, so this system is not able to achieve the required resolution. It demonstrates that the quantisation noise calculations of section 2.3 are too optimistic. This is not only due to the white noise assumption, but also because of the maximum input range. The peak-to-peak value of the maximum input signal is $1.6q/2$, which is smaller than the in equation (14) assumed value of $2^B q=2q$. Recalculating equation (14) for a peak-to-peak value of $1.6q$ gives for the resolution 14bit, which is still too optimistic.

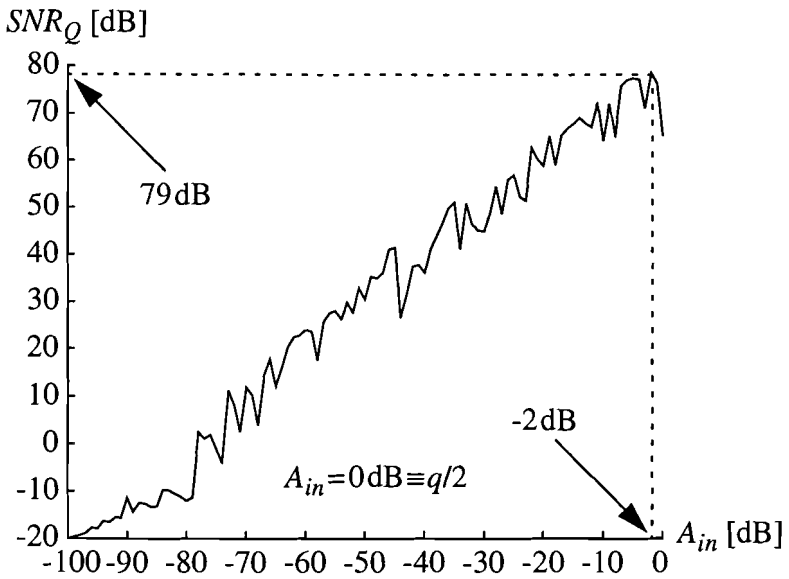

Figure 20. Signal-to-noise ratio characteristic of the second-order system.

Also the condition set by the threshold of section 2.4 is not met. With equation (19) it can be calculated that the oversampling ratio of a second-order system has to be $D \geq 400$, in order to achieve a 14bit resolution. Therefore a new set of parameters has to be determined and again verified by computer simulations.

3.3. Determining the required parameters by computer simulation

The maximum sampling frequency is limited to 300 kHz. Raising it from 256kHz to its maximum value, would according to equation (14) give a gain in resolution of about 1bit. Because the true gain in resolution is less than the calculated one, raising the sampling frequency is not an option. It seems that the order of the sigma-delta modulator has to be raised to three, because a second-order system stays just below the specified resolution of 14bit.

Instead of estimating the parameters by calculation, only computer simulations will be used to optimise the system towards its required resolution. This for two reasons. The first one is the relatively large deviation between calculation and simulation results, especially for a single-bit system. The second one is the stability of the system. If it is optimised towards resolution, there is a possibility that stability can not always be guaranteed. Therefore first the resolution has to be optimised and after that the stability verified. High-level simulations for the verification of stability, are discussed in the appendix. If the system is not stable under the conditions mentioned in section 2.5, its parameters have to be altered and the complete behaviour should be verified again. The aim is to keep the poles within the unity-gain circle, under all conditions. Usually resolution has to be sacrificed, in order to obtain a stable and thus useful system. In Fig.21 the simulation model of the third-order sigma-delta modulator is shown.

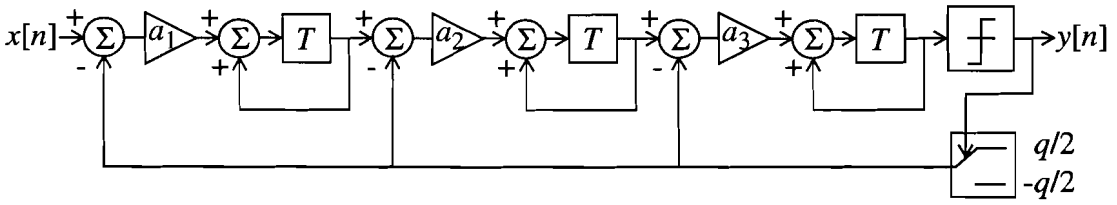

Figure 21. Third-order sigma-delta modulator simulation model.

The oversampling ratio is again $D=100$. The parameters to be determined are the integrator gain factors and the reference levels of the quantiser. At this point the actual circuit properties have to be taken into account, because the power supply sets the hard limit for the integrator output swing. The supply voltages are assumed to be $\pm V_{DD}/2$ and the integrator output range is thus the same. The dimensions of the signals are not relevant yet, so they will be regarded without them.

An incorrect set of parameters can overload the integrators, which means signal degradation and thus loss of resolution. Even if the integrators do not overload and the system is stable during normal operation, certain combinations of parameters can still cause instability. This because the system might not be able to go to normal operation after non-zero initial state conditions or to return to normal operation after an overload. To obtain a stable system under all conditions, the method of design is important. As a starting point the quantiser levels are determined. Their values are decisive for the values of the integrator gain factors obtained later. Instability under normal operation can be prevented by correct scaling of the integrator output signals in proportion to the quantiser levels [5]. Instability because of non-zero initial states and overload can be prevented by using the supply voltages as clipping levels [4]. If correctly scaled the combination of all these parameters will keep the system stable under all conditions. Another possibility is monitoring the integrator outputs and resetting them when necessary [4], but this takes extra circuitry. Note that the oversampling ratio does not affect the stability of the system, but only the resolution. This ratio is limited by the sampling frequency.

The quantiser levels are chosen at $\pm q/2=\pm V_{DD}/5$. The gain factor of the integrator preceding the quantiser does not change the behaviour of the system, so it can be chosen as well. It is set on $a_3=0.1$, in order to keep the integrator output range small and thus reduce the change on integrator overload. The only degrees of freedom left are gain factors a_1 and a_2, which will be determined by computer simulation. There are infinite possible combinations, so in order to limit the number of simulations a selection has to be made. Therefore all combinations of both a_1 and a_2 varying between 0.1 and 1 in steps of 0.1 will be simulated, thus one hundred possibilities. The possibility is high that this step size will provide a usable system, because sigma-delta modulators are relatively insensitive to deviations in the gain factors [4]. If these combinations of gain factors do not give an adequate result, a wider range will be simulated. Out of all the simulation results the most suitable ones are selected and tested on stability under all conditions.

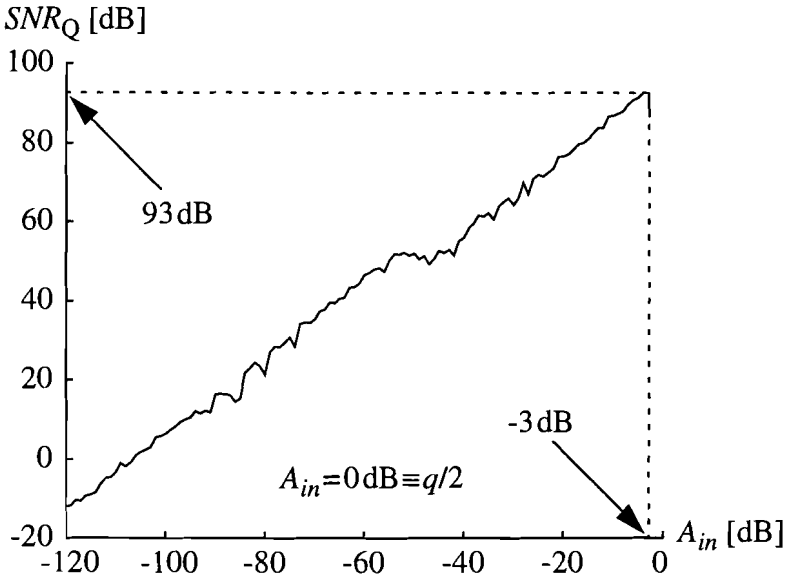

Figure 22. Signal-to-noise ratio characteristic of the third-order system.

The simulation results for the signal-to-noise ratio as function of the input signal amplitude, are shown in Fig.22. The integrator gain factors are determined to be a_1=0.8 and a_2=0.1, so $[a_1\ a_2\ a_3]$=[0.8 0.1 0.1]. The system achieves a maximum signal-to-noise-ratio of 93dB, equivalent to a resolution of 15.2bit, for a stable input range of $|x[n]| \leq 0.7q/2$ (σ=0.7). This leaves a 1.2bit margin to compensate for circuit limitations. The determined parameters offer the best possible compromise between signal-to-noise ratio and stability for all the parameter combinations simulated. This does not imply that there is not a better design possible, but determining this takes extensive computer simulations and at some point a choice has to be made. The simulations also show, that the sigma-delta modulator is relatively insensitive to relatively large variations in the integrator gain factors.

The determined set of parameters has one disadvantage, the output range of the integrators varies per integrator. It stays however always between the clipping levels, so in theory this is not relevant. In order not to overload the integrators in the real system their output range should be small, but for staying well above the circuit noise level it should be large. Scaling the integrator gain factors, in order to adjust their output range, changes the behaviour of the system. Therefore compensation gain factors are inserted in the feedback loops [4]. This is shown in Fig.23.

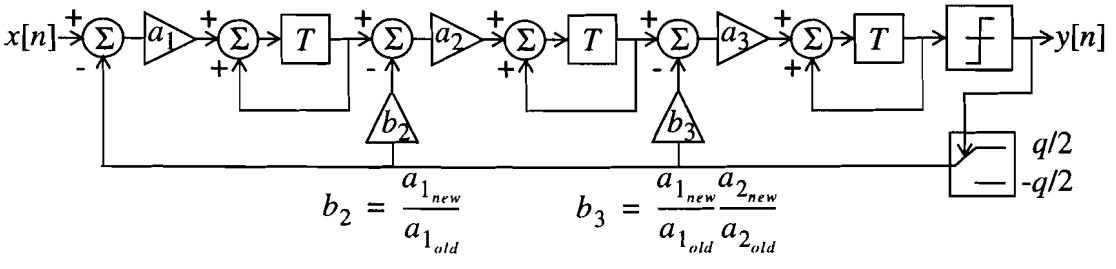

Figure 23. Third-order sigma-delta modulator with compensation gain factors.

Adjustments in a_1 and a_2 are compensated by b_2 and b_3, so the desired integrator output range can be set without changing the resolution of the system. Gain factor a_3 can be changed anyway, as long as the third integrator does not overload. This gives for the gain factors $[a_1\ a_2\ a_3\ b_2\ b_3]=[0.6\ 0.2\ 0.5\ 0.75\ 1.5]$. All integrator output ranges are in this case about $\pm 1.5q/2=\pm 0.3V_{DD}$. Computer simulations show that the signal-to-noise characteristic is unaffected by the changes. The resolution of the system has not changed, but this does not imply that the exact behaviour of the system and thus the stability under all conditions has not either. Stability due to non-zero initial state conditions and due to overload has to be verified again. Computer simulations show that the system is still stable under all conditions.

3.4. Translating the topology into a circuit implementation

Because the circuit design starts at this point, the specifications of chapter 1 become relevant. The implementation of the circuit depends for the application mainly on the character of the signal offered to the sigma-delta modulator. This is the output signal of the position-sensitive detector, which is a very small current. Converting this current to a voltage by means of a transimpedance amplifier, is a possibility to offer the signal to a switched-capacitor sigma-delta modulator. Switched-capacitor techniques are preferred for the implementation of sigma-delta modulators [4]. However, first converting takes extra circuitry and causes thus signal degradation. It is more advantageous to offer the current directly to the sigma-delta modulator. One possibility is the use of switched-current techniques [8], but regarding their state of development and the problems encountered in designs, this option is rejected. A better option is to offer the source current directly to a continuous-time sigma-delta modulator. Implementing the system with continuous-time circuitry has disadvantages, like degradation due to clock-jitter and high deviations in the fabricated time constants [9]. An advantage of continuous-time implementations is that some anti-alias filtering is achieved, without extra circuitry [9]. To combine the advantages of both, the system is chosen to be mixed continuous-time and switched-capacitor. Only the input is continuous-time and the remaining part of the circuit is in switched-capacitor form. Therefore the only mixed-mode element is the first integrator of the sigma-delta modulator. For now the implementation will be discussed for a single-ended circuit, but this can be extended to a differential implementation.

3.4.1. The first mixed-mode integrator

The first integrator of the sigma-delta modulator is shown in Fig.24. One input is a continuous-time current input, which receives the output current $i_d(t)$ of the position-sensitive detector. The other input is switched-capacitor voltage input, which receives the feedback voltage $v_{q/2}[n]$ of the quantiser. Note that the clock phases ϕ_1 and ϕ_2 are non-overlapping.

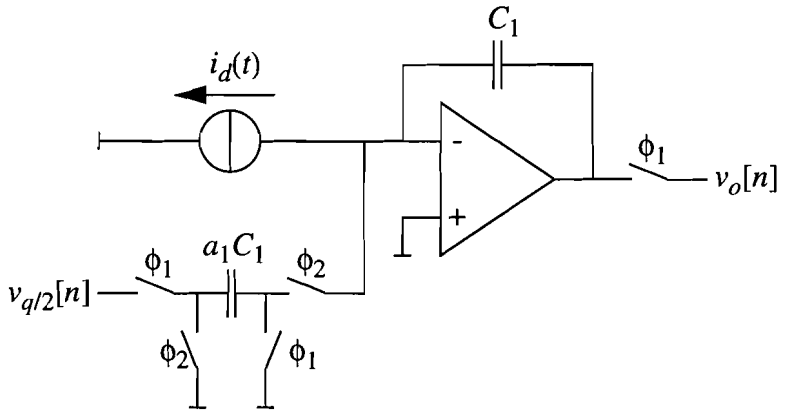

Figure 24. First integrator of the sigma-delta modulator.

The transfer of the input current to the output is determined by capacitor C_1. The output voltage of the integrator is sampled, so it is determined per sampling period $T_s=1/f_s$. The equation describing the output voltage at the end of clock phase ϕ_1 is

$$v_{o,i_d}(nT_s) = \frac{1}{C_1}\int_{[n-1]T_s}^{nT_s} i_d(t)dt + v_o([n-1]T_s) \tag{27}$$

Because the sampling frequency is much higher than the maximum signal frequency, the signal amplitude at two adjacent sample moments can be assumed equal, thus $i_d(nT_s) \approx i_d([n-1]T_s)$. With this assumption the output voltage at the end of clock phase $\phi_1$becomes

$$v_{o,i_d}(nT_s) \approx \frac{T_s}{C_1} i_d([n-1]T_s) + v_o([n-1]T_s) \tag{28}$$

Depending on the output of the quantiser, $v_{q/2}[n]$ has the value of one of the two quantiser levels $\pm q/2$. The transfer of the input voltage $v_{q/2}[n]$ to the output of the integrator is determined by the ratio of capacitors a_1C_1 and C_1. The difference equation describing the output voltage at the end of clock phase ϕ_1 is

$$v_{o,v_{q/2}}[n] = a_1 v_{q/2}[n-1] + v_o[n-1] \tag{29}$$

A condition for C_1 has to be derived, to proportionally relate the magnitude of the input current to the magnitude of the quantiser output voltage. Assume $i_{d,q/2}$ to be the value of the input current which is proportionally related to the quantiser output value $q/2$. Per sampling period both $i_{d,q/2}$ and $q/2$ have to be converted to a difference in the output voltage of $\Delta v_o[n]=a_1 q/2$, so for the value of C_1 can be derived

$$\frac{T_s}{C_1} i_{d,q/2} = a_1 \frac{q}{2} \Rightarrow C_1 = \frac{T_s i_{d,q/2}}{a_1 q/2} \tag{30}$$

The stable input range of higher-order sigma-delta modulators is $\pm\sigma q/2$, thus the input current range of the circuit is $\pm\sigma i_{d,q/2}$. With $i_{d,max}=\sigma i_{d,q/2}$ as the maximum allowed value of the input current the condition for the value of C_1 becomes

$$C_1 = \frac{T_s i_{d,max}}{\sigma a_1 q/2} \tag{31}$$

The switched-capacitor part of the integrator realises a forward-Euler integrator. For the continuous-time part a suitable transformation has to be found, in order to describe its discrete-time transfer function. In general the bilinear transformation is the most suitable for describing the discrete-time model of a continuous-time circuit [10]. However, for this application the value of the input current of two adjacent sample moments can be assumed equal. Therefore the applied transformation is not relevant, because in this case a forward-Euler transformation gives the same result as a bilinear transformation. For modelling the continuous-time part of the integrator, the forward-Euler transformation is taken. This was already implied in equation (28) and is in compliance with the topology of Fig.23. Combining equations (28), (29) and (31) gives for the complete difference equation of the first integrator

$$v_o[n] = a_1\left(\frac{\sigma q/2}{i_{d,max}} i_d[n-1] + v_{q/2}[n-1]\right) + v_o[n-1] \tag{32}$$

In this equation is $(\sigma q/2)/i_{d,max}$ a proportional current-to-voltage converting factor. This is useful for illustrative purposes, so the relation between the integrator gain factor a_1 and the input current $i_d[n-1]$ is clear in models of the sigma-delta modulator. In the z-domain the transfer function is

$$V_o(z) = \frac{a_1 z^{-1}}{1-z^{-1}}\left\{\frac{\sigma q/2}{i_{d,max}} I_d(z) + V_{q/2}(z)\right\} \tag{33}$$

3.4.2. The second and the third switched-capacitor integrators

Because of the specific character of the sigma-delta modulator input signal, the first integrator is a mixed-mode element. The following integrators are not directly connected to this signal, but to voltage outputs of the preceding integrators. Therefore they can be completely realised in switched-capacitor technology. Their configuration is shown in Fig.25.

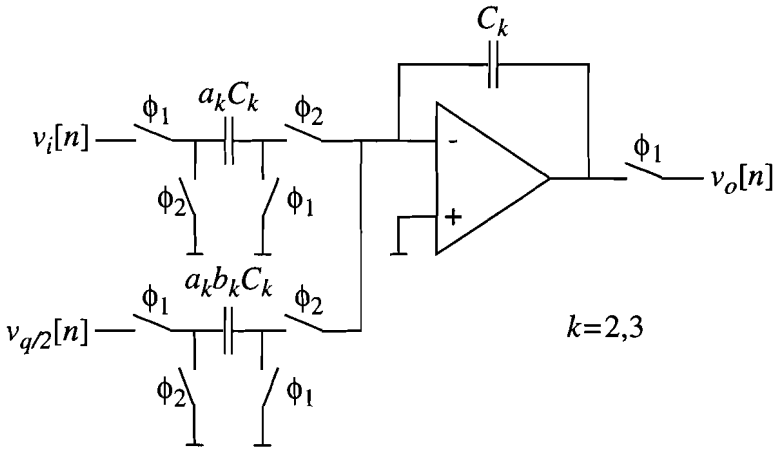

Figure 25. Second and third integrator of the sigma-delta modulator.

Input $v_i[n]$ receives the output voltage of the preceding integrator and input $v_{q/2}[n]$ receives the feedback voltage of the quantiser. The difference equation describing the output voltage at the end of clock phase ϕ_1 is

$$v_o[n] = a_k(v_i[n-1] + b_k v_{q/2}[n-1]) + v_o[n-1] \tag{34}$$

It is a forward-Euler integrator, which is in compliance with the topology of Fig.23. In the z-domain the transfer function is

$$V_o(z) = \frac{a_k z^{-1}}{1-z^{-1}}\{V_i(z) + b_k V_{q/2}(z)\} \tag{35}$$

3.4.3. Analogue-to-digital and digital-to-analogue converter

As previously mentioned, is the combination of the analogue-to-digital converter and digital-to-analogue converter regarded as the quantiser. Its input signal is continuous-amplitude and its output signal discrete-amplitude. Note that the digital output signal of the sigma-delta modulator is taken at the output of the analogue-to-digital converter. For a single-bit output format the analogue-to-digital converter is a comparator. Depending on its input signal, its output signal is a logical 0 or a logical 1. The digital-to-analogue converter converts these logical values to the analogue voltages they represent, the quantisation levels.

In Fig.24 and Fig.25 the output of the integrators is taken at clock phase ϕ_1, because they have to realise forward-Euler integrators. Therefore the timing of the quantiser has to be regarded very accurately, in order to realise the correct delay throughout the system. In the topology of Fig.23 is the delay from the output of the sigma-delta modulator, to the outputs of the integrators exactly one clock cycle. The

analogue-to-digital converter in the topology has no delay, so the delay to the output of the sigma-delta modulator is the same as to the output of the third integrator. Also the digital-to-analogue converter in the topology has no delay. In a circuit implementation however, the analogue-to-digital converter has a delay due to its required tracking and decision phases. Therefore the circuit has to be designed in such a way, that its transfer function is in compliance with the one of the topology. This is the case for the circuit in Fig.26.

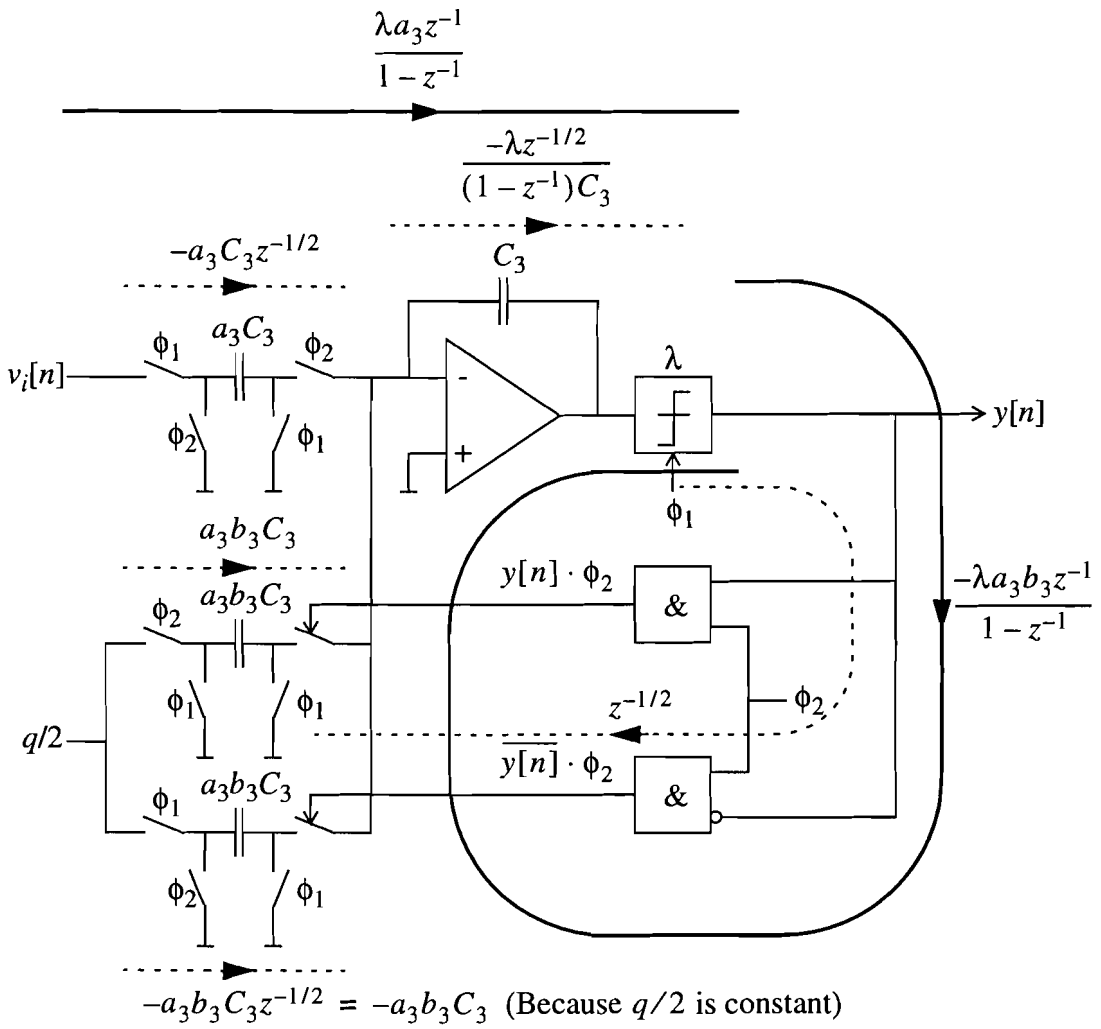

Figure 26. Delay of the third integrator in combination with the quantiser.

The quantiser tracks its input signal on clock phase ϕ_2, while holding its previous output value. On clock phase ϕ_1 the comparator decides, so the sample moment is at the end of this clock phase. For $v_i[n]$ to $y[n]$ is thus a forward-Euler integrator realised, which is in compliance with the topology. The capacitors connected to the constant reference voltage $q/2$ realise the quantisation levels $\pm q/2$. This reference source, together with the two clocked logical AND gates, realises the digital-to-analogue converter. This makes the total quantiser delay one clock phase, thus for the feedback of the sigma-delta modulator output signal an inverting forward-Euler integrator is realised. This is also in compliance with the topology. Note that for a logical 0 the value

$a_3b_3q/2$ is fed back to the system and for a logical 1 the value $-a_3b_3q/2$. Like in section 2.5 represents λ the non-linearity of the quantiser, which causes a quantisation error in the output signal of the third integrator. The total transfer function of Fig.26 in the z-domain is

$$Y(z) = \frac{\lambda a_3 z^{-1}}{(1-z^{-1}) + \lambda a_3 b_3 z^{-1}} V_i(z) \tag{36}$$

This results is basically a first-order sigma-delta modulator, which is in compliance with equation (22) for $L=1$ and $b_3=1$. Note that in this equation the format of $Y(z)$ is not relevant, but the represented quantiser level is.

3.5. The complete circuit

After determining the elements of the circuit, they can be combined to make up the sigma-delta modulator. At this point a single-ended circuit is discussed, but it can be extended to a differential circuit.

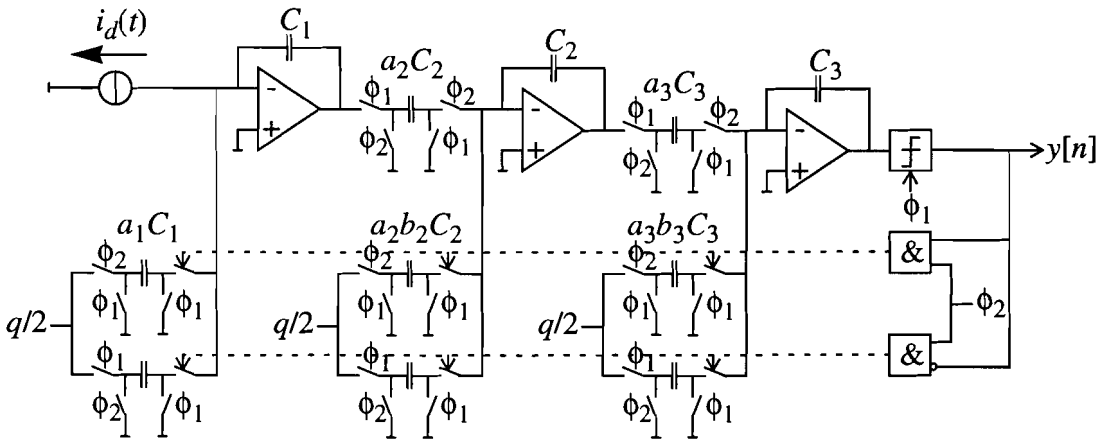

Figure 27. Simplified circuit of the third-order sigma-delta modulator.

The switched-capacitor reference source is repeated for each integrator, in order to realise the correct gain factors for each integrator input. The reference sources and the clocked logical AND gates form the digital-to-analogue converter and this in combination with the comparator is the quantiser. Of course it is only a matter of definition, so the comparison between theory, topology and circuit implementation is clear.

3.6. Summary

The topology of the sigma-delta modulator is a basic third-order one, with a single-bit output format. Its resolution can be approximated by calculation, but especially in the single-bit case this is inaccurate. Therefore the resolution is optimised by high-level computer simulations, which make it also possible to determine if the system is stable under all conditions. In this stage some circuit specifications are already relevant.

The circuit implementation has to realise exactly the same transfer function as the topology. Therefore the timing throughout the circuit has to be carefully designed. The circuit given is a simplification of the one that will actually be implemented, but its basic operation is the same.

The first integrator has a continuous-time current input and a switched-capacitor voltage input. The capacitors of the first integrator are fixed, due to the topology parameters and the specified maximum input current of the sigma-delta modulator. The integrator gain factor and the sampling frequency are the topology parameters, which determine in combination with the maximum input current the value of the feedback capacitor and thus also the value of the switched-capacitor. Therefore the only degree of freedom during the circuit design of the first integrator, is its operational amplifier.

The second and the third integrator are completely realised in switched-capacitor technology. Therefore their capacitor values can be freely chosen, as long as the capacitor ratios are equal to the corresponding gain factors in the topology.

4. THE EFFECT OF CIRCUIT LIMITATIONS

In this chapter the effect of circuit limitations on the performance of the sigma-delta modulator is analysed. The analysis differs for every design, because it depends mainly on the specific circuit implementation. Whenever possible the effect of the circuit limitations is calculated, but in several cases it can only be determined by computer simulation. Limitations that can be calculated will during the circuit design be used to set specifications. Limitations that can not be calculated accurately are modelled. After circuit design the models will be used to evaluate the system. Because not every circuit limitation can be taken into account, only the most relevant ones are discussed.

4.1. Limitations due to circuit noise

Except the quantisation noise, also the circuit noise limits the resolution of a sigma-delta modulator. Circuit noise added somewhere after the first integrator is shaped in a similar way as the quantisation noise [11]. If the circuit noise is added directly after the first integrator it undergoes a first-order noise-shaping function, if it is added directly after the second integrator it undergoes a second-order noise-shaping function and so on. Therefore their contributions are assumed negligible and only the contribution of the first integrator and its input circuitry is relevant. In Fig.28 the first integrator with relevant noise sources is shown. For this analysis the capacitance C_d of the position-sensitive detector has to be taken into account. The displayed noise sources are the operational amplifier noise $v_{n,OA}$, the switched-capacitor noise $v_{n,SC}$ and the reference voltage source noise $v_{n,q/2}$. Their contribution can be represented by an equivalent noise source $i_{n,\,eq_c}$ at the input of the sigma-delta modulator.

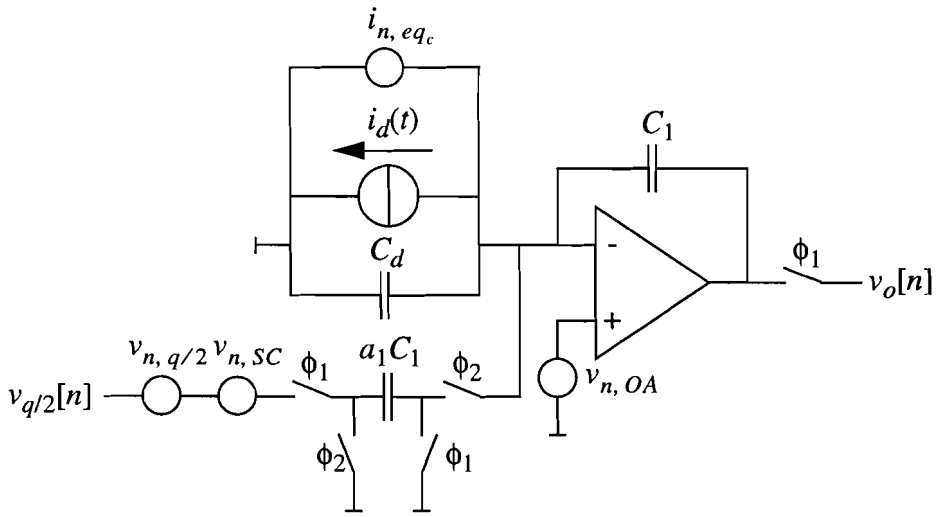

Figure 28. First integrator with noise sources and equivalent input noise source.

4.1.1. Noise contribution of the operational amplifier

The noise of the operational amplifier consists of two parts, white noise and $1/f$ noise [12]. The power spectral density of the equivalent input noise source $v_{n,OA}$ is thus

$$S^2_{n,\,OA}(f) = \gamma_{OA} + \frac{\zeta_{OA}}{f} \tag{37}$$

The noise behaviour of this configuration is analysed per clock phase, which is illustrated in Fig.29. Note that also the input capacitor a_2C_2 of the second integrator is displayed, because it is relevant for the analysis. Voltage source $v_{q/2}[n]$ is assumed to have the value of the positive quantiser level $q/2$.

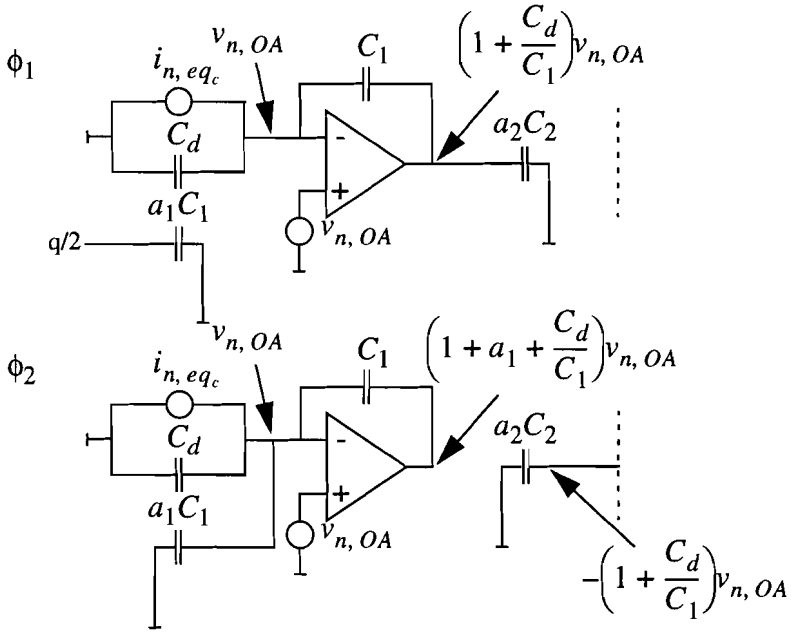

Figure 29. Noise analysis of the first integrator per clock phase.

Due to capacitance C_d this configuration is during clock phase ϕ_1 an amplifier for $v_{n,OA}$, with an amplification of $1+C_d/C_1$. To calculate the equivalent input noise, the operational amplifier noise is first continuous-time amplified to the output of the integrator and after that continuous-time differentiated to the input of the sigma-delta modulator. The power spectral density of the equivalent input noise source during this clock phase is thus

$$S^2_{n,\,eq_{OA,\phi_1}}(f) = \frac{\left(1+\frac{C_d}{C_1}\right)^2}{\left|\frac{1}{j2\pi f C_1}\right|^2} S^2_{n,\,OA}(f) \tag{38}$$

During clock phase ϕ_2 this configuration is again an amplifier for $v_{n,OA}$, with an amplification of $1+a_1+C_d/C_1$. The power spectral density of the equivalent input noise source during this clock phase is thus similar to equation (38)

$$S^2_{n,\,eq_{OA,\phi_2}}(f) = \frac{\left(1+a_1+\frac{C_d}{C_1}\right)^2}{\left|\frac{1}{j2\pi f C_1}\right|^2} S^2_{n,\,OA}(f) \tag{39}$$

During the operation of the sigma-delta modulator the output noise of the integrator on clock phase ϕ_1 is sampled by capacitor a_2C_2. Because of the sampling all the noise power folds into a bandwidth from DC to $f_s/2$. However, it can be regarded as an additive noise source directly after the first integrator. Therefore its spectral density is shaped with a first-order noise-shaping function and thus is its contribution assumed negligible. Note that folding of $1/f$ noise is negligible anyway, because it has a very low bandwidth compared to the sampling frequency [13]. If the operational amplifier is assumed ideal, $v_{n,OA}$ also appears on its inverting input terminal [12]. During clock phase ϕ_2 capacitor a_1C_1 samples this noise, but the voltage over this capacitor becomes $q/2$ in clock phase ϕ_1 and the noise has thus no effect. The total equivalent input noise power spectral density is the average of the ones on both clock phases [13]

$$S^2_{n,\,eq_{OA}}(f) = \frac{1}{2}S^2_{n,\,eq_{OA,\phi_1}}(f) + \frac{1}{2}S^2_{n,\,eq_{OA,\phi_2}}(f) \tag{40}$$

With equations (37), (38) and (39) this becomes

$$S^2_{n,\,eq_{OA}}(f) = 2\pi^2\{[C_d+C_1]^2+[C_d+(1+a_1)C_1]^2\}\{\gamma_{OA}f^2+\zeta_{OA}f\} \tag{41}$$

It is obvious that the capacitance of the position-sensitive detector causes an increase in equivalent input noise. The only way to decrease the noise contribution of the operational amplifier is its design, because a_1 and C_1 are already determined by the topology and the maximum input current of the sigma-delta modulator.

4.1.2. Noise contribution of the switched-capacitor input

The noise added by a switched-capacitor depends on the value of its capacitance. Switched-capacitor a_1C_1 in Fig.28 sees two switch paths per clock cycle and therefore its noise variance or noise power is [14]

$$\overline{v^2_{n,\,SC}} = \frac{2k_bT_{emp}}{a_1C_1} \tag{42}$$

It is assumed that due to the sampling process this noise power is uniformly distributed over a bandwidth from DC to $f_s/2$, so its spectral density is

$$S^2_{n,SC}(f) = \frac{4k_bT_{emp}}{a_1C_1f_s} \tag{43}$$

To calculate the equivalent input noise, the switched-capacitor noise is first discrete-time integrated to the output of the integrator and after that continuous-time differentiated to the input of the sigma-delta modulator. The discrete-time integration is approximated by

$$z = e^{j\theta} \quad , \quad \theta = \frac{2\pi f}{f_s} \Rightarrow \frac{a_1z^{-1}}{1-z^{-1}} = \frac{e^{-j\theta/2}}{j2\sin(\theta/2)} \approx \frac{1}{j2\pi fT_s} \quad ,f_s \gg f_b \tag{44}$$

The power spectral density of the equivalent input noise source becomes in this case

$$S^2_{n,eq_{SC}}(f) = \frac{\left|\frac{a_1}{j2\pi fT_s}\right|^2}{\left|\frac{1}{j2\pi fC_1}\right|^2} S^2_{n,SC}(f) = 4k_bT_{emp}a_1C_1f_s \tag{45}$$

The contribution of this noise source can not be decreased, because a_1 and C_1 are already determined by the topology and the maximum input current of the sigma-delta modulator. The sampling frequency can not be decreased, because this will decrease the resolution of the system.

4.1.3. Noise contribution of the reference voltage source

Reference voltage source $v_{q/2}[n]$ in Fig. 28 adds white and $1/f$ noise to the circuit, so the noise power spectral density is

$$S^2_{n,q/2}(f) = \gamma_{q/2} + \frac{\zeta_{q/2}}{f} \tag{46}$$

The noise is sampled by switched-capacitor a_1C_1, so its total noise power is folded into a bandwidth from DC to $f_s/2$. The noise power spectral density becomes then

$$S^{2^{sampled}}_{n,q/2}(f) = \frac{2BW_{n,q/2}}{f_s}\gamma_{q/2} + \frac{\zeta_{q/2}}{f} \tag{47}$$

In this equation is $BW_{n,q/2}$ the bandwidth of the white noise which is folded, so $2BW_{n,q/2}/f_s$ is the number of times the white noise contribution increases. Note that the

$1/f$ noise is not folded, because its bandwidth is very low compared to the sampling frequency. To calculate the equivalent input noise, the reference source noise is first discrete-time integrated to the output of the integrator and after that continuous-time differentiated to the input of the sigma-delta modulator. The power spectral density of the equivalent input noise source is thus

$$S^2_{n,\,eq_{q/2}}(f) = \frac{\left|\frac{a_1}{j2\pi f T_s}\right|^2}{\left|\frac{1}{j2\pi f C_1}\right|^2} S^{2^{sampled}}_{n,\,q/2}(f) = 2a_1^2 C_1^2 f_s BW_{n,\,q/2}\gamma_{q/2} + \frac{a_1^2 C_1^2 f_s^2 \zeta_{q/2}}{f} \quad (48)$$

The only way to decrease the noise contribution of the reference voltage source is its design. Its noise power spectral density and its noise bandwidth have to be low. Decreasing the sampling frequency is not an option and a_1 and C_1 are determined by the topology and the maximum input current of the sigma-delta modulator.

4.1.4. Total circuit noise contribution of the first integrator

The total equivalent input circuit noise power spectral density of the first integrator, is the sum of equations (41), (45) and (48)

$$S^2_{n,\,eq_c}(f) = S^2_{n,\,eq_{OA}}(f) + S^2_{n,\,eq_{SC}}(f) + S^2_{n,\,eq_{q/2}}(f) \quad (49)$$

The input signal of the sigma-delta modulator is an AM modulated signal, with a carrier frequency of f_C=1 kHz and a modulating bandwidth of f_m=200 Hz. After AM demodulation the total noise power from f_c-f_m to f_c+f_m appears in the base band from DC to f_m [15]. Therefore the relevant circuit noise power is

$$\overline{i^2_{n,\,eq_c}} = \int_{f_c - f_m}^{f_c + f_m} S^2_{n,\,eq_c}(f)\,df \quad (50)$$

The circuit noise power adds to the quantisation noise power of the sigma-delta modulator, so the signal-to-noise ratio of the system decreases. This will be discussed further on in section 4.4, when all noise sources are determined.

4.2. Limitations due to the operational amplifiers in the circuit

For the high-level simulations of the sigma-delta modulator topology in section 3.3, ideal integrator models are used. Mainly because of its non-ideal operational amplifier

the behaviour of a real integrator differs from its ideal model. Therefore the influence of the operational amplifiers in the circuit has to be examined, in order to determine their required specifications. It is not possible to accurately calculate the consequences of every operational amplifier non-ideal effect on the performance of the sigma-delta modulator. Therefore these effects will be modelled in its topology, of which the performance is again verified by high-level computer simulations.

4.2.1. Finite amplifier DC gain

Due to the finite DC gain of an operational amplifier, a fraction of its output voltage is reflected to its input terminals [12]. Therefore the inverting input terminal does not behave as a virtual ground, when the non-inverting input terminal is connected to ground. The consequences will be discussed for a switched-capacitor and a continuous-time integrator. In Fig.30 a non-inverting switched-capacitor integrator with a finite DC gain operational amplifier is shown.

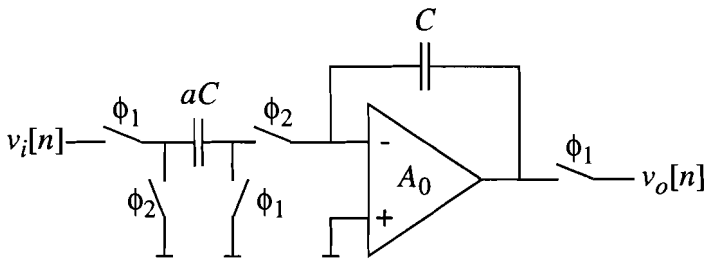

Figure 30. Switched-capacitor integrator with finite DC gain operational amplifier.

The difference equation describing the output voltage at the end of clock phase ϕ_1 is

$$v_o[n] = a\frac{A_0}{A_0+1+a}v_i[n-1] + \frac{A_0+1}{A_0+1+a}v_o[n-1] \tag{51}$$

For $A_0 \gg 1$ this becomes

$$v_o[n] = a\left(1-\frac{1+a}{A_0}\right)v_i[n-1] + \left(1-\frac{a}{A_0}\right)v_o[n-1] \tag{52}$$

With $\varepsilon_{A_1} = (1+a)/A_0$ and $\varepsilon_{A_2} = a/A_0$, the transfer function in the z-domain is

$$\frac{V_o(z)}{V_i(z)} = \frac{a(1-\varepsilon_{A_1})z^{-1}}{1-(1-\varepsilon_{A_2})z^{-1}} \tag{53}$$

Error ε_{A_1} causes a linear deviation in the integrator gain factor a. Like previously mentioned is the performance of sigma-delta modulators not severely affected by relatively large linear integrator gain errors. Error ε_{A_2} causes a linear deviation of the feedback factor from unity, which causes the pole of the integrator to shift from $z_p=1$ to $z_p=1-\varepsilon_{A_2}$. Because of this the integrator gain decreases for low frequencies, so according to equation (8) the system suppresses less quantisation noise from the signal band. The ideal quantisation noise spectral density of the sigma-delta modulator shown in Fig.9, has an L-fold zero at $z_z=1$. This L-fold zero is determined by the poles of the L ideal integrators in the system, thus every integrator pole causes a matching zero at the same frequency. If an integrator pole shifts from $z_p=1$ to $z_p=1-\varepsilon_{A_2}$, its matching zero shifts from $z_z=1$ to $z_z=1-\varepsilon_{A_2}$. In the f-domain the zeros shift from $f_z=0$ to $f_z \approx \varepsilon_{A_2} f_s/2\pi$. The increase in quantisation noise is negligible if the zeros are well below the maximum signal band frequency f_b [4], so the condition for the minimum value of the amplifier DC gain of each integrator is

$$\frac{\varepsilon_{A_2} f_s}{2\pi} \ll f_b \Rightarrow A_0 \gg \frac{a}{\pi} \frac{f_s}{2f_b} = \frac{a}{\pi} D \tag{54}$$

The impact of finite operational amplifier DC gain can not be accurately calculated, so it has to be simulated. Simulations show that if $A_0 \geq D$, the increase of quantisation noise power in the signal band is negligible [16]. Both errors can be modelled like shown in Fig.31, with $\alpha_{A_1}=1-\varepsilon_{A_1}$ and $\alpha_{A_2}=1-\varepsilon_{A_2}$.

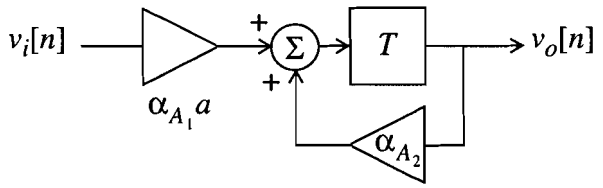

Figure 31. Switched-capacitor integrator model for finite amplifier DC gain.

The analysis of the continuous-time integrator is similar to the one in section 3.4.1, but now the finite DC gain of the operational amplifier is taken into account. In Fig.32 is a continuous-time integrator with a finite DC gain operational amplifier shown.

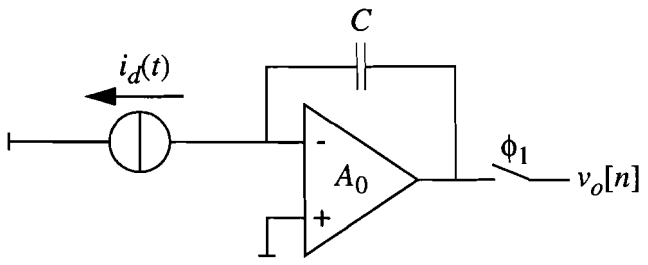

Figure 32. Continuous-time integrator with finite DC gain operational amplifier.

The equation describing the output voltage at the end of clock phase ϕ_1 is

$$v_o(nT_s) = \frac{1}{1+1/A_0}\frac{1}{C}\int_{[n-1]T_s}^{nT_s} i_d(t)dt + v_o([n-1]T_s) \tag{55}$$

With $i_d(nT_s) \approx i_d([n-1]T_s)$ and $A_0 \gg 1$ this becomes

$$v_o(nT_s) = \left(1-\frac{1}{A_0}\right)\frac{T_s}{C} i_d([n-1]T_s) + v_o([n-1]T_s) \tag{56}$$

The difference equation describing the output voltage at the end of clock phase ϕ_1 is

$$v_o[n] = \left(1-\frac{1}{A_0}\right)\frac{T_s}{C} i_d[n-1] + v_o[n-1] \tag{57}$$

With $\varepsilon_{A_3} = 1/A_0$ the transfer function in the z-domain is given by

$$\frac{V_o(z)}{I_d(z)} = \frac{T_s}{C}\frac{(1-\varepsilon_{A_3})z^{-1}}{1-z^{-1}} = \frac{\sigma q/2}{i_{d,max}}\frac{a(1-\varepsilon_{A_3})z^{-1}}{1-z^{-1}} \tag{58}$$

Note that the gain factor for converting the input current to a proportional voltage is present. The continuous-time integrator has a linear error in its gain factor, which will not severely affect the behaviour of the sigma delta modulator. Because the errors caused by the switched-capacitor integrator are more severe than the errors caused by the continuous-time integrator, the model of Fig. 31 will be used to model the entire first integrator of the sigma-delta modulator. Because the second and the third integrator are completely in switched-capacitor technology, this model also applies to them.

Finite integrator DC gain also causes so called low signal-level distortion [4]. This is basically cross-over distortion due to the threshold discussed in section 2.4, which is now regarded for DC input signals. The minimum required value of the total amplifier gain product in the forward path of the sigma-delta modulator, depends on its required resolution. For an Lth-order sigma-delta modulator, the condition for the DC gain of every operational amplifier is given by [4]

$$A_0 \geq 2^{N/L} \tag{59}$$

4.2.2. Non-linear amplifier DC gain

An integrator introduces harmonic distortion due to the non-linear DC gain of its operational amplifier. In order to determine the harmonic distortion of the sigma-delta

modulator caused by this, the contribution of every integrator has to be analysed. The first integrator is shown in Fig.33, with a non-linear DC gain operational amplifier.

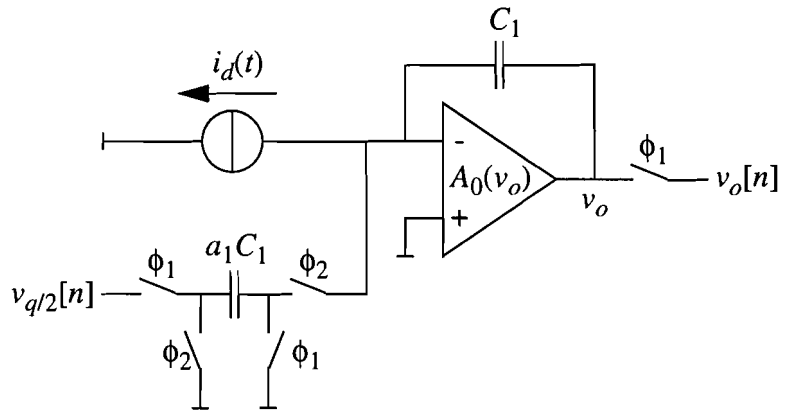

Figure 33. First integrator with non-linear DC gain operational amplifier.

If the switched-capacitor input is omitted, the equation describing the output voltage at the end of clock phase ϕ_1 is similar to equation (56)

$$v_o(nT_s) = \left(1 - \frac{1}{A_0(v_o)}\right)\frac{T_s}{C_1} i_d([n-1]T_s) + v_o([n-1]T_s) \tag{60}$$

If $v_{o,hd}(nT_s)$ is defined as the harmonic distortion at the output of the integrator, this equation can be rewritten as

$$\begin{aligned} v_o(nT_s) &= \frac{T_s}{C_1} i_d([n-1]T_s) + v_o([n-1]T_s) + v_{o,\,hd}(nT_s) \\ v_{o,\,hd}(nT_s) &= -\frac{1}{A_0(v_o)}\frac{T_s}{C_1} i_d([n-1]T_s) \end{aligned} \tag{61}$$

The DC gain of the operational amplifier can as a function of its output voltage be approximated by a polynomial. This polynomial and its inverse are given by

$$A_0(v_o) \approx \sum_{l=0}^{m} \alpha_l v_o^l \quad , \quad \frac{1}{A_0(v_o)} \approx \sum_{l=0}^{m} \beta_l v_o^l \tag{62}$$

With the inverse polynomial, the distortion component can be written as

$$v_{o,\,hd}(nT_s) = -\left\{\sum_{l=0}^{m} \beta_l v_o^l(nT_s)\right\}\frac{T_s}{C_1} i_d([n-1]T_s) \tag{63}$$

The input signal of the first integrator is the difference between the input signal of the sigma-delta modulator and a previous value of it, with a quantisation noise term added. Apart from the quantisation noise term, this can be regarded as a differentiated version of the sigma-delta modulator input signal. The output signal of the first integrator is thus the sigma-delta modulator input signal, multiplied by the integrator gain factor and again with a quantisation noise term added. It is assumed that only a sinusoidal signal $i_{d,sin}[n]$ is present at the input of the sigma-delta modulator and that cross products between the sinusoidal signal and the quantisation give negligible contributions to harmonic distortion [17]. The harmonic distortion is thus entirely determined by the sinusoidal part of the integrator output signal, thus the input signal of the sigma-delta modulator multiplied by the integrator gain factor. The difference equation of the harmonic distortion due to the first integrator is in this case given by

$$v_{o,hd}[n] = -\sum_{l=0}^{k} \beta_l \left(\frac{T_s}{C_1} i_{d,sin}[n-1] \right)^{l+1} \tag{64}$$

In Fig. 34 the harmonic distortion due to the first integrator is modelled. Note that the lower gain factor is only present to convert the input current to a proportional voltage.

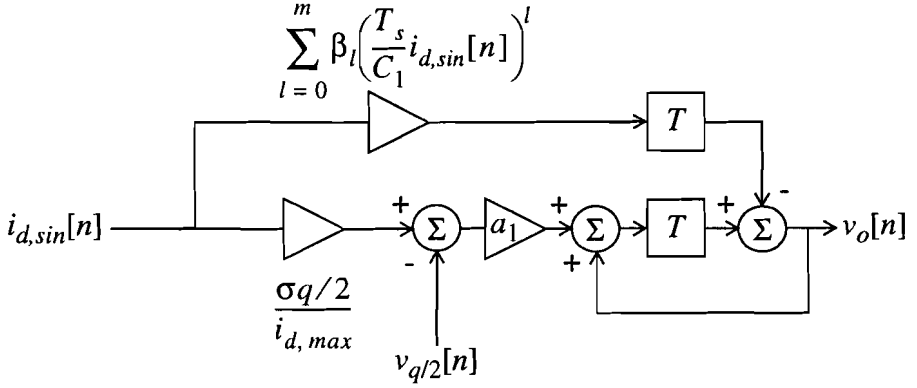

Figure 34. Model of the first integrator harmonic distortion.

The second and the third integrator of the sigma-delta modulator cause also harmonic distortion, but their non-linearity is attenuated by the gain product of the preceding integrator(s) [18]. Therefore their harmonic distortion is negligible, so the harmonic distortion of the sigma-delta modulator is completely determined by its first integrator.

4.2.3. Finite amplifier gain bandwidth product and slew rate

Due to its finite gain bandwidth product and slew-rate, the settling of an operational amplifier is non-ideal. Therefore also the settling of the integrators in the sigma-delta modulator is. The given analysis provides specifications for the design, but the exact performance has to be verified by high-level computer simulations afterwards.

4.2.3.1. Finite gain bandwidth product

This analysis concentrates for now, on the relation between the gain bandwidth product *GBW* of the first integrator and the capacitance of the position-sensitive detector C_d. Because on clock phase ϕ_2 the integrator input changes abruptly, the settling on this clock phase critical. The first integrator on clock phase ϕ_2 is shown in Fig.35.

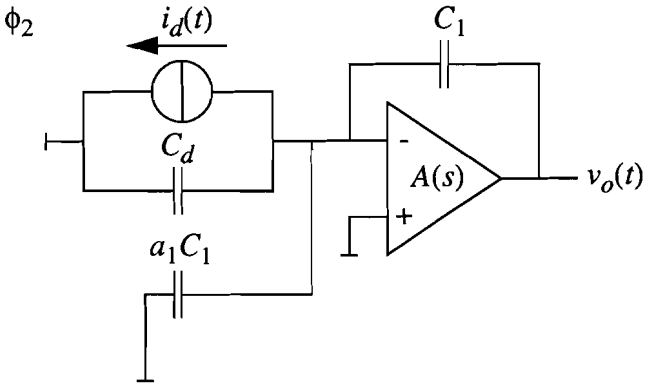

Figure 35. First integrator on clock phase ϕ_2.

For the operational amplifier a single-pole model with DC gain A_0, time-constant $\tau_{p_{OA}}$ and ideal input and output impedances is assumed

$$A(s) = \frac{A_0}{1 + s\tau_{p_{OA}}} \tag{65}$$

The transfer function of the integrator in the *s*-domain on clock phase ϕ_2, can be determined with basic feedback analysis [19]

$$\frac{V_o(s)}{I_d(s)} = \frac{-1}{s\left[C_1 + \frac{C_d + (1 + a_1)C_1}{A_0}(1 + s\tau_{p_{OA}})\right]} \tag{66}$$

The pole frequencies determined with the denominator of this equation are

$$f_{p_1} = 0 \ , \ f_{p_2} = \frac{1}{2\pi\tau_{p_{OA}}}\frac{1}{\left[1 + \frac{A_0C_1}{C_d + (1 + a_1)C_1}\right]} \tag{67}$$

The second pole is determined by the time constant of the non-ideal operational amplifier, which has the following relation with the gain bandwidth product [12]

$$\tau_{p_{OA}} = \frac{A_0}{2\pi GBW} \tag{68}$$

The gain bandwidth product depends on the design of the operational amplifier and its configuration in the circuit. Substituting the time-constant in equation (67) gives for the second pole frequency of the integrator

$$f_{p_2} = \frac{GBW}{A_0}\left[1 + \frac{A_0 C_1}{C_d + (1 + a_1)C_1}\right] \approx GBW \frac{C_1}{C_d + (1 + a_1)C_1} \quad , A_0 \gg 1 \qquad (69)$$

The settling time of the integrator is determined by the time-constant $\tau_{p_2} = 1/2\pi f_{p_2}$ of the second pole. Input current $i_d(t)$ does not suddenly change, but the voltage over capacitor $a_1 C_1$ does on clock phase ϕ_1, with magnitude q of the quantisation step. The exponential settling [12] of the maximum integrator output step is thus given by

$$|\Delta v_o(t)| = a_1 q(1 - e^{-t/\tau_{p_2}}) = a_1 q(1 - e^{-2\pi f_{p_2} t}) \qquad (70)$$

The voltage which is taken from the integrator output on clock phase ϕ_1, is the same as the output voltage at the end of clock phase ϕ_2. The on-time of clock-phases ϕ_1 and ϕ_2 is respectively T_{ϕ_1} and T_{ϕ_2}, with $T_{\phi_1} = T_{\phi_2} < T_s/2$. The integrator has to settle within clock phase ϕ_2 in a time T_{ϕ_2}, so it settles at

$$|\Delta v_o(t)| = a_1 q(1 - e^{-2\pi f_{p_2} T_{\phi_2}}) = a_1 q(1 - \varepsilon_{GBW}) \qquad (71)$$

If in this equation the pole frequency and the on-time of clock phase ϕ_2 are both assumed constant, a finite gain bandwidth product gives a linear settling error ε_{GBW} in the integrator gain factor of the feedback signal $v_{q/2}[n]$. This error can be modelled in the sigma-delta modulator as shown in Fig.36, with $\alpha_{GBW} = 1 - \varepsilon_{GBW}$.

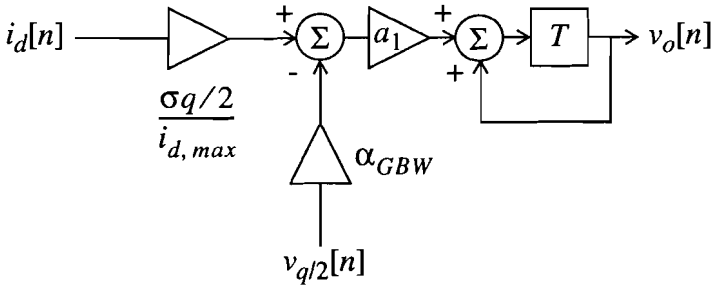

Figure 36. Model of the error due to finite gain bandwidth product.

This can be regarded as an error in the unity-gain feedback of $v_{q/2}[n]$, which causes an error in the difference between the input and the feedback signal. This error thus affects the proportionality between the input signal and the output signal of the sigma-delta modulator. Therefore its effect on the performance has to be determined after the circuit design. Note that the left gain factor converts the input current to a proportional voltage. The settling of the second and third integrator does not depend on the capacitance of the position-sensitive detector. Their settling will be discussed further on, during the circuit design.

4.2.3.2. Finite slew rate

If the derivative of equation (70) is higher than the slew rate of the operational amplifier, slew rate limitation occurs. The output voltage of the integrator rises linearly to a transition point, where the slew rate and the recalculated derivative of equation (70) are equal. From this point on the settling continuous exponential. The derivative of equation (70) is recalculated, to make the transition from slew rate limited to exponential settling is continuous. If Δv_o is the step at integrator output, the settling error due to slew rate limitations at the end of clock phase ϕ_2 is [20]

$$\varepsilon_{SR} = \tau_{p_2} SR e^{-\left(\frac{T_{\phi_2}}{\tau_{p_2}} - \frac{\Delta v_o}{\tau_{p_2} SR} + 1\right)} \quad ,\tau_{p_2} SR < \Delta v_o \tag{72}$$

The step at he output of the integrator is the quantisation error multiplied by the integrator gain factor, which is assumed uncorrelated with the input signal of the sigma-delta modulator. Therefore the settling error due to slew rate limitations can also be assumed uncorrelated with the input signal of the sigma-delta modulator [20]. If $\varepsilon_{SR,max}$ is the maximum settling error due to slew rate limitation, the maximum voltage step $\Delta v_{o,max}$ is present at the output of the integrator. If it is assumed that the settling error is uniformly distributed over the interval $[-\varepsilon_{SR,max}, \varepsilon_{SR,max}]$, the settling error can be regarded as a noise source with power

$$\overline{v_{n,SR}^2} = \frac{1}{2\varepsilon_{SR,max}} \int_{-\varepsilon_{SR,max}}^{\varepsilon_{SR,max}} \varepsilon_{SR}^2 d\varepsilon_{SR} = \frac{\varepsilon_{SR,max}^2}{3} \tag{73}$$

If this noise power is assumed uniformly distributed over a bandwidth from DC to $f_s/2$, its spectral density is

$$S_{n,SR}^2(f) = \frac{2}{3} \frac{\varepsilon_{SR,max}^2}{f_s} \tag{74}$$

It is an additive noise source, shown in Fig. 37, at the output of the operational amplifier. This implies that it is not negligible, because its spectral density is not shaped with a first-order noise-shaping function, like it would be directly after the first integrator.

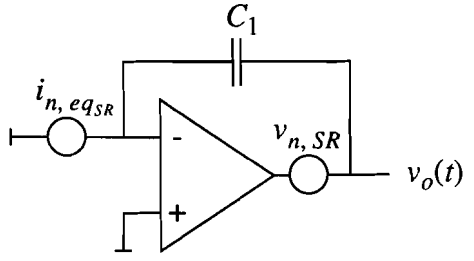

Figure 37. First integrator with slew rate noise source.

The noise source at the output of the operational amplifier can be transformed to an equivalent input noise current $i_{n,\,eq_{SR}}$, at the input of the sigma-delta modulator. By differentiating the noise power at the output of the operational amplifier continuous-time to the input of the sigma-delta modulator, the power spectral density of the equivalent noise current becomes

$$S^2_{n,\,eq_{SR}}(f) = \frac{S^2_{n,\,SR}(f)}{\left|\frac{1}{j2\pi f C_1}\right|^2} = \frac{8\pi^2 \varepsilon^2_{SR,\,max} C_1^2}{3 f_s} f^2 \tag{75}$$

The only possibility to lower the noise due to slew rate limitation is the design of the operational amplifier. The sampling frequency and capacitor C_1 are determined by the topology and the maximum input current of the sigma-delta modulator, so changing them is not an option. Note that according to equation (72) changing the sampling frequency changes the settling error, because $T_{\phi_2} \approx T_s/2$.

After AM demodulation only the bandwidth from f_c-f_m to f_c+f_m is relevant for the noise contribution, like in case of the circuit noise. Therefore the equivalent input noise power due to slew rate limitations is

$$\overline{i^2_{n,\,eq_{SR}}} = \int_{f_c - f_m}^{f_c + f_m} S^2_{n,\,eq_{SR}}(f)\,df \tag{76}$$

The noise power due to slew rate limitations adds to the circuit noise power and the quantisation noise power, so the signal-to-noise ratio of the system decreases. This will be discussed further on in section 4.4, when all noise sources are determined. The slew rate related equivalent input noise sources of the second and third integrator are assumed negligible, because their spectral densities are noise-shaped.

4.3. Jitter of the sampling clock

The sampling clock has some jitter, so the sampling moments are not equidistant in time. Their time uncertainty causes an error during the sampling of an analogue signal, which appears as so called aperture noise [4]. In this design the sampling of the analogue signal occurs directly after the first integrator. The signal-to-noise ratio due to aperture noise can for the output signal of the first integrator be calculated as

$$SNR_A = 10 \times \log_{10}\left[\frac{1}{4\pi^2 f_b^2 \sigma^2(\Delta T)}\right] \tag{77}$$

In this equation is $\sigma(\Delta T)$ the standard deviation of the clock uncertainty, for which relatively large values are acceptable. For example, the condition for $SNR_A \geq 100$dB is

$\sigma(\Delta T) \leq 1.3\text{ns}$. The aperture noise is assumed negligible, because its power spectral density is shaped with a first-order noise-shaping function. This assumption is justified by the large clock uncertainty, that would even without noise-shaping be acceptable.

A switched-capacitor circuit is insensitive to sampling clock jitter, because the charge transferred during one clock phase is independent of its on-time [4]. The switched-capacitor input of the first integrator and the other switched-capacitor elements are thus not affected by sampling clock jitter.

4.4. The total noise of the sigma-delta modulator

It can be concluded that the circuit noise and the settling noise due to slew rate limitations are the relevant noise courses, besides the quantisation noise. The sum of the powers of these three noise sources in the band of interest determines the achievable resolution of the sigma-delta modulator. The power of the circuit noise and the settling noise is given by equations (50) and (76). They are both determined for the bandwidth from f_c-f_m to f_c+f_m, which is relevant after AM demodulation. This also applies for the quantisation noise. The topology of the sigma-delta modulator was designed to achieve the specified resolution for a bandwidth from DC to f_b=f_c+f_m, but the quantisation noise contribution up to f_c-f_m is negligible compared to the contribution in the band of interest. The oversampling ratio and the order of the sigma-delta modulator are thus not chosen unnecessarily high, so the margin left for circuit limitations is the 7dB determined in section 3.3. In that section the maximum signal-to-noise ratio due to quantisation noise was determined for a maximum input signal amplitude $i_{d,max}$. A good approximation for the quantisation noise power in the band of interest is thus

$$\overline{i_{n,Q}^2} = \frac{i_{d,max}^2/2}{10^{SNR_Q/10}} \tag{78}$$

The total noise power can now be calculated with equations (50), (76) and (78)

$$\overline{i_n^2} = \overline{i_{n,eq_c}^2} + \overline{i_{n,eq_{SR}}^2} + \overline{i_{n,Q}^2} = \int_{f_c-f_m}^{f_c+f_m} [S_{n,eq_c}^2(f) + S_{n,eq_{SR}}^2(f)]df + \frac{i_{d,max}^2/2}{10^{SNR_Q/10}} \tag{79}$$

The signal-to-noise ratio of the sigma-delta modulator is in this case

$$SNR = 10 \times \log_{10}\left(\frac{i_{d,max}^2/2}{\overline{i_n^2}}\right) \text{ dB} \tag{80}$$

To achieve a resolution of 14bit the signal-to-noise ratio has to be at least 86dB, so $SNR \geq 86\text{dB}$. In chapter 1 the maximum input current of the sigma-delta modulator is specified at $i_{d,max}$=100nA. Substituting these values in equation (80), gives as a

condition for the noise power in the band of interest $\overline{i_n^2} \leq 1.2\times10^{-23}\,\mathrm{A}^2$. If the noise power spectral density is assumed uniform for the bandwidth from f_c-f_m to f_c+f_m (400Hz), the condition for it is $S_n^2(f) \leq 3\times10^{-26}\,\mathrm{A}^2/\mathrm{Hz}$, which is equivalent to a noise spectral density of $S_n(f) \leq 0.17\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$. The sigma-delta modulator dimensioned in section 3.3 has a signal-to-noise ratio of 93dB, so according to equation (78) the quantisation noise power in the band of interest is $\overline{i_{n,Q}^2} = 2.5\times10^{-24}\,\mathrm{A}^2$. To achieve the required resolution this leaves a margin of $\overline{i_n^2} - \overline{i_{n,Q}^2} = 9.5\times10^{-24}\,\mathrm{A}^2$ for the circuit and settling noise powers. The margins for the noise power and noise spectral densities are thus $S_{n,c+SR}^2(f) \leq 2.4\times10^{-26}\,\mathrm{A}^2/\mathrm{Hz}$ and $S_{n,c+SR}(f) \leq 0.15\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$.

4.5. Offsets, finite integrator output range and capacitor deviations

An integrator without external feedback integrates its offset and is thus DC unstable, but the feedback of the sigma-delta modulator stabilises the integrator operating points [4]. When the second and following integrators have an offset, the loop will build up a DC signal at their preceding integrator output to compensate. Therefore the offset of the second and following integrators is not relevant, it only affect the dynamic output range of the integrators. In the same way the comparator offset causes no signal degradation, because it is compensated by a DC signal build up at the preceding integrator output. The offset of the first integrator is in series with the input signal of the sigma-delta modulator, so it can be regarded as a DC input signal. This is also the case for the offset of the digital-to-analogue converter in the feedback path.

In section 3.3 the topology was dimensioned to have an output range for every integrator of about $\pm1.5q/2=0.3V_{DD}$, which is lower than the supply voltages. This is because the actual output range of an integrator is determined by the output range of its operational amplifier, which has to accommodate the integrator output range under normal operation. If the output signal becomes too large, the gain of the operational amplifier decreases and eventually the signal clips. If the operational amplifier is not rail-to-rail, the clipping levels deviate from the supply voltages. In case the operational amplifiers are overdriven during for example an overload, the resolution decreases but stability can be maintained. High-level computer simulations have to determine if the system stays stable under all conditions, for the clipping levels of the designed operational amplifiers.

Like previously mentioned are sigma-delta modulators relatively insensitive to deviations in their gain factors. High-level computer simulations have to determine the effect of capacitor ratio deviations, on the resolution and stability of the sigma-delta modulator. This applies for errors in the gain factors of the switched-capacitor part of the system.

In the design feedback capacitor C_1 of the first integrator determines, together with the sampling frequency, the proportionality between the analogue input current and the digital output code of the sigma-delta modulator. The maximum allowed value $i_{d,max1}$ of the input current is thus set by this capacitor. This implies that the stable input range

of the sigma-delta modulator changes for deviations in C_1. A larger value of C_1 allows a larger maximum input current $i_{d,max2}>i_{d,max1}$. If a position-sensitive detector with maximum output current $i_{d,max1}$ is connected, the full dynamic range of the sigma-delta modulator is not used, so there is a resolution loss of

$$\Delta N = N_1 - N_2 = \log_2\left(\frac{i_{d,max2}}{i_{d,max1}}\right) \tag{81}$$

A smaller C_1 leads to a smaller allowed maximum input current $i_{d,max3}$. If a position-sensitive detector with $i_{d,max1}>i_{d,max3}$ is connected, the sigma-delta modulator overloads if $i_{d,max1}$ is present at its input.

Basically deviations in capacitor C_1 can be regarded as a gain factor α_{C_1} at the input of the sigma-delta modulator, which is shown in Fig.38. Note that the second gain factor converts the input current to a proportional voltage.

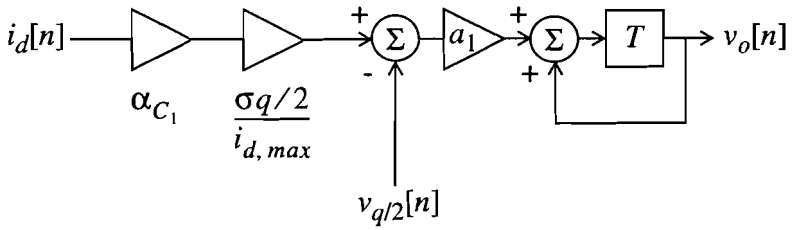

Figure 38. Model of the error due to deviations in capacitor C_1.

4.6. Resolution of the comparator

The effect of limited comparator resolution, or comparator sensitivity, has to be determined by high-level computer simulations. The system can correct the comparator error in a certain degree, but there is a minimum required comparator resolution for the system to be useful.

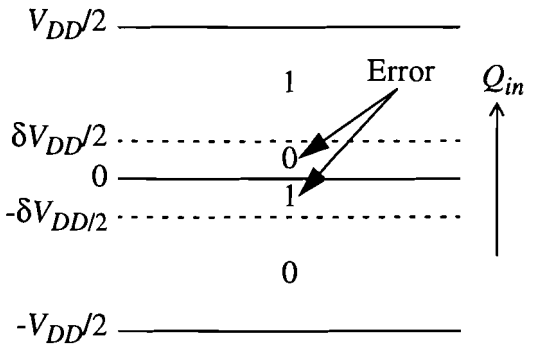

Figure 39. Maximum error comparator model.

To determine the minimum comparator resolution a model is used, which makes the maximum possible error if its input signal is below a certain threshold. This model is shown in Fig. 39. If its input signal Q_{in} is in the range [$-\delta V_{DD}/2$,$\delta V_{DD}/2$] the comparator always makes an error, which gives a comparator resolution of $\delta V_{DD}/2$.

4.7. Summary

The effect of several circuit limitations on the resolution and the stability of the sigma-delta modulator can not be accurately calculated, so it has to be determined by high-level computer simulations. Some specification can be determined before the circuit design and others have to be verified by simulation afterwards. Note that the discussed single-ended circuit can be extended to a differential implementation.

Mainly the circuit limitations of the first integrator are decisive. As discussed in section 3.6, the value of its switched-capacitor is fixed by the topology parameters and the maximum input current of the sigma-delta modulator. Therefore also its noise contribution is, which can lead to a too large circuit noise contribution. If the switched-capacitor turns out to be a resolution limiting factor, the topology has to be redesigned.

Most circuit limitations of the second and the third integrator are suppressed by the feedback action of the system.

5. CIRCUIT DESIGN

This chapter deals with the design of the sigma-delta modulator circuit. Especially the critical first integrator gets extra attention, in order to reduce its non-ideal behaviour within acceptable margins. When possible advantage is taken of the robustness of sigma-delta modulators, in order to relax circuit specifications. Because it is very difficult to take all circuit limitations into account, the circuit will be optimised towards the most critical ones. If the design itself is completed, its performance can be verified by including the circuit specifications in the high-level simulation model.

5.1. The complete circuit and its parameters

A simplified version of the sigma-delta modulator circuit has already been discussed in section 3.5. This circuit is translated into its final form and the circuit parameters, which are the values of the quantisation levels and the capacitors, are determined.

5.1.1. The final circuit of the sigma-delta modulator

The single-ended circuit of section 3.5 is translated into the fully-differential version shown in Fig.40. The advantages of a fully-differential implementation are lower harmonic distortion, better power supply rejection ratio and reduction of clock feed-trough due to charge injection of switches [21].

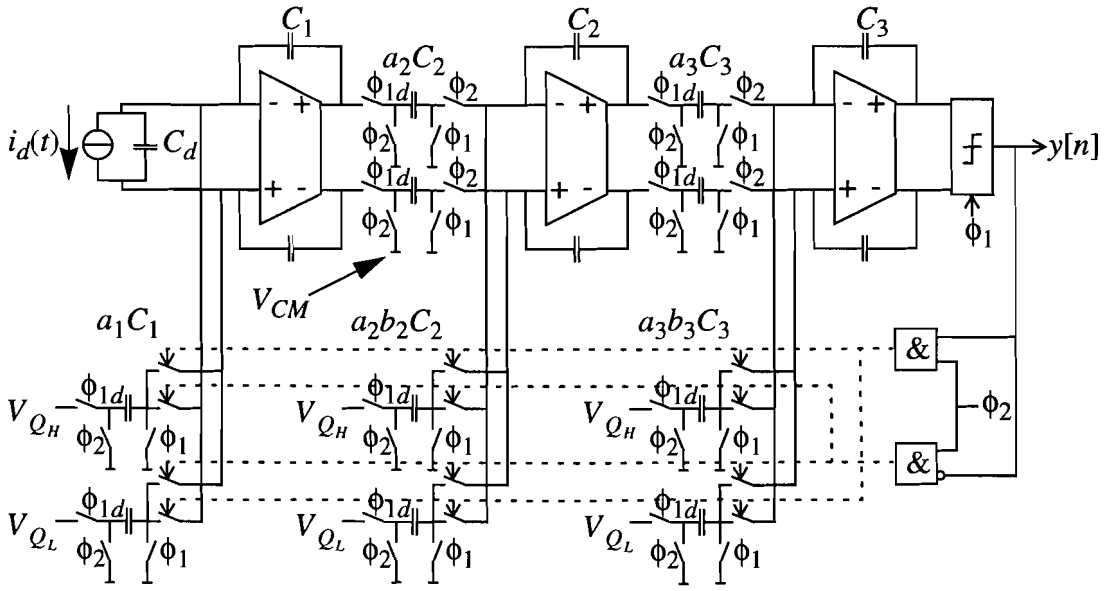

Figure 40. Fully-differential implementation of the sigma-delta modulator.

The basic operation of this circuit is the same as of its single-ended version. Several switches are connected to a delayed version ϕ_{1d} of clock phase ϕ_1, in order to reduce distortion due to clock feed-through [4]. The previously assumed supply voltages $\pm V_{DD}/2$ are replaced by a single supply voltage V_{DD}. This implies that instead of ground, the common-mode voltage $V_{CM}=V_{DD}/2$ is the reference level of the circuit. The quantiser levels $\pm q/2=\pm V_{DD}/5$ become $V_{Q_L}=V_{CM}-V_{DD}/5$ and $V_{Q_H}=V_{CM}+V_{DD}/5$, which are obtained from separate reference sources. According to section 3.3 is the output range of the integrators during normal operation of the sigma-delta modulator around $\pm 1.5q/2=\pm 0.3V_{DD}$, which becomes $V_{CM}\pm 0.3V_{DD}$.

5.1.2. Determining the circuit parameters

The signal levels in the circuit are proportional to the supply voltage, which is $V_{DD}=5\,\mathrm{V}$ and when mentioned $V_{SS}=0\,\mathrm{V}$. The common-mode voltage is in this case $V_{CM}=2.5\,\mathrm{V}$ and the quantisation levels $V_{Q_L}=1.5\,\mathrm{V}$ and $V_{Q_H}=3.5\,\mathrm{V}$. The integrator output range during normal operation is 1 V to 4 V single-ended or ±3 V differential.

For the capacitors a minimum value of 0.5 pF is taken, in order to prevent too large errors due to parasitic capacitances. Capacitor C_1 of the first integrator is calculated with equation (31) at $C_1=0.93\,\mathrm{pF}$. This value is truncated to $C_1=1\,\mathrm{pF}$, in order to avoid overload of the system due to a too small fabricated capacitor. This means that the maximum allowed input current of the sigma-delta modulator becomes $i_{d,max}\approx 108\,\mathrm{nA}$. If a position-sensitive detector with a maximum output current of 100 nA is connected to the sigma-delta modulator, the loss of resolution is according to equation (81) about 0.1 bit.

Capacitor a_1C_1 of the first integrator is determined by C_1 at $a_1C_1=0.6\,\mathrm{pF}$. Capacitor C_2 of the second integrator is chosen at $C_2=4\,\mathrm{pF}$, which gives $a_2C_2=0.8\,\mathrm{pF}$ and $a_2b_2C_2=0.6\,\mathrm{pF}$. Capacitor C_3 of the third integrator is chosen at $C_3=2\,\mathrm{pF}$, which gives $a_3C_3=1\,\mathrm{pF}$ and $a_3b_3C_3=1.5\,\mathrm{pF}$. The capacitors are kept as small as possible, in order to limit the loading and thus the bias currents of the operational amplifiers.

5.2. Process parameters and design equations

The process used to implement the sigma-delta modulator is the AMS 0.8 µm CMOS (CYE) *n*-well process, from Austria Mikro Systeme International AG [22]. In all circuits the transistors are dimensioned to operate in the saturation region, so only the design equations [12] for this region are relevant. The drain current of an *n*MOS (*p*MOS) transistor in saturation is

$$I_{DS} = K_n'\frac{W}{L}(V_{GS}-V_{T_n})^2 \quad , \quad I_{SD} = K_p'\frac{W}{L}(V_{SG}+V_{T_p})^2 \tag{82}$$

The transconductance of an *n*MOS (*p*MOS) transistor in saturation is calculated with equation (82) and its derivative i_{DS} (i_{SD}) to v_{GS} (v_{SG})

$$g_m = \frac{2I_{DS}}{V_{GS}-V_{T_n}} \quad , \quad g_m = \frac{2I_{SD}}{V_{SG}+V_{T_p}} \tag{83}$$

With equations (82) and (83) can for the W over L ratio of the *n*MOS (*p*MOS) transistor be derived

$$\frac{W}{L} = \frac{g_m}{2K_n'(V_{GS}-V_{T_n})} \quad , \quad \frac{W}{L} = \frac{g_m}{2K_p'(V_{SG}+V_{T_p})} \tag{84}$$

The saturation voltage of the *n*MOS (*p*MOS) transistor is given by

$$V_{DS,sat} = V_{GS}-V_{T_n} \quad , \quad V_{SD,sat} = V_{SG}+V_{T_p} \tag{85}$$

K_n' and K_p' are determined by the process parameters

$$K_n' \approx \frac{\mu_{0_n} C_{ox}}{2} \quad , \quad K_p' \approx \frac{\mu_{0_p} C_{ox}}{2} \tag{86}$$

With $\mu_{0_n}=47.89\times10^{-3}$ m^2/Vs, $\mu_{0_p}=21.70\times10^{-3}$ m^2/Vs and $C_{ox}=2.22\times10^{-3}$ F/m^2, the values of these constants become $K_n' \approx 53\times10^{-6}$ A/V^2 and $K_p' \approx 24\times10^{-6}$ A/V^2. The threshold voltages are in the calculations assumed $V_{T_n}=0.8$V and $V_{T_p}=-0.8$V, which are about the values for zero bulk-source voltage. For this process the minimum gate length is taken $L_{min}=3\mu$m, in order to obtain MOS transistors with high enough output impedance to be useful. If the design allows it, a length of $L=5\mu$m or larger is preferred. For switches a minimum length of 0.8μm is taken, in order to obtain low resistance switches with small transistor areas.

5.3. The first integrator

First the type of the operational amplifier is determined and analysed. The capacitors of the first integrator are already determined at $C_1=1$pF and $a_1C_1=0.6$pF. The capacitance of the position-sensitive detector at the input of the sigma-delta modulator, is in the range of 2pF to 50pF. The maximum step at the integrator input is the quantisation step size $q=V_{Q_H}-V_{Q_L}$, because the input signal of the sigma-delta modulator does hardly change for two adjacent samples moments. The maximum output step at the integrator output is thus $|\Delta v_{o_1,max}|=a_1(V_{Q_H}-V_{Q_L})=1.2$V. Because the integrator integrates on clock phase ϕ_2, its settling behaviour is optimised for this clock phase. The operational amplifier is analysed and an approximation of its required parameters is made by hand calculations. After that the design is optimised by HSPICE simulations, using the analysis as a guideline.

5.3.1. Operational amplifier analysis

A fully-differential folded-cascode operational amplifier [12], with switched-capacitor common-mode feedback [11], is chosen for the design. This circuit can achieve high gain and low harmonic distortion, for a large output range. During normal operation all MOS transistors are set in the saturation region. In Fig.41 is the schematic of the operational amplifier shown, without the switched-capacitor common-mode feedback.

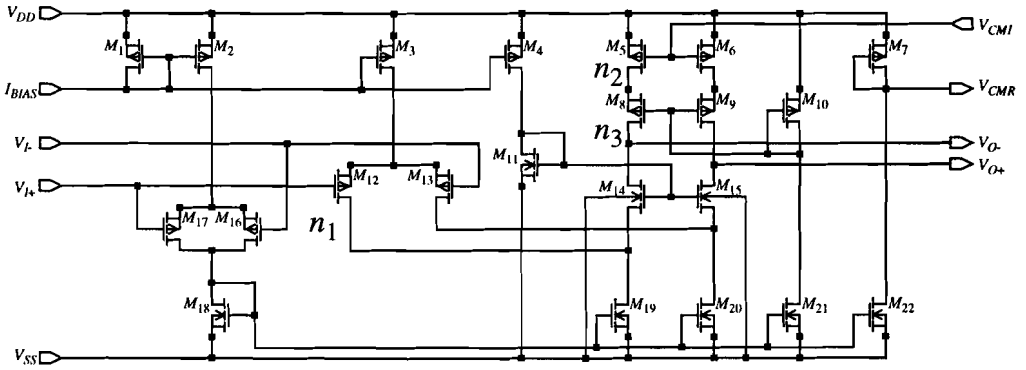

Figure 41. Fully-differential folded-cascode operational amplifier.

Transistors M_{12} and M_{13} form the differential input pair of the cascoded input stage. Because of their lower $1/f$ noise pMOS transistors are selected for the input. Transistors M_{14} and M_{15} form the cascode transistors for the differential input pair. Transistors M_5, M_6, M_8 and M_9 form a load for the input stage. By means of M_5 and M_6 the common-mode voltage of the output terminals is controlled. Transistors M_{16} and M_{17} make up a negative-feedback, in order to keep the currents of transistors M_{19} and M_{20} proportional to the current of transistor M_3. Transistor M_7 generates a reference voltage for the common-mode feedback. The pMOS cascodes are biased by transistors M_{10} and the nMOS cascodes by transistor M_{11}. The currents are set by an external current source and transistors M_1 to M_4 and M_{18} to M_{22}. The currents of transistors M_{19} and M_{20} both have to be equal to the current of transistor M_3.

The common-mode voltage of the output terminals of the operational amplifier has to be kept on $V_{CM}=(V_{DD}+V_{SS})/2$. This is accomplished by the switched-capacitor common-mode feedback circuit shown in Fig.42. Switched-capacitor common-mode feedback is chosen, because the sigma-delta modulator circuit is in switched-capacitor technology. Therefore the required clock signals are already available. Also requires this form of common-mode feedback less circuitry than its continuous-time variant.

For the common-mode voltage of the output terminals to be $V_{CM}=(V_{DD}+V_{SS})/2$, the voltage V_{CMR}-V_{CM} has to be present between the gates of transistors M_5 and M_6 and the output terminals. This is accomplished by means of two switched-capacitors C_2 and C_3. The reference voltage V_{CMR}-V_{CM} is sampled by these capacitors on clock phase ϕ_2.

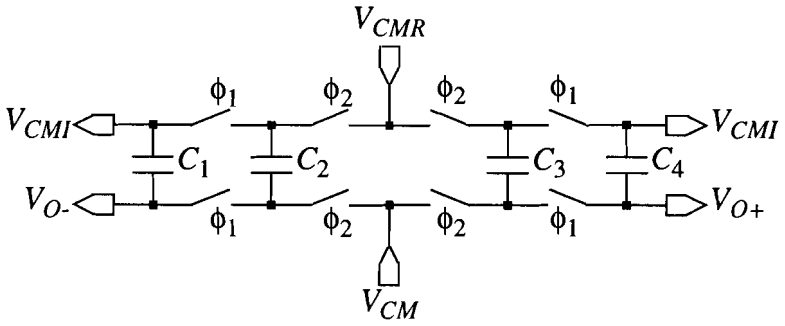

Figure 42. Switched-capacitor common-mode feedback.

On clock phase ϕ_1 reference voltage V_{CMR}-V_{CM} is set over the gates of transistors M_5 and M_6 and the output terminals, forcing their common-mode voltage to $V_{CM}=(V_{DD}+V_{SS})/2$. Capacitors C_1 and C_4 hold the reference voltage on clock-phase ϕ_2. The clock phases are chosen as displayed, because the integrator integrates on clock phase ϕ_2 and its output is sampled on clock phase ϕ_1. Settling during integrating and the correct common-mode voltage during sampling are relevant.

5.3.1.1. Gain bandwidth product and phase-margin

The gain bandwidth product of the operational amplifier is determined by its DC gain A_0 and its dominant pole f_d, which is created on node n_3 and its counterpart. These two nodes carry signals with the same amplitude and opposite phase, thus only one pole is created [12]. Therefore the gain bandwidth product is given by

$$GBW = A_0 \times f_d = g_{m_{12}} R_o \times \frac{1}{2\pi R_o (C_{n_3} + C_l)} = \frac{g_{m_{12}}}{2\pi (C_{n_3} + C_l)} \tag{87}$$

In this equation is R_o the output resistance per output terminal of the operational amplifier, but its exact value is in this case not relevant. Capacitances C_{n_3} and C_l are respectively the capacitance of node n_3 and the equivalent load capacitance connected to this node. Note that this equation is only valid if the non-dominant poles are at higher frequencies than the unity-gain frequency. A large gain bandwidth product is thus obtained, for a large transconductance $g_{m_{12}}$ of the input transistors M_{12} and M_{13}.

To calculate the phase margin, the non-dominant poles have to be determined. The first one is created on node n_1 and its counterpart. Again these two nodes carry signals with the same amplitude and opposite phase, thus only one pole is created. The first non-dominant pole is

$$f_{nd_1} = \frac{g_{m_{14}} + g_{mb_{14}}}{2\pi C_{n_1}} \tag{88}$$

The bulk transconductance $g_{mb_{14}}$ has to be taken into account, because bulk and source are not connected together. The second non-dominant pole is created on node n_2 and its counterpart. Also these two nodes carry signals with the same amplitude opposite phase, thus only one pole is created. The second non-dominant pole is

$$f_{nd_2} = \frac{g_{m_8}}{2\pi C_{n_2}} \tag{89}$$

The phase margin is determined by the non-dominant poles and is given by

$$PM = 90° - \arctan\left[\frac{GBW}{f_{nd_1}}\right] - \arctan\left[\frac{GBW}{f_{nd_2}}\right] \tag{90}$$

By substitution of equations (88) and (89) this becomes

$$PM = 90° - \arctan\left[\frac{g_{m_{12}}}{g_{m_{14}} + g_{mb_{14}}}\frac{C_{n_1}}{C_{n_3} + C_l}\right] - \arctan\left[\frac{g_{m_{12}}}{g_{m_8}}\frac{C_{n_2}}{C_{n_3} + C_l}\right] \tag{91}$$

For a large phase margin $g_{m_{12}}$ should be small and also smaller than g_{m_8} and $g_{m_{14}}$. The first condition contradicts the condition for a high gain bandwidth product. Node capacitances C_{n_1} and C_{n_2} should be kept as small as possible.

5.3.1.2. Slew rate and output swing

The slew rate of the operational amplifier is determined by its bias current and equivalent load capacitance per output terminal

$$SR = \frac{I_{bias}}{C_l} \tag{92}$$

A larger slew rate is obtained increasing the bias current of the operational amplifier.

The output swing of the operational amplifier is determined by the saturation voltages of transistors M_5, M_8, M_{14}, M_{19} and their counterparts. For each output terminal the voltage swing is

$$V_{SS} + V_{DS,\,sat_{19}} + V_{DS,\,sat_{14}} \leq V_{o\pm} \leq V_{DD} - V_{SDsat_5} - V_{SD,\,sat_8} \tag{93}$$

The output swing will be chosen larger than the output range of the integrators during normal operation of the sigma-delta modulator. In this case the gain will be more linear for the required integrator output range. Note that within the range of equation (93) all

transistors stay in saturation. If the sigma-delta modulator becomes unstable due to for example an overload, is returns to normal operations by means of the clipping levels discussed in section 3.3. In that section it was assumed that these clipping levels are set by the supply voltages, but in reality they are near the supply voltages. The output swing can exceed the range of equation (93), but this means that several transistor go out of saturation. This is not relevant, as long as the system goes back to normal operation. During an overload the output signal of the sigma-delta modulator does not contain any information.

5.3.1.3. Noise

The operational amplifier noise consists of a white noise contribution and a $1/f$ noise contribution, due to the thermal noise and $1/f$ noise of its MOS transistors. In Fig.43 the noise model of a MOS transistor is shown. In this figure two noise sources are displayed, which both represent the same noise contribution. The noise is thus referred to the input or referred to the output of the transistor.

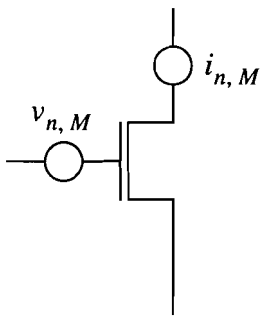

Figure 43. Noise model MOS transistor.

For calculating the equivalent input noise of the operational amplifier, all noise sources are transformed to one input terminal. Therefore the equivalent input noise voltage $v_{n,M}$ of several transistors has to be transformed to an equivalent output noise current $i_{n,M}$ and vice versa, by means of

$$\overline{i_{n,M}^2} = g_m^2 \overline{v_{n,M}^2} \tag{94}$$

The equivalent input noise power spectral density of $v_{n,M}$ for a MOS transistor in saturation is [12]

$$S_{n,M}^2(f) = \frac{8k_bT_{emp}}{3}\frac{1}{g_m} + \frac{KF_F}{WLC_{ox}^2}\frac{1}{f} \tag{95}$$

Constant KF_F is a technology parameter and depends on the transistor type used. This constant is higher for a *n*MOS than for a *p*MOS transistor, so the last one is preferred for lower $1/f$ noise. Every MOS transistor in the circuit contributes noise according to equation (95), but not all noise sources are relevant. Because the circuit is fully differential, common-mode noise sources do not affect the differential signal. Only differential-mode noise sources do, so the noise contribution of transistors M_5, M_8, M_{12}, M_{14}, M_{19} and their counterparts have to be taken into account. The equivalent input noise sources of transistors M_{16} and M_{17} are floating for lower frequencies. Therefore their contribution is not relevant for the band of interest. The equivalent input noise power spectral density of the operational amplifier can thus be derived as

$$S_{n,\,OA}^2(f) = 2\left[S_{n,\,M_{12}}^2(f) + \left(\frac{g_{m_5}}{g_{m_{12}}}\right)^2 S_{n,\,M_5}^2(f) + \left(\frac{g_{m_8}}{g_{m_{12}}}\right)^2 S_{n,\,M_8}^2(f) + \left(\frac{g_{m_{14}}}{g_{m_{12}}}\right)^2 S_{n,\,M_{14}}^2(f) + \left(\frac{g_{m_{19}}}{g_{m_{12}}}\right)^2 S_{n,\,M_{19}}^2(f)\right] \tag{96}$$

Substituting equation (95) in equation (96) gives

$$S_{n,\,OA}^2(f) = \frac{16k_bT_{emp}}{3}\left[\frac{1}{g_{m_{12}}} + \frac{g_{m_5}}{g_{m_{12}}^2} + \frac{g_{m_8}}{g_{m_{12}}^2} + \frac{g_{m_{14}}}{g_{m_{12}}^2} + \frac{g_{m_{19}}}{g_{m_{12}}^2}\right] + \frac{2}{C_{ox}^2}\left[\frac{KF_{F_p}}{W_{12}L_{12}} + \left(\frac{g_{m_5}}{g_{m_{12}}}\right)^2\frac{KF_{F_p}}{W_5L_5} + \left(\frac{g_{m_8}}{g_{m_{12}}}\right)^2\frac{KF_{F_p}}{W_8L_8} + \left(\frac{g_{m_{14}}}{g_{m_{12}}}\right)^2\frac{KF_{F_n}}{W_{14}L_{14}} + \left(\frac{g_{m_{19}}}{g_{m_{12}}}\right)^2\frac{KF_{F_n}}{W_{19}L_{19}}\right]\frac{1}{f} \tag{97}$$

Both white noise and $1/f$ noise decrease if $g_{m_{12}}$ is large and also if larger than $g_{m_5}, g_{m_8}, g_{m_{14}}$ and $g_{m_{19}}$. Only the $1/f$ noise term of transistor M_{12} is not affected by the transconductances of the transistors. Because the transconductance of a MOS transistor is proportional to its drain current, the white noise term is inversely proportional to it, so a larger drain current gives a lower white noise contribution. This is not the case for the $1/f$ noise contribution. The $1/f$ noise is inversely proportional to the area of the transistors, so large areas lowers the $1/f$ noise contribution. Increasing the transistor areas leads however to a smaller phase margin, due to increasing node capacitances.

5.3.2. Operational amplifier design

The design of the operational amplifier will for simplicity be discussed for the differential half-circuit. The analyses of the circuit limitations in chapter 4 also apply to the differential (half-)circuit, but some equations have to be slightly altered. This will be discussed when relevant during the design. The capacitance of the position-sensitive detector is in the range of C_d=2pF to C_d=50pF. Its largest value gives the worst-case conditions for noise and settling, so the design is focused on it. In equations is thus C_d=50pF assumed.

In section 4.1, the circuit noise has been analysed for a single-ended circuit. In order to apply the analysis on the differential half-circuit, the model of the operational amplifier equivalent input noise has to be related to the corresponding HSPICE simulation results. In case of a differential amplifier, HSPICE calculates an equivalent input noise source between its two input terminals. The power spectral density of this noise source is given by equation (97). This noise source can be represented by a noise source of half the value at each input terminal, like is shown in Fig.44.

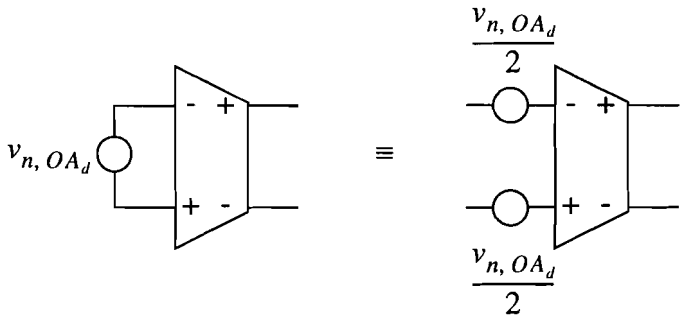

Figure 44. Transformation of the HSPICE equivalent input noise source.

Note that not the noise power is divided by two, but the noise is, because both sources represent the same noise source and are thus correlated. The differential half-circuit with its relevant noise sources is shown in Fig.45.

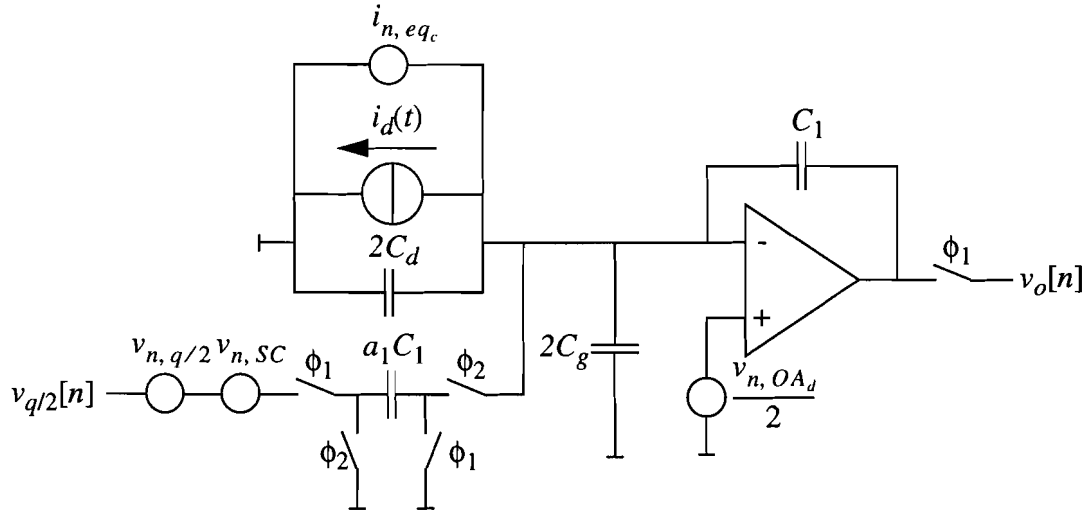

Figure 45. Differential half-circuit of the first integrator with noise sources.

This figure is alike Fig.28, but now also the input capacitance C_g of the differential input pair and the bias current feedback circuit is taken into account. This is the capacitance which is seen between the two input terminals of the operational amplifier. If a MOS transistor is in saturation, mainly a gate-source capacitance is seen at its gate. In the differential circuit two of these capacitances are in series, so half of it is seen at the differential input. In the differential half-circuit, twice that resulting capacitance C_g

is relevant. Note that in the differential half-circuit also twice capacitance C_d is relevant. The input capacitance C_g has to be estimated, because it depends on the design. To be on the safe side a relatively high value of C_g=2pF is taken, in order to take transistors M_{12}, M_{13}, M_{16} and M_{17} into account.

Equations (45) and (48) of the equivalent power spectral densities of respectively $v_{n,SC}$ and $v_{n,q/2}$, do not change for the differential half-circuit. The power spectral density of the differential operational amplifier equivalent input noise is alike equation (37)

$$S^2_{n,\,OA_d}(f) = \gamma_{OA_d} + \frac{\zeta_{OA_d}}{f} \tag{98}$$

Note that in case of the differential half-circuit the noise power spectral density is divided by four. The power spectral density of the equivalent input noise source due to the operational amplifier is thus

$$\begin{aligned} S^2_{n,\,eq_{OA}}(f) &= \frac{\pi^2}{2}\{[2C_d + 2C_g + C_1]^2 \\ &+ [2C_d + 2C_g + (1 + a_1)C_1]^2\}\{\gamma_{OA_d} f^2 + \zeta_{OA_d} f\} \end{aligned} \tag{99}$$

The power spectral density of noise source $v_{n,SC}$ is already determined by the circuit parameters. Substituting their values into equation (45) gives for its noise power spectral density $S^2_{n,\,eq_{SC}}(f) = 2.5\times10^{-27}\,\mathrm{A^2/Hz}$. According to the calculations in section 4.4 this leaves a margin of $2.4\times10^{-26} - 2.5\times10^{-27} \approx 2.2\times10^{-26}\,\mathrm{A^2/Hz}$, for the total power spectral density of other noise sources.

At this point the noise specification for the operational amplifier of the first integrator can be determined. As a condition $S^2_{n,\,eq_{OA}}(f) \ll 2.2\times10^{-26}\,\mathrm{A^2/Hz}$ is taken. Substituting the circuit parameters into equation (99), gives as a condition for the equivalent input noise of the operational amplifier at a frequency of f=1.2kHz

$$\begin{aligned} &S^2_{n,\,eq_{OA}}(1200) = 1.6\times10^{-13}\left\{\gamma_{OA_d} + \frac{\zeta_{OA_d}}{1200}\right\} \ll 2.2\times10^{-26}\,\mathrm{A^2/Hz} \Rightarrow \\ &\gamma_{OA_d} + \frac{\zeta_{OA_d}}{1200} \ll 1.4\times10^{-13}\,\mathrm{V^2/Hz} \Rightarrow S_{n,\,OA}(1200) \ll 375\,\mathrm{nV/\sqrt{Hz}} \end{aligned} \tag{100}$$

This frequency is the highest signal frequency, for the with frequency increasing equivalent input noise spectral density of the operational amplifier. It gives thus the worst-case condition for the noise power spectral density in the band of interest.

In section 4.2.3.1 the settling behaviour has been analysed for a single-ended circuit. In Fig.46 the differential half-circuit of the first integrator on clock phase ϕ_2 is shown.

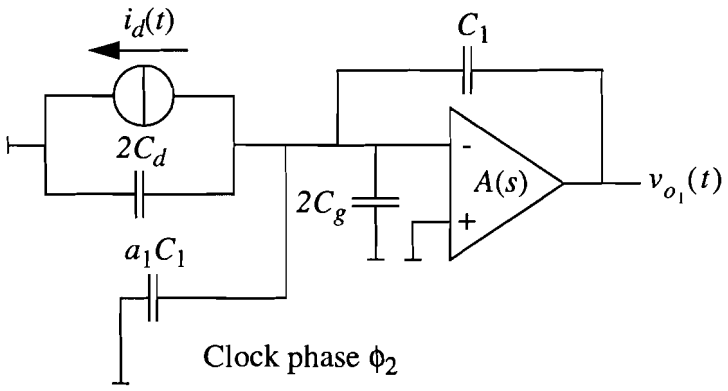

Figure 46. Differential half-circuit of the first integrator on clock phase ϕ_2.

Also for this analysis capacitance C_g has to be taken into account. The equivalent load capacitance C_l of equation (87) is given by

$$C_{l_1} = \frac{(2C_d + 2C_g + a_1C_1)C_1}{2C_d + 2C_g + (1+a_1)C_1} \tag{101}$$

With this equation the maximum equivalent load capacitance is estimated at $C_{l_1} \approx 1\text{pF}$. At this point the actual design can begin. First the bias current is chosen, which has to be sufficiently large in order to obtain low noise, large gain bandwidth product and large slew rate. For the bias current is taken I_{bias}=200µA, which would according to equation (92) give a slew rate of SR=200V/µs. If all transconductances are assumed to be 10^{-3}A/V, the spectral density of the white noise power can with equation (97) be estimated at $\gamma_{OA_d} \approx 10\text{nV}/\sqrt{\text{Hz}}$. This is well below the condition set by equation (100) and leaves thus a large margin for the $1/f$ noise.

It is assumed that the non-dominant poles of the operational amplifier will be located at higher frequencies than the unity-gain frequency. In that case equation (87) is valid for determining the gain bandwidth product. The on-time of clock phase ϕ_2 will be around T_{ϕ_2}=1.5µs, so the settling of the operational amplifier should occur within this time. Sigma-delta modulators are relatively insensitive to relatively large exponential settling errors, so the settling requirements of the operational amplifiers can be relaxed [14]. If as a condition 1% settling error within an exponential settling time of 1.5µs is taken, the frequency of the second integrator pole can with equation (71) be determined to be $f_{p_2} \geq$490kHz. This implies that $\tau_{p_2} SR > |\Delta v_{o_1 max}|$ for C_d=50pF and also for C_d=2pF, so slew rate limitation should not occur. The gain bandwidth product is determined with a for the differential half-circuit altered version of equation (69)

$$f_{p_2} \approx GBW \frac{C_1}{2C_d + 2C_g + (1+a_1)C_1} \quad ,A_0 \gg 1 \tag{102}$$

The gain bandwidth product has according to this equation to be $GBW \geq 52\text{MHz}$. Capacitance C_{n_3} in equation (87) has to be estimated, because it depends on the design. To be on the safe side a relatively high value of $C_{n_3}=1\text{pF}$ is taken. The transconductance of the input transistors has then according to equation (87) to be $g_{m_{12}} \geq 7\times10^{-4}$ A/V. In order to keep the input transistors M_{12} and M_{13} in saturation, a saturation voltage of $V_{SD,sat}=0.2\text{V}$ is chosen. The transconductance of the input transistors is according to equation (83) $g_{m_{12}} = 10^{-3}$ A/V, which is sufficiently large. The W over L ratio of transistors M_{12} and M_{13} is calculated with equation (84) at $W_{12}/L_{12}=104$.

The next step is to dimension load transistors M_5 and M_6, current sources M_{19} and M_{20} and cascode transistors M_8, M_9, M_{14} and M_{15}. These will be dimensioned to accommodate a large output swing. The saturation voltage of load transistor M_5 and its complement is for matching [12] chosen on $V_{SD,\,sat_5}=0.4\text{V}$, which gives $W_5/L_5=25$. Matching is in this case preferred over a larger output swing, because the common-mode feedback is connected at this point. The saturation voltage of current source M_{19} and its complement is chosen on $V_{DS,\,sat_{19}}=0.2\text{V}$, which gives $W_{19}/L_{19}=95$. In this case is chosen to accommodate a larger output swing. The saturation voltage of casode transistors M_8, M_{14} and their complements are chosen on $V_{SDsat_8}=0.2\text{V}$ and $V_{DS,\,sat_{14}}=0.2\text{V}$, so their transconductance is high and they also accommodate a large output swing. This gives for $W_8/L_8=104$ and for $W_{14}/L_{14}=50$. The output swing can be calculated at $V_{SS}+V_{DS,\,sat_{19}}+V_{DS,\,sat_{14}}=0.4\text{V}$ to $V_{DD}-V_{SD,\,sat_5}-V_{SD,\,sat_8}=4.4\text{V}$. The bias voltages of the cascode transistors are set to keep transistors M_5, M_{19} and their complements in saturation. The bias voltage of the pMOS cascode stage is calculated at $V_{DD}-V_{SD,\,sat_5}-V_{SD,\,sat_8}-|V_{T_p}|=3.6\text{V}$ and the bias voltage of the nMOS cascode stage at $V_{SS}+V_{DS,\,sat_{19}}+V_{DS,\,sat_{14}}+V_{T_n}=1.2\text{V}$. In reality the last one will be larger, because bulk and source of these nMOS transistors are not connected together. This causes an increment of the threshold voltage [12].

Transistors M_{16} and M_{17} have the same dimensions as input transistors M_{12} and M_{18}, in order to keep their source-gate voltages about equal. The saturation voltage of transistors M_1 to M_4 is chosen at $V_{SD,\,sat_3}=0.5$, which gives $W_3/L_3=33$. Transistors M_{18} and M_{21} have the same dimensions as transistor M_{19} and its complement. Transistors M_{10}, M_{11}, M_7 and its current source M_{22} will be determined by simulation, in order to obtain the required reference voltages.

The circuit is first simulated with ideal cascode bias voltages and an ideal common-mode feedback loop. It is optimised towards phase margin, $1/f$ noise and linear DC gain for a single-ended output range of 1 V to 4 V or ±3 V differential. Note that the white noise level is already set by the bias current and the W over L ratios of the transistors. The minimum transistor length was already given as $L_{min}=3\mu\text{m}$. Equations (91) and (97) are used to identify the critical points that compromise phase margin and $1/f$ noise.

After that the dimensions of transistors M_{10} and M_{11} are determined, in order to obtain the required cascode bias voltages. The calculated cascode bias voltages are adjusted to 3.5 V for the pMOS cascode stage and 1.4 V for the nMOS cascode stage. Finally the ideal common-mode feedback circuit is replaced by the switched-capacitor circuit.

Capacitors C_1 to C_4 of the common-mode feedback circuit are chosen at 0.5 pF, in order not to load the output terminals too much. Its biasing circuit consisting of transistors M_7 and M_{22}, can now be dimensioned to keep the common-mode voltage at V_{CM}=2.5 V. All the transistor dimensions are given in Table 1. For these dimensions and the other circuit parameters, an adequate compromise between phase margin, $1/f$ noise and linearity is obtained.

Table 1. Dimensions of the MOS transistors.

Transistor	W [µm]	L [µm]
M_1 - M_4	332	10
M_5, M_6	260	10
M_7	20	34.2
M_8, M_9	312	3
M_{10}	254	10
M_{11}	150	10
M_{12}, M_{13}	312	3
M_{14}, M_{15}	140	3
M_{16}, M_{17}	312	3
M_{18} - M_{21}	564	6
M_{22}	21	20

The specifications obtained by simulation are listed in Table 2. The equivalent load capacitance is taken 1 pF larger than calculated, thus C_l=2 pF per output terminal. This is to leave a margin for extra loading due to the switched-capacitor common-mode feedback and due layout parasitic capacitances. If required in the final circuit, it also gives a margin for a small compensation capacitor. All transistors stay in saturation during normal operation of the sigma-delta modulator. The settling, the common-mode feedback and the distortion are verified further on, in the complete circuit.

Table 2. Operational amplifier specifications (differential out).

Parameter	Value[1]
GWB	53 MHz[2]
FM	58°[2]
A_0	>80 dB[3]
$S_{n,\,OA_d}(f)$	59 nV/$\sqrt{Hz}$[4]
P_{diss}	4 mW

1. T_{emp}=300K
2. C_l=2 pF (per output)
3. Output range ±3 V
4. f=1 kHz (differential in)

5.4. The second and the third integrator

The design procedure for the second and the third integrator, is alike the one for the first integrator. Their capacitors have already been determined at C_2=4pF, a_2C_2=0.8pF, $a_2b_2C_2$=0.6pF, C_3=2pF, a_3C_3=1pF and $a_3b_3C_3$=1.5pF. The maximum output step of the second integrator is $|\Delta v_{o_2,\,max}| = a_2|\Delta v_{o_1,\,max}| + a_2b_2(V_{Q_H} - V_{Q_L}) \approx 0.6\,\text{V}$ and of the third integrator $|\Delta v_{o_3,\,max}| = a_3|\Delta V_{o_2,\,max}| + a_3b_3(V_{Q_H} - V_{Q_L}) \approx 1.8\,\text{V}$.

5.4.1. Operational amplifier design

The operational amplifier topology of the second and the third integrator is the same as for the first integrator. Therefore the operational amplifier analyses of section 5.3.1 are also valid here. Again the design procedure will for simplicity be discussed for the differential half-circuit. Noise specifications will is this case not be derived, because the circuit noise contribution of these integrators can be assumed negligible. Nevertheless the operational amplifier noise will be minimised, without compromising the phase margin too much. The settling time and gain bandwidth product equations of section 4.2.3.1 can in a slightly altered version also be used. This will be discussed for the second integrator and when relevant the difference with the third integrator is given. In Fig.47 the differential half-circuit of second integrator on clock phase ϕ_2 is shown.

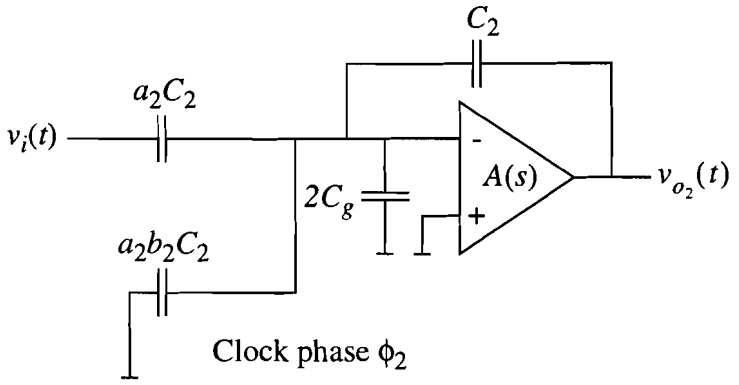

Figure 47. Differential half-circuit of the second integrator on clock phase ϕ_2.

This figure is alike Fig.46, but now the input signal is a voltage source v_i(t) connected to a series capacitor a_2C_2. The equivalent load capacitance C_l of equation (87), which is similar to equation (101), is calculated as

$$C_{l_2} = \frac{[2C_g + a_2(1+b_2)C_2]C_2}{2C_g + [1 + a_2(1+b_2)]C_2} \tag{103}$$

The only difference with the third integrator is at this point. The third integrator is on clock phase ϕ_2 connected to the comparator. During clock phase ϕ_2 it sees thus a capacitance C_c of the comparator, between its two output terminals. Like C_d it is a differential input capacitance, in this case of the differential input pair of the comparator, thus for the differential half-circuit $2C_c$ is relevant. The equivalent load capacitance of the third integrator is thus

$$C_{l_3} = \frac{[2C_g + a_3(1+b_3)C_3]C_3}{2C_g + [1+a_3(1+b_3)]C_3} + 2C_c \tag{104}$$

Capacitances C_g and C_c depend on the design, so to be on the safe side their values are estimated at C_g=2pF and C_c=1pF. The last one is estimated smaller, because in general a comparator can be made with less and smaller input circuitry. This gives $C_{l_2} \approx 2.3$pF and $C_{l_3} \approx 3.5$pF. The third integrator has the largest maximum output step and the largest equivalent load capacitance, so the design of the operational amplifier focuses on it. If it meets the required specifications, it can also be applied in the second integrator. Note that for both integrators the poles are fixed, because they are not affected by the capacitance of the position-sensitive detector.

Again first the bias current is chosen, which mainly has to accommodate the gain bandwidth product. As discussed in chapter 4 noise and slew rate are less relevant for the second and third integrator. For the bias current I_{bias}=20μA is taken, which would according to equation (92) give a slew rate of $SR \approx 6$V/μs.

The same settling condition as in section 5.3.2 is taken here, so the second pole frequency of the third integrator has to be also $f_{p_2} \geq 490$kHz. This implies that $\tau_{p_2} SR > |\Delta v_{o_{3,max}}|$, so slew rate limitations should not occur. Basic feedback calculations for determining the poles of the third integrator, are almost the same as for the first integrator in section 4.2.3.1. Note that in this case an exponential settling error also causes a linear deviation in the corresponding gain factor. The gain bandwidth product is thus determined with an altered version of equation (102)

$$f_{p_2} \approx GBW \frac{C_3}{2C_g + [1+a_3(1+b_3)]C_3} \quad , A_0 \gg 1 \tag{105}$$

The value for the gain bandwidth product has according to this equation to be GBW≥2.1MHz. Capacitance C_{n_3} in equation (87) has to be estimated, because it depends on the design. To be on the safe side a relatively high value of C_{n_3}=1pF is taken. The transconductance of the input transistors has then according to equation (87) to be $g_{m_{12}} \geq 6\times10^{-5}$ A/V. In order to keep the input transistors M_{12} and M_{13} in saturation, a saturation voltage of $V_{SD,sat}$=0.1 V is chosen. The transconductance of the input transistors becomes according to equation (83) $g_{m_{12}} = 2\times10^{-4}$ A/V, which is sufficiently large.

The rest of the design procedure is alike the one in section 5.3.2. The calculated and afterwards by simulation optimised transistor dimensions are listed in Table3.

Table 3. Dimensions of the MOS transistors

Transistor	W [µm]	L [µm]
M_1 - M_4	33.2	10
M_5, M_6	94	10
M_7	48	25
M_8, M_9	41.6	4
M_{10}	60.8	15
M_{11}	31.6	20
M_{12}, M_{13}	208	5
M_{14}, M_{15}	18.8	4
M_{16}, M_{17}	208	5
M_{18} - M_{21}	170	18
M_{22}	18	18

The specifications obtained by simulation are listed in Table4. Again the load capacitance is taken 1 pF larger than calculated, thus C_{l_3}=4.5pF per output terminal. This is to leave a margin for extra loading due to the switched-capacitor common-mode feedback and due layout parasitic capacitances. If required in the final circuit, it also gives a margin for a small compensation capacitor. All transistors stay in saturation during normal operation of the sigma-delta modulator. The settling and the common-mode feedback are verified further on, in the complete circuit.

Table 4. Operational amplifier specifications (differential).

Parameter	Value[1]
GWB	4.1MHz[2]
FM	82°[2]
A_0	>84dB[3]
$S_{n,OA_d}(f)$	36nV/$\sqrt{Hz}$[4]
P_{diss}	0.5mW

1. T_{emp}=300K
2. C_l=4.2pF (per output)
3. Output range ±3V
4. f=1kHz (differential in)

5.5. The comparator

The differential comparator circuit is shown in Fig.48. Note that it are basically two separate circuits, the actual analogue comparator and the digital switch control logic. The analogue part is connected to the same power supply as the operational amplifiers (V_{DD}=5V, V_{SS}=0V) and the digital part is connected to a separate digital power supply (V_{DDD}=5V, V_{SSD}=5V), in order to reduce supply crosstalk [4].

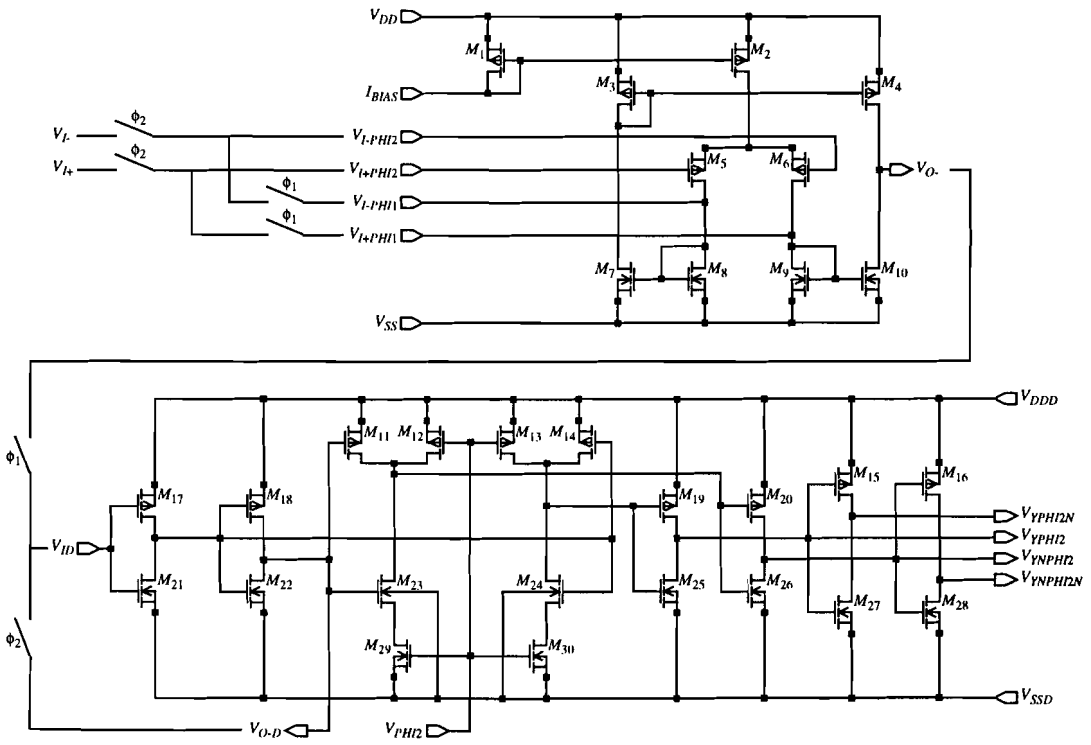

Figure 48. The comparator and the digital switch control logic.

The output terminals of the third integrator are connected to the sign corresponding input terminals V_{I+} and V_{I-} of the comparator. During clock phase ϕ_2 the input signal is tracked by the comparator, a symmetrical operational amplifier made up by transistors M_1 to M_{10}. On clock phase ϕ_1 the comparator makes a decision by means of positive feedback. During this clock phase the output signal V_{O-} of the comparator is inverted twice, by the inverters made up by M_{17}, M_{18}, M_{21} and M_{22}, so the correct logical level is generated. On the next clock phase ϕ_2 the comparator is disconnected from the inverters. These are then connected into a positive feedback loop, to hold the data signal during this clock phase. At the same time two logical NAND gates, made up by transistors M_{11} to M_{14}, M_{23}, M_{24}, M_{29} and M_{30}, transfer the data signal to the output. Note that the output signals of the previously mentioned inverters have already settled at the end of clock phase ϕ_1. The output inverters, made up by the remaining transistors, turn the previous NAND operation into an AND operation and they drive the switches connected to them. An estimation of the total load capacitance is made by the input capacitance of the switches and the capacitance of a clock line, which is about 0.5pF per output terminal. For simulations 0.7pF is taken.

The symmetrical operational amplifier is dimensioned to be stable during the tracking clock phase ϕ_2. The bias current is I_{bias}=20μA. Except the output inverters all logical gates are dimensioned to have a low peak current. All inverters have equal noise margins in both states. The noise margins of the NAND gates, for one high input and the other input swept from low to high are equal. This because the data signal at their inputs has already settled, before clock phase ϕ_2 becomes high. In Table5 the dimensions of the transistors are listed.

Table 5. Dimensions of the MOS transistors.

Transistor	W [μm]	L [μm]
M_1, M_2	80	3
M_3, M_4	25	5
M_5, M_6	106	10
M_7 - M_{10}	3.9	5
M_{11} - M_{14}	2	14
M_{15}, M_{16}	4	0.8
M_{17}, M_{18}	2	16
M_{19}, M_{20}	4	0.8
M_{21}, M_{22}	2	28
M_{23}, M_{24}	2	19
M_{25} - M_{28}	2.5	0.8
M_{29}, M_{30}	2	19

In Fig.49 is the timing-diagram of the comparator shown. At the left are the signal labels of Fig.48 and at the right the signals they represent. Note that to simplify the figure, $V_{YPHI2N} \equiv \overline{y[n] \cdot \phi_2}$ and $V_{YNPHI2N} \equiv \overline{\overline{y[n]} \cdot \phi_2}$ are not shown.

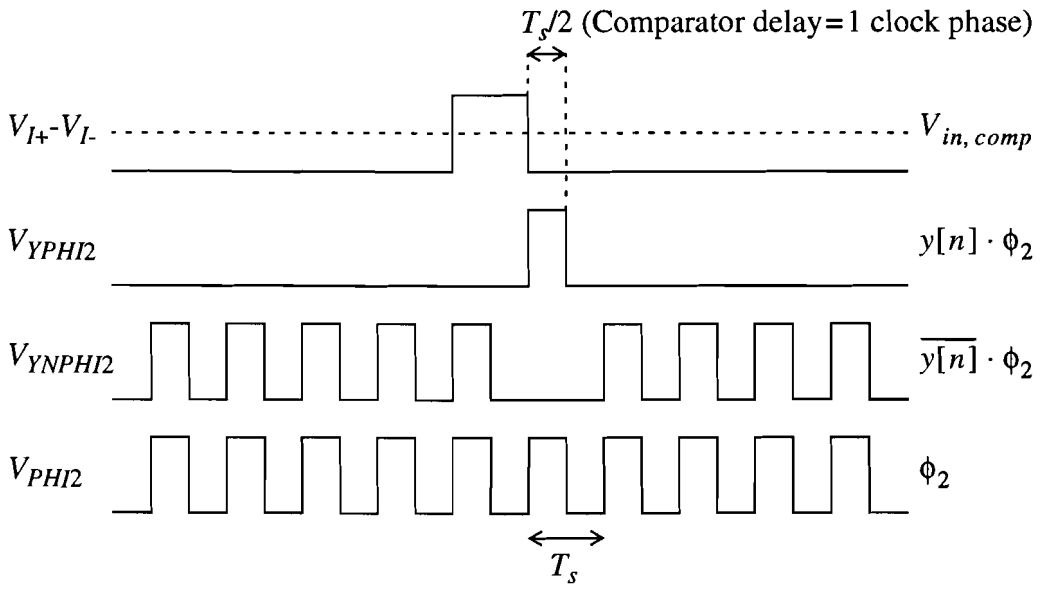

Figure 49. Timing diagram of the comparator.

The comparator delay from the end of decision clock phase ϕ_1, to the end of the following output controlling clock phase ϕ_2 is one clock phase. Note that the output signal of the third integrator, thus the input signal of the comparator, changes on clock phase ϕ_2 and remains at the integrator output on clock phase ϕ_1. Simulations show that the comparator has a resolution of 1.3mV differential, which is equivalent to 0.026% of a maximum differential input signal of $\pm V_{DD}$=±5V. Also for this maximum differential input signal the comparator operates correctly. The relative comparator resolution defined in section 4.6, is thus $\delta = 2.6\times10^{-4}$. The average power dissipation is $\overline{P_{diss}}$=0.3mW. Note that in reality the on-time of the clock phases is smaller then depicted, because they are non-overlapping.

5.6. The clock signal generator

The non-overlapping clock phases ϕ_1 and ϕ_2 are generated by the logic shown in Fig.50. This is a simplified version of the actual circuit, because only two clock phases are displayed. The input clock signal determines the sampling rate, so its frequency is the sampling frequency f_s. With the dimensions of the transistors and the number of inverters, the required timing is obtained.

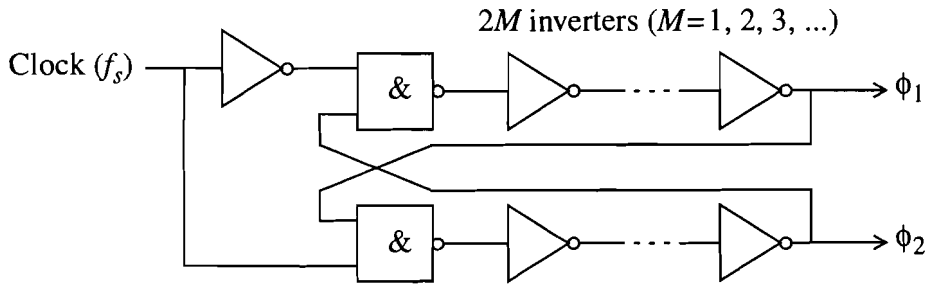

Figure 50. Logic for generating the non-overlapping clock phases.

The circuit for generating the clock signals is shown in Fig.51. Note that this circuit is also supplied by the power supply for the digital circuitry (V_{DDD}=5V, V_{SSD}=0V), in order to decrease supply crosstalk. Transistors M_1 to M_{15}, M_{20}, M_{21} to M_{34}, M_{39} to M_{51}, M_{54} and M_{55} to M_{68} make up the clock logic of Fig.50. All logical gates formed by these transistors are dimensioned to have a low peak current. All inverters have equal noise margins in both states. For the two NAND gates the minimum noise margins are equal for the most outer transfer characteristics, because their inputs can change at the same moment. Transistors M_{16} to M_{19}, M_{35} to M_{38}, M_{52}, M_{53}, M_{69} and M_{70} make up the output buffers, which drive the switches and logic gates connected to them. An estimation of the total load capacitance due to the input capacitance of the switches, the capacitance of the clock lines and the capacitance of the comparator logical gates connected is made. The load capacitance for each output terminal is estimated at 0.6pF for V_{PHI1}, V_{PHI1N}, V_{PHI1D} and V_{PHI1DN}, 1.3pF for V_{PHI2} and 1pF for V_{PHI2N}. For simulation is for these capacitances respectively 0.8pF, 1.5pF and 1.2pF taken.

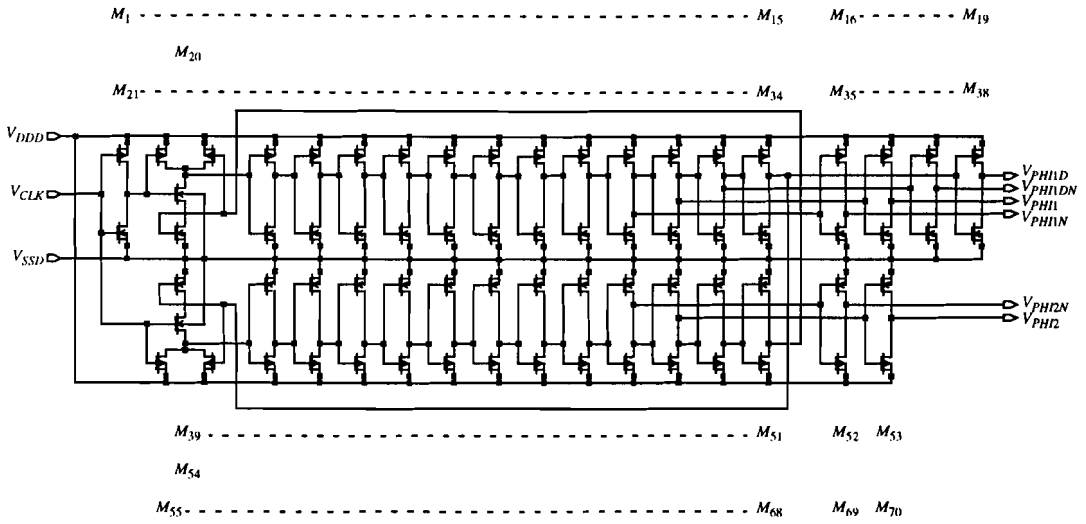

Figure 51. Circuit of the clock logic.

In Table 6 the dimensions of the transistors are listed.

Table 6. Dimensions of the MOS transistors.

Transistor	W [µm]	L [µm]
M_1	2	8
M_2, M_3	2	7
M_4 - M_{15}	2	8
M_{16} - M_{19}	4	0.8
M_{20}	2	9.5
M_{21}	2	14
M_{22}	2	9.5
M_{23} - M_{34}	2	14
M_{35} - M_{38}	2.5	0.8
M_{39}	2	9.5
M_{40} - M_{51}	2	14
M_{52}, M_{53}	2.5	0.8
M_{54}	2	9.5
M_{55}, M_{56}	2	7
M_{57} - M_{68}	2	8
M_{69}, M_{70}	4	0.8

In Fig. 52 the timing diagram of the clock logic is shown. At the left are the signal labels of Fig. 51 and at the right the signals they represent. Clock phases ϕ_1 and ϕ_2 are non-overlapping, with a non-overlap time of about 90 ns. Clock phase ϕ_{1d} changes after about 5 ns when ϕ_1 has already settled. Clock phase ϕ_{1d} is settled about 70 ns before ϕ_2 starts changing. The transition from low to high and vice versa is about 20 ns for all clock phases. The on-time is for all clock phase about 1.8 µs, which is larger than the

estimated 1.5μs. This implies that the assumed settling time for the design of the operational amplifiers has been taken with adequate margin. Note that only the on-time is relevant. The other times not so, as long as the signals change in the order as is displayed. The average power dissipation is $\overline{P_{diss}}$=60μW

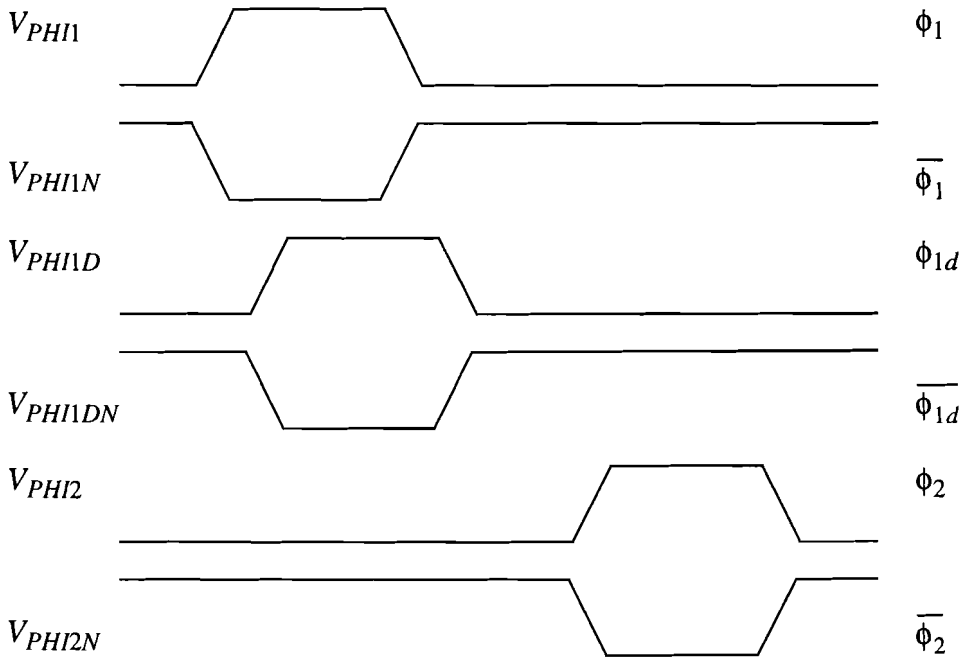

Figure 52. Timing diagram of the clock logic (proportions are not exact).

5.7. The switches

All switches used are CMOS switches, shown in Fig. 53, with equal areas for the *p*MOS and *n*MOS transistors. Equal areas are chosen to minimise charge injection, but thus gives a little increment of harmonic distortion. The feedback action of the system will reduce this harmonic distortion.

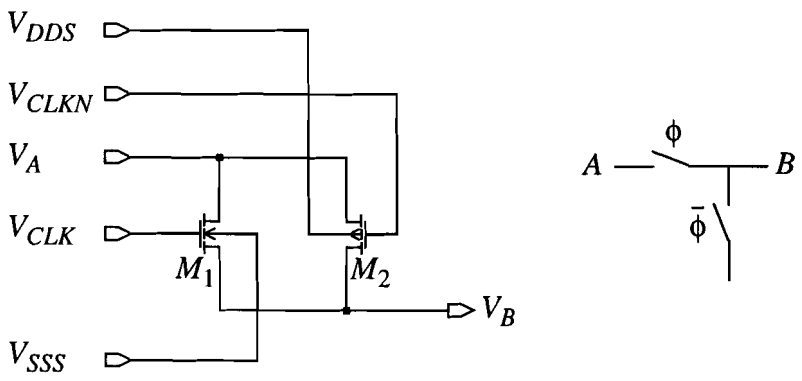

Figure 53. CMOS switch.

As a condition for the maximum on-resistance of the switch is taken 1kΩ, but simulations show that the maximum on-resistance is about 600Ω. The bulks of switches are connected to a separate power supply (V_{DDS}=5V, V_{SSS}=0V), in order to decrease supply crosstalk. The maximum gate capacitance is estimated 40fF per gate.

5.8. Biasing circuitry

The bias currents of the sigma-delta modulator are for the prototype obtained from three separate external current sources. The current bias circuit is shown in Fig.54. Input terminal I_{B_200UA} receives a 200μA current, which is mirrored to the operational amplifier of the first integrator. Input terminal I_{B1_20UA} receives a 20μA current, which is mirrored to the operational amplifiers of the second and third integrator. Input terminal I_{B2_20UA} receives a 20μA current, which is mirrored to the comparator.

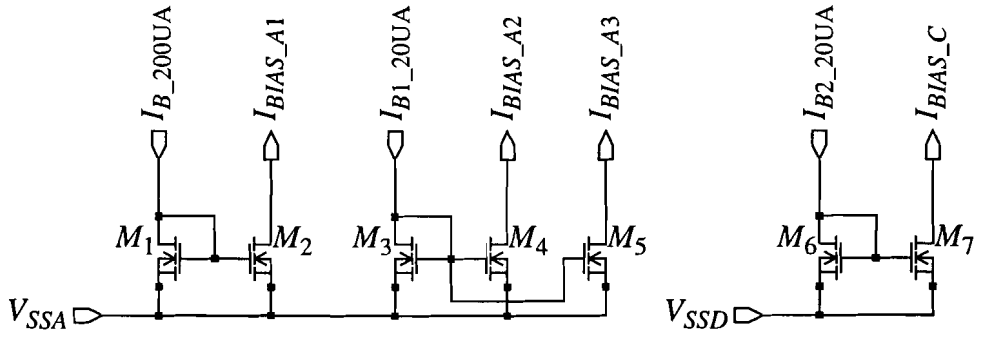

Figure 54. Bias current circuitry.

The saturation voltage of all transistors is for matching chosen at $V_{DS,sat}$=0.5V. Connected to the operational amplifiers and the comparator, the error is 0.8% for the operational amplifier bias currents and 0.9% for the comparator bias current. The power dissipation is P_{diss}=2.5mW. The transistor dimensions are listed in Table 7.

Table 7. Dimensions of the MOS transistors.

Transistor	W [μm]	L [μm]
M_1, M_2	150	10
M_3 - M_7	15	10

The reference voltages are for the prototype are obtained from external voltage sources. These voltages are the common mode voltage V_{CM}=2.5V and the quantiser levels V_{Q_L}=1.5V and V_{Q_H}=3.5V. In the final version of the circuit they are obtained from voltage dividers, with proportions $V_{CM}=V_{DD}/2$, $V_{Q_L}=V_{CM}-V_{DD}/5=0.3V_{DD}$ and $V_{Q_H}=V_{CM}+V_{DD}/5=0.7V_{DD}$.

5.9. Summary

The sigma-delta modulator circuit is fully differential. The power dissipation is 7.6mW and the required chip area about $1.5mm^2$. For the first integrator is a stronger operational amplifier designed as for the second and third integrator, because the capacitance of the position-sensitive detector affects its settling and its circuit noise contribution.

With an extended version of the circuit limitation analyses from chapter 4, several required specifications of the operational amplifiers can be derived as a starting point for the design. When possible the robustness of sigma-delta modulators is exploited, in order to relax the required amplifier specifications.

6. EVALUATION OF THE DESIGN

In this chapter several circuit properties are included in the high-level simulation model of the sigma-delta modulator, in order to determine their effect on its resolution and stability. For several other circuit properties the effect on the resolution of the system can be calculated. The possible combinations of circuit limitations are infinite, so it is not possible to determine a clear worst-case condition. High-level simulations can thus only give an estimation of the robustness of the sigma-delta modulator. Nevertheless this estimation is assumed reliable, regarding the fact that other designs have proven the high insensitivity of sigma-delta modulators to circuit limitations [4][11][14].

6.1. Performance of the operational amplifiers

During the design of the operational amplifiers in chapter 5, several specifications have been estimated by calculation and have been met by the realised circuits. High-level MATLAB simulations and HPSICE circuit simulations have to estimate the actual behaviour of the sigma-delta modulator, due to the operational amplifier properties.

6.1.1. Amplifier DC gain

The conditions for the DC gain magnitude of the operational amplifiers, given by equations (19) and (59), are amply met. Integrator leakage and threshold limitations are according to high-level simulations negligible for every integrator. This is also the case for the linear settling error due to finite DC gain in equation (53).

As discussed in section 4.2.2, the harmonic distortion of the first integrator determines the harmonic distortion of the sigma-delta modulator. To calculate the harmonic distortion, the DC gain characteristic as a function of the output voltage has to be approximated by a polynomial. In case of a differential circuit only the odd harmonics are relevant, because the even ones are cancelled out [21]. In Fig. 55 the simulated DC gain of the first operational amplifier as a function of its differential output voltage is shown. Three coefficients of the approximating polynomial of equation (62) are taken into account, which gives an accurate enough approximation

$$A_0(v_o) \approx \alpha_0 + \alpha_2 v_o^2 + \alpha_4 v_o^4 = 15044 - 160 v_o^2 - 35 v_o^4 \qquad (106)$$

The inverse polynomial is approximated by

$$\frac{1}{A_0(v_o)} \approx \beta_0 + \beta_2 v_o^2 + \beta_4 v_0^4 = 66.5\times10^{-6} + 4.2\times10^{-7} v_0^2 + 2.7\times10^{-7} v_0^4 \qquad (107)$$

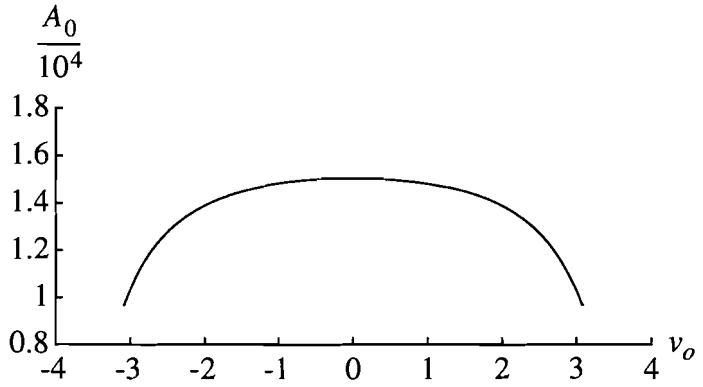

Figure 55. Simulated DC gain characteristic of the operational amplifier.

Taking the differential signal swing into account, the magnitudes of the third and fifth harmonic distortion components, for the maximum allowed input current $i_{d,max}$=108 nA determined in section 5.1.2 are

$$hd_3 = \frac{1}{4}\beta_2\left(2\frac{T_s}{C_1}i_{d,max}\right)^3 \approx 6.3\times10^{-8}$$
$$hd_5 = \frac{1}{16}\beta_4\left(2\frac{T_s}{C_1}i_{d,max}\right)^5 \approx 7.2\times10^{-9} \quad (108)$$

The signal-to-harmonic distortion ratio $SP_{hd}R$ is with these values calculated at

$$SP_{hd}R = 10\times\log_{10}\left[\frac{\frac{1}{2}\left(2\frac{T_s}{C_1}i_{d,max}\right)^2}{\frac{(hd_3)^2}{2}+\frac{(hd_5)^2}{2}}\right] = 142 \text{ dB} \quad (109)$$

This seems a very optimistic estimation, but note that only the sinusoidal part of the integrator output signal determines the harmonic distortion. For a maximum input current of 108nA, the proportional differential output swing of the first integrator is ±0.84 V. For this range is the DC gain characteristic relatively linear, so the harmonic distortion is very low. The harmonic distortion components are outside the band of interest anyway, but their inter-modulation products are not. These are because of the low harmonic distortion negligible.

6.1.2. Settling of the operational amplifiers

The settling of the integrators on clock phase ϕ_2 is verified for their maximum output step. The differential values of the maximum output steps are for the first, the second

and the third integrator respectively $|\Delta v_{o,max_{1d}}|$=2.4V, $|\Delta v_{o,max_{2d}}|$=1.2V and $|\Delta v_{o,max_{3d}}|$=3.6V. The current of every operational amplifier output terminal is monitored, in order to detect slew rate limitation during the rising of the output step. Slew rate limitation occurs if the current of an output terminal reaches its maximum value, which is the bias current of the operational amplifier. For all operational amplifiers the maximum output terminal currents stay well below the value of the bias current, so slew rate limitations do not occur. The settling is thus exponential.

The second and the third integrator settle very fast, which makes their exponential settling errors at the end of clock phase ϕ_2 negligible. This is also the case for the exponential settling error of the first integrator, for a position-sensitive detector capacitance of C_d=2pF. For C_d=50pF the settling of the first integrator is slower, which gives an exponential settling error of 0.7% at the end of clock phase ϕ_2. According to high-level simulations is the settling at this point critical for the design. Due to the linear settling error in the unity-gain feedback factor of the first integrator, discussed in section 4.2.3.1, decreases the stable input range of the sigma-delta modulator with 11%. The consequence is that the maximum allowed input current decreases from 108nA to 96nA. The system still reaches a signal-to-noise ratio of SNR_Q=93dB, equivalent to a resolution of 15.2bit. This is the case for a linear settling error of 1%, but the performance stays stable for larger settling errors. The system is sensitive to this error, because the proportionality between the input signal and the output signal of the sigma-delta modulator is lost. If the error would also occur at the same time for the input signal of the sigma-delta modulator, it would lead to an error in the gain factor of the first integrator, for which the system is relatively insensitive.

The settling on clock phase ϕ_1 is also adequate for all operational amplifiers and the assumption that it is less critical is confirmed. The switched-capacitor common-mode feedback keeps the common-mode voltage of all integrators at the required value, during both clock phases.

6.1.3. Finite integrator output range

During normal operation of the sigma-delta modulator, the differential integrator output range of ±3V is accommodated by the operational amplifiers. When the integrators are overdriven due to instability or overload, they clip at 0.1V and 5V single-ended or ±4.9V differential. High-level simulations show that the system stays stable under all conditions. There is sufficient margin to compensate for different clipping levels, due to variations in the fabrication process of the chip. The clipping levels do not affect the resolution of the system, as long as they not limit the integrator output range during normal operation. Note that for large integrator output signals several transistors go out of saturation, which causes signal degradation. Like previously mentioned is this not relevant, as long as the system is forced back to normal operation.

6.2. Performance of the comparator

The effect of the comparator resolution on the performance of the system is determined with the maximum error model of section 4.6. According to high-level simulations the stable input range of the sigma-delta modulator decreases with 11%. This was also the case for the settling error of the first integrator in section 6.1.2, thus the consequence is also that the maximum allowed input current decreases from 108nA to 96nA. The system still reaches a signal-to-noise ratio of SNR_Q=93dB, equivalent to a resolution of 15.2bit.

Due to the combination of the comparator error and the settling error of the first integrator, the system achieves a signal-to noise ratio of SNR_Q=92dB, equivalent to a resolution of 15bit, for a maximum allowed input current of $i_{d,max}$=108nA. Thus for the combination of the two errors, a larger stable output than for the individual errors is obtained. This demonstrates very well that a clear worst-case condition for the sigma-delta modulator can not be determined. Therefore the worst-case specifications of both errors are taken, thus SNR_Q=92dB and $i_{d,max}$=96nA.

6.3. Circuit and slew rate related noise

Because slew rate limitations do not occur in the circuit, only the circuit noise is relevant. The circuit noise contributions of the second and third integrator have been assumed negligible, because their spectral densities are shaped with a noise-shaping function. Regarding the noise performance of their operational amplifiers, this assumption is justified. Only the circuit noise contribution of the first integrator has to be evaluated. The noise contributions of the operational amplifier and the switched-capacitor can be determined, but the noise contribution of reference sources V_{Q_L} and V_{Q_H} can not. This because for the prototype of the sigma-delta modulator they are obtained from external sources. Only a specification for their acceptable noise contribution can be determined.

In Fig.56 the equivalent input noise spectral density due to the operational amplifier noise and the switched-capacitor noise of the first integrator is shown. This characteristic is calculated by taking the square-root of their summed noise power spectral densities. The equivalent input noise power spectral density of the first integrator due to its operational amplifier, is obtained by HSPICE simulations. First the equivalent input noise spectral density is determined per clock phase and afterwards the square-root of the average of the noise power spectral densities is taken. The equivalent input noise spectral density of the switched capacitor is calculated with equation (45).

The increase in quantisation noise due to the limited resolution of the comparator has to be taken into account. With SNR_Q=92dB and $i_{d,max}$=96nA, the quantisation noise power in the band of interest is according to equation (78) $i^2_{n,Q}=2.9\times10^{-24}$ A^2. To achieve the required resolution, there is a margin of $i^2_n - i^2_{n,Q} = 9.1\times10^{-24}$ A^2 left, for the

circuit noise power. The new margins for the circuit noise power and the circuit noise spectral densities are $S^2_{n,c}(f) \leq 2.3\times10^{-26}\,\mathrm{A^2/Hz}$ and $S_{n,c}(f) \leq 0.15\mathrm{pA}/\sqrt{\mathrm{Hz}}$. These calculations are alike the ones in section 4.4.

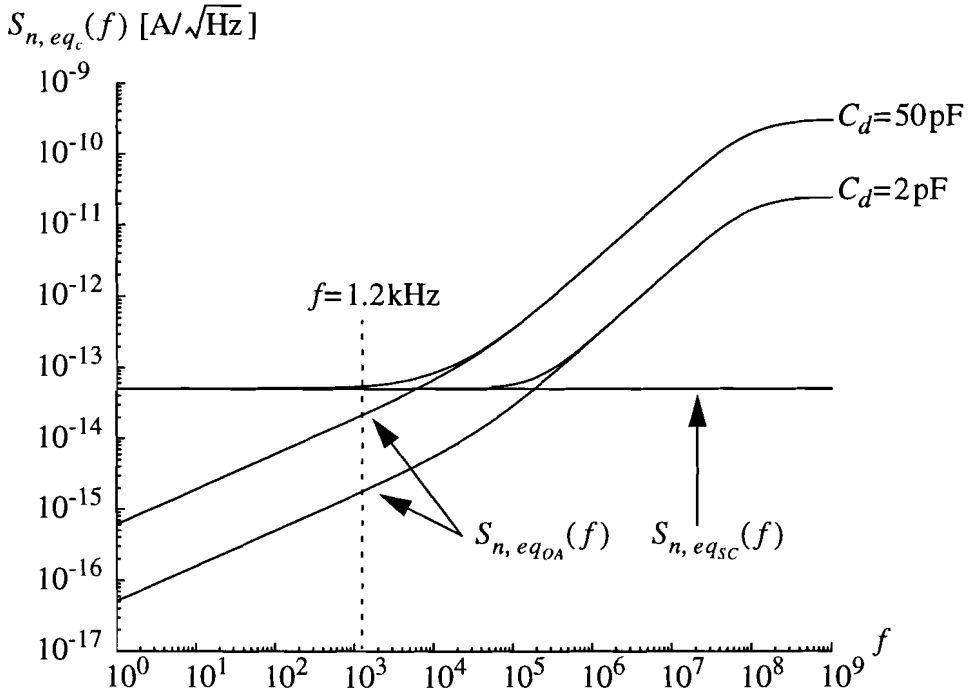

Figure 56. Equivalent noise spectral density due to circuit noise.

For lower values of the position-sensitive detector capacitance C_d, the circuit noise is determined by switched-capacitor a_1C_1. For larger values of C_d the noise of the operational amplifier becomes relevant. For a maximum signal frequency of f_b=1.2kHz, the noise spectral density is $0.06\mathrm{pA}/\sqrt{\mathrm{Hz}}$, which is well below the specification of $0.15\mathrm{pA}/\sqrt{\mathrm{Hz}}$. The margin left for other noise contributions, mainly of the reference sources, is $0.14\mathrm{pA}/\sqrt{\mathrm{Hz}}$. The acceptable noise contribution of the reference sources can be calculated with equation (48). An exact expression is not given, because it also depends on the noise bandwidth of these sources. If the noise of the reference sources is assumed negligible compared to the other noise sources, the total noise power in the band of interest is $i_n^2 = 4.3\times10^{-24}\,\mathrm{A^2}$. With a maximum input current of $i_{i,max}$=96nA, the achievable signal-to noise ratio and resolution are respectively SNR=90dB and N=14.7bit.

6.4. Capacitor deviations

Capacitor matching errors in the process used are well below 1%, thus the error in the integrator gain factors is in the same order. High-level simulations show that the performance of the sigma-delta modulator is insensitive to these small errors.

The absolute error of a capacitor is about 15%, which can cause relatively large deviations for the first integrator. In section 4.5 has been discussed that this causes a change in the stable input range of the sigma-delta modulator, which depends on the value of capacitor C_1. Note that for C_1=1pF, $i_{d,max}$=108nA was calculated in section 5.1.2. If C_1 is 15% too large the maximum allowed input current becomes 124nA. According to equation (81) the loss of resolution is 0.4bit, if a position-sensitive detector with a maximum output current of 96nA is connected. The resolution of the sigma-delta modulator becomes in this case 14.3bit.

If C_1 is 15% too small, the maximum allowed input current becomes 93nA. If a position-sensitive detector with a maximum output current of 100nA is connected, the sigma-delta modulator overloads for input current around this value. This is also the case in section 6.1.2, for the maximum allowed input current 96nA. If the system overloads, its digital output signal does not contain any usable information, but the system returns to normal operation when the input signal decreases. In the prototype this kind of overload can be avoided by increasing the sampling frequency, so the ratio between T_s and C_1 is corrected. For the eventual circuit this is not an attractive solution. In this case on-chip tuning of capacitor C_1 is a better option, but this leads to higher production costs of the chip. Therefore the maximum allowed input current will be set at $i_{d,max}$=90nA, which leaves according to equation (81) a worst-case resolution of N=14.2bit.

6.5. Summary

According to a combination of high-level computers simulations, circuit simulations and calculations, the designed sigma-delta modulator achieves a worst-case resolution of N=14.2bit. In this case the noise contribution of the reference voltage sources V_{Q_L} and V_{Q_H} is assumed negligible. The dominant circuit noise source is the switched-capacitor input of the first integrator. The system maintains stability under all conditions, for a input current range of $i_{d,max}$=±90nA.

The worst-case resolution is determined by the largest capacitance C_d of the position-sensitive detector and the largest possible deviation of feedback capacitor C_1 of the first integrator. The system is still usable for larger values of C_d, but in that case the resolution decreases. If this is acceptable depends on the application.

7. DIGITAL POST-PROCESSING

The single-bit output signal of the sigma-delta modulator has a pulse-density modulated format. In the application it contains the information of interest in AM modulated form. For recovering this information, filtering and AM demodulation are required. Digital low-pass filtering removes undesired signals present at higher frequencies, which consist mainly of quantisation noise. For a pulse-density modulated signal, a digital low-pass filter is realised relatively simple with full-adders and delay-elements [4]. For AM demodulation of a pulse-density modulated signal, a method has to be developed.

The output signal of a sigma-delta modulator can basically be considered as a binary random process. Therefore it is assumed that its AM demodulation is similar to AM demodulation of an analogue random process, which is shown in Fig.57.

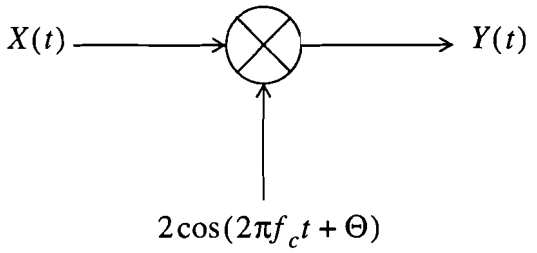

Figure 57. AM demodulation of an analogue random process.

An AM modulated input signal $X(t)$, is multiplied by a carrier with frequency f_c and phase-uncertainty $\Theta \in (0,2\pi]$. The amplitude of the carrier is for correct scaling, but is not relevant for the demodulation process itself. The demodulated output signal $Y(t)$ is

$$Y(t) = X(t)2\cos(2\pi f_c t + \Theta) \tag{110}$$

Signals $X(t)$ and $Y(t)$ are both random processes with power spectral densities $S^2_{XX}(f)$ and $S^2_{YY}(f)$. Their auto-correlation functions [15] are $R_{XX}(t)$ and $R_{YY}(t)$. The auto-correlation function of $Y(t)$ can be calculated as

$$\begin{aligned} R_{YY}(t, t+\tau) &= E[Y(t)Y(t+\tau)] \\ &= 2R_{XX}(\tau)E[\cos(4\pi f_c t + 2\pi f_c \tau + 2\Theta) + \cos(2\pi f_c \tau)] \\ &= 2R_{XX}(\tau)\frac{1}{2\pi}\int_0^{2\pi}[\cos(4\pi f_c t + 2\pi f_c \tau + 2\Theta) + \cos(2\pi f_c \tau)]d\Theta \\ &= 2R_{XX}(\tau)\cos(2\pi f_c \tau) \end{aligned} \tag{111}$$

The power spectral density of this auto-correlation function is

$$S_{YY}^2(f) = \frac{S_{XX}^2(f-f_c) + S_{XX}^2(f+f_c)}{2} \tag{112}$$

In Fig.58 the AM demodulation process is illustrated, with $X(t)$ assumed to have a similar spectral density as the quantisation noise of the sigma-delta modulator. Note that in this case both negative and positive frequencies are regarded.

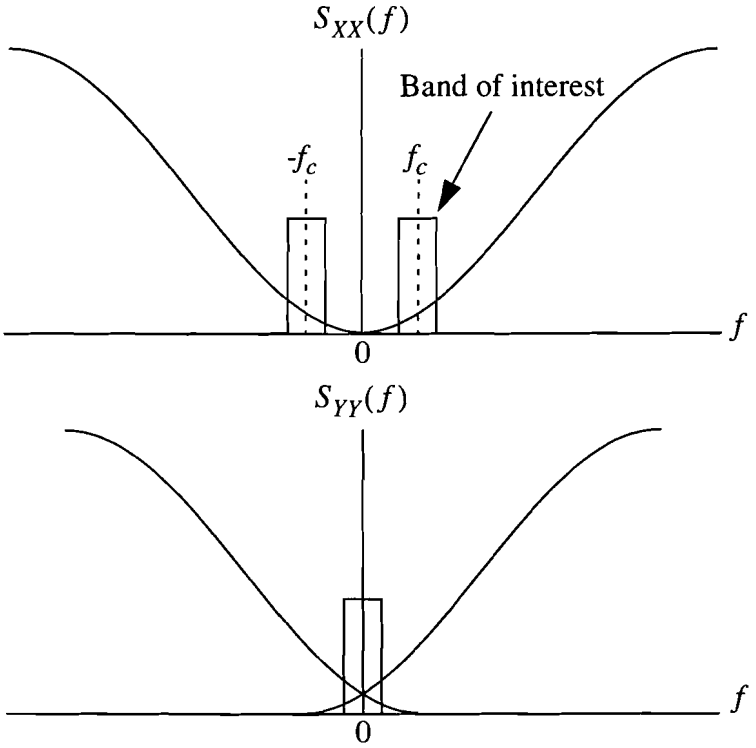

Figure 58. Spectral densities before and after AM demodulation.

Multiplication of logical signals is realised with an EXOR gate. It should thus be possible to realise AM demodulation of a binary random process with a single EXOR gate. To verify this assumption a high-level simulation of an EXOR gate is performed, with at one input the single-bit output signal of the sigma-delta modulator and at the other input a clock signal with frequency f_c. The simulation model is shown in Fig.59.

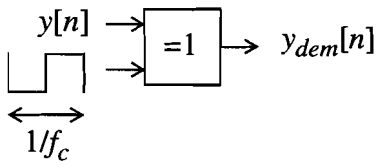

Figure 59. AM demodulation of a single-bit digital signal.

The clock signal is a square-wave, so its Fourier series consists of a fundamental frequency and a number of harmonics at higher frequencies, of which the amplitudes decrease with increasing frequency. The fundamental frequency performs the desired AM demodulation, but every harmonic also acts as a demodulating carrier. Therefore more quantisation noise is multiplied down into the base band, than in case of the AM demodulation of an analogue random process. The in section 4.1.4 expected doubling of the quantisation noise in the band of interest is thus too optimistic.

An estimation of the performance is made by high-level simulation. In Fig.60 the simulation result for the designed third-order sigma-delta modulator is shown.

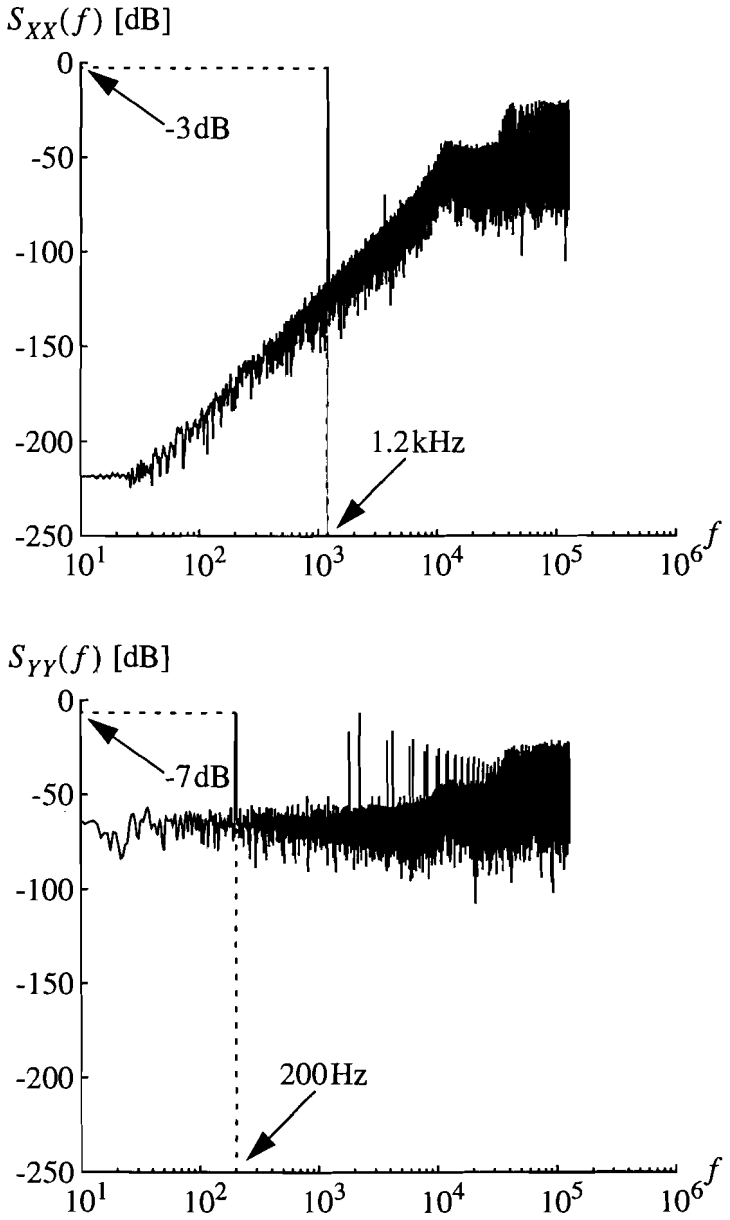

Figure 60. AM demodulation with an EXOR gate.

AM demodulation is accomplished, but the resolution of the resulting signal $y_{dem}[n]$ is decreased to 5.4bit. Due to the specific character of the quantisation noise spectrum and due to the harmonics of the clock signal, too much quantisation noise is multiplied down into the base band. This makes the configuration as shown in Fig.59 useless. The demodulation can thus not be realised directly after the sigma-delta modulator, but it seems that digital pre-filtering is required. The proposed method of AM demodulation requires thus further development.

After demodulation digital low-pass filtering is required, to remove the undesired high frequency components. Finally the signal is decimated, so a multi-bit signal at a lower sampling rate is obtained.

8. SUMMARY AND FUTURE DIRECTIONS

A sigma-delta modulator for optical detector applications is designed, using the AMS 0.8μm CMOS (CYE) process. The achievable resolution is 14bit, for a stable input current range of ±90nA, giving a total input reduced noise current spectral density of $0.16pA/\sqrt{Hz}$ at 1kHz. This is equivalent to an input reduced noise current spectral density, of a transimpedance amplifier with a 650kΩ feedback resistor. The switched-capacitor input of the first integrator is the dominant circuit noise source. The power dissipation is 7.6mW and the required chip area about $1.5mm^2$. The circuit is suitable for position-sensitive photodetectors and other types of photodiodes, with a capacitance between 2pf and 50pF.

To reduce chip area and to improve linearity, the output current of the source device is directly offered to the sigma-delta modulator. A preamplifier can thus be omitted, but the configuration requires continuous-time discrete-time mixed-mode circuitry. The capacitors of the first integrator are fixed, due to the topology parameters and the specified maximum input current of the sigma-delta modulator.

First the topology of the sigma-delta modulator is determined. Calculations give an estimation for the required parameters of the topology, but high-level MATLAB computer simulations have to verify and optimise them. Also high-level simulations have to determine the stability of the system under all conditions. After these simulations, a set of suitable parameters is obtained and the topology can be translated into a circuit. It is relevant that the circuit realises exactly the same transfer function as the topology.

When the circuit implementation is determined, the effect of its limitations can be analysed. These limitations mainly affect the resolution and the linearity of the sigma-delta modulator, but its stability can also be affected. The first integrator is identified as the most critical element in the design. By analysing the circuit limitations, several circuit specifications are obtained, which are taken into account during the circuit design.

The circuit is fully-differential and the critical first integrator is built around a stronger operational amplifier than the second and the third integrator. Where possible the robustness of sigma-delta modulators is exploited, in order to relax circuit specifications. Finally the system is evaluated by a combination of calculations, high-level simulations and HSPICE circuit simulations. The specifications are met and because of the robustness of the design it should be possible to use it for position-sensitive detectors, which have a larger source capacitance than specified. Performance will in this case decrease, but if the application allows this the sigma-delta modulator is still useful, as long as it stays stable under all conditions.

The digital pulse-density modulated output signal of the sigma-delta modulator has to be AM demodulated. A proposal for this operation has been given, in the form of a logical EXOR gate. It seems that direct demodulation of the sigma-delta modulator output signal is not possible in this way. Due to the specific character of the

quantisation noise spectrum, too much quantisation noise is multiplied down into the base band. Digital pre-filtering is required, in order to remove the quantisation noise at higher frequencies. This method of demodulation needs further development.

The performance of the sigma-delta modulator can be evaluated directly at its digital output. The output signal of a position-sensitive detector does not contain large components at high frequencies, so an anti-alias filter is redundant. This would also degrade the source signal. Note that the first integrator of the system already performs some anti-alias filtering. Because the clock frequency is relatively low, digital post-processing logic can be simulated real-time by computer.

REFERENCES

[1] Mäkynen, A.; T. Ruotsalainen; J. Kostamovaara: High accuracy CMOS position-sensitive photodetector (PSD), Electronics Letters, Vol. 33, No. 2, pp. 128-130, January 1997

[2] Mäkynen, A.J.; J.T. Kostamovaara; T.E. rahkonen: CMOS photodetectors for industrial position sensing, IEEE Transactions on Instrumentation and Measurement, Vol. 43, No. 3, pp. 489-492, June 1994

[3] Mäkynen, A.J.; J.T. Kostamovaara; R.A. Myllylä: A high-resolution lateral displacement sensing method using active illumination of a cooperative target and a focused four-quadrant position-sensitive detector, IEEE Transactions on Instrumentation and Measurement, Vol. 44, No. 1, pp. 46-52, February 1995

[4] Op 't Eynde, F.; W. Sansen: Analog interfaces for digital signal processing systems, Kluwer Academic Publishers, Boston (USA) 1995

[5] Plassche, R. van de: Integrated analog-to-digital and digital-to-analog converters, Kluwer Academic Publishers, Boston (USA) 1994

[6] Engelen, J.A.E.P. van; R.J. van de Plassche: New stability criteria for the design of low-pass sigma-delta modulators, to be published at the International Symposium on Low-Power Electronics and Design (ISLPED97), Monterey (USA), August 1997

[7] Cataltepe, T.; A.R. Kramer; L.E. Larson; G.C. Temes; R.H. Walden: Digitally corrected multi-bit sigma-delta data converters, IEEE Proc. ISCAS'89, pp. 647-650, May 1989

[8] Toumazou, C.; J.B. Hughes; N.C. Battersby: Switched-currents an analogue technique for digital technology, Peter Peregringus Ltd., on behalf of the Institution of Electrical Engineers, London (UK) 1993

[9] Redman-White, W.; A.M. Durham: Integrated fourth-order sigma-delta convertor with stable self-tuning continuous-time noise shaper, IEE Pro.-Circuits Devices Syst., Vol. 141, No. 3, pp. 145-150, June 1994

[10] Enden A.W.M. van den; N.A.M. Verhoeckx: Digitale signaalbewerking, Delta Press BV, Overberg (The Netherlands) 1987 (In Dutch)

[11] Baird, R.T.; T.S. Fiez: A low oversampling ratio 14-b 500-kHz delta-sigma ADC with self-calibrated multibit DAC, IEEE Journal of Solid-State Circuits, Vol. 31, No. 3, pp. 312-320, March 1996

[12] Laker, K.R.; W.M.C. Sansen: Design of analog integrated circuits and systems, McGraw-Hill Inc., New York (USA) 1994

[13] Fischer, J.H.: Noise sources and calculation techniques for switched capacitor filters, IEEE Journal of Solid-State Circuits, Vol. SC-17, No. 4, pp. 742-752, August 1982

[14] Hauser, M.W.; R.W. Brodersen: Circuit and technology considerations for MOS delta-sigma A/D converters, IEEE Proc. ISCAS'86, pp. 1310-1315, May 1986

[15] Shanmugam, K. S.: Digital and analog communication systems, John Wiley & Sons Inc., New York (USA) 1985

[16] Boser B.E.; B.A. Wooley: The design of sigma-delta modulation analog-to-digital converters, IEEE Journal of Solid-State Circuits, Vol. SC-23, pp. 1298-1308, December 1988

[17] Dias, V.F.: G. Palmisamo; F. Maloberti: Harmonic distortion in SC sigma-delta modulators, IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, Vol. 41, No. 4, pp. 326-329, April 1994

[18] Yin, Guangmin; W. Sansen: A high-frequency and high-resolution fourth-order sigma-delta A/D converter in BiCMOS technology, IEEE Journal of Solid-State Circuits, Vol. 29, No. 8, pp. 857-865, August 1994

[19] Gray, P.R.; R.G. Meyer: Analysis and design of analog integrated circuits, Third Edition, John Wiley & Sons Inc., New York (USA) 1993

[20] Dias, V.F.; G. Palmisano, P. O'Leary, F. Maloberti: Fundamental limitations of switched-capacitor sigma-delta modulators, IEE Proceedings-G, Vol. 139, No. 1, pp. 27-32, February 1992

[21] Lee, Kuang-Lu; R.G. Meyer: Low-distortion switched-capacitor filter design techniques, IEEE Journal of Solid State-Circuits, Vol. SC-20, No. 6, pp. 1103-1113, December 1985

[22] Austria Mikro Systeme International AG: 0.8µm CMOS process parameters, document 9933006, revision B, Unterpremstätten (Austria), 1997

Appendix

General simulation of the third-order sigma-delta modulator

This simulation offers the possibility, to monitor all state signals of the sigma-delta modulator during normal operation. Besides normal operation, overload of the input signal and different initial state conditions are used to determine the stability of the system under all conditions. Note that the ability to recover from instability also depends on the amplitude of the input signal. Circuit limitations can be included, according to their models of chapter 4.

```
% Basic third-order Sigma-Delta modulator

% Number of output samples
nmax=262144;

% Sampling frequency
fs=256000;

% Input signal
amp=0.7;
f=1000;
n=1:nmax;
x=amp*sin(2*pi*f*n/fs);

% Integrator gain factors
a1=0.6;
a2=0.2;
a3=0.5;

% Feedback gain factors
b2=0.75;
b3=1.5;

% Integrator initial states
t=0;
u=0;
v=0;

% Sigma-delta modulator with clipping levels +/-2.5
for n=1:nmax
 intt(n)=t;
 intu(n)=u;
 intv(n)=v;

 % Comparator
 co=sign(v);
 y(n)=co;

 % First integrator
 t=t+a1*(x(n)-co);
  if t>2.5
    t=2.5;
  elseif t<-2.5
    t=-2.5;
  end

 % Second integrator
 u=u+a2*(t-b2*co);
  if u>2.5
    u=2.5;
  elseif u<-2.5
    u=-2.5;
  end

 % Third integrator
 v=v+a3*(u-b3*co);
  if v>2.5
    v=2.5;
  elseif v<-2.5
    v=-2.5;
  end
end
```

```
xx=1:nmax;

% Input signal sigma-delta modulator
figure(1)
plot(xx,x)
xlabel('TIME'),ylabel('IN')
grid

% Output signal sigma-delta modulator
figure(2)
plot(xx,y)
xlabel('TIME'),ylabel('OUT')
grid

% Output signal first integrator
figure(3)
plot(xx,intt)
xlabel('TIME'),ylabel('INT T')
grid

% Output signal second integrator
figure(4)
plot(xx,intu)
xlabel('TIME'),ylabel('INT U')
grid

% Output signal third integrator
figure(5)
plot(xx,intv)
xlabel('TIME'),ylabel('INT V')
grid

% Output histogram first integrator
figure(6)
hist(intt,50)
title('INT T OUTPUT HISTOGRAM')

% Output histogram second integrator
figure(7)
hist(intu,50)
title('INT U OUTPUT HISTOGRAM')

% Output histogram third integrator
figure(8)
hist(intv,50)
title('INT V OUTPUT HISTOGRAM')

% Windowing of the sigma-delta modulator output signal
win=kaiser(nmax,20)';
sumw=sum(win)/2;
% Fast Fourier transform of the result and correct scaling
hh=abs(fft(win.*y))/sumw;

f=(fs/nmax)*(0:(nmax-1)/2);

% Spectral density of the sigma-delta modulator output signal
figure(9)
semilogx(f,20*log10(hh(1:(nmax/2))))
xlabel('FREQUENCY')
ylabel('Spectral density OUT [dB]')
grid
```

Simulation of the signal-to-noise ratio characteristic

This simulation makes a sweep of the sigma-delta modulator input signal, from -120dB to 0dB in steps of 1dB. The sweep starts well below the least significant bit value and ends well above the maximum allowed value of the input signal. The signal-to-noise ratio is calculated with the power of the sinusoidal input signal and the total quantisation noise power in the band of interest, so from DC to f_b. Circuit limitations can be included, according to their models of chapter 4.

```
% Basic third-order Sigma-Delta modulator

% Number of output samples
nmax=262144;

% Sampling frequency
fs=256000;

% Initialisation input signal
f=1000;
amp=1e-6;

% Sweep of the input signal from -120 dB to 0 dB
for i=1:121

 % Input signal
 n=1:nmax;
 x=amp*sin(2*pi*f*n/fs);

 %Integrator gain factors
 a1=0.6;
 a2=0.2;
 a3=0.5;

 %Feedback gain factors
 b2=0.75;
 b3=1.5;

 % Integrator initial states
 t=0;
 u=0;
 v=0;

 % Sigma-delta modulator with clipping levels +/-2.5
 for n=1:nmax
  intt(n)=t;
  intu(n)=u;
  intv(n)=v;

  %Comparator
  co=sign(v);
  y(n)=co;

  % First integrator
  t=t+a1*(x(n)-co);
   if t>2.5
     t=2.5;
   elseif t<-2.5
     t=-2.5;
   end

  % Second integrator
  u=u+a2*(t-b2*co);
   if u>2.5
     u=2.5;
   elseif u<-2.5
     u=-2.5;
   end

  % Third integrator
  v=v+a3*(u-b3*co);
   if v>2.5
     v=2.5;
   elseif v<-2.5
     v=-2.5;
   end
 end

 % Windowing of the sigma-delta modulator output signal
 win=kaiser(nmax,20)';
 sumw=sum(win)/2;

 % Fast Fourier transform of the result and correct scaling
 hh=abs(fft(win.*y))/sumw;

 % Calculating the power spectral density
 kk=hh.*hh;

 % Removing the spectral component of the input signal
 for j=928:1152
   kk(j)=0;
 end

 % Accumulating the spectral noise power components
 gg=cumsum(kk);

 % Noise power and signal power in the band of interest
 noise=10*log10(gg(1229));
 signal=10*log10((amp^2)/2);

 % Calculating the signal-to-noise ratio in dB
 snr(i)=signal-noise;

 % Calculating the magnitude of the input signal in dB
 xx(i)=20*log10(amp);

 % Calculating the next amplitude of the input signal
 amp=10.^((20*log10(amp)+1)/20);
end

% Signal-to-noise ratio characteristic as function of the input signal
plot(xx,snr)
xlabel('IN [dB]'),ylabel('SNR [dB]')
grid
```