Electrical characterization of ferroelectric field-effect transistors

Zinnemers, S.E.

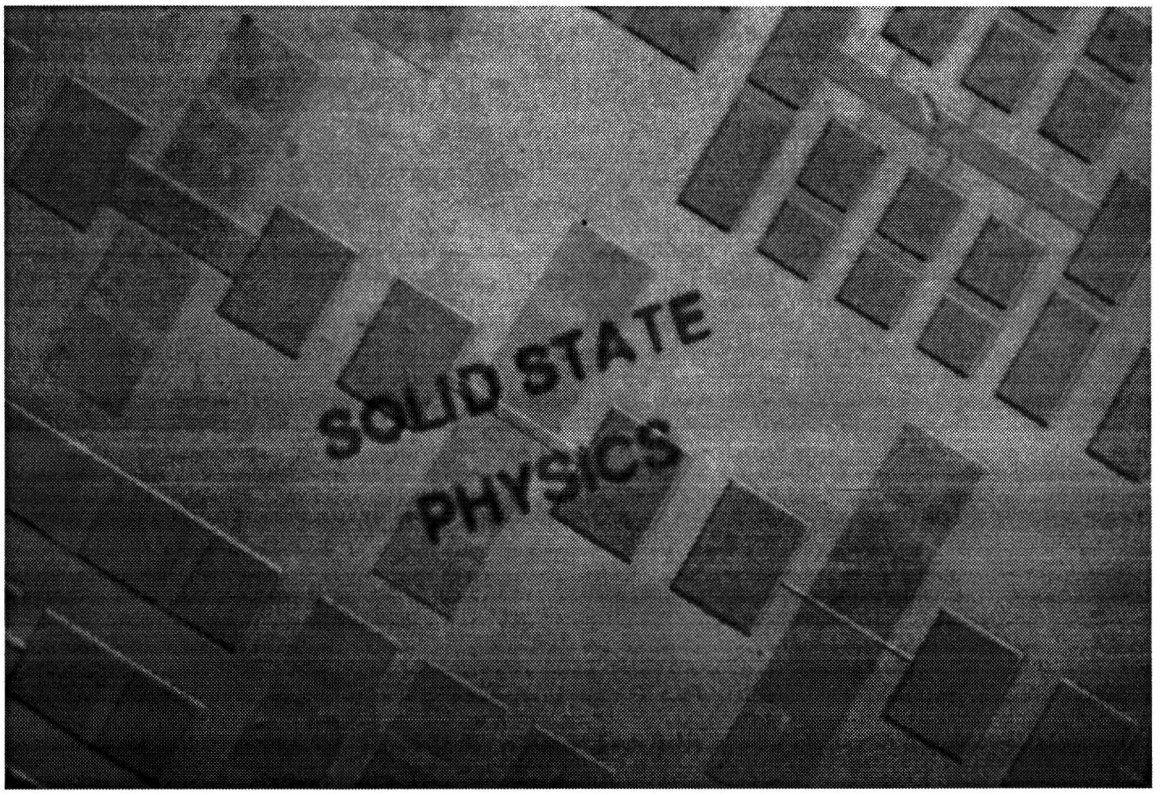
Award date:
1997

Master of Science Thesis
Eindhoven University of Technology
Faculty of Applied Physics
Department of Semiconductor Physics

Electrical characterization of ferroelectric field-effect transistors

S.E.Zinnemers

February 11, 1997



Research carried out from March 1996 to February 1997 at the department
Microsystems Technology, Philips Research Laboratories Eindhoven
Graduation Professor Dr. J.H. Wolter (Eindhoven University of Technology)
Project under supervision of Dr. M.W.J. Prins (Philips)

Abstract

At the department Microsystems Technology of Philips Research Laboratories, the use of thin film oxidic materials for applications is investigated. As a demonstrator device, a ferroelectric field-effect transistor has been developed, using $PbZr_{0.2}Ti_{0.8}O_3$ as material for the ferroelectric insulator and SnO_2:Sb or In_2O_3:Sn as material for the semiconductor channel. The device exhibits a memory effect due to the remnant polarization of the ferroelectric material. The goal of this report is to create a more physical understanding of the operation of the field-effect transistor with the use of an in-depth electrical analysis. Due to properly chosen semiconductor parameters, the transistor channel can be fully depleted, resulting in a difference in conductance of three orders of magnitude between the depleted and the non-depleted state. The presence of a contact resistance is limiting the maximum conductance. Charge injection has been observed but is not of great influence on the channel conductance. Transistor characteristics as device speed, the changes due to repeated switching, the influence of light and temperature behaviour are well understood. The field-effect mobility has been determined as a function of the amount of charge in the transistor channel and is not constant due to the presence of trap states. The mobility in the non-depleted state amounts roughly 2 cm^2/Vs.

Contents

Chapter 1

Introduction

A ferroelectric field-effect transistor is interesting to develop for memory applications. The main advantage of the ferroelectric component in this device is the memory effect, which the ferroelectric material exhibits due to the remnant polarization of the material. In the past, others have tried to develop a ferroelectric field effect device. A first proposal was made by Moll [1], followed by others in the sixties and seventies [2][3], who successfully fabricated a ferroelectric field effect transistor using ceramic ferroelectric materials and thin film semiconductors. A disadvantage of a bulk ferroelectric material is that large voltages (> 100 V) are required to switch the device.

In the group Microsystems Technology (the former group Exploratory Physics) at Philips Research Laboratories, in which this graduation project is performed, a project group *New Oxidic Thin Films* was started in 1990 with the goal to investigate the use of oxidic thin films for applications. Pulsed Laser Deposition turned out to be a suitable method to produce oxidic thin films [4]. Oxidic materials can behave like an insulator, a semiconductor or a metal. To study these oxidic materials a field-effect transistor is developed as a demonstrator device, first with a dielectric insulator and later with a ferroelectric insulator, using $PbZr_{0.2}Ti_{0.8}O_3$ as the ferroelectric material. The use of materials, like $PbZr_{0.2}Ti_{0.8}O_3$, is widespread. For its ferroelectricity, it is mostly used in memory devices, and for its piezoelectricity, for example, in small loudspeakers or in piezo-lighters.

The advantage of a thin film ferroelectric field-effect transistor is that the device is a low-voltage, programmable, non-volatile memory with a non-destructive read-out. The operating voltages are similar to standard IC voltages. Non-volatile means that a particular memory-state is stable in time. These four characteristic properties of the ferroelectric field-effect transistor makes the device exceptional to other memory devices. For example, low-voltage programmable memories, exist already like DRAM (Dynamic Random Access Memory). This memory cell consists out of a transistor (normally a MOSFET) and a capacitor in which charge is stored. The information on the capacitor leaks away in time, and causes the device to be volatile. Also after the read-out of the device, the information is lost. Programmable non-volatile memories also exist, for example ROM's (Read Only Memory). These memories consist mostly out of an EEPROM (Electrically Erasable and Programmable Read Only Memory). This is a so called floating gate device. A disadvantage is that when programming the device, a high voltage is needed (>15 V). The memory-state is defined with a very long retention time (> years).
The use of only oxide materials causes the device to be transparent due to the wide band gap of the materials. This is of interest for on-screen applications. An advantage of this particular application is the low-power consumption of the device, as there is no applied voltage necessary to maintain a certain state, due to the memory effect. Another advantage is the fact that the transistor can be placed in the light-way itself, in stead of silicon transistors which are placed out side of the light way.

In the past the project group *New Oxidic Thin Films* first successfully developed a field-effect transistor with a dielectric insulator, where after the insulator was substituted by a ferroelectric

material [5, 6, 7]. First results were promising and showed a field-effect of three orders of magnitude. In this report we will give an in-depth electrical analysis. After presenting the theory necessary to understand the field-effect of the ferroelectric transistor, device fabrication and the experimental setup are given in chapter 3. In chapter 4 we will present transistor characteristics, including a discussion about the device speed and the presence of a contact resistance. For applications, the endurance or the life-time of a device is always of importance (chapter 5). External influences like light and environment temperature are discussed in chapter 6. In the next chapter the time relaxation will be investigated, as it is important to have knowledge about the life-time of a memory-state when the device is switched to it. The field-effect mobility as a function of the amount of charge carriers in the semiconductor channel is discussed in chapter 8. A few experiments are automized using LABVIEW (a graphical oriented programming language), which are described in appendix A. Posters presented during this graduation project, and a published article in *Applied Physics Letters* are given in appendix C.

Chapter 2

Theory

In this chapter we will discuss the operation of a ferroelectric field-effect transistor. The field effect in the semiconductor is caused by the charge displacement of the insulator which depends not only on the applied voltage across the insulator but also on the time evolution of the applied voltage. After introducing the principle of ferroelectricity, we will explain the operation of the transistor in a simple way, followed with a more physical treatment. Concluding the chapter we sum up requirements for good transistor behaviour and discuss the device speed.

2.1 Ferroelectricity

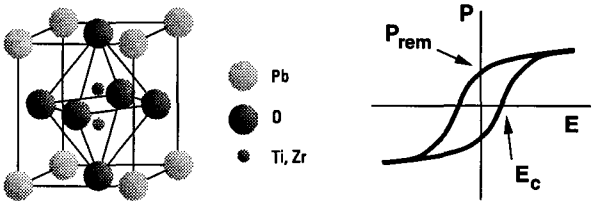


Figure 2.1: (a) Crystal structure of PZT and (b) typical hysteresis curve

An example of a unit cell of a ferroelectric material ($Pb(Zr,Ti)O_3$) is depicted in figure 2.1(a). It is energetically favourable for an ion (Zr or Ti) to be positioned off-center and therefore two energetic states are possible which can cause a positive or negative dipole-moment, even in the absence of an external field. The total electrical dipole moment per volume unit, or polarization, is designated as P. A typical plot of polarization vs. electrical field is shown in figure 2.1(b). When applying an electrical field to the crystal, the dipole moments will line up to the field direction. When all of the dipole moments are lined up to the field, the ferroelectric material is saturated. Increasing the field will only result in a dielectric behaviour of the ferroelectric material and therefore there is no hysteresis behaviour. After decreasing the electrical field to zero, there will be a remnant polarization, P_{rem}. A coercive field E_c is necessary to reduce the polarization to zero. Note that there is hysteresis (P vs. E) which is similar to ferromagnetic hysteresis (M vs. H).
Although $PbZrO_3$ or $PbTiO_3$ alone exhibit ferroelectricity, a combination of these two materials is often used to adjust the hysteresis behaviour. $PbTiO_3$ has a very rectangular hysteresis curve and adding Zr to the compound the curve will become more slim.

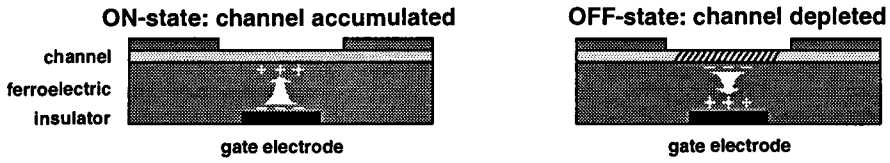


Figure 2.2: Schematic representation of the ON- and OFF-state for an n-type semiconductor channel.

2.2 Transistor on- and off-state

Corresponding to a bottom-gate thin film field-effect transistor our device has a semiconductive layer (called the channel) separated from a metal (the gate electrode) by a ferroelectric insulator. By applying a voltage to the gate electrode with respect to the channel, we can change the direction of the polarization in the insulator. The polarization modulates the number of charge carriers in the channel. As the polarization can either be in the up or down direction, there are two memory states (see figure 2.2). If the polarization is directed upwards (indicated by the arrow), the channel is accumulated with charge carries (defined as the ON-state) in case of an n-type semiconductor. When the direction of the polarization is reversed, charge carriers are repelled and the channel is depleted (the OFF-state). The mentioned accumulation and depletion involve bending of the energy bands in the semiconductor.
First we will describe the band-bending in a semiconductor when it is brought into contact with an insulator, followed by an energy-band-diagram to explain the mentioned states.

2.3 Band-bending

When a metal and a semiconductor separated by an insulator, are brought into contact, the Fermi levels will line up in equilibrium. If the metal is brought to a certain potential, the band-structure in the semiconductor will bend corresponding with the creation of a sheet of charge at the semiconductor/insulator interface.
Suppose that there is a surface potential at the insulator/semiconductor interface, V_{bb}, such that the semiconductor is depleted over a thickness W. If we take the surface potential negative, the electrons in the semiconductor will form a charge sheet Q^- at the metal/insulator interface. In the semiconductor a mirror charge Q^+ (i.e., the non-mobile positive ions) will be attracted.

$$Q^+ = eN_D W, \tag{2.1}$$

with N_D the doping concentration, under the depletion approximation that the donors are fully ionized, and neglecting grain-boundary states.
An electric field E in the semiconductor is formed due to the positive charge, with Poisson's equation:

$$\frac{dE}{dx} = \frac{eN_D}{\epsilon_0 \epsilon_r}, \tag{2.2}$$

with ϵ_0 the permittivity of free space and ϵ_r relative dielectric constant of the semiconductor.
Using $\frac{d^2V}{d^2x} = -\frac{dE}{dx}$, we find an expression for the potential distribution V:

$$V(x) = -\frac{eN_D}{\epsilon_0 \epsilon_r}\left[\frac{x^2}{2} - Wx\right]. \tag{2.3}$$

The equation shows that if the distance to the interface increases, the potential also increases. Thus the band-bending at a position x decreases if the distance to the interface increases. If the total band-bending voltage is V_{bb}, the depletion width W is given by:

$$W = \left(\frac{2\epsilon_0 \epsilon_r V_{bb}}{eN_D}\right)^{1/2}. \tag{2.4}$$

The band-bending in the transistor is similar. A surface potential at the interface caused by the ferroelectric polarization will bend the bandstructure in an identical way.

2.4 Energy band-diagram and depolarization field

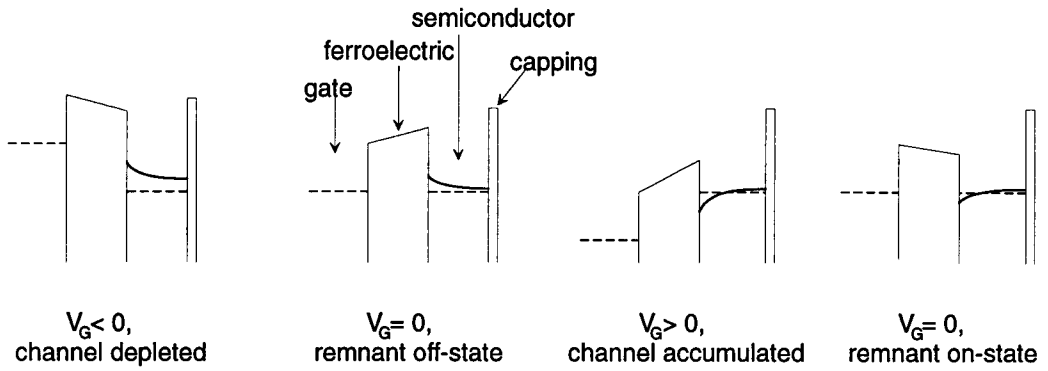


Figure 2.3: Band diagram of four different state of the transistor.

The operation of the field-effect transistor can be described by means of an energy band-diagram (Fig. 2.3). In the figure the gate voltage is altered, resulting in four transistor states. In the figure a capping layer is also depicted to illustrate the finite thickness of the thin semiconductor film. When a negative gate voltage is applied, the conduction band edge of the semiconductor will bend upwards. Charge is repelled in this region. After removing the gate voltage, a remnant state will be present. This is defined as the OFF-state. Applying a positive gate voltage the conduction band will bend through the Fermi-level, accumulating charge. When no gate voltage is present, the band is bent less although accumulation is still noticeable. This state is defined as the ON-state.
Note that the energy band of the ferroelectric insulator has a different slope and opposite of sign when V_G=0 than when a gate voltage is a applied. This is called the depolarization effect. When the corresponding depolarization field becomes too large, the system is unstable and the ferroelectric film will depolarize. When a ferroelectric capacitor is short-circuited, charge carriers in the electrodes will compensate the polarization charge. The screening-length of the compensating charge will be much smaller in a metal than in a semiconductor due to the large charge density of the metal. Therefore the band-bending of the semiconductor causes the depolarization field which becomes large as the insulator thickness decreases. Thus, in bulk ferroelectric materials this depolarization field is small as has been reported by others [8][9]. Using a differential form of Gauss's law, we find an expression for the field in the ferroelectric layer E_{FE}:

$$\sigma_{SC} = \epsilon_0 E_{FE} + P_{FE}, \tag{2.5}$$

with σ_{SC} the areal charge density in the semiconductor and P_{FE} the polarization of the ferroelectric layer. This equation shows that when there is not enough charge inside the semiconductor, the field in the ferroelectric can become equal to P_{FE}/ϵ_0 and opposite of sign.

2.5 Channel conductance and field-effect mobility

Using a band-conduction model, the drain current is proportional to the amount of charge carriers in the conduction band, with a mobility μ. The drain-current I_D increases as the polarization will induce more charge in the channel, under the assumption that there are no gap-states present:

$$I_D = \frac{W}{L} V_D \mu \left(\tilde{Q}_0 + \Delta \tilde{Q}_G \right), \tag{2.6}$$

with W and L the width and length of the channel, V_D source-drain voltage, μ the field-effect mobility, $\tilde{Q}_0$ the available charge and $\Delta\tilde{Q}_G$ the charge induced by the gate.
The equation above can be expressed in a geometry independent way, by introducing the sheet conductance $G_\square$:

$$G_\square = \frac{L}{W}\frac{I_D}{V_D} = \mu\left(\tilde{Q}_0 + \Delta\tilde{Q}_G\right). \tag{2.7}$$

This equation no longer holds when there are gap-states present. The charge $\Delta\tilde{Q}_G$ induced in the semiconductor, can also fill gap-states with a mobility of zero. The field-effect mobility μ is defined as the increase of conductance due to the increase of charge carriers per unit area $\tilde{Q}$:

$$\mu = \frac{\partial G_\square}{\partial \tilde{Q}}. \tag{2.8}$$

To find an expression for the mobility as a function of V_G, we differentiate equation 2.6 with respect to $\Delta\tilde{Q}_G$, defined as the transconductance, g_m:

$$g_m = \frac{\partial I_D}{\partial \Delta\tilde{Q}_G} = \frac{W}{L}V_D\mu. \tag{2.9}$$

$\Delta\tilde{Q}_G$ depends on the gate voltage V_G as follows:

$$\Delta\tilde{Q}_G = \tilde{C}_G(V_G)\ V_G = \frac{C_G(V_G)}{A_G}V_G, \tag{2.10}$$

with $\tilde{C}_G(V_G)$ the differential capacitance of the insulator per unit area, $C_G(V_G)$ the differential capacitance of the insulator, both as a function of gate voltage and A_G the area of the capacitor. For convenience $\tilde{C}_G(V_G)$ and $C_G(V_G)$ will further be denoted as $\tilde{C}_G$ and C_G.
Combining equations 2.9 and 2.10 we get:

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{W}{L}V_D\frac{C_G}{A_G}\mu. \tag{2.11}$$

We then get a mobility μ (taking $A_G = LW$):

$$\mu = \frac{L^2}{V_D}\frac{g_m}{C_G}. \tag{2.12}$$

When we change the charge displacement, the Fermi-level will shift through the energy bands. If, for example, the Fermi-level shifts upwards, more charge carriers are created in the conduction band with a certain mobility μ. This mobility is constant whether the Fermi-level is in the band or underneath the conduction band.
We have to reconsider this statement if we assume the possibility of gap-states. Suppose the Fermi-level is situated below the conduction band. An increase of the Fermi-level would create charge carriers in the band with a mobility μ or charge in a gap-state with a very low mobility. If the Fermi-level would lie in the band, all of the created charge due to an increase of Fermi-level would have a constant mobility μ, for the gap-states are totally filled.
We can conclude that the mobility is not constant as a function of the gate voltage if gap-states are present.
In this section we discussed the operation of a field-effect transistor with a ferroelectric insulator briefly as the ferroelectric behaviour is not a clear function of the applied gate voltage, in contrast of transistors with a dielectric insulator [10]. Modeling can give more insight as has been done by Rep [11].

2.6 Subthreshold behaviour of the semiconductor channel

Assuming a constant mobility μ in the conduction band, we can calculate the conductivity σ:

$$\sigma = n(\tilde{Q})\ e\ \mu, \tag{2.13}$$

where $n(\tilde{Q})$ is the amount of charge carriers in the semiconductor channel as a function of the displaced charge in the insulator and e the elementary charge.
When the charge displacement is altered, the energy bands will bend and the Fermi-level is shifting through the conduction band. Suppose that the Fermi-level is positioned underneath the conduction band. Charge carriers are then thermally excited in to the conduction band, or, in other words, the amount of charge carriers $n(\tilde{Q})$ in the channel, are Boltzmann distributed with respect to the energy difference between conduction band and Fermi-level $\Phi(\tilde{Q})$ (see figure 2.4 for a graphical definition):

$$n(\tilde{Q}) \sim e^{-\Phi(\tilde{Q})/kT}, \tag{2.14}$$

where k the Boltzmann factor is, and T the temperature.

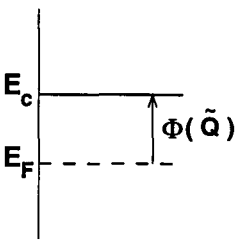


Figure 2.4: The potential Φ is defined as the difference between the conduction band energy E_c and the Fermi-level E_F (E_c-E_F).

The conductivity of the channel increases exponentially with the $\Phi(\tilde{Q})$. When the Fermi-level is positioned above the conduction band, the charge displacement in the insulator will directly induce charge carriers in the conduction band, according to $G_\square = \mu\Delta\tilde{Q}$ (equation 2.7). The channel conductivity is now linearly related to the charge displacement.
Neglecting initial band-bending we can conclude that for a negative charge displacement the conductance depends exponentially on the displaced charge and for a positive charge displacement the conductance depends linear on the displaced charge. The exponential dependence of conductance on $\tilde{Q}$ is called the subthreshold behaviour [10]. In a field-effect transistor with a dielectric insulator, the subthreshold behaviour simplifies to an exponential dependence of conductance on the gate voltage.

2.7 Charge injection

A common phenomenon in field-effect devices is charge injection into trap states in the insulator [12]. Even devices have been developed which operate with the use of this principle (e.g., floating gate transistor [10]).
When we apply a positive gate voltage, charge carriers are attracted to the ferroelectric layer and can even be trapped in the ferroelectric layer (i.e., charge injection). Removing the gate voltage, the injected charge will not immediately relax but it will take a certain time. The relationship between the electrical field in the semiconductor E_{sc} due to the ferroelectric displacement D_{FE} is given by a differential form of Gauss's law:

$$\epsilon_0\epsilon_{sc}E_{SC} = \tilde{Q}_{inj} + D_{FE}, \tag{2.15}$$

with $\tilde{Q}_{inj}$ the injected charge per unit area and ϵ_{SC} the relative permittivity of the semiconductor. Note that Q_{inj} and D_{FE} can be of opposite sign (see figure 2.5), so injected charge causes a reduction of charge induction in the semiconductor film. In other words, the ON-state current will decrease and the OFF-state current will increase. In figure 2.6 the polarization P, and the injected charge Q_{inj}, vs. the gate voltage are plotted. The form of the charge injection curve has been chosen similar to [12]. Note that the circulation direction of the two curves is different. In this

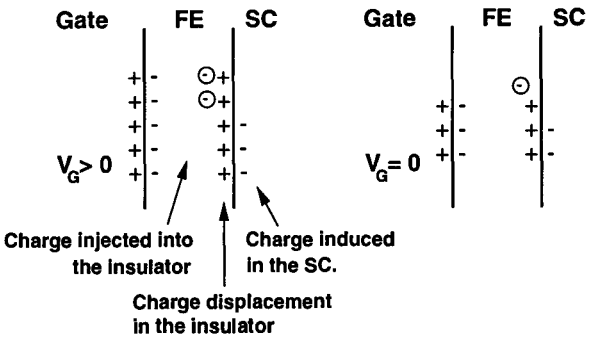


Figure 2.5: Schematic representation of charge injection

case, at $V_G = 0$V, Q_{inj} equals P (as was reported in [3], for example). In a good device, the size of Q_{inj} is smaller than P.

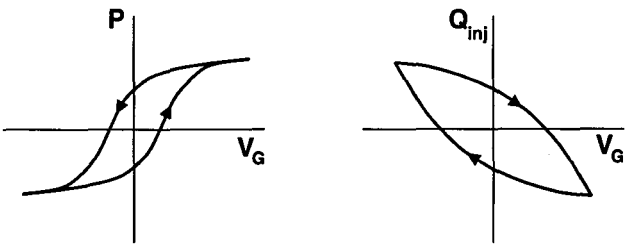


Figure 2.6: Polarization and injected charge vs. electrical field. Both axes are in arbitrary units.

2.8 Requirements for good transistor behaviour

For good transistor behaviour one should take two conditions into account for the total charge, $\tilde{Q}_{SC}$, in the semiconductor and for the band-bending potential, V_{bb}.

- $\tilde{Q}_{SC} = eN_D t_{SC} < P_{rem}$,
- $V_{bb} = \frac{eN_D}{2\epsilon_0\epsilon_r} t_{SC}^2 < V_c$.

The first condition is that the amount of charge in the semiconductor should be smaller than the remnant polarization, otherwise it will be impossible to deplete the channel. Secondly the band-bending potential should not become too large to cause depolarization effects.
Taking $P_{rem} = 20\ \mu$C/cm^2, $V_{bb} = 2$ V we can draw the conditions into figure 2.7. The transistor can only be depleted if the parameters (N_D and t_{SC}) are positioned to left-bottom of the two lines. Using practical minimum values for film thickness (larger than 5 nm) and doping concentration (larger than 10^{18} cm^{-3}), we can draw an area of most interest for the transistor. A maximum ON-state current will occur when N_D is as large as possible (indicated with the black area). The figure shows that in this particular case the band-bending potential and not the remnant polarization, limits the parameters.

2.9 Device speed

The device speed depends on several time factors, namely the time that is needed for polarization switching (< 1 ns [13]), the time for transport of charge through the interface layer, and the time

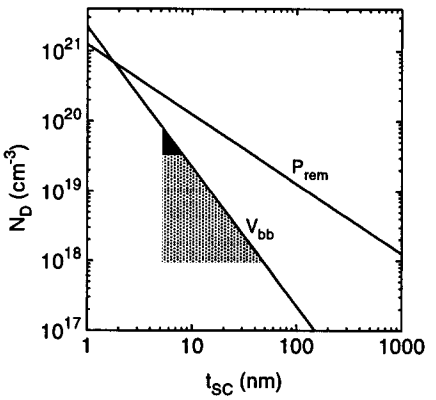


Figure 2.7: Requirements for good transistor behaviour. The shaded triangle shows area for optimum performance.

for transport of charge through the semiconductor. The ferroelectric polarization switching has been measured at a capacitor with metal electrodes. We assume that interface layers, like Schottky barriers, are not present in the device. The device has a semiconductive channel through which the charge has to move, which has a much higher resistivity than that of a metal. Thus, when we assume that transport of charge through the semiconductor causes the dominant time factor, we can deduce an approximation of the switching time for the transistor.
We have to know how fast the polarization can be switched from one direction to the opposite direction. Or, in other words, how fast can an amount of charge ($\tilde{Q}_{switch}$ times the gate area LW) move from one side to the other. If we assume that when we apply a gate voltage, the voltage at the insulator/semiconductor interface will be the same, then a current will flow: $I = R/V_G$, with R the maximum resistance of the channel. After a time τ all charge is switched, and therefore the polarization has reversed direction.

$$\tau = \frac{\Delta Q}{I} = \frac{\tilde{Q}_{switch} LW R_{max}}{V_G}, \tag{2.16}$$

where ΔQ equals the switch charge, R_{max} the maximum resistance in the circuit (i.e., the resistance of the channel when it is depleted) and V_G the applied gate voltage.
Or if we take the field-effect mobility constant (which can occur if there are no gap states or when the channel is not fully depleted), the minimum switching time yields:

$$\tau = \frac{L^2}{V_G \mu}. \tag{2.17}$$

It is also of interest, in what way the device will respond to gate voltage pulses smaller than the minimum switching time, τ. The minimum switching time is proportional to (see equation 2.16):

$$\tau \sim \tilde{Q}_{switch} R_{max} = \tilde{Q}_{switch}/G, \tag{2.18}$$

where G is the minimum conductance of the channel.
In the section 2.6 we showed that with only a small change in the displaced charge the channel conductance changes exponentially. So in the case of partially switching, we can assume that when a voltage pulse is applied, the total switched charge is still roughly the same as in totally switching. Therefore the switching time τ is proportional to the reciprocal conductance:

$$\tau \sim G^{-1}. \tag{2.19}$$

This equation shows that when a voltage pulse is applied with a pulse width smaller than the minimum required pulse width, the channel conductance will end up to be larger than the minimum conductance of the channel.

Chapter 3

Experimental

3.1 Device description

The fabricated wafers can be divided into 2 classes which are with respect to the insulator film:

- Transistors with a ferroelectric insulator. Devices consist of a thin film ferroelectric insulator ($PbZr_{0.2}Ti_{0.8}O_3$, thickness in the order of 100 nm) with a patterned gate electrode, or of a bulk ceramic ferroelectric insulator ($PbZr_{0.5}Ti_{0.5}O_3$, thickness in the order 100 μm) with a common gate electrode.
  A preliminary study has been made to investigate the use of spun materials, using a spun semiconductor layer on a bulk ferroelectric insulator ($PbZr_{0.5}Ti_{0.5}O_3$, thickness in the order 100 μm).

- Transistors with a dielectric insulator, consisting of a SiO_2 or $BaZrO_3$ insulator with thicknesses in the order of 100 nm, and a common gate structure.

Although the purpose of the *New Oxidic Thin Film* project is to produce an operating transparent all-oxide transistor, other materials than thin films films or non-oxides have been used. However the semiconductor layer is always a thin film using SnO_2:Sb or In_2O_3:Sn. As most of the thin films are grown with pulsed laser deposition, we will first discuss the principle of this deposition method, followed with a description of the fabricated devices.

3.1.1 Pulsed laser deposition

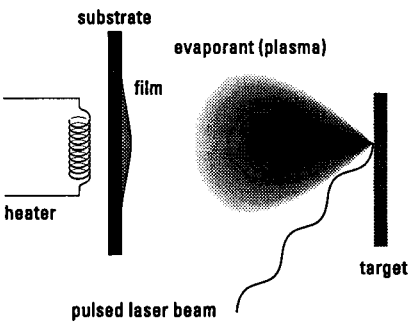


Figure 3.1: Schematic representation of pulsed laser deposition method.

The pulsed laser deposition (PLD) principle is schematically given in figure 3.1. A pulsed laser beam (pulse width 15 ns, frequency 3 Hz) is focussed on a rotating target. The beam will evaporate the target material. Species of the induced plasma will deposit on the substrate. The substrate

is heated in order to obtain a high surface mobility. An oxygen partial pressure (0.2 mbar) is maintained in order to restore oxygen deficiencies. $SrRuO_3$ and $PbZr_{0.2}Ti_{0.8}O_3$ layers are grown at a deposition temperature of 600 °C c.q. 575 °C; as the semiconductor layers (SnO_2:Sb or In_2O_3:Sn) are grown at a deposition temperature of approximately 500 °C.
The advantage of PLD is that multiple layers directly and *in-situ* can be grown when the target materials are available. This is unlike other deposition methods, like MBE, where first effort has to be made to compose the right concentrations in the supply-containers. A disadvantage of PLD is the small deposition area, resulting in small wafers (smaller than one inch). Concluding, PLD is suitable for easy change of materials but not suitable for the production of devices.

3.1.2 Thin film ferroelectric field-effect transistor

A bottom gate thin film device has been produced using all-oxide materials to obtain transparency. In order to grow an epitaxial gate and insulator layer on the substrate, the gate layer is first deposited, whereafter insulator and semiconductor layers are deposited. In IC technology it is common that the gate layer is deposited on top of the insulator layer instead at the bottom of the device. The semiconductor layer is a polycrystalline material as has been investigated by Grosse-Holz et al. [14]. The lithographic process to fabricate a device is as follows (a more detailed description is given in [15]):

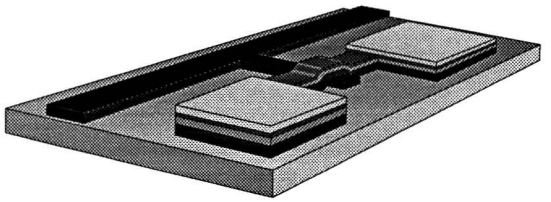
- On a polished $SrTiO_3$ crystal (100) the gate material ($SrRuO_3$) is deposited. After a molybdenum layer is sputtered, a resist mask is spun. The desired pattern is defined with photolithography. The molybdenum layer is structured with reactive ion etching using a CF_4/O_2 plasma. The $SrRuO_3$ is etched away with a CHF_3/Ar plasma. The resist is removed with acetone whereafter the molybdenum leftovers are removed with an aqueous solution of $K_4Fe(CN)_6/H_2O_2$.
- After depositing (PLD) the $PbZr_{0.2}Ti_{0.8}O_3$ layer, semiconductive layer and its capping, a molybdenum mask is sputtered and patterned to define source, drain and the channel.
- In order to remove the semiconductor layer with its capping between the different devices at the wafer, the layers are etched away with CHF_3/Ar.
- To contact the gate, first a resist is spun, whereafter the $PbZr_{0.2}Ti_{0.8}O_3$ layer is etched away with CHF_3/Ar.
- Finally, to separate source and drain, a spun resist is patterned and molybdenum on top of the channel is removed with an aqueous solution of $K_4Fe(CN)_6/H_2O_2$. The resist is removed with acetone.

This process results in a non-total transparent device as there are molybdenum contact pads. To obtain an all transparent device using highly doped In_2O_3:Sn as source-drain contact material, two other process steps are used after making contactholes to the $SrRuO_3$ layer.

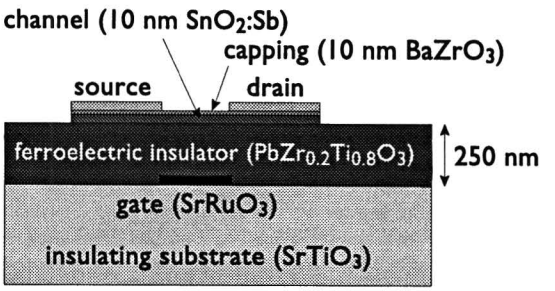
- After spinning resist, molybdenum on top of the contact pads is removed with an aqueous solution of $K_4Fe(CN)_6/H_2O_2$, whereafter an In_2O_3:Sn layer is sputtered.
- After dry etching the In_2O_3:Sn contact pads, molybdenum on top of the channel is removed to separate source and drain.

Two kinds of masks (called FET1 and FET2) are used, each containing several structures with different geometries, like metal/insulator/semiconductor diodes, Hall bars, transistors and resistance test structures. In appendix B the layout of the two mask sets is given.

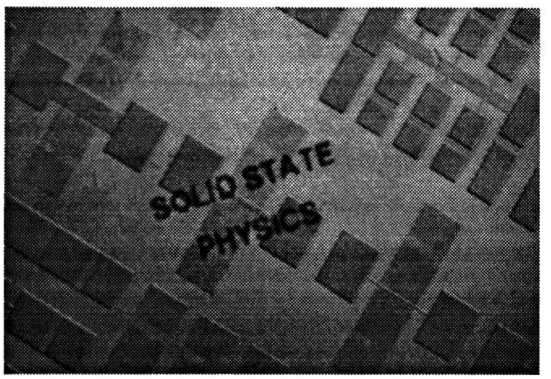
The layout and a cross-section of the device are depicted in figure 3.2 as well as a TEM picture and a photograph. In the photograph the text SOLID-STATE PHYSICS is placed under the wafer. Light shining through the wafer from the bottom, shows that the device is optically transparent. Table 3.1 gives a summary of the produced wafers with their characteristic parameters.



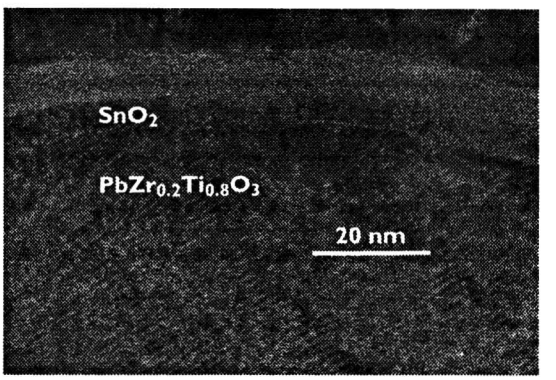
(a) The device layout.



(b) Cross section of the device



(c) Photograph of the device, the text SOLID STATE PHYSICS is placed under the wafer.



(d) TEM picture of the device.

Figure 3.2: The thin film transparent field-effect transistor.

Transistor	Wafer	t_{gate} nm	t_{PZT} nm	t_{SC} nm	Sb doping cm^{-3}	t_{BZO} nm
A_{thin}	JC5376	140	250	10	$4\ 10^{19}$	10
B_{thin}	JC5404	35	350	25	$8\ 10^{18}$	10
C_{thin}	JC5375	110	250	10	$4\ 10^{19}$	10
D_{thin}	JC5383	50	225	5	$4\ 10^{20}$	10
E_{thin}	JC5386	20	250	12	$4\ 10^{19}$	10
F_{thin}	JC5401	35	350	10	$4\ 10^{19}$	10
G_{thin}	JC5463	35	350	15	$4\ 10^{19}$	10
H_{thin}	JC5385	20	250	7.5	$4\ 10^{20}$	10

Table 3.1: Wafer number, thickness of the gate layer (t_{gate}), the $PbZr_{0.2}Ti_{0.8}O_3$ insulator (t_{PZT}), the semiconductor layer (t_{SC}), doping concentration, thickness of $BaZrO_3$ capping layer (t_{BZO}) of all thin-film devices.

3.1.3 Field-effect transistor with a bulk ferroelectric insulator

Besides a thin film ferroelectric field-effect transistor, another field-effect transistor has been fabricated, containing a ceramic bulk ferroelectric insulator ($PbZr_{0.5}Ti_{0.5}O_3$), made with a sinter process (thickness is 0.18 mm). As a semiconductor, In_2O_3:Sn has been used with two different doping-concentrations. After structuring the semiconductor layer with its capping, molybdenum contact pads are sputtered. The bottom side of the bulk ceramic material contains a nickel-alloy electrode. This sandwich is glued with a silver-powder suspension on a circuit board. The nickel-alloy electrode will function as the gate electrode (i.e., a common gate structure). In table 3.2 a summary of characteristic parameters is given.

Transistor	Wafer	t_{FE} μm	t_{SC} nm	Sn doping cm^{-3}	t_{BZO} nm
A_{BULK}	JC5503	180	20	$2\ 10^{20}$	10
B_{BULK}	JC5533	180	15	$2\ 10^{18}$	25
C_{BULK}	JC5550	180	10	$2\ 10^{18}$	25

Table 3.2: Wafer number, thickness of bulk ferroelectric insulator (t_{FE}), semiconductor thickness (t_{SC}), doping concentration, thickness of $BaZrO_3$ capping layer (t_{BZO}).

In the structuring process of wafers $B_{BULK}$and C_{BULK} an extra process step was inserted. Before sputtering molybdenum contact pads the wafers are dipped in HCl for 1 min. c.q. 3 min. in order to etch the $BaZrO_3$ layer. This has been done to investigate the possibility that the $BaZrO_3$ layer would form a contact resistance.

3.1.4 Field-effect transistor using spin-deposited materials

A SnO_2 layer is spun upon a bulk ceramic $PbZr_{0.5}Ti_{0.5}O_3$ layer, whereafter it is annealed at 500 °C for a few hours. The bottom of the bulk ceramic material contains a nickel-alloy, which will function as the gate electrode. This sandwich is glued on a circuit board with a silver-powder solution. In table 3.3 characteristic parameters are given.

Transistor	t_{PZT}	t_{SC} nm	Semiconductor	doping cm^{-3}
A_{spun}	180 μm	10	SnO_2	–

Table 3.3: Ferroelectric insulator thickness (t_{PZT}), semiconductor thickness (t_{SC}), semiconductor material, doping concentration. At the wafer, there is no capping layer present.

3.1.5 Thin film field-effect transistor with a SiO_2 insulator

For the purpose of a possible gassensor, a SnO_2:Sb layer without a $BaZrO_3$ capping layer is deposited on Si/SiO_2 substrate (see table 3.4). Punching through the SiO_2 layer with a large voltage (>200 V) will contact the Si common gate. The thickness of the SiO_2 layer is 400 nm.

Transistor	Wafer	t_{SiO_2} nm	t_{SC} nm	Sb doping cm^{-3}	t_{BZO} nm
A_{Si}	JC5551	400	10	$8\ 10^{18}$	–

Table 3.4: Wafer number, insulator thickness (t_{SiO_2}), semiconductor thickness (t_{SC}), doping concentration, thickness of $BaZrO_3$ capping layer (t_{BZO}).

3.1.6 Thin film field-effect transistor with a $BaZrO_3$ insulator

A SnO_2:Sb layer without a $BaZrO_3$ capping layer is deposited on a $BaZrO_3$ layer which will function as the insulator. The $SrRuO_3$ layer is patterned and functions as the gate electrode. In table 3.5 a summary of the characteristic parameters is given.

Transistor	Wafer	t_{gate} nm	t_{BZO} nm	t_{SC} nm	Sb doping cm^{-3}
A_{BZO}	JC5184	88	300	100	$8\ 10^{18}$

Table 3.5: Wafer number, gate layer thickness (t_{gate}), $BaZrO_3$ insulator thickness (t_{BZO}), semiconductor thickness (t_{SC}), doping concentration. No capping layer is present.

3.2 Measurement techniques

3.2.1 Measurement environment

The wafer to be characterized is placed in a closed compartment, which gives the possibility to insert a particular gas. Using micromanipulators with golden probes, contact can be made to the contact pads.
To measure at higher temperatures than ambient, a hotplate (3 cm diameter) is used. This hotplate is mounted onto an adapted brick in which space has been made for supply wires as well as for a thermo-couple. The maximum temperature of this hotplate exceeds 1000 °C. For low temperature measurements a cryostat is used, where a helium flow cools the wafer down to temperatures of 10 K.
For the bulk ceramic wafers a voltage amplifier (gain factor = 100, max. 600 V) is used to apply a voltage to the gate electrode. The amplifier has been fabricated inside the laboratory.

3.2.2 Transfer characteristic measurement

The relationship between I_D and V_G is called the transfer characteristic. Using a HP Semiconductor Parameter Analyzer 4155A it is possible to set and measure current or voltage at the same time. In this case a voltage V_G is applied to the gate electrode and a drain voltage to the drain electrode. The source electrode is connected to the ground. In figure 3.3 the electrical circuit is depicted to measure the transfer characteristic.

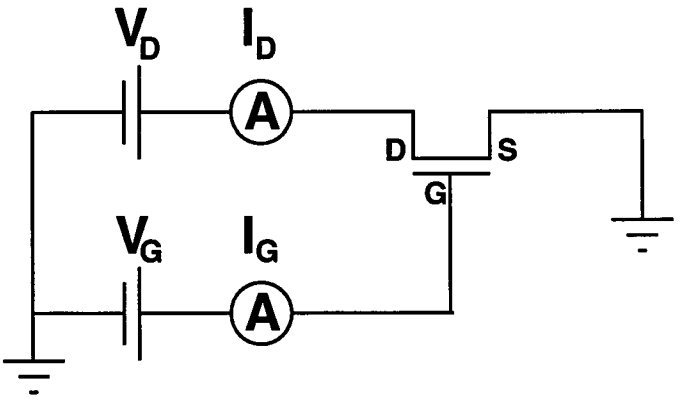


Figure 3.3: Electrical circuit for the transfer characteristic measurement.

3.2.3 Polarization hysteresis measurement

Ferroelectric behaviour can be characterized with a Sawyer-Tower circuit (see figure 3.4) [16]. A reference capacitor C_{ref} is placed in series with the ferroelectric capacitor. By applying an AC voltage (using a Philips PM5139 function generator) the displaced charge will cause a voltage drop over C_{ref}. The applied voltage is monitored at the x-axis of a Tektronix TDS320 oscilloscope, while the reference voltage is monitored at the y-axis of the scope.
To a good approximation, the polarization P is given by the amount of charge at the reference capacitor per unit area:

$$P \approx \frac{V_{ref} C_{ref}}{A}, \tag{3.1}$$

where V_{ref} is the voltage drop over the reference capacitor and A the area of the ferroelectric capacitor.
We have taken the polarization, P, equal to the displaced charge per unit area D using a differential form of Gauss's law: $D = \epsilon_0 E + P$, neglecting the term $\epsilon_0 E$. Taking typical values of a $PbZr_{0.2}Ti_{0.8}O_3$ material for E ($\sim 10^6$ V/m) and P (~ 0.2 C/m^2), we get that $\epsilon_0 E$ is much smaller than P ($9\ 10^{-6}$ C/m$^2 \ll 0.2$ C/m^2), causing equation 3.1 to be valid.

This measurement has been automatized with LABVIEW (see for a description appendix A.2). Note that instead of a ferroelectric capacitor also a transistor can be used for this experiment. At the source electrode the AC voltage is applied and the gate electrode is connected to the reference capacitor, while the drain electrode is floating.

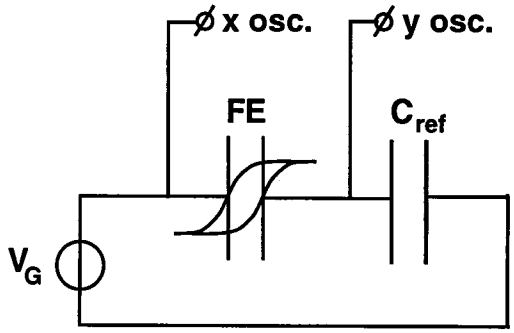


Figure 3.4: Sawyer-Tower circuit

Three conditions have to be taken in account, for a correct measurement of the hysteresis:

- $\omega \gg (R_{oscilloscoop} C_{ref})^{-1}$: charge on the reference capacitor should not discharge over the oscilloscope,
- $\omega \ll (R_{series} C_{ref})^{-1}$: charge must be given a certain transfer time limited by a possible series resistance,
- $C_{ref} \gg C_{ferroelectric}$: the applied voltage must drop across the ferroelectric capacitor with a negligible drop across the reference capacitor.

3.2.4 Pulse measurement

To determine the switching speed of the device a so called pulse measurement has to be carried out. With the HP8161a pulse generator a positive voltage pulse with a pulse width and pulse height is applied to the gate. After a delay time of 5 seconds, the drain current is measured using the HP Semiconductor Analyzer HP4155A. Then a negative voltage pulse with the same height and pulse width is applied. The drain current is again measured. The ON-state and OFF-state currents are now determined at one specific voltage pulse. Varying the pulse width at a constant pulse height,

will give the minimum switching speed and varying the pulse height at a constant pulse width will give the minimum voltage needed to switch the transistor from one state to the other (see also appendix A.3).

3.2.5 Endurance measurement

To determine the endurance (i.e., the resistivity to repeated switching of the device), a squarewave is applied to the gate using a Philips PM6666 pulse generator. A programmable counter counts the number of cycles (i.e., number of waves). At certain intervals the squarewave is switched off, and voltage pulses are applied to the gate to determine the source-drain current in either two states. (For a explanation of the software see A.4.)

3.2.6 Relaxation measurement

To study the time evolution of the drain current, we have to perform a relaxation measurement. The drain current is sampled every 5~10 seconds with the HP4155A after a voltage pulse with a given pulse height and pulse width is applied to the gate. This can then be repeated for other voltage pulses varying the pulse height or pulse width. It is also possible to set a bias voltage at the gate electrode (see for LABVIEW description A.5).

3.2.7 Measurement of gate capacitance and transconductance

With the aid of equation 2.12, we can determine the mobility if we can determine the transconductance and the capacitance of the transistor. It is useful to define the admittance, Y:

$$Y = \frac{I}{V} = G + j\omega C, \tag{3.2}$$

where G is the measured conductance, ω the radial frequency and C the measured capacitance. Using a HP Impedance Analyzer HP4192a, we can determine the admittance. The analyzer has four probes, and operates as follows. The analyzer sets an AC voltage, V_{osc}, with a bias voltage (V_G) at output H_{cur} and measures the current, I, flowing from L_{cur} to ground. The voltage is measured over probes H_{pot} and L_{pot}. It then calculates the admittance, and puts this output on a display.

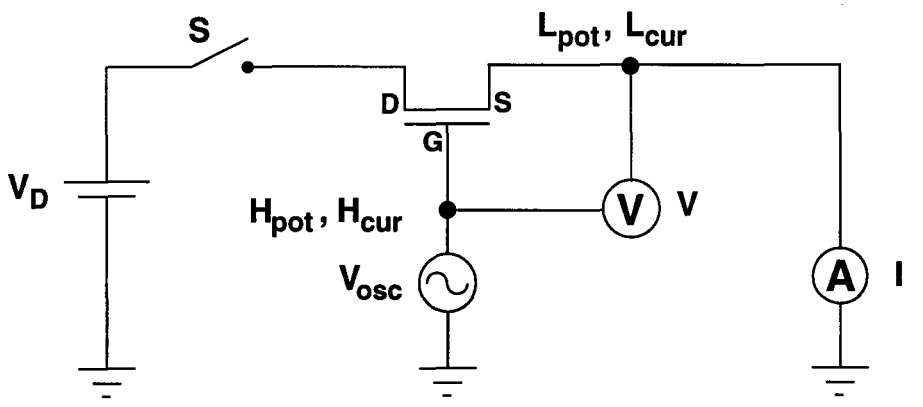


Figure 3.5: Gate capacitance measurement (switch S open) or transconductance measurement (switch S closed) setup for the transistor. H_{pot}, L_{pot}, H_{cur} and L_{cur} are probes used by an impedance analyser, V and I are the measured voltage c.q. current.

In figure 3.5 a schematic representation is given of the four probes connected to a transistor. When we connect H_{cur} to the gate, the gate-source current will fluctuate is switch S is open, otherwise the source-drain current will fluctuate. We can measure this current by connecting L_{cur} to the source

electrode. Connecting H_{pot} to the gate electrode and L_{pot} to the drain electrode, we measure the applied gate voltage.
If the switch S is open, a two points measurement is performed which calculates the capacitance of the transistor. Care must be taken that the gate leakage current does not become not too high to disturb the capacitance measurement. Or in other words the frequency must be high enough to ensure that $\omega C \gg G$.
When the switch is closed, a drain voltage, V_D, is set to the channel. The measured conductance G, is then equal to the transconductance g_m. Care must be taken that the frequency in ωC_G is not too high to disturb the measurement of the channel transconductance. Or in other words the frequency must be low enough to ensure that $g_m \gg \omega C_G$.
If the gate capacitance and transconductance are determined with a frequency sweep, the right frequency satisfying the two conditions, can then be chosen. Sweeping the gate bias voltage, the gate capacitance and transconductance are obtained as a function of the gate voltage, yielding a field-effect mobility according to equation 2.12.
As well as the frequency sweep measurement as the gate voltage sweep measurement have been automatized using LABVIEW (see appendix A.6).

Chapter 4

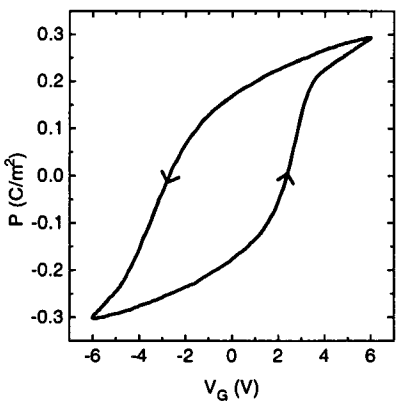
Transistor characteristics

In this chapter we will first present transfer characteristics (i.e., I_D vs. V_G) of the thin film transistor as well as the ceramic transistor, followed by device speed measurements. The possibility of a contact resistance is then discussed and transfer characteristics, obtained using either a two-points or four-points measurements, are compared. Finally the influence of the structuring process on the behaviour of the transistor is discussed.

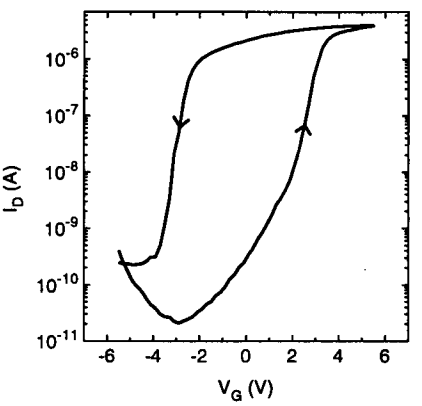
4.1 Transfer characteristics

4.1.1 Thin film transistors

In figure 4.1(a) a hysteresis measurement is depicted measured at a transistor at wafer C_{thin} using a Sawyer-Tower circuit. From the figure the remnant polarization is about 0.2 C/m^2 and the coercive voltage is about 2.5 V, not unlike values found in literature [13][17].



(a) Charge displacement. (C_{ref} = 56 nF, A = 100×300 μm^2, f = 110 Hz)

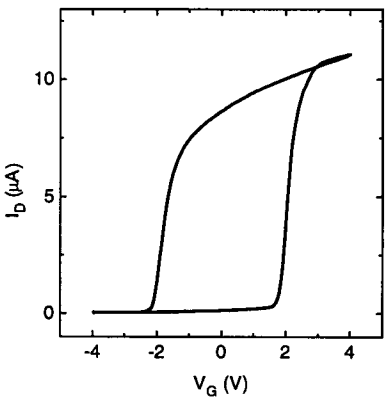


(b) Transfer characteristic. (V_D = 0.1 V, L ×W=5×300μm^2, G=4μm)

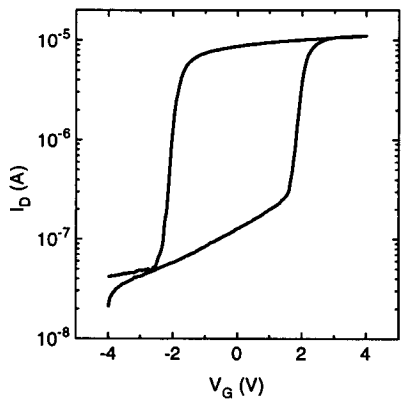
Figure 4.1: Displaced charge and transfer characteristic of wafer C_{thin}, measured at two different transistors.

In figure 4.1(b) the drain current vs. gate voltage is depicted. The hysteresis of the drain current has the same counter-clockwise circulation as the displaced charge. In the following transfer characteristics, the circulation direction is always counter-clockwise, unless noted otherwise. If we define the coercive voltage as the difference in gate voltage at the points with the steepest slopes in the transfer characteristic, the figure shows that this coercive voltage is also the same as the

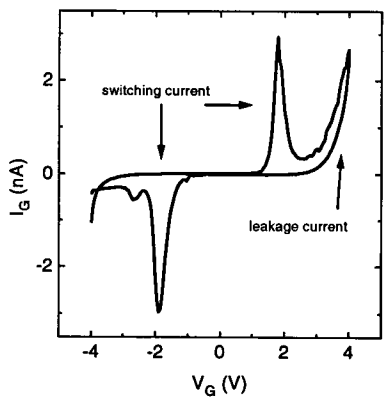
coercive voltage in panel (a). The increase of current in panel (b) below -3 V is due to gate leakage current, which is maximal 1 nA at -5 V.
In figure 4.2 besides the transfer characteristics the gate current is depicted. Panel (a) with a linear current scale is depicted to emphasize the transition between the ON- and OFF-state. Quite suddenly the current decreases as the gate voltage becomes larger than the coercive voltage. Panel (b) shows an ON/OFF-ratio of roughly two orders. It also shows some disturbance at -4 V probably due to initial charging of the device. In Panel (c) the gate current is depicted. At -2 V and at +2 V two peaks in the gate current occur and at +4 V an increase in current occurs. This increase is due to a leakage current through the insulator, but the two peaks are switching currents of the polarization. Charge has to move to get from one remnant state to the other remnant state and equals the remnant polarization plus the maximum displaced charge. The area of the current peak ($\frac{1}{2}$ × 3nA × 1 V) times the sweep speed (2.5 s/V) gives the total charge that is moved (4 ± 1 nC). The total charge per areal unit yields then 0.6 ± 0.2 C/m^2 which roughly equals the amount of charge needed to go from the remnant state to the saturated state (~0.5 C/m^2, see figure 4.1(a)).



(a) Transfer characteristic depicted at a linear vertical scale.



(b) Transfer characteristic depicted at a logarithmic vertical scale.

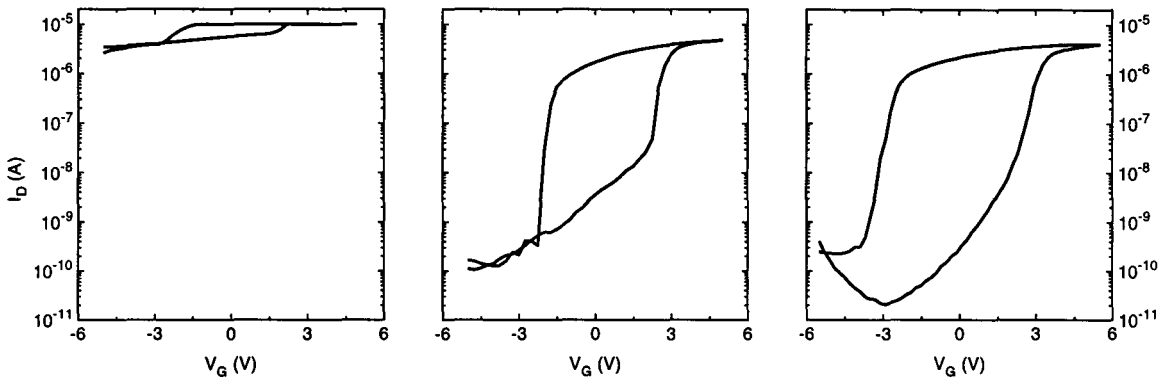


(c) Gate current. Note the difference between switching current and leakage current.

Figure 4.2: Transfer characteristics and gate current for wafer A_{thin}. (V_D = 0.1V, L×W=20×300μm^2, G=16μm)

When varying the transistor parameters like semiconductor layer thickness or doping concentration, we observe different transfer characteristics. In figure 4.3, transfer characteristics are depicted

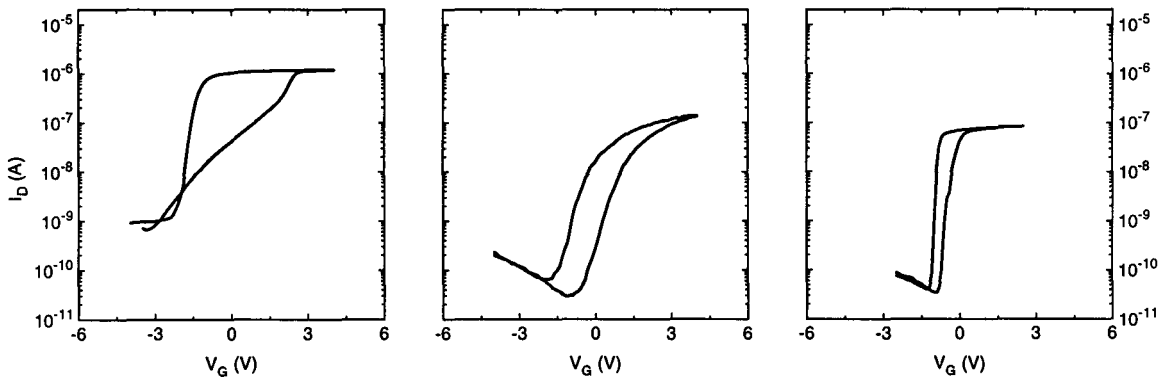
for several transistors. The figures shows that in panel (a) the transistor has got hysteresis but the ON/OFF-ratio is rather small due to the fact that the transistor contains too much charge for full depletion. For panels (b) to (f), the coercive voltage decreases as well as the maximum current. This can be explained as follows. The applied gate-voltage mainly drops over the semiconductor channel as the resistance is increasing. The ferroelectric layer experiences a smaller applied voltage causing a smaller coercive field. In other words, as the amount of charge carriers is decreasing from panel (b) to (f) the depolarization field is increasing, causing a smaller coercive field. As a result, the hysteresis loops become more slim.



(a) E_{thin}(L×W=20×300μm^2, G=16μm).

(b) A_{thin}(L×W=10×300μm^2, G=8μm).

(c) C_{thin}(L×W=5×300μm^2, G=4μm).



(d) D_{thin}(L×W=20×300μm^2, G=16μm).

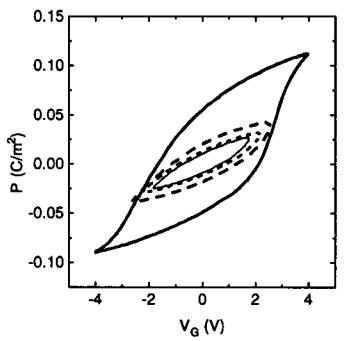
(e) G_{thin}(L×W=12×50μm^2, G=8μm).

(f) F_{thin}(L×W=10×250μm^2, G=6μm).

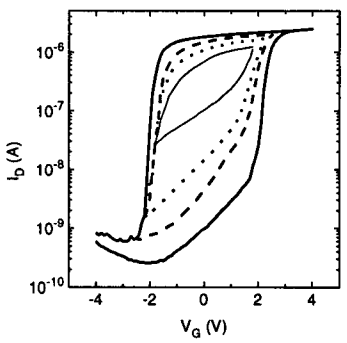
Figure 4.3: Different transfer characteristics for several transistors. Note the figures have the same vertical as well as horizontal scales. (V_D = 0.1 V)

Comparing panels (a) to (c) we can conclude that it is hard to control the operation of the transistors as the semiconductor parameters are nearly the same (for details see table 3.1). The product eN_Dt_{sc} is the same but the figure shows that transistors in panels (b) and (c) are depleted and the transistor in panel (a) not. The difference in processing between the wafers is that the growth temperature of $B_{thin}$is 450 °C and of the two others 500 °C.
Ref. [7] shows that with increasing deposition temperature the charge carrier density is decreasing

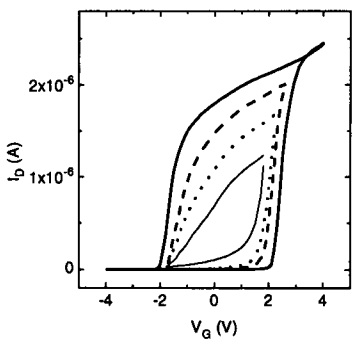
due to chemical interaction of the $PbZr_{0.2}Ti_{0.8}O_3$ layer and the semiconductor layer, creating a dead layer and thus a smaller effective thickness. If we calculate the eN_Dt_{sc} product taking values for N_D from Ref. [7], we get for panel (a) 1.0 ± 0.2 C/m^2 and for panels (b) and (c) 0.32 ± 0.06 C/m^2. This explains the non-full depletion of the transistor in panel (a).
To illustrate the behaviour of the transistor while sweeping the ferroelectric at non-saturized loops or inner loops, several sweeps of displaced charge and transfer characteristic are depicted in figure 4.4, measured wat wafer A_{thin}. For the inner loops it is quite remarkable that with only a small increase in displaced charge, the minimum current of the transistor is getting smaller by two orders of magnitude. Apparently the transition between depleting a part of the channel and the entire channel is small.
This is the effect of the subthreshold slope. With only a little change in charge displacement, the conductance can change for over more than a few orders of magnitude.



(a) Charge displacement measured at a MIS-diode. (f = 90 Hz, C_{ref} = 56 nF, A = 200×200 μm^2)



(b) Transfer characteristic depicted at a logarithmic current scale. (V_D = 0.1 V, L×W=10×300μm^2, G=8μm)



(c) Transfer characteristic depicted at a linear current scale. (V_D = 0.1 V, L×W=10×300μm^2, G=8μm)

Figure 4.4: Charge displacement and transfer characteristics of wafer A_{thin} for several sweep voltages (equal line types correspond with the same sweep voltage amplitude).

4.1.2 Transistors with a bulk ceramic $PbZr_{0.5}Ti_{0.5}O_3$ insulator

In figure 4.5 typical polarization curves for the ceramic bulk $PbZr_{0.5}Ti_{0.5}O_3$ transistors are depicted, measured on wafer B_{BULK}. The outer curve is the saturated loop while the inners loops are measured with a smaller applied voltage sweep. The figure shows that the remnant polarization is 0.33 C/m^2. This value is similar to measured values on the other wafers.

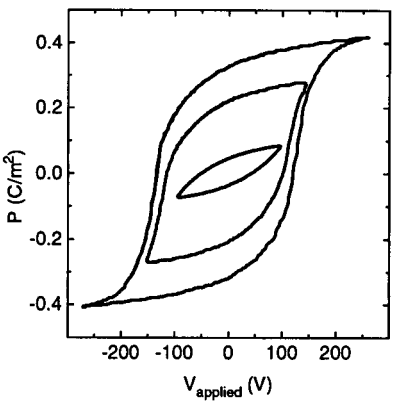
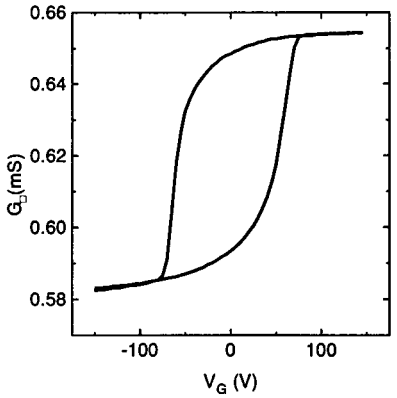


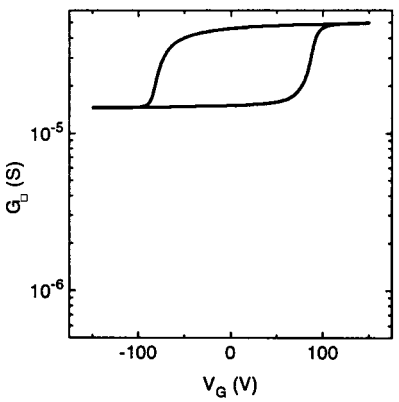
Figure 4.5: Polarization vs. applied field for a saturated loop and two inner loops. (C_{ref} = 56 nF, A = 0.15 mm^2, f = 110 Hz)

In figure 4.6 transfer characteristics of the three fabricated wafers with a bulk ferroelectric insulator are depicted. In order to compare the three graphs we converted the drain current into sheetconductance, $G_\square$, to eliminate geometric differences, using $G_\square = I_D/V_D \times L/W$. Note that figure 4.6(a) has a linear current scale, while the current scales of the other two graphs are logarithmic. Panel (a) has a very small ON/OFF-ratio (~1.1) and for panels (b) and (c) this ratio increases (3.3 to 19). The conductance of the ON-state is roughly the same in panels (b) and (c) if we consider the thickness differences [(b) 15nm and (c) 10 nm].

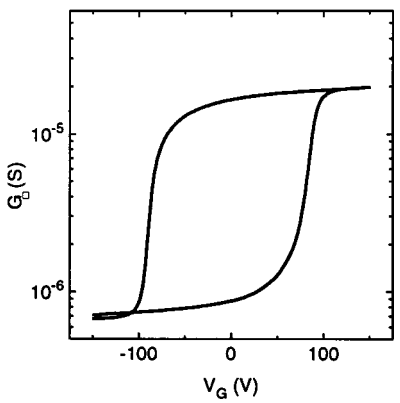
If we calculate the charge per unit area in the semiconductor layer using $\tilde{Q} = eN_D t_{SC}$, we obtain for the three wafers: 51 ± 5, 0.48 ± 0.05 and 0.32 ± 0.03 C/m^2. The polarization modulates the charge in the semiconductor channel with an amount of 0.4 C/m^2 (see the inner loop in figure 4.5), so we can see that is impossible to deplete wafer A_{BULK} as it contains too much charge. We also see that as the charge in the semiconductor layer decreases, the channel-depletion increases (panels (b) and (c)). In the figure the coercive voltage is about between 55 and 70 V, while in the displaced charge curve (figure 4.5) the coercive voltage amounts 120 V. We attribute this difference to the relaxation of the ferroelectric. The transfer characteristic is measured a low frequency (~0.03 Hz), while the sweep frequency of the displaced charge measurement is 110 Hz. The relative differences in coercive voltages between panels (a), (b) and (c) could be explained by the differences in conductance. The wafer in panel (c) has a lower conductance than the wafer in panel(a). When a gate voltage is applied, there could be a electrostatic potential drop present across the channel. This drop would result in a less effective potential across the insulator and thus the coercive field would increase.



(a) A_{BULK} ($L \times W$=6×250μm^2)



(b)
B_{BULK} ($L \times W$=10×250μm^2)



(c) C_{BULK} ($L \times W$=10×25μm^2)

Figure 4.6: Transfer characteristics for three transistors with a bulk ferroelectric insulator. Note the different scales on the vertical axes.

4.1.3 Thin film field-effect transistor with a SiO_2 insulator

In figure 4.7 the transfer characteristic is given for wafer A_{Si}. Note the large applied gate voltage of 100 V. The figure shows that there is a field-effect which is linear as we are used to hysteresis behaviour, but with small a ratio of about 2 between the maximum and minimum drain current. The leakage current (not shown) is smaller than 0.1 nA at 100 V. If we calculate the displaced charge at the insulator/semiconductor interface, we obtain (using $\tilde{Q} = CV = \epsilon_0 \epsilon_r V/d$) $\tilde{Q}$= 6 mC/m^2 (ϵ_r= 2.6, V = 100 V, and d = 400 nm). The amount of charge carriers in the semiconductor layer, $eN_D t_{sc}$, yields 1.3 C/m^2. Thus it is quite obvious that the insulator and the semiconductor layer are too thick for full depletion of the channel.
From the slope of the transfer characteristic and the above calculated displaced charge, we can calculate the field-effect mobility using equation 2.7, which yields 20 cm^2/Vs.

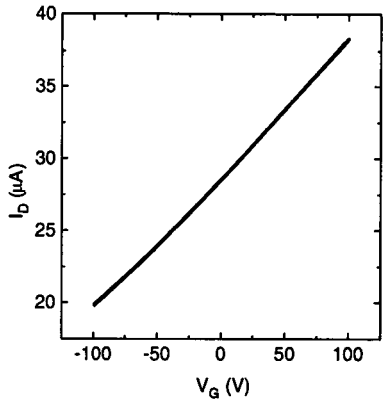


Figure 4.7: Transfer characteristic of A_{Si}. (V_D = 0.1 V, $L \times W$=25×200μm^2)

4.2 Transistor with a spun SnO_2 semiconductor and a bulk ferroelectric insulator

In figure 4.8 the transfer characteristic of wafer A_{spun} is depicted. The figure shows proper hysteresis behaviour with an ON/OFF-ratio of 500, but there is a difference of five orders in the minimum and maximum conductance. Note that the minimum current is not limited by the influence of a gate leakage current, in contrast to the transfer characteristics of the thin film ferroelectric transistors. The charge displacement is not depicted as the semiconductor layer at the wafer is not structured, causing a too large electrode area for the hysteresis measurement.

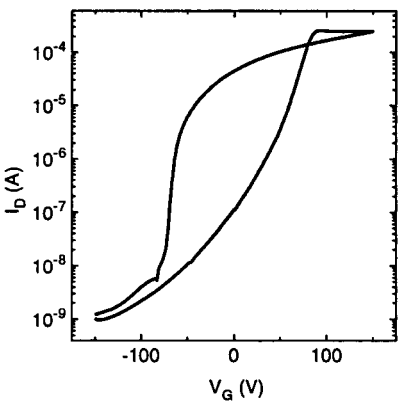
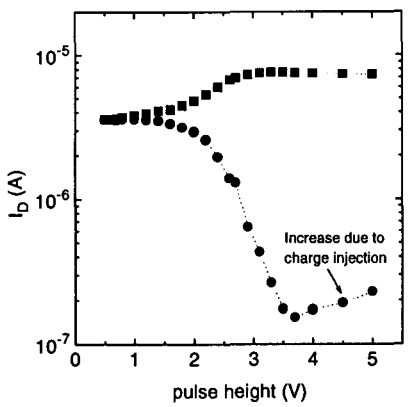


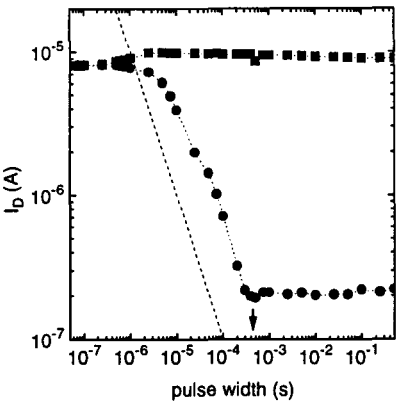
Figure 4.8: Transfer characteristic of wafer A_{spun} (V_D = 10 V, $L \times W$=10×300μm^2).

4.3 Device speed

The device switch speed can be determined with a pulse measurement. That is, a voltage pulse is applied to the gate electrode and after a delay time of five seconds, the drain current is measured. This action is repeated for a variable pulse height while the pulse width is kept constant or for a variable pulse width while the pulse height is kept constant. So the channel conductance is successively switched to the ON-state or to the OFF-state. In figure 4.9(a) the measurement is performed varying the pulse width with a constant pulse height (5V). In figure 4.9(b) the pulse height is varied at a constant pulse width (1 ms).
In figure 4.9(a) both ON-state and OFF-state current are depicted as a function of the pulse height. At high applied voltages the ON-state current is constant, and decreases when the pulse height is



(a) Variation of pulse height at a constant pulse width (1ms).



(b) Variation of pulse width at a constant pulse height (5V). The arrow indicates the theoretical value for the switching time. The dashed line represents the function: $I_D \sim \tau^{-1}$.

Figure 4.9: Pulse measurement at wafer A_{thin}. ($L \times W$=20×300 μm^2, G=16μm).

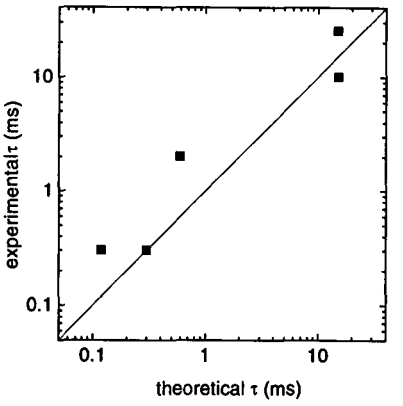
getting below 3 V. For the OFF-state current the figure shows a decrease in current from a pulse height from 5 V to 3.5 V and then an increase when the pulse height is getting smaller.
In figure 4.9(b) the ON-state and OFF-state current are depicted as a function of the pulse width. The OFF-state current is constant above large pulse widths but the current increases when it gets below 0.3 ms. The ON-state current remains nearly constant except for a small decrease when the pulse-width gets below 1 μs.

The switching of the transistor with variable pulse height can be divided in three parts. At pulse heights below 1 V the ferroelectric layer is not switched by the applied voltage pulses. Between 1 V and 3.5 V the ferroelectric layer switches in non-saturized states and becomes saturized at 3.5 V. At larger applied voltages charge injection (see theory section 2.7) occurs, which causes the OFF-state current to increase. Charge injection is not observed in the ON-state current.
Panel (b) shows that there is a minimum switching time of roughly 0.3 ms. Using equation 2.16, a theoretical value is given for the switching time and yields 0.3 ms. This value is illustrated with the arrow in panel (b). In table 4.10(a) the experimentally obtained minimum switching times vs. theoretical values are given and depicted in figure 4.10(b). The figure shows that the experimental data corresponds with the theoretical values. The drawn line is the line when theory and experiment coincide.
In panel (b), below the minimum switching time of 0.3 ms the OFF-state current increase. The slope of this part of curve is roughly parallel to the plotted dashed line, which represents the function: $I_D \sim \tau^{-1}$ as predicted in the theory section 2.9.
The ON-state currents in both figures are flat. We attribute this to the presence of series-resistances limiting the channel conductance. Placing resistors in series with the channel, we observed a decrease in the ON-state-current equal to the conductance of the resistor (not shown). The ON-state current behaviour still remains flat. In the case that the channel resistance is larger than any series resistance we will observe even in the ON-state current charge injection as will be shown in chapter 5 (Endurance experiments).

For the ceramic transistor, the device switching speed measurement shows that the transistor could switch down to switching times of 1 ms. Due to the band-width of the voltage amplifier we could

Wafer	τ_{theor} ms	τ_{exper} ms
C_{thin}	15	25
A_{thin}	0.3	0.3
D_{thin}	15	10
E_{thin}	0.12	0.3
B_{thin}	0.6	2

(a)



(b)

Figure 4.10: Table and figure of theoretical and experimental minimum switching times obtained at different wafers.

not measure below 1 ms. Theoretically this minimum pulse width time would be in order of 1 μs in case of transistor C_{BULK}.

4.4 Contact resistance

The total resistance of the channel, R_{TOT}, depends on the geometry of channel (i.e., length and width) and depends on a possible contact resistance, $R_{contact}$:

$$R_{TOT} = \frac{L}{W} R_{\square} + R_{contact} \tag{4.1}$$

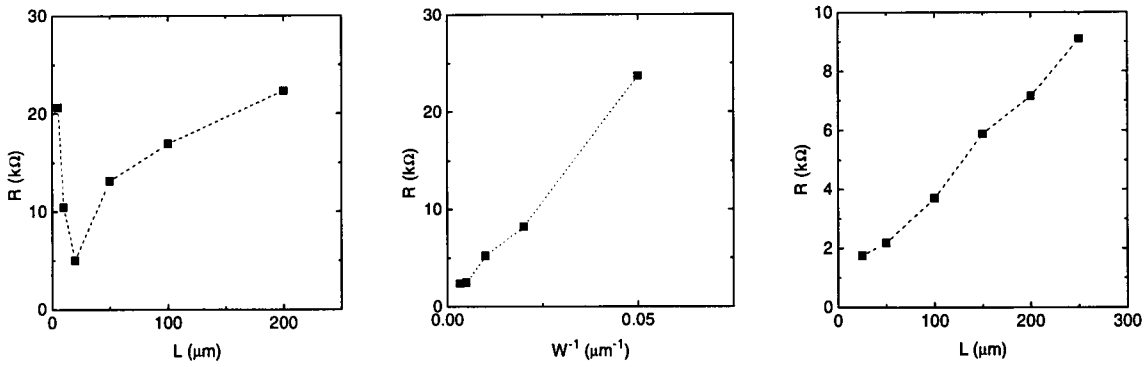
We can determine $R_{contact}$ by measuring the channel resistance for several source-drain lengths and widths at a single wafer. In figure 4.11(a) the resistance vs. source-drain length is depicted. The resistance is obtained in the absence of a gate voltage after a positive gate voltage is applied of +4 V. A contact resistance for wafer A_{thin} is determined to 10 kΩ by extrapolating the trend taking L to 0. For other wafers the contact resistance is in the range of 10$\sim$50 kΩ. The resistance for several channel widths is depicted in figure 4.11(b). Extrapolating the trend taking W to infinity, the figure shows that there is no axis offset. This has also been observed for other wafers.

From these two measurements we can conclude that there is a contact resistance in the order of 10 kΩ, and that the contact resistance is a phenomenon that is uniformly spread over the entire contact pad.

The $BaZrO_3$ layer between the contact pad and the semiconductor channel is probably obstructing the conductance. Therefore in wafer B_{BULK} the $BaZrO_3$ layer is removed by etching for 1 minute in HCl, after which the molybdenum contact pads are sputtered.

In figure 4.11(c) the resistance of this wafer is plotted with channel length variation. The figure shows that the curve has a smaller axis offset of about 1 kΩ. At wafer C_{BULK} the $BaZrO_3$ layer was etched for 3 minutes in HCl, resulting in a contact resistance of 2 kΩ. At several intervals in the etching process the conductance is measured by placing two probes at one contact pad. The resistance measured by placing two probes at the semiconductor layer, increased during the etching process from 40 kΩ to 2 MΩ.

Etching with HCl can be convenient to reduce the contact resistance, however care should be taken that the etching fluid does not affect the semiconductor layer.



(a) Channel length variation for A_{thin}(W=300 μm).

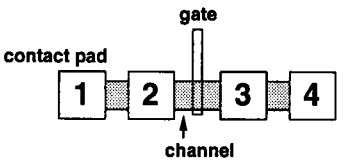
(b) Channel width variation for A_{thin}(L=100 μm).

(c) Channel length variation for B_{BULK}(W=250 μm).

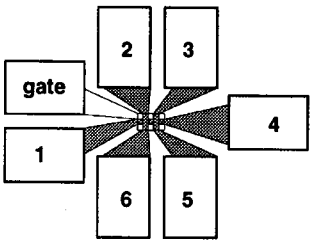
Figure 4.11: Resistance as a function of either source-drain length or width.

4.5 Two-points and four-points measurements

The transfer characteristic can be measured with either a two-points or a four-points measurement. The advantage of a four-points measurement is that a possible contact resistance or supply-wire resistances are elimated. We will compare three four-points measurements, which will be first described whereafter a comparison with the two-points measurement will follow.
In figure 4.12(a) a top view of the transistor channel is given, which are present on the mask set FET1 (see appendix B). There are four contact pads on top of the channel, between contact pads two and three the gate is positioned. In a two-points measurement a voltage is set over contact pads two and three, while the current through contact pads two and three is measured. In a four-points measurement a current is driven through contact pads one and four, while the voltage is measured over contact pads two and three. Instead of measuring the voltage over contact pads two and three, the probes can alo directly be placed on top of the channel. In an ideal voltage-measurement device no current is flowing through the probes so no voltage drop will occur at the $BaZrO_3$ capping-layer.
The third four-points measurement is to use a gated Hall-bar, i.e., a Hall-bar structure with underlying gate which are present on mask set FET2 (see appendix B). A top view of a gate Hall-bar is depicted in figure 4.12(b).
In figure 4.13(a) the two-points and four-points measurement are depicted measured at a transistor with the layout as shown in figure 4.12(a) at wafer A_{thin}. The conductance is obtained in the two-points measurement by applying a drain voltage of 0.1 V and measuring the current, and in the four-point measurement by setting a channel current of 10 nA and measuring the voltage. The curves show good resemblance. At first sight this would mean that there is no contact resistance present. At second sight, taking a closer look at the layout of the device (Fig. 4.12(a)), we see that when measuring the voltage drop across the channel, the voltage is not measured at one point but over an area. So an average voltage is measured which results in an extra resistance. If we assume that this extra resistance is of the same order as the contact resistance, it is logical that the two curves coincide.
If the two inner contact pads were thin, the problem would not have arisen. We can bypass this problem by placing the two voltage probes directly on the $BaZrO_3$ capping-layer on the channel between contact pads two and three. In figure 4.13(b) the channel conductance is given. Note that there is still a gap in the curve at V_G = -2 V for the same reason as mentioned above. The conductance in the ON-state is about 0.1 mS. When we compare this conductance with the conductance in the two-points measurement, we should take in mind that the two probes are closer positioned causing a higher conductance.

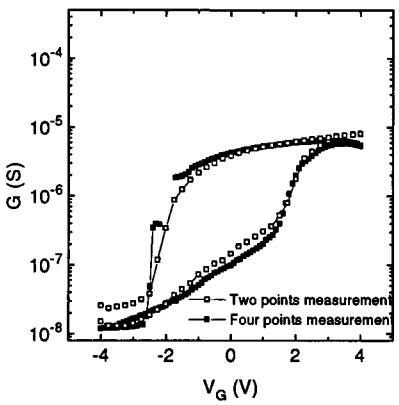


(a) Top view of the transistor; contact pads and underlying gate are also plotted.

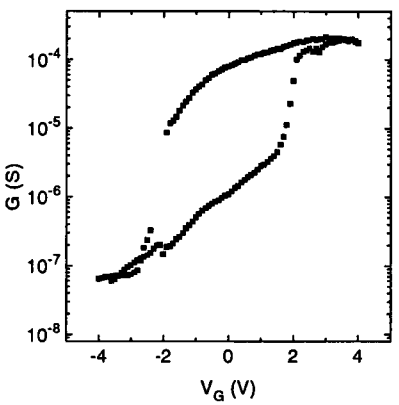


(b) Top view of a gated Hall-bar: contact pads and underlying gate are also plotted.

Figure 4.12: Two different layouts of a transistor to perform a four-points measurement.



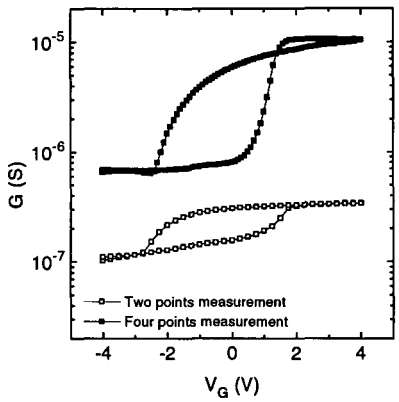
(a) Two- and four-points measurement.



(b) Four-points measurement with probes positioned on the top of the channel.

Figure 4.13: Two- and four-points measurement at wafer A_{thin}. In the four-points measurement at V_G = -2 V there is a gap noticeable. In this region the switching current of the ferroelectric layer is disturbing the voltage measurement, causing the driven current to flow from drain to gate and not to source, which results in noise. ($L \times W$=100×300 μm^2, G=100 μm).

To estimate the contact resistance, we have to take in account for this geometric increase in conductance. The geometric factor is obtained by comparing the OFF-state conductances in both figures, as the contact resistance is then negligible. The geometric factor yields roughly 6. Multiplying this factor with ON-state conductance in figure 4.13(a), we can compare the two conductances in both figures and the difference will give the contact resistance ($\sim$ 20 kΩ). This contact resistance is in good agreement with the contact resistance determined in the previous section.



(a)

Figure 4.14: Two- and four-points measurement at a gated Hall-bar. (wafer B_{thin})

Using a gated Hall-bar structure, the transfer characteristic of a transistor at wafer B_{thin} has been derived. In figure 4.14 the two- and four-points measurement are depicted using gated Hall-bar 3 (see figure 4.12(b) for a top view of the gated Hall-bar). In the two-points measurement a drain voltage of 0.1 V is applied at contact pads two and three while the current is measured. In the four-points measurement a current of 100 nA is driven through contact pads one and four while the voltage drop is measured over contact pads two and three.
The figure shows that in the two-points measurement the ON-state resistance is about 0.3 μS and in the four-points measurement about 10 μS. The contact resistance is not the difference between the reciprocal of these two numbers, as in the two-points measurement there are series resistances due to the presence of the contactpaths and the current-path in the two-points measurement is larger by a factor of roughly three. The contact resistance will then be about 1 MΩ which is quite large in comparison with the contact resistance obtained from the channel length variation. The ON/OFF-ratio is in the two-points measurement is about 2 and about 10 in the four-points measurement. So it seems like there is a contact resistance present.

4.6 Increase in channel conductance due to structuring

Directly after the deposition of the semiconductor layer with its capping layer, the conductance of the semiconductor layer is measured by placing two probes with indium contacts on top of the semiconductor layer near the edge of the wafer. In all fabricated wafers this conductance is lower than the conductance after structuring (i.e., the entire process between depositing the semiconductor layer and defining the semiconductor channel). For the wafers with an SnO_2:Sb semiconductor film the conductance per square (denoted by ΔG) increases by an amount in the order of 10^{-5} S while for the In_2O_3:Sn semiconductor wafers the increase is in the order of 10^{-4} S.
In order to investigate this phenomenon, several wafers are made with various semiconductor layer thicknesses. After deposition of an In_2O_3:Sn semiconductor layer (N_D = 2 10^{18} cm^{-3}) a molyb-

denum film is sputter-deposited and removed with an aqueous solution of $K_4Fe(CN)_6/H_2O_2$. In table 4.1 the measured conductivity as well as the increase of conductance before and after the molybdenum removal is summed up for the various thicknesses.

Wafer	t_{SC} (nm)	t_{BZO} (nm)	σ_{before} $(\Omega m)^{-1}$	σ_{after} $(\Omega m)^{-1}$	ΔG $(10^{-4}S)$
JC5529	150	10	$7.0\ 10^2$	$3.7\ 10^3$	4.5
JC5530	15	10	$6.0\ 10^2$	$2.0\ 10^4$	2.9
JC5533	15	25	$1.3\ 10^2$	$7.5\ 10^3$	1.1
JC5534	5	25	$8.0\ 10^1$	$4.2\ 10^3$	0.2

Table 4.1: Wafer number, semiconductor layer thickness (t_{SC}), thickness of $BaZrO_3$ capping layer (t_{BZO}, conductivity before and after molybdenum removal (σ_{before} and σ_{after}) and the increase in conductance (ΔG).

The table shows that the increase in conductivity is roughly the same for a 15 nm or 150 nm semiconductor layer. Only for a 5 nm layer the increase is one order of magnitude smaller. These values show that the semiconductor layer is affected by the removal process and an affected layer which is created, is larger than 5 nm.
To calculate the affected layer thickness, we assume that the semiconductor layer of the 5 nm sample is totally affected and that the wafers with the 15 nm or 150 nm semiconductor layers are partially affected over a thickness δ (see figure 4.15). The partially affected semiconductor layer consists now of two parallel resistances, one with high conductivity (the affected part) and one with a low conductivity (the non-affected part). We take for the conductivity of the affected part the conductivity of the 5 nm wafer after molybdenum removal and we take for the conductivity of the non-affected part the conductivity of the wafer before the molybdenum removal. The total conductance of the semiconductor layer after structuring (thickness times conductivity) yields then:

$$t_{SC}\ \sigma_{after} = (d - \delta)\ \sigma_{before} + \delta\ \sigma_{5nm,after}, \tag{4.2}$$

where t_{SC} is the thickness of the semiconductor layer.
This equation results in an affected layer of 13 nm for the 15 nm wafers and 17 nm for the 150 nm wafer.

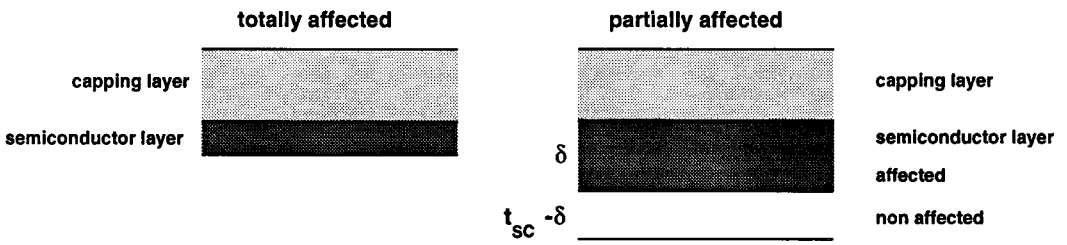


Figure 4.15: Schematic representation of a totally affected semiconductor layer and a partially affected semiconductor layer over a thickness δ. The semiconductor layer remains non-affected over a thickness of $t_{SC} - \delta$.

We verified that $K_4Fe(CN)_6/H_2O_2$ (the fluid to etch molybdenum) is not the cause of the increase increase. A wafer with an SnO_2:Sb semiconductor layer with a 10 nm $BaZrO_3$ layer on top has been put in the etch fluid for several minutes (~15 minutes). The resistance remains the same during the experiment. Dry etching (with a Barrel etcher) in stead of wet etching still gives an increase of conductance.
We might conclude that the semiconductor layer is affected by the molybdenum sputter process. It is possible that the semiconductor layer is modified but it is hard to confirm this as comparing the semiconductor structure before and after molybdenum removal is difficult. SIMS spectroscopy shows that there is indeed a large molybdenum concentration in the $BaZrO_3$ layer. Due to this large concentration, it is not possible to measure whether there is molybdenum inside the semiconductor

layer. With this measurement, it was not possible to obtain absolute values of molybdenum concentrations, only relative values compared to a reference sample could be given.
For future studies, it is worthwhile investigating molybdenum evaporation instead of sputtering, as the energy of molybdenum ions in an evaporation process is much lower. Another possibility to eliminate the molybdenum influence, is to use other materials for masking like, for example, lacquer.

Chapter 5

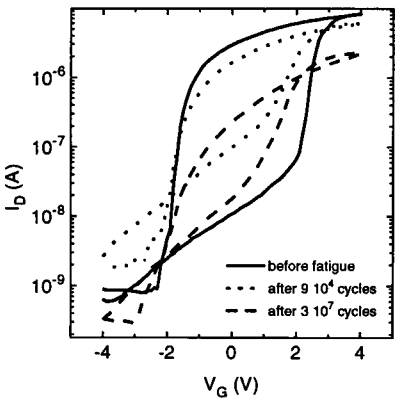
Endurance experiments

Knowledge about the life-time of a device is important, especially when the device is implemented in an application. In this chapter we will investigate the endurance or the fatigue behaviour of the devices. The concept of endurance is the insensitivity of the device to repeated switching, while the concept of fatigue is that irreversible changes in the device originate from repeated switching. So after the device has become sensitive to repeated switching, the fatigue of the device has started. We will compare the endurance of ferroelectric devices with a bulk or a thin film ferroelectric insulator, and the endurance of devices containing a dielectric insulator. In the fatigue experiment we will apply a square wave voltage at the gate electrode at the highest frequency as possible, in order to reduce the total measurement time. At several intervals, transfer characteristics are determined and the ON-state and OFF-state currents are obtained by switching the channel in either state using a voltage pulse.

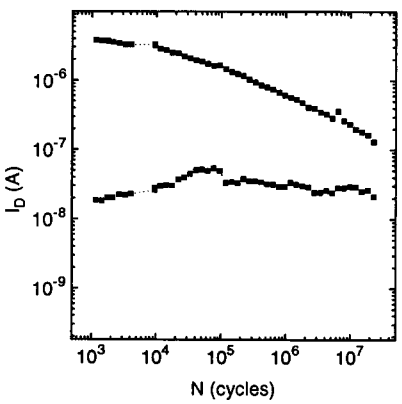
5.1 Thin film transistors with a ferroelectric insulator

In figure 5.1 results of an endurance experiment performed at a transistor of wafer A_{thin}, are depicted. At a frequency of 100 Hz a square wave is applied to the gate with amplitude of 4 V. During the endurance experiment several transistor characteristics are measured, like transfer characteristics, ON- and OFF-state currents and pulse measurements. The ON- and OFF-state currents are determined by applying a voltage pulse of 4 V and a pulse width of 5 ms.
Transfer characteristics measured before, during and after the fatigue are depicted in figure 5.1(a). Before the start of the endurance measurement, the transfer characteristic is quite rectangular but as the number of passed cycles increases (from 10^4 up to 10^7 cycles), the curve is getting more slim. The coercive voltage decreases as well as the maximum current. The gate current at +4 V (not shown) increases from 0.5 nA at the start of the experiment, up to 9 nA after 10^7 cycles.
The ON- and OFF-state currents at several intervals are depicted in figure 5.1(b). The figure shows that the ON-state current immediately decreases as the OFF-state current increases up to 10^5 cycles whereafter it tends to decrease. The ON/OFF-ratio depicted in figure 5.1(c) shows a decrease almost linear with the logarithm of passed cycles.

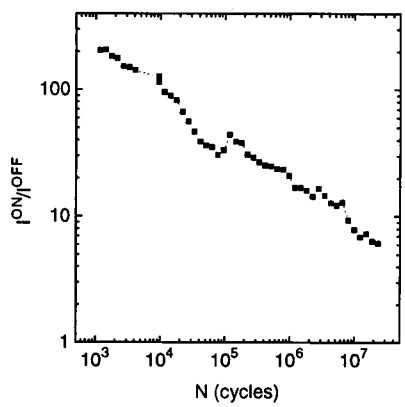
Pulse measurements measured before the fatigue and after 10^7 cycles are depicted in figure 5.2. Panel (a) shows clearly a difference between the measurement before the fatigue and at the end of the fatigue (10^7 cycles). Before the fatigue, the voltage necessary to switch the channel conductance to a minimum or maximum value, is about 2.7 V and after the fatigue about 3.5 V. Before the endurance experiment the ON-state current shows no charge-injection, whereas for the OFF-state current charge injection occurs. After the fatigue the pulse measurement is different. The ON-state current is decreased and there is even charge injection noticeable. The OFF-state currents in both cases coincide at voltages smaller than 1.5 V or larger than 3.5 V.
Panel (b) shows the pulse measurement with a variable pulse width (pulse height = 5 V). Again the ON-state current is smaller than the current before the start of the endurance measurement.



(a) Transfer characteristic at three different numbers of passed cycles.

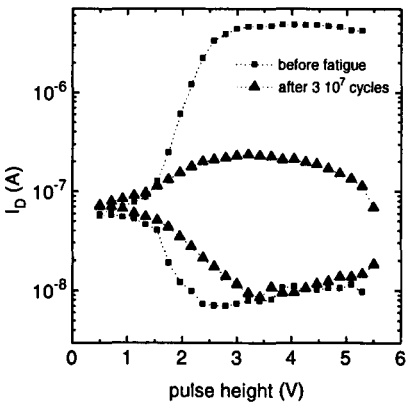


(b) ON- and OFF-current evolution.

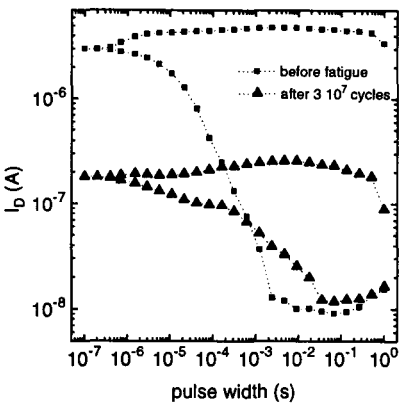


(c) ON/OFF ratio.

Figure 5.1: Endurance measurement at wafer A_{thin} (f= 100 Hz, pulse height 4 V, V_D = 0.1 V, $L \times W$=10×300μm^2).



(a) Variation of pulse height at a constant pulse width (999 ms).



(b) Variation of pulse width at a constant pulse height (5 V)

Figure 5.2: Pulse measurement measured during the same endurance experiment as in figure 5.1.

The minimum pulse width increases from 2 ms to 40 ms.

The transfer characteristics show that the coercive voltage decreases. This could indicate that there is a dielectric layer created at the semiconductor/insulator interface. Pulse measurements show that the voltage necessary to switch the device properly, is increased due to repeated switching. When a voltage pulse is applied, there is a voltage drop across this possible dielectric layer causing the effective voltage drop across the ferroelectric layer to be smaller. The switching time of the transistor is also increased during the endurance measurement. We can attribute this increase to the creation of a possible dielectric layer. Panel (a) and (b) show that the minimum current or the maximum resistance remains roughly the same. As the switching time is related to an RC time, it means that a capacitor C and thus a dielectric layer, has been created during the endurance measurement.
These three statements give enough evidence to sustain the idea that the semiconductor channel is affected, resulting in a dielectric layer.

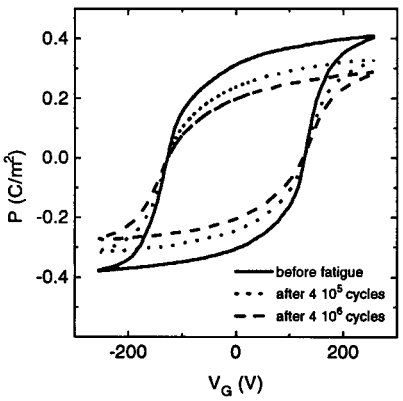
5.2 Transistors with a bulk ferroelectric insulator

5.2.1 Charge displacement

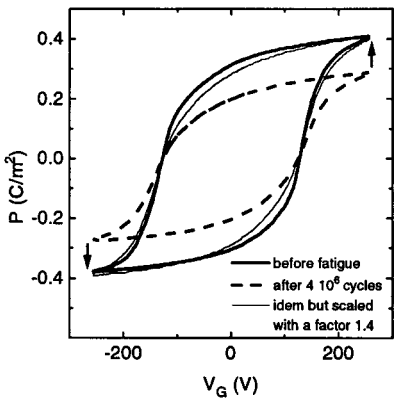
Results from endurance experiments with a bulk ferroelectric capacitor are depicted in figure 5.3. Figure 5.3(a) shows three displaced charge measurements, measured before the start of the endurance measurement, after 4 10^5 and 4 10^6 cycles. The remnant polarization decreases with a factor of 1.4 after 4 10^6 cycles. Note that the coercive voltage remains the same.
Two remarks should be made while observing the wafer during the experiment. The piezoelectric effect of the ferroelectric insulator was visible through a microscope, because the reflection of the light shining at the surface of the wafer was oscillating at the spot of the transistor. Secondly, the exterior of the molybdenum contact pads changed. Through a light microscope, it was noticeable that the sticking of the molybdenum was not good and that the surface had become flaked off. The semiconductor did not conduct below the contact pads at the places where the molybdenum had come off ($R > \mathrm{G}\Omega$).
Using a smaller sweep amplitude (150 V, $f = 1$ kHz) we observed a decrease of 10 % in displaced charge after 2 10^6 cycles, the displaced charge then remained constant up to 7 10^6 cycles (not shown).

In figure 5.3(b) we scaled the curve of the charge displacement after the fatigue with a factor of 1.4. This up scaled curve roughly coincides with the curve measured before the fatigue. This proves that the reduction in charge displacement after the fatigue is due to a surface reduction. In case of the creation of a dielectric layer at the semiconductor/ferroelectric interface, we would expect a lower remnant polarization, but the coercive field would decrease as the ferroelectric is sweeping at inner loops. However we cannot exclude the possibility of the creation of a dielectric layer. As the ferroelectric insulator has a large impedance due to the large thickness, compared to the semiconductor thickness (180 μm vs. 10 nm), the possible dielectric layer can not influence the charge displacement.

Thus, although it seems that the ferroelectric capacitor shows fatigue, we can conclude that it is a contact electrode effect. The piezoelectric effect of the insulator causes the molybdenum to flake off, yielding a smaller contact area. At smaller applied voltages this is effect is smaller. For the thin film ferroelectric layer no fatigue was observed after 10^6 switching cycles.



(a) Displaced charge measured at several intervals during the fatigue measurement (see inset).

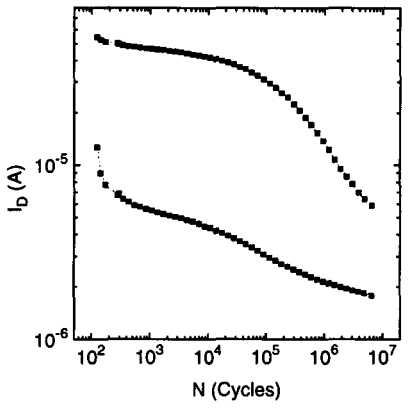


(b) Displaced charge measured before and after the fatigue. The thin line represents the measurement after the fatigue but scaled with a factor of 1.43.

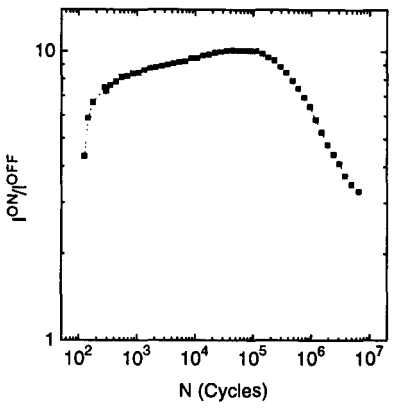
Figure 5.3: Displaced charge at transistor B_{BULK} (f = 1 kHz, C_{ref} = 56 nF, A = 0.18 mm^2).

5.2.2 Transfer characteristic

In figure 5.4(a) ON- and OFF-state currents are depicted, measured during an endurance experiment. The figure shows that the ON-state current to be rather constant up to 10^4 cycles whereafter it decreases. The OFF-state current decreases almost quite linearly with the logarithm of time. At other samples the ON- and OFF-state current often collapse to a highly resistive state ($R > G\Omega$), after $10^6 \sim 10^7$ cycles (not shown). Figure 5.4(b) shows first an increase in ON/OFF-ratio and after 10^5 cycles the ratio drops from 10 to 3. We showed in the previous section (5.2.1), that the ferroelectric does not show any fatigue behaviour. Therefore the decrease in ON- and OFF-state currents must be due to fatigue of the semiconductor channel. This can occur in two possible ways, namely by the creation of cracks in the semiconductor caused by the piezoelectric effect of the insulator or by the creation of a dielectric layer at the semiconductor/ferroelectric interface at the cost of the semiconductor layer. Due to the displaced charge, each cycle a switching current will flow, causing the semiconductor to degrade locally.



(a) ON- and OFF-state versus the number of switched cycles.



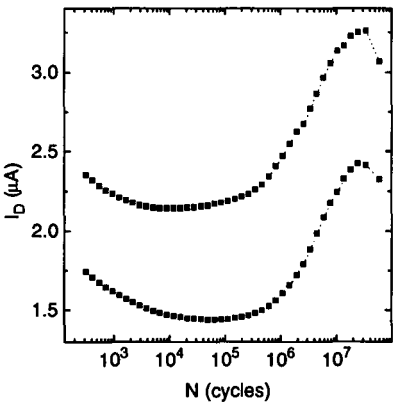
(b) ON/OFF-ratio versus the number of switched cycles.

Figure 5.4: Endurance measurement at transistor C_{BULK} (f= 100 Hz, pulse height 120 V, V_D = 0.1 V, $L\times W$=25×200 μm^2).

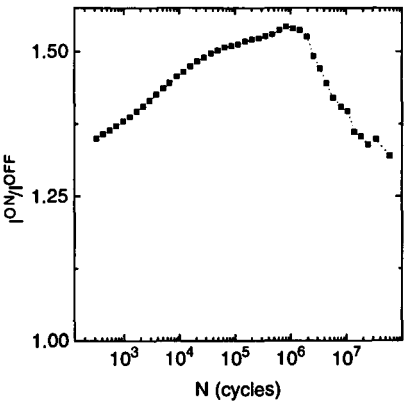
5.3 Wafers with a dielectric insulator

5.3.1 Thin film field-effect transistor with a $BaZrO_3$ insulator

As an interesting comparison, we investigated the influence of the ferroelectric insulator on fatigue behaviour, we used sample A_{BZO}, as it has a dielectric insulator. At a frequency of 100 Hz, a square wave with amplitude of 3 V is applied to the gate electrode. In figure 5.5(a) the ON- and OFF-state currents are depicted as a function of the number of switching cycles. The figure shows that both curves progress the same way. The currents first decrease and start to increase after 4 10^5 pulses. The difference in currents of the two states (i.e., $I^{ON} - I^{OFF}$) is roughly the same during the fatigue test. In other words, the modulation of the channel conductance (i.e., the field-effect) is the same. In figure 5.5(b) the ON/OFF-ratio is depicted. The figure shows that the ratio starts at a factor of 1.3 to 1.5 and then decreases. This can be attributed to the increase in the ON-state and OFF-state currents.



(a) ON- and OFF-state versus the number of switched cycles.



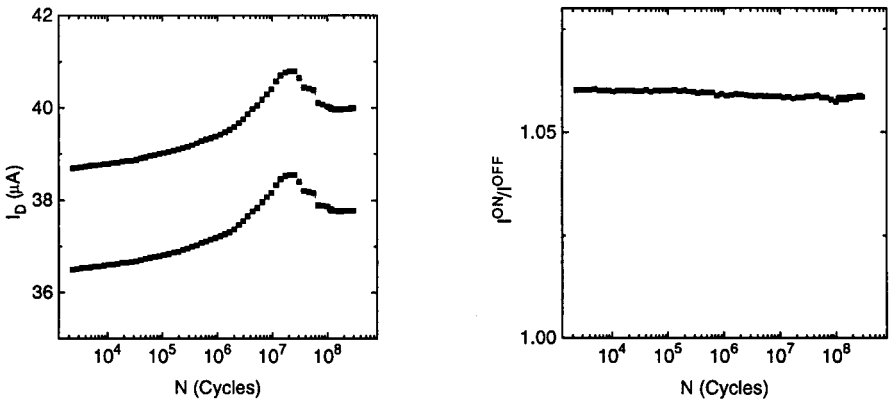
(b) ON/OFF-ratio versus the number of switched cycles.

Figure 5.5: Endurance of sample A_{BZO} (f = 100 Hz, pulse height = 3 V, V_D =0.1 V, $L\times W$=100×300μm^2).

The increase in currents can be attributed to external influences, as there is no $BaZrO_3$ capping layer present on the semiconductor layer and the measurement time is roughly one day. The main conclusion to be drawn from this experiment, is that the transistor does not show any fatigue up to 10^7 cycles.

5.3.2 Thin film field-effect transistor with a SiO_2 insulator

With sample A_{Si} a fatigue experiment is performed using a square wave with amplitude of 9 V and a frequency of 1 kHz or 100 kHz. After 6 10^7 the frequency was raised to 100 kHz. We experimentally verified that the transistor can operate at frequencies of 100 kHz. Figure 5.6(a) shows an increase in current of about 5%. Another experiment shows a decrease in current of the same order (not shown). From the figure it follows that the difference in current of the two states is rather constant (~2 μA). The ON/OFF-ratio is also constant during the fatigue.
We attribute the changes in current to external influences as the experiment lasts for a long period of time (~1 day). We can conclude from this experiment, that the device does not show any fatigue.



(a) ON- and OFF-state versus the number of switching cycles.

(b) ON/OFF-ratio versus the number of switching cycles.

Figure 5.6: Endurance measurement of a thin film silicon field-effect transistor (f= 1 kHz (< 6 10^7 cycles), f = 100 kHz (> 6 10^7 cycles), pulse height = 9 V, V_D = 0.1 V, $L \times W$=25×300μm^2).

5.4 Summary and discussion

The experiments with the ferroelectric transistors have shown fatigue behaviour which becomes crucial after 10^7 cycles. At that point, the ON-state current have become equal to the OFF-state current within one order of magnitude for the thin-film field-effect transistors. For the field-effect transistor with a bulk ferroelectric insulator, the ON-state current after 10^7 cycles becomes equal to OFF-state before the start of the fatigue measurement. The endurance of the thin-film transistor is better, because during the switching cycles the OFF-state current is rather constant causing a clear difference between the ON- and OFF-state current, in contrast to the bulk ferroelectric transistor where the ON-state current becomes equal the OFF-state current.
We have excluded the possibility of ferroelectric fatigue. Other research shows that ferroelectric fatigue shows up after 10^9~10^{10} cycles [18][19]. The semiconductor layer can be affected due to three reasons. The piezoelectric effect of the insulator can cause cracks in the semiconductor layer. The transistors with a dielectric layer showed no fatigue, this could mean that the amount of charge that is switched during each cycle, creates defects at the cost of the semiconductor layer. Chemical

interaction at the semiconductor/insulator interface could cause degradation of the semiconductor layer. For example, when charge carriers with a high energy are filling defect states, the energy is liberated and can cause more defect states.

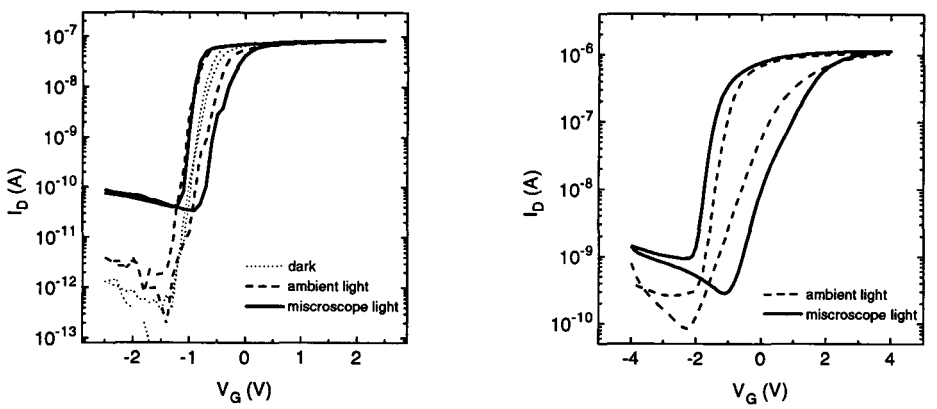
5. Endurance experiments

Chapter 6

Light dependence and temperature behaviour

In this chapter we will discuss the influence of light on the transistor behaviour. Then the temperature behaviour in a range of 20 K to 600 K will be discussed of the thin film as well as the bulk ferroelectric field-effect transistor.

6.1 Light dependence



(a) F_{thin} (L×W=10×250 μm^2).

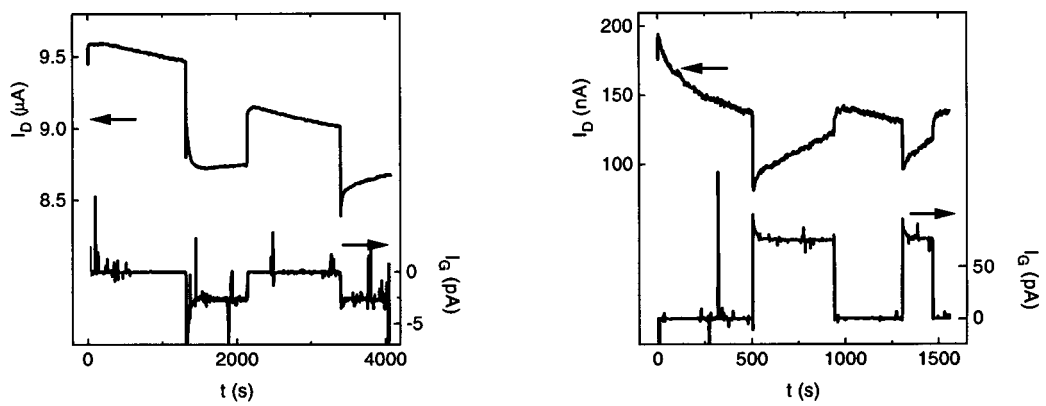
(b) D_{thin} (L×W=20×300 μm^2).

Figure 6.1: Transfer characteristics of wafer F_{thin} and D_{thin} under different light conditions (V_D = 0.1 V).

In figure 6.1 transfer characteristics of two wafers are depicted measured at different light conditions. Figure 6.1(a) shows three different transfer characteristics of wafer F_{thin}, measured in dark, in ambient light and with light added from with a microscope lamp. The curve when the wafer is placed in dark, is very slim and broadens when the wafer is placed in normal room light or when light from a microscope is added. The minimum current increases when light is added, from about 1 pA to about 100 pA. This is due to an increase in gate leakage current (not shown). The maximum current remains roughly the same in the three different cases.
In figure 6.1(b) two transfer characteristics are depicted. The curve measured in ambient light is more slim than the curve measured when added microscope light. The ON-state current is in the two cases roughly the same but the minimum current is larger when there is light added.

The results above show two matters, namely that the coercive voltage and the gate current increases when the light intensity increases. When the light intensity increases, more charge carriers are created in the semiconductor, causing the depolarization field to be smaller and thus the coercive voltage to be larger.
Due to the light, charge carriers are excited. Electrons can be excited from the gate electrode into the conduction band of the insulator. Or holes, excited into the valence band in the semiconductor layer can move into the valence band of the insulator. The excited charge carriers cause an increase in gate current. As the conduction mechanism of the ferroelectric insulator is unclear, preciser conclusions cannot be drawn.

Figure 6.2(a) shows the time-evolution of the ON-state current of wafer A_{thin}. The sample has been pulsed in to the ON-state with a voltage pulse of 4 V and pulse width of 1 ms. After 1200 s microscope light is added, and switched off at 2100 s. After 3400 s it is switched on again. The figure shows that when no light is added the gate current is zero and the drain current relaxes to a lower current. When light is added the gate current becomes negative ($\sim$ 3 pA) and the drain current suddenly decreases to relax upwards in time. The same behaviour is observed when light is added after 3400 s. Note that there is noise in the gate current which has not been investigated further.
In figure 6.2(b) first the sample is pulsed in to the OFF-state with a voltage pulse of 4 V and pulse width of 1 ms. At two intervals light is added, namely between 500 s and 900 s and between 1300 s and 1450 s. The gate current increases from zero when there is no light to 70 pA when light is added. The drain current decreases also when light is added. The relaxation of the drain current when no light is added is negative and becomes positive when light is added. The same light dependence in gate current is observed in either two states, when the drain voltage is set to zero.



(a) ON-state current

(b) OFF-state current

Figure 6.2: Light dependence of drain and gate current at wafer A_{thin}(V_D = 0.1 V, L×W=10×300 μm^2).

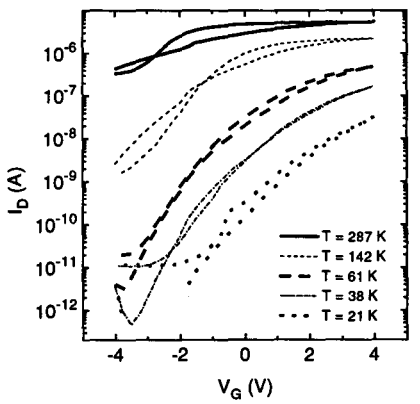
We attribute this the measured gate current to the fact that charge carriers are excited by the light and thus can move in the conduction band or the valence band of the insulator. In the OFF-state the energy bands are bend upwards, the gate-current is positive. For the ON-state the energy bands are bend downwards, causing the gate-current to be negative. The sign of the gate-current corresponds to the correct sign of the depolarization field as is sketched in theory section 2.3.

Both the ON-state as the OFF-state drain current decrease when there is light added; this to the filling of electron trap states in the ferroelectric insulator. As charge carriers now are trapped in the insulator, they will not contribute to the current and thus the drain current will decrease.

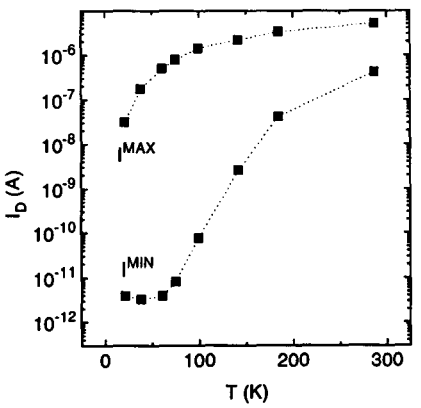
The relaxation of the drain current in the ON-state is upwards when light is added, else it relaxes to a lower drain current. The latter is attributed to the relaxation of the ferroelectric polarization. And when there is light added, the relaxation of the polarization is slower. This could be due to the fact that depolarization fields have become smaller due to the light, resulting in a lower rate of relaxation.
The relaxation of the OFF-state current is negative without light, and positive when light is added. The negative relaxation is attributed to the relaxation of injected charge. The increase in drain-current when there is light added is yet unexplained.

6.2 Temperature behaviour

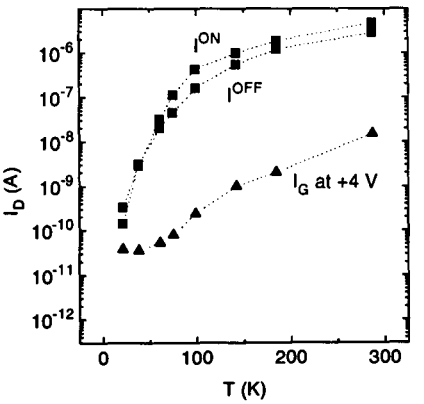
6.2.1 Low temperature behaviour of the thin film ferroelectric field-effect transistor



(a) Transfer characteristic as a function of different temperatures.



(b) Maximum I^{MAX} (measured at +4 V) and the minimum current I^{MIN} (measured at -4 V) as a function of temperature.



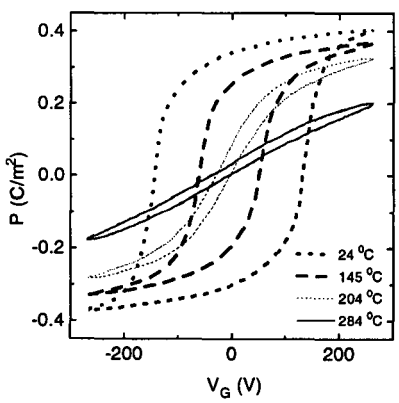
(c) ON- and OFF-state current as a function of temperature.

Figure 6.3: Temperature behaviour of wafer H_{thin} (V_D = 0.1 V, $L \times W$=20×300 μm^2).

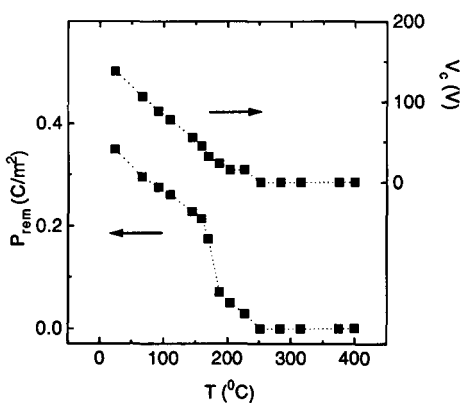
Wafer H_{thin} was mounted on an IC-holder and placed in the He-cryostat. The wafer was then cooled to a minimum temperature of 21 K. In the temperature range from room temperature to 21 K, several transfer characteristics were measured and depicted in figure 6.3(a). In figures 6.3(b) and 6.3(c) data deduced from the transfer characteristics are depicted, like the maximum current I^{MAX}, the minimum current I^{MIN}, the ON-state current I^{ON}, the OFF-state current $I^{OFF}$and the gate leakage current measured at a gate voltage of +4 V. The transfer characteristic at room temperature has a ON/OFF-ratio of 3 and a MAX/MIN-ratio of about one orders of magnitude. At lower temperatures the transfer characteristics get slimmer and steeper resulting in a MAX/MIN-ratio of 5 orders of magnitude at a temperature of 38 K. The gate leakage current decreases roughly logarithmically with a decrease in temperature. The minimum current I^{MIN} decreases also down to a temperature of 80 K, where below I^{MIN} is disturbed by the gate leakage current ($\sim$ 40 pA). The ON- and OFF-state currents roughly decrease the same way when the temperature is getting smaller. The transfer characteristics below 61 K show clockwise rotation, opposite of the ferroelectric rotation direction (counter clockwise).
As the temperature decreases the number of charge carriers also decreases due to less thermal activation, resulting in a decrease in the maximum current. As the resistance increases the voltage drop across the ferroelectric insulator decreases, resulting in non-saturized loop of the ferroelectric layer. This causes the transfer characteristics to become more slim and even the proper hysteresis rotation disappears. The observed hysteresis can be attributed to charge injection. Although the ferroelectric layer is swept in inner loops, there is enough charge displacement to deplete the channel to a difference in MAX- and MIN-state current of five orders of magnitude.

6.2.2 High temperature behaviour of charge displacement

The displaced charge as a function of temperature of a thin film as well as a bulk ferroelectric material have been measured. In case of the thin film ferroelectric material the gate leakage current becomes too high at temperatures above of 150 °C. This results in a non proper hysteresis measurement (not shown). For the bulk ferroelectric layer it is possible to perform hysteresis measurement, due to the absence of a gate leakage current (figure 6.4). Figure 6.4(a) shows that the displaced charge curve gets slimmer when temperature increases, and above 230 °C an almost linear relation between P and V_G is observed. Figure 6.4(b) shows that the remnant polarization decreases from 0.35 C/m^2 at room temperature to zero above 230 °C. The coercive field, V_c, also decreases to zero at the same temperature.



(a) Charge displacement at measured at several temperatures.



(b) Remnant polarization and coercive voltage vs. temperature.

Figure 6.4: Charge displacement as a function of temperature measured at wafer A_{BULK}(f = 70 Hz, C_{ref} = 56 nF, A = 0.18 mm^2).

Literature predicts the same behaviour as we observe [20]. Above a temperature of 230 °C (called the Curie-temperature) there is no net dipole moment in the ferroelectric material, which then becomes dielectric. Therefore it will result in an almost linear behaviour of displaced charge vs. applied field. The remaining hysteresis can be attributed to the presence of a possible series resistance, causing a phase shift of the signal measured at the reference capacitor. For $PbZr_{0.2}Ti_{0.8}O_3$ layers, the Curie-temperature is about 400 °C [20]).

6.2.3 High-temperature transfer characteristics

Figure 6.5 shows several transfer characteristics measured at wafer A_{thin} at different temperatures, from room temperature up to 175 °C. The ON-state current increases with a factor of two in the temperature interval. The OFF-state current increases with three orders of magnitude. The transfer characteristics roughly maintain the same shape with the exception of the increase of drain-current at negative gate voltages (due to an increae in gate current.

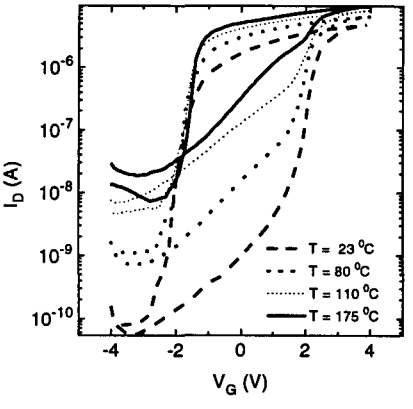


Figure 6.5: Temperature dependence of wafer A_{thin} (V_D = 0.1 V, $L \times W$=5×300 μm^2).

The same experiment as above has been performed at wafer E_{thin}. The maximum temperature to which the wafer is exposed, is about 330 °C. The shape transforms the same way as is plotted in figure 6.5, even at a temperature of 330 °C there is proper hysteresis behaviour. The ON-state current increases with one order of magnitude between room temperature and 330 °C (not shown). Gate leakage current gets large and comparable with the drain current at temperatures above 250 °C. In figure 6.6 the gate current measured at V_G = +5 V is depicted versus temperature. The figure shows that the gate current increases exponentially with temperature. After heating the wafer up to 330 °C, the wafer was exposed to room temperature without any slow cooling down of the wafer afterwards. At room temperature the semiconductor channel at the entire surface does not conduct. Hysteresis measurements at ferroelectric capacitors at the wafer only show a dielectric behaviour.
We attribute the latter to too fast cooling down of the wafer, causing cracks in either the ferroelectric layer or semiconductor channel. The dielectric behaviour of the ferroelectric capacitor can be due to the creation of a dielectric layer of the semiconductor film or due to cracks in the ferroelectric layer itself. The increase in gate current is possibly due to defect conduction. When a leakage current flows through the insulator, it creates more defects, resulting in an increase in leakage current. That there is still hysteresis behaviour at 330 °C, is comprehensible, as the Curie temperature of $PbZr_{0.2}Ti_{0.8}O_3$ is about 400 °C [20].

At wafer H_{thin} transfer characteristics are measured as a function of temperature (see figure 6.7). The characteristics are measured before the wafer is heated. After being exposed to a temperature of 200 °C, the wafer is cooled down slowly (~ 2 hours). Then, again the transfer characteristic is measured. The figure shows that, after the heating process, the current at V_G = +4 V is smaller than the ON-state current with 1 order in magnitude and becomes even negative when V_G is larger

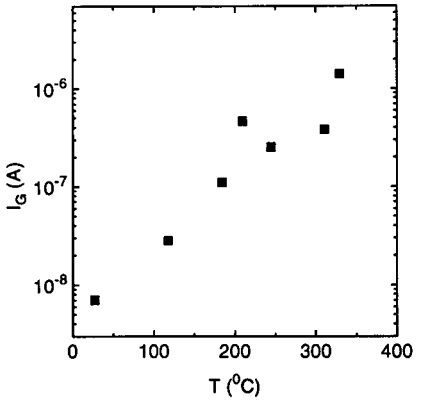


Figure 6.6: Temperature dependence of the gate current (measured at V_G = +5 V) at wafer E_{thin}. ($L \times W$=10×300 μm^2).

than +4 V. The gate leakage current at V_G = +5 V (not shown) is roughly 5 μA. The ON/OFF-ratio drops from 10 to 3. This increase in leakage current is remnant and does not disappear in time. Other transistors at the wafer do not show an increase in gate leakage current at room temperature. We attribute this increase to the large leakage current at 200 °C. This current causes defects in the ferroelectric layer, which are remnant and thus causing a larger gate current after the heating process than before.

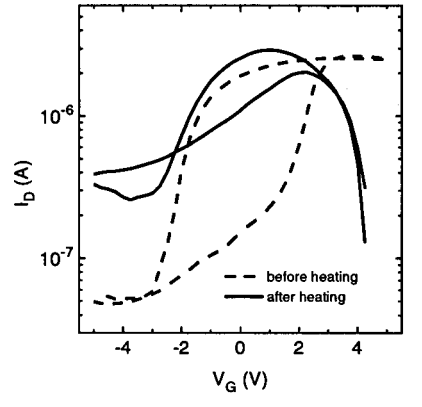


Figure 6.7: Transfer characteristic of wafer H_{thin} at room temperature before and after heating the wafer up to 200 °C. The after heating curve is strongly disturbed by the large gate leakage current (~A). (V_D = 0.1 V, $L \times W$=100×300 μm^2, G=105 μm).

Wafer F_{thin} is exposed to temperatures up to 150 °C. Transfer characteristics are depicted in figure 6.8 in a temperature range from room temperature up to 150 °C. The ON-state current increases with one order of magnitude. The current at V_G = -2 V is disturbed by the gate leakage current which is roughly 10 nA at 150 °C. There is a gap noticeable in the transfer characteristic measured at 150 °C. Gate leakage current which is comparable to the drain current in this region, disturbs the drain current, which becomes even negative. The coercive voltage increases as the temperature increases. After the heating process, the transfer characteristic remained the same as measured before heating.

We attribute the broadening of the transfer characteristics to thermal activation of charge carriers. As temperature increases, more charge carriers are created, and thus the depolarization field becomes smaller, resulting in a larger coercive voltage. The ON-state current increases also due to the amount of charge carriers.

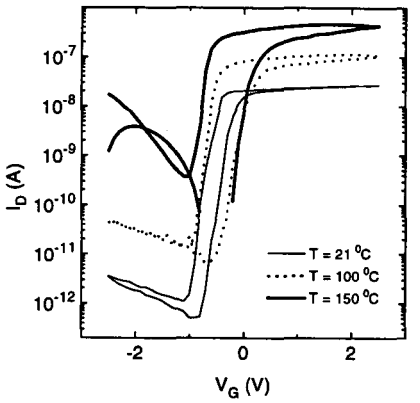


Figure 6.8: Temperature dependence of wafer F_{thin} (V_D = 0.1 V, $L \times W$=10×250 μm^2).

6.2.4 High temperature behaviour of the bulk ceramic transistor

In figure 6.9 transfer characteristics measured at the temperature interval between room temperature and 350 °C are depicted. The ON-state current at a temperature of 119 °C is reduced with a factor of three compared the curve at room temperature. The coercive voltage also has become smaller with a factor of 2.3 (from 70 V to 30 V). The curves at 24 °C and 119 °C show a counter clock wise rotation while the other two (162 °C and 350 °C) rotate clock wise. The curve at 350 °C shows almost no hysteresis. When the wafer is cooled down, the transfer characteristic reproduces as measured before the heating cycle.

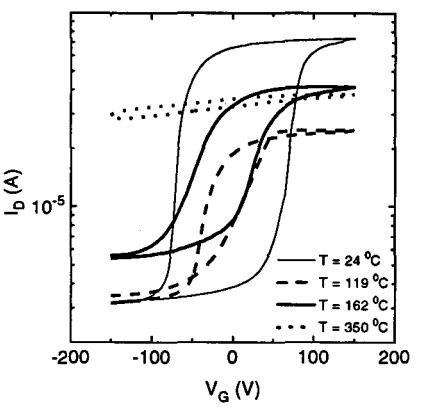


Figure 6.9: Transfer characteristic at several temperatures with wafer C_{BULK} (V_D = 0.1 V, $L \times W$=25×250 μm^2). Note that the 24 °C and 119 °C curves rotate counter-clockwise and the 162 °C and 350 °C curves rotate clockwise.

When the temperature is increased to 119 °C, the polarization is getting smaller as shown in figure 6.4(b) where the polarization vs. the temperature is depicted. Therefore resulting in a smaller ON-state current and larger OFF-state current. The drain current is proportional to the displaced charge, $I_D \sim \Delta\tilde{Q}$. In figure 6.4(b) the reduction in remnant polarization (from 0.34 to 0.22 C/m^2) is roughly by a factor of 1.5 between room temperature and 119 °C, while the difference in drain current (57 and 13 μA) is roughly by a factor of 4. That these two values do not correspond is probably due to the fact that the mobility in both cases is not constant. The reduction in coercive voltage (from 70 V to 30 V) is proportional to the reduction in coercive voltage (from 140 V to 70 V) measured in the hysteresis measurement (see figure 6.4(b)).
Above the Curie-temperature (in this case 230 °C) the ferroelectric behaves like a dielectric, thus resulting a no hysteresis behaviour at a temperature of 350 °C with the exception of a small hysteresis behaviour due to injected charge.
Although there is a ferroelectric hysteresis behaviour at 162 °C as shown in figure 6.9, the curve

exhibits a clockwise direction of rotation. We attribute this phenomenon to charge injection. The injected charge exceeds in this case the polarization of the ferroelectric insulator causing the actual drain-current at $V_G < 0$ V to be larger than the drain current at $V_G > 0$ V. Relaxation experiments show that the OFF-state current decreases in time and the ON-state current increases, just as expected in charge injection relaxation measurements (not shown).

6.3 Summary and discussion

The amount of charge carriers in the semiconductor channel of field-effect transistor can be increased by either adding light causing charge carriers to be excited in the conduction band, or by increasing the temperature causing thermal activation of charge carriers. When the amount of charge carriers increases, the depolarization field decreases, causing the coercive voltage to increase. When light is added the ON-state current only changes within a factor of 2, which is small compared to the ON/OFF-ratio (normally larger than 2 orders of magnitude).
We have shown that a large difference in the maximum and minium current can be obtained, if we adjust the amount of charge carriers in the semiconductor channel, in this case by lowering the temperature to 40 K.
At high temperatures up to 300 °C, the gate leakage current becomes so high in a transistor with a thin-film insulator, that defects are created in the insulator which are non-reversible. A bulk insulator shows no leakage current. Thus using a bulk ferroelectric insulator makes the device operational even for temperatures up to the Curie temperature (400 °C for $PbZr_{0.2}Ti_{0.8}O_3$). A disadvantage of a thicker insulator is that the voltage necessary to switch the device also increases.

Chapter 7

Relaxation of the channel conductance

Knowledge of the retention time of a memory state is important for memory application. Therefore we will investigate the stability of the channel conductance for the ON- and OFF-state. Also the time-evolution of the channel conductance is studied as function of different applied voltage pulses.

7.1 Thin film transistors with a ferroelectric insulator

The time evolution of the drain current is depicted in figure 7.1, for the ON-state as well as the OFF-state. The channel is pulsed with a voltage pulse of 6 V and pulse width of 1 s. The figure shows that the logarithm of the ON-state current slowly decreases linear with the logarithm of time (roughly 16 % per decade). The logarithm of the OFF-state current increases with the logarithm of time (roughly 60 % per decade). The ON/OFF-ratio at t = 50 s is roughly 700 and after 10^4 s it is reduced to a ratio of roughly 170. Extrapolating the curves, the two curves would intersect after roughly 10^9 s ($\approx$ 30 years). This time-scale is huge and therefore it is more of interest after what time-scale the ON-OFF-ratio is reduced to 10. Extrapolating the curves, this time-scale is roughly 10^7 s ($\approx$ 100 days).

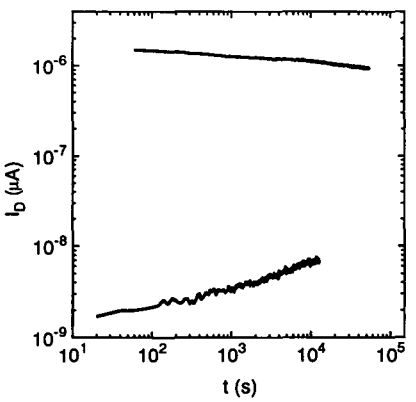


Figure 7.1: Time evolution of the drain current measured at wafer C_{thin} (pulse height = 6 V, pulse width = 1 s, V_D = 0.1 V, $L \times W$=20×300μm^2, G=16μm).

In figure 7.2 the time evolution of the drain current is depicted for different voltage pulses applied to the gate electrode with different pulse heights (between 3 and 5 V). To measure the time evolution of the ON-state, the channel is first pulsed into the OFF-state, whereafter a positive voltage pulse is applied to the gate electrode. Then the drain-current of the ON-state is measured. The same

action is repeated for the time evolution OFF-state.
The figure shows that the ON-state current pulsed with a pulse height of 3 V decreases in time, while the ON-state currents pulsed with a pulse height of 4 and 5 V first increase and then decrease in time. For the OFF-state current, pulsed with a pulse height of 3.5 V, the current first decreases for a short time whereafter it increases. For a pulse height of 4 V the OFF-state current first increases whereafter it increases, only with a smaller slope than the 3 V curve. For a pulse height of 5 V only a decrease in the OFF-state current is observed.
We attribute the increase in drain current in the ON-state to the relaxation of injected charge (see theory section 2.7). Once the charge is relaxed, the current decreases due to relaxation of the polarization of the ferroelectric material. The decrease in current when a voltage pulse of 3 V is applied, is caused by the fact that this voltage is too small to inject charge in the ferroelectric layer. The decrease in the OFF-state current can also be attributed to charge injection. When the voltage pulse increases, it will cause more injected charge in the ferroelectric layer. Thus the relaxation of the injected charge will take more time. Therefore the increase in current starts for the 3.5 V pulse after roughly 30 s, while for the 5 V pulse no increase is observed after roughly 500 s.

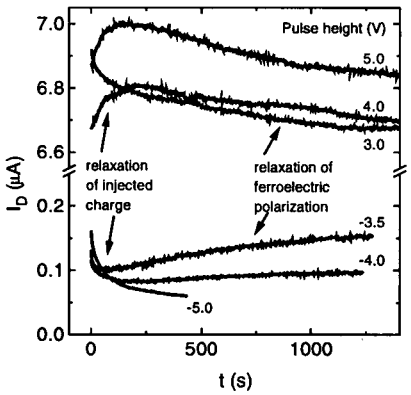


Figure 7.2: Time evolution of the drain current with different applied voltage pulses, measured at wafer A_{thin} (pulse width = 1 ms, V_D = 0.1 V, $L \times W$=20×300 μm^2, G=16μm).

7.2 Transistors with a bulk ferroelectric insulator

At wafer C_{BULK} the time evolution of the ON-state and OFF-state current has been determined during 10^5 s (roughly 1 day). Figure 7.3 shows the time evolution of the drain-current of both states. The OFF-state remains nearly constant and after 5 10^4 s there is an sudden increase in current. The ON-state shows a linear decrease with the logarithm of time (~ 20 % per decade).
We attribute the decrease in ON-state current to the relaxation of the polarization. However the behaviour of the OFF-state current is not understood. It is expected to increase due to the relaxation of the ferroelectric layer, but it remains constant for 3 10^4 s.

In figure 7.4(a) the time evolution of the ON-state current is depicted after several voltage pulses are applied (between 100 V and 150 V). First the channel was pulsed in the OFF-state with the same pulse height, whereafter the channel was pulsed into the ON-state. The figure shows that the ON-state current remains constant for roughly 50 s whereafter it decreases linearly with the logarithm of time. The slope of the decreasing part of the curves is nearly the same for all the different applied voltage pulses. In figure 7.4(b) the time evolution of the channel conductance is depicted. The OFF-state current remains constant for 100 s whereafter it increases linearly with the logarithm of time. The slopes of the curves are nearly constant for the different applied voltage pulses.
The behaviour of the ON-state current after 100 s is attributed to the relaxation of the ferroelectric

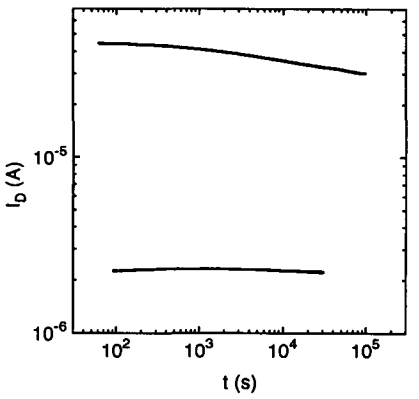
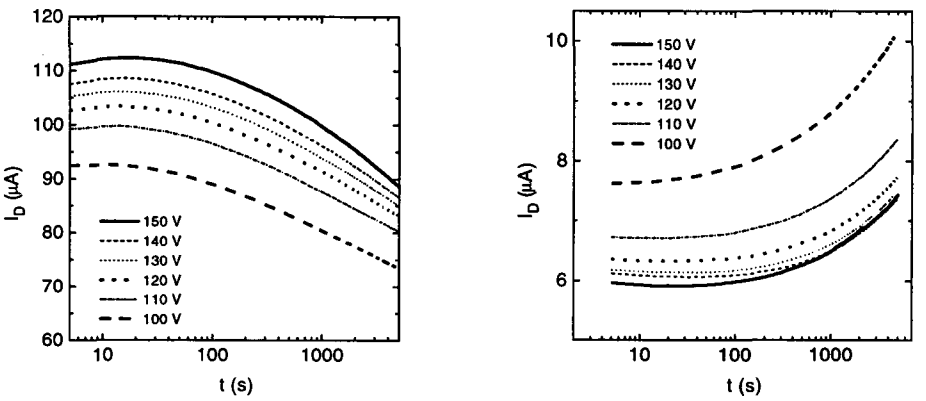


Figure 7.3: Time evolution of drain current measured at wafer C_{BULK} (V_{pulse} = 150 V, τ = 999 ms, $L \times W$=10×150μm^2).

polarization and is the same for different kind of voltage pulses. The constant drain current before 100 s, can be attributed to charge injection. The injected charge causes the drain current to be lower in the ON-state. After a time of 50 s the injected charged is relaxed, whereafter the current decreases. The same argument applies for the OFF-state current.



(a) ON-state relaxation

(b) OFF-state relaxation

Figure 7.4: Time evolution of drain current measured at wafer C_{BULK} for different applied voltage pulses (pulse width 999 ms, $L \times W$=12×250 μm).

7.3 Summary and discussion

The retention time of a memory state for the thin film transistor is roughly 10^7 s. The retention time for the bulk ferroelectric transistor is larger than 10^5 s. Ref. [2] showed for bulk ferroelectric devices a retention time smaller than 10^4 s. After this time the ON-state current was equal to the OFF-state current. The cause of the difference between the two retention times of the bulk ferroelectric devices is unknown. Charge injection has been observed but for the thin film transistor as well as the bulk ferroelectric transistor the influence of injected charge is small (< 5 %); this in contrast to floating gate devices which operate due to the phenomenon of charge injection.

7. Relaxation of the channel conductance

Chapter 8

Field-effect mobility and subthreshold behaviour

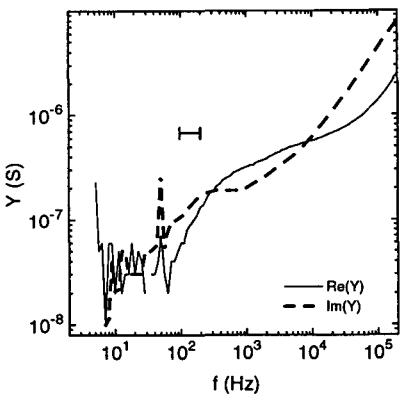
Knowledge of the field-effect mobility of the semiconductor layer is important, as it limits the maximum conductance of the transistor channel. In this chapter we will discuss the field-effect mobility measured with the differential method as explained in section 3.2.7, for transistors with a thin film as well as a bulk ferroelectric insulator. The field-effect mobility can also be obtained in a non-differential way, using the fact that the channel conductance is a function of the field-effect mobility and the displaced charge. This relationship also involves the subthreshold regime.

8.1 Thin film field-effect transistors with a ferroelectric insulator

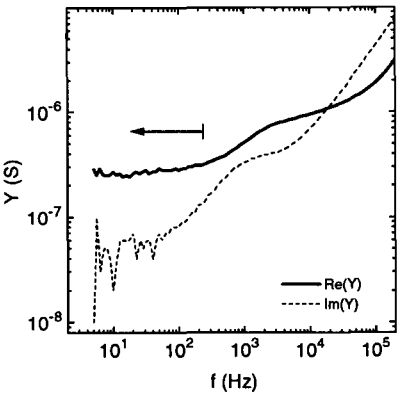
To measure the field-effect mobility according to equation 2.12, we have to measure the gate capacitance, C_G, and the transconductance, g_m. Using a frequency sweep of the capacitance measurement as well as the transconductance measurement, we will obtain the frequency band in which the gate capacitance and transconductance correctly are measured. Then with a gate voltage sweep both quantities are measured as a function of the gate voltage resulting in a calculated mobility as a function of the gate voltage.

In capacitance measurements, resistances in the circuit are always influencing the measurement involving RC-times, which limits the frequency band. We will apply a gate bias voltage of -4 V in order to obtain the highest channel resistance.
Figure 8.1 shows both measurements. In the two-points measurement a bias voltage and oscillating voltage of 0.3 V (rms) is applied. The large oscillating voltage is necessary to obtain a signific output from the impedance analyzer. In panel (a) the real part and the imaginary part of the measured admittance are depicted as a function of the frequency. The imaginary part equals ωC, in other words the imaginary part is proportional to the gate capacitance. Below frequencies of 50 Hz the real part and imaginary part pass through each other. Between 50 Hz and 200 Hz the imaginary part is larger than the real part. The slopes of the imaginary part and real part in this interval are roughly 1 and 2 in this log/log plot. At 100 Hz the imaginary part of the admittance yields 10^{-7} S. Between 300 Hz and 7 kHz the real part of the admittance exceeds the imaginary part, whereafter the imaginary part increases with a slope of roughly 1 in a log/log plot.
The noisy behaviour of the admittance below 50 Hz is due to the fact that the impedance analyzer is not capable of measuring the admittance with a signific output in this frequency range. In the range between 50 Hz and 200 Hz the admittance behaves like the admittance of a capacitor C ($\sim$0.3 nF) placed in series with a resistor R ($\sim$10 MΩ). The admittance Y of such a circuit, yields:

$$Y = \frac{\omega^2 C^2 R + j\omega C}{1 + \omega^2 R^2 C^2} \tag{8.1}$$



(a) Admittance of a two-points measurement in order to measure the gate capacitance; the bar indicates the frequency interval in which the gate capacitance can be measured.



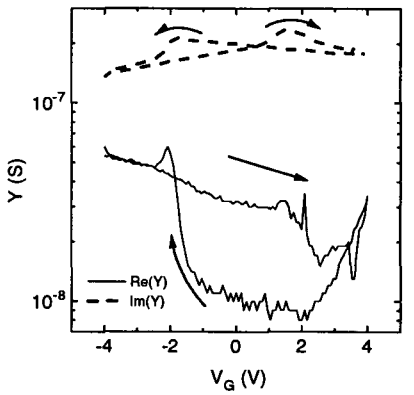
(b) Admittance of a three-points measurement in order to measure the transconductance. The arrow indicates the frequency interval in which the transconductance can be measured.

Figure 8.1: Gate capacitance measurement and transconductance measurement at a transistor at wafer A_{thin} at a gate bias voltage of -4 V. (f = 100 Hz, V_D = 1 V, V_{OSC} = 0.3 V, $L{\times}W$=100×300μm^2, G=105μm).

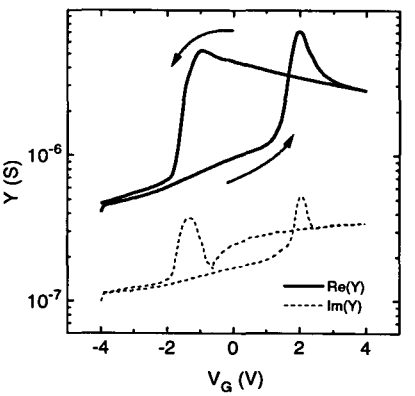
We see that when $\omega < (RC)^{-1}$ that the imaginary part vs. frequency holds a linear dependence (slope of 1 in a log/log plot) while the real part shows a square behaviour (slope of 2 in a log/log plot). The measured capacitance per square at a frequency of 100 Hz (0.01 C/m^2) roughly equals other measurements at $PbZr_{0.49}Ti_{0.51}O_3$ capacitors with metal electrodes [13]. Above a frequency of 7 kHz the imaginary part increases again, we attribute this to a parasitic capacitance (~8 pF). Therefore we can conclude that in the frequency interval between 50 Hz and 200 Hz the gate capacitance can be accurately determined. This interval is plotted with a bar in panel (a).

In Panel (b) the admittance is determined in the three points measurement. An oscillating voltage with a bias voltage (-4 V) is applied at the gate electrode and at the drain electrode a voltage of 1 V is applied. The real part of the admittance shows a little increase in the frequency interval up to 200 Hz, whereafter the imaginary part becomes roughly equal to the real part and exceeds the real part after 10 kHz.
The little increase up to 200 Hz is attributed to the slow filling of trap states. When the frequency increases, these trap states cannot be filled resulting in a higher conductance. At higher frequencies the real part is disturbed by the imaginary part which roughly equals the measured capacitance in panel (a). We can conclude that in the frequency up to 200 Hz, the transconductance is correctly measured. Above 200 Hz, the transconductance is disturbed by the real part of the admittance measured in the gate capacitance measurement.

We have determined the frequency at which the gate capacitance as well as the transconductance has to be measured, namely between 50 and 200 Hz. In the gate voltage sweep measurement we choose 100 Hz for the frequency. The gate voltage is swept from a negative bias to a positive bias and back again. In figure 8.2 the gate capacitance as well as the transconductance are depicted. In panel (a) the gate capacitance and the real part of the admittance are depicted. The real part is smaller than the gate capacitance by a factor between 3 and 10. The gate capacitance is roughly constant and shows two peaks, and each peak is positioned at the coercive voltage of the ferroelectric material. The same curve has been observed by Ref. [13].
Panel (b) shows the transconductance vs. the bias gate voltage. The imaginary part is about one order smaller than the transconductance. From -4 V the transconductance increases slowly and



(a) Gate capacitance measurement.



(b) Transconductance measurement.

Figure 8.2: Gate capacitance measurement and transconductance measurement at a transistor at wafer A_{thin}. The arrows indicate the rotation direction as the gate voltage is swept. (Same parameters as in figure 8.1).

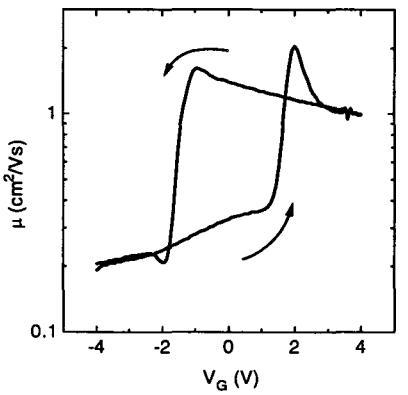


Figure 8.3: Field-effect mobility vs. gate voltage measured at wafer A_{thin}. The arrows indicate the rotation direction as the gate voltage is swept (Same parameters as in figure 8.1).

at +1.5 V the transconductance suddenly increases with a factor of 7 and starts to decrease after this peak. From a positive gate voltage to a negative gate voltage the transconductance increases and drops at -1.5 V whereafter it coincides with the other curve.

The increase after a gate voltage of +2 V can have two causes. Firstly, when there is a contact resistance present and the channel is brought into accumulation, the transconductance is limited by the conductance of such a contact resistance. The real transconductance of the channel becomes larger as the gate voltage increases. But because the contact resistance is independent of the gate-voltage, the transconductance will tend to zero. Secondly, when there is charge injection present, more charge will be injected as the gate voltage increases. This results in a decrease in transconductance as there are less charge carriers available. However there is no peak observed at a negative gate voltage. It is unlike that in this case only charge injection occurs at positive voltages. The minimum resistance in the transfer characteristic is roughly 15 kΩ, which is roughly equal to the determined contact resistance (see section 4.4). From the transfers characteristic (not shown) the charge injection is roughly 20 % at positive applied voltages and a factor of 5 at negative voltages.
The absence of a peak in the transconductance measurement at negative gate voltages and the

fact that the minimum resistance is roughly equal to the contact resistance, sustain the statement that the transconductance at positive gate voltages ($V_G > 2$ V) is limited by a contact resistance.

In figure 8.3 the field-effect mobility calculated with equation 2.12 is depicted. As the gate capacitance measurement showed a nearly constant behaviour, the mobility curve resembles the transconductance curve. We observe a mobility of maximum 2 cm^2/Vs and a minimum mobility of 0.2 cm^2/Vs. The maximum mobility is in good agreement with the Hall-mobility measured in Hall measurements [7] which is roughly 2 cm^2/Vs.

8.2 Field-effect transistors with a bulk ferroelectric insulator

To measure the mobility for a bulk ceramic transistor the same approach is used as mentioned in the previous section. First the correct frequency interval (50~400 Hz) was determined with a frequency sweep. Then with a gate voltage bias sweep, the gate capacitance and the transconductance are measured. Combining the two results with equation 2.12 gives the field-effect mobility which is plotted in figure 8.4 for a transistor at wafer C_{BULK}.
The maximum field-effect mobility is roughly 3 cm^2/Vs, while the minimum mobility yields 0.08 cm^2/Vs. Note that the curve in the figure resembles with the curve in figure 8.3. At wafer B_{BULK} the measurement is also performed, resulting in a mobility between 0.3 and 2 cm^2/Vs.

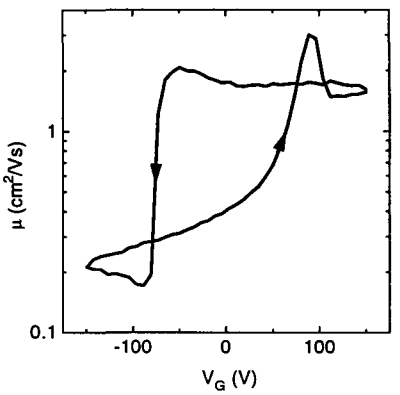
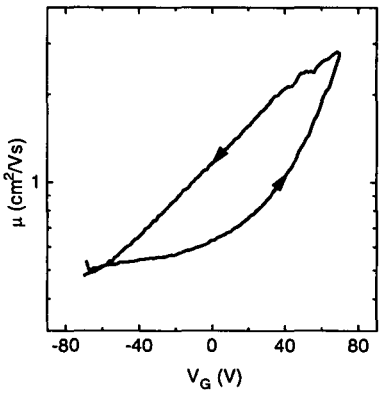


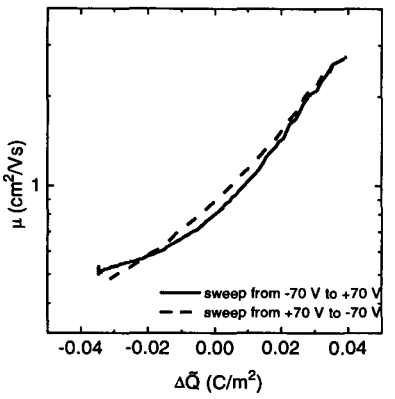
Figure 8.4: Field-effect mobility vs. gate voltage measured at wafer C_{BULK}. (f = 100 Hz, V_{osc} = 4 V, $L \times W$=25×250μm^2).

Using the transfer characteristic we can obtain the minimum channel resistance, which is about 8 kΩ. The contact resistance (see section 4.4) is 2 kΩ. The transconductance measurement (not shown) showed for positive gate voltages and for negative voltages a peak. As the channel resistance is higher than the contact resistance, we attributed these two peaks to the charge injection. This results also in two peaks in the calculated mobility versus gate voltage.

As there could be charge injection present, sweeping at inner loops would result that the charge injection is less. Therefore instead of sweeping up to 150 V, we applied a maximum gate bias voltage of 70 V. In figure 8.5(a) the mobility is depicted. It does not show any peaks as in the previous measurements. In figure 8.5(b) the mobility is depicted against the displaced charge measured with a Sawer-Tower circuit (f = 200 Hz, C_{ref} = 56 nF). The two curves, i.e., the forward sweep and the backward sweep coincide.
Hall measurements [21] with a 30 nm In_2O_3:Sn layer with the same doping concentration on a epitaxial $PbZr_{0.2}Ti_{0.8}O_3$ layer yield a larger value for the mobility (8 cm^2/Vs). We attribute this to the fact that the ceramic bulk material is porous. Therefore the contact areas of grains in the semiconductor layer are smaller, which results in more scattering, yielding a smaller mobility.



(a) Mobility vs. applied gate voltage.

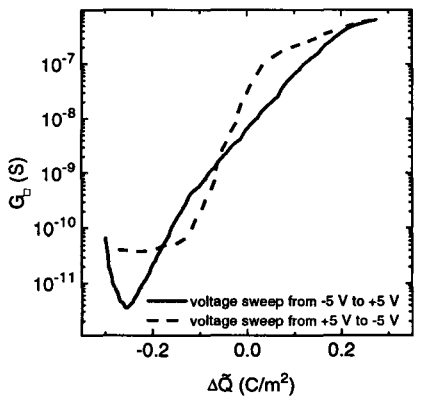


(b) Mobility vs. displaced charge.

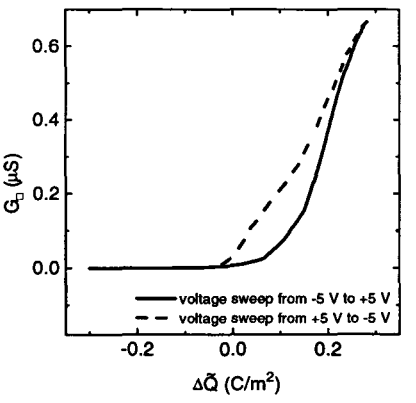
Figure 8.5: Mobility measured at a maximum applied voltage smaller than the coercive voltage (wafer C_{BULK}, f = 250 Hz, V_{osc} = 4 V, $L \times W$=50×250μm^2).

8.3 Subthreshold slope

To investigate the subthreshold behaviour, we have to create a conductance vs. displaced charge graph. Using the displaced charge measurement and the transfer characteristic given in figure 4.1, figure 8.6 is created. In panel (a) the sheet conductance is plotted at a logarithm vertical scale for either the forward voltage sweep and the backward voltage sweep. The logarithmic of conductance vs. the displaced charge shows a quite linear behaviour, but the forward and backward curve do not coincide. The increase in sheet conductance below $\Delta\tilde{Q}$ = -0.2 C/m^2 is due to the influence of gate leakage current, and should therefore be ignored. In panel (b) the sheet conductance is plotted at a linear vertical scale. At positive values of displaced charge the conductance shows a linear behaviour, but the forward and backward curve do not coincide. Using equation 2.7, the field-effect mobility is obtained from the slope of the forward curve (at $\Delta\tilde{Q}$ = +0.2 C/m^2) in the graph and yields 0.1 cm^2/Vs.



(a) Sheet conductance depicted at a logarithmic vertical scale.

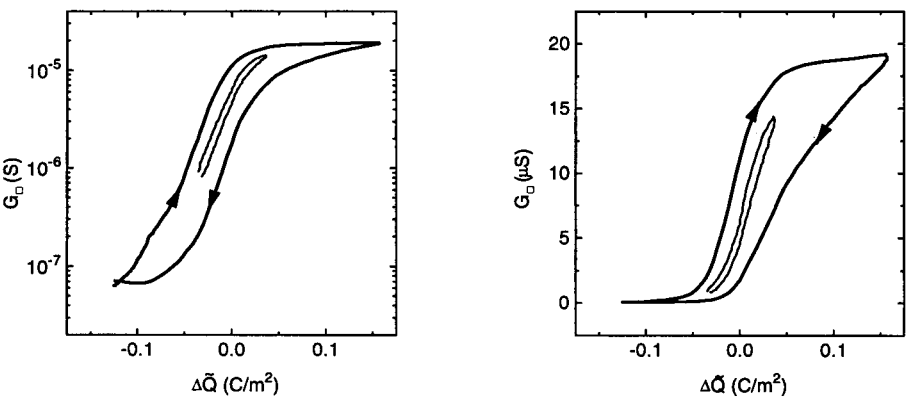


(b) Sheet conductance depicted at a linear vertical scale.

Figure 8.6: Sheet conductance vs. displaced charge measured at wafer C_{thin}. The charge displacement measurement and the transfer characteristics from figure 4.1 are combined in this graph. ($L \times W$=5×300μm^2, G=4μm).

The observed behaviour is in good agreement with the theory section 2.6. For a negative charge displacement we observe a exponential relationship between the channel conductance and the displaced charge, while for a positive charge displacement the channel conductance is proportional to the charge displacement.

In figure 8.7 a similar measurement is depicted. The charge displacement is measured at a MIS-diode ($200\times200\mu m^2$) with a Sawyer-Tower circuit (f = 90 Hz, C_{ref} = 56 nF), while the transfer characteristic is measured using a drain voltage of 0.1 V and a frequency of 0.03 Hz. The sheet conductance vs. displaced is depicted, the outer loop is measured with a gate voltage amplitude of 4 V while the inner loop is measured with a gate voltage amplitude of 2 V. Panel (a) shows that the slope of the forward and backward curve are roughly the same, but in panel (b) the forward loop coincides with the backward loop at a positive amount of displaced charge. From the slope (at $\Delta\tilde{Q}$ = 0.1 C/m^2) the field-effect mobility yields 0.9 cm^2/Vs.
We attribute the horizontal shift between the forward and the backward curve in both figures to charge injection. For example, at a negative charge displacement, positive charge carriers are injected into the ferroelectric layer. This results in an increase in channel conductance. At a positive charge displacement, the injected charge relaxes and now negative charge carriers are injected in the insulator, causing the conductance to be smaller than the conductance in case there is no charge injection.



(a) Sheet conductance vs. displaced charge at a logarithmic vertical scale.

(b) Sheet conductance vs. displaced charge at a linear vertical scale.

Figure 8.7: Sheet conductance vs. displaced charge measured at wafer A_{thin}. The outer loop is obtain measuring with a gate voltage amplitude of 4V, while the inner loop is obtained with a gate voltage amplitude of 2V ($L\times W$=100×300μm^2, G=95μm^2).

In figure 8.6 and in figure 8.7 the field effect mobility is determined to 0.1 cm^2/Vs and 0.9 cm^2/Vs, respectively. As the semiconductor layer has the same thickness and composition, the difference is rather large. However, the lower mobility is measured on a transistor with a shorter source-drain length (5 nm) than the transistor with a higher mobility (100 nm). We now will show that this is caused by a series resistance or a contact resistance.
With $G_\square = \mu\Delta\tilde{Q}$ (equation 2.7), the mobility is obtained. The sheet conductance $G_{\square,calc}$, is calculated using the meaured conductance G_{meas} and the geometry of the device:

$$G_{\square,calc} = \frac{L}{W} G_{meas}. \tag{8.2}$$

The reciprocal of the measured conductance is related to the real sheetresistance of the channel

$R_{\square,chan}$ and any other series resistance R_{series} (including a contact resistance):

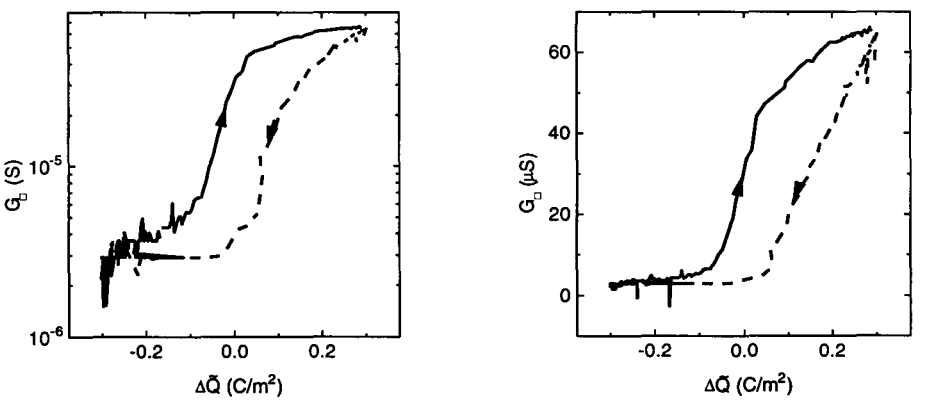
$$G_{meas}{}^{-1} = \frac{L}{W} R_{\square,chan} + R_{series}. \tag{8.3}$$

Thus the calculated sheet conductance is related to (equation 8.2):

$$\begin{aligned} G_{\square,calc} &= \frac{L}{W}\left[\frac{L}{W} R_{\square,chan} + R_{series}\right]^{-1} \\ &= \left[R_{\square,chan} + \frac{W}{L} R_{series}\right]^{-1} \end{aligned} \tag{8.4}$$

The last equation shows that when L increases the term with R_{series} decreases. This results in an increase in the calculated sheet conductance and therefore an increase in the mobility. In our case the series resistance also depends on the source-drain length, as a part of the channel which is not covered by the gate increases from 1 μm to 5μm. However the increase in channel length is a factor of 20, and this results always in a increase of the calculated sheet conductance and therefore an increase in mobility.

In figure 8.8 the same measurement is repeated. Charge displacement and transfer characteristic are measured at the same frequency. The measured frequency is 1 Hz, as at higher frequencies the gate switching current is disturbing the channel conductance measurement. The charge displacement is measured with a Sawyer-Tower circuit (C_{ref} = 1 Hz), while the channel conductance is measured by a voltage drop over a reference resistance of 330 Ω. The same behaviour is observed as in the previous figure. Charge injection causes a shift in the two curves. From the slope the field-effect mobility yields 2.8 cm^2/Vs, which is similar to the differential measured mobility. This value is not limited by the presence of a contact resistance (~2 kΩ, see section 4.4), as the minimum channel resistance is roughly 10 kΩ.



(a) Sheet conductance depicted at a logarithmic scale.

(b) Sheet conductance depicted at a linear scale.

Figure 8.8: Sheet conductance vs. displaced charge measured at wafer C_{BULK} (f = 1 Hz, C_{ref} = 330 Ω, R_{ref} = 330 Ω, V_D = 1 V, L×W=150×250μm^2).

8.4 Summary and discussion

We showed that the calculated field-effect mobilities are limited in case of the thin film transistor (μ = 2 cm^2/Vs) by a contact resistance and in case of the bulk ferroelectric transistor

(μ = 2 cm^2/Vs) by charge injection. The calculated mobilities are in good agreement with the mobility determined using the sheet conductance versus charge displacement graphs (thin film μ = 1 cm^2/Vs; bulk ferroelectric μ = 3 cm^2/Vs). Charge injection causes a shift in the channel conductance versus charge displacement. Without the occurrence of injected charge, we would expect no hysteresis behaviour of channel conductance versus displaced charge.

Chapter 9

Conclusions

In this report we presented the electrical characteristics of several field-effect transistors, the most important being an operating depletion-type thin-film field-effect transistor with a ferroelectric insulator. The remnant polarization of the ferroelectric insulator causes the channel to be fully depleted, resulting in a difference in resistance of nearly four orders of magnitude between channel depletion and non-depletion. A few concepts arise in this report overlapping the different chapters and therefore they will be discussed here.

The *depletion of the transistor channel* can be influenced in a few ways. Increasing the doping concentration and the thickness of the semiconductor channel, or increasing the environment temperature, cause the channel to contain too much charge for depletion. In the case that the amount of charge carriers is low, the ferroelectric material is influenced by a depolarization field, which can be reduced by increasing the light intensity or the environment temperature.
The maximum conductance is limited by the field-effect mobility and the maximum charge displacement. The minimum conductance is limited by the charge displacement of the insulator and the depolarization field. In order to lower the minimum conductance, either the charge displacement has to increase or the depolarization field compared to the coercive field has to be reduced. The first can be done by using other ferroelectric materials with a larger charge displacement. The influence of a depolarization field can be reduced by either increasing the insulator thickness or reducing the semiconductor thickness.

Charge injection causes a reduction of induced charge in the semiconductor channel. Pulse measurements show that the amount of injected charge increases as the applied gate voltage increases. Relaxation measurements show also the occurrence of charge injection. The injected charge influences the channel conductance by an amount smaller than 5% for the ON-state current, and for the OFF-state current by an amount smaller than a factor two. Endurance measurement show that the influence of injected charge for the ON-state current increases to a factor of 2 in channel conductance, due to the fact that the channel resistance is longer comparable to the contact resistance. At higher temperatures we observed for the transistor with a bulk ferroelectric layer, that charge injection is dominating the field-effect, while the polarization decreases. The field-effect of charge injection is similar to the field-effect in floating gate devices.

The presence of a possible *contact resistance* between the mobyldenum contact pads and the semiconductor layer, has been shown in a few experiments; first of all, by variation of the length of the semiconductor channel. Secondly, by comparing the transfer characteristics using a four-points measurement or a two-points measurement. Pulse measurements show no-charge injection for ON-state current, when the ON-state resistance is comparable to the contact-resistance. The measured field-effect mobility turnes out to be smaller than the real mobility when there is a contact resistance present. This contact resistance is due to a $BaZrO_3$ capping layer between the contact pad and the semiconductor channel.

We have shown that the *life-time* of the device can be reduced in two ways. First, the device is sensitive to repeated switching, and shows a crucial fatigue behaviour after 10^6 switching cycles. Secondly, gate leakage currents cause irreversible defects in the thin film ferroelectric insulator at high temperatures ($> 200°C$); this in contrast to the bulk ferroelectric transistor which is not affected by exposing to high temperatures. To solve the first problem, further research has to done to investigate the degradation mechanism of the semiconductor layer. If operation at high temperatures using a thin film ferroelectric device is needed for applications, new ferroelectric materials with lower leakage currents have to be investigated.

For future directions the following remarks are made. Other deposition methods could be considered, as pulsed laser deposition is not suitable for real production. The preliminary investigation using a spun SnO_2 semiconductor layer showed promising results. A large difference between the minimum and maximum resistance ($\sim 10^5$) was observed.
If operation at high temperatures of the thin film ferroelectric transistor is necessary for applications, the ferroelectric insulator should be improved to reduce gate leakage currents. When the operation of the device is necessary at a bias gate voltage, the maximum resistance can be increased if another insulator with smaller leakage currents is used. To obtain a larger ON-state conductance, first the contact resistance has to be eliminated, and the mobility of the semiconductor layer should increase. Therefore further research has to be done to investigate new semiconductor materials and the deposition method has to be reconsidered; this, because the semiconductor layer is consisting out of grains which are limiting the mobility. Increasing the grain size, should result in a higher mobility.

9.1 Acknowledgments

My graduation professor J.H. Wolter is acknowledged for giving me the oppurtunity to perform my graduation project at Philips Research Laboratories. I am indebted to Menno Prins for his continous enthousiastic mentorship, to the members of the *New Oxidic Thin Film* project Hans Cillessen, Ben Giesbers, and Harry van Esch, besides wafer preparation, for their abundant material- and processing knowledge. I would like to thank my fellow students at Philips for giving my stay a more student-like character: Bas Hendriksen, Benoit Lemonnier and Diederik B.A. Rep. The latter, together with M. Kerskes, is thanked for their enthousiastic and challenging discussions about physical as well as non-physical matters.

References

[1] J.L. Moll and J. Tarui, *A new solid state memory resistor*, IEEE Trans. Electron Devices **ED-10**, pp. 338-339 (1963)

[2] J.C. Crawford and F.L. English, *Ceramic Ferroelectric Field Effect Studies*, IEEE transactions on electron. devices, **ED-16** 6, pp. 525-532 (1969)

[3] S.Y. Wu, *Memory retention and switching behavior of metal-ferroelectric-semiconductor transistors*, Ferroelectrics **11**, pp. 379-383 (1976)

[4] J.F.M. Cillessen, *Pulsed laser deposition of oxidic films*, thesis University of Twente, the Netherlands (1996)

[5] E. Pastoor, *Electrical characterization of oxidic thin film field effect devices*, Report of the graduation project at Phlips Research Laboratories (1995)

[6] R.P. Weening, *Memory effect of all-oxide transparent thin film transistors*, Report of a traineeship at Philips Research Eindhoven (1995)

[7] B.L.M. Hendriksen, *Electrical characterization of Pulsed Laser Deposited semiconductive SnO_2 and ZnO:Al thin films for use in an all-oxide transistor*, Report of a training at the Philips Reasearch Laboratories, (1996)

[8] P. Wurfel, I.P. Batra, and J.T. Jacobs, *Polarization Instability in Thin Ferroelectric Films*, Physical Review Letters **30**, 24, pp. 1218-1221 (1973)

[9] R.R. Mehta, B.D. Silverman and J.T. Jacobs, *Depolarization fields in thin ferroelectric films*, J. Appl. Phys., **44**, 8, pp. 3379-3385 (1973)

[10] S.M. Sze, *Physics of semiconductor devices - 2nd Edition*, Wiley, New York (1981)

[11] Diederik B.A. Rep and Menno W.J. Prins, *A compact model for a ferroelectric field-effect transistor*, Technical Note, Philips Research Laboratories (1997)

[12] C.H. Seager, D.C. McIntyre, W.L. Warren, and B.A. Tuttle, *Charge trapping and device behavior in ferroelectric memories*, Appl. Phys. Lett **68** 19, pp. 47-68 (1996)

[13] P.K. Larsen, G.J.M. Dormans, D.J. Taylor, and P.J. van Veldhoven, *Ferroelectric properties and fatigue of $PbZr_{0.51}Ti_{0.49}O_3$ thin films of varying thickness: Blocking layer model*, J. Appl. Phys. **76** 4, pp. 2405-2413 (1994)

[14] K.-O. Grosse-Holz, J.F.M. Cillessen, M.W.J. Prins, P.W.M. Blom, R.M. Wolf, L.F. Feiner, and R. Waser, *Semiconductive behavior of Sb doped SnO_2 thin films*, Epitaxial Oxide Thin Films II, Mater. Res. Soc. Symp. Proc. **401**, 67 (1996)

[15] J.B. Giesbers, M.W.J. Prins, J.F.M. Cillessen, and H. van Esch, *Dry etching of all-oxide transparent thin film memory transistors*, to appear in Microelectronics Engineering (1997)

[16] C.B. Sawyer and C.H. Tower, *Rochelle salt as a dielectric*, Physical Review **35**, pp. 269-273 (1930)

[17] R. Moazzami, *Ferroelectric thin film technology for semiconductor memory*, Semicond. Sci. Technol. **10**, pp. 375-390 (1995)

[18] H.M. Duiker, P.D. Beale, J.F. Scott, C.A. Paz de Araujo, B.M Melnick, J.D. Cuchiaro, and L.D. McMillan, *Fatigue and switching in ferroelectric memories: Theory and experiment*, J. Appl. Phys. **68**, pp. 5783-5791, (1990)

[19] R. Moazzami, C. Hu, and W.H. Shepherd, *Endurance properties of ferroelectric PZT thin films*, IEEE Tech. Digest Int. Electron Devices Meeting pp. 417-420 (1990)

[20] L.L. Hench and J.K. West, *Principles of electronic ceramics*, John Wiley & Sons, New York, pp. 254-273 (1990)

[21] R.A. van Dam, *Electrical characterization of In_2O_3:Sn as channel material for a ferroelectric field effect transistor*, Report of a training at Philips Reasearch Laboratories Eindhoven (1996)

[22] M.W.J. Prins, S.E. Zinnemers, J.F.M. Cillessen, and J.B. Giesbers, *Depletion-type thin-film transistors with a ferroelectric insulator*, Appl. Phys. Lett. **70** 4, (1997)

Appendix A

Developed Labview software

The experimental setup has been automized using a graphical oriented programming language, LABVIEW. In this appendix we first explain the principle of LabVIEW, followed with a description of the several developed programs.

A.1 LabVIEW

LabVIEW is a program development application, much like C or Pascal. However, LabVIEW is different from those applications in one important respect. Other programming packages use text-based languages to create a programming code, while LabVIEW uses a *graphical* programming language to create programs in a block diagram form. LabVIEW is a general-purpose programming system with extensive libraries of functions for any programming task. LabVIEW includes libraries for data acquisition, GPIB control, data analysis, data presentation and data storage. The LabVIEW environment also includes conventional program development tools, like single step debugging, and breakpoint setting.

A.2 Hysteresis measurement

A program to measure the hysteresis loop with a Sawyer-Tower circuit has already been made [6]. In this program hysteresis measurements are performed with the option to measure at several frequencies. We adapted this program to use it at one single frequency. After initializing the necessary instruments, an AC voltage from a function generator (PM5139) is applied to the device and to the x-channel of the Tektronics oscilloscope. The voltage across the reference capacitor is connected with the y-channel of the oscilloscope. After a delay time (default 4 s) the program reads out the display of the oscilloscope and writes the data to disc. To the AC voltage, a DC bias voltage can be added. Also an external DC voltage can be applied to the device.

A.3 Pulse measurement

This program uses two function generators (HP8161a) and a HP Semiconductor Analyzer (HP4145a). The principle of a pulse measurement is to measure the source-drain current after a voltage pulse is applied to the gate electrode. Two pulse generators are used to give either a positive or negative voltage pulse. After initializing the instruments the program sets a desired pulse width and pulse height at the pulse generators. Then it triggers one of the pulse generators and measures the source-drain current after a delay time. This step is repeated for the other pulse generator. These two steps are then repeated for an entire sequence, first with a variable pulse height and secondly with a variable pulse width.

A.4 Endurance measurement

The goal in an endurance measurement is to switch the device continuously using a square wave and measuring after a certain amount of cycles the ON- and OFF-state current. The ON- and OFF-state currents can be measured in two ways:

- After a pulse is given by the pulse generator,
- or during a constant gate voltage (positive or negative).

The last option is used in an endurance test of a device without a memory effect. After initializing the instruments one pulse generator is set to produce a continuously running square wave. After a certain amount of cycles (counted by a programmable timer/counter PM 6666) the output of the pulse generator is switched off and the ON- and OFF-state current are measured in the two possible ways. The pulse generator which produces the continuously block wave is then switched on again. This entire loop is repeated and the program terminates when a maximum number of cycles has passed.

A.5 Relaxation measurement

To measure the time evolution of the drain current, a positive voltage pulse is applied to the gate electrode. The HP Semiconductor analyzer samples the drain current, with a desired sample time (default 10 s). When the total measurement time has elapsed, the measured current as a function of time is written to disc. The same action is then repeated for a negative voltage pulse. This entire sequence can be repeated for other (user-defined) voltage pulses with a pulse height and a pulse width.

A.6 Impedance measurement

This measurement uses the HP4192 impedance analyzer. A frequency or a bias voltage sweep can be performed. After initializing the instrument, the frequency and the bias voltage are set. The impedance is then measured by the analyzer and sent to the memory of the computer. This action is repeated for a variable frequency or bias voltage. Afterwards the data is written to disc.

Appendix B

Mask layout

B.1 Mask set 1

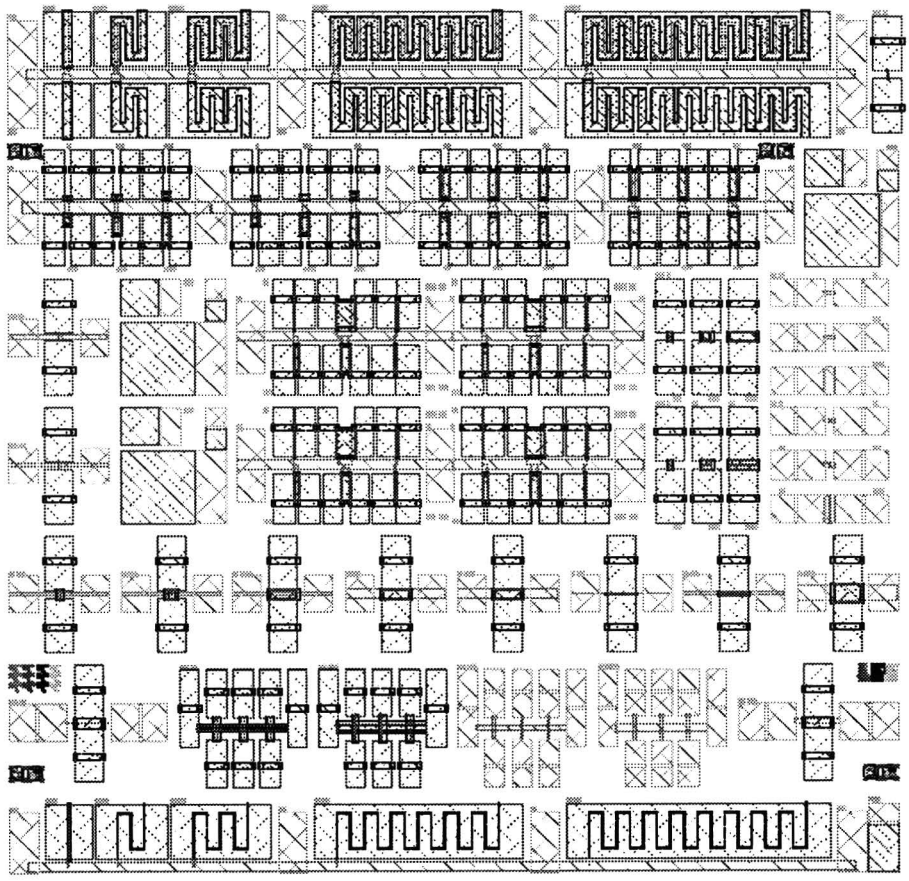


Figure B.1: FET1 mask set

B.2 Mask set 2

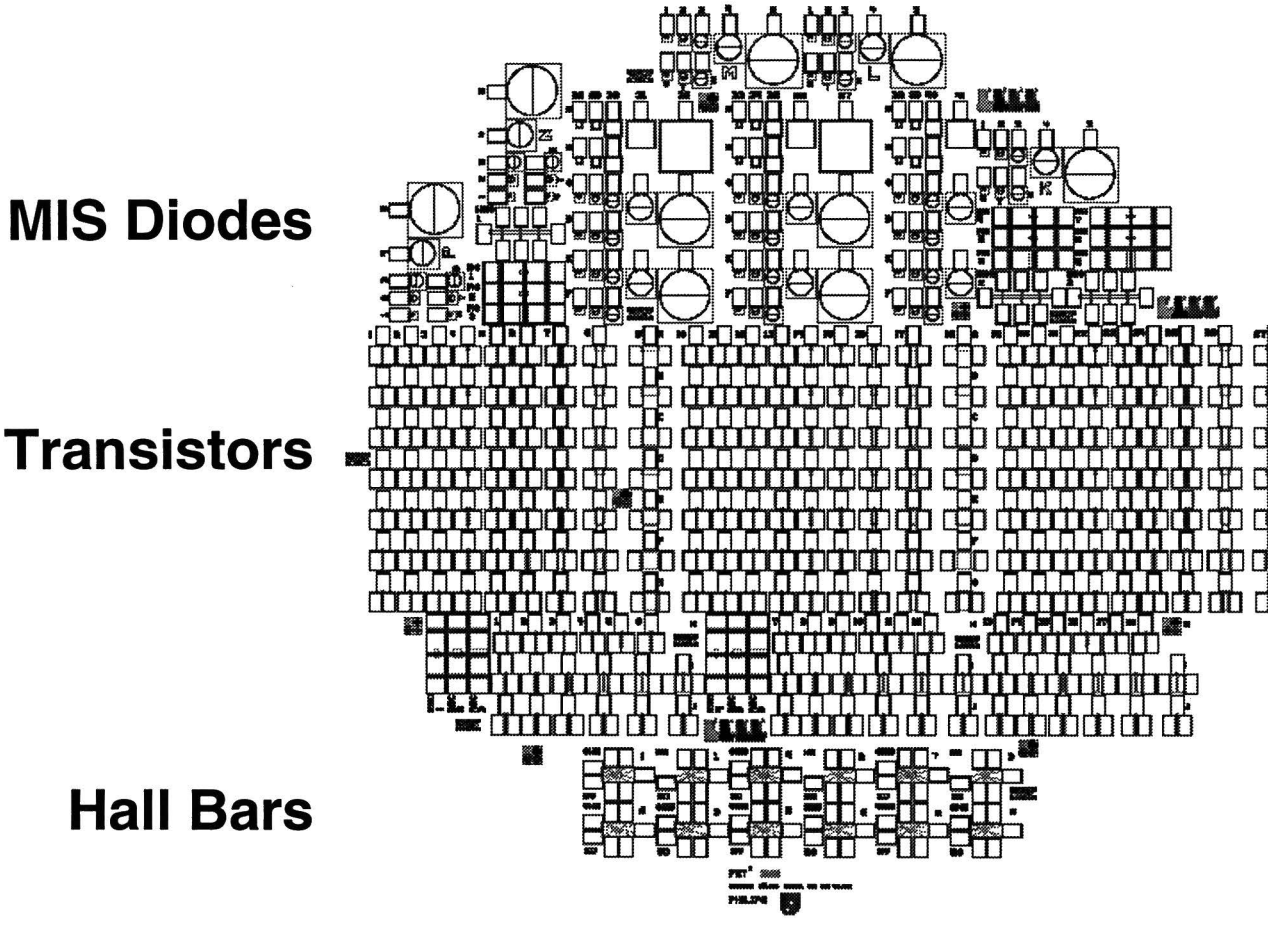


Figure B.2: FET2 mask set

Appendix C

Presented posters and published article

In this appendix, two posters are depicted. The first poster *All-oxide transistors* was presented at the National Solid State day at the Eindhoven University of Technology (8 may 1996). The second poster *A compact model of ferroelectric field-effect transistors* was presented at the F.O.M. days in Veldhoven (18 december 1997).
An article *Depletion-type thin-film transistors with a ferroelectric insulator* is published in *Applied Physics Letters* [22]. As the article is not available at the moment of printing this report, an abstract is given below.

Depletion-type thin-film transistors with a ferroelectric insulator

M.W.J. Prins, S.E. Zinnemers, J.F.M. Cillessen, and J.B. Giesbers

We present a study of electrical characteristics of ferroelectric field-effect transistors made of $PbZr_{0.2}Ti_{0.8}O_3$ and SnO_2:Sb thin films. Due to properly chosen semiconductor parameters, the transistor channel can be totally depleted by the ferroelectric charge displacement. The observed remnant on/off ratio of the channel current amounts to 7×10^3. Pulse response measurements give information on data retention, device speed, and the occurrence of charge injection. The results lead to important design considerations for ferroelectric transistors.

C. Presented posters and published article

ALL-OXIDE TRANSISTORS

S.E. Zinnemers *), B.L.M. Hendrikson **), J.F.M. Cillessen, and M.W.J. Prins

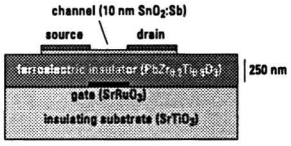
Philips Research Laboratories, Eindhoven, Prof. Holstlaan 4, 5656 AA Eindhoven, The Netherlands
*) Department of Semiconductor Physics, Eindhoven University of Technology, The Netherlands
**) Faculty of Applied Physics, University of Twente, The Netherlands

Introduction

New functions can be implemented in a transistor by using special materials in the design. In this poster we present a novel thin-film field-effect transistor with non-conventional oxidic constituents:

- The insulator consists of a ferroelectric material, giving rise to a memory behavior.
- The channel consists of SnO_2:Sb, a

Thin-film transistor



Materials

- The substrate is a polished $SrTiO_3$ (100) single crystal.
- The gate electrode consists of an epitaxial $SrRuO_3$ film.
- The insulator is composed of an epitaxial ferroelectric $PbZr_{0.2}Ti_{0.8}O_3$ layer.

Previous studies show an excellent ferroelectric behaviour for the combination of these perovskite-type materials (in a capacitor).

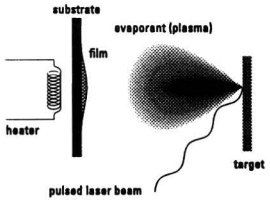
- The semiconducting channel consists of an Sb doped SnO_2 film.

SnO_2:Sb is a well known transparent conductive oxide, however, for the first time we apply SnO_2:Sb for its semiconductive properties in a transistor. Our films show a fine grained structure (grainsize 30-60 nm). For SnO_2 films with a Sb doping concentration ranging between 10^{17} and 10^{20} cm^{-3}, Hall measurements show n-type conduction and carrier mobilities upto 10 cm^2/Vs.

Transistor preparation

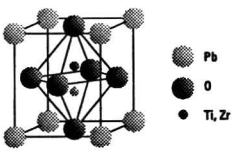
The thin films are grown by pulsed laser deposition. First a conducting $SrRuO_3$ layer is deposited on $SrTiO_3$ and gate electrodes are structured by reactive ion etching. Thereafter, the $PbZr_{0.2}Ti_{0.8}O_3$ and the SnO_2:Sb films are grown. The channel is defined by structuring the SnO_2:Sb.

Pulsed laser deposition:
An intense pulsed laser beam explosively evaporates an amount of target material. Species of the induced expanding plasma are deposited on the heated substrate. This way a stoichiometric transfer of target material onto the substrate is achieved.



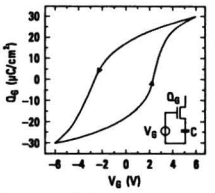
Memory states

The remnant electrical polarization of the ferroelectric insulator causes a displacement of the charge carriers in the semiconductor: $\sigma_{sc} = \varepsilon_0 E_{fe} + P_{fe}$, with σ_{sc} the charge density in the semiconductor, E_{fe} the electrical field in the ferroelectric layer and P_{fe} the ferroelectric polarization.



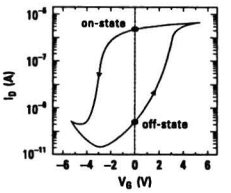
Bistable ionic displacement causes ferroelectric polarization.

Charge displacement



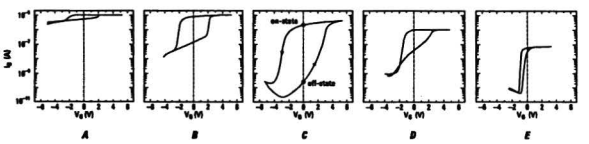
The electrical charge per unit gate area displaced in the ferroelectric insulator (Q_G) as a function of the gate voltage (V_G). The displaced charge is measured with an external capacitor C (see inset).

Transfer characteristic



Transfer characteristic (I_D versus V_G). The source is at zero potential and V_D=0.1 V. The gate leakage current (I_G<0.5 nA) disturbs the transfer characteristic below –3V.

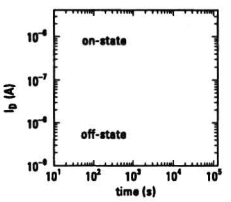
Transfer characteristics for different transistors. The hysteresis behaviour is due to the ferroelectric polarization.



	A	B	C	D	E
$R_\square$ (Ω)	2.4×10^4	2.6×10^4	2.6×10^4	2×10^5	4×10^6
Semiconductor thickness (nm)	12	10	10	5	10
Sb doping concentration (cm^{-3})	4×10^{19}	4×10^{19}	4×10^{19}	4×10^{20}	4×10^{19}
Insulator thickness (nm)	250	250	250	225	350

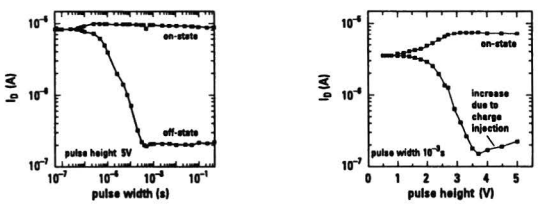
Relaxation measurements

Time evolution of the drain current, with V_G=0 V and V_D=0.1 V. At time=0 a gate voltage pulse is applied, with an amplitude of +6 V for the on-state and –6 V for the off-state (transistor C).



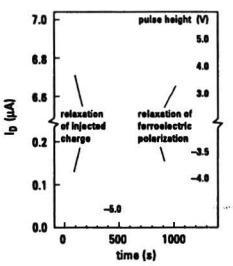
Pulse measurements

A minimum pulse width and height is required to switch the polarization (transistor B).



Charge injection

Charge injection into the insulator occurs for large pulse height. This reduces the electric displacement. Charge injection may be compared with charge storage in a floating gate device (transistor B).



Summary and conclusions

We demonstrated the operation of field-effect transistors made of optically transparent oxidic thin films. The transistors exhibit a memory function due to the usage of a ferroelectric insulator. Our optimize

C. Presented posters and published article

A compact model of ferroelectric field-effect transistors

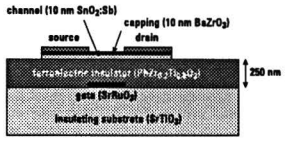
D.B.A. Rep*, S.E. Zinnemers and M.W.J. Prins**

Philips Research Laboratories, Prof. Holstlaan 4, 5656 AA Eindhoven, The Netherlands
* Department of Applied Physics, University of Groningen, The Netherlands
** Department of Applied Physics, Eindhoven University of Technology, The Netherlands

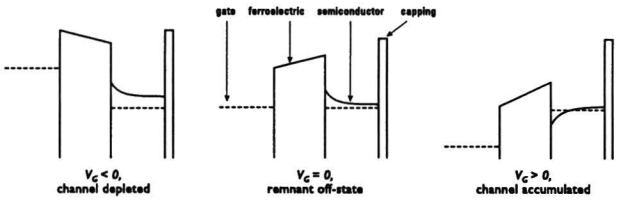
Introduction

A thin-film field-effect transistor with a ferroelectric insulator has been developed. This device is similar to a standard field-effect transistor, only the oxide has been replaced with ferroelectric material, enabling the transistor to be used as *non-volatile* memory device. Modeling can serve to gain more insight into the operation of the device. Therefore a compact model has been developed to describe the ferroelectric as well as the (polycrystalline) semiconducting layer.

Ferroelectric transistor

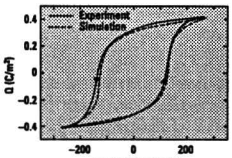


Band diagram



Modeling the ferroelectric layer

Previously proposed models of the ferroelectric layer are not appropriate for a compact description. Some are too mathematical for treatment in a device simulation package, others are far from based on the physical properties of ferroelectric layers. On the basis of a compact description of ferroelectric charge displacement, we propose a model that consists of only a few electronic components, namely resistors (energy dissipation) and capacitors (charge storage).

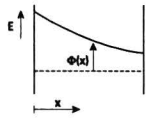


The ferroelectric charge displacement can be described by a compact model.

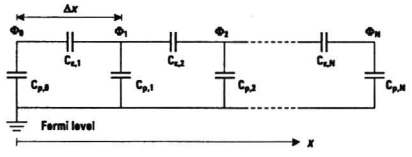
Modeling the semiconductor layer

Band-bending

The charge that is induced in a unit area semiconducting layer of thickness s is correlated with the band-bending $\Phi(x)$ of the conduction band-edge.
$\Phi(x)$ is described as a function of charge density $\rho(x)$ by Poisson's equation $\nabla^2\Phi = \frac{-\rho}{\varepsilon_0\varepsilon_r}$.



Poisson's equation can be solved using an electronic equivalent circuit:



$$C_{\varepsilon,i}: \quad Q_{\varepsilon,i} = \frac{\varepsilon_0\varepsilon_r}{\Delta x}\,[\Phi(x_i) - \Phi(x_{i+1})] \qquad \text{(dielectric capacitors)}$$

$$C_{\rho,i}: \quad Q_{\rho,i} = -e\int_{-\infty}^{\infty} f(E)\,D(E-\Phi_i)\,dE + Q_0 \qquad \text{(filling of states)}$$

$D(E)$: density of states
$f(E)$: Fermi-Dirac distribution function
Q_0 : to ensure that $Q_{\rho,i} = 0$ for $\Phi_i = 0$

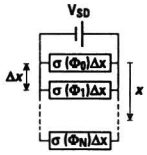
Transport

If we assume a constant mobility for the electrons in the conduction band, we have for the source-drain conductivity:

$$\sigma(x) = e\cdot\mu\cdot\int_{\Phi(x)}^{\infty} f(E)\,D(E-\Phi(x))\,dE$$

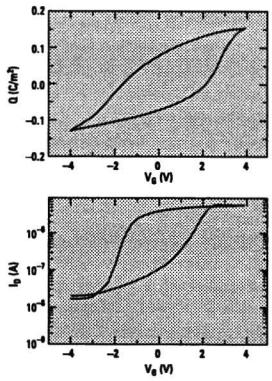
Finally, the sheet-conductance is modeled by an array of resistors:

$$G_\square = \int_0^s \sigma(x)\,dx$$

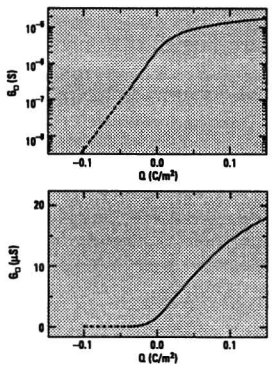


Experiment

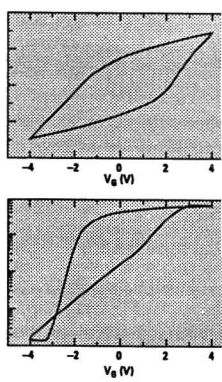
Ferroelectric behaviour

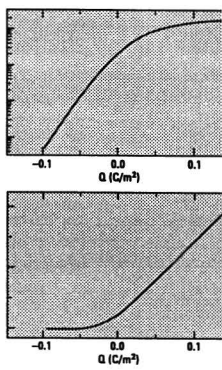


Semiconductor properties



Simulation



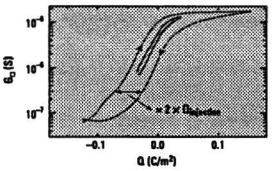


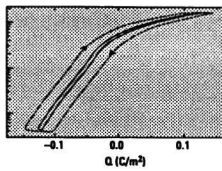
The combined model correctly describes the operation of the transistor.

From analysis of the data and simulations, it follows that:

- The hysteresis of the transistor is due to the ferroelectric charge displacement.
- The modulation of the channel conductance is mainly caused by semiconductor depletion.
- The density of states inside the bandgap D_g (E) is constant and approximately 10^{21} $cm^{-3}eV^{-1}$, i the correct range for a micro-polycrystalline semiconductor.
- The field-effect mobility is about 1 cm^2 / Vs, similar to the measured Hall-effect mobility.
- The semiconductor thickness effective for transport is less than the nominal thickness. This ca be due to the granular structure of the film or due to channel depletion near the capping layer.

Interface properties





The experimental curves show hysteresis behaviour due to charge injection. For the inner loop le charge injection occurs. Charge injection is modeled by a resistor and a capacitor at the ferroelectri semiconductor interface.

Summary and conclusions

We demonstrated that a ferroelectric field-effect transistor can be described with a compact mod consisting of only capacitors and resistors. The model describes the ferroelectric charge displacemen depletion of the semiconductor channel and charge injection into the interface. Comparison wit transient experiments (device speed, relaxation of the ferroelectric and the injected charge) should allo for further model improvements.

Acknowledgments

The authors are indebted to J.F.M. Cillessen, J.B. Giesbers and H.A. van Esch for sample preparation.

Philips Research

PHILIPS