Design of a low power 100MHz, 8-bit, bipolar, folding Analog-to-Digital Converter

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"Design of a low power 100MHz, 8-bit, bipolar, folding Analog-to-Digital Converter"

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ABSTRACT

The architecture of this 8-bit ADC is based on a three-stage conversion, using Cascaded Folding & Interpolating techniques. Compared to the other multi-stage ADC architectures, Folding & Interpolating ADCs are based on non-linear analog preprocessing the input signal. This architecture is an attractive solution for ADCs, as extremely linear circuit topologies are not required. In order to raise the resolution of Folding & Interpolating ADCs, without rising the number of parallel input stages or the number of comparators in the fine-comparator, a Cascaded Folding & Interpolating architecture is used. The ADC preprocessing part achieves a 55 dB Spurious-Free Dynamic Range (SFDR), while quantizing a 50 MHz full-scale input signal at 100 MSample/s. The ADC will be fabricated in an advanced bipolar IC process and the preprocessing part only dissipates 6 mW from a single 3.0 V supply. The preprocessing part consists of the fine folding circuit with input gain stages, reference ladder and bias circuits and the total coarse signal generation. This report is based on simulation results. Additional the layout of the preprocessing part has been extracted. For further research, the implementation of the folding ADC offers possibilities to scale down the power consumption when the bipolar process is better stabilized. The 'Nat. Lab.' transistors parameters, used in the first simulations, should be better implemented in the IC-lab in Hamburg. The total ADC power can be scaled down a factor 3. Also a two metal layer (or more) bipolar process, with small interconnect via's, reduces the total wirering capacitance and saves more power.

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LIST OF SYMBOLS

ADC		: Analog-to-Digital Converter
A		: amplitude of output voltage input stage amplifier
b		: gain at zerocrossing
c		: voltage step between two non-interpolated nine folding signals
DAC		: Digital-to-Analog Converter
DNL		: Differential Non Linearity [LSB]
F9.	(A to D)	: nine folding signal at the output of the interpolation ladder
g		: normalized delay variation
INL		: Integral Non Linearity [LSB]
δ_{INL}		: interpolated zerocrossing - ideal zerocrossing [LSB]
ipf		: interpolation factor
LSB		: Least Significant Bit Value defined as V_{range} / (ipf * N_{ref})
N_{ref}		: number of voltage levels in the reference ladder
SFDR		: Spurious-Free Dynamic Range
S/H		: Sample and Hold
SNR		: Signal to Noise Ratio
t_d		: delay time
δt_d		: delay time difference
VCC		: voltage supply of 3V
$V_{ref\,(high,\,i,\,low)}$		: voltage reference source (high =2.5V, i $\in$ [1,36], low = 1.5V)
V_{in}		: input voltage (maximum voltage range = 1V)
V_{inp}		: differential input voltage of the input gain stage
V_{tt}		: output voltage swing of differential output of amplifiers
V_{lr}		: linear range of the input gain stage
V_{range}		: maximum input voltage range defined as $V_{ref,max}$ - $V_{ref,min}$ - 4*c
$V_{s..}$	(1 to 36)	: output signals of the input gain stages
$V_{sc..}$	(1 to 36)	: complementary output signals of the input gain stages
$V_{s..} - V_{sc..}$	(1 to 36)	: differential output signals of the input gain stages
$V_{f..}$	(1 to 12)	: output signals of the three folding blocks
$V_{fc..}$	(1 to 12)	: complementary output signals of the three folding blocks
$V_{f.}$	(A to D)	: output signals of the three folding comb. blocks
$V_{fc.} - V_{f.}$	(A to D)	: differential output signals of the three folding comb. blocks
δV_y		: difference between two folding signals
x		: V_{in}

PREFACE

This master thesis is performed at the Philips Research Laboratories and the Eindhoven Technical University. The simulations, in the beginning of the assignment, are performed at the University with the circuit-simulator HSPICE. The final part of the assignment is performed at the Philips Research Laboratories. Here, linearity and distortion measurements on the Analog-to-Digital Converter are performed, and the layout of the chip is developed. The total design of the Analog-to-Digital Converter (ADC) is split up into two parts. The analog preprocessing part of the ADC is described in this report. The 'digital' part is designed by Roland van Wegberg and will be described in his report. The workgroup, where these simulations are performed, is called "Integrated Transceivers". The aim of this group is to do research into signal processing and electronics design for integrated circuits and electronic equipment and terminals. Nearly all the expertise's of the group are essential to personal communication products. The application field for the Analog-to-Digital Converter is the digital cellular mobile telephone market.

1. INTRODUCTION

Advances in consumer electronics are creating new requirements for high speed data converters: Personal (portable) communication products requires all 6-12 bit converters with power dissipation as important key parameter. The demand for low power consumption with fewer batteries in applications such as wireless and personal communications have motivated engineers scaling down the supply voltage and to develop new IC processes. The availability of high speed analog-to-digital converters gives in digital receivers the opportunity to realize some of the base-band and intermediate frequency processing to be done in the digital domain. The advantage of digital receivers is that they can be made programmable to comply with different standards and that they can be integrated into IC's in order to get very compact (receiver) circuits. At this moment the disadvantage of fully integrated digital receiver circuits is that they consume relative high power. Therefore, the introduction of digital receivers will be done first in base stations, car systems and television receivers. With the use of new IC process techniques, the introduction of more digital signal processing circuits in a receiver will be inevitable in the future. The A/D converter, as described in this report, is making use of a new advanced bipolar IC technology, which can be useful in designing low power integrated circuits.

At first in this report, there will be a short introduction about A/D converter architectures where the folding A/D converter is derived from. The converter is a combination of the well known flash A/D converter [6,7,15] and the two-step A/D converter [20,21]. A short overview of these two types ADC's is described below.

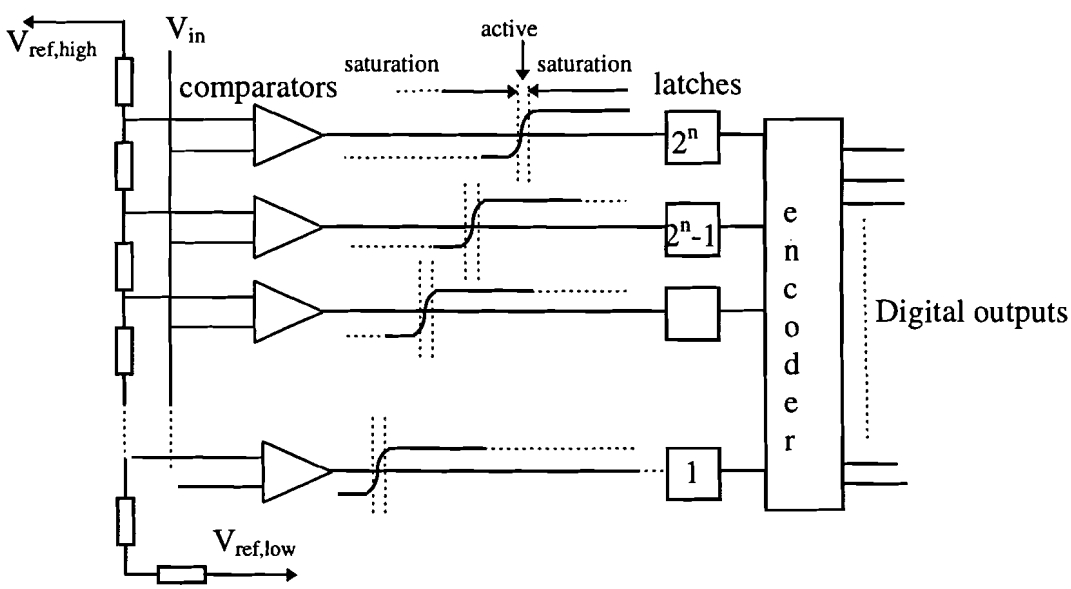


Figure 1.1 : Full-flash A/D converter structure

The most straightforward technique to convert an analog signal into an 8-bit output code is the so called 'full-flash structure' (see Figure 1.1). The full-flash architecture requires (2^n-1) comparators, with n the number of bits. The power, die-area and the input capacitance are proportional to (2^n-1). An 8-bit flash structure requires 255 comparators, together with a set of 255 reference voltages to define all quantisation levels of the ADC. In practice, there is a limit to the power dissipation that can be handled in IC packages. Therefore, the power-dissipation in the comparators stage must be reduced drastically to keep the over-all power dissipation as low as possible. The bandwidth of the system is related mostly to biasing currents, which in turn results in power dissipation. Because of increase of the die size, it is difficult to distribute the clock and input signal lines, and to match all the properties of all these comparators within the same specification. The large numbers of comparators also makes it difficult to make a clockdriver, which can drive the heavy (capacitive) loading. Small rise and fall times are difficult to obtain for these clockdrivers. When a ramp is applied at the input, S-shaped curves will be generated at the output of the comparators. It also can be seen from figure 1.1 that over the entire full-scale input range a sample latch in a full parallel implementation only makes *one* decision that results in a change of the output code. The use of the latches is not efficient. The comparator outputs yield a thermometer-like code and only the position in the array of the transition between ONE's and ZERO's contains relevant information concerning the immediate level of the analog signal. When the output of, for instance, comparator k is "high", all comparator outputs below k are known to be "high". Although this is common practice in full-flash converters, there is no need to retain the output levels of the comparators that are known anyway during the sample process. Therefore, full-parallel systems retain information that is redundant.

To avoid some problems encountered with the full-flash converter, the two-step architecture was developed. This structure reduces the amount of comparators drastically. The two-step architecture uses a coarse and a fine quantisation to increase the resolution of the converter. At first, a coarse decision is made, using a k-bit flash ADC.

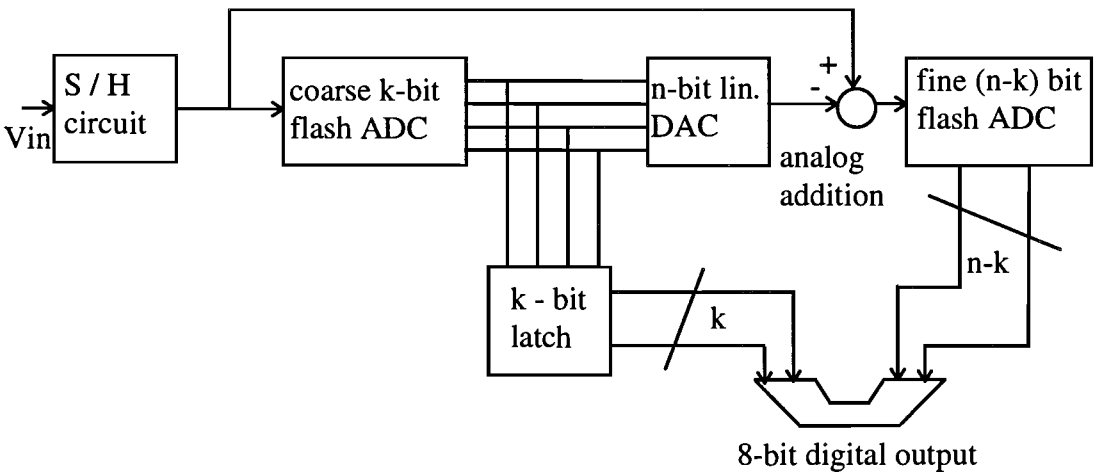


Figure 1.2 : Two-step A/D converter structure

This decision is converted back into an analog value using a digital-to-analog converter (DAC) and is subtracted from the original applied input signal. The residual signal is then converted into a 2^{n-k} quantisation levels using (n-k)-bit fine flash ADC. In this system an ideal coarse-fine matching is required. The succeeding conversion steps takes time. The analog signal, to be converted, is held at a constant value by a S/H amplifier. During this hold time, the conversion takes place making it virtually "timeless". In practical applications, timing and accuracy limitations can result in conversion problems resulting in "missing" codes. The number of comparators is now reduced from 2^n comparators to $(2^k-1) + (2^{n-k}-1)$, which reduces the power dissipation as well as the die area. The DAC must have a resolution of at least n-bit to avoid limiting the performance of the converter. A good balance between circuit complexity, power consumption and die size is obtained in this type of converter. The final dynamic performance however depends on the quality of the S/H amplifier. The structure of the *n*-bits two-step principle is shown in figure 1.2.

The advantages of this structure in comparison with the flash structure are:

- smaller die size
- less hardware then flash structure
- moderate power

The disadvantages are:

- (n-k) DAC needs n-bit linearity
- substractor difficult to implement
- hardware increases exponential with resolution

In a folding analog-to-digital converter the problems discussed above, can be avoided. Therefore this type analog-to-digital converter will be explained in the following chapters. The design parameters of the ADC based on the first transistor models will be shown in the next chapter. Special attention will be given in the following chapters of the design of the preprocessing part of the ADC. Each subcircuit of the preprocessing part will be described thoroughly. Measurements incorporating gain, bandwidth, power dissipation, noise and linearity will be presented from each subcircuit of the preprocessing block. From the finally design a layout is drawn and the floorplan of the preprocessing part will be shown. Finally, conclusions and recommendations on this design will be shown in chapter 11. For the total design of the ADC, with digital part as comparators, rom table, latches and output drivers, will be referred to the graduation report of Roland van Wegberg. In this thesis the final specifications of the total ADC are presented.

2. INITIAL DESIGN SPECIFICATIONS

The goal of this project was to design and implement an 8-bit folding ADC with all the necessary subcircuits. The specifications of the ADC, how they are specified at the beginning of the assignment, are shown in table 1. The specifications are based on the first parameters of the IC process.

Table 1 : Design constraints of the Analog-to-Digital Converter

Technology	bipolar:	SPIRIT
Principle	folding and interpolation architecture	
Resolution	8-bit + overflow/underflow outputs	
Signal to Noise Ratio (SNR)	> 50	dB
Maximum analog bandwidth	50	MHz
Conversion rate	100	MHz
Power consumption	6 - 9	mW → 25 - 30 mW
Analog input signal voltage range	1	V_{pp}
Supply voltage, V_{CC}	3	V

These specifications are an estimation of the performances of a low power A/D converter built in this new IC technology. The technology SPIRIT is an advanced bipolar IC process, which produces very small diffusion capacitors in the transistor. The inevitable process parasitic capacitors, later measured in the process, introduces a heavy load for the small transistors. The specifications shown above are too stringent for the new process parameters. The power dissipation shall increase from 6-9mW to approximately 25-30mW due to these additional parasitic capacitors. The transistor model with parasitics is shown in chapter 5. In that way the other specifications, as shown in table 1, remain the same. These specifications show that the folding ADCs are favorable comparing to the original flash converters. The final specifications of the ADC determined by simulation are shown in this thesis later. From the preprocessing block a layout will be drawn. From this layout, an estimation will be done, incorporating the additional wirering capacitance and dummy resistors and shall all be added in the final circuit of the preprocessing part.

3. FOLDING AND INTERPOLATING PRINCIPLE

3.1 INTRODUCTION

The systems presented here consists only black boxes at this moment. In further chapters, the total implementation of the preprocessing part is discussed. In a folding ADC, the advantages of digital sampling of signals used in a full-flash system are combined with the component saving architecture of the two-step system. No S/H amplifier is required for this system [1,2,3,5,8,9]. The architecture uses an analog preprocessing block to transform the input signal into a repetitive set of output signals to be applied to the fine (flash) converter (see Figure 3.1).

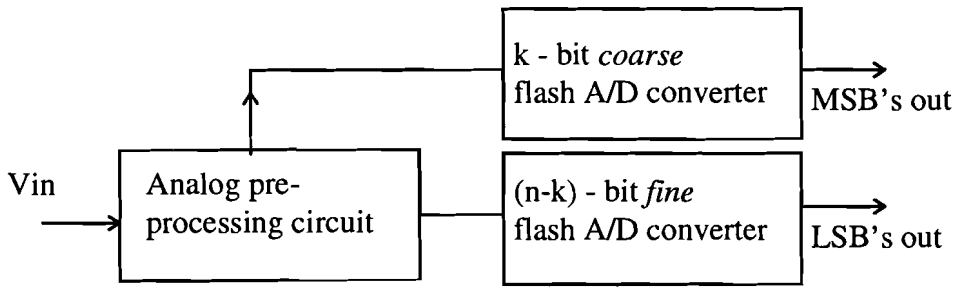


Figure 3.1 : Folding A/D converter architecture

In this system the most significant bits k are determined by the coarse quantizer, which determines the number of times ($k = \lfloor \log_2(\#\text{foldings}) \rfloor$ bit) a signal is folded. The fine bits (n-k) are determined by the fine quantizer which converts the preprocessed "folded" signal into LSB bits. The preprocessing part is a time continuous circuit which contributes a small amount of propagation delay. As example the principle of an 8 times folding process is shown in figure 3.2.

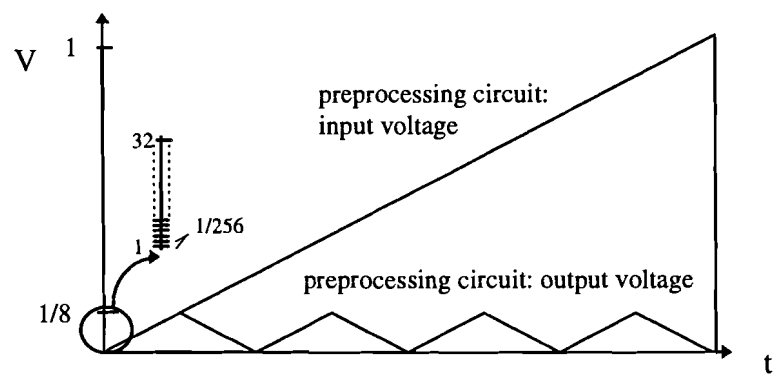


Figure 3.2 : The folding process, input and output voltages V versus time t

Note that for the folded signal a triangular signal is used instead of a sawtooth signal. The discontinuities of a sawtooth signal contain very high frequency components, which are difficult to realize in the circuit. Therefore a triangular signal is being used, containing the same information differently coded.

The input signal is applied to a folding circuit. The folded signal at the output of this circuit is applied to a flash converter. Because the folded signal has a smaller range than the input signal, this flash converter can be small. For example, if the input signal is folded 8 times (see figure 3.2) then the folded signal has only 1/8 of the range of the input signal. To get an 8-bit resolution with the folding A/D converter, the folded signal uses 5 bits or 31 comparators. These 5 bits will indicate the value of the input signal within the eight subranges of the input signal. A separate coarse quantisation is required to find out in which subrange the input signal is located. Because there are eight subranges the coarse quantisation requires 3-bit or 7 comparators. The number of comparators of the folding A/D converter brings it back from 255 to 38 comparators. The folding structure is different from the two-step principle in that it performs the conversion of the input signal into fine and coarse quantisation in the *analog* domain. This makes it possible to operate the ADC without S/H circuit.

If the frequency of the input signal is increased, the edges of the folding signal will tend to round off, because the bandwidth of the folding circuit is limited. The edges contain the highest frequency components (figure 3.3).

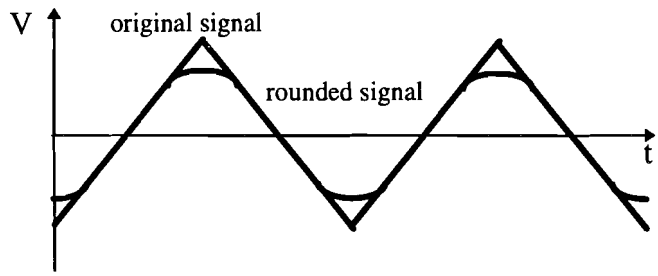


Figure 3.3 : High frequency rounding of the folding signal

This problem of frequency rounding can be avoided by using two folding signals with a 90°-degree phase shift. If one signal is near the edge, the other signal will be around a zero crossing which is his most accurate region. This double folding technique is shown in figure 3.4. The information around the tops can be discarded. For any input signal, one of the two folding signals will be in its linear region.

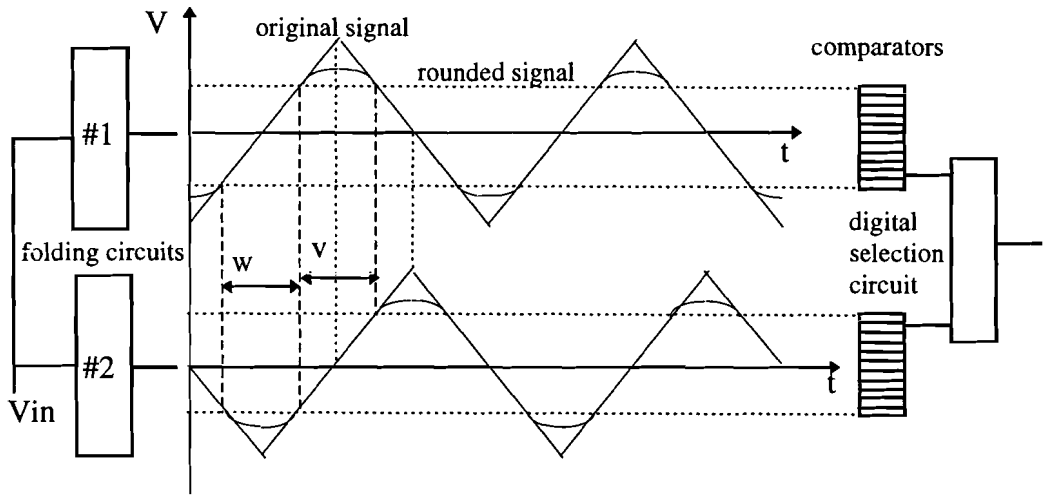


Figure 3.4 : Double folding technique for the fine selection

For still higher frequencies, even the double folding technique may not be sufficient. By increasing the number of folding circuits, only a decreasing part (W from folding signal #1 cq. V from folding signal #2 in figure 3.4) of the folded signal around zero is used. Although folding saves a lot of comparators, extra circuitry is used to perform the folding operations. The use of folding techniques is only attractive if the die size of the ADC is smaller than the flash-ADC. Fortunately, it is possible to make small size folding circuits. With the folding technique the input signal frequency is multiplied by the number of foldings. So the bandwidth of the preprocessing circuit ($B = f_{max} * \#foldings$) is the limiting factor for high frequency input signals.

It is important to see, that the sensitivity for rounding the triangular waveform at high frequencies can be avoided by not quantizing the waveform in amplitude, but quantizing it in the *zerocrossings*. In a differential folding signal, the only information to be gathered is whether it is positive or negative. So, only the zerocrossings in the folding signals are important. Zerocrossings are not affected by the bandwidth of the preprocessing part, so each zerocrossing can represent an input reference level.

By transforming each input reference level into a zerocrossing, the area, input capacitance and power consumption of the ADC would be the same as a flash ADC. By interpolating between two folding signals extra zerocrossings can be defined without folding circuitry. This interpolation is implemented by a resistor network. Moreover the interpolation method will be discussed in the following chapter. At first shall be described how the folding structure of the designed ADC will be implemented.

3.2 FOLDING PRINCIPLE USED IN LOW-POWER A / D CONVERTER

As stated before, the actual shape of the folding signal is not important anymore. As long as a folding signal is not affected around the region of the zerocrossing the performance of the ADC will not be influenced. For an 8 bit resolution, the next partitions can be made between the fine and coarse folding circuits. In table 2 an overview of the possible partitions is depicted.

Table 2 : Partitions between the fine - and the coarse part

k -bit coarse	(n-k)-bit fine	# comparators	folding factor
1	7	$128_{fine}+2_{coarse}$	1
2	6	$64_{fine} + 4_{coarse}$	4
3	5	$32_{fine} + 8_{coarse}$	8
4	4	$16_{fine} + 16_{coarse}$	16
5	3	$8_{fine} + 32_{coarse}$	32
6	2	$4_{fine} + 64_{coarse}$	64
7	1	$2_{fine} + 128_{coarse}$	128

When all the characteristics as power consumption, chip area and bandwidth of the subcircuits are defined the best partition can be made. These characteristic are not available at the beginning of the design, but it can be stated that a partition of 128 times folding will not gain the best partition. This configuration leads to very high internal frequencies (128 * maximum input frequency) which is very difficult to design for the specifications given. Also a partition of 2 times folding will not give the best balance between power and die area of the total ADC. Practical solutions of the partition will be in 4,8 or 16 times folding.

In the process, where the ADC is designed in, it should be possible to fold the input signal 8 times. Chapter 5 makes clear that with a folding rate of eight the bandwidth required for the preprocessing part is available in the implemented process. This will result as denoted in table 2, in a partition of 3-bit coarse and 5-bit fine quantisation. This partition shall be worked out during this design. The number of comparators (NC) in the fine folding part can be directly derived from the folding rate (FR): $NC_{fine} = 2^n / FR$.

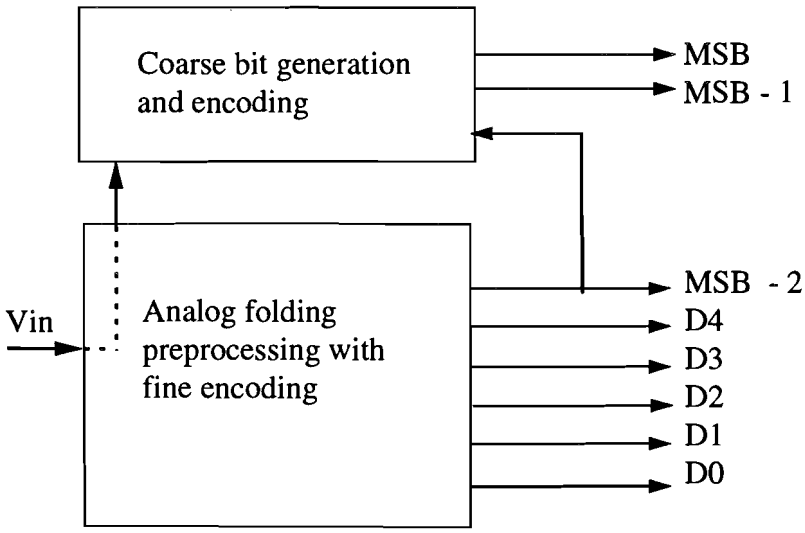


Figure 3.5: Generation of the 3 coarse bits and 5 fine bits in folding architecture

One folding signal contains 2^3 zerocrossings. With a number of 2^5 folding signals 8 x 32 = 256 zerocrossings are incorporated, resulting in an eight bit resolution. Actually, the folding signal incorporates nine zerocrossings in the preprocessing design. This is a result that the

first folding signal both marks the minimum input signal and the maximum input signal! Consider figure 3.6 in this case:

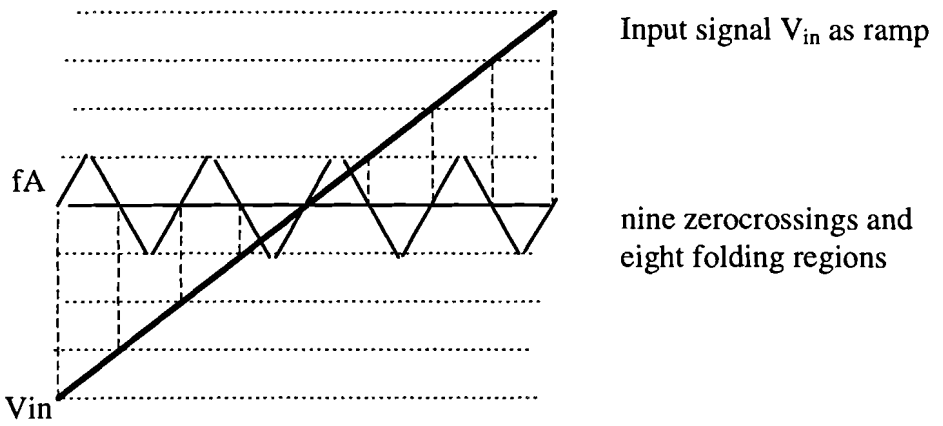


Figure 3.6: Nine zerocrossings in 'fA' due to marking both min. and max. input signal

Extra circuitry shall be added for signaling overflow and underflow of the input signal and synchronization of the coarse - part with the fine folding part. A 9 times folding signal can be generated by making use of nine differential pairs with the collectors of the even and odd differential pairs cross coupled and connected to two identical load resistors, and whose inputs are connected to appropriately defined reference voltage levels [9,14] (see figure. 3.7). A disadvantage of this approach is that the output capacitance (nine base-collector capacitance for one single output) of the nine folding block will be to large. The bandwidth of the folding block is limited too much by this approach. Implementing 9 folding blocks consisting 9 differential pairs will put also a restrain on the matching of the folding blocks. The input gain amplifiers, coupled on the one side to the reference voltage and on the other side to the input signal transforms the input signal into 36 'one' folding signals. Moreover, these input gain stages will be explained in the chapter 6. Another preprocessing implementation shall be used in this design, namely ***Cascaded folding***.

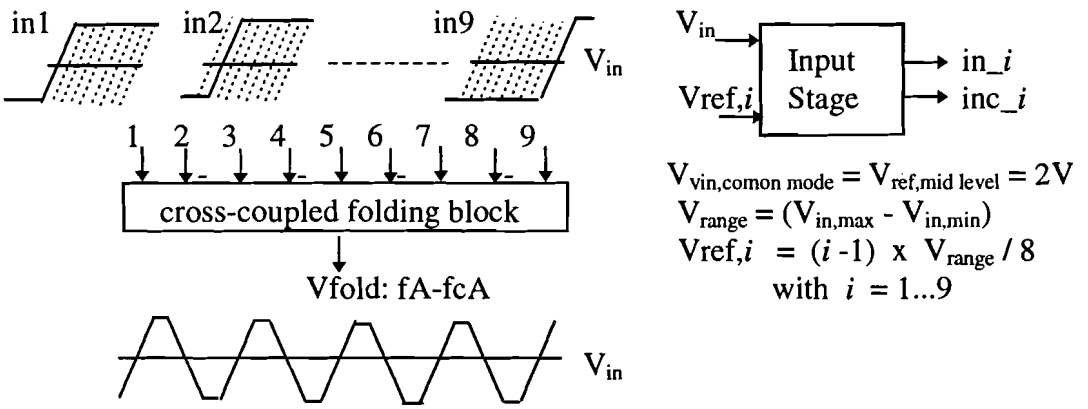


Figure 3.7 : Combination of input signals *in1* to *in9* into a single nine folding signal

A nine folding block composed of nine cross-coupled differential pairs can be split up into 3 times 3 folding blocks of each three cross-coupled differential pairs [23](see figure 3.8). The

output signals of the input gain blocks are now folded three times and for the combination of the three folding signals another three times folding block should be used (from now on called three folding combination block). This split up relaxes the restrains of transistor matching in the three folding block.

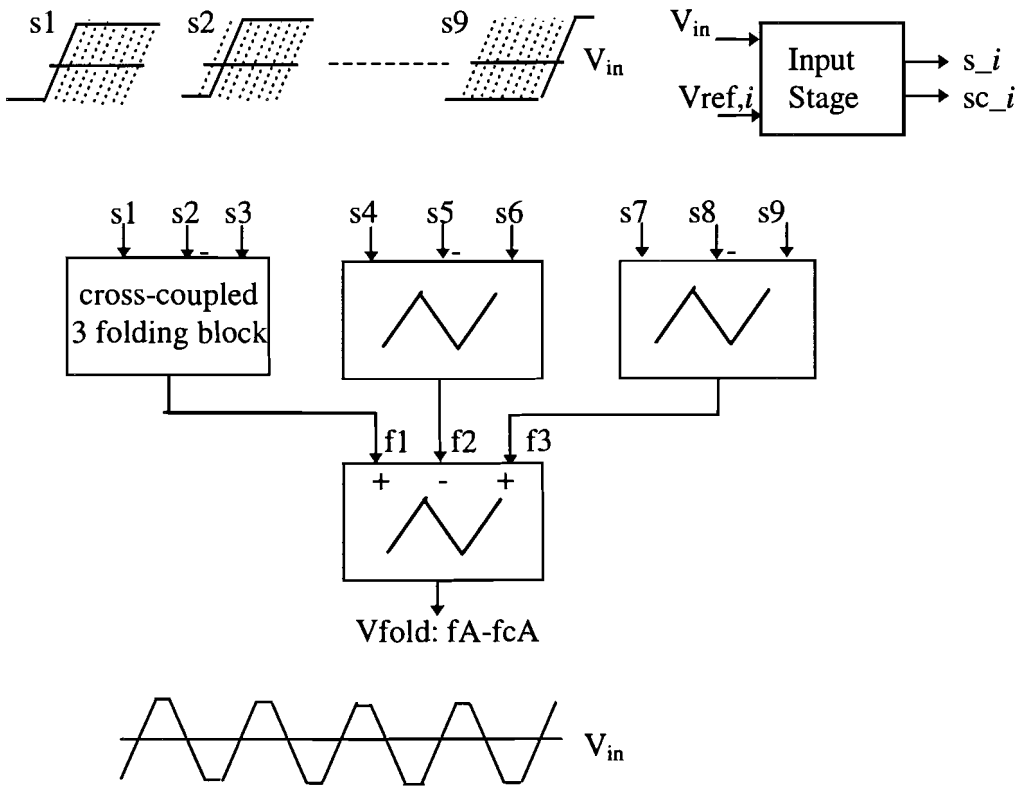


Figure 3.8: Cascaded folding of the input signals *s1* to *s9* into a nine folding signal

In an actually implementation, the shape of the nine folding signal is as a 'sine' wave. But as stated before, the shape of the folding signal does not matter. The information is contained in the position of the zerocrossing!

3.3 FINE FOLDING SIGNAL GENERATION

The implementation of the folding blocks is discussed for the generating the fine folding signals. From the nine times folding signal five 'fine' bits should be generated. Due to this 32 folding signals should be generated within the fine folding circuit. These 32 folding signals can be made by 4 nine folding signals (fA,fB,fC,fD) with between each two folding signals an 8 times interpolation. The number of interpolations (ipf) multiplied by the number of folding signals must be equal to 32 folding signals. The 4 nine folding signals are generated parallel by four identically blocks. When using 4 nine times folding signals at least 36 reference voltage levels (N_{ref}) should be needed for the definition of the quantisation levels. The zerocrossings of the folding signal fB is shifted along the V_{in} -axes $-1/32*V_{range}$

with respect to the fA zerocrossings. Generation of the fC zero crossings have been shifted -2/32*V_{range} and fD zerocrossings -3/32*V_{range}.
The generation of the missing 28 folding signals will be performed by resistive interpolation. Moreover, this interpolation is discussed in the next chapter. A schematic overview of the generation of the fine folding signals with the *cascaded folding principle* is given in figure 3.9. The 36 reference voltages are generated by a ladder of 36 resistors. The top level of the ladder is connected to $V_{ref,max}$ and the minimum level is connected to $V_{ref,min}$.

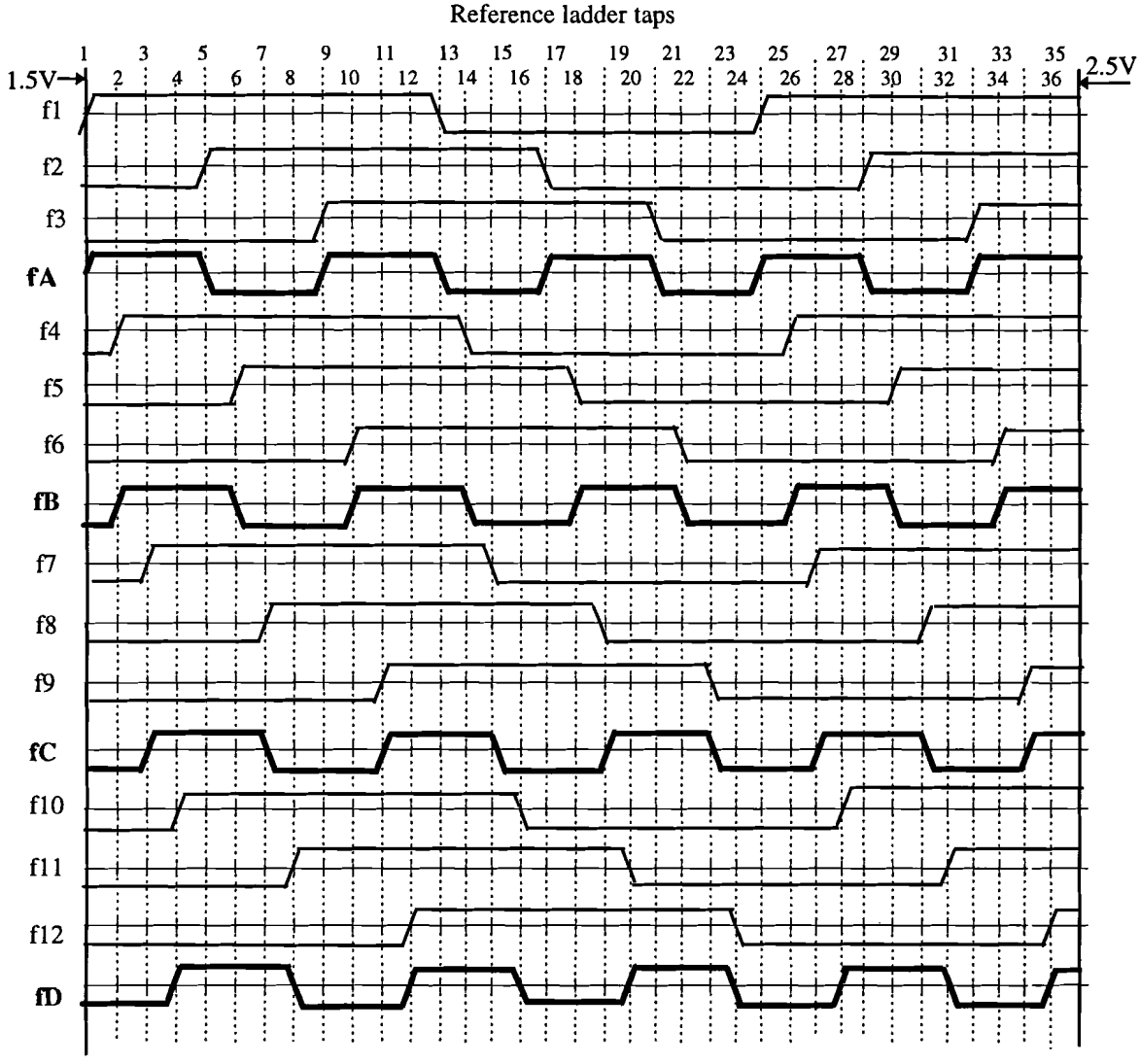


Figure 3.9 : Overview of the '3' - and '9' folding signals as function of the input voltage

In appendix A an other '3' folding implementation is shown. This technique has the only advantage of the short routing between the three folding block to the three folding combination block. The three folding method, as discussed above, gives a better spreading of the '3' folding signal over the input range. The voltage distance between the three 'one' folding signals in the three folding block is less: (4/36V) instead of 12/36V in the principle used above in figure 3.9. At high frequency operation of the ADC, the slope of the folding signals is smaller. When the distance between the zerocrossings is small, the folding signal does not reaches his output swing as in total saturation.

3.4 INTERPOLATING PRINCIPLE USED IN LOW-POWER A/D CONVERTER

As stated before, the generation of the missing 28 folding signals should be generated by interpolation. Interpolation is a convenient way to generate the missing folding signals. Interpolation can be performed with a few different methods [11,12,13,18]:

- current interpolation
- voltage interpolation

The method current interpolation, is not compatible with the low power specification of the ADC. Voltage interpolation is the most popular way for interpolation in bipolar technologies. It does not results in additional power dissipation and it occupies a relative small die area on the chip.

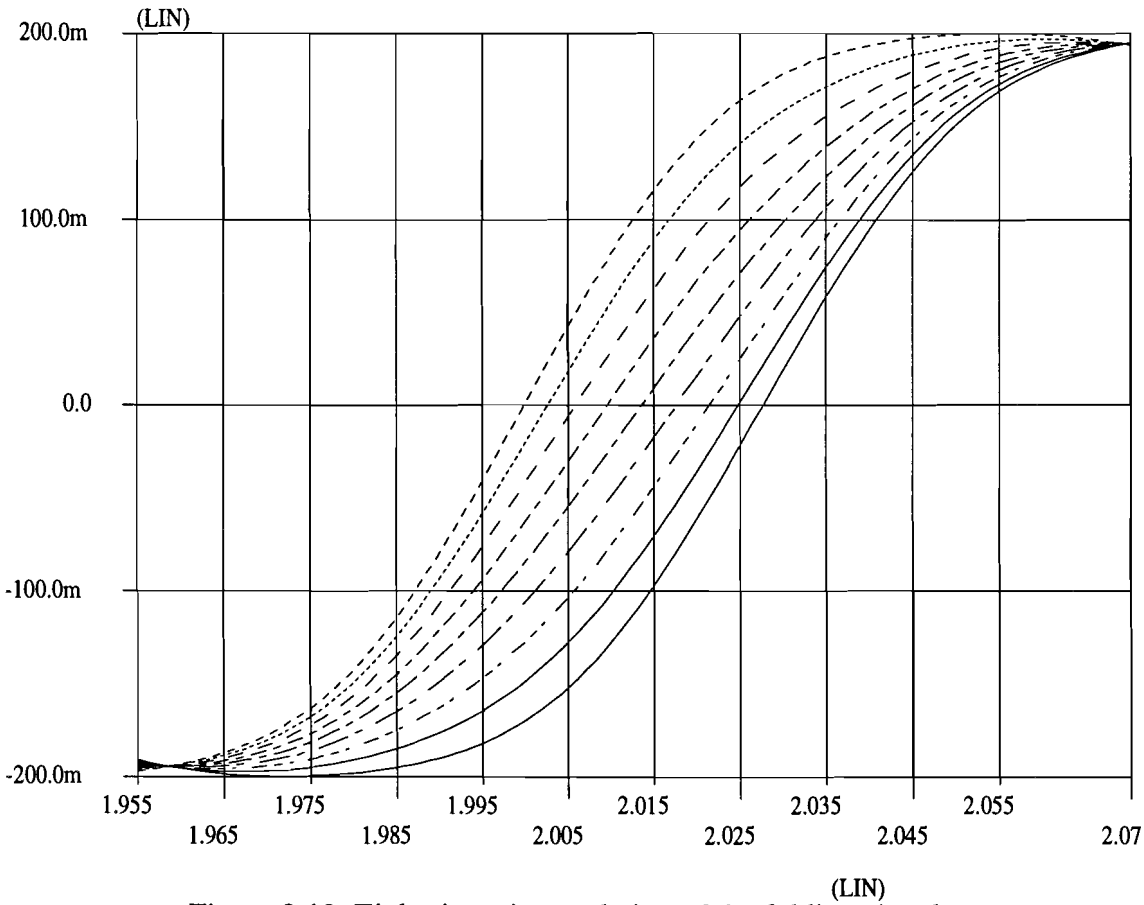


Figure 3.10: Eight times interpolation of the folding signals

The output voltages of two neighboring nine folding signals are applied to a resistive network of eight resistors. This network performs a resistive division and generates the signals equivalent to the nine folding signals. In figure 3.10 a division by eight is implemented. With the interpolation circuit the seven extra folding signals are generated. Between the four non-interpolated folding signals the missing 28 signals are generated and forms a total of 32 folding signals. Other practical realizations of voltage interpolation circuits have been published in [9,12,13]. As depicted in figure 3.10, interpolation will fail in the tops of the folding signals, but the shape of the tops of the interpolated folding signals does not affect the performance of the ADC. Nonlinearities in the folding signals causes

shifts in the zerocrossings of the interpolated signals with respect to the desired equidistant zerocrossings. Therefore, this phenomenon is discussed in the next chapters as the INL (Integral Non Linearity) of the folding circuit.
Because of the symmetry of the folding encoder outputs, the interpolation circuit has a circular symmetry. This means that each folding signal has two neighboring folding signals. Care has been taken to compensate of the delay difference introduced by the different output impedance's of the taps of the interpolation circuit. The form of the implemented interpolation circuit is depicted in figure 3.11.

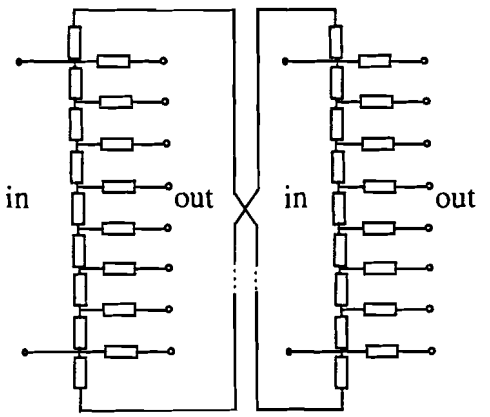
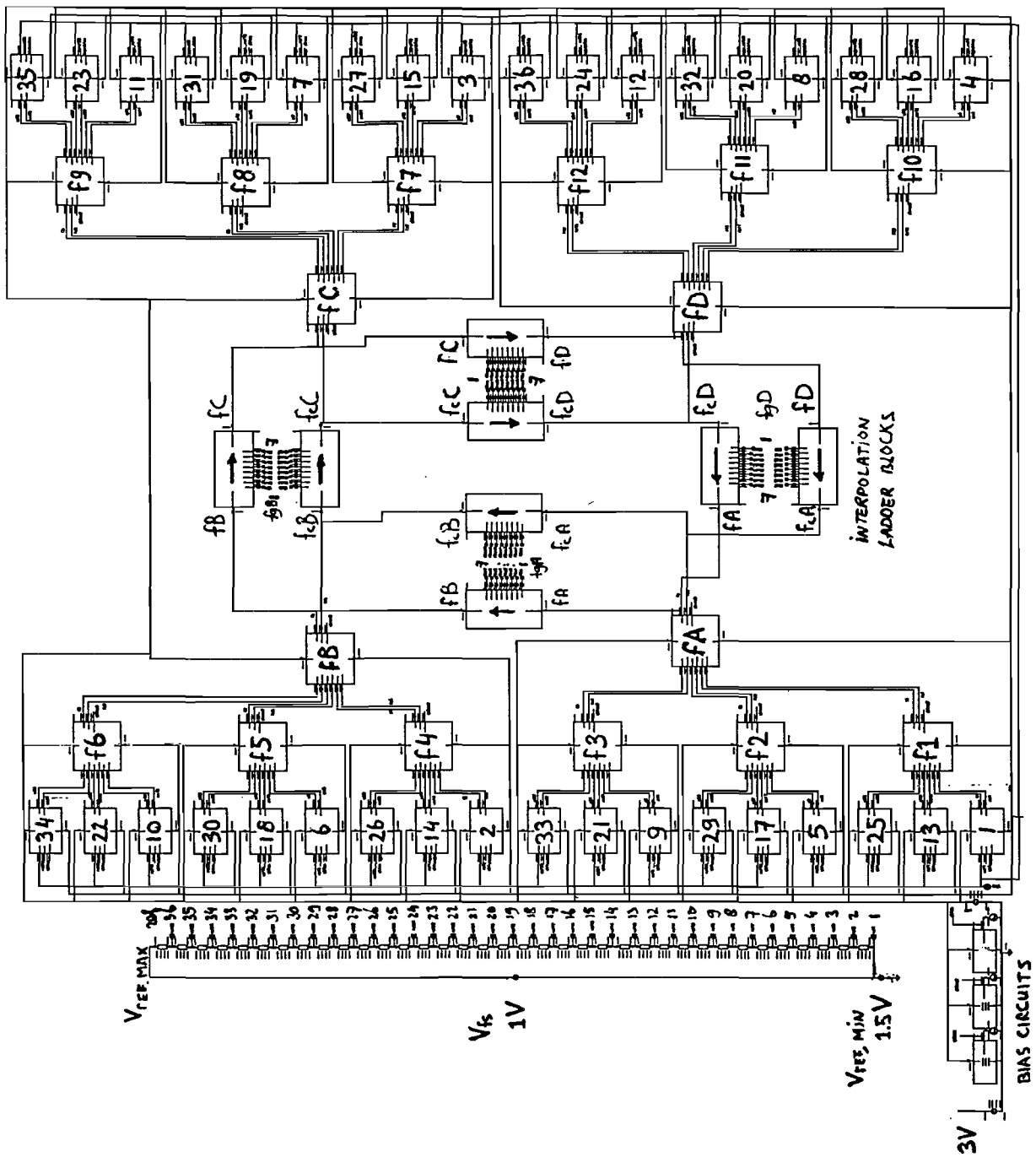


Figure 3.11 : Circular interpolation circuit

The zerocrossings of the 32 folded signals, coming out of the interpolation circuit, are detected by 32 comparators. These comparators are of the master/slave type to increase their sensitivity. The folding signals are made 'digital' in the slave comparator. With the 32-bit circular code the actually fine bits are generated.

3.5 OVERVIEW OF THE USED PREPROCESSING TECHNIQUE

This section deals with the total fine signal processing part in block diagram of the ADC. The generation of the folding signals, discussed in the previous chapter, is given in a schematic overview of folding block with the input gain stage connected to the folding blocks. In this figure the circular symmetry of the interpolation structure is seen. The symbols of the biasing circuits, discussed later, also are depicted in figure 3.12.



reference ladder taps: ref1 to ref36
input gain stages: 1 to 36
three folding blocks: f1 to f12
three folding combination blocks: fA to fD
output signals interpolation ladder: f9., f9.1 to f9.7 with . = A, B, C, D

Figure 3.12: Overview cascaded fine folding principle in preprocessing part

4. BLOCK DIAGRAM FOLDING A / D CONVERTER

A short explanation of the rest of the ADC after the analog signal processing part is discussed in this chapter. The structure of the total folding A/D converter is depicted in figure 4.1. The preprocessing part consists of the input gain stages with reference ladder, cascaded fine folding circuits with interpolation ladder and coarse folding part. The digital transformation of the analog folding signals converter begins with the comparators. From the 32 fine folding signals a circular thermometer-like output code will be generated.

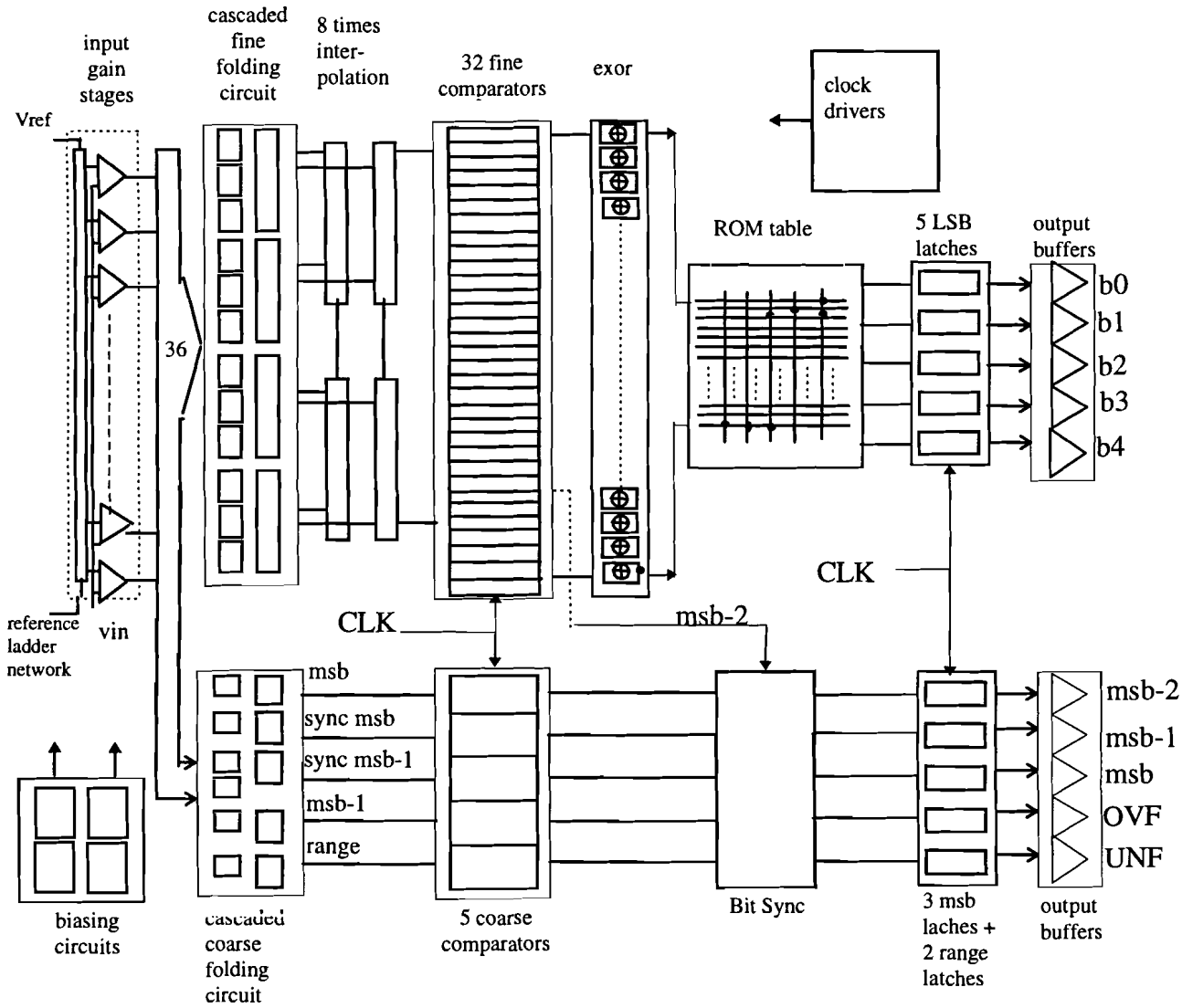


Figure 4.1 : Structure of the folding Analog-to-Digital Converter

In the comparators, an error correction circuit is built in to ensure that their outputs are consistent which each order [4,23]. The first encoding step is the isolation of the 0 to 1 transition in the circular 32 bit code. This is performed by the application of an EXOR operation directly behind the comparators (see figure 4.2).

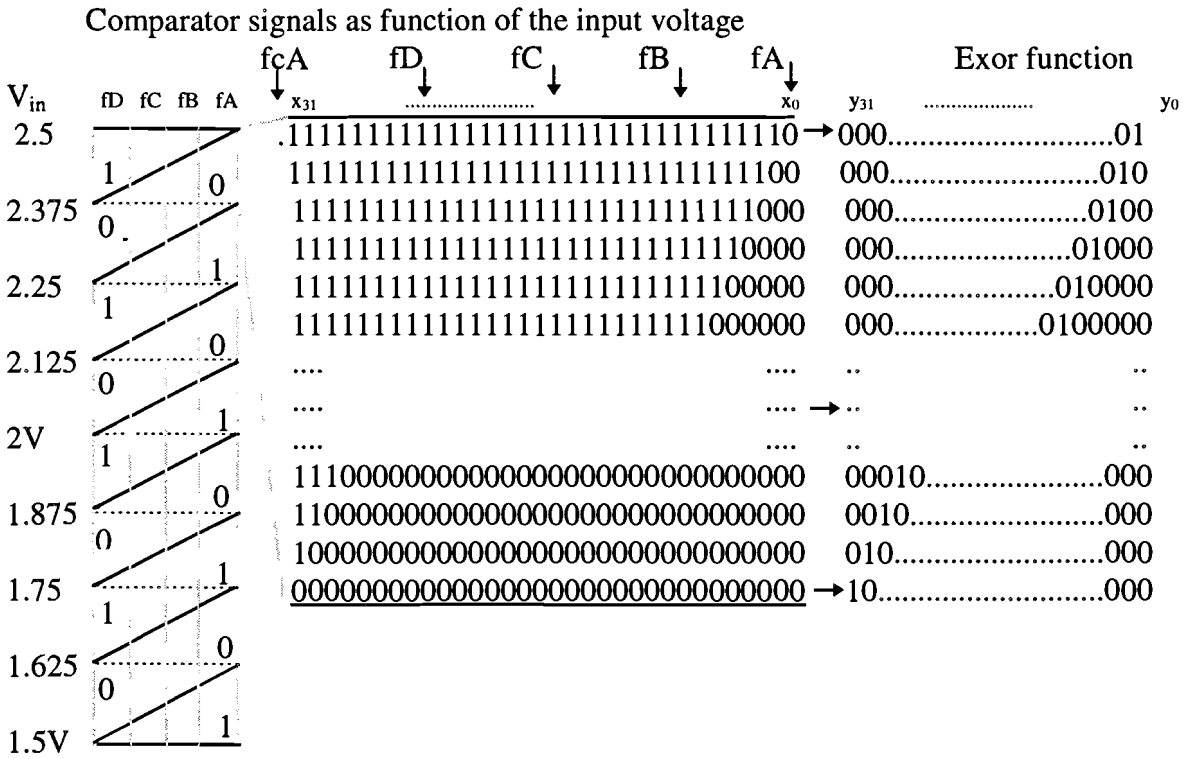


Figure 4.2: Output code comparators including EXOR-operation

The output code of the EXOR-operation (figure 4.3) is a so called *one high* code. This type of code can easily be decoded into a five bit binary code. A ROM structure for encoding is used. The functions implemented in the ROM table can be derived. For example the function for the LSB bit is: $D_0 = \sum_{i=1}^{16} y_{2i-1}$, this summation means a normally digital OR function. The other functions for the fine bits can also be derived from table 3.

Table 3: 5-bit Fine Encoder

Fine comp. levels	*EXOR code yi*	*Binary code*
0	-	0 0 0 0 0
1	y_1	0 0 0 0 1
2	y_2	0 0 0 1 0
3	y_3	0 0 0 1 1
4	y_4	0 0 1 0 0
..	..	..
..	..	..
28	y_{28}	1 1 1 0 0
29	y_{29}	1 1 1 0 1
30	y_{30}	1 1 1 1 0
31	y_{31}	1 1 1 1 1

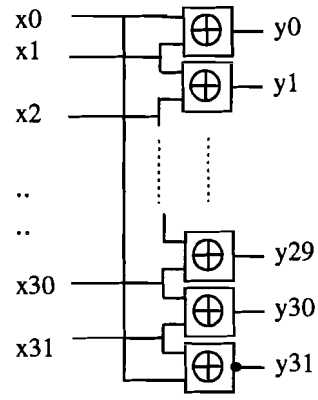


Figure 4.3: Exor function

The generation of the coarse signals will be discussed in chapter 8. These signals cannot be generated by a flash A/D converter because there is a delay in the preprocessing block. The coarse folding signals should be derived from the fine folding signals. There is one of the four non interpolated fine folding signals which is equal to the MSB-2 bit. From this MSB-2 signal, the other coarse bits can be generated and synchronized. Digital logic should extracts and synchronizes the desired coarse bits in the Bitsync block. Signals for overflow (OVL) or underflow (UVL) are also generated by this block. Overflow forces all outputs to logical "1", and underflow forces all the outputs to logical "0". What remains of the ADC are auxiliary circuits: clock drivers, bandgap reference circuits, output latches and output buffers. The bandgap reference circuits will be discussed in chapter 9. All the other remaining circuits shall be discussed in the master thesis of Roland van Wegberg.

To conclude the discussed block diagram of the ADC some remarks can be summarized:

- Analog preprocessing in the folding and interpolation A/D architecture reduces the number of comparators significantly compared to flash converter architectures. The architecture presented in this thesis needs 32 comparators for the fine encoding and 5 comparators for the coarse encoding. This reduction of comparators is also a reduction in power dissipation and chip area.
- By incorporating the folding technique there also is a noise reduction. The noise generated in the digital part of the ADC is less, because less encoding circuitry is required in this type of converter.
- The bandwidth of the circuit depends on the folding factor, input frequency and the maximum allowable distortion components (mostly third-order components). Therefore, the relation bandwidth/input frequency of the system is discussed in chapter 6.
- The eight times interpolation circuit is an easy way to generate the missing folding signals at the costs of relative small die area and power consumption.

The preprocessing part and the generation of the coarse folding signals on transistor level are discussed in the chapter 6,7 and 8. In chapter 5 the implementation of the architecture into bipolar transistor logic is discussed.

5. BIPOLAR TECHNOLOGY : SPIRIT

5.1 INTRODUCTION

The A/D converter will be implemented in the SPIRIT process. SPIRIT is an advanced new bipolar process developed by Philips Research. In this new process low power circuits can be realised due to the small process parasitics. There is no coupling between substrate and the active region. In the ADC design there is only made use of vertical integrated NPN transistors. Normally, for low power designs CMOS circuits are used. The advantage of CMOS technology over bipolar is that the A/D converter can be integrated on the same die as the digital signal processing part. This new technology however, has very small parasitic capacitance and is developed especially for RF circuits. During the assignment the parameters of the bipolar transistors has changed several times. At this moment, the process is not clearly defined, which is a great disadvantage of this process. The transistor parameter settings of the IC process Lab. in Hamburg has been taken for the final realisation of the A/D converter. These parameter settings are worse than the parameter settings from the process at the Nat.Lab. The geometry of the 'Hamburg' transistor is much larger, so the junction capacitance and the maximum f_t is higher than was assumed first. In the beginning of the assignment, the maximum power dissipation of the total A/D converter was set on 6-9mW. With the transistors of the NatLab, this could be possible with a few additional mWatts. With the 'HamburgLab' parameters the specification of 6-9mW is not realistic anymore. In the design specifications, the power dissipation should be a factor 3 to 4 times higher (about 25-30mW), for a realistic specification with the same full-scale analog input signal bandwidth.

5.2 RESISTORS

There are three types of resistors used in the ADC. A summarize of the resistors with sheetresistance and sort of material is given below:

1. Epi resistors: sheetresistance of 20kΩ/square
This is a high resistivity resistor made in mono crystalline silicon.

2. "PSS" resistors: sheetresistance of 115Ω/square
A medium resistivity resistor made in the emitter poly-silicon layer.

3. "BN" resistor: sheetresistance of 22Ω/square
A low resistivity resistor made from the collector contact layer. This layer is used as local interconnect layer. Due to the one metal layer technology there are no crossings possible. Crossings are made with these resistors. Also the reference ladder is implemented with this

type of resistor. The "BN" resistor has better matching properties than the medium ohmic "PSS" resistor.

5.3 NPN TRANSISTORS

The type of transistor used in the preprocessing part is the vertical N10L24PM transistor. This type is derived from the earlier 'D-25' NatLab. transistor. A full parameter list of transistor N10L24PM is given in appendix B. The most important design parameters are summarized and listed in table 4.

Table 4: Important design parameters of NPN TYPE: 'N10L24PM'

```
IS      = 1.6000E-18; collector emitter saturation current,
BF      =   356.9000; ideal forward current gain,
QBO     = 6.5100E-15; base charge at zero bias,
RCC     =    66.6500; constant part of the collector resistance,
RCV     = 5.4880E+03; resistance of the unmodulated epilayer,
RBC     = 1.1120E+03; constant part of the base resistance,
RBV     = 3.3333E+03; variable part of base resistance at zero bias,
RE      =   444.5000; emitter serie resistance,
CJE     = 1.2400E-15; zero bias emitter-base depletion capacitance,
XCJE    =     0.0000; fraction CJE that belongs to the side wall,
CJC     = 3.2500E-16; zero bias collector-base depletion capacitance,
XCJC    =     0.2040; fraction CJC under the emitter area,
Additional parasitics in the transistor model:
CBC     = 2.0200E-16,     CBE     = 1.3000E-15,     CBG     = 1.0700E-15,
CCE     = 4.8700E-16,     CCG     = 4.7000E-16,     CEG     = 5.6000E-16;
```

These PSTAR parameters are used in the level 503 bipolar NPN transistor TNS model. The model with parasitic capacitors is depicted in figure 5.1a.

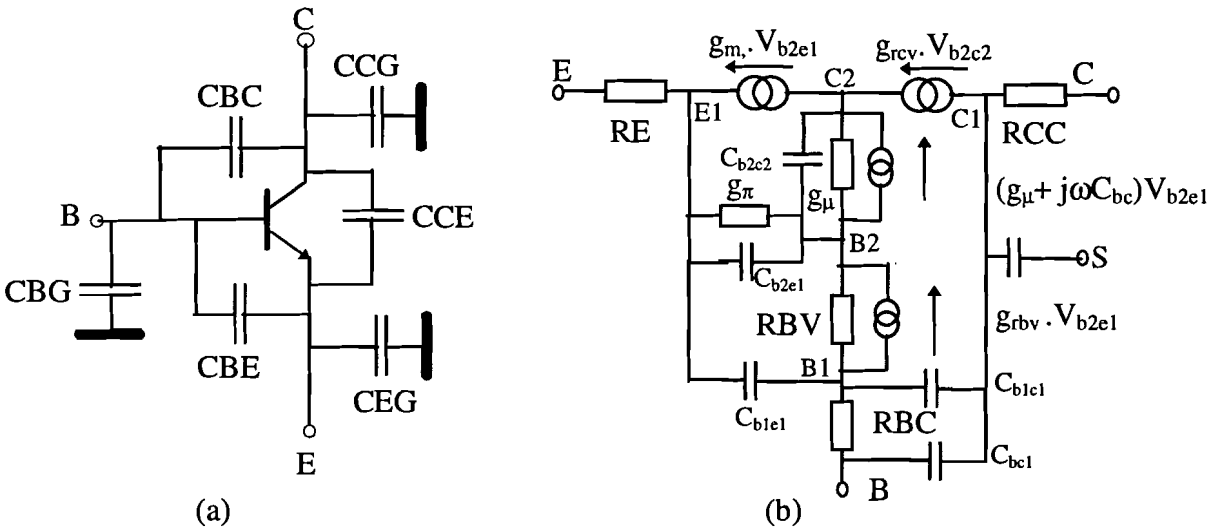


Figure 5.1: (a) NPN transistor with additional parasitic capacitors
(b) Simplified small signal equivalent circuit for vertical NPN transistor

The small signal AC model is simplified represented in figure 5.1b. The values of the capacitors in the small signal model are defined as follows:

C_{b1c1} =(1 - XEXT)*(1 - XCJC)*CJC= 2.46E-16 F (XEXT = 0.05 , see appendix B)
C_{bc1} = XEXT*(1 - XCJC)*CJC = 1.29E-17 F

C_{b1e1} = XCJE*CJE	=	0.00	F
C_{b2e1} = (1 - XCJE)*CJE	=	9.87E-16	F
C_{b2c2} = XCJC*CJC	=	6.63E-17	F
C_{js}	=	0.00	F (no coupling between the substrate!!)

The base-emitter capacitance is the sum of the junction and diffusion capacitance and is supply dependent. The dependent current sources g_m*V_{b2e1}, is the collector current in the transistor which is controlled by the internal base-emitter voltage. The parameter g_m is called the transconductance of the transistor; $g_m = Ic / V_T = q*Ic / kT$ only when $V_{be} >> V_T$.
It is directly proportional to the current itself. The input conductance g_π is derived from the large signal Ebers-Moll equations: $g_\pi = 1/r_\pi = g_m / \beta_F$.
Now some parameters of the transistor are calculated needed in the design of the circuits:
The effective base resistance near peak f_T: $R_b = RBC + \frac{RBC}{1 + \frac{V_{de}\, C_{je}}{QBO}} \approx 4333\ \Omega$
according the PSTAR parameters. The base-emitter diffusion capacitance can be calculated with: $C_d = \frac{g_m}{2\pi f_T}$. The extrinsic input bandwidth f_V as function of the bias current is shown in figure 5.2 and can be written as: $f_V = \frac{1}{2\pi R_b \left(2C_{jc} + C_{je} + C_d\right)}$.
Also an important characteristic for the design of high speed low power circuits is the cut-off frequency as function of the collector current (see figure 5.2).

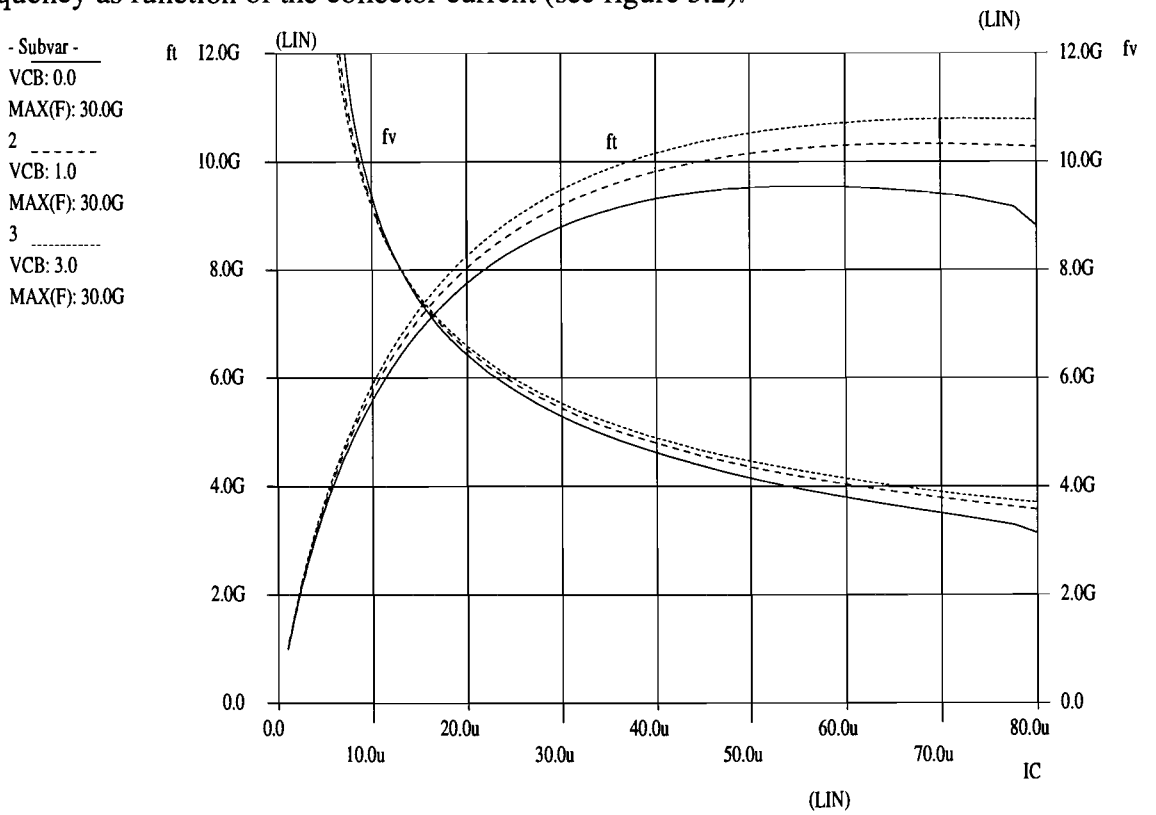


Figure 5.2: f_T and f_V as function of I_c: transistor N10L24PM

In the following chapters, the design of the preprocessing part on transistor level is discussed. In all the circuits, the used transistors are implemented as transistor N10L24PM.

6. REFERENCE LADDER WITH INPUT GAIN STAGES

6.1 INTRODUCTION

Differential pairs are perhaps the most widely used two-transistor sub-circuits in the monolithic analog circuits. The usefulness of this circuit comes from the fact that the emitter coupled pairs can be directly coupled to one another without interstage of coupling capacitors. In this chapter, the function of the differential pair in the folding A/D is discussed. The dc and frequency properties will be considered of the simplest circuit, a common-emitter amplifier. Because of the low power dissipation of the ADC the input gain stages are implemented as simple as possible. So, no emitter followers are used, where possible, and the tail current is kept as low as possible. The biasing circuit is implemented as a current mirror and the amplifier is restively loaded. One side of the differential pair is coupled to one tap of the resistor reference ladder. The reference ladder consisting of 36 resistors forms the quantisation levels for the input signal. Also the influence of the performance of the input gain stages will be analysed with respect to the reference ladder in this chapter. An input gain stage with a part of the reference ladder is given below in figure 6.1.

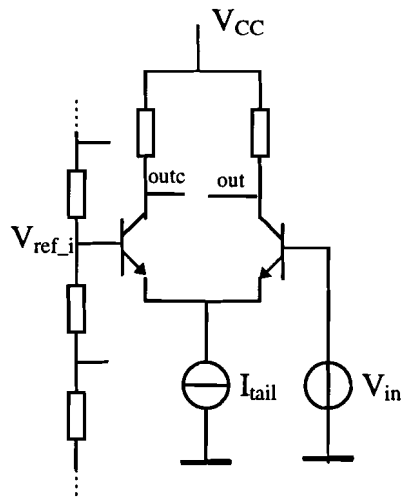


Figure 6.1 : Simple differential pair with reference ladder tap connection

First, the range of the input signal V_{in} will be discussed. For this moment assume that the V_{be} of the transistor is approximately 0.8V. The current source of the differential pair needs at least a minimum voltage on the common emitters of 0.6V. A minimum input voltage of 1.4V is proposed. The base collector diode in the current source transistor is now 200mV forwarded. For safe operation of the current source, the minimum input voltage is adjusted

to 1.5V. The circuits should operate at a power supply of V_{CC} = 3V. The maximum amplitude of the input signal is $1V_{pp}$. The range of the input signal lies between the ranges:

$$V_{ref,min} \leq V_{in} \leq V_{ref,high}$$
$$1.5V \leq V_{in} \leq 2.5V$$

6.2 BANDWIDTH VERSUS INPUT FREQUENCY RATIO OF THE ADC

In a folding ADC the amplitude of the input signal (V_{fs}) is much larger than the linear range of the input gain stages (V_{lr}). The input gain stages are overdriven by the input signal, and the zerocrossings at the output of the amplifier are delayed in time. The input signal is compared with 36 voltage reference levels. A zerocrossing occurs when the input signal equals the reference voltage level. The delay of the zerocrossing can simply be calculated by modeling the amplifier stage as an amplitude limiting circuit and a bandwidth (f_b) limiting circuit. The result of the normalized delay variation $g = \delta t_d/RC$ after simplification becomes [20,21]:

$g \approx e^{-2b_n \frac{V_{lr} \cdot f_b}{V_{fs} \cdot f_{in}} - 1}$,where b_n is the relative output voltage at which the signal delay is determined. In the situation of the ADC we have a value of $b_n = 0.5$. From this equation the following can be concluded for a minimum delay variation:

- The linear range V_{lr} of the input gain amplifier must be large
- A large amplifier bandwidth f_b
- A small full scale range V_{fs} of the converter

In the bipolar technology a linear range of the input gain stage of about 120 to 180mV can be obtained, depending of the gain and the amplitude of the output signal. The bandwidth of the system is mostly related to the dc bias conditions of the amplifier stages. A large bias current results in a large power dissipation, so there must be a compromise in choosing the bias current in relation with bandwidth. These results can be used in the distortion calculations in relation with the bandwidth/input frequency ratio. A good approximation (δt) of the delay difference δt_d as a function of the input frequency is :

$$\delta t = -\delta t_d \, |\cos \omega t \, |$$

This delay function is normalized for zero variations at the tops of the input signals.
The distortion can now be calculated by inserting this equation in the function:

$$V_{out} = \sin(\omega(t+\delta t)) = \sin(\omega t)\cos(\omega \delta t_d \, |\cos \omega t \, |) - \cos(\omega t)\sin(\omega \delta t_d \, |\cos \omega t \, |)$$

assume that $\delta t_d << t$ and $|\cos \omega t \, | \cong 2/\pi + 4/(3\pi)*\cos(2\,\omega t)$ results in:

$$V_{out} = \sin \omega t + 8/(3\pi)\,\omega \delta t_d \cos \omega t + 2/(3\pi)\,\omega \delta t_d \cos 3\omega t$$

From this equation it is shown that signal-dependent delay results in third harmonic distortion of the input signal after conversion takes place in a linear ADC.

For a third harmonic distortion of at least -50dB with a full scale input range of 1V the bandwidth/input frequency ratio should at least be 10 [20,21]. This results in a bandwidth of the preprocessing block of the folding A/D converter of minimal 500MHz. In this calculation other distortion products due to ladder non-linearity, comparator offset voltages and so on do not occur. The actual input range is smaller than 1V. Of the 36 reference levels are only 32 levels needed for an eight bit resolution. The input range becomes now 1V - 4/36V = 8/9V. The bandwidth/input frequency ratio of 10 is high enough for this input range.

6.3 INPUT GAIN STAGES

6.3.1 Standard implementation of a differential input amplifier

We assume that the base of the transistor is driven by a voltage source of value V_{in}. The large-signal behaviour of the differential pair is important because it illustrates the limited range of the input voltages over which the circuit behave linearly. For the simplicity the output resistance of the current source is infinity, and the base resistance of the transistor are neglected. These assumptions do not affect the large signal behaviour and the low frequency aspect of the circuit. In the bipolar differential pair of the A/D converter only the zerocrossing is important, so both transistors are conducting and not saturated. We first sum the voltages around the loop of the two voltage sources and the two base-emitter junctions:

$$V_{ref\_i} - V_{be1} + V_{be2} - V_{in} = 0$$

From the Ebers-Moll equations, assuming that $V_{be1}, V_{be2} >> V_T$ = kT/q, (Thermal voltage)

$$V_{be1} = V_T \ln \frac{I_{c1}}{I_{s1}}$$

$$V_{be2} = V_T \ln \frac{I_{c2}}{I_{s2}}$$

Combining these two relations and assuming that $I_{s1} = I_{s2}$, and $-(I_{e1} + I_{e2}) = 1/\alpha_F (I_{c1} + I_{c2})$ we will find :

$$\frac{I_{c1}}{I_{c2}} = e^{\left(\frac{V_{in}}{V_T}\right)}$$

$$V_{out\_dif} = V_{outc} - V_{out} = \alpha_F I_{bias} R_{load} \cdot tanh\left(\frac{V_{in} - V_{ref\_i}}{2 * V_T}\right)$$

The output voltage swing: $A_{tt} = 2 * A = 2* I_{bias}*R_{load}$.

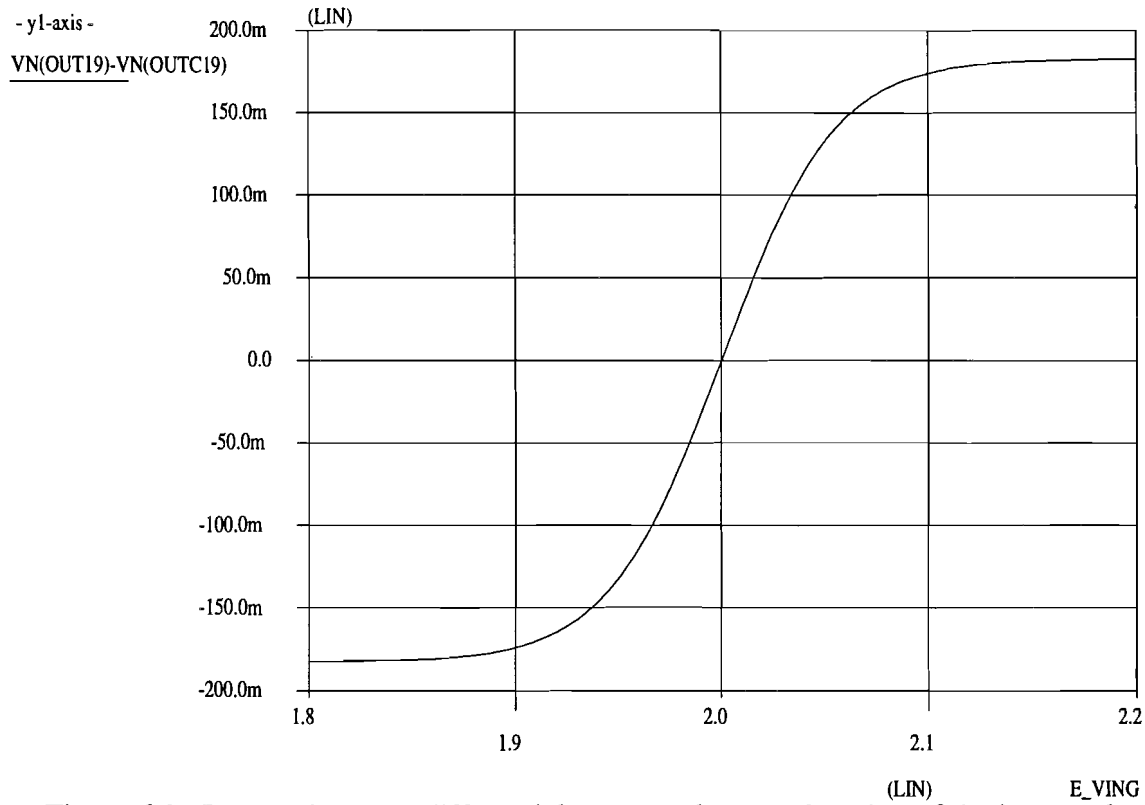


Figure 6.2 : Input gain stage, differential output voltage as function of the input voltage

This output voltage function is plotted in figure 6.2. Here, a significant advantage of the differential pair is apparent: When $V_{in} = V_{ref\_i}$ the output voltage is zero, which allows direct coupling of cascaded stages without introducing dc offsets.
Note that for input voltages of several hundred millivolts, the collector current Ic becomes independent if the input signal, since all current flow through one of the two transistors. Only for differential voltage less than approximately 50mV does the circuit behave like a linear circuit. In the folding A/D converter 36 input amplifiers are used, connected with the reference ladder and the input signal. The voltage step between two successive taps is 1 V / 36 ≈ 27.8mV, so the circuit behaves in linear fashion round V_{ref_i} . The gain of the input stage can be derived as follows; the differential mode gain A_{dm} , is the change in the differential output V_{out} per unit change in the differential input $V_{inp} = V_{ref\_i} - V_{in}$.

$$A_{dm} = \left.\frac{dV_{out}}{dV_{inp}}\right|_{V_{ref\_i} = V_{ing}} = \frac{I_{bias} * R_{load}}{2 * V_T} = g_m * R_{load}$$

The common mode gain A_{cm}, is the change in the common-mode output voltage $(V_{out}+V_{outc})/2$ per unit change in the common-mode input:

$$A_{cm} = \frac{g_m * R_{load}}{1 + 2 g_m R_o \left(1 + \frac{1}{\beta}\right)},$$

with R_o the output impedance of the current source for biasing the differential pair.

The current source can be a single bipolar transistor as depicted in figure 6.3.

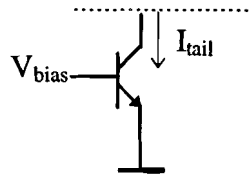


Figure 6.3 : Current source using a single transistor

With the approximation that $\alpha_F = 1$ and assuming $V_{bias} >> V_T$, the tail current follows out:

$$I_{tail} = I_s \, e^{\frac{V_{bias}}{V_T}}$$

A feature of the current source is the sensitivity for variations in V_{bias}. The sensitivity is defined as:

$$S_V = \frac{\partial I_{tail}}{\partial V_{bias}} = \frac{I_s}{V_T} e^{\frac{V_{bias}}{V_T}} = \frac{I_{tail}}{V_T} = g_m$$

The high sensitivity to voltage variations is a great disadvantage of this approach biasing a differential pair. The tail current must be as stable as possible. The sensitivity of the current source can be decreased by using an emitter resistor (see figure 6.4).

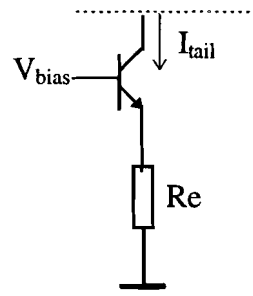


Figure 6.4 : Current source using a transistor with emitter resistor

Now the variation of the output current with the V_{bias} can be written as:

$$S_V = \frac{\partial I_{tail}}{\partial V_{bias}} = \frac{I_s}{V_T + Re \cdot I_{tail}} e^{\frac{V_{bias}}{V_T}} = \frac{I_{tail}}{V_T + Re \cdot I_{tail}} = \frac{g_m}{1 + Re \cdot g_m}$$

The output current variation of the current source is now decreased a factor 1 / (1+Re*g_m). The maximum voltage on the emitters of the input gain stage is 750mV. The V_{bias} cannot be chosen to high, because the maximum allowable forward voltage of the base-collector voltage is 200mV. For an insensitive current source to voltage variations, the voltage over

the emitter resistor Re must be approximately 200 - 300mV. The V_{bias} must be generated with additional circuits discussed in chapter 9.

One of the most important aspects of the current source performance is the variation of the current source with changes in the voltage at the output (common emitter point) terminal. This is characterised by the small-signal output resistance of the current source. The common mode rejection ratio depends directly on this resistance. Mostly it is assumed that the collector current is independent of their collector-emitter voltages. Actually, the collector current slowly increases with the increasing collector-emitter voltage, due to the base-width modulation effect. The output impedance of the current source can be defined as:

$$R_o = \frac{\partial V_c}{\partial I_{tail}} = ro\left(1+\frac{I_{tail}Re}{V_T}\right) \quad \text{, with ro} = V_{early}/I_{tail}$$

Thus, the R_o depends on $I_{tail}*R_e$, which is the dc voltage across R_e. A large R_o results in improvement of the common-mode-rejection-ratio (CMMR). For a conventional differential pair used as in the input gain stage, the CMMR can be defined as [22]:

$$CMMR = \frac{A_{dm}}{A_{cm}} = 1+2g_m R_o\left(1+\frac{1}{\beta}\right) \approx \frac{I_{tail}\cdot R_o}{V_T}$$

Because of the low power constraint, the use of emitter followers in each input gain stage is not useful. The advantage of emitter followers is the low output impedance for driving the wirering capacitive load and the dc-shift of 'one' Vbe. The total bias current through each input gain stage would be too high, so other possibilities should be investigated. Without emitter followers, problems occurs by coupling the input stage to the inputs of the three folding block. The minimum voltage at the bases of the three folding block is to high for direct coupling of the input gain stage with the three folding block. In order to establish the needed level shift in the differential pair, a resistor R_{cm} is used as shown in figure 6.5.

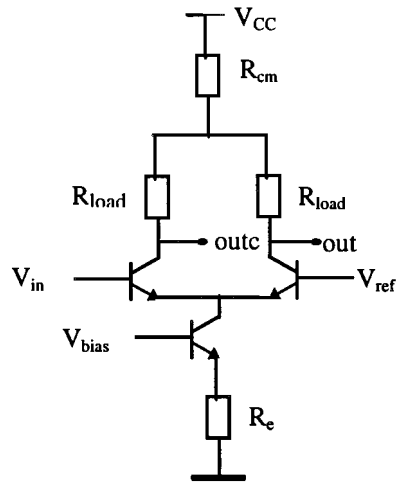


Figure 6.5: Levelshift in input gain stage with R_{cm}

For the finally dc settings will be referred to the chapter 6.6. First the ideal output swing, I_{bias} and gain should be extracted. These factors also depend on the AC behavior and the Integral Non Linearity (INL) of the converter.

In the dc behaviour described above, the effects of parasitic capacitance and charge storage in transistors were not considered. However, as the frequency of the signal being increased, the capacitive elements in the circuit eventually dominated the behaviour of the circuit. AC-analysis on the input gain stages and other fine folding circuits are performed in chapter 7.5.2.

6.4 REFERENCE LADDER NETWORK

6.4.1 Influence of noise on the ladder network

In a folding A/D converter the step size of the reference ladder is larger than in a flash converter. The reference levels are generated with a resister ladder network. Noise sources can result in inaccurate decisions of the comparator. The zerocrossing detoriates by influence of noise (1/f noise is not included). The maximum rms noise voltage for one side of the input of the differential pair can be calculated as follows:

$$e_{rms} = \sqrt{\left(4kT\left(R_{bb'} + \frac{1}{2g_m}\right)\Delta f\right)} = \sqrt{\left(4kT\left(4445 + \frac{25\cdot 10^{-3}}{8\cdot 10^{-6}}\right)500\cdot 10^{6}\right)} = 0.25mV$$

This formula includes the independent noise sources: thermal noise and shot noise. The base resistance Rbb' exists out a constant and a variable part. In the formula is assumed that the bandwidth is 500MHz and the bias 'tail' current through the differential pair 8uA. The base resistance according the MEXTRAM transistor model transformed to the HSPICE model in a transistor can be calculated as:

$$R_{bb'} = RBC + \frac{3RBV}{q1+q2} \approx RBC + RBV = 1112 + 3333 = 4445\Omega$$

These assumption is based on the translating of the Mextram models parameters to the Spice models for performing the analysis on a HSPICE circuit simulator.
The noise voltage of 0.25mV corresponds with an error of 0.072LSB and hence the noise plays no important role here.

6.4.2 Definition maximum ladder resistor value

The definition of the maximum ladder resistance comes from the fact that there is a capacitive coupling between the input signal and the reference ladder. The standard implementation discussed in chapter 6.3.1 is depicted with base-emitter capacitance in figure 6.6.

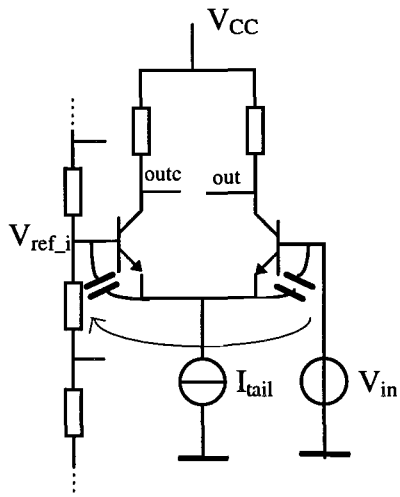


Figure 6.6 : Reference ladder feedthrough of input signal via series capacitive combination in the differential pairs of the input stages

These capacitive coupling detoriates the reference voltage V_{ref_i}. This voltage determines the position of the zero crossing and variation in this zerocrossing will result in distortion of the ADC. A simple model can be given [14] to calculate the maximum allowed reference ladder resistance. In figure 6.7 this model is shown. The maximum feedthrough will occur at the middle tap of the reference ladder.

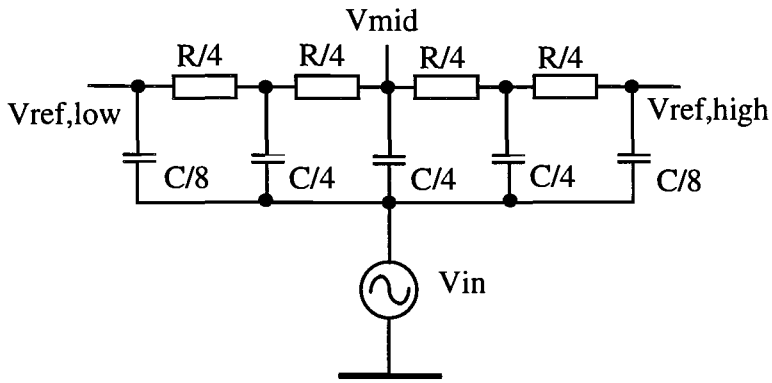


Figure 6.7 : Calculation model to derive the maximum feedthrough on the reference ladder

The total reference ladder resistance R is divided into four equal sections R/4, and the total coupling capacitance C of all the input stages has been divided into five capacitors. The model shown in figure 6.7 is symmetrical, so only one half of this model has to be used to calculate the feedthrough on the middle tap of the reference ladder. The transfer function V_{mid}/V_{in} is calculated in [14] with V_{in} the input voltage and f_{in} the input frequency given by:

$$\frac{V_{mid}}{V_{in}} = \frac{\alpha(\alpha+32)}{\alpha^2+32\alpha+128} \quad \text{, with } \alpha = \pi f_{in} RC.$$

When it is assumed that $\alpha << 1$ then the equation can be simplified to

$$\frac{V_{mid}}{V_{in}} = \frac{\pi}{4} f_{in} RC.$$

The maximum reference ladder resistance for a given feedthrough is now defined by:

$$R_{ladder,max} = \frac{4\frac{V_{mid}}{V_{in}}}{\pi f_{in} C} = \frac{4\theta}{\pi 2^n f_{in} C}.$$

In this equation θ represents the feedthrough in LSB and is n the resolution of the ADC in number of bits. The total coupling capacitance of one input gain stage consisting of two base-emitter capacitors and two parasitic process base-emitter capacitance in serie.

Simulation results show that for the DC operation point (Ibias = 8uA) the total base-emitter capacitance of one transistor is 4.78fF. Two of these capacitors in serie give a total coupling capacitance of approximately 2.4fF. Other parasitic capacitance are not included with this simulation result. For an 'exact' value of the total coupling capacitance a simulation is done by assuming the differential pair as a black box. The simulation setup is shown in figure 6.8.

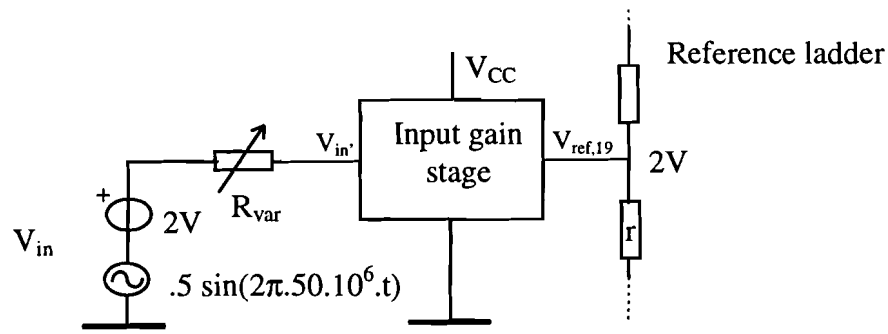


Figure 6.8: Simulation setup for measuring the coupling capacitance of one input gain stage

The input of the input gain stage is connected to a sine wave of 50MHz with amplitude of 500mV. The black box is in balance. With the variable resistor R_{var} , the input signal $v_{in'}$ is adjusted to exactly $½\sqrt{2}*V_{in}$ after a few periods. The resistor value where this $V_{in'}$ level is achieved is 1.6MΩ. The coupling capacitance can now be derived as follows:

$$C_{coupling} = \frac{1}{2\pi \cdot 50 \cdot 10^6 \cdot 1.6\,M\Omega} = 2\,fF$$

The total coupling capacitance for 36 input gain stages become:

$$36 * C_{coupling} = 72fF.$$

The maximum ladder resistor value becomes now:

$$R_{ladder,max} = \frac{4\theta}{\pi\, 2^n\, f_{in}\, C} = \frac{4}{\pi \cdot 256 \cdot 50 \cdot 10^6 \cdot 72 \cdot 10^{-15}} = 1440\Omega$$

$$r_{max} = \frac{1440}{36} = 40\Omega$$

$$P_{refladder,max} = 694\,\mu W$$

The power dissipation is calculated with a input range of 1V. It is possible to the reduce the feedthrough by external decoupling the middle tap of the ladder. A disadvantage of this external decoupling is the inductance of the bondwire, reducing the decoupling at higher frequencies.

6.5 NONLINEARITY OF THE INPUT STAGE

In this chapter, the influence of the nonlinearities of the input curves is discussed. A formula is derived for the position of the interpolated zerocrossings. The non-linear output curves causes the main part of the total Integral Non Linearity of the ADC.

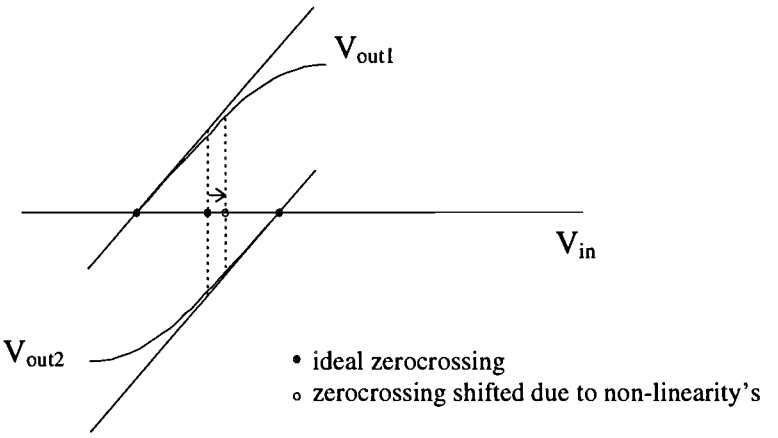


Figure 6.9: Interpolation errors due to nonlinearities of the input stage

The position of the interpolated zerocrossings is depended of the gain, the distance between two folding signals and the amplitude of the fine folding signals. A definition of the used symbols in the following derivation is depicted in figure 6.10. The nonlinear output curve of the input gain stage is defined as:

$$V_{out1} = \alpha_F\, I_{bias}\, R_{load} \cdot tanh\left(\frac{V_{in} - V_{ref\_1}}{2 * V_T}\right)$$

$$V_{out2} = \alpha_F\, I_{bias}\, R_{load} \cdot tanh\left(\frac{V_{in} - V_{ref\_2}}{2 * V_T}\right),$$

with $V_{ref,2}$ - $V_{ref,1}$ = c = (V_{range})/32 = (8/9)/32 = 1/36 V as the distance between two nine folding signals. The output swing is defined as $A=\alpha_F I_{bias} R_{load}$ and the gain b can be defined as: $b= g_m R_{load} = \frac{I_{bias}}{2V_T} R_{load} = \frac{I_c}{V_T} R_{load}$.

The non-linear output curves can be rewritten now to the function:

$$V_{out1} = A \cdot tanh\left(\frac{b \cdot x}{A}\right)$$

$$V_{out2} = A \cdot tanh\left(\frac{b \cdot (x-c)}{A}\right)$$

Interpolation occurs by taking the difference (in y-direction) between the two folding signals and divided this difference by eight. The interpolation signals between V_{out1} - V_{out2} can be defined as follows:

$$V_{int\_i} = V_{out1} - \frac{i}{8} \cdot \delta V_y = V_{out2} + \frac{8-i}{8} \cdot \delta V_y, \text{ with } i \in [1,7] \text{ (see figure 6.10)}$$

In the following section the voltage δV_y will be derived.

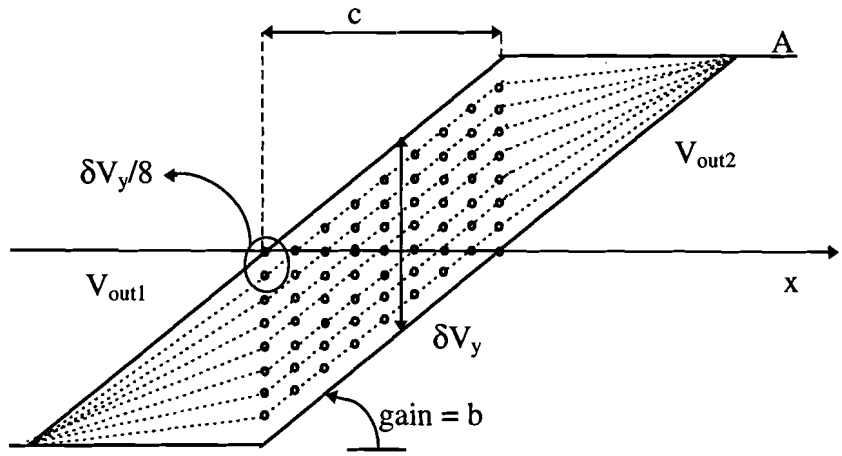


Figure 6.10: The 7 interpolation signals with linear transfer curve: V_{out1} - i*δV_y/8

The transfer curves in figure 6.10 are perfectly linear. The ideal interpolated zerocrossings are defined at the positions:

$$Vip_{ideal} = \frac{i}{256} * V_{range} \text{ , with } i \in [1 , 288] \text{ and } V_{range} = 8/9V.$$

The nonlinear curves of the input gain stages introduce errors in the interpolated zero crossings. The errors are depended of the gain and the output voltage swing of the folding signals. The voltage δV_y, for the non-linear output curves, can be calculated as follows:

$$\delta V_y = A \tanh\left(\frac{bx}{A}\right) - A \tanh\left(\frac{b(x-c)}{A}\right)$$

Rewriting this function into:

$$\delta V_y = A\left\{\left(\frac{e^{\frac{bx}{A}} - e^{-\frac{bx}{A}}}{e^{\frac{bx}{A}} + e^{-\frac{bx}{A}}}\right) - \left(\frac{e^{\frac{b(x-c)}{A}} - e^{-\frac{b(x-c)}{A}}}{e^{\frac{b(x-c)}{A}} + e^{-\frac{b(x-c)}{A}}}\right)\right\}$$

$$\delta V_y = A\left\{\frac{\left(e^{\frac{bx}{A}} - e^{-\frac{bx}{A}}\right)\cdot\left(e^{\frac{b(x-c)}{A}} + e^{-\frac{b(x-c)}{A}}\right) - \left(e^{\frac{bx}{A}} + e^{-\frac{bx}{A}}\right)\cdot\left(e^{\frac{b(x-c)}{A}} - e^{-\frac{b(x-c)}{A}}\right)}{\left(e^{\frac{bx}{A}} + e^{-\frac{bx}{A}}\right)\cdot\left(e^{\frac{b(x-c)}{A}} + e^{-\frac{b(x-c)}{A}}\right)}\right\}$$

and by taking $\frac{bx}{A} = z$ and $\frac{b(x-c)}{A} = z - w$,

the function δV_y can be further simplified to:

$$\delta V_y = A\left\{\frac{\left(e^{z} - e^{-z}\right)\cdot\left(e^{z-w} + e^{-(z-w)}\right) - \left(e^{z} + e^{-z}\right)\cdot\left(e^{z-w} - e^{-(z-w)}\right)}{\left(e^{z} + e^{-z}\right)\cdot\left(e^{z-w} + e^{-(z-w)}\right)}\right\}$$

$$\delta V_y = A\left\{\frac{\left(e^{z}\cdot e^{z-w} + e^{z}\cdot e^{-(z-w)} - e^{-z}\cdot e^{z-w} - e^{-z}\cdot e^{-(z-w)} - e^{z}\cdot e^{z-w} + e^{z}\cdot e^{-(z-w)} - e^{-z}\cdot e^{z-w}\right)}{\left(e^{2z-w} + e^{w} + e^{-w} + e^{-(2z-w)}\right)}\right\}$$

$$\delta V_y = A\left\{\frac{2\left(e^{w} - e^{-w}\right)}{e^{z}\left(e^{z-w} + e^{-(z-w)}\right) + e^{-z}\left(e^{z-w} + e^{-(z-w)}\right)}\right\}$$

$$\delta V_y = A\left\{\frac{4\sinh(w)}{4\cosh(z)\cdot\cosh(z-w)}\right\} = \frac{A\sinh\left(\frac{bc}{A}\right)}{\cosh\left(\frac{bx}{A}\right)\cdot\cosh\left(\frac{b(x-c)}{A}\right)} .$$

The interpolated folding signals can now be calculated with:

$$V_{int\_i} = V_{out1} - \frac{i}{8}\cdot\delta V_y = A\cdot tanh\left(\frac{b\cdot x}{A}\right) - \frac{i}{8}\cdot\frac{A\sinh\left(\frac{bc}{A}\right)}{\cosh\left(\frac{bx}{A}\right)\cdot\cosh\left(\frac{b(x-c)}{A}\right)}$$

From the function V_{int_i} the interpolated zero crossing can be derived and compared with the ideal zerocrossing. The interpolated zero crossing x_i can be calculated with:

$$V_{int\_i} = A\cdot tanh\left(\frac{b\cdot x}{A}\right) - \frac{i}{8}\cdot\frac{A\sinh\left(\frac{bc}{A}\right)}{\cosh\left(\frac{bx}{A}\right)\cdot\cosh\left(\frac{b(x-c)}{A}\right)} = 0$$

$$\tanh\left(\frac{b\cdot x}{A}\right)=\frac{i}{8}\cdot\frac{\sinh\left(\frac{bc}{A}\right)}{\cosh\left(\frac{bx}{A}\right)\cdot\cosh\left(\frac{b(x-c)}{A}\right)}$$

$$\sinh\left(\frac{2bx-bc}{A}\right)=\frac{1}{2}\left(\left(\frac{i}{2}-2\right)\cdot\sinh\left(\frac{bc}{A}\right)\right)$$

$$x_i=\frac{c}{2}+\frac{A}{2b}\left(\sinh^{-1}\left(\left(\frac{i}{4}-1\right)\right)\cdot\sinh\left(\frac{bc}{A}\right)\right)$$

The difference between the ideal zero crossing and the interpolated zero crossing can be calculated:

$$\delta_{INL}=\frac{256}{V_{range}}\cdot\left[\frac{i\cdot V_{range}}{256}-\left(\frac{c}{2}+\frac{A}{2b}\left(\sinh^{-1}\left(\left(\frac{i}{4}-1\right)\right)\cdot\sinh\left(\frac{bc}{A}\right)\right)\right)\right].$$

The difference, called δ_{INL}, can be plotted for various of parameters A, b and c. From this figure the best gain, amplitude ratio can derived for a minimum interpolation error. In the preprocessing block the actual V_{range} = 8/9V and the distance between two folding signals c = 1/36V. The parameter A and b can now be optimized by drawing the plots of δ_{INL} in figure 6.11 and 6.12. In these figures the distance c = 1/36V is taken!

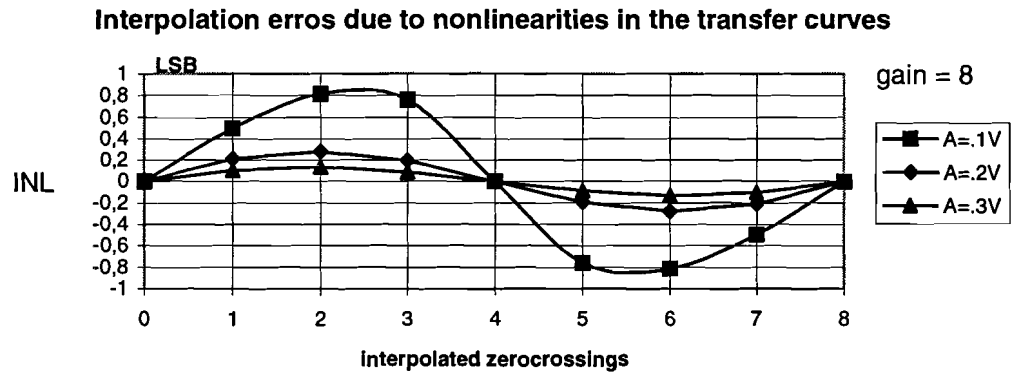


Figure 6.11 : δINL in LSB's with gain = 8 and amplitude A of nine folding as variable

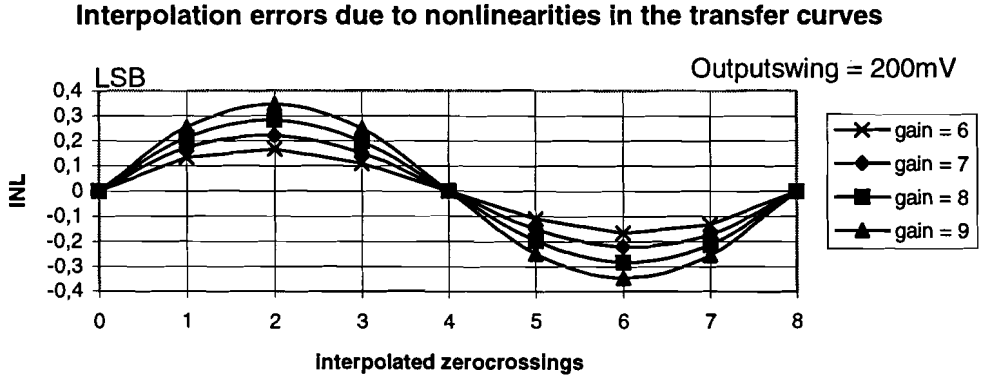


Figure 6.12: δINL in LSB's with amplitude = 200mV and $gain_{tot}$ nine folding as variable

With these two graphics the best gain / amplitude ratio can be chosen. For the realization of the total fine folding circuit a total gain of eight is chosen with a total nine folding amplitude of 200mV. The V_{tt} (output swing) of the fine folding signal is then 400mV. The output swing cannot be chosen to high because this would require large current through the emitter follower of the nine folding block. The emitter follower has to drive the interpolation ladder. The maximum resistance of the interpolation ladder is depended of the input circuit of the comparators. The interpolation ladder and fine folding circuits are discussed in chapter 7.

The gain for the total preprocessing circuit is split up into three parts; input gain stages, three folding block and the three folding comb. block. The gain of the input gain stage is dependent of the output swing. With an amplitude of 200mV the maximum gain of the input stage, without emitter degeneration resistors, is 200mV / (2*25mV) = 4. The remaining gain of 2 should be divided over the three and three folding combination block. The gain plan for the preprocessing block is: gain input stage = 4, gain three/three comb. folding block = $\sqrt{2}$ for a total gain of 8. In table 5 the interpolated - and ideal zerocrossings are calculated and the difference between the zero crossings is calculated in LSBs.

Table 5: Summarized interpolation error with parameter A = 200mV and gain = 8.

Ideal zero crossing [mV]	interpolated zero-crossing [mV]	difference δ_{INL} [LSB]
3.47	2.73	+0.213
6.94	5.97	+0.282
10.42	9.73	+0.196
13.88	13.88	0
18.04	17.36	-0.196
19.85	20.83	-0.282
23.57	24.31	-0.213

In the derivation above, additional interpolation errors generated in folding circuits are not taken in account. Offset voltage of the input circuit is not included and the total output noise of the folding circuits is not taken in account. It can be assumed that the interpolation errors due to the non linear transfer curves of the input gain stages and folding circuits are dominant for the total (dc) INL. In chapter 7, the measurement with a special developed INL program is performed with the total fine folding circuit. From the derivation above, with an amplitude of 200mV and a gain of 8, the INL should be about 0.3LSB.

6.6 DC SETTINGS INPUT GAIN STAGE

The amplitude A (I_{bias} * R_{load}) of the differential pairs should be at least 200mV for keeping the INL below .3LSB. The gain - outputswing relation is constant. The biasing current is an important parameter for setting the bandwidth of the input gain stage. The biasing current is minimized for the bandwidth specification. In figure 6.12 a relation is shown between the collector current of the current source and the base-emitter voltage of the current source. The current can be calculated now by taking 990mV - 760mV / 30KΩ = 7.67μA. The other settings for the input gain stages without emitter followers are shown in table 6.

Table 6 : Reference ladder / Input stage without emitter follower parameter summary

Parameters ref. ladder	Value
reference tap resistor	40 Ω (# 36)
power consumption	694 μW ($V_{ref,max}$ - $V_{ref,min}$)
input gain stage	
transistor type	n10L24pm (mult. = 1)
V_{bias}	990 mV
R_{bias}	30 kΩ
I_{tail}	7.67 μA
R_{cm}	50 kΩ
R_{load}	28 kΩ
g_m	0.154 mA/V
V_{out}, V_{outc}	2.5 V
power consumption	23 μW @ V_{CC} = 3V
DC - gain	4
output swing (2*A)	400 mV

The common mode output voltage is calculated with: V_{CC} - I_{bias}*R_{cm} - .5 * A. The total power consumption of the input stage /reference ladder combination is calculated with: $P_{tot,input\ /reference\ stage}$ = 694μW + 36*23μW = 1.52mW, with V_{CC} = 3V and 36 reference levels.
With the function $V_{be}(I_C)$ in figure 6.13 the R_{bias} can be calculated and to the desired current.

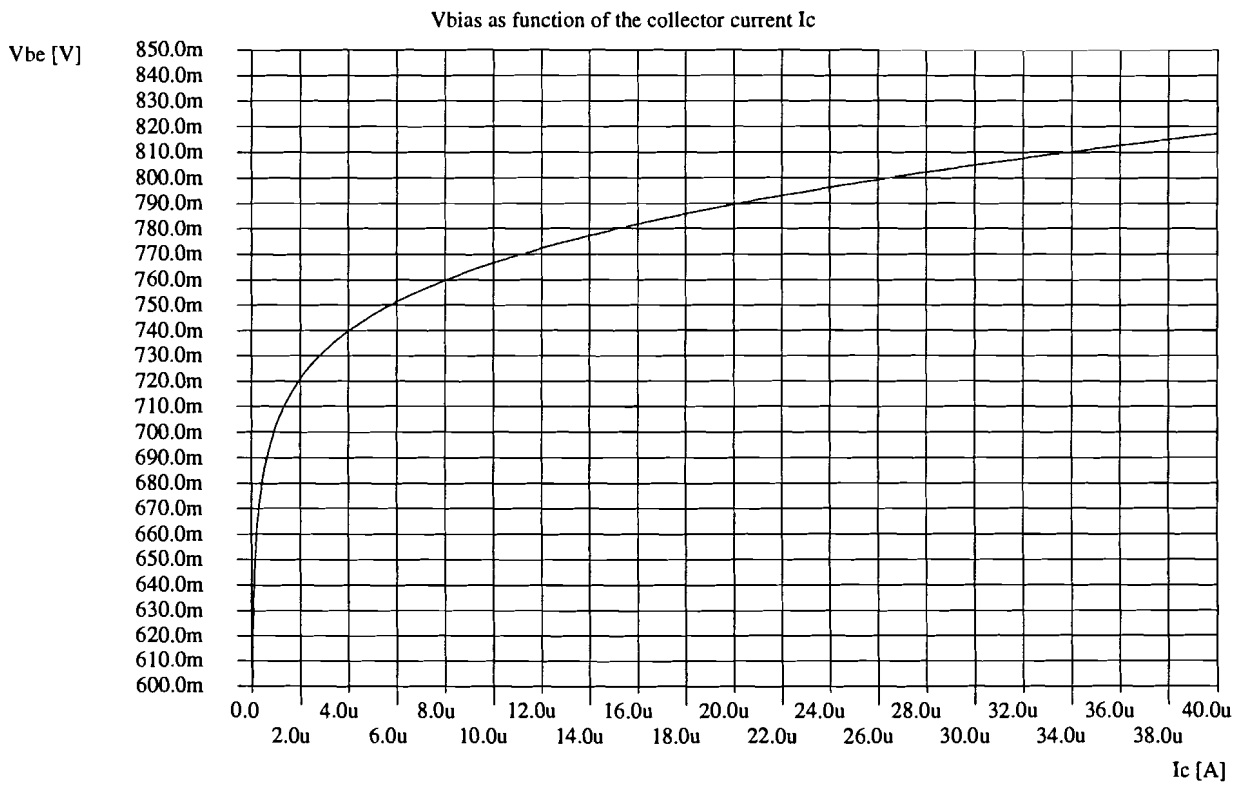


Figure 6.13: Vbias as function of the collector current Ic

7. FINE FOLDING CIRCUITS

7.1 INTRODUCTION

Up till now the reference ladder and the input gain stages have been discussed. From the input 'one' folding signals 12 'three' folding signals are generated. The 12 'three' folding signals are combined to 4 'nine' folding signals. Because the output of the input gain stages are differential, the folding signals can be implemented by using a circuit with three cross-coupled differential pairs. The differential pairs are connected to two load resistors. The discussion of the three folding block is nearly the same as the three folding combination block. The only difference is that the combination folding block has to drive the interpolation network, so in this circuit emitter followers are used. In normal operation of the folding circuit, only one differential pair will operate in its linear range. In the other two differential pairs the tail current will flow through only one of the common emitter transistors. The current supplied by the differential pairs which are out of their linear range should be equally distributed over the load resistors. *For an equal distribution of the tail currents the number of folding stages always should be odd! A folding scheme with an even folding factor would require an extra 'dummy' differential pair for a proper common biasing.*

7.2 STANDARD THREE FOLDING BLOCK

In this chapter, the standard implementation of the three folding block is discussed. An implementation form is depicted in figure 7.1. The inputs s_i are the outputs of the input gain stages with i ∈ [1,12] in this case.

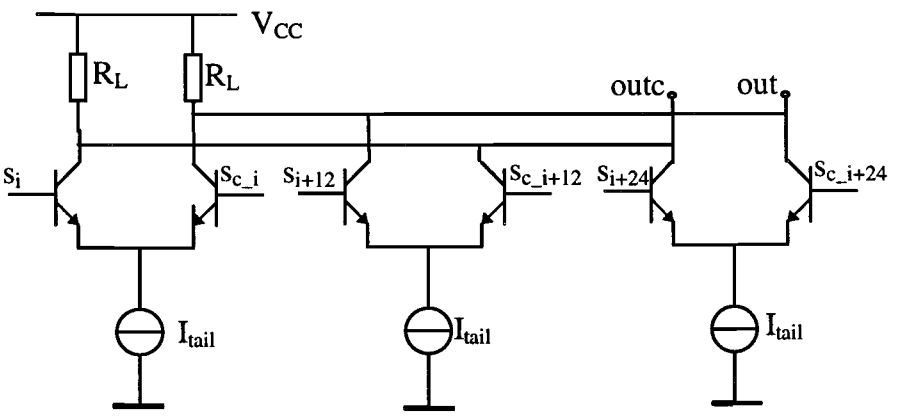


Figure 7.1 : Implementation of standard 'three' folding block

The distance between the zerocrossings of the three 'one' folding signals is $12*V_{range}/32$. As mentioned before, it can be stated that only 'one' of the three differential pairs is in it linear range. The common-mode voltage level at the output will be shifted, with respect to the output level of a single differential pair, with $3/2*I_{tail}*R_L$. The output voltage equations can be derived for the circuit in figure 7.1 with the first differential pair in the linear range:

$$V_{out} = V_{cc} - R_L \cdot \left(\frac{3}{2} \cdot I_{tail} + \frac{1}{2} \cdot I_{tail} \tanh\left(\frac{V_{s\_i} - V_{sc\_i}}{2\,V_T} \right) \right)$$

$$V_{outc} = V_{cc} - R_L \cdot \left(\frac{3}{2} \cdot I_{tail} - \frac{1}{2} \cdot I_{tail} \tanh\left(\frac{V_{s\_i} - V_{sc\_i}}{2\,V_T} \right) \right)$$

$$V_{out} - V_{outc} = R_L \cdot I_{tail} \tanh\left(\frac{V_{s\_i} - V_{sc\_i}}{2\,V_T} \right)$$

The output voltage as function of all the three differential pairs can also be derived.

$$V_{out} - V_{outc} = R_L \cdot I_{tail} \cdot \left(\tanh\left(\frac{V_{s\_i} - V_{sc\_i}}{2\,V_T} \right) - \tanh\left(\frac{V_{s\_i+12} - V_{sc\_i+12}}{2\,V_T} \right) + \tanh\left(\frac{V_{s\_i+24} - V_{sc\_i+24}}{2\,V_T} \right) \right)$$

with $i \in [1, 12]$ and $V_{s\_i} - V_{sc\_i}$ as the differential output voltage of the input gain stages. The gain of the three folding block should be approximately $\sqrt{2}$. The gain is the same as derived for the input gain stage. Inserting this gain of $\sqrt{2}$ into the equation:

$gain = \frac{I_c \cdot R_L}{\frac{kT}{q}} = \sqrt{2} \Rightarrow I_c \cdot R_L = \sqrt{2} \cdot 25mV = 35.35\,mV$. The total output swing becomes now approximately 71mV which is too low for this application. The output voltage swing of the differential output should be at least 400mV. The configuration of the three folding block as in figure 7.1 has a constant gain-output swing relation. The linear range of the differential pair can be enlarged by using emitter-degeneration resistors. In the differential pair a local series-feedback is generated. A differential pair with feedback is shown in figure 7.2.

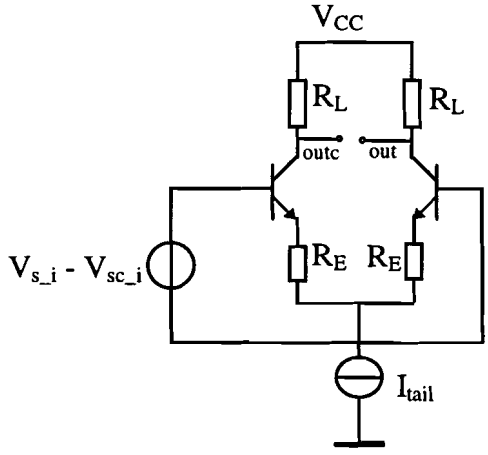


Figure 7.2 : Differential pair with local serie feedback

The differential output voltage and gain is given by:

$$V_{diff,out} = V_{out} - V_{outc} = I_{bias} \cdot R_L \cdot \tanh\left(\frac{V_{s\_i} - V_{sc\_i} - \frac{R_E}{R_L} V_{diff,out}}{2V_T} \right)$$

$$gain_{3fold} = \frac{R_L}{R_E} \cdot \frac{1}{1 + \frac{g_m R_E}{1 + \frac{r_b + R_E}{r_\pi}}}$$

The gain becomes about R_L/R_E if $I_{bias}*R_E >> V_T$ or the gain is $R_L/R_E*(1/(1+g_mR_E)$ for values of $(r_b + R_E) << r_\pi$. In case of the three folding amplifier in the ADC, the current I_{bias} cannot be chosen too high (power consumption). The current is chosen at the value where the minimum required bandwidth is reached. With this current all the other values of the resistors can be calculated. The output voltage A of the three folding amplifier should be approximately 200mV. In the three folding block no emitter followers are used for keeping the power consumption low. The level-shift needed to drive the next 'three folding comb' block is created with a 'common-mode' resistor as used in the input gain stages. The basic circuit of the three folding amplifier is modified to the circuit in figure 7.3.

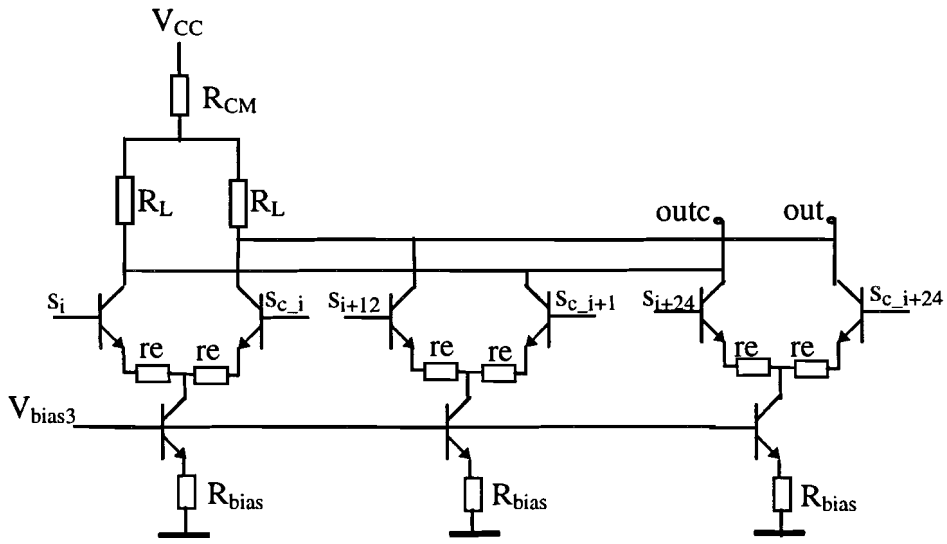


Figure 7.3 : Implementation of 'three' folding block in ADC

The total gain for small signals up till now is the product of the gain of the input gain stage and the gain of the three folding block.
The parameter setting of the three folding amplifier is summarized in table 6.

Table 6 : Three folding amplifier parameters

Parameter	Value
transistor type	n10L24pm mult. 1
V_{bias3}	1.17 V
R_{bias}	30 kΩ
I_{bias}	13.2 μA
R_{CM}	3.4 kΩ
g_{m3fold}	0.25 mA/V
R_{load}	15.385 kΩ
Re	6.154 kΩ
V_{out}, V_{outc}	2.56 V
power consumption	118.8 μW @ V_{CC} = 3V
DC - gain	1.47
output swing (2*A)	400 mV

The common-mode output voltage is calculated with: V_{CC} - 3*I_{bias}*R_{CM} - 3/2*I_{bias}*R_{load}.

7.3 THREE FOLDING COMBINATION BLOCK

With this block the 12 'three folding' signals are combined to 4 'nine folding' signals. Also this circuit has to drive the interpolation ladder. In this circuit emitter followers are used, because it costs relatively a little more power. The three folding comb block is build the same as the three folding block. The only difference is that the level-shift resistor is not needed anymore. The dc shift (of one V_{be}) is now created with the emitter followers. The circuit is shown in figure 7.4.

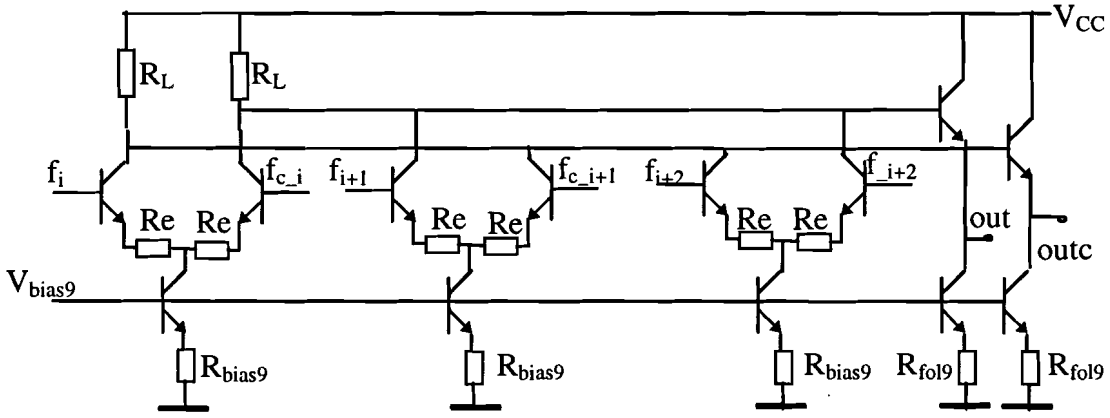


Figure 7.4 : Implementation of 'three' folding comb. block in ADC

The values of the resistors with the biasing currents are summarized in table 7.

Table 7 : Three folding combination amplifier parameters

Parameter	Value
transistor type	n10L24pm mult. 1
V_{bias9}	1.16 V
R_{bias9}	30 kΩ
I_{bias9}	13.67 µA
R_{fol9}	8 kΩ
I_{fol9}	41.88 µA
g_{m9fold}	0.25 mA/V
g_{mfol}	1.71 mA/V
R_{out}	585 Ω
R_{load}	16.5 kΩ
R_e	5.8 kΩ
V_{out}, V_{outc}	2 V
power consumption	405 µW @ V_{CC} = 3V
DC - gain	1.47
output swing (2*A)	400 mV

7.4 INTERPOLATION NETWORK

The function of the interpolation ladder is discussed in chapter 3. The missing 28 folding signals are generated by a circular 8 times interpolation network. The extra resistors added in series with the outputs compensates the output resistance inequalities. The values of these serie resistors can be calculated as function of the interpolation resistor R. The values of the serie resistors are depicted in figure 7.5. If there are no serie resistors used, the maximum difference in the output resistance occurs at the mid-tap of the interpolation ladder. This output resistance at the mid-tap is (4R//4R) 2R.

The value of the interpolation resistor R is depended of the input circuit of the comparator. Because the interpolation network is driven from the voltage-followers, the output impedance of the network, which drives the comparators varies from zero to R (with no serie compensation). The capacitive load of the comparator input stages on the interpolation network results in a variable signal delay, which can easily be more than is allowed in this system.
The maximum timing error of the 8-bit ADC can be calculated as follows [2]:

$$dT \leq \frac{2^{-(N+1)}}{\pi f_{in}} = \frac{2^{-9}}{\pi 50 \cdot 10^{6}} = 12\,ps.$$

Therefore, additional resistors $R_{serie\_1,2,3,4}$ in figure 7.5 are added in serie with the outputs to make all outputs impedance equal to 2R. Now all comparator stages have an equal delay.

A cross coupling between the beginning and the end of the interpolation network is needed to obtain interpolated signals "around the corner", which is necessary because of the repetitive properties of the nine folding signals.

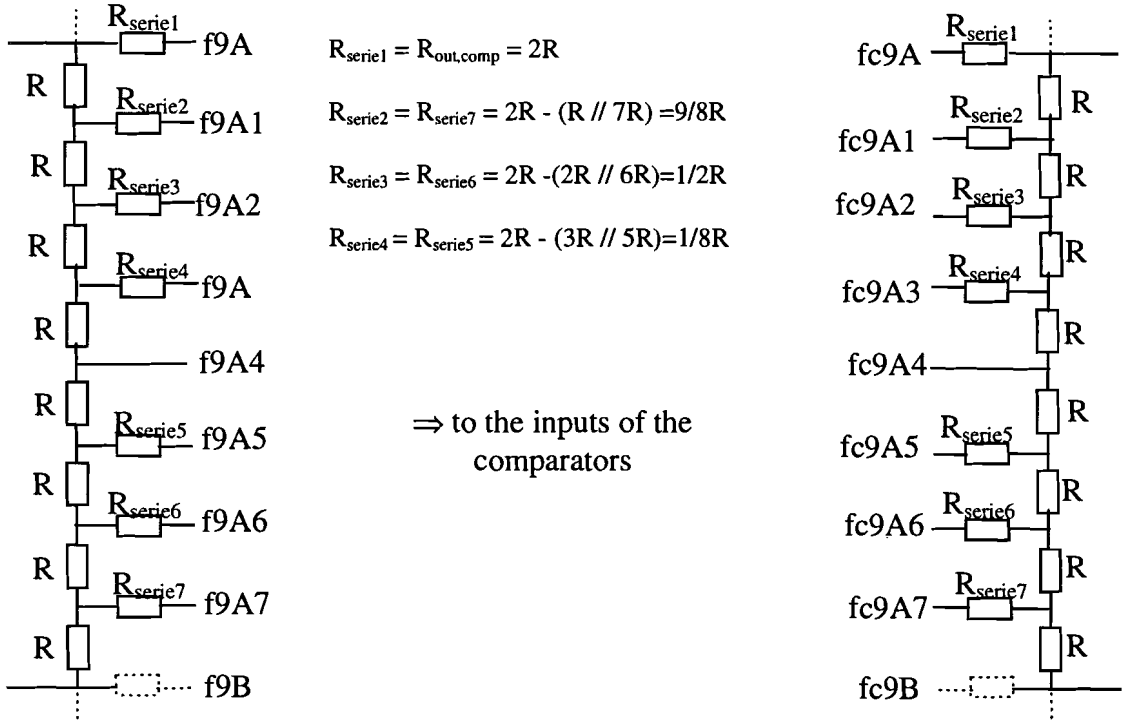


Figure 7.5 : Interpolation ladder with serie resistors for delay compensation

Simulations on the input stage of the comparator have proved that due to the switching of the master comparator, the base current variation in the comparator input stage is approximately .35μA. This base current may cause a maximum voltage, across the 2R output resistance of the interpolation network, of a ½LSB. The maximum resistor value R of the interpolation network is calculated as follows:

$$2R = V_{½LSB} / I_{bmax,comp} = ½ * (1/288) / 0.35\mu A = 5k\Omega \Rightarrow R = 2.5k\Omega.$$

The maximum current flowing through the interpolation network is depended of the maximum voltage difference between the two nine folding signals. In the DC - simulations of the fine folding circuit the maximum voltage difference is 170mV. The current flowing through the ladder is now 170mV/(8*2.5kΩ) = 8.5μA. The current through the emitter-followers in the three folding combination block is chosen approximately a factor 5 higher. In the INL simulations of the fine preprocessing part this current has a great influence on the interpolation errors. There was almost a linear relation between the emitter follower current and the maximum third order distortion component. For higher emitter currents (factor 10) the third order distortion component remain at the same level, but by lowering the emitter current the third harmonic distortion increased almost linear. Moreover, the distortion components is discussed in the dynamic performance of the fine folding circuit in chapter 7.6.

7.5 PERFORMANCE OF FINE FOLDING CIRCUIT

7.5.1 Simulation with input signal as ramp between 1.5V and 2.V

The analog preprocessing part is discussed in this chapter and the most important simulations are described. The first simulation is performed to get an overview of the total fine folding structure with the cascaded folding technique. In the simulation a ramp from 1.5V to 2.5V is applied at the input of the circuit. With this signal all the zerocrossing occurs once, and the output voltage swing can be measured of each sub circuit. In figure 7.6 an overview of the folding signals is given.

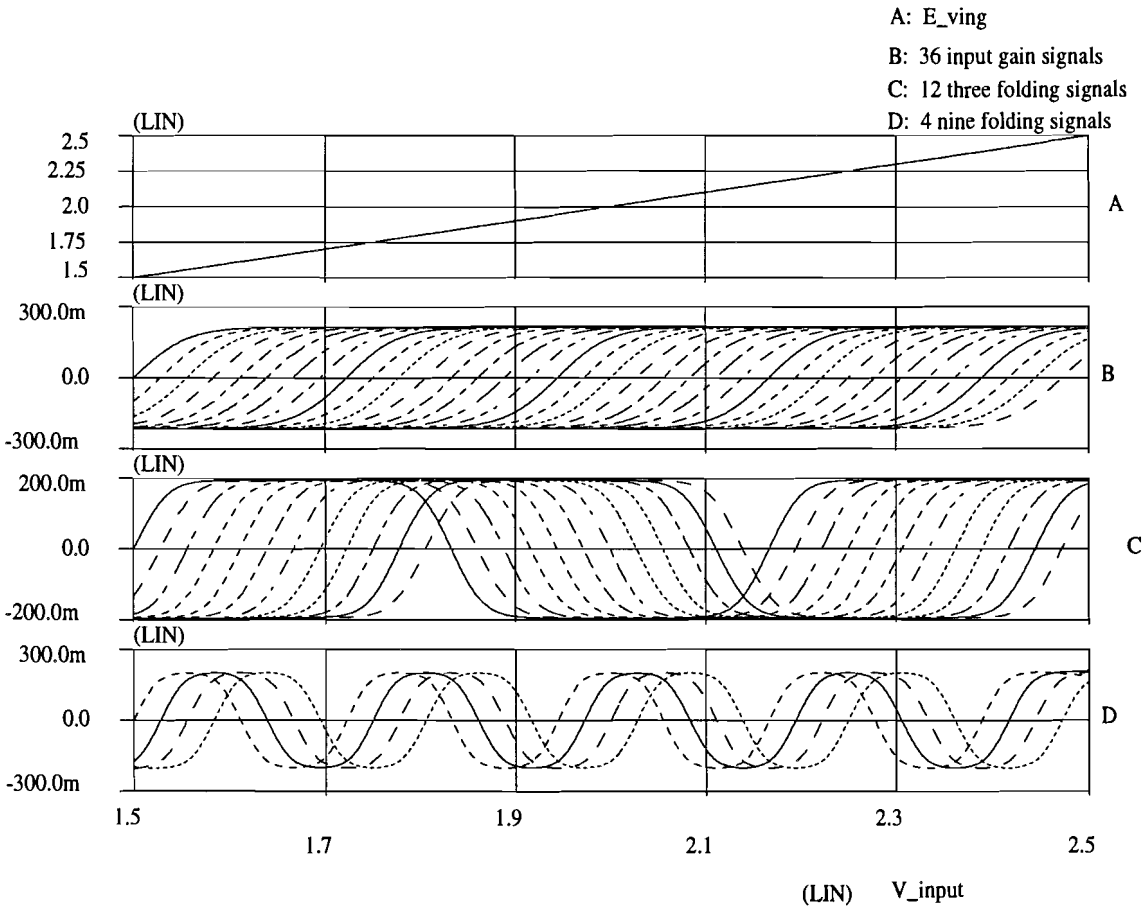


Figure 7.6 : Overview fine folding signals as function of the input voltage

7.5.2 AC - simulation for measuring the small signal bandwidth

The bandwidth of the preprocessing part is measured with a small signal (1mV) at the input of the ADC and a specified reference voltage level. The bandwidth is measured with the coarse folding part, discussed in the next chapter, as extra loading of the input gain stages. The signal path for measuring the -3dB bandwidth of the preprocessing part is;

$(V_{in}, ref_{20})_{\text{input gain stage}} \Rightarrow (f_{11,inb}, f_{11,incb})_{3\text{ fold}} \Rightarrow (f_{D,inb}, f_{D,incb})_{3\text{ fold comb}} \Rightarrow (f_{9D}, f_{9cD})_{interpol}$,
with ref_{20} as the voltage of tap number 20 of the reference ladder network

With this signal part, the additional loading of the coarse folding part is not included. The amplitude of the input signal is 1mV or -60dB. The result of the simulation is shown in figure 7.7. In this figure the gain of the input gain stage, three folding block and three folding combination block can be derived. The bandwidth of the preprocessing part for small signals with this signal path is 487MHz.

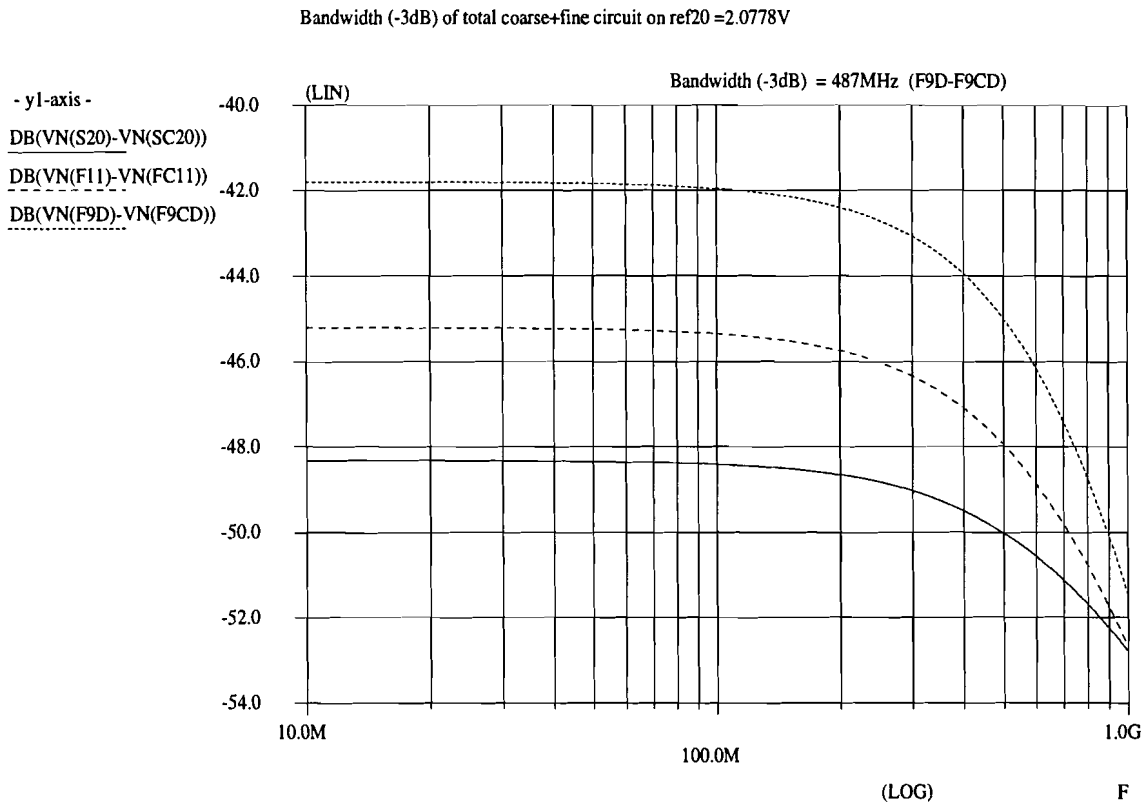


Figure 7.7 : Small signal bandwidth on ref_{20} of the preprocessing part

The gain and bandwidth of the stages summarized from figure 7.7 are shown in table 8;

Table 8: Gain/bandwidth preprocessing part with input signal of -60dB on ref_{20}

type folding circuit with differential output connection	level / gain [dB] / ..	Bandwidth [MHz]
input gain stage (s_{20} - sc_{20})	-48.3 / 3.85	720
three folding block (f11 - fc11)	-45.2 / 1.42	530
three folding comb. block (fD - fcD)	-41.9 / 1.47	487

The total gain of the preprocessing part equals 3.85*1.42*1.47 = 8.04 with a total bandwidth of 487MHz.

For measuring the bandwidth of the preprocessing part with a signal path which includes the loading of the coarse folding part another signal path is chosen:

$(V_{in}, ref_{19})_{input\ gain\ stage} \Rightarrow (f_{8,\ inb}, f_{8,incb})_{3\ fold} \Rightarrow (f_{C,inb}, f_{C,\ incb})_{3\ fold\ comb} \Rightarrow (f_{9C}, f_{9cC})_{interpol}$.

The result of the simulation is shown in figure 7.8. The input signal amplitude is 1mV added on a common mode voltage level of ref_{19} (2V, tap number 19 of reference level).

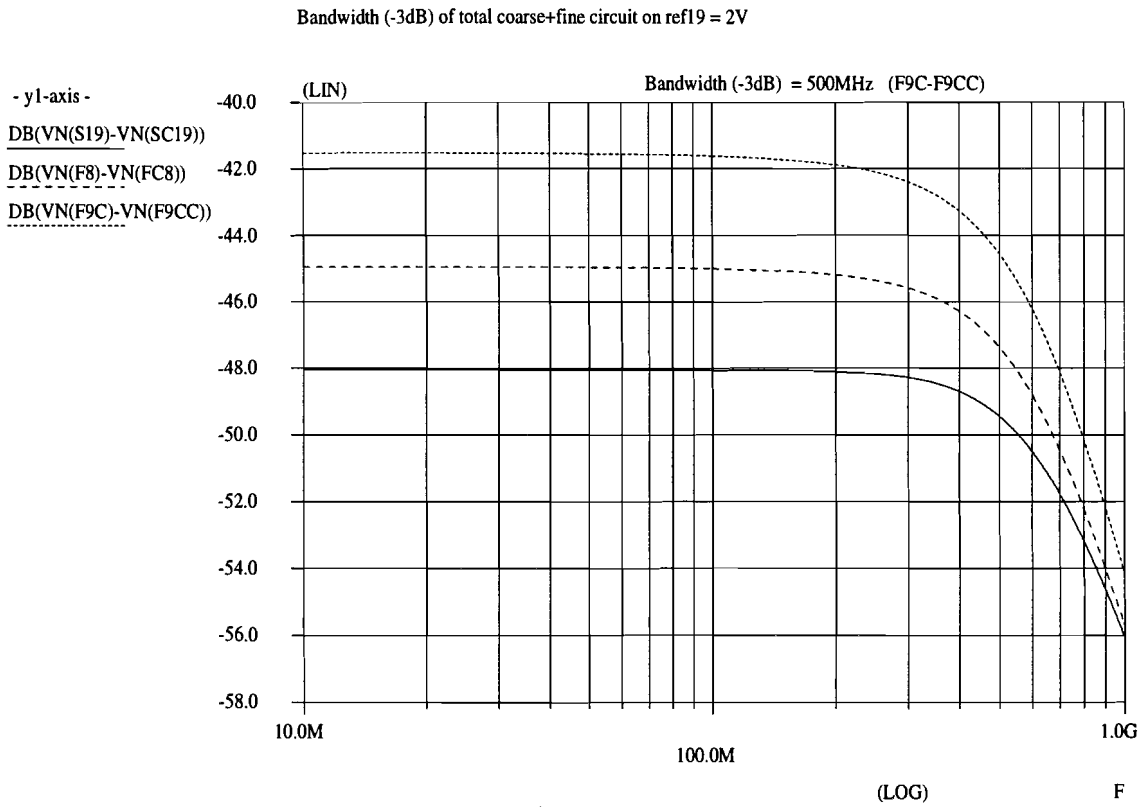


Figure 7.8 : Small signal bandwidth on ref_{19} of the preprocessing part

The results of the simulation shown above are summarized in table 9.

Table 9: Gain/bandwidth preprocessing part with input signal of -60dB on ref_{19}

type folding circuit with differential output connection	level / gain [dB] / ..	Bandwidth [MHz]
input gain stage (s_{19} - sc_{19})	-48 / 4	651
three folding block (f8 - fc8)	-44.9 / 1.43	544
three folding comb. block (fC - fcC)	-41.5 / 1.47	500

The total gain, with this signal path, of the preprocessing part is a little higher: $gain_{tot} = 4*1.43*1.47 = 8.35$ and a bandwidth of 500MHz.

The gain of the three folding - and three folding combination block remain the same, but due to the extra loading of the coarse folding part an emitter follower is added to the input gain stages which are double loaded. The gain and the bandwidth are a little higher than the input gain stages without emitter followers. The gain and bandwidth, which are specified in chapter 6 for the preprocessing block are reached with these simulations. A total gain of 8 (b = 8) with a output voltage swing of 400mV (A = 200mV) are needed for a minimal interpolation error of 0.3LSB. The simulations of the interpolation errors are discussed in the next chapter.

7.5.3 DC - simulation for measuring interpolation errors

The INL (integral non-linearity) is defined by the maximum deviation of the output of the preprocessing part from a straight line between zero (1.5V) and full scale (2.5V). The INL of

the total preprocessing part is simulated with PSTAR. As input signal, a ramp from 1.5V to 2.5V is applied. With this signal all the zerocrossings occur once. The position of the zerocrossing depends on several factors (A, b, c) as discussed in chapter 6. The difference in the interpolated zerocrossing and the ideal zerocrossing can be calculated in LSBs as INL. A special developed software tool calculates the position of the interpolated zerocrossing and compares this with the position of the ideal zerocrossing. The result of this simulation is shown in figure 7.9.

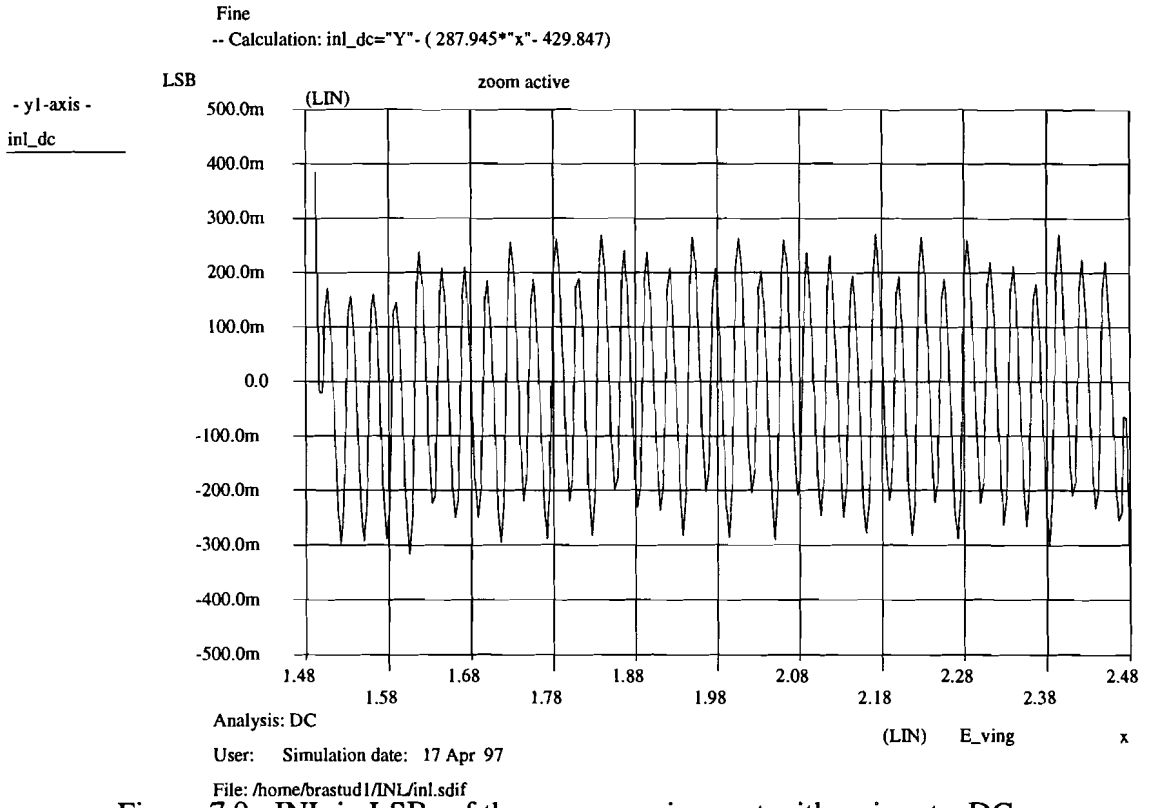


Figure 7.9 : INL in LSBs of the preprocessing part with as input a DC-ramp

In figure 7.9 the maximum deviation of the ideal - with interpolated zerocrossing is about 0.3LSB. This result was also calculated in chapter 6.5 (see figure 6.11 and 6.12).

7.5.4 Conclusions of the performance preprocessing part

From the initial design specifications shown in chapter 2 the following can be maintained;

- the small signal bandwidth of 500MHz is reached
- with the design plan, an output swing of 400mV and a gain of 8, the interpolation errors stay below 0.3LSB
- The power consumption of the preprocessing part, including reference ladder and input gain stages is 4.56mW.

7.6 DYNAMIC PERFORMANCE OF THE PRE-PROCESSING BLOCK

7.6.1 Introduction

In this section, the dynamic performance of the preprocessing block is discussed. The operation of the folding blocks is discussed by examining the transient 'CGAP'(the graphic

analyzer in the cadence design environment) graphs of the folding signals. The schematic includes the cascaded folding blocks with interpolation ladder. The frequencies analyzed are the low frequencies 500kHz and 5MHz and the maximum input frequency 50MHz. The most important dynamic specification of a converter is the signal to noise ratio (SNR). The signal to noise ratio depends on the resolution of the ADC. These SNR automatically includes specifications as Integral Non Linearity (INL), distortion components, noise and the sampling time uncertainty of the ADC. For the preprocessing block the distortion component can be measured and the noise can be simulated. With the theoretical formula: SNR_{max} = 6.02* n +1.79 dB, a SNR of 50dB is possible with this 8 bit converter. The SNR is calculated with a sine wave input with a amplitude of half the maximum input range. To calculated the total SNR, the distortion components, the thermal noise and quantisation noise should be added together.

7.6.2 Dynamic performance at low frequencies

In this section, the dynamic operation of the preprocessing block will be treated. The input frequency of the signal V_{in} equals 500kHz. For the presented system architecture 500kHz can be considered as 'low frequency'. The effects of the capacitance in the circuit are neglected with this frequency. The amplitude of the input signal is very critical in this simulations. The amplitude should be a little larger than the input range, but not larger than one LSB. The analyze is started with the first zerocrossing occurred in the differential MSB-2 signal, fcC - fC. The neighboring interpolated folding signals should at that time not cross the time-axis. In other words: *in a one LSB region around the zerocrossing the comparator may decide either '1' of '0' without losing the eight bit performance of the ADC.* Only one folding signal (MSB-2) is in this region at that time. The delay-time of the preprocessing block is taken into account with the INL simulation and is verified through transient simulations. With the applied sine wave all the zerocrossings occur twice. The delay time introduced by the preprocessing block adds no additional INL error to the simulation. The ideal time of the zerocrossing of the non-interpolated nine folding signal can be calculated with:

$$2\,V + \frac{4}{9}\sin(2\pi f\,t) = 1.5V + \frac{2}{36}\,V + \frac{k-1}{36}V \quad \text{, with } k \in [1,32].$$

In this equation, the input signal with common mode voltage of 2V and an input voltage range of 8/9V is compared with the reference levels started with ref3 (1.5V + (i-1)/36) as the first zerocrossing of the MSB-2 signal. The time difference between two non-interpolated nine folding signals divided by eight is the ideal time of the interpolated zerocrossing.
The time of the non interpolated zerocrossing as function of k is:

$$t_k = \frac{1}{2\pi f}\cdot\arcsin\left(-\frac{1}{2}+\frac{k-1}{32}\right), \text{ with } k \in [1,32].$$

The interpolated ideal zerocrossings occur at:

$$t_{int,k} = \frac{t_{k+1} - t_k}{8}.$$

The interpolated simulated zerocrossings are calculated with a special software tool. From the calculated zerocrossings a sine wave is reconstructed. For an accurate reconstruction of

the sine wave, at least 10 periods of the input signal should be taken into account. In the simulations performed with the preprocessing block 15 periods are simulated and calculated.

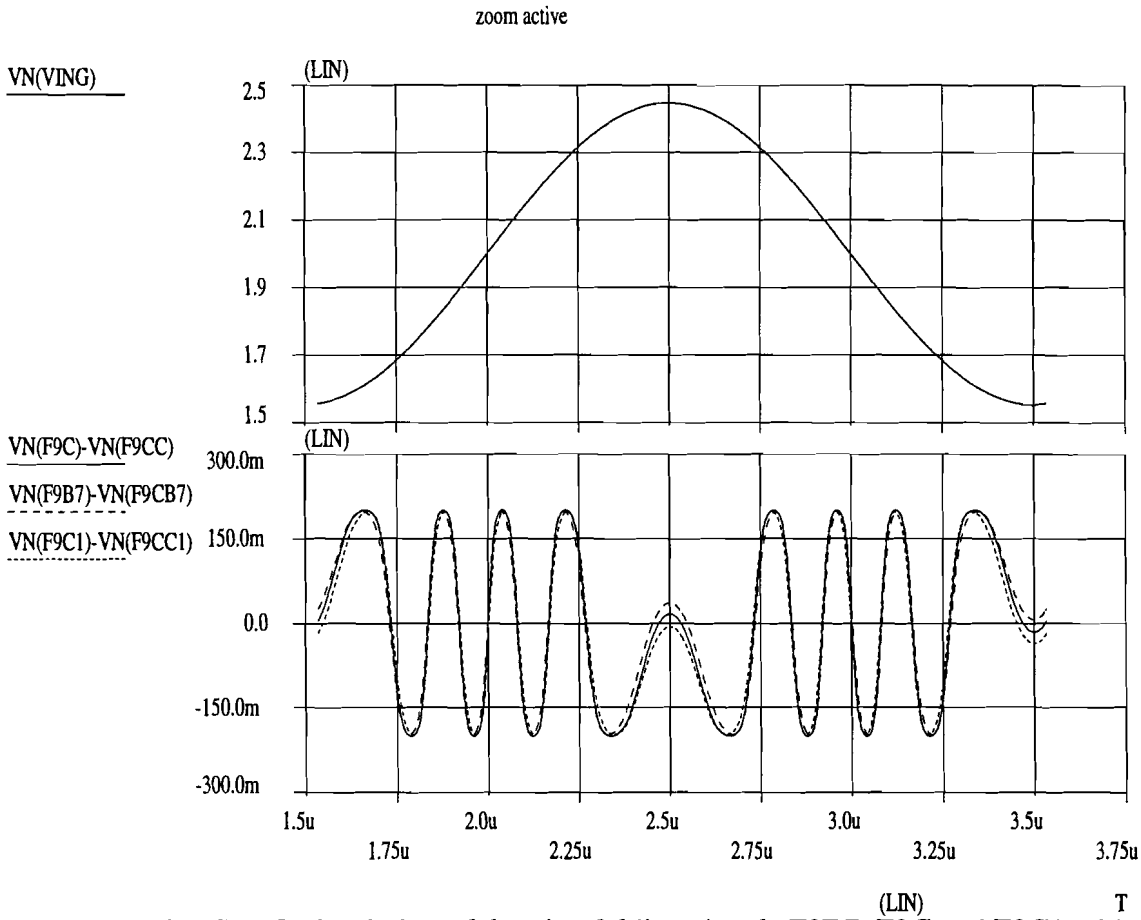


Figure 7.10: PSTAR simulation of the nine folding signals F9B7, F9C and F9C1 with the input signal frequency of 500kHz

In figure 7.10 the result of a part of the transient analysis is shown. For the simplicity, the total 32 folding signals are omitted in this figure. Only the folding signals of the MSB-2 signal and the interpolated signals just above (F9C1) and under (F9B7) the MSB-2 signal are shown (see also the overview of the fine folding circuit in figure 3.12).

The harmonic distortion of the preprocessing block can be analyzed with the folding signals. For this purpose a software tool has been used. The moments of the zerocrossings correspond to the level of the input signal, a reconstruction of this input signal can be made from the zerocrossings. This means, a figure is constructed with the non-equidistant moments of the zerocrossings on the x-axis and the equidistant reference levels on the y-axis. With CGAP, the interpolation function 'natural spline' and FFT options are used for the distortion analysis on the reconstructed sine wave of 15 periods. In figure 7.11, this analyze is shown for a input frequency of 500kHz. The interpolation function 'natural spline' is used, because this with interpolation method the position of the calculated zerocrossings are not affected. The FFT is performed with a Hamming window ($\alpha = 0.54$).

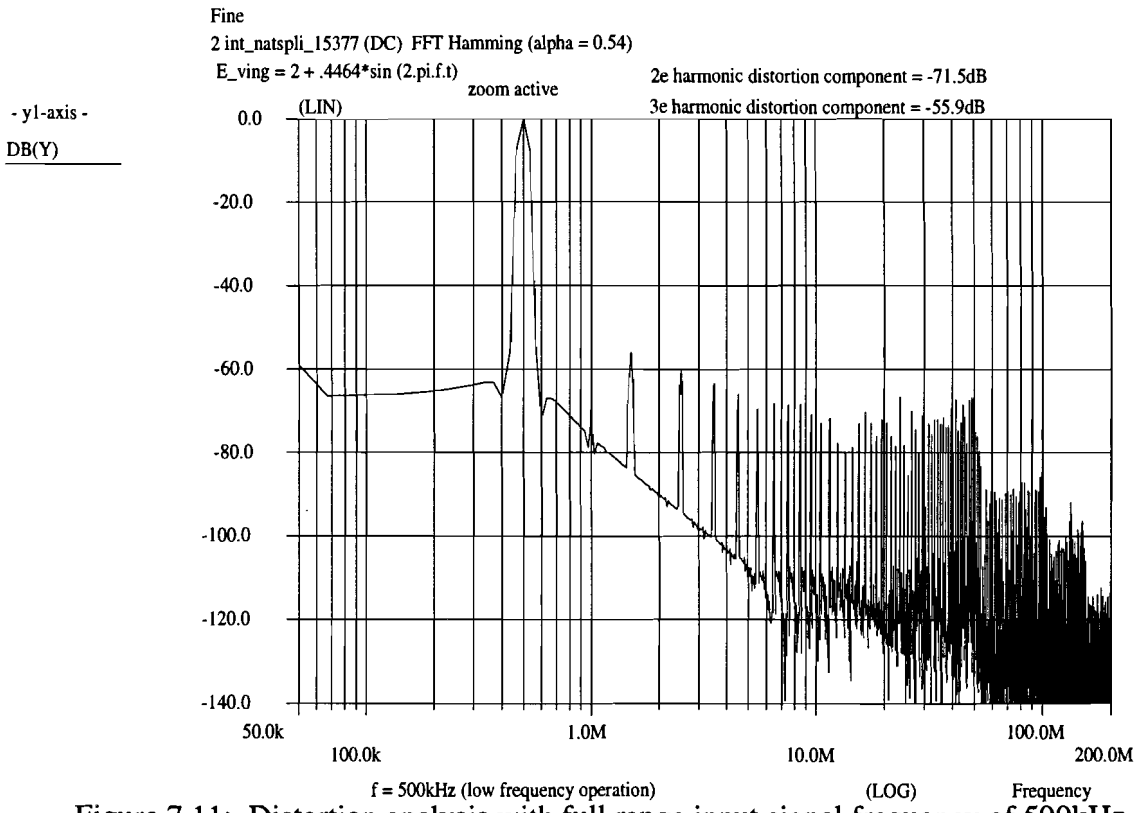


Figure 7.11: Distortion analysis with full range input signal frequency of 500kHz

The distortion components for this input frequency achieves an 8-bit performance.
The input frequency is normalized to 0dB. The second harmonic distortion component (1 MHz) is 71.5dB below and the third harmonic 56dB. For the input frequency of 5MHz the same simulation is done. In figure 7.12 the transient simulation is shown and the result of the distortion analyze is depicted in figure 7.13.

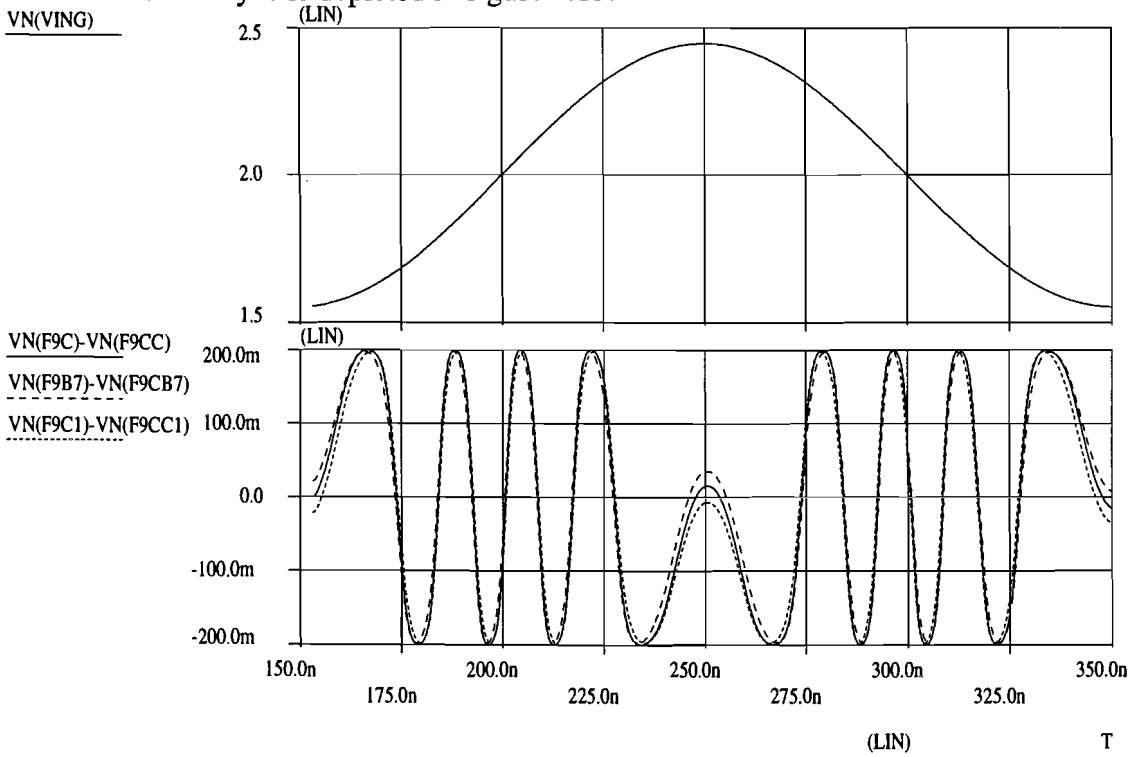


Figure 7.12: PSTAR transient simulation of the nine folding signals F9B7, F9C and F9C1 with the input signal frequency of 5MHz

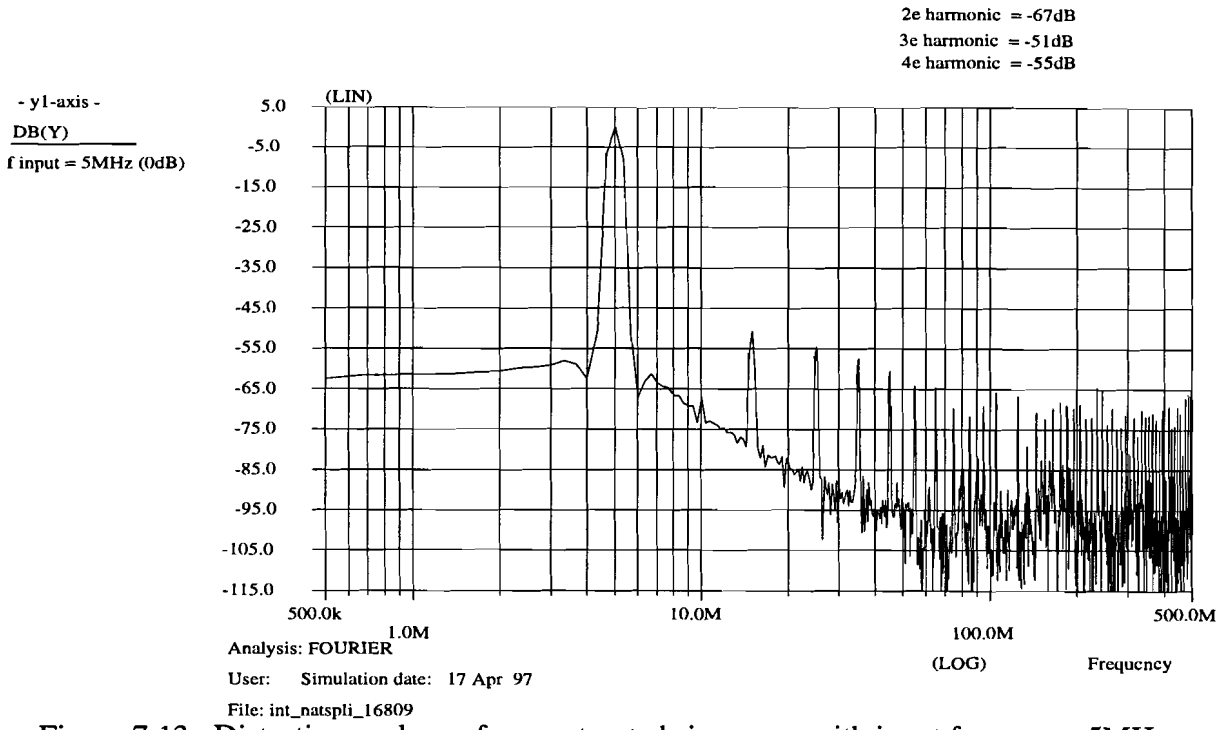


Figure 7.13 : Distortion analyze of reconstructed sine wave with input frequency 5MHz.

7.6.3 Dynamic performance at high frequencies

One of the design goals, summarized in chapter 2, was to have an analog input bandwidth of 50MHz. In the previous section it was clear that the low frequency performance satisfies the design goals. The high frequency equivalent of figure 7.10 is shown in figure 7.14. Figure 7.14 shows the nine folding signals F9C (MSB-2) , F9B7 and F9C1 for an input frequency of 50MHz. Comparing figure 7.10 with 7.14 the difference is a decrease of the amplitude and an increase of the delay. A decrease in amplitude gives a increase of the errors in the zerocrossings.

Distortion analyze of the preprocessing part for an input frequency of 50MHz is shown in figure 7.15. Analyzing this figure, it can be concluded that the preprocessing part still satisfies the design goals of an 8-bit converter. The second harmonic distortion component is -54 dB and the third harmonic distortion is at -55dB.

In all the simulations, the analog preprocessing part is extra loaded with the coarse folding block. Some input gain amplifiers (11) are double loaded, and gives some extra distortion. The position of the zerocrossing is affected by the double loading of the input gain amplifier. The third harmonic distortion component plays a dominant role in the dynamic simulations. In the reconstructed sine wave the third harmonic distortion was seen in the tops of sine wave. The third harmonic distortion is relatively frequency independent. In the simulations, the variation of the current through the emitter followers of the three folding comb. block has a great influence on the third harmonic distortion component. Distortion in emitter followers is relative frequency independent (large bandwidth) and is mainly caused by the amplitude of the nine folding signals. The current through the interpolation ladder causes a deviation of the V_{be} of the emitter follower. This deviation from the ideal point causes distortion:

$$\Delta V_{be} = V_T \ln\left(\frac{I_{fol9} + I_{int}}{I_{fol9}}\right)$$

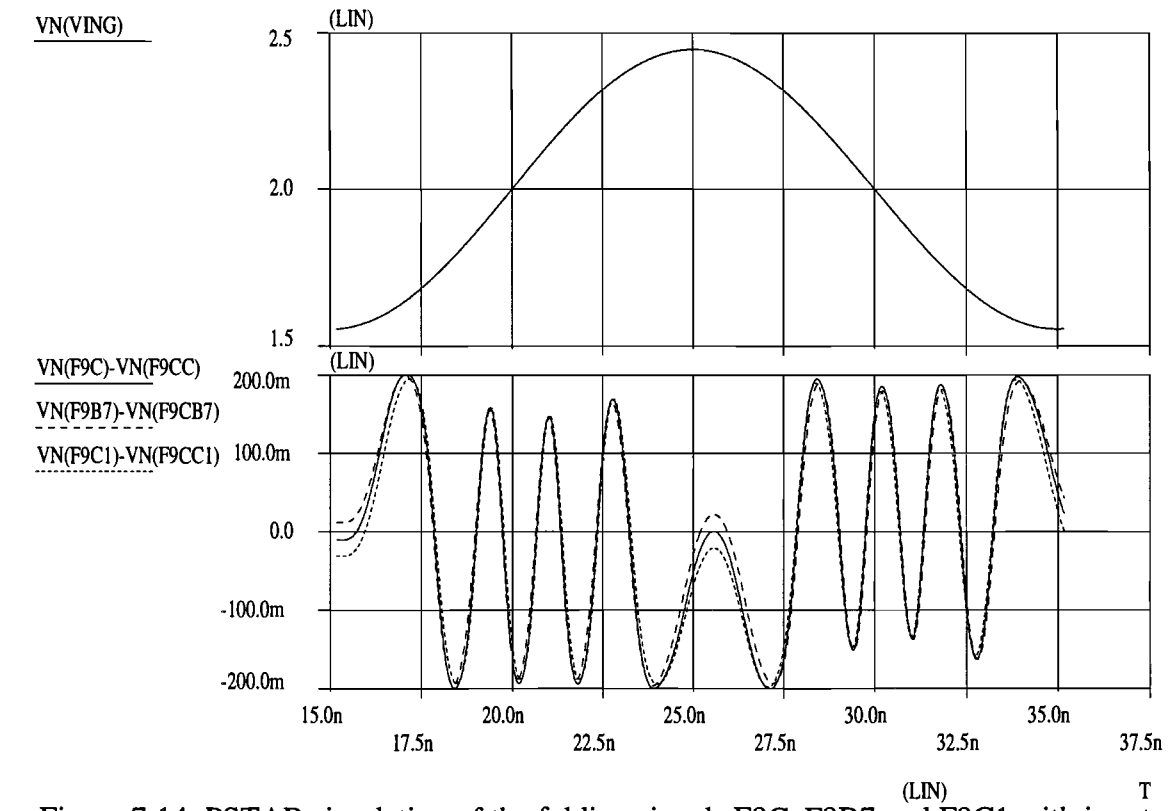


Figure 7.14: PSTAR simulation of the folding signals F9C, F9B7 and F9C1 with input signal frequency 50MHz.

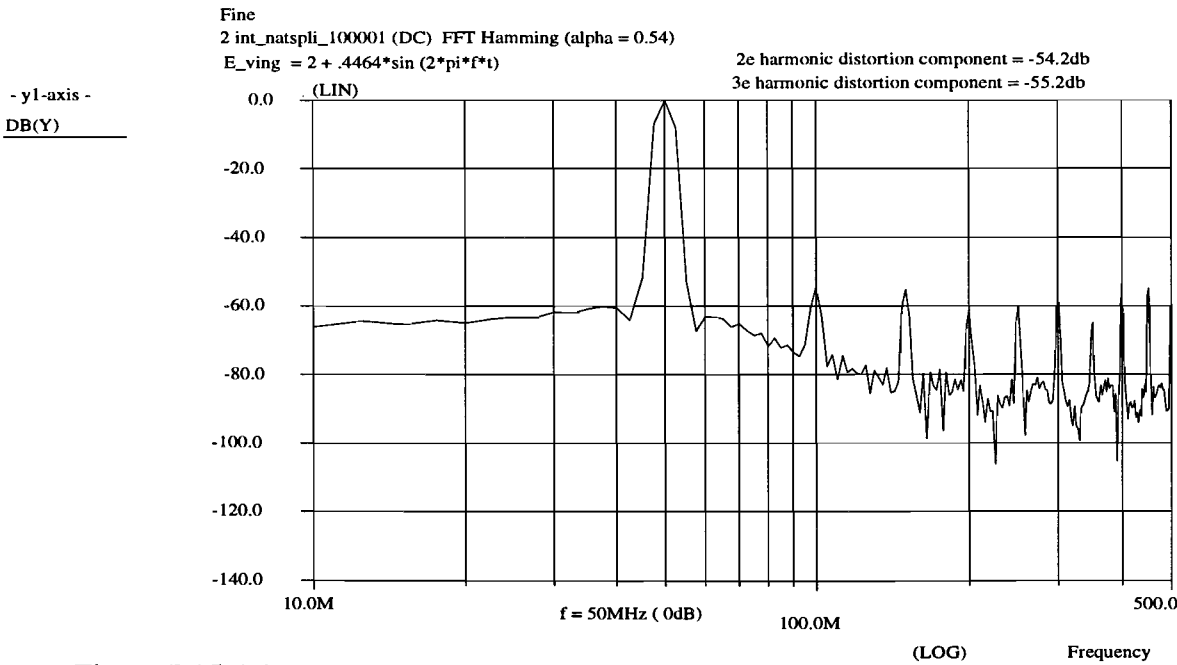


Figure 7.15: Distortion analysis of the reconstructed sine-wave with f_{in} = 50MHz.

A figure of the reconstructed sine-wave with frequency 50MHz is depicted in figure 7.16.

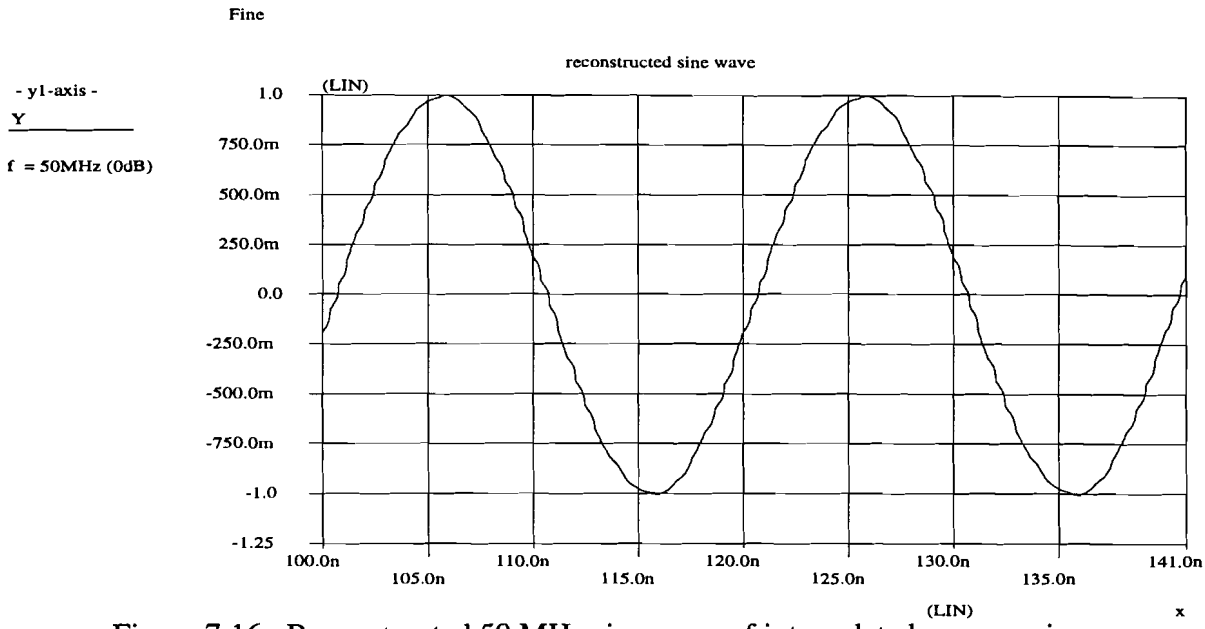


Figure 7.16 : Reconstructed 50 MHz sine wave of interpolated zerocrossings

7.7 NOISE ANALYSIS OF THE ANALOG PREPROCESSING

In this section, the noise behavior of the preprocessing block will be discussed. Noise (thermal noise, 1/f-noise) will influence the zerocrossings of the folding signals. However, a deviation due to noise within the V_{LSB} region will not result in a decrease of the ADC performance. Due to the large preprocessing bandwidth, it is difficult to keep the noise in the system low enough not to detoriate the dynamic performance of the ADC. In a figure 7.17 a result is shown of a PSTAR noise simulation of the fine folding structure. The noise power spectrum is depicted in the characteristic of figure 7.17. The noise is measured in the frequency range from 100KHz to 10GHz. At 10GHz the noise power spectrum of the fine circuit is almost zero. The maximum noise rms. voltage v_{noise}, obtained by integration (summing the noise power spectrum to 10GHz) and taking the root of the noise power spectrum, in a folding fC accounts at 10GHz 4.8mV.

The bandwidth of the fine folding circuit equals about 500MHz. The LSB value of the fine folding circuit is $V_{LSB,fine}$ = 1V / 36 = (8/9)V / 32 = 27.7mV. The rms. quantisation error voltage is represented by $1/\sqrt{12} * V_{LSB,fine}$ = 8mV. Now it can be concluded that the noise in the analog preprocessing block will not detoriate the ADC total performance.

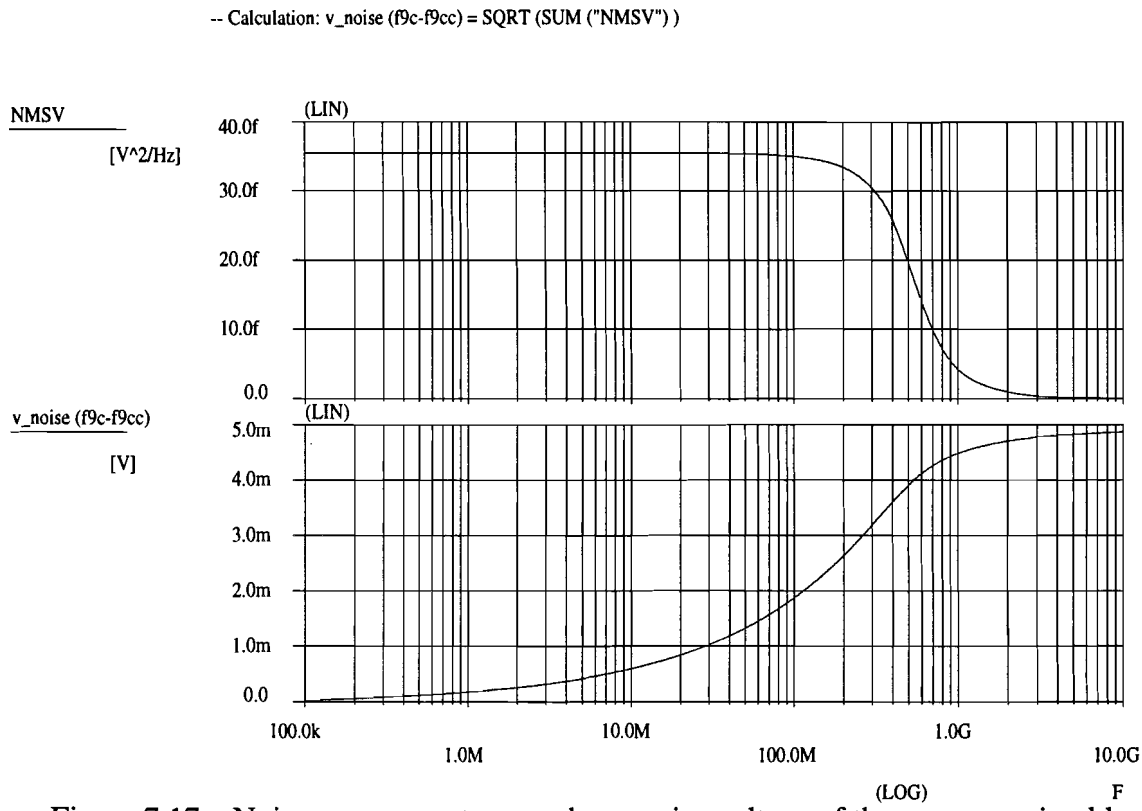


Figure 7.17 : Noise power spectrum and rms noise voltage of the preprocessing block

7.8 OVERALL PERFORMANCE OF THE PREPROCESSING BLOCK

The overall performance depends on several factors such as linearity, noise, harmonic distortion, sampling time uncertainty. All these factors can be captured by one value : Effective Number Of Bits (ENOB) [9] with the function:

$$ENOB = \frac{20\log\left(\frac{signal}{noise + distortion}\right) - 1.76}{6.02}.$$

An ideal 8-bit ADC has no distortion, and the only noise is the quantisation noise of -50dB, and has, according the formula above, 8.0 effective bits. All the non linearity's of the ADC are not present at this moment. From the preprocessing part the distortion components for the maximum input frequency is below the initial specifications in chapter 2. In the static analyses the interpolation error stay below 0.3LSB with an output swing of 400mV and gain of 8.

8. COARSE FOLDING CIRCUITS

8.1 INTRODUCTION

The coarse bits MSB and MSB-1 cannot be generated directly with a flash ADC structure. The delay in the preprocessing block especially around the MSB-2 bit could lead to errors in the output code. It has been mentioned before, that the MSB-2 bit is generated by the analog fine preprocessing. For the position of the MSB-2 bit there is a choice between the non-interpolated folding signals fA, fB, fC and fD, because there is redundancy in the number of reference levels. There are 36 input zerocrossings in order to obtain 32 zerocrossing in one folding. With the eight times folding strategy the 256 zerocrossing can be generated. In chapter 3 it is already mentioned that the transitions of the MSB and MSB-1 bit need to be marked for synchronization. This synchronization is done by the SYNC signals. Synchronization is necessary because different circuitry is used for the different parts of the output code. The windows, symmetrical located around the transitions of the coarse bits, equalize all delay variations of the fine block.

This method of generation of MSB's have some drawbacks. The most important one is the loading of the fine folding circuit. Some of the input gain stage are double loaded. This can cause errors in the position of the zerocrossings. By implementing the input gain stages, which are double loaded, with an emitter follower this error could be reduced. The parameter settings for the input gain stage with emitter follower is shown in table 10.

Table 10 : Input stage with emitter follower parameter summery

Parameter	Value
transistor type	n10L24pm (mult. = 1)
V_{bias}	990 mV
R_{bias}	50.526 kΩ
I_{tail}	4.65 µA
R_{fol}	136.4 kΩ
I_{fol}	2 µA
R_{load}	45 kΩ
g_m	8.89 µA/V
V_{out}, V_{outc}	2.1 V
power consumption	25.7 µW @ V_{CC} = 3V
DC - gain	4
output swing (2*A)	400 mV

The interconnection lines between the input gain stages and the coarse folding block are much longer than the interconnections between the fine folding circuit. Due to the emitter followers, the interconnection lines can be longer than without followers. The low output

impedance of the followers can drive more capacitive (wirering) load. The schematic of the differential pair with emitter followers is shown in Appendix C.

8.2 DEFINITION OF THE COARSE FOLDING SIGNALS

The coarse signals can be defined in the following order. The position of the MSB-2 bit is derived from the mid-level of the reference ladder. The 0 $\Rightarrow$ 1 transition of the MSB gives the position of the MSB-2 bit. The midlevel of the reference ladder is 2V, or *ref19*. From figure 3.9 the MSB-2 bit is the inverse of the differential (fC - fcC) nine folding signal. In figure 8.1 is a schematic overview shown with the taps of the reference ladder network. The minimum reference voltage is 1.5V and the maximum reference voltage is set on 2.5V. For a symmetric MSB 0 $\Rightarrow$ 1 flank, the reference level *ref19* is chosen as the midlevel. The level *ref19* appears in the nine folding signal C. From this signal the other MSB bits can be subtracted. The range of the input voltage become now 1V - 4/36V = 8/9V. The range signal R is made from the reference levels *5* and *33* appeared in signal A. This signal detects if there is an over- or underflow from the input signal compares to the reference ladder network.

The wanted wave-form for the MSB-1 is shown in figure 8.1 as *msb-1*. The double load of input gain stage 19, can be removed by not using ref_{19}. The MSB-1 folding signal contains only information at the ¼ and ¾ full scale locations. Another implementation of the MSB-1 folding signal is depicted in figure 8.1 as *msb-1'*.

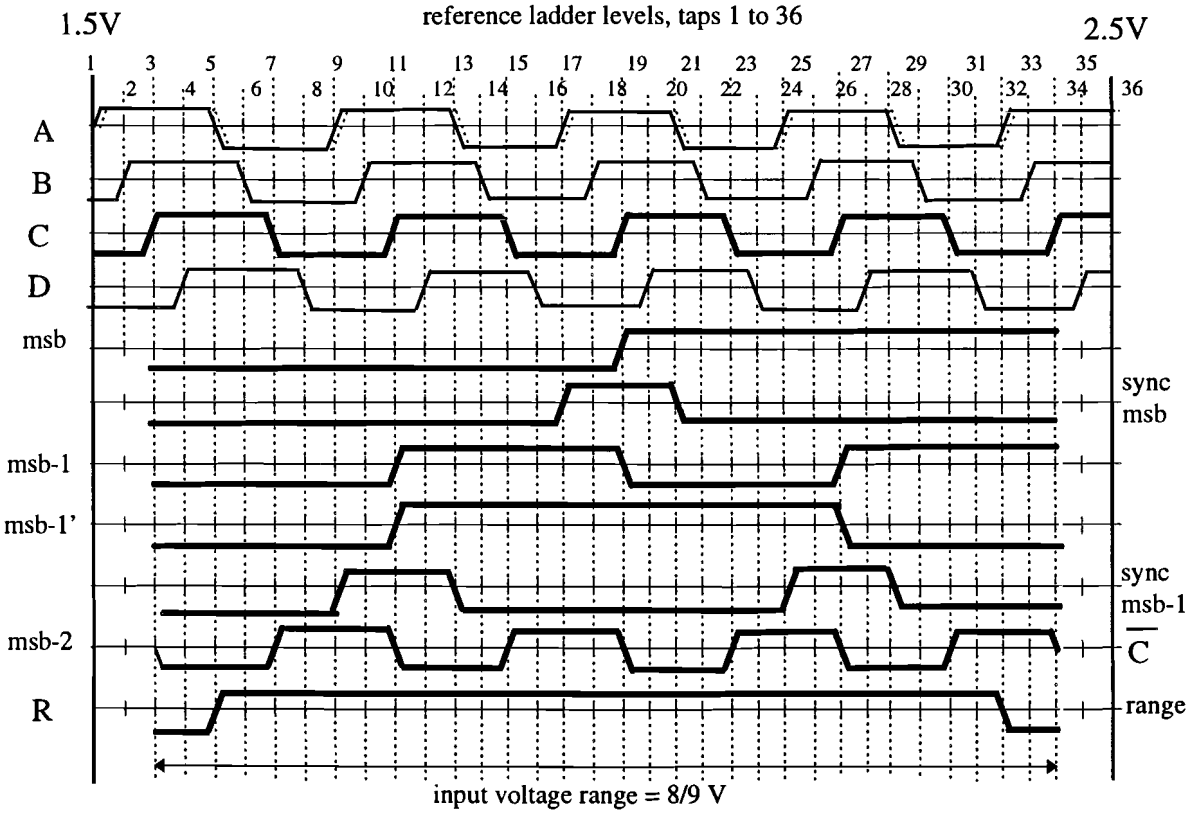


Figure 8.1 : Definition of the coarse folding signals

In nine folding signal A an example is given of the delayed folding signal A' due to fine folding path. This delay is essential for synchronizing the fine with the coarse part later on.

8.3 DESIGN COARSE FOLDING BLOCK

The implementation of the coarse folding block is performed in the same way as the fine folding circuit. The only difference is that the high current through the emitter follower in the three folding combination block isn't needed anymore. The outputs of the coarse folding block are coupled directly to the coarse comparators. The emitter current can be much lower now, which saves power. Omitting the emitter followers is not sensible, because the long wirering between the coarse folding block and the comparators.

In the discussion of the folding block already is mentioned that the folding factor always is odd. *Because their is always 'one' differential pair in its linear range, the remaining differentials pairs, which are out their linear range should equally distribute the tail currents over the load resistors.* In the scheme of the definition of the coarse signals (figure 8.1) there are some 'even' folding signals (sync msb, msb-1', sync msb-1 and range). Considering the low power constraint, a two (or even) folding block would be handy. This could save at least one tail current of a differential pair, but cannot realized with the coupling of two differential pairs. Keeping the signal delay for each coarse folding the same, the three folding block, as used in the fine circuit, is used here as two folding circuit. One input of the three folding block is biased in such a way that the tail currents of the not active differential pairs are equally distributed over the load resistors. The use of two voltage reference sources (vx and vx2) are needed in that way.

The MSB signal consists of one 0⇒1 transition. The use of only a 'one' folding amplifier, with the same tail current as the three folding stage, is permitted. The chip-area and the power of the coarse folding part can be reduced significantly. Compared to the conventional coarse folding scheme, a reduction of power of at least 460μW is obtained. With the use of 'one' folding amplifiers, the common-mode resistor R_{cm} should be adapted. The common-mode output voltage level should be the same as in the three folding amplifier. As example, a 'transformation' of the three folding block to a single differential pair is shown in figure 8.2 with the same common-mode voltage. The calculation of this R_{cm} in the differential pair also is given in this figure. The parameters of the 'one' folding coarse amplifier, needed at four places in the total coarse folding scheme (figure 8.3), are shown in table 11.

Table 11 : 'One' folding coarse amplifier parameters

Parameter	Value
transistor type	n10L24pm mult. 1
V_{bias9}	1.17 V
R_{bias9}	30 kΩ
I_{bias9}	13.2 μA
g_{m9fold}	0.25 mA/V
R_{cm2}	25.585 kΩ
R_{load}	15.385 kΩ
R_e	6.154 kΩ
V_{out}, V_{outc}	2.56 V
power consumption	39.6 μW @ V_{CC} = 3V
DC - gain	1.47
output swing (2*A)	400 mV

The 'original' three folding amplifier, as used in the fine folding circuit, remain the same in the coarse folding block. For the parameters of this three folding block used in the coarse folding part will be referred to table 6 of chapter 7.2.

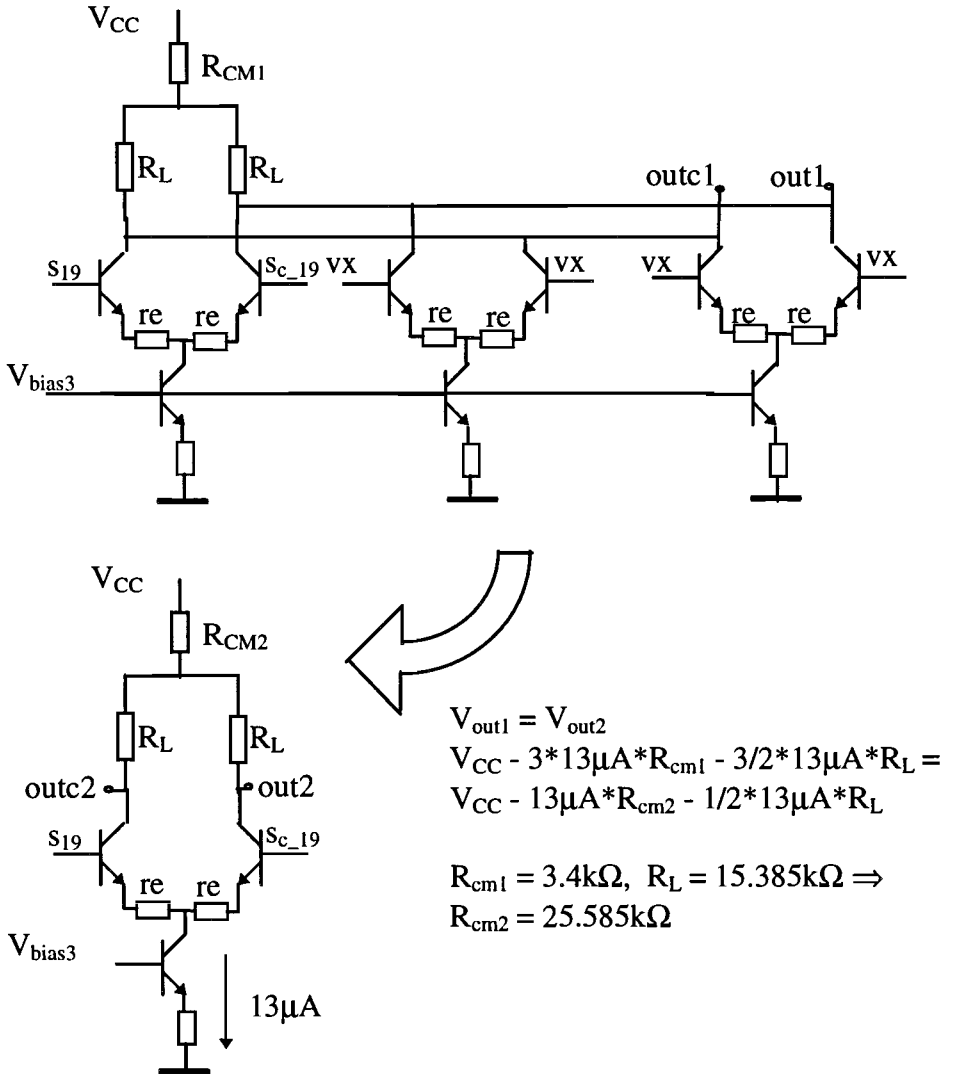


Figure 8.2 : Transformation of MSB 'three' folding block to MSB 'one' folding block

The implementation of the coarse *'one' folding combination block* can also be performed by omitting two cross-coupled differential pairs. The same common-mode output voltage level can now be established with the use of an extra R_{cm} in this circuit. In the three folding combination block, as used in the fine circuit, no common-mode resistor was needed. The value of this resistor, for an equal common-mode voltage at the output, can be obtained by taking $R_{CM} = R_L$. The current through the emitter followers can be reduced to the same current as through the differential pair in the folding block. The high current through the emitter followers in the fine circuit is not needed for the coarse folding block. The coarse folding block has only to drive the coarse-comparators.

In table 12a the parameters of this transformed 'one' folding combination block are listed. In the coarse folding block (see figure 8.3), there is 1 three folding combination coarse amplifier needed for generating the sync_mbs-1 signal.

The parameters of this three folding combination amplifier are shown in table 12b. The only difference with table 12a is that there is no common-mode resistor R_{cm} used in this circuit.

Table 12a: 'One' folding combination coarse amplifier parameters

Parameter	Value
transistor type	n10L24pm mult. 1
V_{bias9}	1.16 V
$R_{bias9} = R_{fol9}$	30 kΩ
$I_{bias9} = I_{fol9}$	13.67 µA
g_{m9fold}	0.25 mA/V
$R_{load} = R_{CM}$	16.5 kΩ
R_e	5.8 kΩ
V_{out}, V_{outc}	2 V
power consumption	123 µW @ $V_{CC} = 3V$
DC - gain	1.47
output swing (2*A)	400 mV

Table 12b: Three folding combination coarse amplifier parameters

Parameter	Value
transistor type	n10L24pm mult. 1
V_{bias9}	1.16 V
$R_{bias9} = R_{fol9}$	30 kΩ
$I_{bias9} = I_{fol9}$	13.67 µA
g_{m9fold}	0.25 mA/V
R_{load}	16.5 kΩ
R_e	5.8 kΩ
V_{out}, V_{outc}	2 V
power consumption	205 µW @ $V_{CC} = 3V$
DC - gain	1.47
output swing (2*A)	400 mV

In figure 8.3, the differential pair of the three folding block, which is not connected to an input gain stage, is connected to a bias DC-voltage vx - vx2. The voltage vx is set on 1.9V and vx2 on 2.1V.
The block diagram generating the coarse folding signals is depicted in figure 8.3.

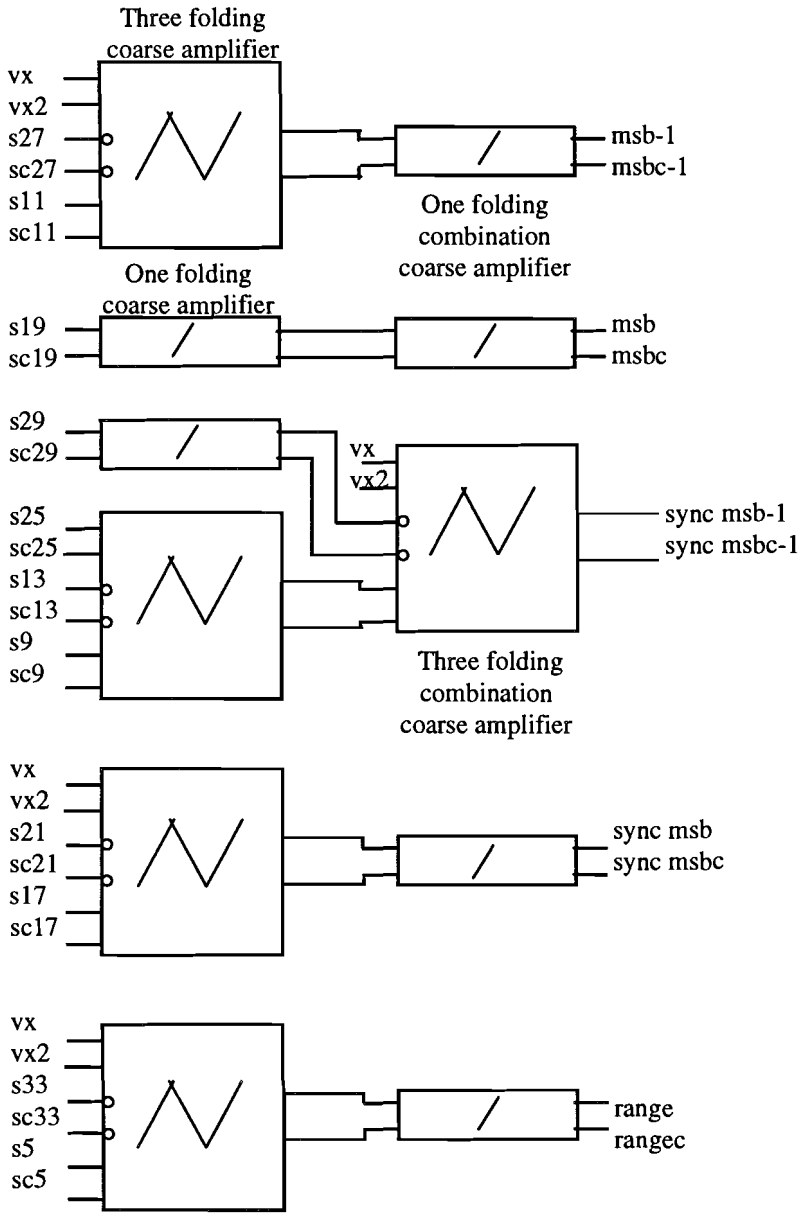


Figure 8.3: Coarse folding implementation

8.4 SIMULATION RESULTS OF THE COARSE FOLDING BLOCK

On the coarse folding block several simulations are done. The first simulation is to verify the correct folding of the coarse folding signals. In this simulation, the input signal is a ramp from 1.5V to 2.5V, which includes all the zerocrossings of the input gain stages. The result of this simulation is depicted in figure 8.4.

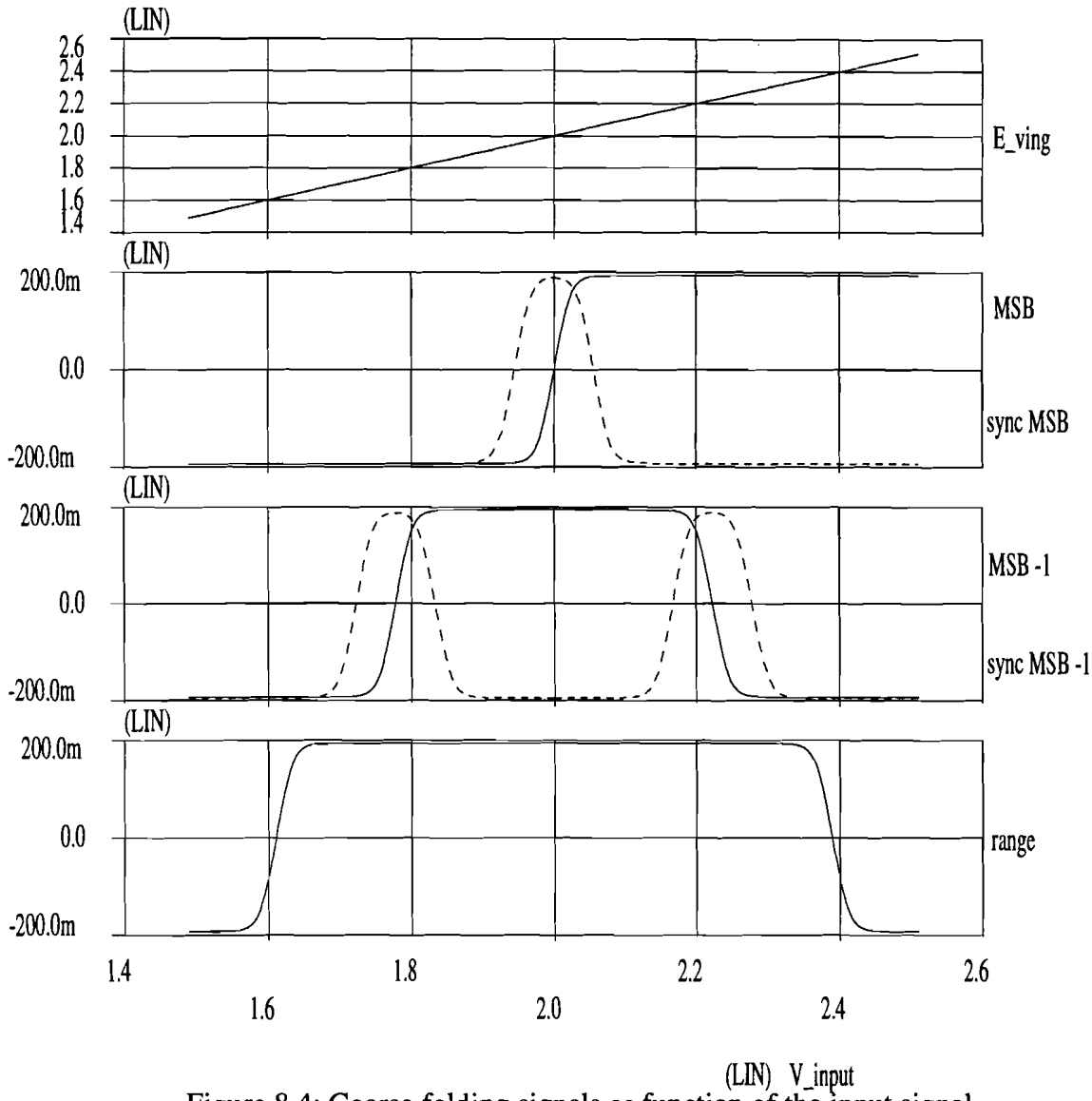


Figure 8.4: Coarse folding signals as function of the input signal

The output voltage swing of the coarse folding signals is the same as the fine folding block. By omitting some differential pairs in the three folding block, the bandwidth of the signals increases compared to the fine folding circuit. The bandwidth of the coarse folding block is minor of importance, because the influence of signal dependent delay is less. The way of folding is only chosen the make the propagation delay approximately the same as in the fine folding block.

The total power dissipation of the preprocessing part, including reference ladder, become 5.73mW with a power supply of 3V. The power needed for the biasing circuits is not included. In the following chapter the voltage reference circuits needed biasing the folding amplifiers are discussed.

9. PREPROCESSING BIAS CIRCUITS

9.1 INTRODUCTION

The tail currents of the input gain stages and folding blocks are controlled by a voltage V_{bias}. This voltage will be supplied by means of a temperature compensated reference source.
The question now rises; which voltage or current has to be stabilized with the temperature? When supplying a constant V_{bias}, the tail current of the current source will decrease with the temperature. For a proper operation of the preprocessing block, the most important parameters are a stabilized gain and output swing. Stabilizing the gain or outputswing is most different than stabilizing the tail current or V_{bias}. The relation between the Temperature Coefficient (TC) of the bias current and the TC of the load resistor results in a constant gain. The exact TC parameters for the temperature dependency are not available. Assuming that:

$$G = \frac{q \cdot V_{swing}(T)}{k \cdot T} \equiv constant$$

$$V_{swing}(T) = V_0 \left(1 + \chi \left(T - T_{ref}\right)\right)$$

The output swing of the differential pair is now proportional to the temperature. Stabilizing the gain is better than stabilizing the output swing. With a constant output swing the gain would be negative proportional to temperature, which is worse for the INL. Assuming that the temperature dependency function of the resistor and bias current can be written as:

$$R(T) = R_0 \left(1 + \alpha \left(T - T_{ref}\right)\right)$$

$$I_{bias}(T) = I_0 \left(1 + \beta \left(T - T_{ref}\right)\right) \Rightarrow$$

$$V_{swing}(T) = V_0 \left(1 + (\alpha + \beta)\left(T - T_{ref}\right) + \alpha\beta\left(T - T_{ref}\right)^2\right)$$

The output swing voltage derived above is only valid for differential pairs without feedback!

9.2 PARTITION FOR SEPARATE BIAS CIRCUITS

The matching of the subcircuits with each other, for a proper operation of the preprocessing part, is also an important key-factor. The voltage reference sources are split up into three parts; the input gain stage reference source, the three folding amplifiers reference source and the three folding combination reference source. The sub-blocks are all supplied with the same biasing voltage. The biasing voltage of the input gain stages is lower than the biasing voltage of the folding blocks, because the minimum voltage of the reference ladder is 1.5V.

With a tail current of 8μA, the V_{be} of the current source is approximately 760mV, so the V_{bias} in case cannot be higher than 1V. With a V_{bias} of 1V the base-collector voltage is maximum 240mV forward biased. The bias current needs to be adjustable and is controlled with the emitter resistor in the current source (see also the function $V_{be}(I_c)$ figure 6.13). An overview of the total biasing current to drive is shown in table 13:

Table 13: Overview biasing current sub-circuits for separate biasing blocks

sub-circuit preprocessing part	# in preprocessing	total biasing current
input gain stage	25	191.75 μA
input gain stage, with e-follower	11	95.15 μA
three folding block, coarse+fine	$12_{fine} + 4_{coarse}$	633.6 μA
one folding block, coarse	2	26.4 μA
three folding comb. block, fine	4	499.1 μA
three folding comb. block, coarse	1	68.35 μA
one folding comb. block, coarse	4	164.04 μA
Total biasing current preprocessing		1678.37 μA

The total biasing current is divided into three parts for three biasing circuits and is shown in table 14.

Table 14: Partition of the total biasing current over three biasing circuits

Biasing circuit to drive the	Total biasing current
Input gain stages	286.9 μA
Three folding blocks (fine + coarse)	660 μA
Three folding comb. blocks (fine + coarse)	731.47 μA

The total load current is defined as the total biasing current divided by the average β of 270. The V_{bias} can be higher for the three folding and three folding combination block than the input gain stages. The common mode input voltages for these blocks are 2.5V and 2V respectively. For the biasing circuits of the three folding and three folding combination blocks the same circuit is used.

9.3 IMPLEMENTATION OF THE BIASING CIRCUITS

The voltage reference source only uses NPN transistors and is built using the bandgap voltage of silicon as low-temperature dependent reference voltage. In this section, the voltage reference source is described which uses this bandgap principle. The basic idea behind the bandgap voltage stabilization is the following: With an increasing temperature it is known that the base-emitter voltage of a transistor decreases with increasing temperature. At the same time, the positive temperature coefficient of the current source generates a voltage across a resistor R, which increases linearly with the temperature. The decrease in base-emitter voltage, in that case, is compensated by the increase in the voltage across the resistor R. In figure 9.1 an implementation form of a voltage reference source that uses only NPN transistors is shown. The circuit consists of a cross-coupled quad transistor unit (T1,T2,T3,T4) and the current converting resistor R_1. Transistor T2 and T4 have a respectively m2 m4 times larger emitter area than the other transistors. The current I_2 is

flowing through R_1, T2 and T3 can be expressed in the following parameters of the quad unit: $I_{R1} = \frac{kT}{qR_1}\ln(m2 * m4)$

Transistors T6 and T7 act as a buffer and makes the variation of the current through R_3 more independent with supply voltage V_{CC} variations.

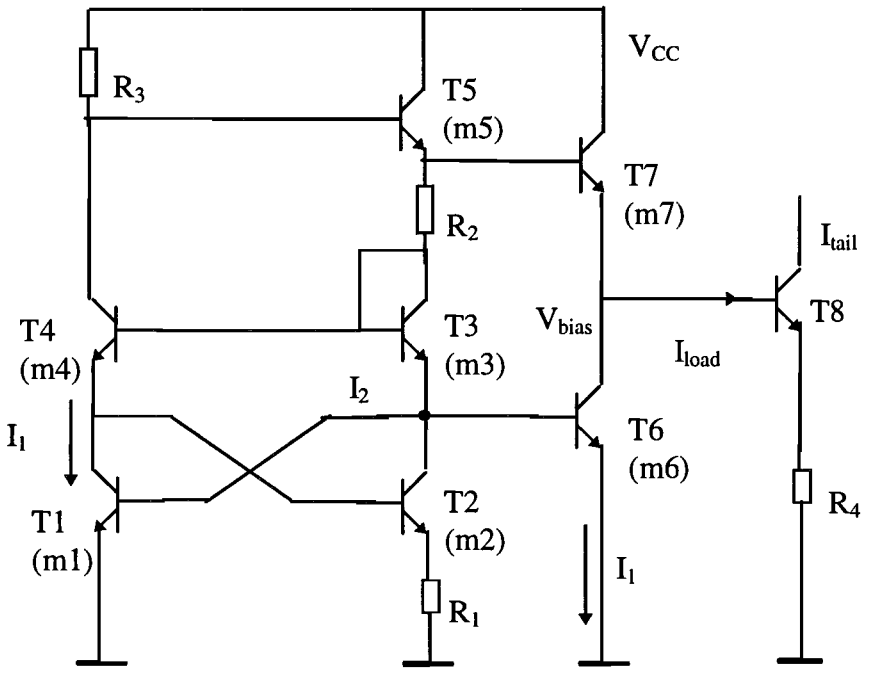


Figure 9.1 : Voltage reference source for biasing the preprocessing part

The current I_1 is supplied by resistor R_3 to the circuit, and has no influence on the current I_2. Resistor R_2 is added to the circuit to obtain an adjustable, within certain ranges, output voltage V_{bias}. Transistor T6 has the same base voltage as transistor T1, so the collector current through T6 (with m6=m7=1) is the same as through transistor T1. The output voltage V_{bias} can be expressed as:

$$V_{bias} = V_{be1} + V_{be3} + V_{R2} - V_{be7}$$

$$V_{be1} = V_{be7}$$

$$V_{bias} = V_{be3} + I_2 \cdot R_2 = V_{be3} + \frac{R_2}{R_1} \cdot \frac{kT}{q} \cdot \ln(m2 * m4)$$

Making $V_{be1} = V_{be7}$ is allowed here, because the current flowing through T6 is also flowing through T7. With the ratio R2/R1 the TC of V_{bias} can determined for a constant gain. The temperature dependence of the resistor R2 and R1 is canceled, when the TC of the resistors are the same, with this expression. V_{be3} has a negative TC and the second term is proportional to T. The biasing current to drive is given in table 14 and with a β of approximately 200, the I_{load} is approximately 1μA. The corrected voltage V_{bias} for this I_{load} is given by:

$$V_{bias} = \frac{k\,T}{q} \cdot \ln\left(\frac{I_1 . I_2}{I_s \cdot \left(I_1 + I_{load}\right)} \right) + \frac{R_2}{R_1} \cdot \frac{k\,T}{q} \cdot \ln\left(m2 * m4\right)$$

The parameter setting for a constant gain of the input gain stage is shown in table 15.

Table 15: Parameter setting for the input gain stages voltage reference source

Parameter	Value
transistor type	n10L24pm
m1, m3, m5	mult. 1
m2, m4	mult. 5
m6, m7	mult. 4
R1	15 kΩ
R2	40 kΩ
R3	100 kΩ
I_1	4 µA
I_2	5.58 µA
I_{load}	≈ 1 µA
V_{bias}	990 mV
Power consumption	76.74 µW

The current I_1, in transistor T6 is multiplied by 4 through the mult. factor m6. The collector current through this transistor equals now about 16 µA. With these parameter settings for the reference voltage source, the gain of the input stage varies .25% in a temperature range from -20° to +80° C. The result of this simulation is shown in appendix E. The V_{bias} varies -1.025 mV/°C.

The same voltage reference circuit is designed for biasing the folding blocks. The only differences with these circuits are the higher V_{bias} and the higher total bias current to drive. The voltage reference source for the three folding block and the three folding combination block will not vary a lot. For the sake of completeness, the parameter settings of these two circuits are shown in table 16 and 17.

Table 16: Parameter setting for the three folding block voltage reference source

Parameter	Value
transistor type	n10L24pm
m1, m3, m5	mult. 1
m2, m4	mult. 5
m6, m7	mult. 2
R1	15 kΩ
R2	70 kΩ
R3	53.85 kΩ
I_1	6.02 µA
I_2	5.98 µA
I_{load}	≈ 2.42 µA
V_{bias}	1167 mV
Power consumption	72.12 µW

Table 17: Parameter setting for the three folding comb. block voltage reference source

Parameter	Value
transistor type	n10L24pm
m1, m3, m5	mult. 1
m2, m4	mult. 5
m6, m7	mult. 2
R1	15 kΩ
R2	70 kΩ
R3	50 kΩ
I_1	6.02 μA
I_2	5.98 μA
I_{load}	≈ 2.81 μA
V_{bias}	1167 mV
Power consumption	72.12 μW

All the current biasing in the preprocessing block is performed with these three circuits. The total power consumption of the three circuits is 221μW @ V_{CC} = 3V. Exact temperature calculations for a constant gain at the output of the folding circuits are not performed in this thesis. The constant is gain is only verified through simulations.

9.4 POWER CONSUMPTION TOTAL PREPROCESSING PART

All the circuits in the preprocessing part are now designed and verified through simulations. In table 18 the total power consumption of the preprocessing part, including biasing circuits and reference ladder network, is given. The single power supply voltage of 3V is the minimal voltage to supply the whole ADC. Lowering this V_{CC} voltage gives problems in designing the biasing circuits and the comparators.

Table 18 : Power distribution of total analog preprocessing of folding ADC

Power consumption @ V_{CC} = 3 V	Value [μW]
Reference ladder network	694.45
Input gain stages	860.70
Fine folding circuits	2922.84
Coarse folding circuits	1251.57
Voltage reference circuits	221.00
Total power preprocessing part	**5950.55 μW**

The fine folding block includes the three folding and three folding combination circuits. The coarse folding block is designed with some (# 6) 'one' folding blocks, which reduces the power approximately 470μW (#6 x 2 x 13μA x 3V).
All these values are obtained by simulation results at a temperature of 27° C !!.
In the total circuit, additional interconnect -, cross - and wirering capacitance are not included with these simulations! In the following chapter the layout of the preprocessing part is discussed.

10. LAYOUT DESIGN OF PREPROCESSING BLOCK

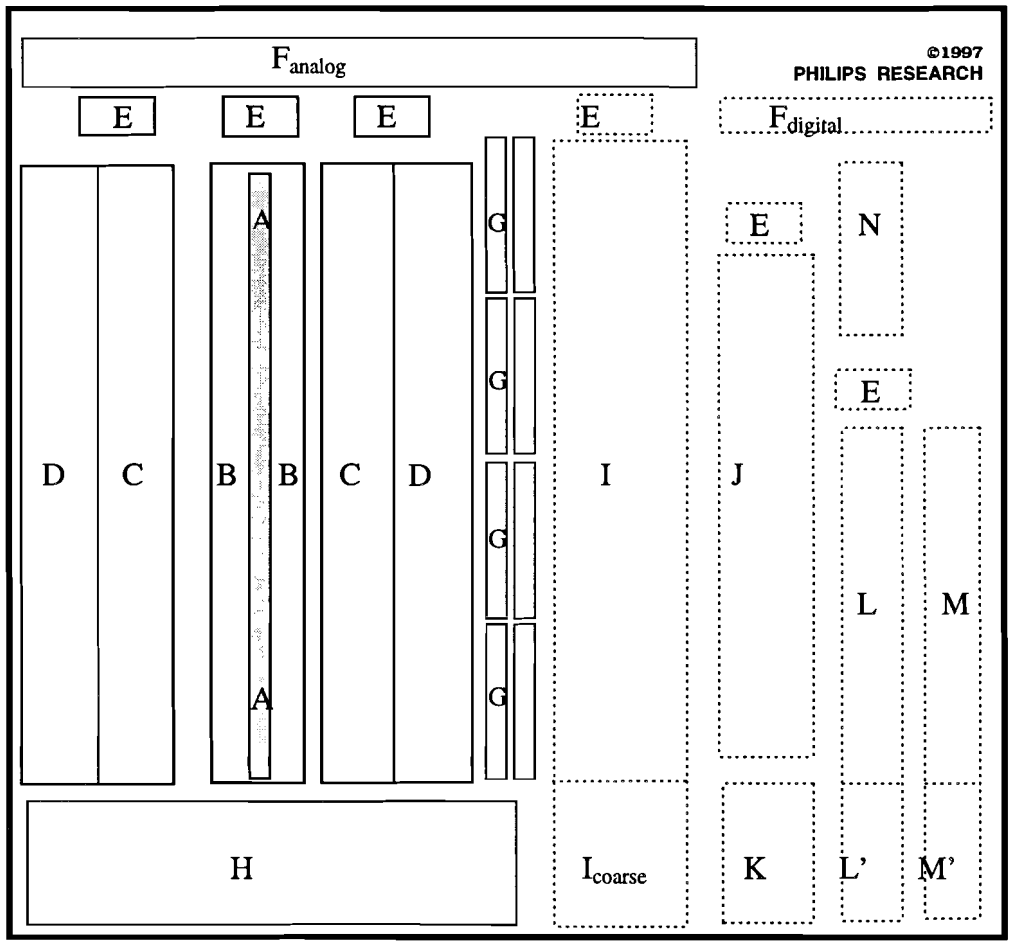
10.1 PLACEMENT CONSIDERATIONS

In this chapter, the strategy of the layout design is discussed. The ADC will be integrated in a one metal layer bipolar SPIRIT process. The design of the floorplan of the preprocessing block is given in this chapter. In the placement the following considerations were made:

- The orientation of the transistors which need a good matching, as the transistors in a differential pair for example, are placed in the same direction as close as possible to each other.
- In the three folding blocks, the orientation of the cross-coupled differential pairs are placed in the same direction, for the best matching considerations.
- The layout of the subcircuits are implemented in such a way that by stacking the circuits, the leads V_{CCA}, V_{SSA} and V_{bias} automatically are connected with each other. This gives the most compact layout of the preprocessing part.
- Cross-resistors (dummy resistors) are only used in the high impedant connection leads, and if this is not possible the resistor value is deducted with the other resistors to preserve a symmetric circuit
- The wires between the input gain stages and the reference ladder should be as short as possible, with equals length and width to obtain a low serie resistance. Therefore the 36 input gain stages are split up into two parts (even /odd) 18 input gain stages.
- The tail current sources wires to the bias circuits should be as short as possible. Long wires to the bias circuits give a considerable voltage drop across the leads due to the I_{load}.
- The reference ladder is implemented with low ohmic 'BN'- resistors. These resistors have better matching properties than the 'PSS'- resistors. The BN-resistors are relatively wide for a 40Ω tap resistor. A disadvantage is the increase of the parasitic capacitance, but good matching is most important for the reference ladder.
- The analog power supply V_{CCA} and the digital power supply V_{CCD} are separated implemented. On-chip there are no internal connections. The preprocessing part (with including biascircuits), the input stage and master comparators will be supplied with the V_{CCA}, the other circuits are supplied with V_{CCD}.

10.2 FLOORPLAN TOTAL ANALOG-TO-DIGITAL CONVERTER

For the time being, a floor plan of the ADC is given in figure 10.1. Possible modifications in the floorplan can be made when the layout of all the sub-circuits of the digital part are designed. The best floorplan, with the correct dimensions, can then be designed.



Contents of the blocks:
A. reference ladder
B. input gain stages
C. three folding stage
D. three folding comb.
E. bias circuit
F. supply rails
G. interpolation
H. coarse folding
I. comparators
J. rom table
K. bitsync
L. latches
M. output stages
N. clock driver

Figure 10.1 : Floorplan of the folding ADC

10.3 LAYOUT DESIGN OF THE PREPROCESSING CIRCUITS

In the bipolar SPIRIT process, there is officially one metal layer available. Because of the 'low frequency' operation of the ADC an additional metal layer can be used. With this second metal, originally spiral inductors are made. The second metal (metal2) is twice as wide as metal1. The width of metal1 is 1.5μm. The needed via's (metal1 with metal2) are at least 9μmx9μm and the spacing between metal2 is also 9μm. This puts a restraint on the minimal chip dimensions of the sub-circuits. The three leads, V_{CCA}, V_{SSA} and V_{BIAS} are placed vertically (in metal2), so stacking of the subcircuits is possible. Since offsets in the reference ladder directly result in non-linearity errors of the ADC, in the layout wide "BN" resistors are used. The sheet resistance of the BN-resistor is about 22 Ω/ . For a perfect symmetry wide resistors are needed. With the medium ohmic "PSS" resistor the tap resistor of 40 Ω are too small for a proper matching. The reference ladder is stretched over the length of the 18 input amplifiers. The leads to the input gain stages are so as short as possible. A layout with 36 stacked input gain stages gives too long interconnection leads

from amplifiers to the ladder. Spreading the ladder resistors over the total length of 36 amplifiers is not sensible, because the width of the tap resistor is too great and causes too much parasitic capacitance.

The problem with this floorplan in figure 10.1 is the long interconnection leading from the three folding combination block (fA and fC) to the interpolation ladder. These leads can be longer than normally, because the use of emitter followers in the three folding combination circuits.

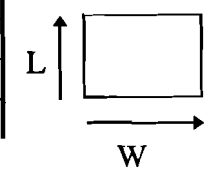
The input gain stages are placed alternating around the reference ladder. On the left side of the ladder the odd input gain stages are placed, with the nine folding signals fA and fC. From this side of input gain stages all the interconnections to the coarse folding block are made. Most interconnections to the coarse folding block are made from the nine folding signal fA. Therefore, the coarse folding block is placed under the fine folding block. Between the odd input gain stages and the three folding blocks additional space is left open for the wirering matrix to the coarse folding blocks. This wirering matrix is carried out in metal1 (width 1.5μm). The width between the input gain stage blocks and three folding blocks is now minimal 11 x 3μm. Moreover, the subcircuits layout realization is shown in appendix C.

The interconnect capacitance to ground is approximately 50aF/μm!. An interconnect line of length 100μm adds 5fF capacitance to the node in the total layout!! A 5fF capacitive load for the circuits is very high. The simulated power dissipation of the preprocessing part shall be, through these capacitance, higher than first was assumed. At the moment of writing this report, not all the wirering and cross capacitance were known. The layout of the preprocessing is not extracted with CAD-tools. With these CAD-tools, from the extraction a net-list is returned including all interconnect capacitance and cross capacitance's. A simulation of the total circuit with these capacitance's gives a more realistic overview of the performance of the preprocessing part. The performance of the preprocessing part will decrease as a result of these capacitance: especially the third-order distortion will become dominant for the ADC's performance at high frequency operation. The bandwidth of the preprocessing shall also reduce due to these capacitance. The maximum input signal frequency of the ADC, able to convert with an eight bit accuracy, shall be reduced. This loss in bandwidth can be reduced by increasing the bias current in the preprocessing circuits. Exact simulations on the layout of the preprocessing are not performed in this thesis!

The layout of the subcircuits are shown in appendix C. In the subcircuits dummy resistors, needed for a compact layout realization, are taken into account. The dimensions of the folding subcircuits are depicted in table 19:

Table 19: Layout dimensions of the folding subcircuits

subcircuit preprocessing part	dimensions in μm W	L
input gain stage	53	53.4
input gain stage with e-followers	71.2	71.7
three folding block fine/coarse	51.8	134.5
three folding combination block fine/coarse	68	119.1



11. CONCLUSIONS AND RECOMMENDATIONS

The preprocessing part of the ADC has been designed. Considering the design constraints, given in chapter 2, the following can be concluded:

- A summarize of the *simulated* characteristics of the preprocessing block of the ADC:

System architecture ADC	Cascaded folding with 8 times interpolation
Resolution	8 bit
Input voltage range	8/9 V
Bandwidth preprocessing part	500 MHz
Maximum analog input signal frequency	50 MHz
Maximum gain at zerocrossings	8
Maximum output voltage swing (2*A)	400 mV
Integral non linearity (INL)	< ±0.3 LSB
Max. distortion component @ f_{in} = 50MHz	-55 dB
Power supply voltage	3 V
Total power dissipation preprocessing part	5950.55 μW

- The preprocessing part consists of: reference ladder with input gain stages, cascaded fine folding circuits, interpolation ladder, coarse signal generation and biascircuits
- SPIRIT is a specialized advanced bipolar RF technology with very small parasitic capacitance
- The ADC could not be implemented with other digital (receiver) circuitry on one chip: Multi Chip Modules!! This is a disadvantage of the technology. The costs of the technology are relatively high compared with CMOS technologies
- The technology roadmap of SPIRIT is unclear at the moment
- With the standard bipolar circuits, high linearity is obtained in the ADC preprocessing part due to good matching of the small transistors. In the total preprocessing part design, no special offset-cancellation or error-correction techniques are used. With the ordinary standard bipolar circuits, the linearity stays within the specified ranges
- The low power dissipation of the ADC is the main advantage of this technology in comparison with other state-of-art technologies (Bipolar or even CMOS)
- The power dissipation of the preprocessing part accounts 6mW @ V_{CC} = 3V. This number includes the power dissipation of the reference ladder and biasing circuits. An estimation of the total power dissipation of the ADC is about 30mW!. This result is based on the first simulations of the digital part, including comparators, rom table, latches and synchronizing circuits. With a clock frequency of 100MHz, this result is very promising for implementation of the ADC. The initial design specification of 6-9mW is based on the earlier transistor parameters fabricated at Philips Research. The assumption of a factor 3 to 4 higher power dissipation is permitted in comparison with the 'old' technology.

For further research on the ADC in this advanced bipolar technology, the following recommendations can be stated:

- The original 'Nat.Lab.' transistors parameters should be better implemented in the IC-Lab in Hamburg. With the Nat. Lab. transistors the total power of the ADC can be reduced by a factor 4 with the same bandwidth of 500MHz
- It is possible to enlarge the input range to 1V instead of 8/9V. The minimum reference voltage level must now be 1.44V and the maximum reference level 2.55V. A disadvantage is that the signal dependent delay is depended of the voltage input range and the bandwidth of 500MHz may not be enough
- The three folding stategy can be changed by taking the one folding signals in the three folding block together as: { (j, j+4, j+8), (j+12, j+16, j+20), (j+24, j+28, j+32) } $j \in [1,4]$ instead of the presented three folding technique in this thesis (see also appendix A). The only advantage of this folding technique is that the layout could be more compact. DC-simulations on the INL show no difference with the presented technique
- Not investigated in this report are the effects of the device mismatch by connecting the differential stage together as described in [19]. A correct ratio between R2/R1 can reduce the non linearity error in the folding ADC
- A different interpolation approach can be investigated by not interpolating 8 times at once, but splitting up the interpolation into 2 x 4. Because of interpolating two times no errors are made due to the symmetry in the folding signals. So, the errors can further be reduced by interpolating 2 x 4 times, because now there are three interpolated signals which do not have any interpolation error

Overviewing the total preprocessing part of the ADC the specifications are very promising for the rest of the ADC design. With standard bipolar techniques, very linear low power circuits can be realized, without special offset cancellation techniques. For the final specifications of the total ADC design will be referred to the graduation report of Roland van Wegberg.

12. ACKNOWLEDGE

I specially want to thank prof. dr. ir. R.J. van de Plassche for giving me the opportunity to fulfil my graduation project at the University and Philips Research. Also I want to thank my supervisors at the University, ir. G.G. Persoon and dr. ir. D.M.W. Leenaerts for their useful comments. At Philips Research, I also want to thank ir. T. Wagemans for the information he gave me about the IC process, where the chip has to be implemented in and the support with the development of the layout. The simulations for INL / distortions calculations could not be achieved without the software tool developed by ir. A.G.W. Venes. Finally, I wish to thank all the other members of the Research Group headed by ir. A. Sempel and the members of the group SES at the University, who have been supported my project.

Eindhoven, June 1997

John Compiet

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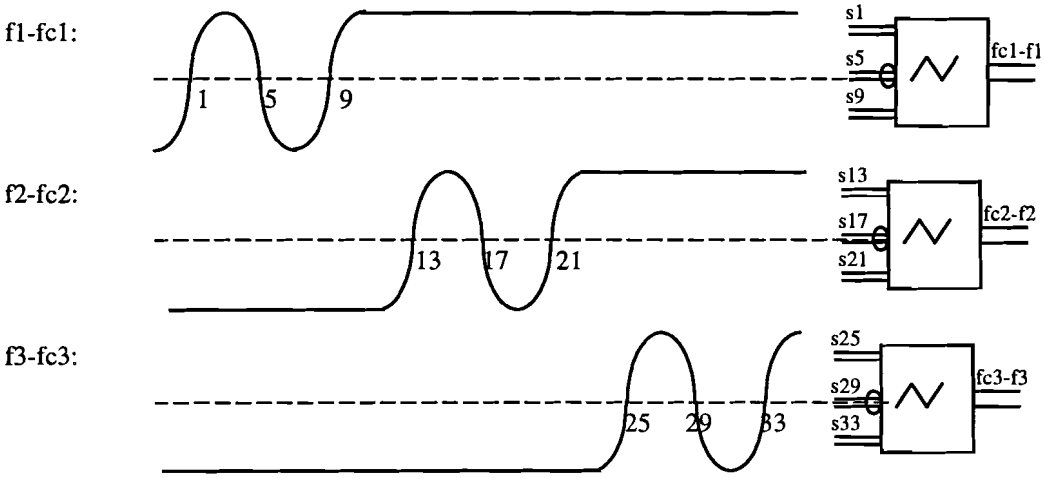
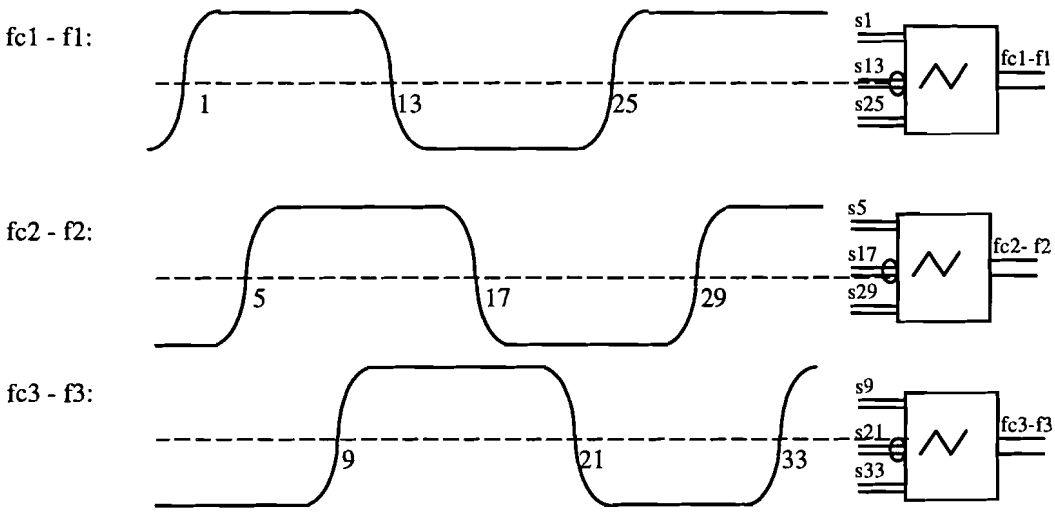
Appendix A: CASCADED FOLDING PRINCIPLE

12 'three' folding signals (f_1.. f_{12})

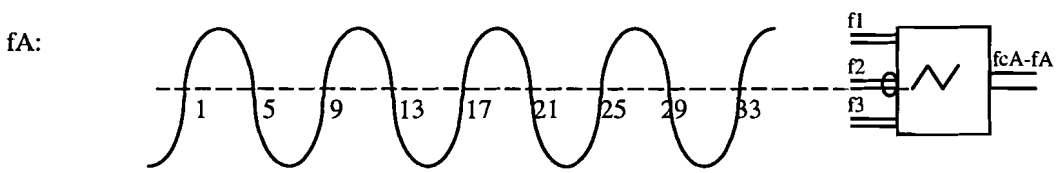
possibility one:



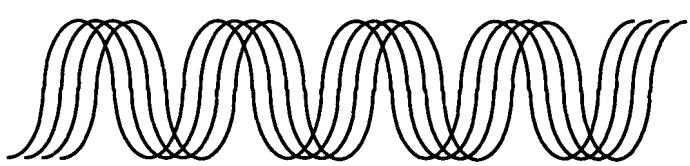
possibility two (used in ADC preprocessing part):



the combination of these three folding signals forms one differential nine folding signal



4 differential nine folding signals (A, B, C, D):
fcA-fA, fcB-fB, fcC-fC, fcD-fD

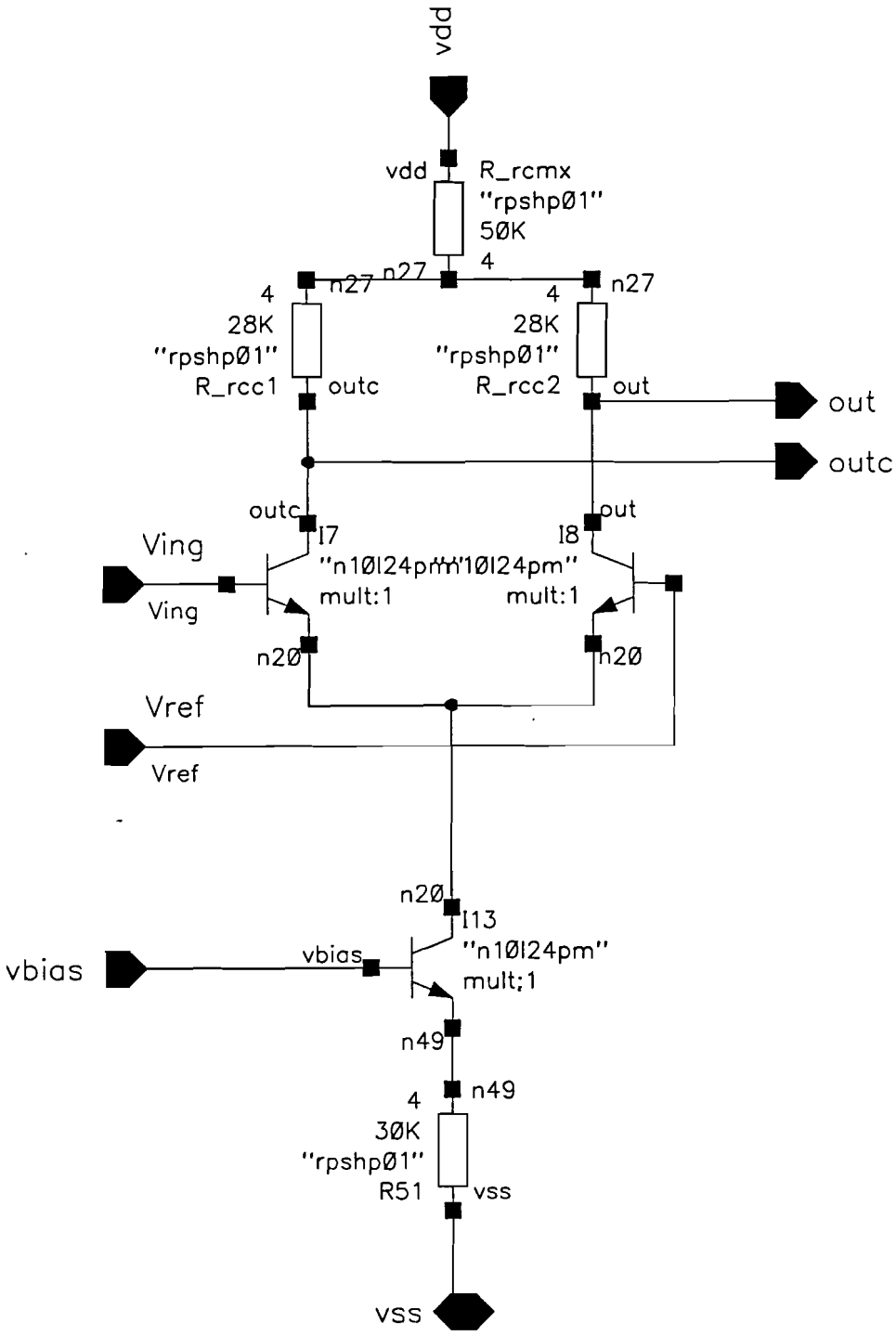


Appendix B

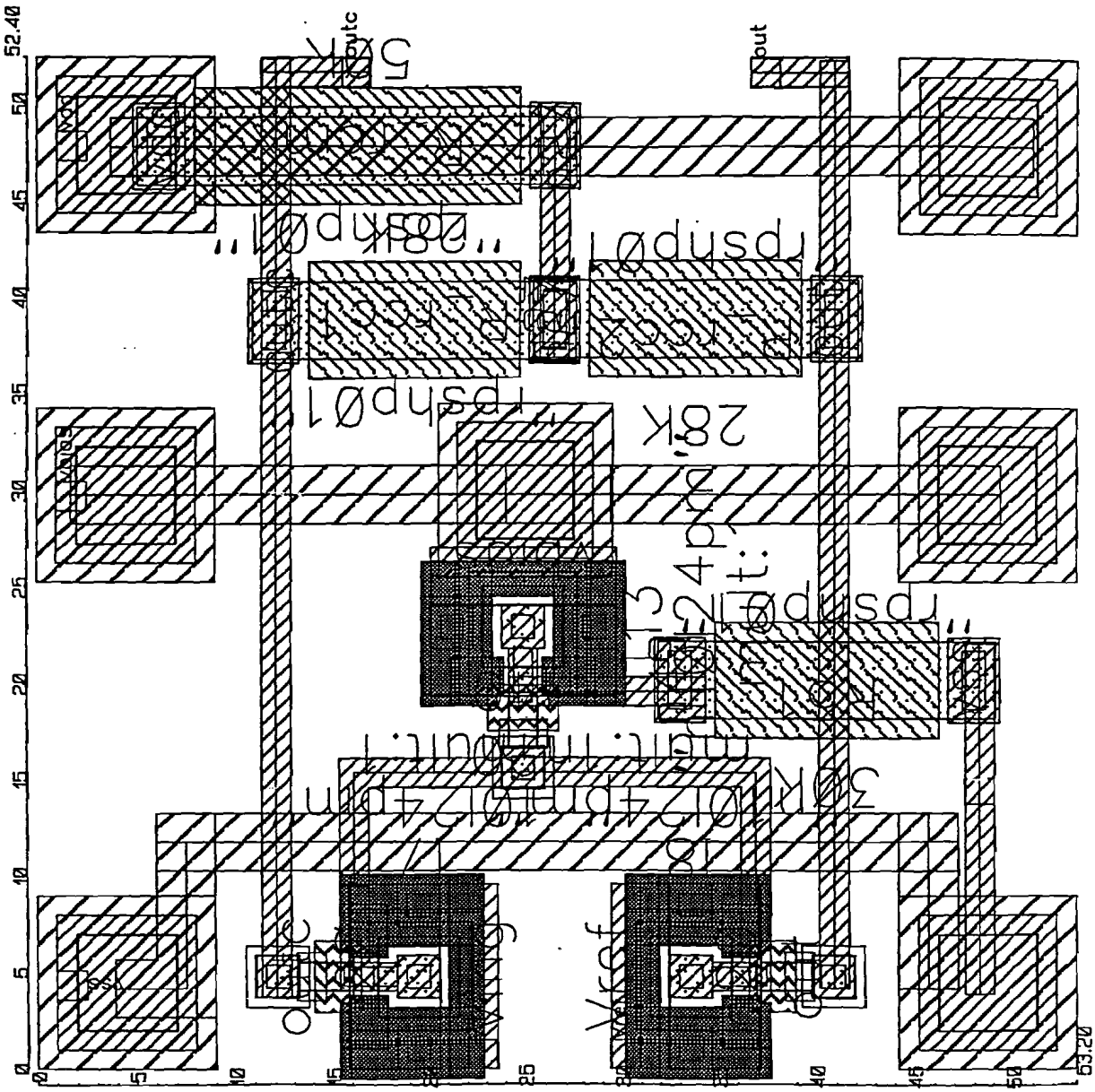
Transistor parameters in SPIRIT

```
          * !! VERY PRELIMINARY PARAMETER SET FOR SPIRIT NPN !!

TYPE: 'N10L24PM'

LEVEL  =   503.0000,     EXMOD  =     1.0000,     EXPHI  =     0.0000,
EXAVL  =     1.0000,     IS     = 1.6000E-18,     BF     =   356.9000,
XIBI   =     0.0000,     IBF    = 1.1500E-15,     VLF    =     0.4510,
IK     = 1.0000E-03,     BRI    =    35.3300,     IBR    = 6.2500E-16,
VLR    =     0.2650,     XEXT   = 5.0000E-02,     QBO    = 6.5100E-15,
ETA    =     3.0000,     AVL    =    32.2800,     EFI    =     0.8353,
IHC    = 2.8000E-04,     RCC    =    66.6500,     RCV    = 5.4880E+03,
SCRCV  = 1.2350E+05,     SFH    =     8.0000,     RBC    = 1.1120E+03,
RBV    = 3.3333E+03,     RE     =   444.5000,     TAUNE  = 1.5000E-12,
MTAU   =     1.0000,     CJE    = 1.2400E-15,     VDE    =     0.8000,
PE     =     0.3300,     XCJE   =     0.0000,     CJC    = 3.2500E-16,
VDC    =     0.6960,     PC     =     0.5000,     XP     =     0.1251,
MC     =     0.3000,     XCJC   =     0.2040,     TREF   =    25.0000,
DTA    =     0.0000,     VGE    =     1.1290,     VGB    =     1.2060,
VGC    =     1.1200,     VGJ    =     1.1290,     VI     = 2.0000E-02,
NA     = 2.0000E+17,     ER     = 2.0000E-03,     AB     =     1.0000,
AEPI   =     1.9000,     AEX    =     0.3100,     AC     =     0.2600,
KF     = 2.0000E-16,     KFN    = 2.0000E-16,     AF     =     1.0000,
ISS    =     0.0000,     IKS    =     1.0000,     CJS    =     0.0000,
VDS    = 5.0000E-02,     PS     = 1.0000E-02,     VGS    =     0.1000,
AS     =     0.0000,
CBC    = 2.0200E-16,     CBE    = 1.3000E-15,     CBG    = 1.0700E-15,
CCE    = 4.8700E-16,     CCG    = 4.7000E-16,     CEG    = 5.6000E-16;

Transistor model definition part;

MODEL: TNSM  (C, B, E, S)
   LEVEL,MULT,TREF,DTA,EXMOD,EXPHI,EXAVL,IS,BF,XIBI,IBF,VLF,IK,
   BRI,IBR,VLR,XEXT,QBO,ETA,AVL,EFI,IHC,RCC,RCV,SCRCV,SFH,RBC,RBV,RE,
   TAUNE,MTAU,CJE,VDE,PE,XCJE,CJC,VDC,PC,XP,MC,XCJC,VGE,VGB,VGC,VGJ,VI,
   NA,ER,AB,AEPI,AEX,AC,KF,KFN,AF,ISS,IKS,CJS,VDS,PS,VGS,AS,CBC,CBE,CBG,
   CCE,CCG,CEG;

      C_BC (C,B)    CBC*MULT;
      C_BE (E,B)    CBE*MULT;
      C_BG (S,B)    CBG*MULT;
      C_CE (E,C)    CCE*MULT;
      C_CG (S,C)    CCG*MULT;
      C_EG (E,S)    CEG*MULT;

      TNS_1 (C,B,E,S)

LEVEL=Level,MULT=MULT,TREF=TREF,DTA=DTA,EXMOD=EXMOD,EXPHI=EXPHI,EXAVL=EXAV
L,IS=IS,BF=BF,XIBI=XIBI,IBF=IBF,VLF=VLF,IK=IK,BRI=BRI,IBR=IBR,VLR=VLR,XEXT
=XEXT,QBO=QBO,ETA=ETA,AVL=AVL,EFI=EFI,IHC=IHC,RCC=RCC,RCV=RCV,SCRCV=SCRCV,
SFH=SFH,RBC=RBC,RBV=RBV,RE=RE,TAUNE=TAUNE,MTAU=MTAU,CJE=CJE,VDE=VDE,PE=PE,
XCJE=XCJE,CJC=CJC,VDC=VDC,PC=PC,XP=XP,MC=MC,XCJC=XCJC,VGE=VGE,VGB=VGB,VGC=
VGC,VGJ=VGJ,VI=VI,NA=NA,ER=ER,AB=AB,AEPI=AEPI,AEX=AEX,AC=AC,KF=KF,KFN=KFN,
AF=AF,ISS=ISS,IKS=IKS,CJS=CJS,VDS=VDS,PS=PS,VGS=VGS,AS=AS;
```

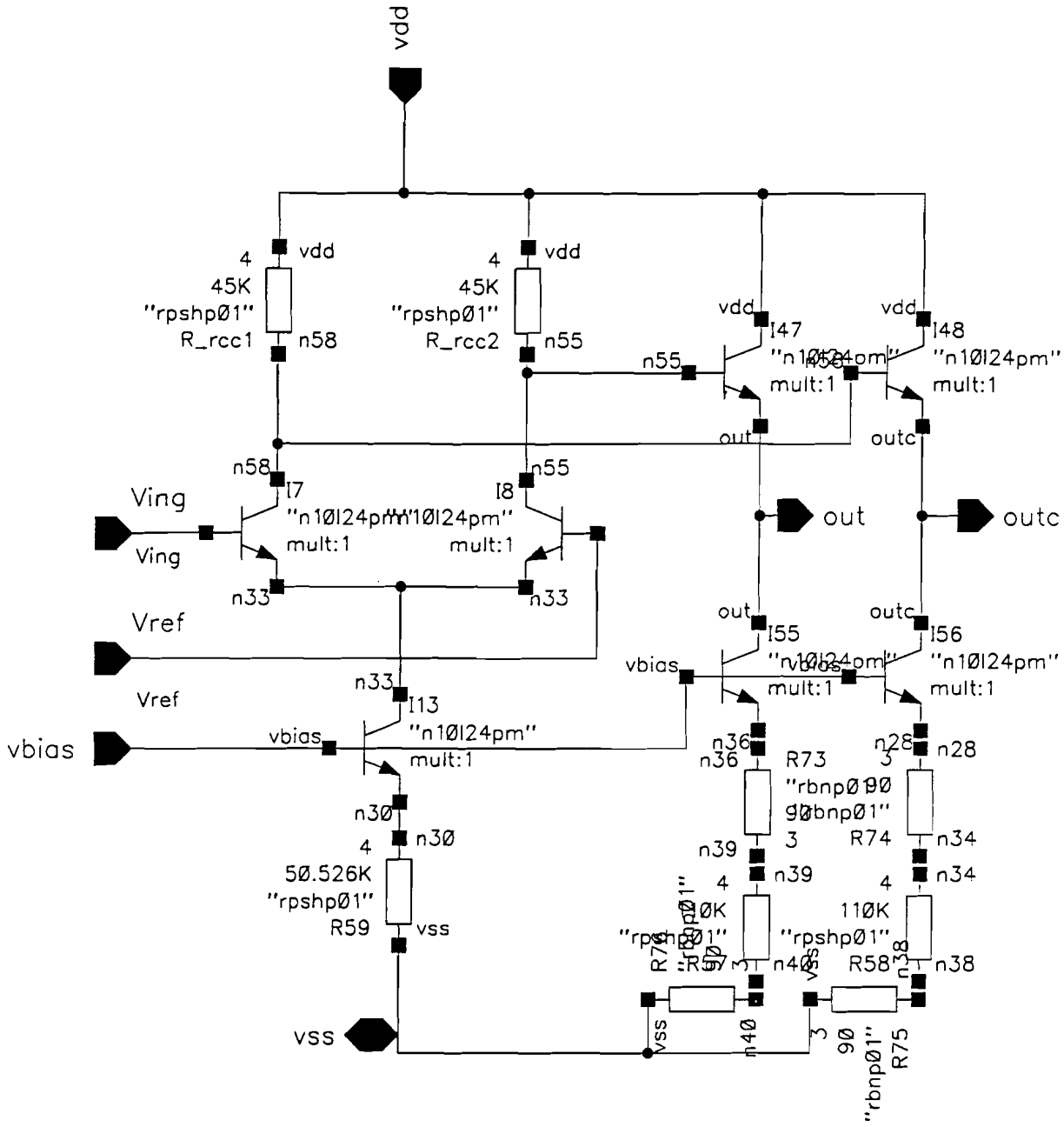
Appendix C: Schematics / layout of the fine and coarse folding circuits



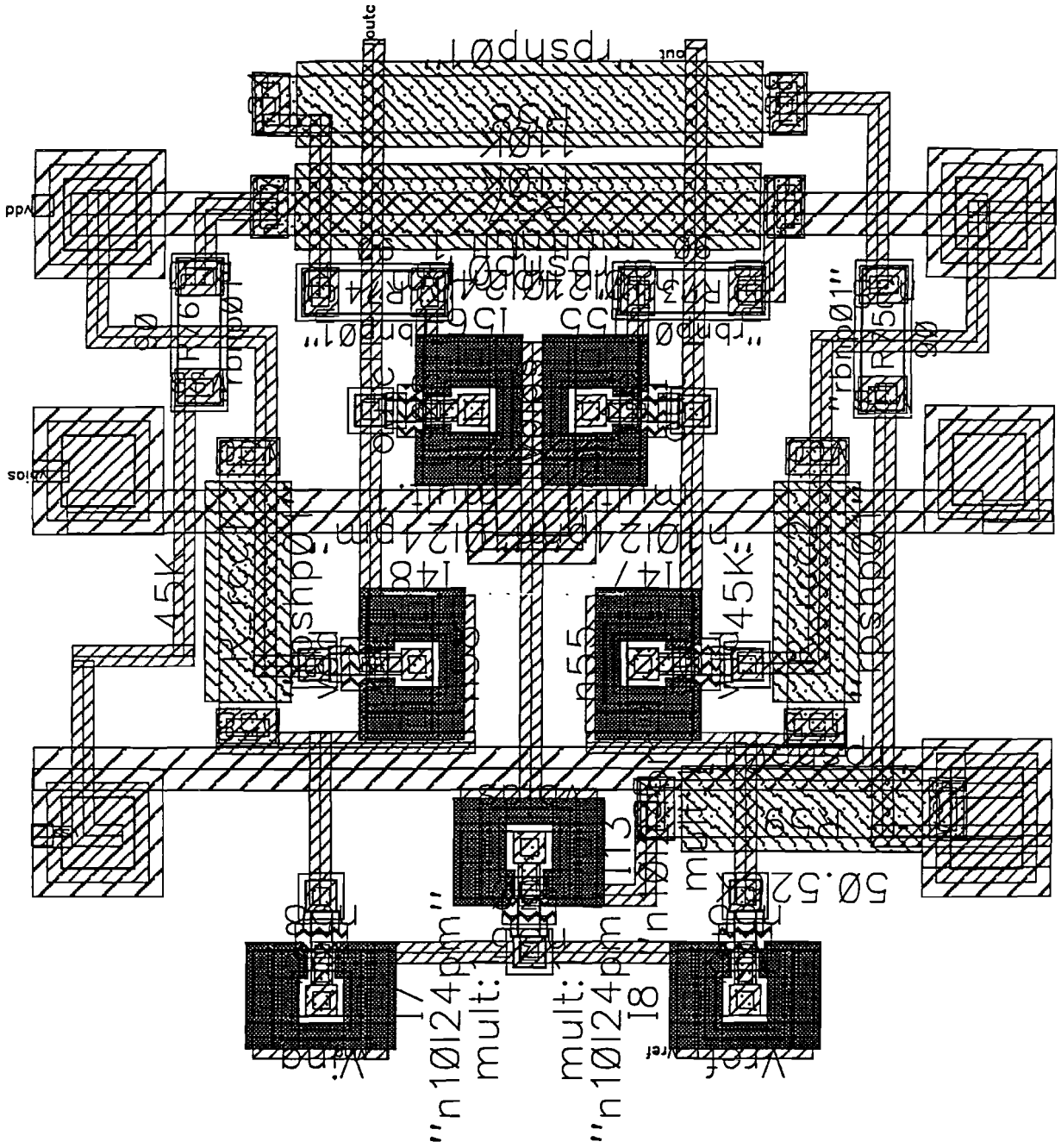
input gain stage 1: Schematic



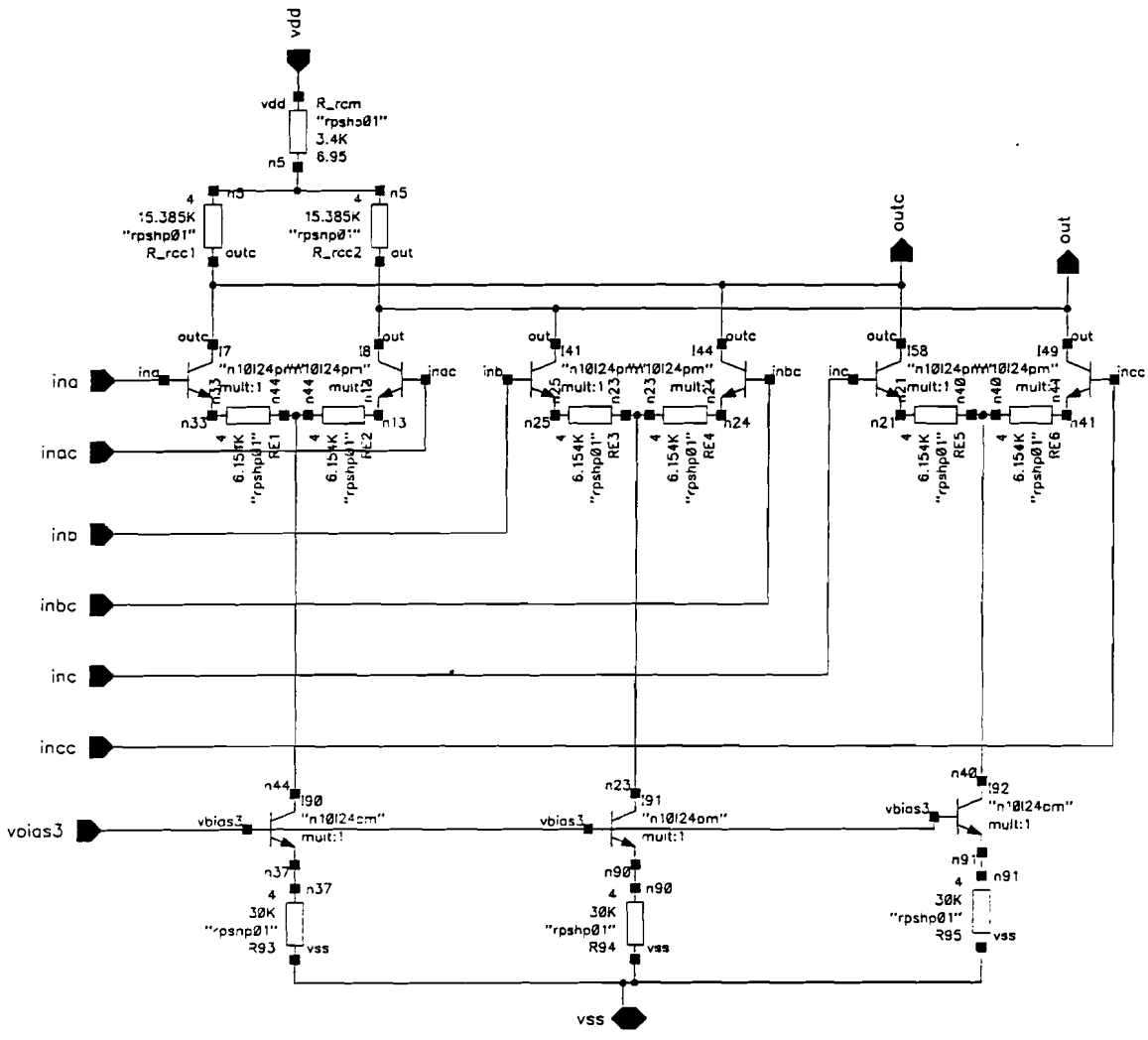
input gain stage 1: Layout realization



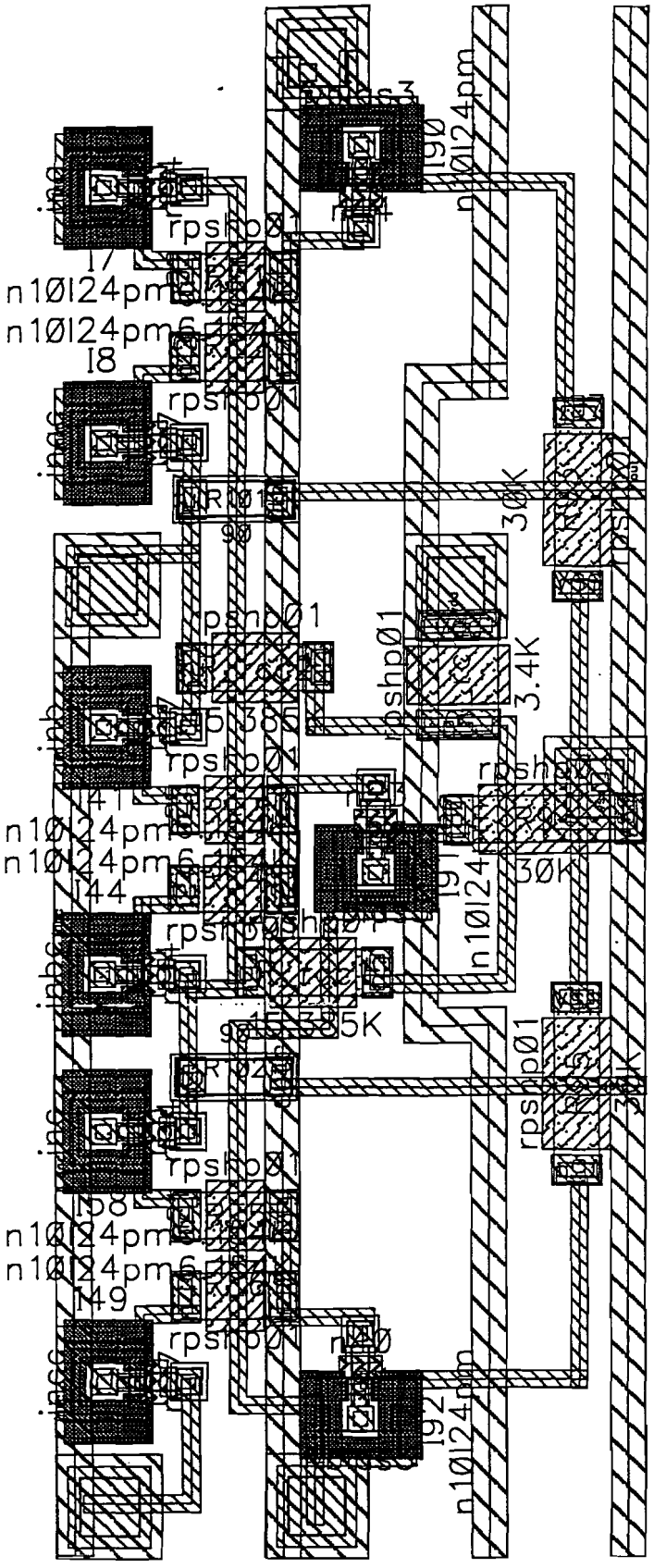
input gain stage 2: Schematic



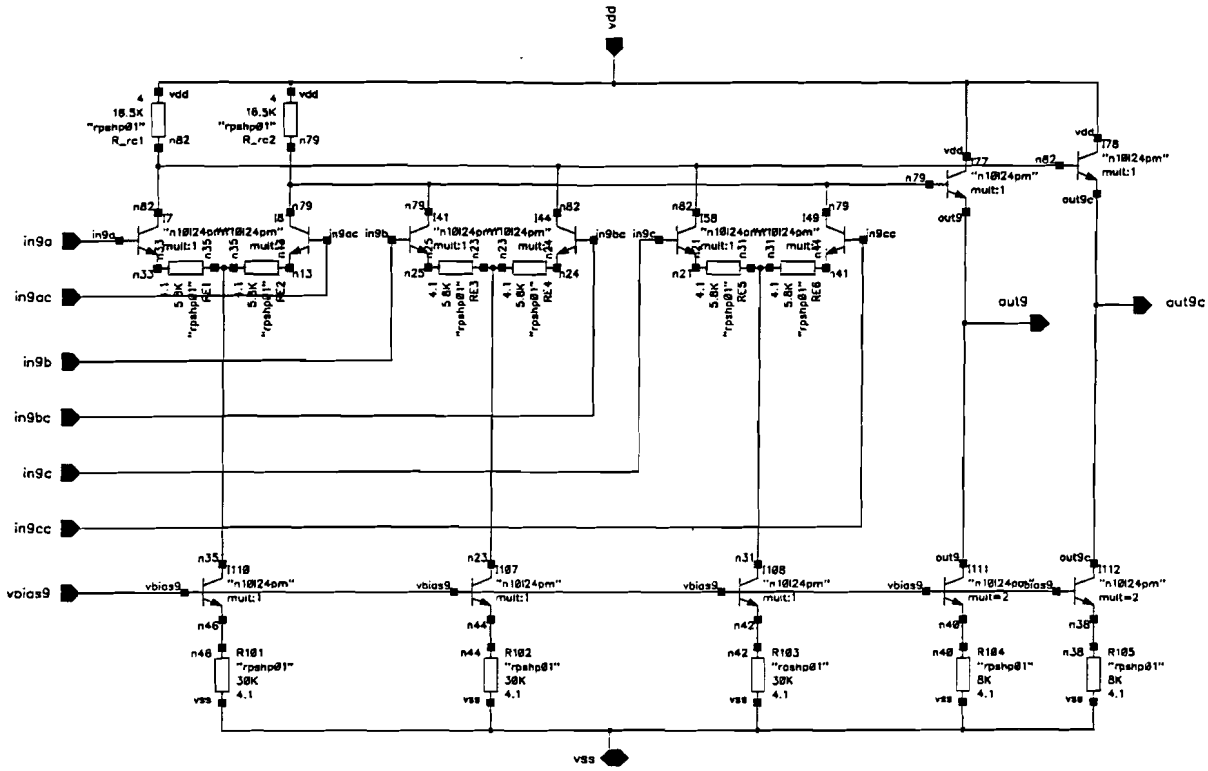
Input gain stage 2: Layout realization



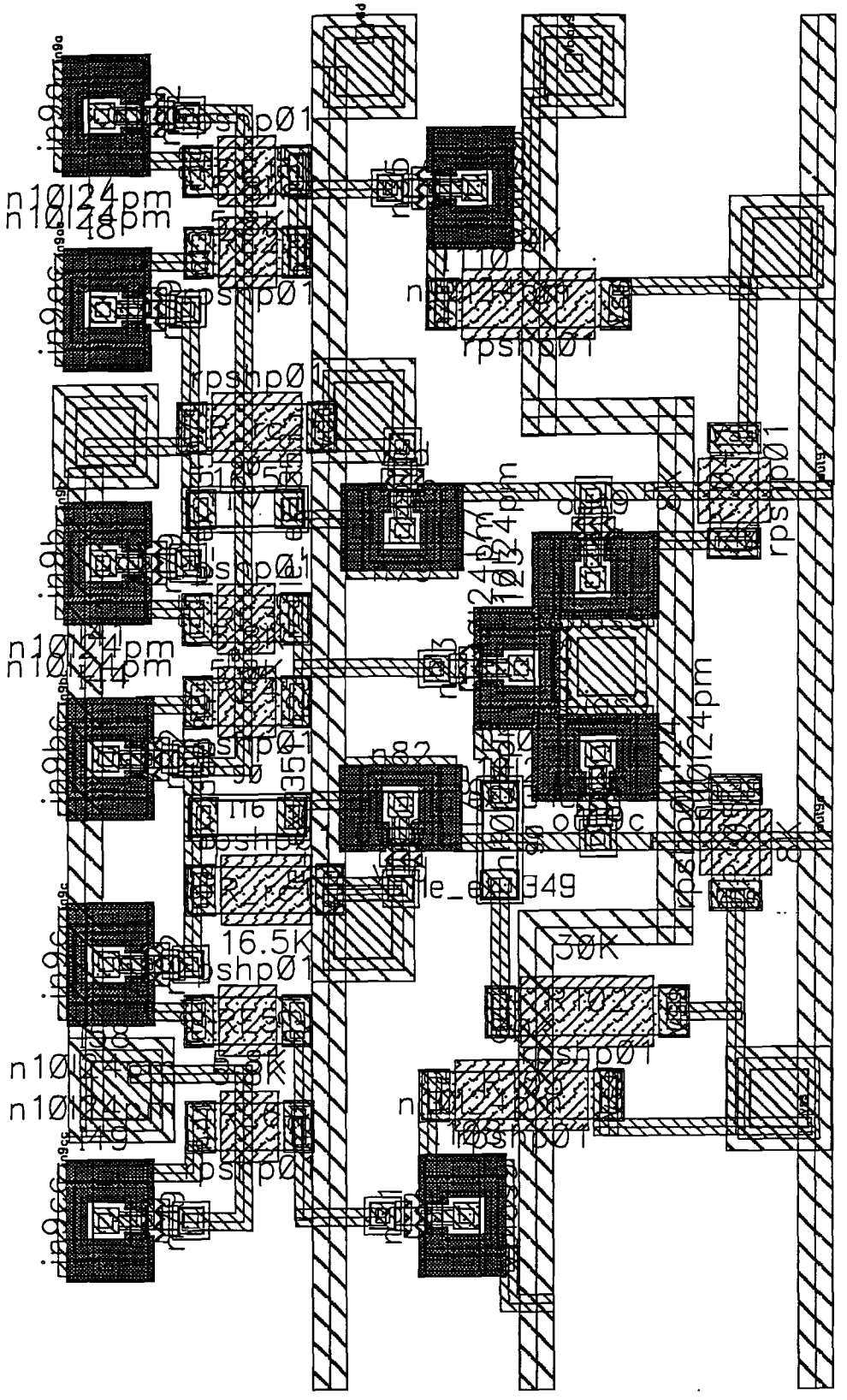
three folding block fine/coarse: Schematic



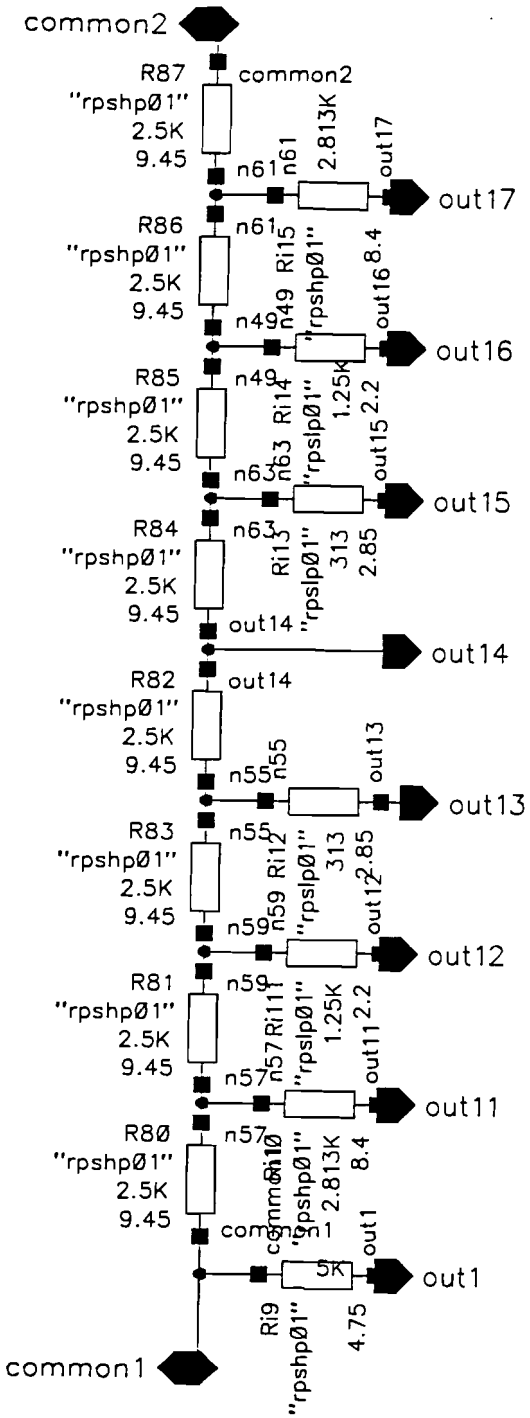
three folding block fine/coarse: Layout realization

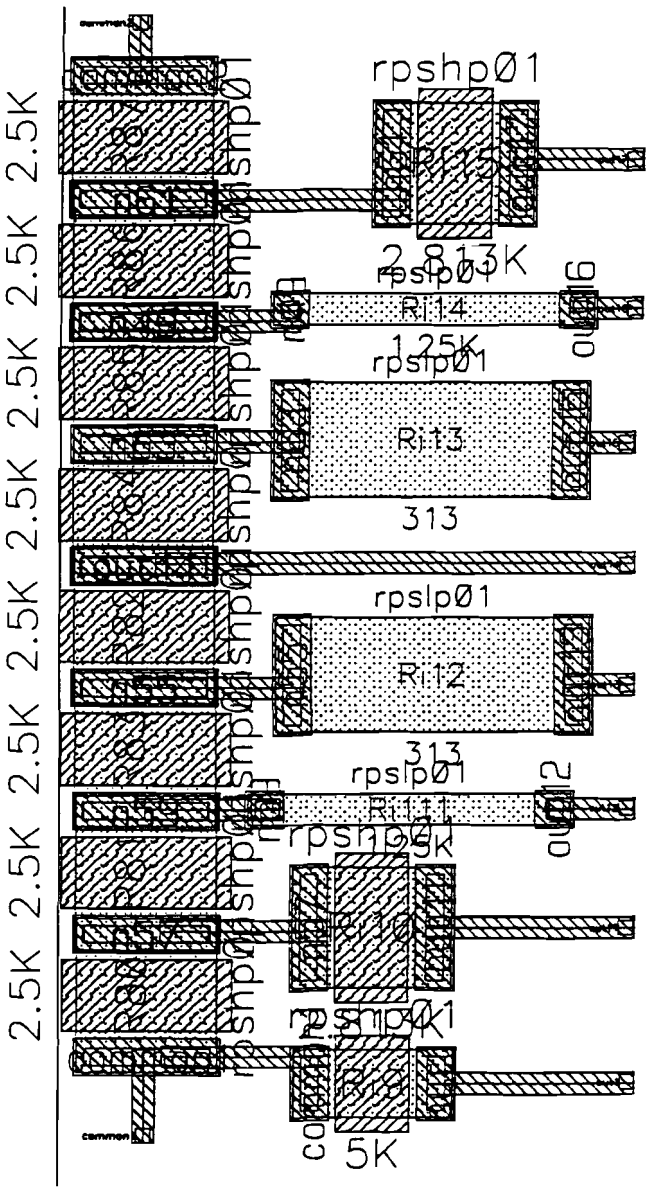


three folding fine combination block: Schematic



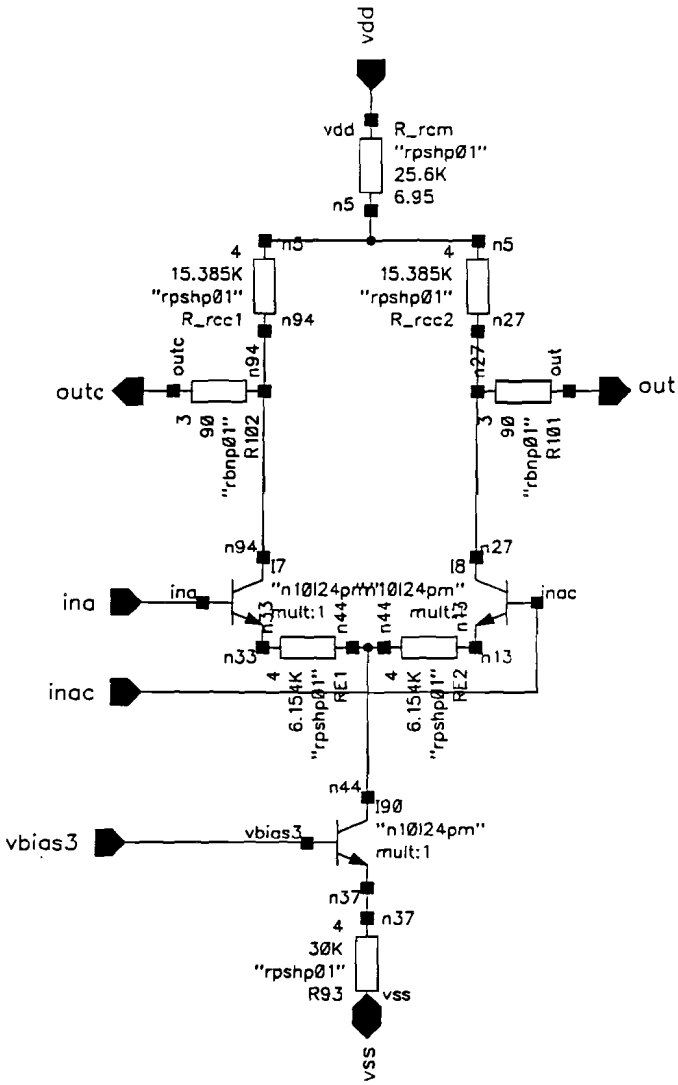
three folding fine combination block: Layout realization



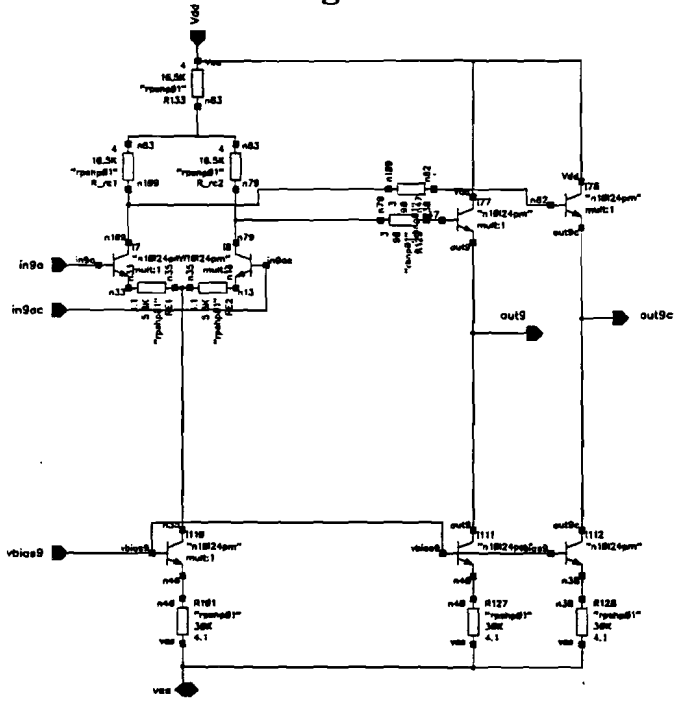


Interpolation ladder: Schematic

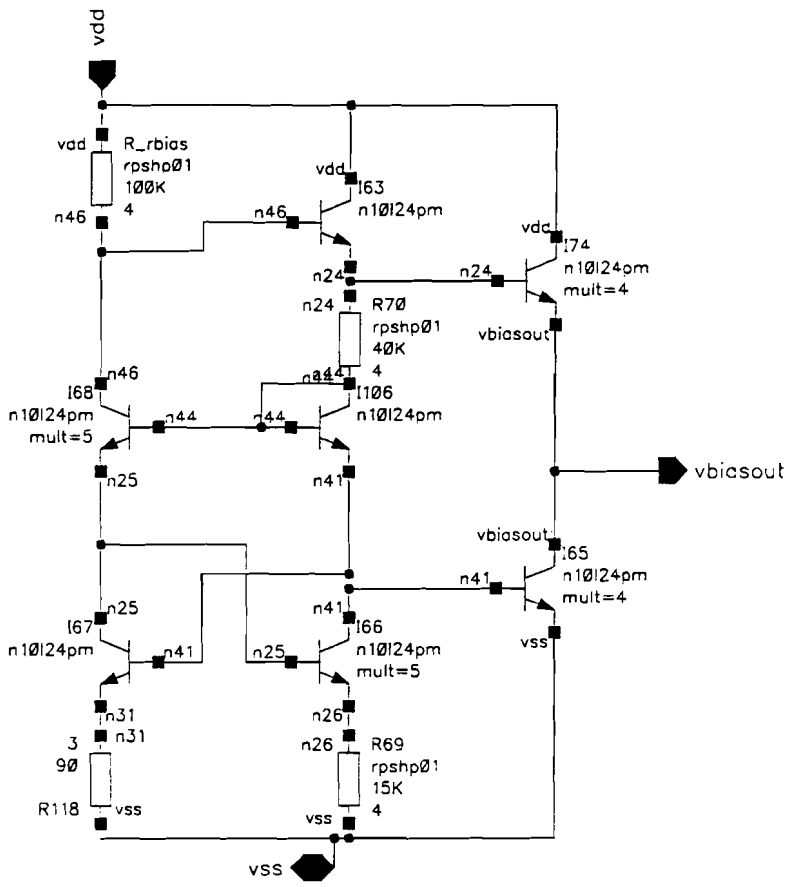
Interpolation ladder: Layout realization



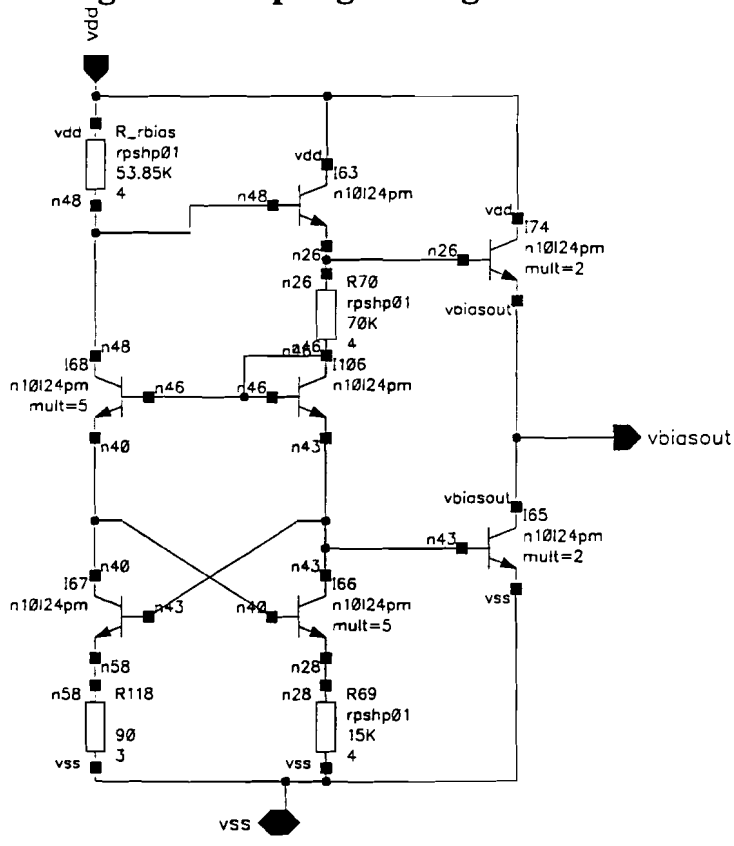
coarse one folding block: Schematic



coarse one folding combination block: Schematic



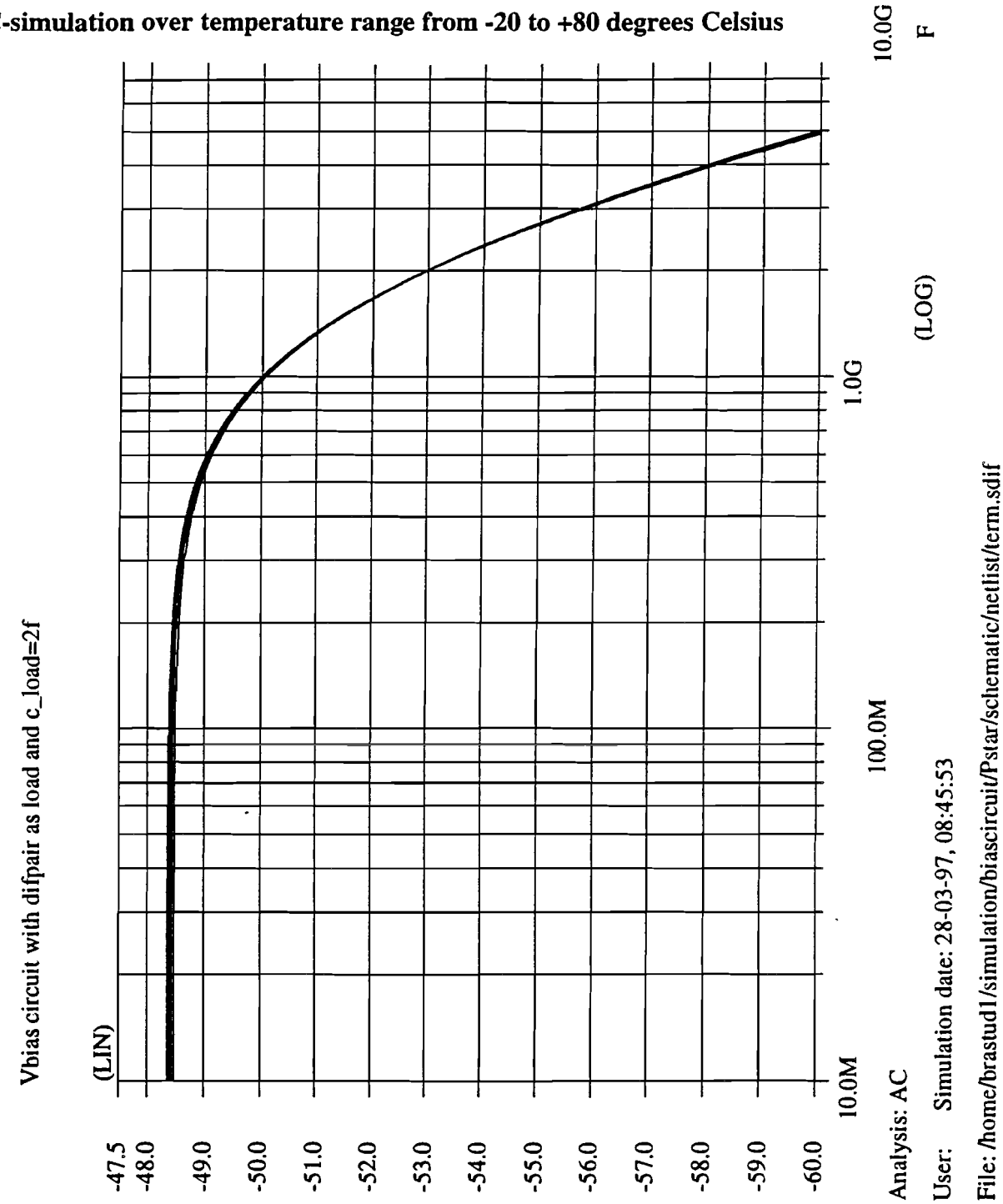
biasing circuit input gain stage: Schematic

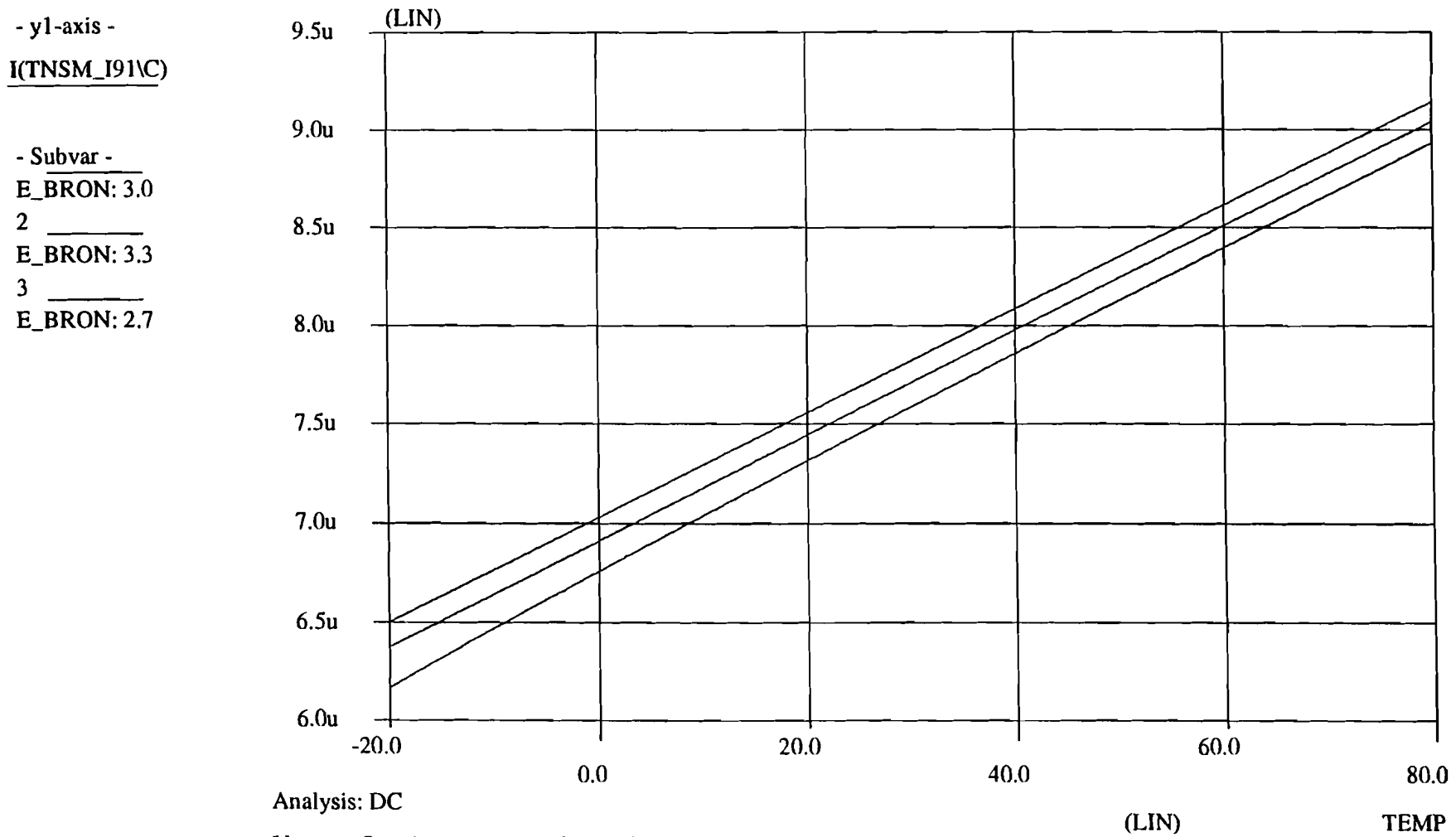


biasing circuit three folding part/ three folding combination: Schematic

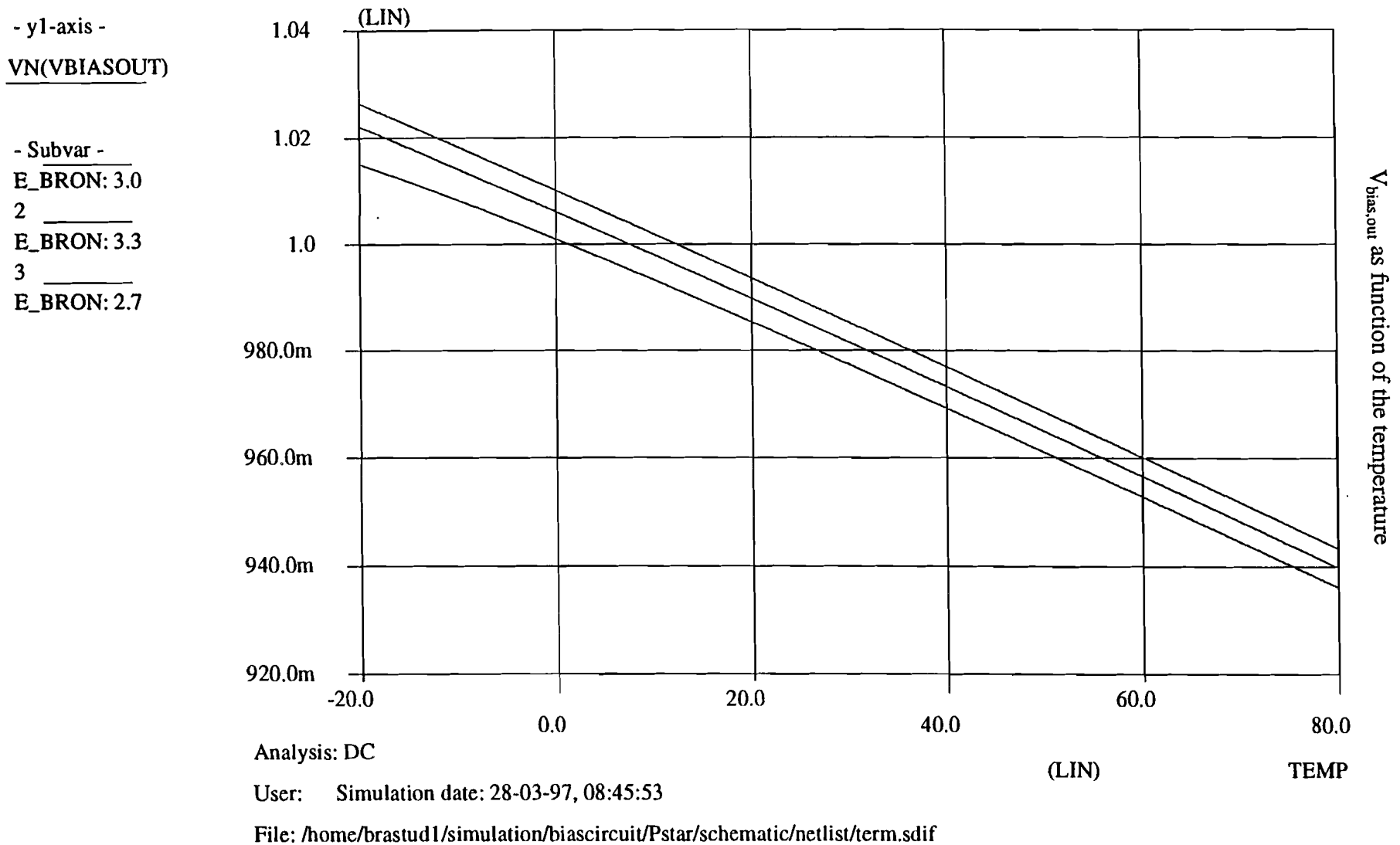
Appendix D: Biasing circuits with constant gain over temperature range

AC-simulation over temperature range from -20 to +80 degrees Celsius





I_{tail} as function of the temperature



$V_{bias,out}$ as function of the temperature