High speed comparator circuit for broadband transmitter architecture

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Master thesis assignment

High speed comparator circuit

for broadband transmitter architecture

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Abstract

This report presents the results of my master thesis project, which is the design and the circuit implementation of the driver stage (comparator) for the Class-S Power Amplifier (PA). The comparator is designed for the transmitter topology, that is based on the *Duty-Cycle* principle, with 0.18μ and 0.13μm CMOS technology.

The comparator circuit must be able to drive a load impedance, that consists of a standard 50Ω and a parallel capacitance of 1pF. The operating frequency is 2GHz and the required output voltage swing is 1V. The needed current for this operation is 20mA (minimal) and the large widths of the MOS devices are required.

At the beginning of the project, the literature investigation is done and several circuit topologies have been analyzed. The comparator types that uses switch-capacitor circuits are not suitable, because the use of external clock is not desired. Two types of comparator that are suitable, Open-loop and open-loop/regerenative, have been analyzed.

Design 1, is a comparator that consist out of three stages and it is a open-loop comparator type. The first two stages will amplify the minimal input signal of 50mV to a rail-to-rail signal. This signal is applied to the last stage, which is an push-pull inverter. The major advantage of this circuit is a low circuit area and simplicity, that is essential at high frequency operations. For 2GHz operation, the minimal propagation time of 100psec is achieved (with CMOS13 technology) and the dc-power dissipation of 45mW.

Design 2, is a comparator circuit that consists out of the latch circuit. Major advantage of the latch circuit is the low power dissipation. However, the major disadvantage is the low resolution of the latch. For this reason the preamplifying circuit is needed in order to achieve the sufficient amplification of the minimal input signal. For 500MHz operation, the minimal propagation time of 230psec is achieved (with CMOS13 technology) and the dc-power dissipation of 28mW. In order to obtain 2GHz frequency operation, preamplifiers are need and the circuit size becomes unacceptable.

Contents

Chapter 1

Introduction

This chapter gives an introduction to the master thesis project, where the background information of a project is presented as well as the design goals and methodology. Also a chapters overview of this report is given.

1.1 The project background

A new concept topology of the switching transmitter is designed within the MsM group at the Technical University of Eindhoven. The transmitter topology is based on the *Duty-Cycle* principle and consists of the driver, switching **P**ower **A**mplifier (PA) and a low pass filter that are connected together in a feedback circuit as shown in *figure 1.1.*

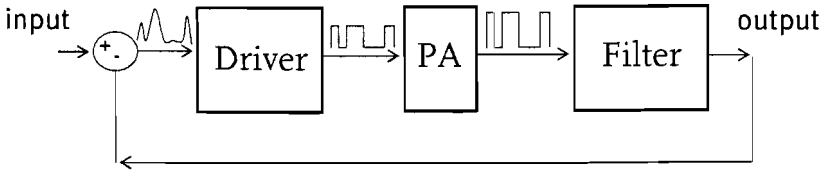


Figure 1.1: Duty-Cycle based transmitter

This transmitter topology provides high power efficiency because of the use of the switching power amplifier. The switching power amplifiers are capable of achieving a higher power efficiency than the conventional (non-switching type) power amplifiers. The power efficiency of theoretically 100% can be obtained. This topology would fulfill the customer demand, which is long-talk battery and fast (broadband) application.

The feedback and the phase shift of the filter will cause that the system oscillates. The oscillation frequency will be significantly higher than the input frequency. This means that the circuits

inside the loop will operate at high frequencies. For example if the input frequency is 2GHz, the oscillation frequency will be approximately 10GHz and it will lead to that the circuits inside the loop must be operating at 10GHz. At these high frequencies is hard to achieve the needed power efficiency, because of the parasitic effects that are introduced. This is one disadvantage of this transmitter, namely it is highly dependant on the technology (efficiency).

1.2 Design goals

The main goal is to design the driver circuit for the switching type of amplifier. The driver is actually a comparator circuit and for the design the Philips CMOS technology 0.18μm and 0.13μm must be used. The comparator must provide sufficient peak-to-peak output voltage for proper functionality of the whole system. The switching power amplifier will provide large loading effect to the comparator. The load consist of the standard 50 Ω resistance and a parallel capacitance (1pF). The speed is an important parameter of the comparator and thus several parameters must be optimized. Comparator should be functional at 2GHz frequencies and this means that the parameters such as slew-rate, propagation time delay, rise-time and fall-time time must be determined and optimized. These parameters will also influence the achieved power efficiency.

1.3 Method of research

The method of research is similar to *Bottom-up* method as shown in *figure 1.2.* Literature investigation is the starting point. This includes getting familiar with the simulation tools and conventional comparator topologies. Comparator theory will provide more insight information into circuits advantages/disadvantages.

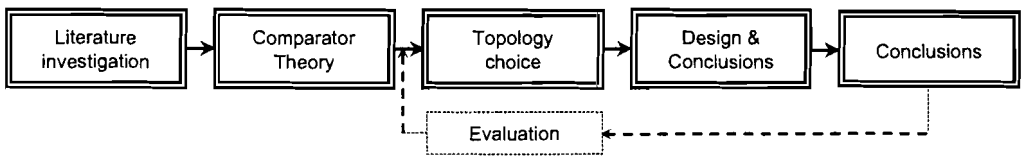


Figure 1.2: Comparator design method (*Bottom-up*)

Eventually the suitable topology will be chosen, simulated and optimized. At the end of the project, the necessary evaluation of the simulation results will be made and the conclusions and the recommendation will be reported.

1.4 Chapters overview

This report contains 6 chapters where the first chapter is devoted to the project introduction. The following chapters are shortly summarized;

Chapter 2 CMOS technology
Brief summary of available technology, namely Philips CMOS technology 0.18μm and 0.13μm. Standard CMOS curves are simulated and presented in order to gain more insight of technology advantage.

Chapter 3 Comparator theory
Basic comparator characterization is discussed. Furthermore, different comparator topologies are analyzed.

Chapter 4 The comparator design
Design considerations are made and two comparator topologies are investigated, *Design 1* and *Design 2*.

Chapter 5 Simulations
In this chapter the simulation results are presented. Simulations are done for both designs, (*Design 1* and *Design 2*).

Chapter 6 Conclusions and Recommendations
The conclusions provides a short summary of the whole report and the obtained results are presented. Several recommendations are given concerning the further development of the project.

Chapter 2

CMOS technology

For current generation wireless systems, the high operating frequency conditioned under low power consumption and costs, complicate the circuit design. Hence, **R**adio **F**requency (RF) operation of MOS transistor (MOST) circuits face some very hard design conditions.

A good RF capable semiconductor process should provide sufficient gain at the operating frequency, with a small current consumption. In RF terms, the primary performance parameters are the *unity current gain frequency* f_t and the *maximum oscillation frequency* (f_{max}). Although these parameters depend on the bias-conditions, a conservative rule of thumb can be used, namely each of these parameters should be et least 10 times greater than the maximum system frequency in order to ensure sufficient overall performance. Thus, for RF designs around 2GHz, the f_t and f_{max} values should exceed 20GHz.

High linearity and low noise properties of CMOS devices at low bias currents are also desirable. In the case of the comparator, linearity of MOST is not investigated because the comparator is a non-linear circuit. Further, the active devices should have low threshold voltages to allow low-voltage operation of the high speed circuits.
There are two Philips technologies available for simulation of the high speed comparator circuits, are CMOS18 (also RF model, CMO18RF) and CMOS13. Because the technology is one of the design boundaries, MOST simulation is the first step towards the final circuit design. Dc-curves are simulated and MOST parasitic effect are investigated. Unity-current-gain frequency (f_t) of the transistor will be simulated, as explained further on in this chapter.

2.1 CMOS modeling

For the simulations the MOST models are used. A model is a set of mathematical equation that describe electrical properties of the device. For the circuit design it is important to understand how a simple MOST model is build. Large signal and small signal models are introduced in this chapter.

2.1.1 Large-signal model

In *figure 2.1* the n-channel and p-channel MOS transistors are shown. The associated voltage polarities and currents are indicated. Source (S), drain (D), gate (G) are the three device terminals [1]. Bulk (B) is not shown since it is connected to ground. Three operating regions are defined, *Cutoff*, *Triode (linear)* and *Saturation* regions. The boundary between these regions is defined by the drain-source voltage v_{ds}(sat) ($=v_{GS} - V_T$). If the v_{ds} is less than the $v_{GS} - V_T$ than the MOST is in the triode region. For an n-channel MOST, in this region the current is defined by *equation 2.1.*

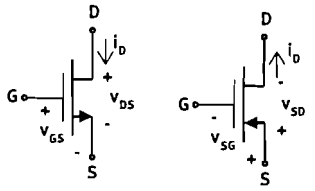


Figure 2.1: N-channel and P-channel MOS transistor

$$i_D = K'\frac{W}{L}[(V_{GS} - V_T) - \frac{V_{DS}}{2}] \qquad 0 < (V_{GS} - V_T) \leq V_{DS} \tag{2.1}$$

If $v_{DS} > v_{GS} - V_T$, than the MOST is in the saturation region and for an n-channel MOST int this region the current is defined by *equation 2.2.*

$$i_D = K'\frac{W}{2L}(V_{GS} - V_T)^2, \qquad 0 < (V_{GS} - V_T) \leq V_{DS} \tag{2.2}$$

Where:
V_T = Threshold voltage [V]
K' = Transconductance parameter (K'=$\mu_0 C_{ox}$) [$\mu A/V^2$]
μ_0 = Mobility of the channel [cm^2/Vs]
C_{ox} = Capacitance of the oxide layer separating gate from channel [F]
W = Effective channel width [μm]
L = Effective channel length [μm]

Equation that represents the saturation region can be extended by introducing the *channel length modulation*. This parameter should be accounted into the model with the addition of the factor $(1+\lambda V_{ds})$ as shown in *equation 2.3*. Here, λ is a device contant that mainly depends on L (length), and generally
$\lambda \propto 1/L$ can be applied.

$$i_D = K'\frac{W}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}), \qquad 0 < (V_{GS} - V_T) \leq V_{DS} \tag{2.3}$$

The output characteristics that represents all these regions is shown in *figure 2.2*. Notice that if channel length modulation is included, the current (I_D) will increase with increasing drain-source voltage.

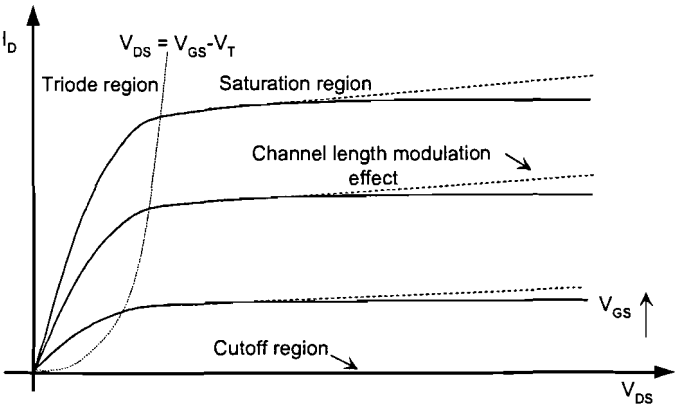
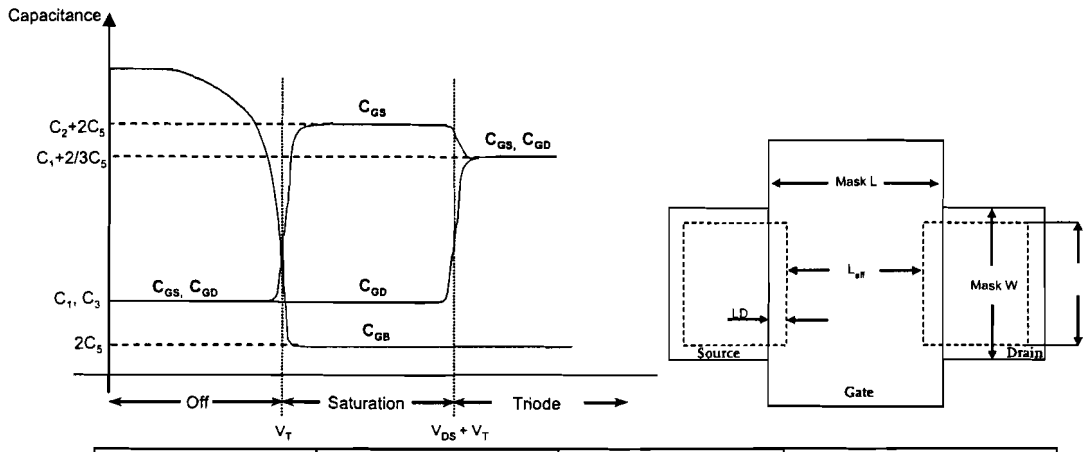


Figure 2.2: Drain current vs. drain-source and gate-source voltages

The same equations can be used for the p-channel MOST if all voltages and currents are multiplied by -1 and absolute value of the p-channel threshold voltage is used. In CMOS technology, p-channel devices are inferior to n-channel, namely n-channel devices are faster. The main reason is the low mobility of holes [6]. The approximate ratio between the mobility of n-channel and p-channel is around three to four times. This lower mobility results in low current drive and lower gain (transconductance). In order to achieve with p-channel device the same current as with n-channel (with same constant values of V_{DS}. For these reasons, it is preferred to use n-channel devices rather than p-channel devices.

The large signal capacitors model of the MOST consist of gate-to-source (C_{GS}), gate-to-drain (C_{GD}) and gate-to-bulk (C_{GB}) capacitances. It is important to understand the behavior of these capacitances if a high speed circuit is designed. The capacitances are examined as V_{DS} is held constant and V_{GS} is increased from zero. The MOST will first be in cutoff region until V_{GS} reaches V_T. If V_{GS} is further increased the device will enter the saturation region. In this region C_{GS} is the most dominant capacitance. If V_{GS} becomes equal to v_{ds}(sat) + V_T the device will enter the triode region. In *figure 2.3* the voltage dependent capacitances are shown.



Region of Operation	C_{GS}	C_{GD}	C_{GB}
Cutoff region	$C_{ox}(LD)(W_{eff})$	$C_{ox}(LD)(W_{eff})$	$C_{ox}(L_{eff})(W_{eff})$+CGBO(L_{eff})
Saturation	C_{ox}(LD+0.67 L_{eff})(W_{eff})	$C_{ox}(LD)(W_{eff})$	CGBO(L_{eff})
Triode	C_{ox}(LD+0.5 L_{eff})(W_{eff})	C_{ox}(LD+0.5L_{eff})(W_{eff})	CGBO(L_{eff})

Figure 2.3: Capacitances of a MOST in three main regions of operation

These capacitances are due to an overlap of two conducting materials, where a certain distance is introduced by the dielectric material. The overlap capacitance can be approximated $(\mathrm{LD})(W_eff)C_{ox} = (W_eff)(\mathrm{CGXO})$. CGXO (X = S, D or B) is thus overlap capacitance in F/m of gate, source, drain or bulk respectively. $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ is the capacitance of the oxide layer separating the gate from the channel. LD is equal to overlap distance where W_{eff} and L_{eff} are the effective width and length of the device (also shown in *figure 2.3*). Other parasitics effects are caused by the layout circuit. For example, bond-wire will also have a parasitic effect (inductance and capacitance) and it will degrade the circuit performance at high frequencies. For the eventual comparator design all these capacitances are of major importance.

2.1.2 Small-signal model

The small-signal model of a MOST is shown in *figure 2.4*. A small-signal model is a linearized model of the device for a given DC operating point.This model is only valid over voltage (current) regions where the large-signal voltage (current) are reasonably represented by a straight line.

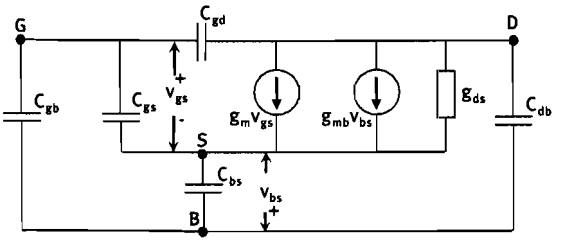


Figure 2.4: Small-signal MOST model

Transconductance g_m, channel conductance g_{ds} and g_{mb} are defined:

$$g_m = \frac{\partial i_D}{\partial v_{GS}} \tag{2.4}$$

$$g_{ds} = \frac{\partial i_D}{\partial v_{DS}} \tag{2.5}$$

$$g_{mb} = \frac{\partial i_D}{\partial v_{BS}} \tag{2.6}$$

The DC operating point influences the small-signal parameters. In the case of saturation g_m can be found from *equation (2.7)*. This parameter is important because it will eventually provide information about the device gain. It can be noticed that g_m will increase if W (width) is increased or if the I (current) through the device is increased.

$$g_m = \sqrt{(2K'W/L)I_D(1 + \lambda V_{DS})} \tag{2.7}$$

In saturation region, *equation (2.8)* defines g_{ds}. Channel length modulation will directly influence this parameter. If the CMOS device is used as a current source, it is important that the current source resistance is low, meaning that g_{ds} must be high. This can be achieved by increasing channel length modulation (λ). As mentioned before, λ will increase if the length (L) is made smaller.

$$g_{ds} = \frac{I_D\lambda}{1 + \lambda V_{DS}} \approx I_D\lambda \tag{2.8}$$

The unity-current-gain-frequency (f_t) of the transistor is calculated as shown in *figure 2.5.* The unity current gain frequency is defined as the frequency point where the current gain is equal to 1 (=0db).

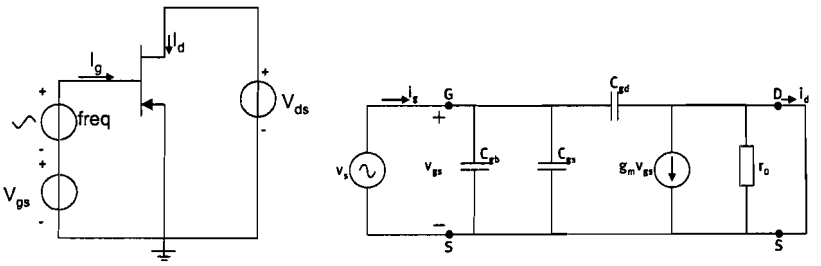


Figure 2.5: ft measurement and calculation

From this model the small-signal current gain is derived as

$$\frac{i_d}{i_g} = \frac{g_m \cdot v_{gs}}{v_{gs} \cdot j\omega(C_{gb} + C_{gs} + C_{gd})} = \frac{K' \cdot \frac{W}{L} \cdot (V_{gs} - V_T)}{v_{gs} \cdot j\omega(C_{gb} + C_{gs} + C_{gd})} \tag{2.9}$$

By setting the current gain equal to 1 (=0db) *equation (2.10)* is obtained.

$$|\frac{i_d}{i_g}| = 1 = \frac{K' \cdot \frac{W}{L} \cdot (V_{gs} - V_T)}{v_{gs} \cdot j\omega(C_{gb} + C_{gs} + C_{gd})} \tag{2.10}$$

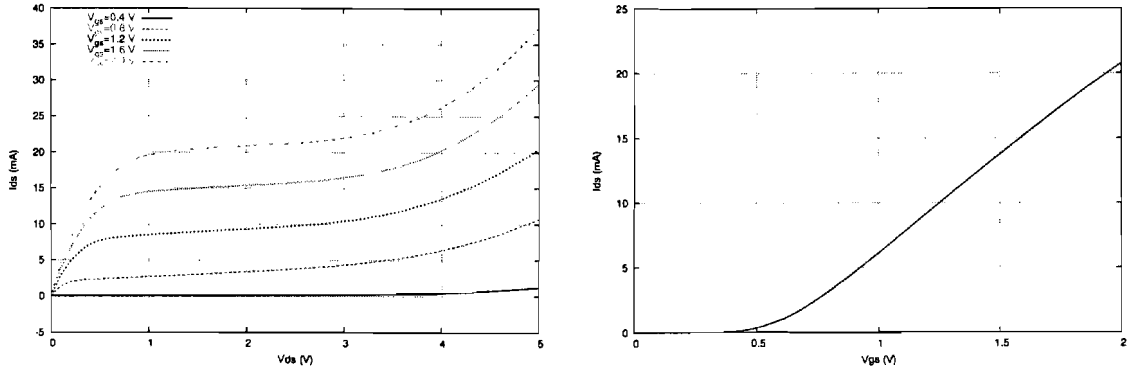
Deriving the ω from the last equation (and deviding by 2π) leads to *equation (2.11).*

$$f_t = \frac{K' \cdot W(V_{gs} - V_T)}{2\pi L \cdot (C_{gb} + C_{gs} + C_{gd})} = \frac{K' \cdot W(V_{gs} - V_T)}{2\pi L \cdot C_{gs}} \tag{2.11}$$

It can be noticed that the capacitance C_{gs} will decrease the unity current gain frequency. Furthermore V_{gs} is also directly influencing this parameter.

2.2 CMOS18

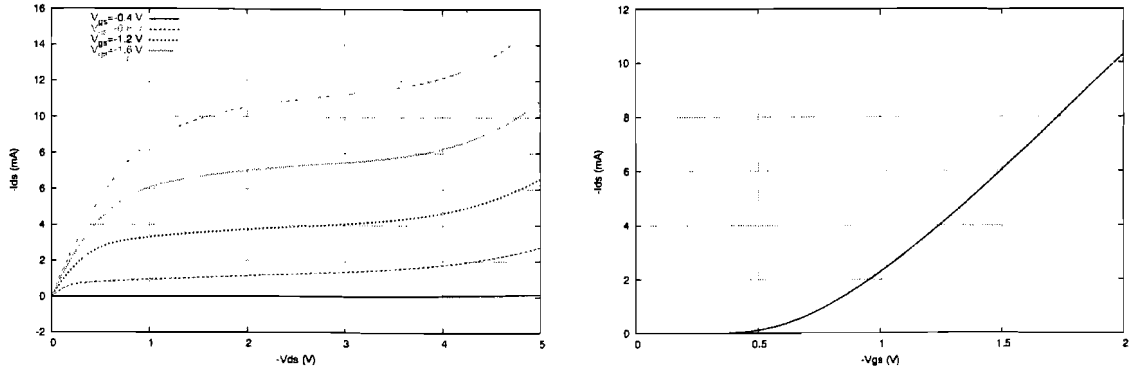
For the n-channel MOST (CMOS18 Philips technology), the simulation results are shown in *figure 2.6.* The width is chosen to be 30μm and length 0.18μm. The dc-characteristic in *figure 2.6(a)* represents the drain current as the gate-source (V_{gs}) and drain-source (V_{gs}) voltages are increased. In the *figure 2.6(a)* the drain current is simulated while the (V_{gs}) is increased. When (V_{gs}) reaches 0.4V the CMOS device starts to conduct the current, meaning that the threshold voltage is equal to $V_T = 0.4$V.



(a) I_{ds} vs. V_{ds}, V_{gs} is a parameter (b) I_{ds} vs. V_{gs}

Figure 2.6: N-channel curves for W=30μm and L=0.18μm

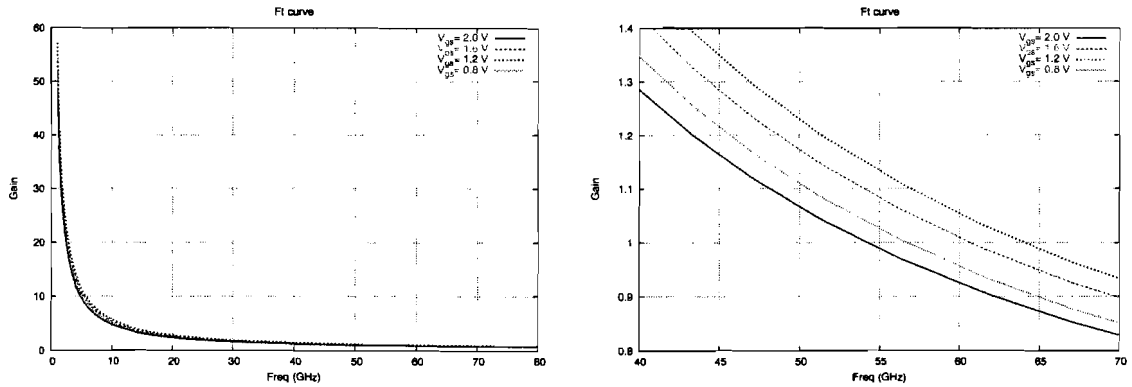
These simulations are also done for the p-channel device with the same W and L parameters, as shown in *figure 2.7.* It can be noticed that the n-channel device provides more current than the p-channel device. Threshold voltage of the p-channel device is also equal to $V_T = 0.4$V.



(a) $-I_{ds}$ vs. $-V_{ds}$, $-V_{gs}$ is a parameter (b) $-I_{ds}$ vs. $-V_{gs}$

Figure 2.7: P-channel curves for W=30μm and L=0.18μm

The unity current gain frequency (f_t) simulations are done for the n-channel device in CMOS18 technology. The ac-analysis is used for the simulation. As already discussed f_t, the unity current gain frequency is defined as the frequency point where the current gain is equal to 1 (=0db). In *figure 2.8* this current gain is simulated and shown. In *figure 2.8(a)* the frequency range up to 80 GHz is shown, where in *figure 2.8(b)* the frequency range between 40 and 70 GHz is shown. It can be seen that the f_t is ranging between approximately 50 GHz and 65 GHz. This conclusion fulfils one of the technology requirements concerning the operating frequency of the designed comparator circuit.



(a) f_t simulation, (range = 0 - 80GHz)

(b) f_t simulation zoomed, (range = 40 - 70GHz)

Figure 2.8: N-channel CMOS 18 unity current gain frequency

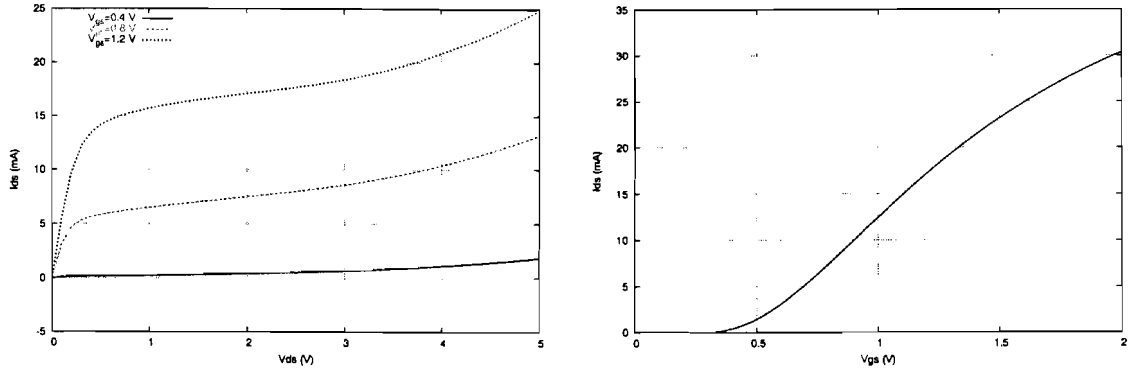
Simulation for the CMOS18 p-channel device of the same geometry (W, L), are done. P-channel device have lower hole mobility and normally, f_t for p-channel devices will be lower. From the simulations this is also concluded, namely f_t ranges approximately from 20GHz to 40Ghz. The performed simulation results confirm this conclusion and are shown in *Appendix A2.*

2.3 CMOS18RF

At high frequencies lots of unwanted effect occur that are hard to predict. Therefore, Philips designed more accurate CMOS18 model, namely RFCMOS18. This model will provide better approximation of the circuit behavior at high frequency of operation. This model will differ from the previous one (CMOS18) not in the large-signal but in the small-signal behavior, as concluded from the simulations (*Appendix A2*). These differences are shown in the latest paragraph of this chapter.

2.4 CMOS13

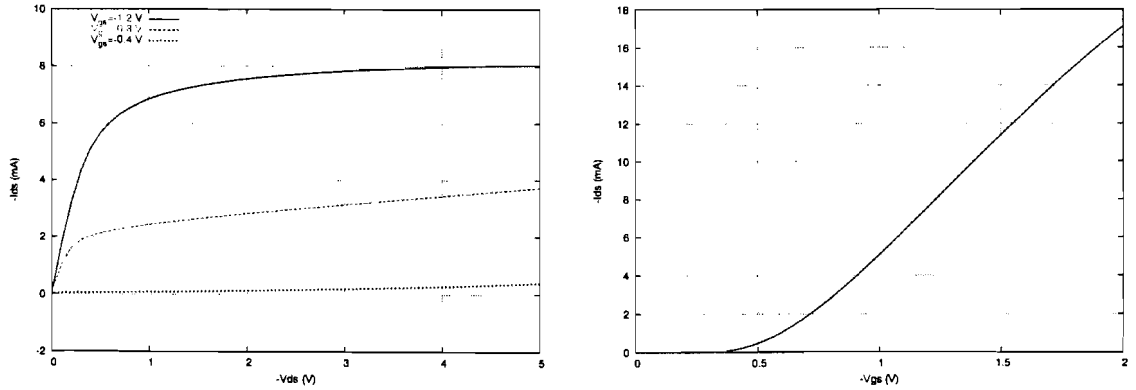
For the n-channel MOST (CMOS13 Philips technology), the simulation results are shown in *figure 2.9.* The width is chosen to be 30μm and length 0.18μm. The dc-characteristic in *figure 2.9(a)* represents the drain current as the gate-source (V_{gs}) and drain-source (V_{gs}) voltages are increased. In *figure 2.6(a)* the drain current is simulated while the (V_{gs}) is increased. When (V_{gs}) reaches 0.35V the CMOS device starts to conduct the current meaning that the threshold voltage is equal to $V_T = 0.35$V.



(a) I_{ds} vs. V_{ds}, V_{gs} is a parameter (b) I_{ds} vs. V_{gs}

Figure 2.9: N-channel curves for W=30μm and L=0.13μm

These simulations are also done for the p-channel device with the same W and L parameters, as shown in *figure 2.10.* It can be noticed that the n-channel device provides more current than the p-channel device. Threshold voltage of the p-channel device is also equal to $V_T = 0.35$V.



(a) $-I_{ds}$ vs. $-V_{ds}$, $-V_{gs}$ is a parameter (b) $-I_{ds}$ vs. $-V_{gs}$

Figure 2.10: P-channel curves for W=30μm and L=0.13μm

The unity current gain frequency (f_t) simulations are done and for n-channel device f_t ranges between 87GHz and 93GHz as the V_{gs} increases from 0.8 to 1.2V. For p-channel device, f_t ranges between 48GHz and 57GHz as the $|V_{gs}|$ increases from 0.8 to 1.2V. The simulation results are shown in *Appendix A2.*

2.5 Technology parameter comparison

In *tables 2.1 and 2.2* a short overview is shown for n-channel and p-channel device. The magnitudes parameters will be used for the calculations that are needed for the comparator design.

Technology		CMOS18	CMOS18RF	CMOS13
Voltage supply (V)		1.8	1.8	1.5
K'	($\mu A/V^2$)	100	100	120
C_{ox}	($\mu F/cm^2$)	83.2	83.2	1.65
λ	($1/V$)	0.0013	0.0013	0.001
f_t	(GHz)	54 - 64	53 - 63	87 - 93

Table 2.1: CMOS models comparison (N-channel)

Technology		CMOS18	CMOS18RF	CMOS13
Voltage supply (V)		1.8	1.8	1.5
K'	($\mu A/V^2$)	50	50	60
C_{ox}	($\mu F/cm^2$)	83.2	83.2	186
λ	($1/V$)	0.0003	0.0003	0.0014
f_t	(GHz)	23 - 38	23 - 41	48 - 57

Table 2.2: CMOS models comparison (P-channel)

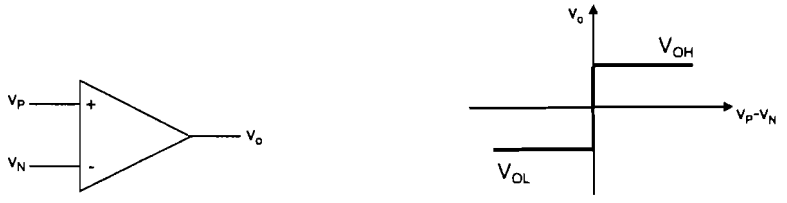
Chapter 3

Comparator theory

In this chapter, the comparator theory is introduced. A comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. Speed is a major requirement for a comparator, namely a fast transition between states is important. In fact, the transition speed is limited by the decision (making) response time of the comparator. In this thesis, topology that provides superior speed performance will be considered. Comparator is normally separated into stages. Several building blocks that can be used for these stages will be explained.

3.1 Comparator

The most common symbol used for comparator is shown in *figure 3.1(a)*. The output signal V_O is based on the comparison of the two analog input signals (V_P and V_N) and the two possible values of the output signal are V_{OH} (high) and V_{OH} (low) as shown in *figure 3.1(b)*.



(a) Comparator symbol (b) Transfer function

Figure 3.1: Ideal comparator

One of the **static characteristics** of comparator is the *gain* and for this ideal comparator it can be expressed by *equation 3.1*, where the input difference is defined by ΔV. Ideally, the gain is infinitive and therefore the input change ΔV approaches zero.

$$Gain = A_v = \lim_{\Delta V \to 0} \frac{V_{OH} - V_{OL}}{\Delta V} \tag{3.1}$$

This infinitive gain is in reality not achievable and a more realistic dc-transfer function is shown in *figure 3.2*. The gain of this model is given in *equation 3.2*, where V_{IH} and V_{IL} represent the input voltage difference, needed to bring the output to saturation, $V_o = V_{OH}$ and $V_o = V_{OL}$, respectively.

$$f(v_P - v_N) = \begin{cases} V_{OH} & for \quad (v_P - v_N) > 0 \\ A_v(v_P - v_N) & for \quad V_{IL} < (v_P - v_N) < V_{IH} \\ V_{OL} & for \quad (v_P - v_N) < 0 \end{cases}$$

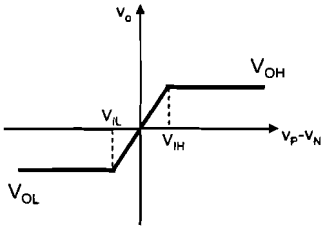


Figure 3.2: Transfer funtion for infinitive gain

$$Gain = A_v = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}} \tag{3.2}$$

This input difference is called the *resolution* of the comparator. The resolution is thus highly dependant of the comparator gain. The practical resolution value is of the order of 10-50 mV. For the comparator design, this resolution should be specified. Another non-ideal effect is the *input-offset voltage* of comparator, V_{OS}. In *figure 3.3* this offset effect is illustrated and the transfer function is shown.

$$f(v_P - v_N) = \begin{cases} V_{OH} & for \quad ((v_P \pm V_{OS}) - v_N) > 0 \\ A_v((v_P \pm V_{OS}) - v_N) & for \quad V_{IL} < ((v_P \pm V_{OS}) - v_N) < V_{IH} \\ V_{OL} & for \quad ((v_P \pm V_{OS}) - v_N) < 0 \end{cases}$$

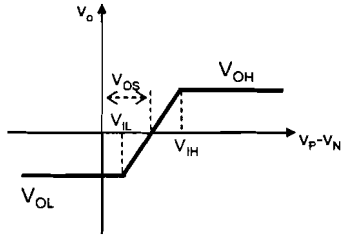


Figure 3.3: Transfer curve including input-offset voltage

The output changes when the input difference crosses zero and in the absence of the input-offset voltage (V_{OS}=0), the comparator transfer curve will be symmetrical around the reference voltage. If the input-offset voltage effect is included, the output will not change until the input difference

reaches the value of V_{OS}. Accurate prediction of the input-offset voltage is normally very hard to achieve because it is highly dependant on the circuit design and layout. The difference is made between two types of the offset voltage:

- *Systematic offset*, which is caused by improper dimensions and/or bias conditions.
- *Random offset*, which is due to the random errors that are made during the fabrication. These errors often result in the mismatch of ideally symmetrical devices.

Another important comparator characteristic is the input impedance. Several number of stages are used to build the complete comparator circuit. Every stage will provide the loading effect to the previous stage. For this reason a approximation of the input impedance is necessary. In the case of the MOS device, the input impedance will be mainly capacitive. This input impedance will impose the speed limitation, as it will be explained further on in this chapter.

Input stage is a differential circuit and hence the input common-mode range (ICMR) must be observed. This is the range of the input signal where all transistors of the comparator remain in the saturation. A comparator is often employed in mixed-signal system and possibly connected to noisy power-supply lines. Performance of the comparator in presence of power-supply noise is important and fully differential topologies will provide the best rejection to this unwanted effect. The power supply rejection ratio (PSRR) is defined as the gain from the input to the output, divided by the gain from the supply to the output.

DC power dissipation will be mainly influenced by the biasing of the circuit. By calculations and simulations, it is possible to determine power supply current and the power dissipation ($P_{diss} = I_{supply} \cdot V_{supply}$).

The **dynamic characteristics** of the comparator should also be observed, because it includes both small-signal and large signal behavior. The small-signal dynamics of the comparator are characterized by the frequency model. In the frequency model, the differential voltage complex gain A_v is determined. $A_v(0)$ is the dc-gain of the comparator and ω_c represents a corner (-3dB) frequency of the dominant pole approximation. This behavior is presented by *equation 3.3.*

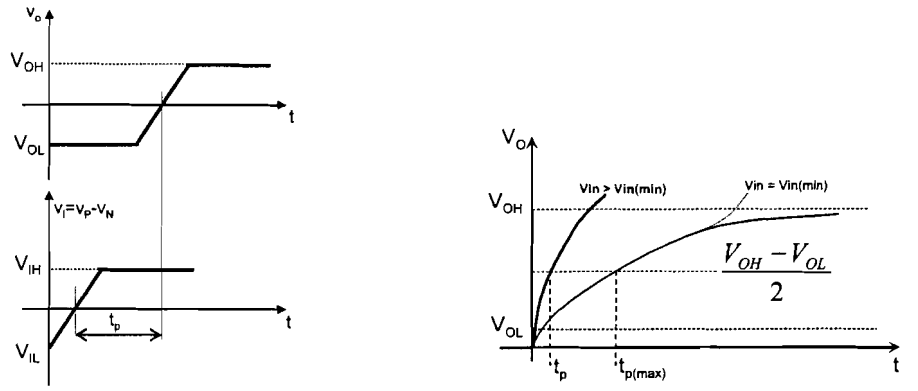
$$A_v(s) = \frac{A_v(0)}{\frac{s}{\omega_c} + 1} = \frac{A_v(0)}{s\tau_c + 1} \tag{3.3}$$

The minimum input voltage (resolution) is equal to the output difference (V_{OH} - V_{OL}) divided by the dc-gain of the comparator. If the (minimum) step input voltage is applied to the input, the output behavior can be modeled by the first-order exponential time response, as shown in *equation 3.4.*

$$\frac{V_{OH} - V_{OL}}{2} = A_v(0)(1 - e^{\frac{-t_p}{\tau_c}})V_{in}(min) \tag{3.4}$$

Solving the *propagation delay time* (t_p), by using $V_{in}(min) = \frac{V_{OH}-V_{OL}}{A_v(0)}$, will result into *equation 3.5.* Propagation delay time is a time difference between the input (V_P) crossing the reference voltage and the output changing the state (V_{OH} or V_{OL}), as shown in *figure 3.4(a).*

$$t_p = \tau_c ln(2) \approx 0.693\tau_c \tag{3.5}$$



(a) The propagation delay

(b) Input-amplitude vs. propagation time delay

Figure 3.4: Propagation time delay and input amplitude influence

In *figure 3.4(b)* the comparator response for two different input-amplitude is shown. If the input-amplitude becomes higher, the comparator response time will increase, resulting in the shorter propagation time.

This input-amplitude influence on the propagation time delay is modeled by *equation 3.6*, where $k = \frac{V_{in}}{V_{in}(min)}$ is the ratio between the applied input voltage and the minimal input voltage.

$$t_p = \tau_c \cdot ln(\frac{2k}{2k-1}) \tag{3.6}$$

Normally, the comparator will be designed with the intention to achieve as minimal as possible propagation time delay. It will be proven that the delay (t_p) is reduced by cascading several gain stages. In other words, the delay of single high-gain stage is larger then the delay of several low-gain stages. Noise will introduce some uncertainty in the comparator transition between two states, as illustrated in *figure 3.5*. The noise performance of the comparator will be influenced by both , thermal and 1/f noise. At low frequency 1/f noise is important, whereas at higher frequencies the thermal noise is important [1]. The comparator will be used in the transmitter topology and the expectations are that the noise influence will be minimal because of the feedback.

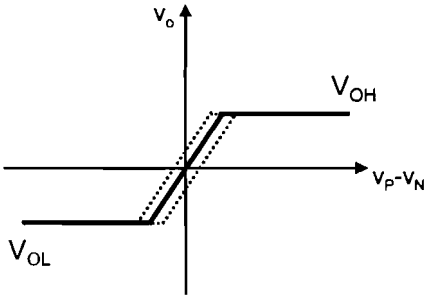


Figure 3.5: Noise influence

The *slew-rate* ($SR = \frac{dV}{dt}$) is defined as an ratio between output voltage-rate limit and the needed time. SR is usually influenced by the available current (I) and a load capacitance (C_L) ($SR = \frac{I}{C_L}$). The propagation time is often determined by the SR requirements, especially when the operating frequency is high and low power circuit operation is required. In this case the challenge is to minimize the propagation time by maximizing the sinking or sourcing capability of the comparator. The propagation time that is determined by the slew-rate can be calculated by *equation 3.4*.

$$t_p = \Delta T = \frac{\Delta V}{SR} = \frac{V_{OH} - V_{OL}}{2 \cdot SR} \tag{3.7}$$

3.2 Gain stages

Before several comparator types are investigated, the basic circuits (gain stages) that are used for the comparator design will be discussed. In this section the following circuit topologies are examined:

- Differential stages
- Inverters
- Latches

3.2.1 Differential stage

Differential amplifier is a circuit that amplifies the difference between the two input signals ($V_{in} = V_P - V_N$). In most comparator types, the differential amplifier is used as the input stage. In *figure 3.6*, the differential amplifier that uses current-mirror as a load is shown. One input is often set to a reference dc-voltage, V_{DC}. By increasing/decreasing the input voltage the transfer characteristics can be obtained. In order to understand how the propagation time delay is influenced by this stage, the following analysis is done.

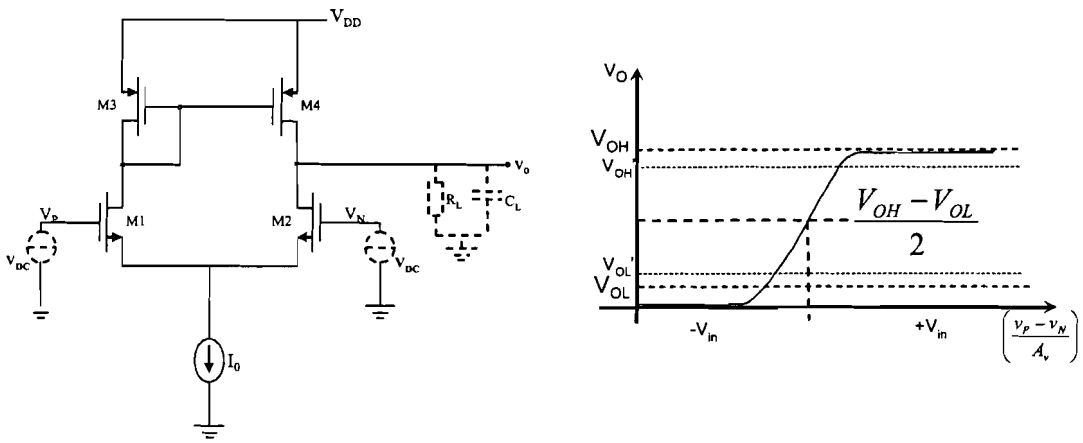


Figure 3.6: Differential amplifier with current-mirror load and the transfer characteristic

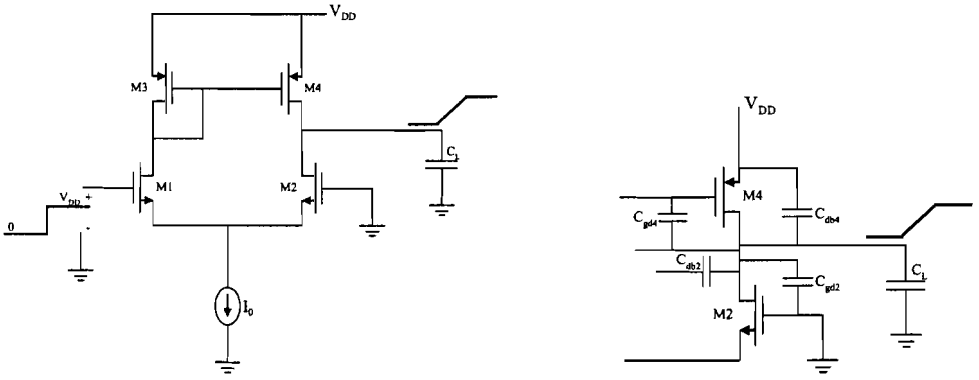
Assume that V_{GS2} is fixed to a certain dc-voltage V_{DC} and that $v_{G1} > V_{DC}$, such that $i_1 < I_o$ and $i_2 < 0$. In this case, the MOST M4 is in the saturation region and $i_4 = i_3 = i_1$ is valid. v_o increases because of the difference current flowing into C_L.
Eventually, $|V_{ds}|$ of M4 will decrease to the point that it $i_4 = i_2$ and the output voltage will stabilize at V_{OH}.

Assume now that V_{GS2} is still fixed to a certain DC voltage V_{G2} and that $v_{G1} < V_{DC}$, resulting in $i_1 > 0$ and $i_2 < I_o$. In this case MOST M4 is in the saturation region and $i_4 = i_3 = i_1$ is less than current i_2. Because most of the current I_o flows through M_2, the output v_o will decrease. Eventually, $v_o \leq V_{G2} - V_{T_N}$ will be valid and the current i_2 will decrease until $i_2 = i_1$. At this point the output voltage will stabilize to V_{OL}.

The differential transconductance g_{md} and the gain for this stage are defined by *equation 3.8*. The voltage gain is based on the small-signal model and is given as the product of g_{m1} (which is equal to g_{m2}, assuming the circuit symmetry $W_1/L_1 = W_2/L_2$) and the output resistance $r_o = \frac{1}{g_{ds2}+g_{ds4}}$. By increasing the transconductance a higher gain will be achieved. This can be done by increasing the tail current I_0 or by increasing the width of the MOS devices, M1 and M2.

$$g_{md} = \frac{\partial i_{out}}{\partial v_{id}} = \sqrt{\frac{K_1 I_0 W_1}{L_1}} \qquad A_v = \frac{g_{md}}{g_{ds2} + g_{ds4}} \tag{3.8}$$

Furthermore, the slew-rate will be influenced by the total current I_0 and the capacitive load ($SR = I_5/C_{tot}$). In *figure 3.7* this slew rate limitation is presented, where $C_{tot} = C_L + C_{db4} + C_{gd4} + C_{db2} + C_{gd2}$ and $\omega_c = \frac{g_{ds4}+g_{ds2}}{C_{tot}}$.



(a) Step response (b) Output capacitances

Figure 3.7: Slew-rate limitations of the differential amplifier

The maximal and minimal input-common range are defined by *equation 3.9* [1].

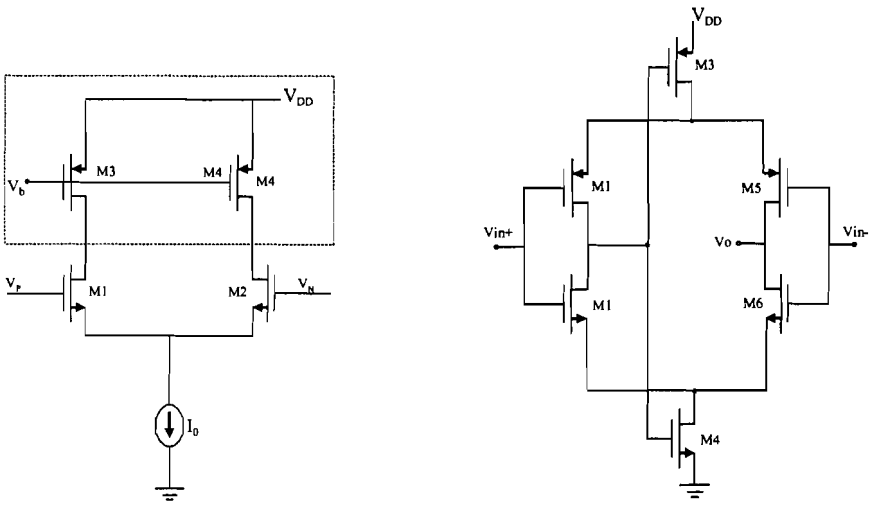
$$V_{IC}(max) = V_{DD} - V_{SG3} + V_{TN1} \qquad V_{IC}(min) = V_{DS5}(sat) + V_{GS1} \tag{3.9}$$

The static power dissipation is determined by the current I_0 as $P_{diss} = V_{DD}I_0 = V_{DD}(I_3 + I_4)$.

Another differential amplifier topology is shown in *figure 3.8(a)*. This configuration uses the current-source load and it has an advantage of a larger input common-mode range, because M3

is no longer connected in the diode configuration. This amplifier can be applied as a differential-in differential-out and it has the same gain as the current-mirror loaded amplifier. However, if the output is single ended, the small signal voltage gain is half of the current-mirror loaded amplifier.

Complementary Self-biased Differential Amplifier (CSDA) [13] is used in order to increase the output current sinking and sourcing capability of comparator. In *figure 3.8(b)* the CSDA circuit is shown. This amplifier consists of two differential amplifiers (inverters) serving as the load for the other. The circuit configuration of CSDA differs from conventional differential amplifier in two important aspects. Firstly, the amplifiers are completely complementary meaning that each n-channel MOST operates in push-pull fashion with the corresponding p-channel MOST. Secondly, the amplifiers are self-biased through the local negative feedback (M3 and M4).



(a) Differential amplifier with current source load

(b) Complementary self-biased differential amplifier

Figure 3.8: Differential amplifier types

The circuit depicted in *figure 3.8(b)* operates as follows. If the input voltage $v_{in}+$ increases, the drain voltages of M1 and M2 will decrease. M3 will start to conduct the current and all of this current will be sourced to the output capacitance through M5. At this moment the gate-source voltage of M4 is bellow V_T and no current will be flowing through it. In case that the input voltage $v_{in}+$ decreases, M4 turns on and the current will be sunk through the output load via M6.

The circuit speed is increased if it is possible to source/sink large amount of current and CSDA is capable of supplying currents that are significantly greater than the quiescent bias current. This is major advantage of CSDA topology, however disadvantage is that CSDA circuit is more sensitive to variations in processing, temperature and supply.

3.2.2 Latch

A latch is a regenerative type of comparator that uses positive feedback to accomplish the comparison of two signals [9], [11]. The simple form of a latch is shown *figure 3.9* and consists of inverters in positive feedback.Suppose that nodes V_x and V_y have an initial voltage level and by opening the switch, the circuit is placed in the regenerative mode. At this instance the feedback is enabled and the outputs will change in a certain time period (V_x = *low* and V_y = *high*, or visa-versa). This time constant of the latch can be found by analyzing a simplified circuit as shown in *figure 3.9*. With the assumption that the inverters are in their linear range, the inverters can be modeled as voltage controlled current sources, driving an RC load. A_v is the low frequency gain of inverter and for this linearized model *equation 3.10* holds.

$$\frac{A_v}{R_L}V_y = -C_L\frac{dV_x}{dt} - \frac{V_x}{R_L} \qquad \textit{and} \qquad \frac{A_v}{R_L}V_x = -C_L\frac{dV_y}{dt} - \frac{V_y}{R_L} \tag{3.10}$$

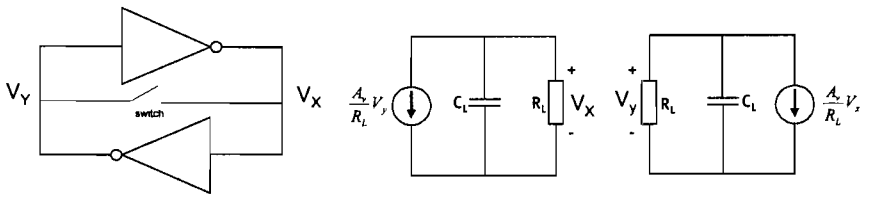


Figure 3.9: Simplified latch circuit

Multiplying *equation 3.10* gives,

$$\tau(\frac{dV_x}{dt}) + V_x = -A_vV_y \tag{3.11}$$

and

$$\tau(\frac{dV_y}{dt}) + V_y = -A_vV_x \tag{3.12}$$

where $\tau = R_LC_L$ is the time constant at the output node of each inverter. Subtracting the last two equations, *equation 3.13* is obtained.

$$(\frac{\tau}{A_v - 1})(\frac{d\Delta V}{dt}) = \Delta V \tag{3.13}$$

where $\Delta V = V_x - V_y$ is the voltage difference between the output nodes of the two inverters. The solution for this first-order differential equation is given by,

$$\Delta V(t) = \Delta V_i \cdot e^{(A_v-1)t/\tau} \tag{3.14}$$

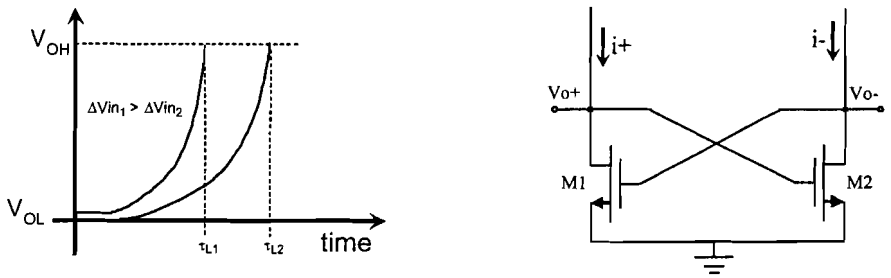
ΔV_i is the initial voltage difference at the beginning of the latch phase. Thus, the voltage difference increases exponentially in time, with a time constant given by *equation 3.15.*

$$\tau_L = \frac{\tau}{A_v - 1} = \frac{R_L \cdot C_L}{A_v} = \frac{C_L}{G_m} \tag{3.15}$$

G_m is the transconductance of each inverter. C_L is the capacitance seen from each inverter. The propagation time delay of the latch can be found from the previous equations, by setting the output level to $\frac{V_o(max)}{2}$. Thus the propagation time delay is given by

$$t_p = \tau_L = ln\frac{V_{OH} - V_{OL}}{2 \cdot \Delta V_i} \tag{3.16}$$

The time required for the output to reach maximal output level is decreased by applying a larger input difference to the latch (ΔV_i). If the input is small, the latch takes a long time to reach the maximal output level, as shown in *figure 3.10(a).* Therefore, it is desirable to apply a larger input signal in order to take advantage of faster latch response. If the input signal is low, the preamplifier circuit can be used to achieve shorter response time. A major advantage is that the power dissipation of the latch is relatively small compared to the differential amplifying circuit. Latch only dissipates the dynamic power. In *figure 3.14(b)* the latch circuit is shown, where the n-channel MOST is used.



(a) Response time of latch

(b) NMOS latch

Figure 3.10: Latch response time and n-channel MOST latch circuit

3.2.3 Inverters

Inverters are basic circuits that are often used as gain stages or as output stages (buffers). In *figure 3.11* three typical inverter configurations are shown, namely active PMOS load inverter, current-source load inverter and push-pull inverter [4]. By comparing the large-signal voltage-transfer function characteristics of these three circuits, it can be concluded that the push-pull inverter can achieve the highest gain. Another major advantage of this topology is that the output swing is capable of operation from rail-to-rail, while the other two configurations do not operate from rail-to-rail. For these reasons the push-pull inverter will be the most suitable for the comparator design and a more detailed analysis will be done.

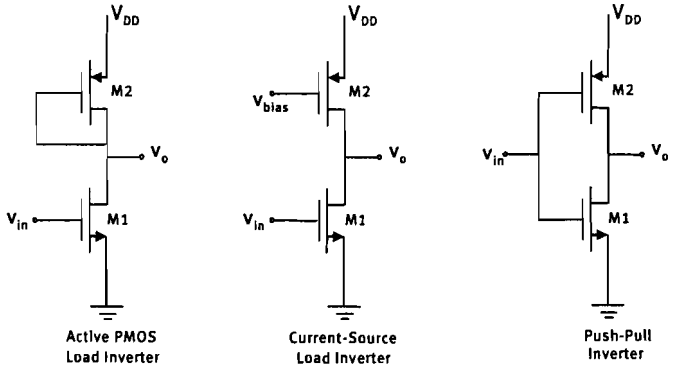


Figure 3.11: Inverter configurations

In *figure 3.12* the voltage transfer curve of the push-pull inverter is shown. There are three regions of operation, region **1**, **2** and **3** .

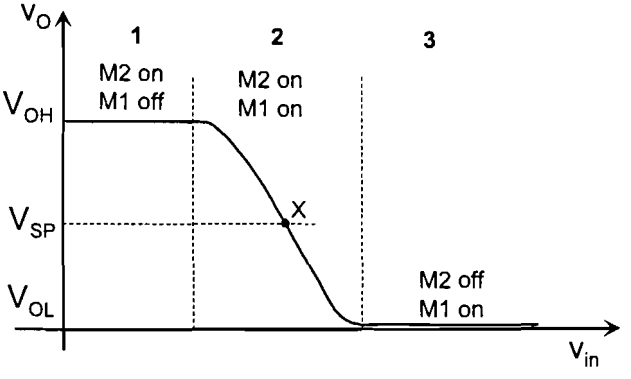


Figure 3.12: Transfer characteristic of the push-pull inverter

The circuit operates in *Region 1* when the input voltage of the inverter is connected to the ground. In this case, the output is pulled to V_{OH} through p-channel MOST, i.e. M2 is 'on' (saturated) and M1 is 'off' (cutoff).
In *region 2* both MOS devices are saturated and transition between two states (V_{OH} and V_{OL}) will occur. M1 enters the saturation region when $v_{DS1} \geq V_{GS1} - V_T$ (or $V_o \geq V_{in} - V_T$) and M2 is in the saturation region when $v_{SD2} \geq V_{SG2} - |V_T|$ (or $V_{DD} - V_o \geq V_{DD} - V_{in} - V_T$). The point X is called inverter switching point, V_{SP}. The drain current in each MOST must be equal at this point X, i.e.

$$K' \frac{W}{2L}(V_{SP} - V_{T_N})^2 = K' \frac{W}{2L}(V_{DD} - V_{SP} - V_{T_P})^2 \tag{3.17}$$

By using the simplification $K' \frac{W}{L} = \beta$ and solving V_{SP} *equation 3.18* is obtained.

$$V_{SP} = \frac{\sqrt{\frac{\beta_N}{\beta_P}} V_{T_N} + (V_{DD} - V_{T_P})}{1 + \sqrt{\frac{\beta_N}{\beta_P}}} \tag{3.18}$$

Region 3 occurs when the input is connected to V_{DD}. The output is then pulled to ground through the n-channel MOST, i.e. M1 is 'on' (saturated) and M2 is 'off' (cutoff).

The small-signal model of the push-pull inverter is shown in *figure 3.13*. In region 2, where both MOS devices are in the saturation region, the largest voltage gain will be achieved and *equation 3.19* is valid.

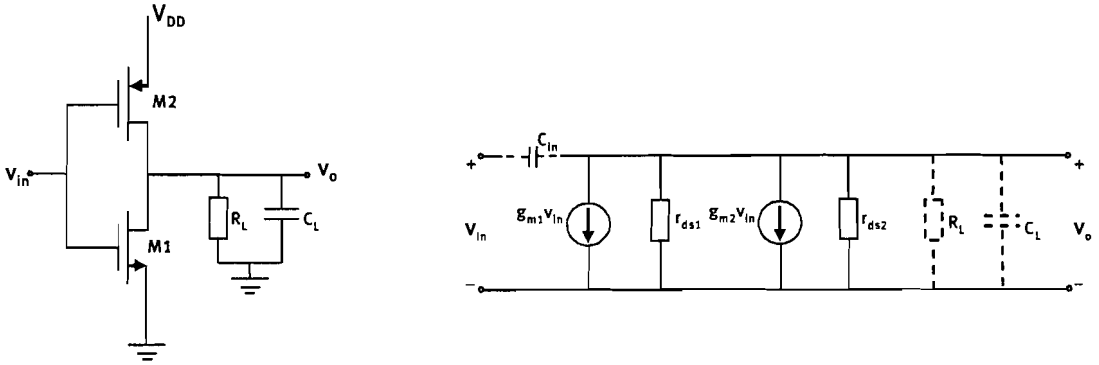


Figure 3.13: Push-pull inverter and the equivalent small-signal circuit

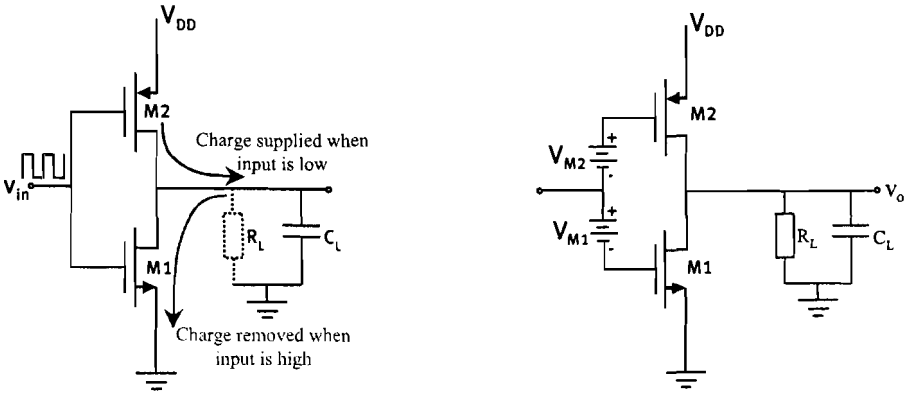
The small-signal voltage gain can be found as

$$\frac{v_{out}}{v_{in}} = \frac{-(g_{m1} + g_{m2})}{g_{ds1} + g_{ds2}} = -\sqrt{\frac{2}{I_D}} \left[\frac{\sqrt{K'_N (W_1/L_1)} + \sqrt{K'_P (W_2/L_2)}}{\lambda_1 + \lambda_2} \right] \tag{3.19}$$

The output resistance and the pole are defined by

$$R_o = \frac{1}{g_{ds1} + g_{ds2}} \qquad p_1 = \frac{-1}{Ro(C_L + C_{in})} = -\frac{g_{ds1} + g_{ds2}}{C_L + C_{in}} \tag{3.20}$$

For the comparator design, the inverters are also used as output stages (buffers). The primary objective of the output stage is to efficiently drive signals into the output load. The output load can be only a resistor, only a capacitor, or both. Normally, the output resistance is typically ranging from 50 to 1000 Ω and the output capacitance from 1-1000 pF. The output stage should provide sufficient current for proper driving of such loads.



(a) The push-pull inverter driven by rail-to-rail signal

(b) Power efficiency improvement

Figure 3.14: Push-pull inverter as a output stage

Power efficiency is important parameter and higher power efficiency can be obtained with the push-pull inverter. The higher efficiency is due to the fact that the both MOST devices are used as switches rather than as current sources. Since an ideal switch has either zero voltage across it or zero current through it, no power is dissipated. Push-pull amplifier has the disadvantage that a large quiescent current flows when the circuit operates in the high-gain region. If the voltage sources V_{M1} and V_{M2} are added to the circuit, higher power efficiency can be obtained.

The average power dissipation of the inverter stage can be approximated for the case when a square pulse signal is applied to the input of the inverter, with a period T. The average amount of current that the inverter must pull from V_{DD} is $I_{avg} = \frac{V_{DD} \cdot C_{tot}}{T}$. The average dynamic power dissipated by the inverter is defined in *equation 3.21.* It can be noticed that the power dissipation is a function of the clock frequency as

$$P_{avg} = V_{DD} I_{avg} = \frac{C_{tot} V_{DD}^2}{T} = C_{tot} V_{DD}^2 f_{clk} \tag{3.21}$$

3.3 Comparator types

Several comparator types are existing and depending on the design requirement, one topology will provide better results then the other. However, technology is a major boundary, and often the trade-offs must be made between the speed, resolution and the power dissipation. Topologies are divided into *Open-loop*, *Regenerative* or the combination of these two. In the case that the comparator is used for the fixed frequency, the combination of switched capacitors and open-loop comparators can be used to achieve better resolution [2]. The most advantageous topology (high speed, small circuit area) will be chosen for the comparator design .

3.3.1 Open-loop

Open-loop comparator uses the amplifier stages (open-loop) to perform the comparison of two input signals. The optimum number of stages can be determined if the comparator is modeled by *figure 3.15.*

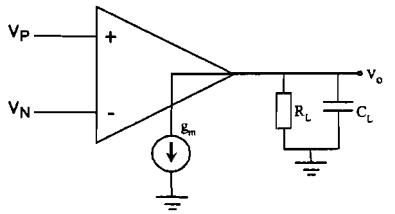


Figure 3.15: Comparator model

If $t << \tau = R_L C_L$, then the output can be approximated with $V_o = g_m R_L V_{in}(1 - e^{-t/(R_L C_L)} \approx V_{in}\frac{g_m}{C_L}t$. It can be noticed that speed is increased by increasing the gain $A_v = \frac{g_m}{C_L}$. In order to decrease the propagation time delay, the chain of identical stages can be used. Under the same assumption, output voltage can be expressed as, $V_o = V_{in}(\frac{g_m}{C_L})^n \cdot \frac{t^n}{n!}$, where n is the number of stages. For a given gain, the optimum number of stages can be found, $A_{v_n} = \frac{(n+1)^n}{n!}$ and the propagation time delay $t_{p_n} = (n+1)\frac{C_L}{g_m}$. Single amplifier has a limited capability and normally a gain of maximally 10 times can be achieved. For example, if the gain is ≈ 3, then the optimum number of stages is 6. However, this optimum will require a large circuit area and three stages with the gain of 6 time (per stage) will provide equally good results with less circuit area. This means that a trade-off must be made between the circuit size and performance.

3.3.2 Regenerative

Regenerative type of converters (latches) uses the positive feedback to detect small differences between two voltages. The resolution is one of the key requirements which determines the power dissipation of the total comparator circuit. A stand-alon latch cannot be used for high resolution

comparison since it exhibits large offset voltage (≈100mV). Therefore, the latch will need one or more pre-amplifying circuits depending on the requirements. The use of pre-amplifying circuits will lead to a decrease in the power efficiency.

3.3.3 Open loop Regenerative

In the case that the regenerative circuit is not able to satisfy the design requirements, the combination is made, where the open-loop amplifier and latch are used, as shown in *figure 3.16.* In order to improve the comparator resolution, the preamplifier is used. It is followed by the latch circuit and the output buffer. This type of comparator will improve the comparator functionality in terms of propagation time delay and resolution. However, if the load impedance requires high currents, then the circuit area will be large.

Figure 3.16: Comparator that combines open-loop amplifier and latch circuits

Chapter 4

Comparator design

In this chapter, the comparator design approach is presented. For high frequency circuit operation, the trade-off must be made between *speed* and *power dissipation*. Speed will be mainly influenced by the slew-rate requirements and the load impedance. The lower the load resistance (or higher the load capacitance), the more current will be needed to achieve a desired speed of operation. The *gain* of the comparator will influence the speed and power dissipation. The gain per stage that can be obtained is limited. The total gain can be increased by inserting more stages, but this method has one disadvantage, namely the unacceptable circuit size. The gain could also be increased by increasing the *power supply voltage*. However, the maximal power supply is limited by the chosen technology. The *input impedance* of the comparator should ideally be infinitive, but is often capacitive and must be also taken into slew-rate analysis. The low *output impedance* is important concerning the (minimal) power dissipation within the last stage. In *figure 4.1* the coherence between all of these design requirements is illustrated.

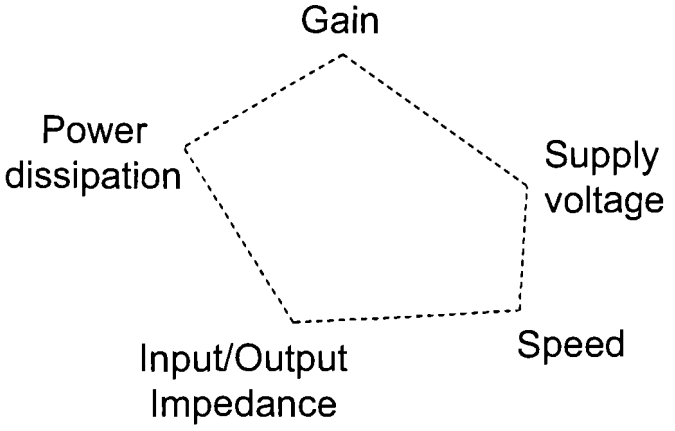


Figure 4.1: The design trade-offs

4.1 Design considerations

Design considerations are made in order to satisfy following requirements:

- Operating frequency of 2GHz (and 500MHz)
- Minimal input voltage (resolution) of Vin(min)=50mV
- 1V output voltage swing (Load $R_L = 50\Omega$ and with $C_L = 1$pF in parallel)
- Layout parasitics minimized

The *first design step* it to specify the *boundaries*. Technology will provide boundaries in terms of maximal supply voltage (1.8V for CMOS18 and 1.5V for CMOS13). For the CMOS technology of Philips f_t is determined in Chapter 2, and a conservative rule of thumb is fulfilled, namely f_t (for n-channel and p-channel MOST) is at least 10 times greater than the maximum system frequency.

The *second design step* is to make a topology choice that will be the most suitable for the *Duty-Cycle* based transmitter architecture. Two topologies are investigated, open-loop *(Design 1)* and open-loop/regenerative *(Design 2)*. Switched capacitor comparator type will minimize the offset voltage and possibly provide better resolution. However, in the case that the comparator must be operating in the *Duty-Cycle* based transmitter system, there is one major disadvantage that makes this topology unsuitable, namely the use of switches is not desirable. Because the feedback signal is not a constant phase signal, switches can not be driven by clock. Other disadvantage is that the circuit is operating at high frequency (2GHz) and the switches would introduce the feed-through effect, which would degrade the power efficiency of the whole system.

The *third design step* is the preanalysis of the circuit, where several dimension (W, L, g_m etc.) are calculated. The slew-rate requirements will determine the needed current. The calculated values will not always provide expected results and on the base of the simulation results, these values will be adjusted.

The *fourth design step* is the simulation. The simulation will include all the parasitic effects that are present at high frequency operations [14].

The *fifth (final) design step* is the summery of the obtained results. The simulation results will be critically analyzed.

In *figure 4.2* an output block wave signal is shown. It includes the non-ideal transitions between two output states. The currents needed to achieve satisfying rise and fall time (t_r, t_f) and 1V output swing, are calculated from the slew-rate requirements:

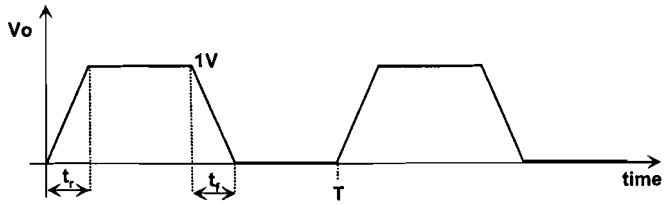


Figure 4.2: Rise and fall time of output signal

Frequency 2GHz → period time T=0.5nsec

Assuming that the required rise/fall time is

t_r, t_f=50psec (10% of the period time) → I= $C_L \frac{\Delta V}{t_r}$ = 1pF $\frac{1V}{50psec}$=20mA

Frequency 500MHz → period time T=2nsec

Suppose that required rise/fall time is

t_r, t_f=200psec (10% of period time) → I= $C_L \frac{\Delta V}{t_r}$ = 1pF $\frac{1V}{200psec}$=5mA

This simple analysis shows that circuit operation at 2GHz requires significantly larger current.

4.2 Design 1

Design 1 is an open-loop comparator that consists of three stages and the circuit diagram is shown in *figure 4.3*. Advantage of this comparator is that a minimal number of MOS devices is used, and the circuit area is small. However, rather large currents will be needed to achieve the desired operation.

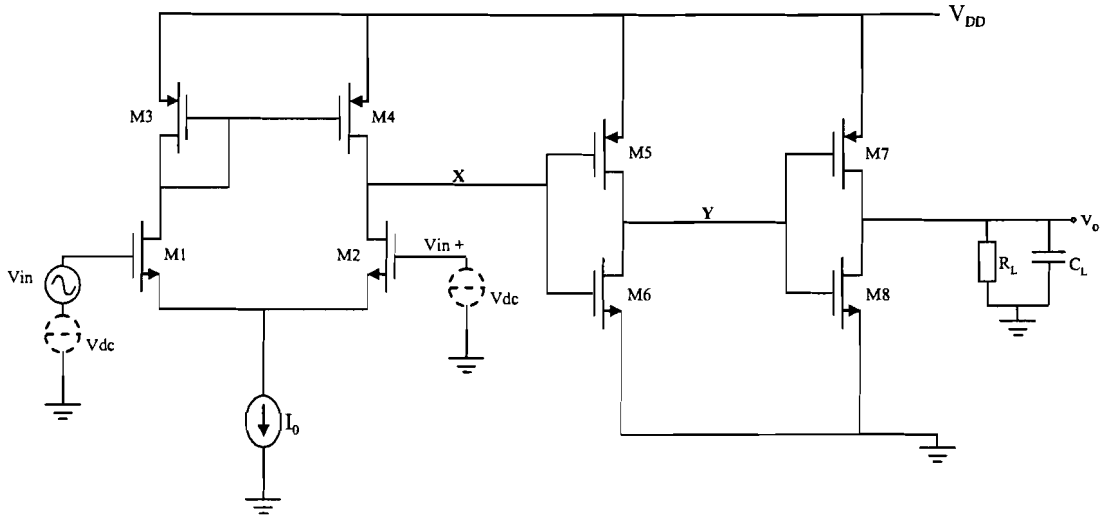


Figure 4.3: Design 1 topology

The load impedance consist of a relatively low resistor value, meaning that the output stage must be able to provide large currents. The output stage is a push-pull inverter and by assuming that the signal at point Y is a rail-to-rail block-wave, either M7 or M8 will be in the triode region. The needed current is 20mA and W_7 and W_8 are calculated by *equations 4.1 and 4.3*.

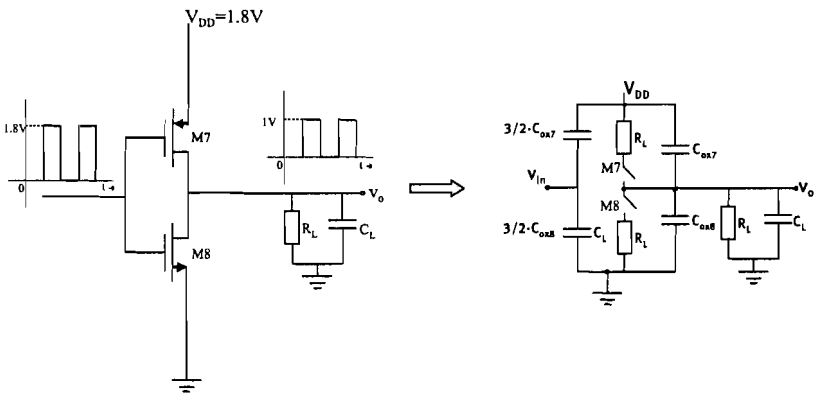


Figure 4.4: The output stage of Design 1

$$i_{D8} = K'_N \cdot \frac{W}{L}(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \tag{4.1}$$

$$20mA = 400\mu\frac{W}{L}(1.8 - 0.4)0.1 - \frac{0.1^2}{2} \rightarrow W \approx 35\mu m \tag{4.2}$$

$$i_{D7} = K'_P \cdot \frac{W}{L}(V_{SG} - |V_T|)^2 \tag{4.3}$$

$$20mA = 600\mu\frac{W}{L}(1.8 - 0.4)0.1 - \frac{0.1^2}{2} \rightarrow W \approx 75\mu m \tag{4.4}$$

The assumption is made that first two stages will be able to amplify the minimal input signal. The propagation time delay of this stage is determined by the slew-rate requirements and for used current of 20mA, the propagation time delay is equal to t_p=50psec.

The second stage is also a push-pull inverter. This stage must provide rail-to-rail output swing in order to effectively drive the output stage. Because of the slew-rate requirements and a large input capacitance of the output stage (approximately 1pF), this stage will have the same dimensions as the output inverter.

The input (first) stage has to amplify the minimal input signal and is shown in *figure 4.5*. This stage will also be loaded by a large input capacitance of the second stage. M3 and M4 will operate in the saturation region and therefor the gate-source voltage must be higher than the threshold voltage, $|V_{GS}|$ of 900mV will fulfil this requirements. Widths of this stage should not exceed 100μm and hence the tail current I_0 ≈7mA is chosen. This current is obtained by slew-rate requirements. W_3 and W_4 are equal and they are calculated by *equations 4.5 and 4.6*.

$$i_{D3} = K'_N \cdot \frac{W}{2L}(V_{SG} - V_T)^2 \tag{4.5}$$

$$3.5mA = 50\mu\frac{W}{2L}(0.9 - 0.4)^2 \rightarrow W \approx 55\mu m \tag{4.6}$$

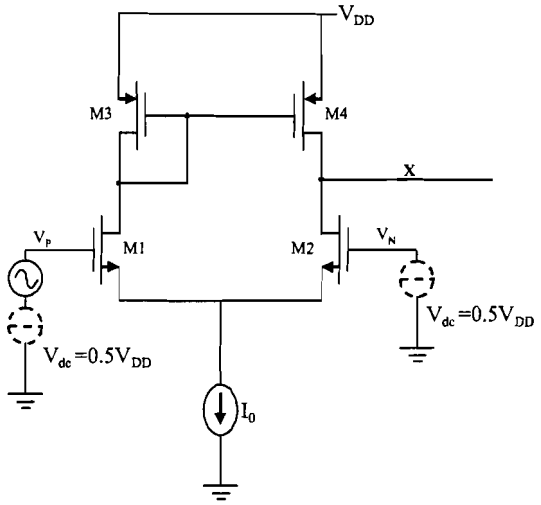


Figure 4.5: Input stage

The high transconductance of this differential stage will provide large gain. Transconductance is increased by increasing the width of M1. The values of W1 and W2 are determined by the MOST (saturation region) equation. However, this value will be adjusted depending on the simulation results.

The same calculations are done for the case of circuit design in CMOS13 technology. In *table 4.1* the calculated dimensions of the MOS devices (for both technologies) are shown. These values will be used for simulations. Furthermore, expected propagation time delay is approximately 150psec for 2GHz input frequency.

Technology	W/L (CMOS18)	W/L (CMOS13)
M1	80	60
M2	80	60
M3	55	35
M4	55	35
M5	90	80
M6	35	30
M7	90	80
M8	35	30

Table 4.1: Design 1 calculated W/L ratios (that will be used for the simulations)

4.3 Design 2

Design 2 consists of threes stages: an input preamplifier, a latch (decision circuit) and an output buffer. The block diagram of this comparator is shown in *figure 4.6*. A major disadvantage of the latch circuit is low resolution. That is the reason that the preamplifier is needed. The output buffer is needed to amplify the signal coming from the latch and to provide enough current for the load.

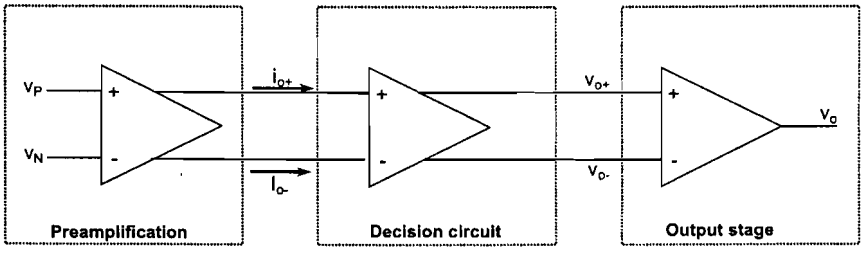


Figure 4.6: Design 2 block diagram

In *figure 4.7* the output stage is shown. It consists of the push-pull inverter (as in Design 1) and a self-complementary differential amplifier. This high gain amplifier is used to drive the push-pull inverter. The gain is equal to $A_v = \frac{g_{m1}+g_{m2}}{g_0}$, where g_{m1} and g_{m2} are the transconductances of devices M12M11 and M15M16 respectively. g_0 is the output conductance of the amplifier. The widths are determined by the slew rate requirements. For input signal of 500MHz W12=W15=20μm and W11=W16=7μm are chosen.

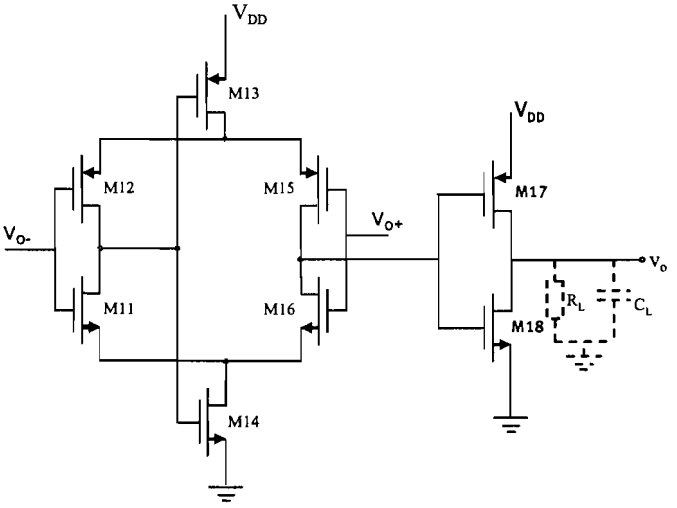


Figure 4.7: Design 2, output stage

The latch circuit should be capable of discriminating low-level voltages, of the order of mV. The circuit uses a positive feedback from the cross-gate connection of M8 and M9 to increase the gain.

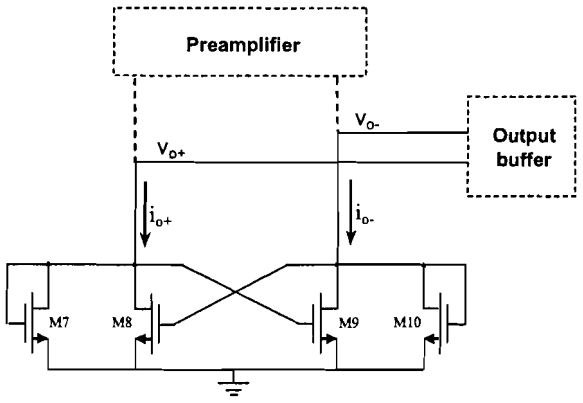


Figure 4.8: Design 2, the latch circuit

Assume that the current i_{0+} is much larger than i_{0-}. The MOS devices M7 and M9 will be 'on' and M8 and M10 will be 'off'. The output signal v_{0-} will be zero and *equation 4.7* is valid.

$$v_{0+} = \sqrt{\frac{2i_D(sat)}{K'\frac{W}{L}}} + V_{T_N} \tag{4.7}$$

In the case that, i_{0-} increases and i_{0+} decreases, switching will occur when the drain-source voltage of M9 is equal to V_{T_N} of M8. At this point, M8 starts to take current away from M7. This will decrease the drain-source voltage of M7 and eventually M7 will turn off.

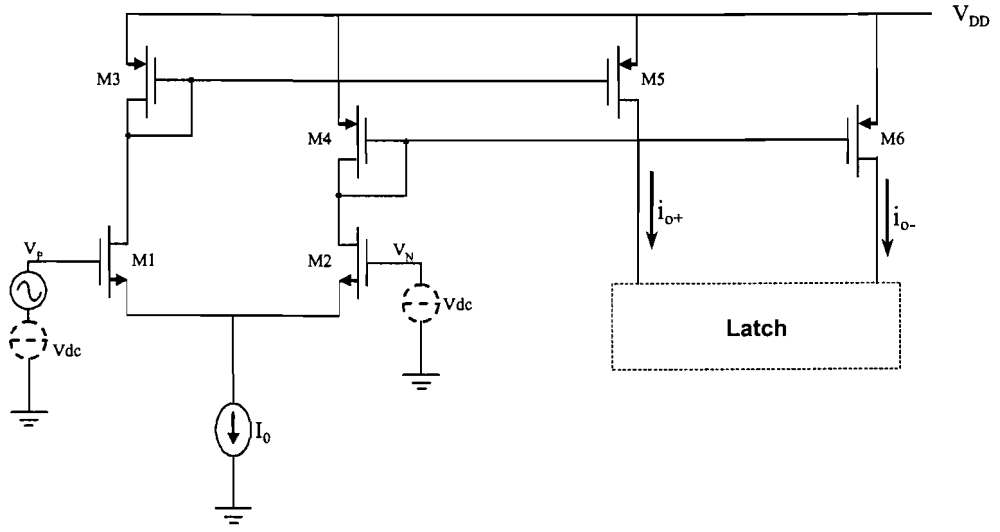


Figure 4.9: Design 2, preamplifier

In *figure 4.9* the preamplifier is shown. It is a differential amplifier with active load. The dimensions of M1 and M2 are set by considering the desired transconductance of this stage. Transconductance can be increased by either increasing the width of M1 and M2 or by increasing the bias current I_0. *Equations 4.8* presents the output current and the transconductance is defined by *equations 4.9*.

$$i_{0+} = \frac{g_m}{2}(V_+ - V_-) + \frac{I_0}{2} = I_0 - i_{0-} \tag{4.8}$$

$$g_m = g_{m1} = g_{m2} = \sqrt{(K'W/L)I_0} \tag{4.9}$$

Suppose that I_0 is set to 3mA, then the corresponding widths W3=W4=50μm. High g_m is desired and the choice is made for W1=W2=50μm. The calculated transconductance is g_m=9.1$\frac{mA}{V}$. In other words, if the input difference is 50mV, the output currents i_{0+} and i_{0-} are 1.725mA and 1.275mA, respectively.

In *figure 4.6* the total circuit of Design 2 is shown. It can be notice that this circuit is rather large, which is a major disadvantage.

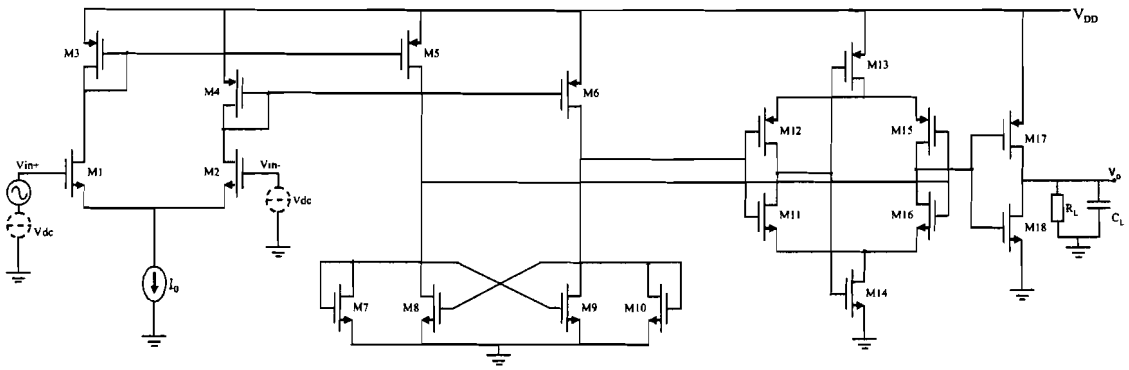


Figure 4.10: Design 2 Total circuit

In *table 4.1* the calculated dimensions (only for CMOS18 technology) are shown. These values will be used for the simulation at 500MHz. Higher frequencies will require more current or more preamplifiers and that will enormously increase the circuit size, which is not desired.

Technology	W/L (CMOS18)
M1=M2	50
M3=M4	50
M7=M8=M9=M10	5
M12=M13=M15	20
M11=M14=M16	7
M17	90
M18	35

Table 4.2: Design 2 calculated W/R ratios

4.4 Layout considerations

The bond-wires are used to connect the circuit to the outside world. Each bond-wire and its corresponding trace will be featured by the finite self-inductance. In practice these values will range approximately between 1nH and 10nH depending on the length of the wire and the type of package. It is also possible to approximate these values by using equations given in [3]. In the cases that the high transient currents are drown from the power-supply, the effect of the parasitics will be very large. The effect of bond-wires on the circuit performance is shown in *figure 4.11*, where inverter circuit is used. Suppose that the inverter is loaded by capacitance of 1pF and that the transition time is less than 0.5nsec, meaning that the inverter requires the current of $C\frac{\Delta V}{\Delta T} = 1pF\frac{1V}{0.5n} = 2mA$. This current is drown from the power supply V_{DD1} and GND_1 in 0.5nsec.

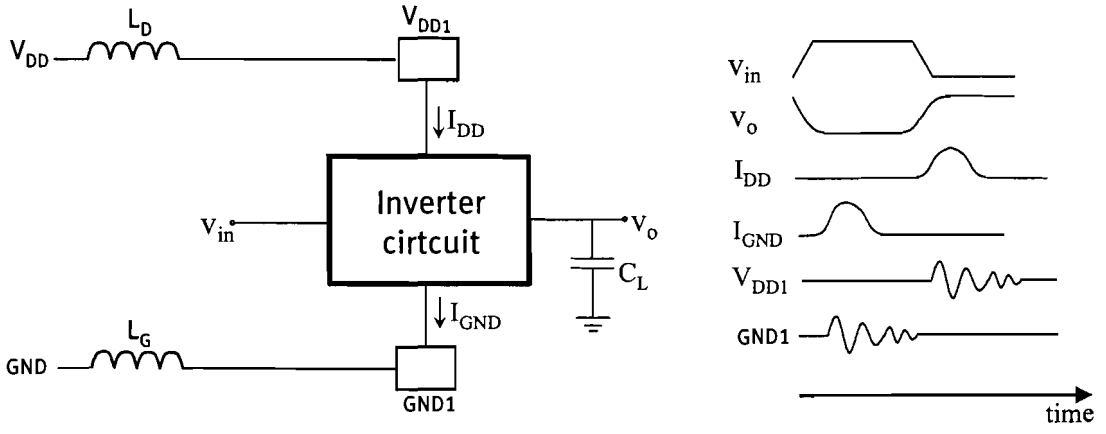
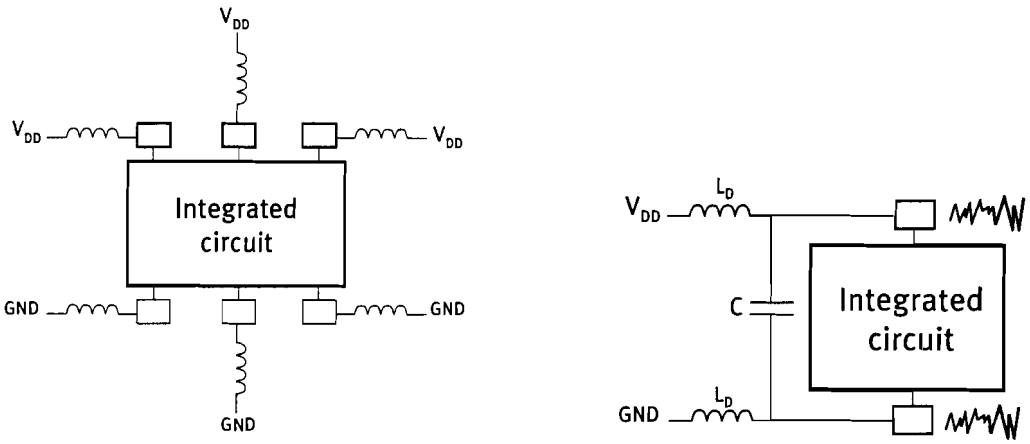


Figure 4.11: Bond-wire influence

The estimation of the voltage drop across the inductance L_D can be made by the use of relation, $L\frac{\Delta I}{\Delta t} = 5nF\frac{2mA}{0.5n} = 20mV$. This effect becomes important if the circuit power supply voltage is low.

The inductance bond-wire value can be minimized by use of parallel bond-wires (*figure 4.12(a)*), but this solution is rather expensive.

Another option is the use of a large on-chip capacitor in order to stabilize the difference between V_{DD} and ground. This is illustrated in *figure 4.12(b)*.



(a) Multiple wires method

(b) On-chip method

Figure 4.12: Reduction of the parasitic layout effect (methods)

The idea is that if the capacitance (C) is made large enough, then V_{DD} and GND bounce in harmony. If the differential stages are used, the noise reduction will be maximal. More information about layout influence can be found in [7] and [3].

Chapter 5

Simulations

A software tool Cadence is used to simulate the two designed comparators (*Design 1* and *Design 2*). Simulations are done with both technologies (CMOS18 and CMOS13). A sinusoid is used for the input signal and simulations are done at frequencies of 500MHz and 2GHz. Minimal amplitude is applied (50mV) and the propagation time delay is simulated. Furthermore the achieved gain, input-offset voltage and power dissipation are determined.

Influence of the layout is included into simulations. Monte Carlo analysis is used to predict the effect of mismatch and the layout parasitics. Also the presence of bond-wire inductance in the power-supply line is taken into account and the obtained simulation results are analyzed.

5.1 Design 1

In *figure 5.1* a circuit of Design 1 is shown. The widths of the MOS device are adjusted in the way that the minimal propagation time delay is obtained. The reference voltage V3 is set to 900mV and the input voltage is varying around this reference voltage. If the input is higher than 900mV the comparator output will become high.

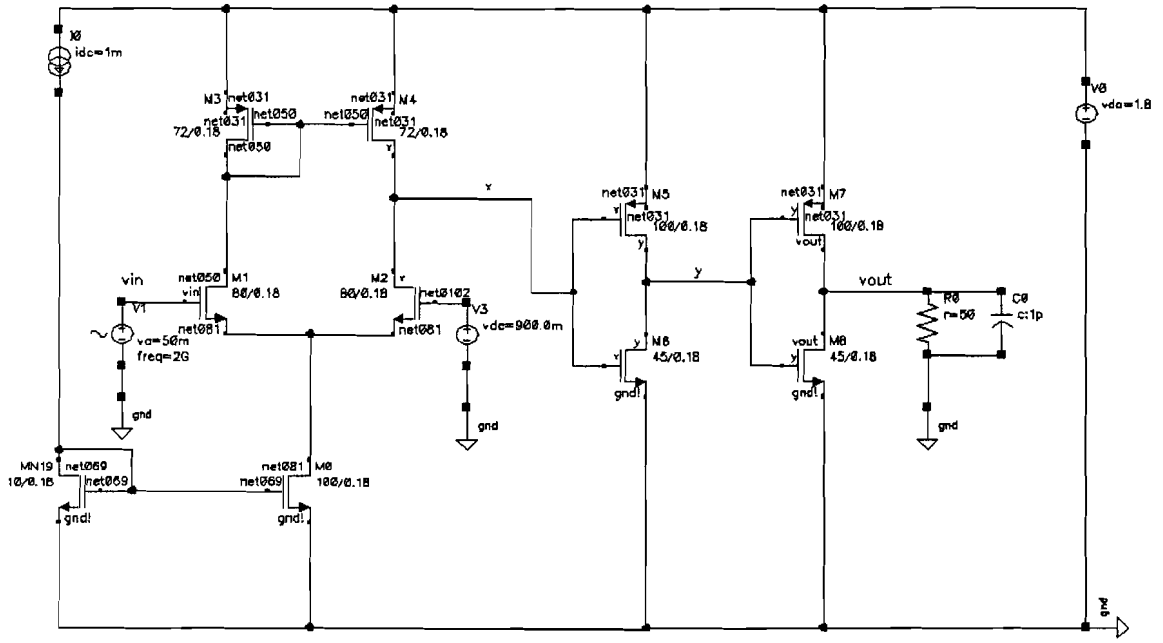


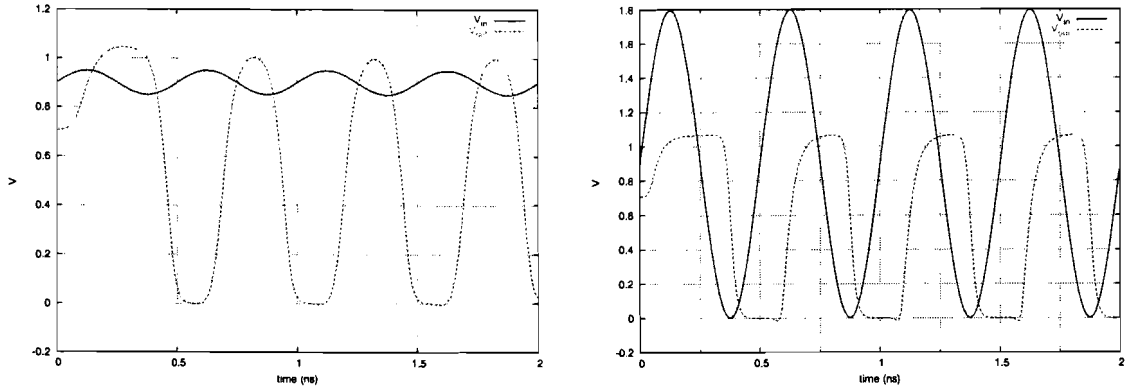
Figure 5.1: Design 1 circuit

The current mirror (consisting of M0 and MN19) is used to provide the input differential stage with the current of $\approx$ 7mA. The input signal is applied and voltage waveforms at nodes X, Y and Vout are observed. In the following section simulation results are presented.

5.1.1 Simulation results

***Design 1* with CMOS18 technology**

In *figure 5.2* the output signals are shown for two different input amplitudes at the frequency of 2GHz. If the input amplitude is set 50mV, the propagation time delay of t_p=200psec is obtained, (*figure 5.2(a)*). However, for the case of a full-swing input signal, the delay shortens to t_p=120psec,(*figure 5.2(b)*).

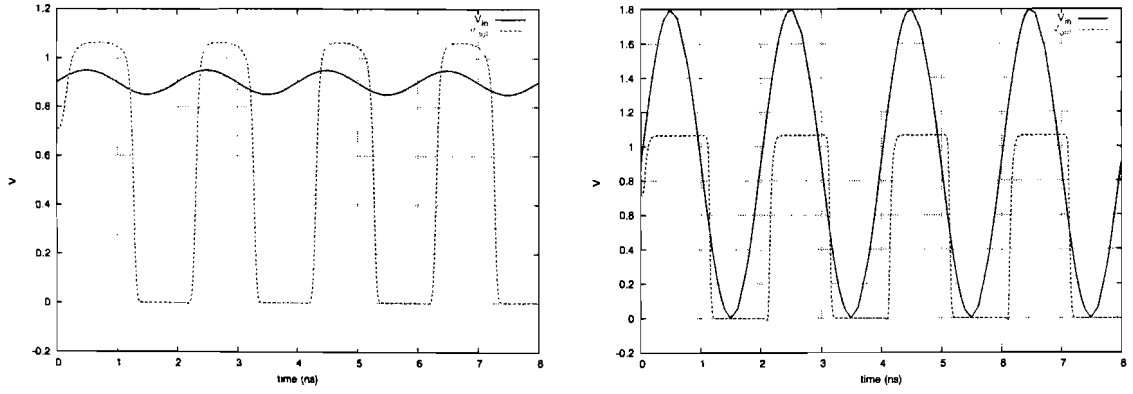


(a) Input (50mV) and output signal

(b) Input (900mV) and output signal

Figure 5.2: Design 1 (CMOS18), simulation results for 2GHz

The simulation results for operation at 500MHz are displayed in *figure 5.3*. If the input amplitude is 50mV, t_p=320psec and for amplitude of 900mV t_p=150psec.



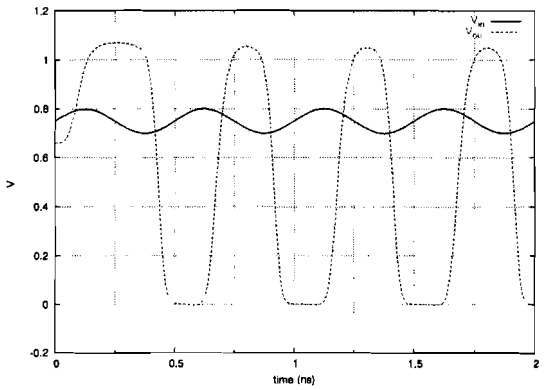
(a) Input (50mV) and output signal

(b) Input (900mV) andoutput signal

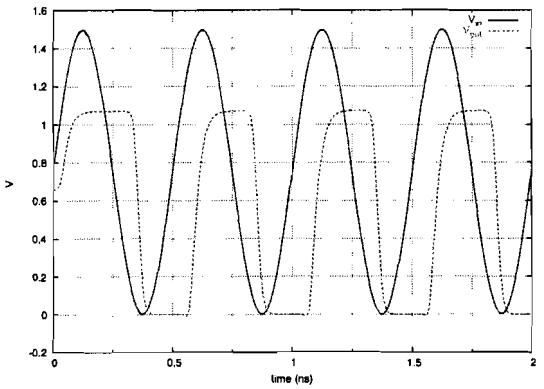
Figure 5.3: Design 1 (CMOS18), simulation results for 500MHz

***Design 1* with CMOS13 technology**

In *figure 5.4* the output signals are shown for two different input amplitudes (at 2GHz). If the input amplitude is 50mV (*figure 5.4(b)*), t_p=180psec is obtained. For full-swing input signal the (minimal) delay of t_p=120psec is achieved (*figure 5.4(a)*).



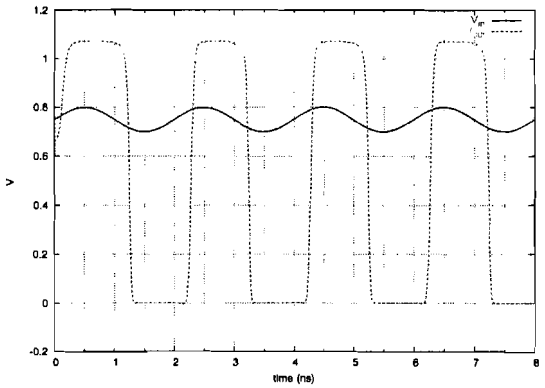
(a) Input (50mV) and output signal



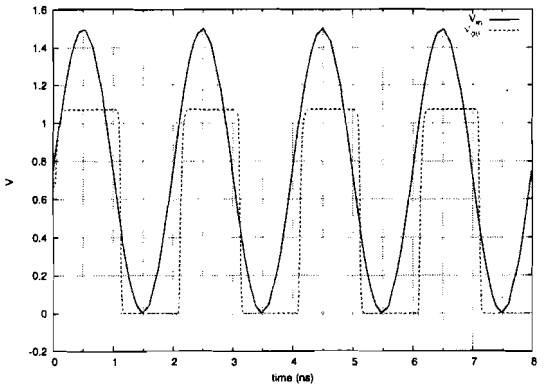
(b) Input (750mV) and output signal

Figure 5.4: Design 1 (CMOS13), simulation results for 2GHz

In case that applied input frequency is 500MHz simulation results are shown in *figure 5.5*. If the input amplitude is 50mV, t_p=290 and for amplitude of 750mV t_p=135ps.



(a) Input (50mV) and output signal



(b) Input (750mV) and output signal

Figure 5.5: Design 1 (CMOS13), simulation results for 500MHz

Input-offset voltage is simulated as shown in *figure 5.6*. V_{DC} is set to a certain dc-voltage level and the input is varied around this dc-voltage. The input-offset voltage is caused by the mismatch, and if the widths of MOS device are small, this input-offset voltage will become important. However, for Design 1, rather large MOS devices are used in order to obtain required speed. Hence, the input-offset voltage can be negligible. Simulations are done, and the value $V_{OS} \approx 1mV$ is obtained.

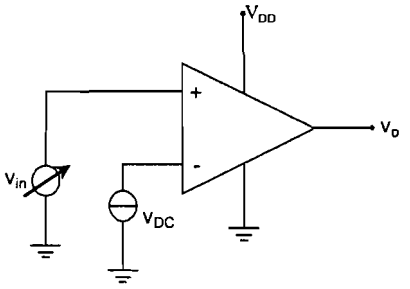


Figure 5.6: Input-offset simulation

5.1.2 Layout influence

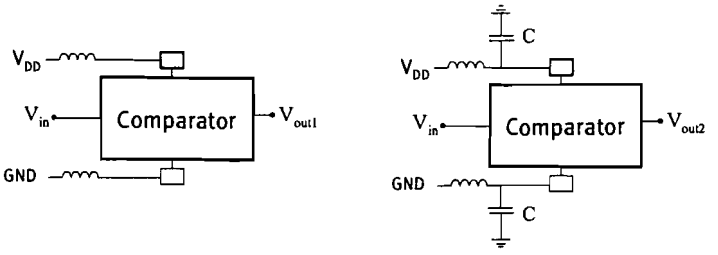
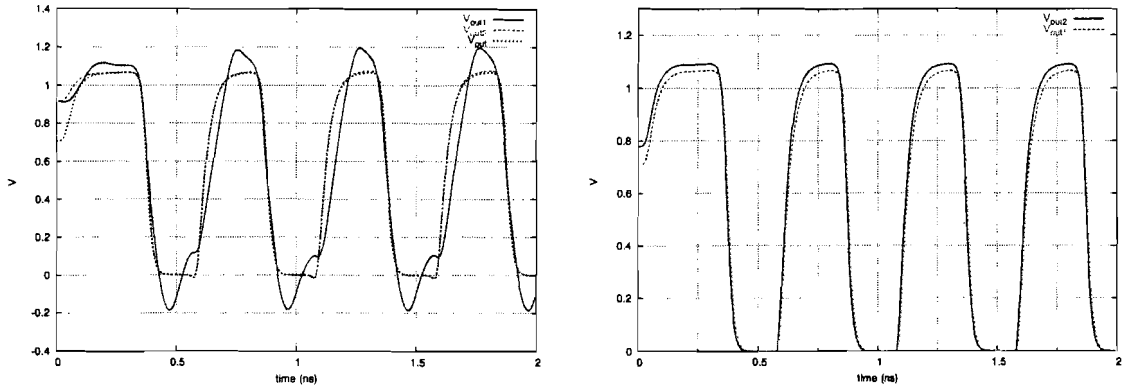


Figure 5.7: Layout inductance and on-chip capacitance

Figure 5.7 shows how the layout influences are included into circuit simulation. An inductance of 1nH is inserted into the power supply and grounding lines. The simulations are done and results are shown in *figure 5.8(a)*. V_{out1} is the output signal in the case that 1nH inductance is used. On-chip capacitance of 1pF is used to minimize this effect, and V_{out2} is obtained. Also the Monte-Carlo simulations are shown in *figure 5.8(b)*. Monte-Carlo simulation includes the influence of mis-match and process variation. The Monte-Carlo simulation results show that the output signal is almost unaffected by mismatch and by process variations.



(a) Bond-wire inductance (1nH) influence

(b) Monte-Carlo simulation

Figure 5.8: Layout parasitic influence

5.2 Results summary Design 1

Simulation results for the circuit operation at 2GHz and 500MHz are summarized in *table 5.2.* The simulations are done in both technologies CMOS18 and CMOS13. For the CMOS13 circuit lower widths are used than for circuit with CMOS18 technology, as shown in *Appendix A.3.*. Furthermore a lower propagation time delay is achieved for the circuit with CMOS13 technology as shown in table. This means that the CMOS13 technology is more suitable for the design. DC-power dissipation is simulated and is approximately 45mW, as shown in table.

Technology	CMOS18	CMOS13
Circuit operation at f=2GHz		
t_p for $V_{in} = 50mV$	200psec	180psec
t_p for $V_{in} = 900$ and $750mV$	120psec	100psec
DC-power dissipation	$\approx$ 45mW	$\approx$ 45mW
Input-offset voltage	<5mV	<5mV

Table 5.1: Design 1 Simulation results, for circuit operation at 2GHz

The Monte-Carlo simulations are done for both technologies and the conclusion is that the output signal is almost unaffected by the mismatch and the process variations. However, the inductance value introduced by the bond-wires will have major impact on the circuit performance. On-chip capacitance can be used in order to minimize this bond-wire influence.

5.3 Design 2

In *figure 5.9* a circuit diagram of Design 2 is shown. The widths of the MOS devices are adjusted in the way that the best circuit performance is obtained. The reference voltage is set to 900mV (V3) and the input voltage is varying around this reference voltage. If the input is higher than 900mV the comparator output will become high.

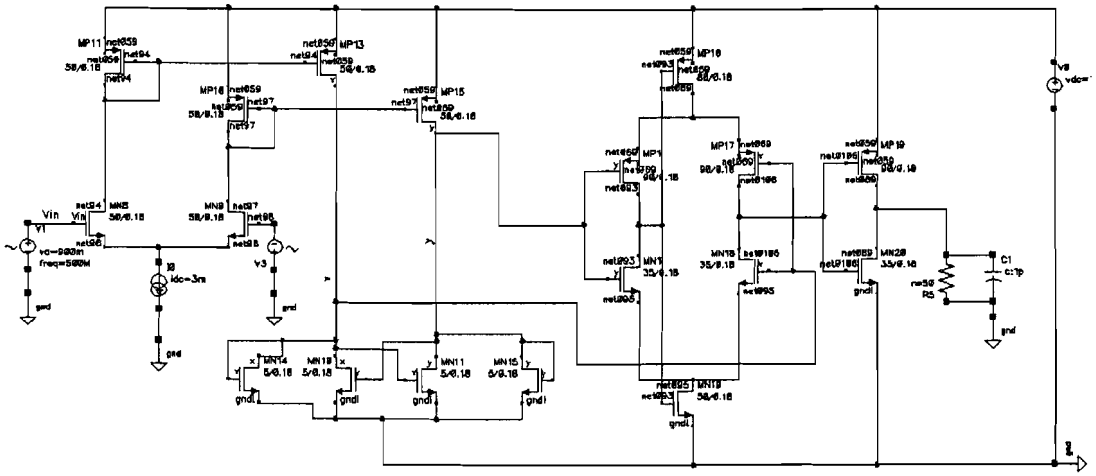
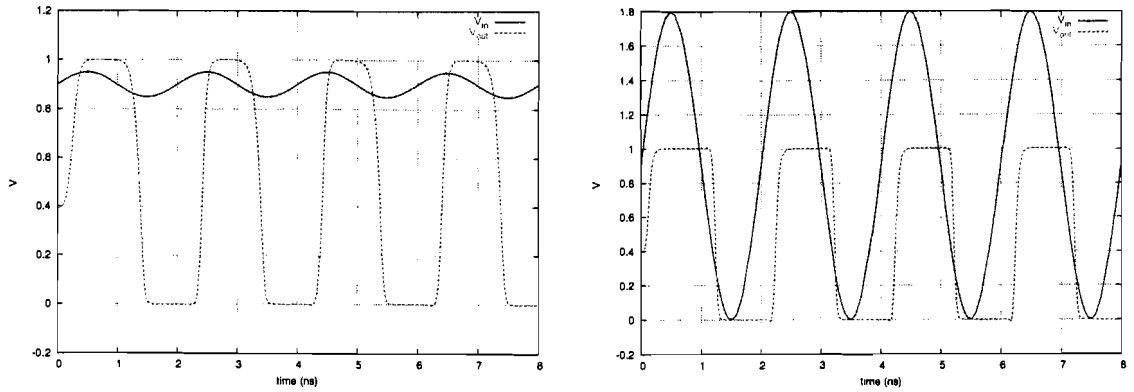


Figure 5.9: Design 2 circuit

The simulation results for the input signal of frequency f=500MHz are given in *figure 5.10*. If the input amplitude is 50mV, t_p=290 and for amplitude of 900mV, t_p=135ps.



(a) Input (50mV) and output signal

(b) Input (90mV) and output signal

Figure 5.10: Design 2 (CMOS18), simulation results for 500MHz

5.4 Results summary Design 2

Simulation results for the circuit operation at 500MHz are summarized in *table 5.2.* The simulations are done in both technologies CMOS18 and CMOS13. The propagation time delay of Design 2 is higher than for the Design 1. This is a result of the low resolution of the latch circuit. In order to lower the delay, more preamplifying circuits must be used. This however is not acceptable, because of increase circuit area. Furthermore, input-offset voltage is measured and the dc-power dissipation.

Technology	CMOS18	CMOS13
Circuit operation at f=2GHz		
t_p for $V_{in} = 50mV$	270psec	250psec
t_p for $V_{in} = 900$ and $750mV$	230psec	200psec
DC-power dissipation	$\approx$ 28mW	$\approx$ 28mW
Input-offset voltage	<10mV	<10mV

Table 5.2: Design 2 Simulation results, for circuit operation at 500MHz

Simulations of the Design 2 at 2GHz frequency are done, but the results are not acceptable, namely the large circuit area and high propagation time delay are not acceptable.

Chapter 6

Conclusions and recommendations

6.1 Conclusions

In this thesis the comparator circuits are investigated. Main application for this comparator is a transmitter architecture, based on the Duty-Cycle principle. The compactor circuit will provide sufficient voltage swing that will be applied to a class-S power amplifier.

The designs are mainly optimized for the low propagation time, minimal input resolution of 50mV and minimal circuit area. Based on the investigation of available circuit topologies, two designs are analyzed, *Design 1* and *Design 2*. The both designs are simulated with CMOS18 and CMOS13 technology and the comparison of the simulation results are made.

Design 1 is a open-loop comparator that consists out of three stages and thus has a minimal circuit size. The minimal propagation time delay of 100psec is achieved (with CMOS13 technology). The layout influence are included into simulations by introducing the bond-wire inductance into the power supply lines and by using the Monte-Carlo simulations. Bond-wire of 1nH has a major influence on the circuit performance. By use of the on-chip capacitance of 1pF (which is acceptable), this effect is minimized. Monte-Carlo simulation results show that the output signal is almost unaffected by mismatch and process variations.

Design 2 is a regenerative comparator that consists out of preamplifier, latch circuit and a output buffer. This design uses the advantage of the latch circuit. Latch circuit has a short response time and low power dissipation. Major disadvantage of the latch circuit is the low resolution. For the input frequency of 500MHz the simulation results are acceptable, however 2GHz operation would require more preamplifiers, which would increase the circuit size.

Furthermore, CMOS13 provides advantage of achieving lower propagation time delay with lower transistor widths. This technology advantage will improve the system performance.

6.2 Recommendations

Recommendations are mainly focused on the further project development. It is important to gain more information about the system requirements. The designed comparator circuit (*Design 1* or *Design 2*) can be used to build a *Duty-Cycle* based transmitter.
First step should be, lowering the input frequency (for example 10MHz) and analyzing the circuit behavior. The second step is to compare the circuit (Cadence) simulation results with the system-level simulation results (ADS, which are already available). If the results are matching and the power efficiency is acceptable, the input frequency should be increased and the circuits inside the loop will be optimized. By repeating these steps, the more specific performance requirements for the comparator, PA and loop-filter will be defined.

Furthermore, the noise influence should also be included into the system analysis. From the environment a high frequent peaks could lead to erroneous switching of the PA. These errors can not be recovered by the feedback, since they are filtered out by the loop filter. The errors could be minimized by proper shielding of the comparator and the power amplifier circuits.

Fully differential transmitter system will definitely provide best performance at GHz frequencies. PSRR and CMRR will improve if the differential system topologies are used.

Appendix A

Appendices

A.1 Project assignment

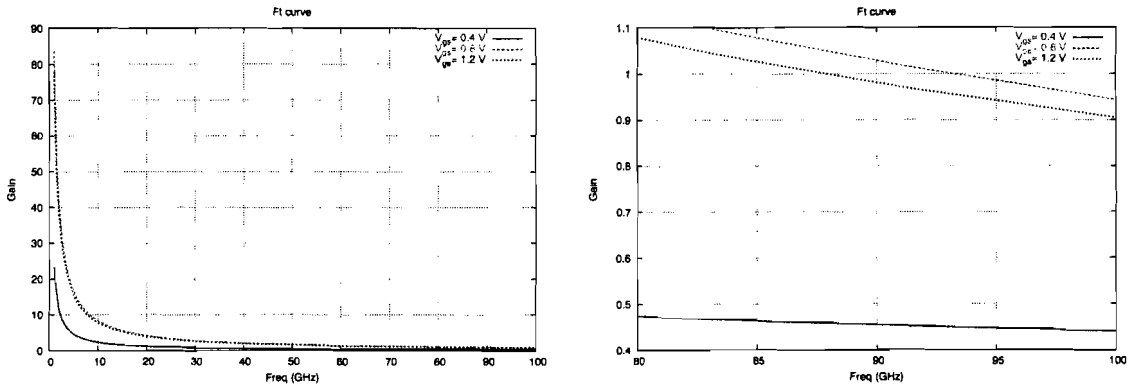
The main goal of the project is design and circuit implementation of the suitable driver stage for the Class-S Power Amplifier (PA) for RF applications. The driver stage should perform a hard limiting function (strong amplification and clipping) of the input signal at the GHz range of frequencies (up to 2GHz).

The driver circuit will operate in the large signal regime. It will be used as a buffer between the Sigma-Delta/Kappa modulation and the power amplifier of the transmitter, acting as a signal inverter and providing the appropriate signal conditioning for the input of the PA stage. The output signal from the driver is a rain of pulses with a variable frequencies and width. The driver must provide sufficient peak-to-peak voltage swing. It is important to achieve a high slope during the transient period, with the output signal rapidly varying between the two discrete amplitude states.

The following stage (Class-S power amplifier) will employ large power transistor whose input impedance will have a significant loading effect on the driver stage. Both the topology and Technology for the implementation of the driver circuit are not strictly defined, but are closely related to the topology of the class S PA. For example, the driver must be designed for low power consumption and efficient operation, since the efficiency of the driver is related in the efficiency equation of the whole system.

A.2 The unity current gain frequency simulations

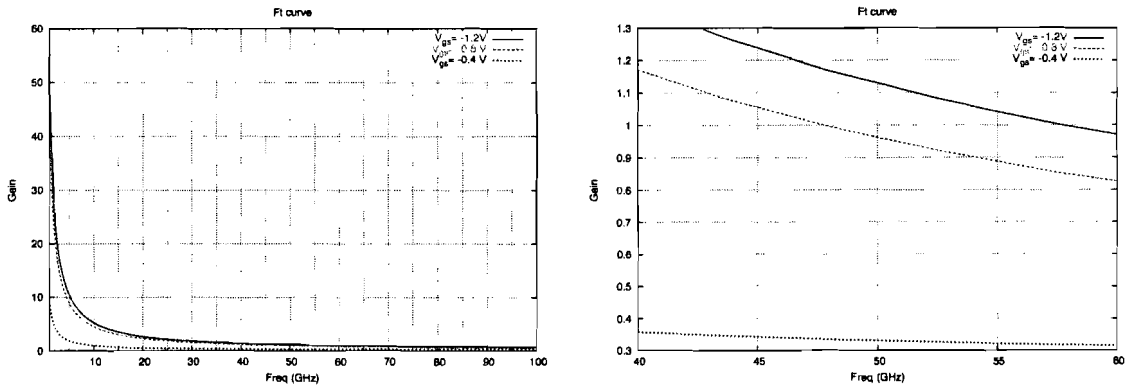
CMOS13



(a) f_t simulation, (range = 0 - 100GHz)

(b) f_t simulation, (range = 80 - 100GHz)

Figure A.1: N-channel CMOS 13 unity current gain frequency

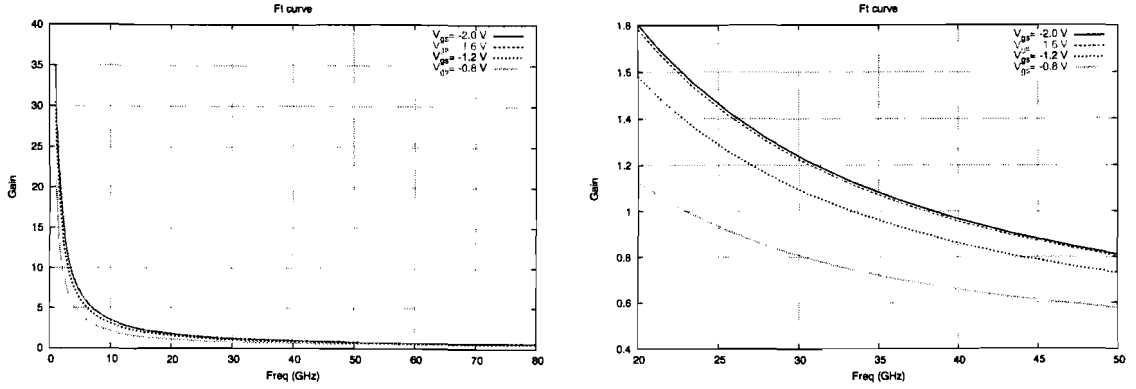


(a) f_t simulation, (range = 0 - 100GHz)

(b) f_t simulation, (range = 80 - 100GHz)

Figure A.2: P-channel CMOS 13 unity current gain frequency

CMOS18

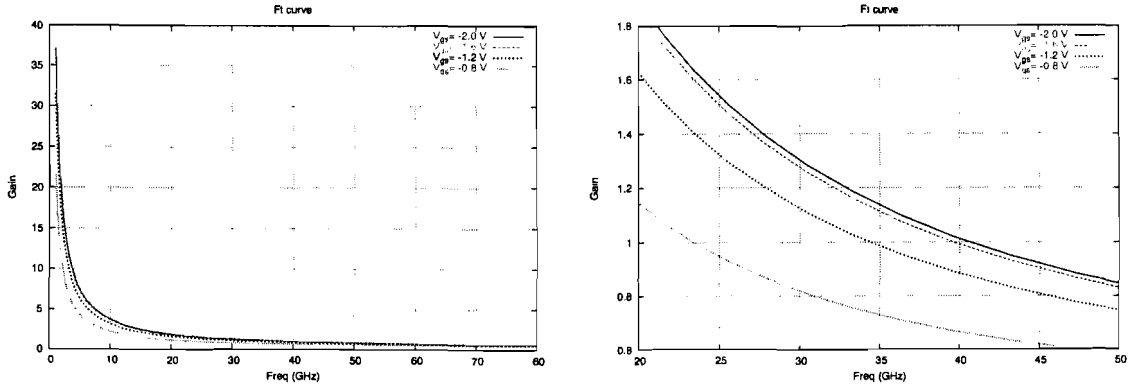


(a) f_t simulation, (range = 0 - 100GHz)

(b) f_t simulation, (range = 20 - 50GHz)

Figure A.3: P-channel CMOS 18 unity current gain frequency

CMOS18RF



(a) f_t simulation, (range = 0 - 100GHz)

(b) f_t simulation, (range = 20 - 50GHz)

Figure A.4: P-channel CMOS 18 RF unity current gain frequency

A.3 Design 1 in CMOS13 technology simulations

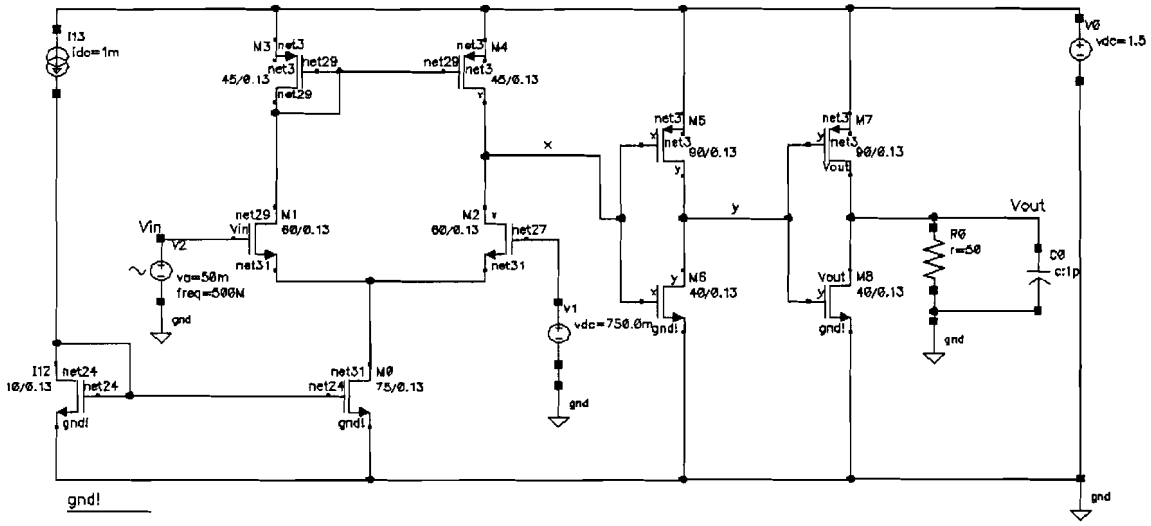


Figure A.5: Design 1 circuit, with CMOS13 technology

Bibliography

[1] Allen, P. E. and Holberg, D. R.
CMOS ANALOG CIRCUIT DESIGN, second edition.
New York, Oxford University Press Inc., 2002, ISBN 0-19-511644-5

[2] Gregorian, R.
INTRODUCTION TO CMOS OP-AMPS AND COMPARATORS
New York, John Wiley and Sons,Inc., 1999,
ISBN 0-471-31778-0

[3] Razavi, B.
DESIGN OF ANALOG CMOS INTEGRATED CIRCUITS
New York, The McGraw-Hill COmpanies, Inc., 2001,
ISBN 0-07-118815-0

[4] Baker, R. J. and Li, H. W. and Boyce, D. E.
CMOS CIRCUIT DESIGN, LAYOUT AND SIMULATION
New York, The Institute of Electrical ans Electronics Engineers,
Inc., 1998, ISBN 0-7803-3416-7

[5] Cripps, S. C.
RF POWER AMPLIFIERS FOR WIRELESS COMMUNICATIONS
London, Arthech House Publishers, Inc., 1999, ISBN 0-89006-989-1

[6] Gray, P. R. and Hurst, P. J. andLewis, S. H.
ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS
Newyork, John Wiley & Sons, Inc., 1999, ISBN 0-471-32168-0

[7] Hastings, A.
THE ART OF ANALOG LAYOUT
Pearson Education, 2000, ISBN 0-130-87061-7

[8] Kim, D.Y. and Kwon, O. S. and Bang, J. H.
THE DESIGN OF THE HIGH SPEED AMPLIFIER CIRCUIT FOR USING IN THE ANALOG SUBSYSTEM
Circuits and Systems, 1992., 9-12 Aug. 1992 P.485-488

[9] Wang, Z.H.
CMOS ADJUSTABLE SCHMITT TRIGGER.
IEEE Transactions on Instrumentation and Measurement. Vol. 40, June 1991, P.601-605

[10] AL-SARAWI, S.F.
LOW POWER SCHMITT TRIGGER CIRCUIT.
Electron. Lett., 2002, 38, (18), P.10091010

[11] Le, H.P. and Zayegh, A. and Singh, J.
PERFORMANCE ANALYSIS OF OPTIMISED CMOS COMPARATOR
Electronics Letters, Vol. 39 , Issue: 11 , 29 May 2003, P.833-835

[12] Wei-Shang, C. and Current, K.W.
A RAIL-TO-RAIL INPUT-RANGE CMOS VOLTAGE COMPARATOR
In: Circuits and Systems, Proceedings of the 40th Midwest Symposium,
Vol. 1, 3-6 Aug. 1997, P.160-163

[13] Bazes, M.
TWO NOVEL FULLY COMPLEMENTARY SELF-BIASED CMOS DIFFERENTIAL AMPLIFIER Solid-State Circuits, Feb 1991 , Vol. 26 ,P.165-168

[14] Razavi, B.
CMOS TECHNOLOGY CHARACTERIZATION FOR ANALOG AND RF DESIGN
Custom Integrated Circuits Conference, 1998., Proceedings of the IEEE 1998 , 11-14 May 1998 Pages:23 - 30