Design of a dual-band LNA in 0.18 um CMOS for DECT and Bluetooth

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Award date:
2004

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Design of a Dual-Band LNA in 0.18 μm CMOS for DECT and Bluetooth

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Master of Science Thesis

Project period: December 2003 - October 2004

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Group: Information and Communication Systems (ICS)
Chair: Mixed-signal Microelectronics (MsM)

Abstract

In order to develop a dual-band Low Noise Amplifier (LNA) in CMOS, two different designs are discussed. The frequencies of operation are 1.9 GHz and 2.4 GHz, because this LNA will be used in a DECT/Bluetooth front-end. Both of the presented LNA designs are based on a common-source amplifier with a cascode transistor. Therefore, the design parameters of a common-source amplifier are investigated thoroughly.

In practical applications, the LNA is connected to an antenna, which usually has an impedance of 50 Ω. In order to reduce reflection, an impedance matching between the antenna and the LNA is needed. Therefore, the LNA is designed to have a 50 Ω input impedance. The first topology presented, uses on-chip inductive degeneration to achieve matching. On-chip inductors occupy a large chip area. A method to minimize chip area is presented, which achieves on-chip matching at two frequencies using the same inductor. This way the inductors are reused at both frequencies. The gate inductor is implemented as a bondwire. This avoids the need for the second on-chip inductor, so chip area is reduced significantly. At a frequency of 1.9 GHz, this LNA design achieves a Noise Figure (NF) of 2.5 dB, an IIP3 of 0.5 dBm, an S11 of -16 dB and a gain of 17 dB. At a frequency of 2.4 GHz, it achieves a NF of 2.3 dB, an IIP3 of 3 dBm, a gain of 15 dB and an S11 of -14 dB.

The second LNA design uses an off-chip matching network. This matching network consists of two Microstrip transmission lines that are situated on the PCB. The matching network can again be reused by placing a capacitor between gate and source of the input transistor. This transistor is enabled or disabled by a transistor switch. This way, the same matching network achieves matching at 1.9 GHz as well as 2.4 GHz. For this LNA design, the following overall performance is achieved at 1.9 GHz: NF is 3.2 dB, IIP3 is 5 dBm, S11 is -11 dB and gain is 16 dB. At 2.4 GHz, it achieves a NF of 2.0 dB, an IIP3 of 5 dBm, a gain of 19 dB and an S11 of -12 dB.

Both designs are compared extensively. Particularly, cost-effectiveness of both designs is evaluated thoroughly. Because of the large chip area that is needed for the on-chip matching, this design approach is quite cost-ineffective. However, this design is fully integrated and a clear and simple design procedure is possible. Using off-chip matching has the disadvantage that the physical dimensions of Microstrip lines are large.

Contents

Chapter 1

Introduction

1.1 Project background

This Master Thesis project is part of the research in the context of the Ph.D. project of Vojkan Vidojkovic (M.Sc.). The Ph.D. project focuses on designing a single chip RF front-end for both DECT and Bluetooth and is illustrated in Figure 1.1. As the DECT and Bluetooth standards operate at two frequencies (1.9 GHz and 2.4 GHz), this system asks for dual-band building blocks. The Dual-Band Low Noise Amplifier (LNA) that is part of this system, is under investigation in this Master Thesis. This thesis continues the research on the LNA described in [3] and [7].

1.2 Design goal

The goal of this Master Thesis project is optimizing an inductively degenerated cascoded dual-band LNA, which is already available. Also, in the case of unsatisfying results, another design should be investigated and compared with the existing one.

1.3 Thesis overview

This thesis consists of two parts. The first one relates to the design and implementation of an inductively degenerated common-source LNA with on-chip matching. The second part is related to the design of a common-source

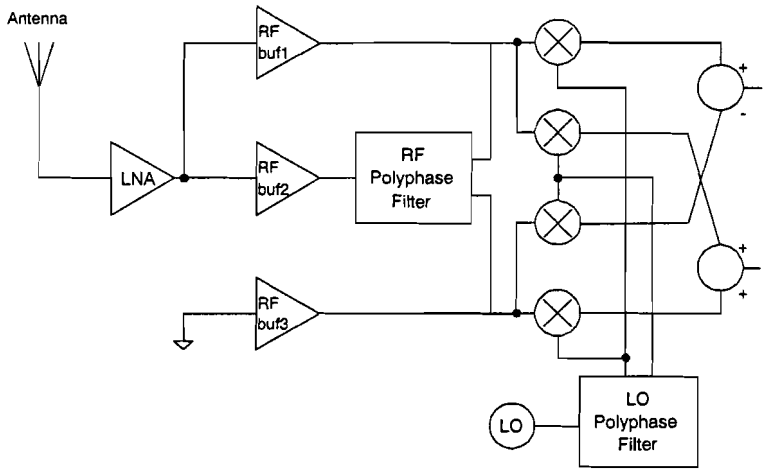


Figure 1.1: The RF Front-end that is designed in the Ph.D. project.

LNA with an off-chip matching network. At the end, two different LNA designs are compared. The advantages and disadvantages of both designs are discussed and based on that, final conclusions are drawn.

Chapter 2

Common-source amplifier

2.1 Introduction

The main performance parameters of a LNA, are gain, Noise Figure, linearity and power consumption.

To get an insight in the design of an amplifier, a very simple topology is under investigation. This amplifier consists of a common source stage, which is suitable for application as a LNA because of its small Noise Figure. Transistor size (W/L ratio), overdrive voltage ($V_{gs} - V_t$), drain resistance (R_d) and drain current (I_d) are the main parameters in this design. This amplifier is illustrated in Figure 2.1.

The following sections describe the influence of design parameters on the LNA performance. The design challenge is in the fact that the same set of LNA design parameters influences different functions of the LNA. Basically, all LNA functions can not be optimal in the same design. Therefore, some trade-offs must be made. These trade-offs are described thoroughly.

2.2 Voltage gain

A small-signal equivalent of the amplifier is constructed in order to determine the voltage gain (see Figure 2.2). This results in the following expression for

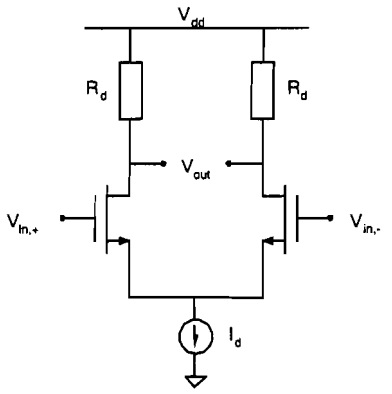


Figure 2.1: Differential Common-source Amplifier

the small-signal gain:

$$G = \frac{V_{out,+} - V_{out,-}}{V_{in,+} - V_{in,-}} = \frac{-g_m(V_{gs1} - V_{gs2})}{V_{in,+} - V_{in,-}} \cdot R_d = -g_m \cdot R_d \qquad (2.1)$$

In this expression (and the accompanying figures), R_d is the load resistance and g_m is the transconductance of the amplifying transistors.

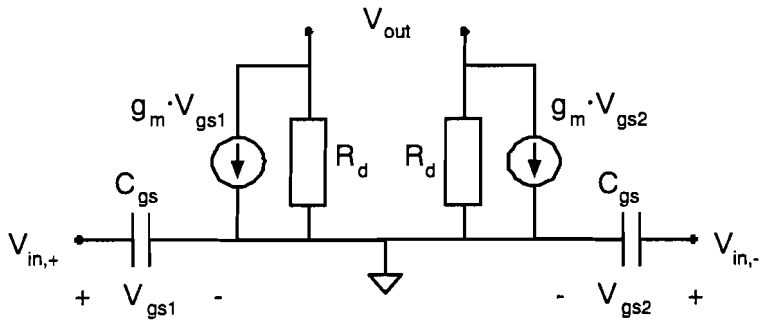


Figure 2.2: Small-signal Equivalent of a Differential Common-source Amplifier

Small-signal gain of the common-source amplifier depends on the load resistance and the transconductance, so the influence of R_d and g_m on the gain is investigated.

2.2.1 Load resistance R_d

Simulations are carried out to verify the relation between gain and load resistance R_d. In these simulations, the load resistance is varied. As is illustrated by Figure 2.3, the gain increases proportionally when R_d is increasing. This is the case for low values of R_d ($R_d < 200\ \Omega$).

Unfortunately, an increase of the load resistance also causes a decrease in the DC-voltage between drain and source of the transistors. As transistors should be in saturation to provide amplification, this puts a limit to the maximum achievable gain. The limit for a transistor to be in saturation is described by the following condition:

$$V_{ds} > V_{gs} - V_t \tag{2.2}$$

V_{ds} is the voltage between drain and source of the transistor, V_{gs} is the voltage between gate and source of the transistor, and V_t is the threshold voltage of the transistor. This is the reason why the relation between gain and R_d is less linear for higher values of R_d and why the gain drops for higher values of R_d.

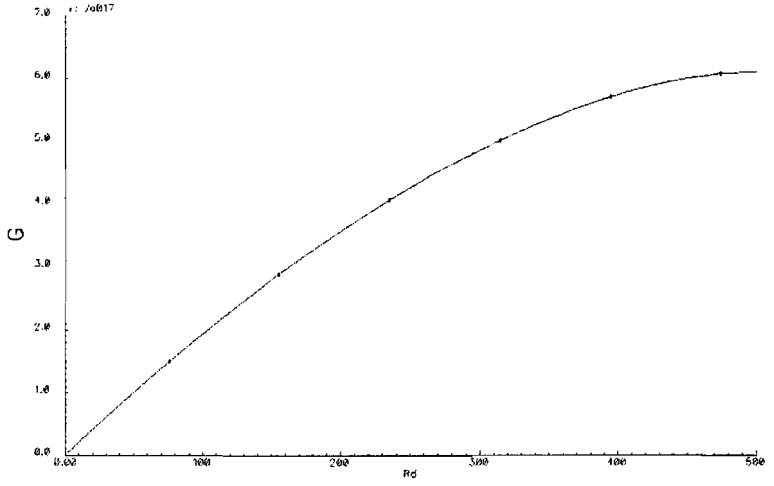


Figure 2.3: Gain as a function of R_d.

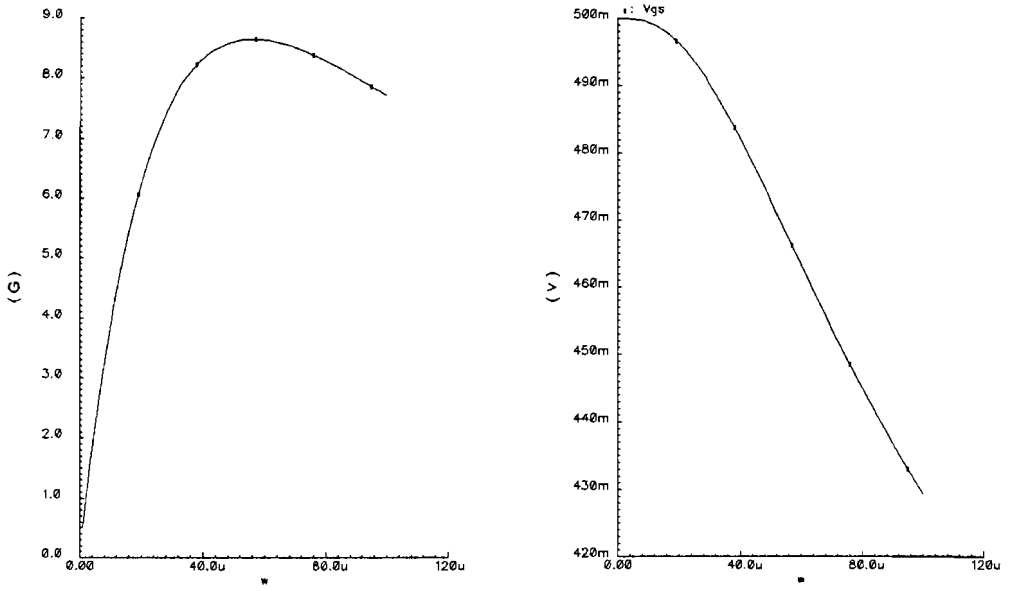
2.2.2 Transconductance g_m

The gain is also proportional to the transconductance (g_m) of the transistors. In [5], the following expression for g_m is given:

$$g_m = \sqrt{\mu_n C_{ox} \frac{W}{L} I_d} = \frac{I_d}{V_{gs} - V_t} \tag{2.3}$$

Increasing the drain current I_d would enable a larger gain. However, the current is limited because of power consumption limits.

As can be seen in (2.3), the transconductance can also be influenced by transistor dimensions. This behavior is verified by simulation results, which are shown in Figures 2.4(a) and 2.4(b). In these simulations, the transistor width W is varied for a fixed transistor length L (limited by technology, i.e. 0.18 μm). Also, the drain current is kept constant (5 mA). With these settings, the best transistor width can be determined.



(a) Gain as a function of W.

(b) V_{gs} as a function of W.

Figure 2.4: Simulation results for different values of W.

From (2.3), it is clear that the transistor width should be large to achieve a large g_m. Unfortunately, this also increases the parasitic capacitance between

gate and source. In this topology, this causes a decrease in the gate-source voltage of the transistor (Figure 2.4(a)), which results in a decrease of the gain (and a decrease of the linearity; see section 2.4).

2.3 Noise Figure

In general, Noise Figure (NF) is represented by the following equation [7]:

$$NF = 10\log\left(1 + \frac{2}{3g_m R_s} + \frac{1}{g_m^2 R_d R_s}\right) \tag{2.4}$$

This equation shows that the NF is related to the transconductance g_m. As the transistor width (W) has a large influence on g_m, it is a very interesting variable to investigate. A wider transistor realizes a higher transconductance and results in a lower NF. If the transconductance increases, the other terms in (2.4) will become more dominant, which is illustrated by the the lower limit in Figure 2.5.

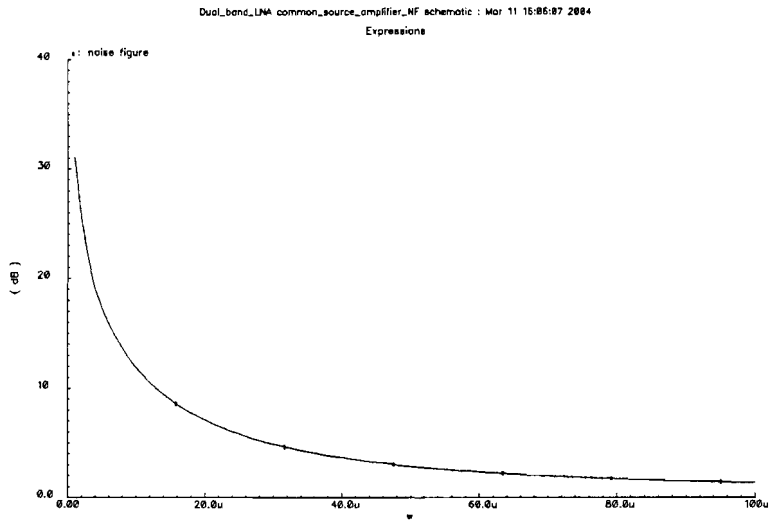


Figure 2.5: NF as a function of W.

Equation (2.4) also shows that NF is influenced by the load resistance R_d. This is illustrated by the simulation results in Figure 2.6. For increasing

values of R_d, NF becomes better. Again, this is limited by the saturation condition of the transistor (see section 2.2.1).

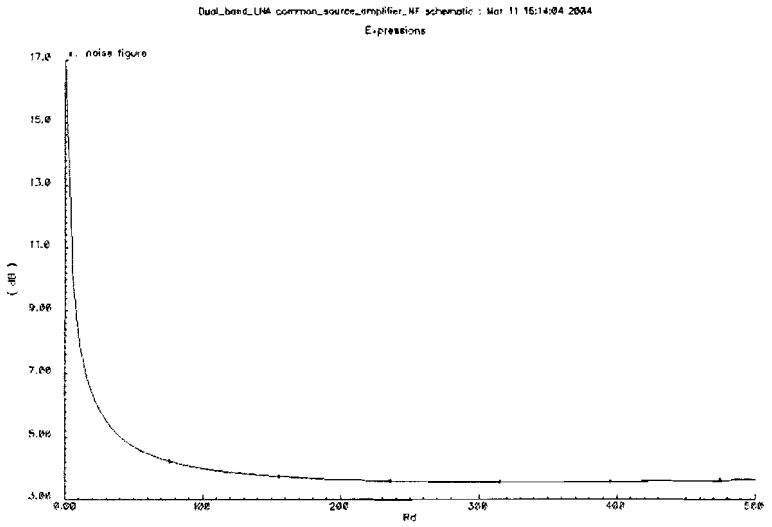


Figure 2.6: NF as a function of R_d.

2.4 Linearity

Linearity investigation is a complex task. In general, the linearity figure of merit ($IIP3$) is proportional to the overdrive voltage ($V_{gs} - V_t$) of the transistor (reference [7]). Simulations are carried out to confirm the validity of this approximation. Figure 2.7 illustrates the simulation results for varying the DC-voltage at the gates of the transistors. The maximum value for the gate-voltage is determined by the saturation conditions of the transistor.

2.5 Design flow

These experimental and theoretical results are used to suggest a design flow for a differential common-source amplifier. First of all, transistor width should be determined on the basis of power budget. Then, the overdrive voltage ($V_{gs} - V_t$) has to be chosen, to determine the value for g_m. A higher value for the overdrive voltage results in a higher linearity. This also has a

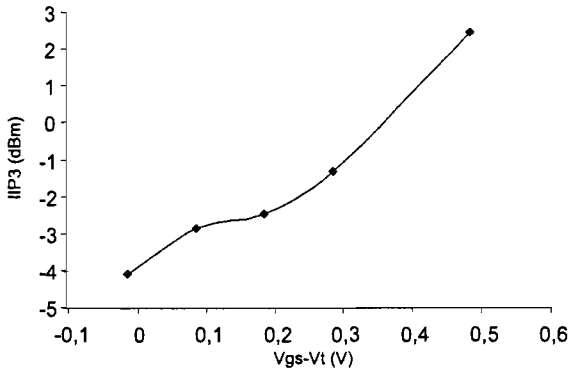


Figure 2.7: *IIP3* as a function of $V_{gs} - V_t$.

drawback because it is harder to keep the transistor in saturation.

When the transistor width is known, R_d should be chosen. The resistance should be large to provide maximal voltage gain and minimal noise. If it is too large, the transistor is no longer in saturation (process spread may even worsen this) and linearity is decreasing.

Chapter 3

Cascoded LNA with on-chip matching

3.1 Introduction

The common-source amplifier is not directly applicable as LNA in a system. As it is placed directly after the antenna, input impedance matching has to be considered at two different frequencies. Furthermore, LNA performance should not be influenced by the load. These issues and their consequences are discussed in the following sections. Afterwards, some implementation considerations are discussed and simulation results are presented.

3.2 Impedance matching

3.2.1 Inductive degeneration

Figure 3.1 depicts an inductively degenerated cascoded LNA. The inductive degeneration takes care of impedance-matching at a desired frequency. The cascode stage takes care of the isolation of the load. There are several other topologies that achieve these input- and output-requirements as well, but choosing between these topologies is beyond the scope of this document.

It is assumed that input impedance should be matched to 50 Ω to have minimal reflection. The gate-inductor is too large when matching has to be achieved with the intrinsic parasitic capacitor between gate and source

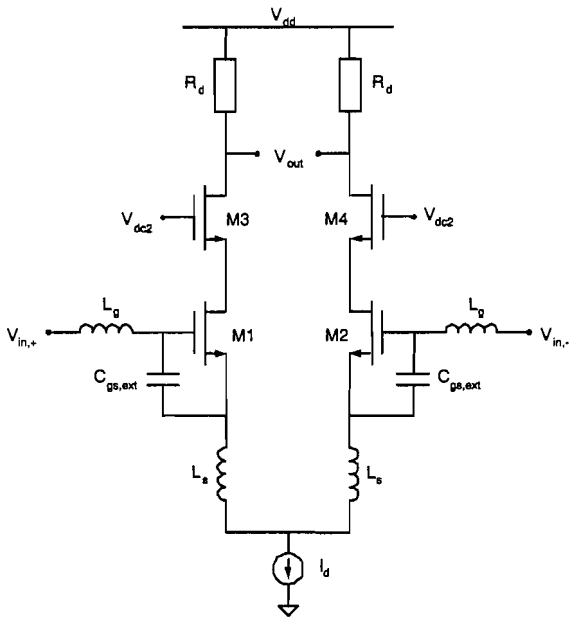


Figure 3.1: Inductively degenerated cascoded LNA.

(C_{gs}). Therefore, an external capacitor is added between gate and source. When body-effect is not significant, the input impedance is represented by the following equation:

$$Z_{in} = \frac{1}{j\omega C_{gs}} + j\omega(L_s + L_g) + g_m \frac{L_s}{C_{gs}} \tag{3.1}$$

For impedance matching, the imaginary part of (3.1) has to be equal to zero:

$$\omega(L_s + L_g) - \frac{1}{\omega C_{gs}} = 0 \tag{3.2}$$

Substituting (3.2) into (3.1), the input impedance can be expressed as:

$$Z_{in} = \frac{g_m}{C_{gs}} L_s \tag{3.3}$$

Using $n = \frac{L_g}{L_s}$, this results in the following expressions.

$$L_s = \sqrt{\frac{R_s}{(n+1)g_m\omega^2}} \tag{3.4}$$

$$C_{gs,total} = \sqrt{\frac{g_m}{(n+1)R_s\omega^2}} \tag{3.5}$$

3.2.2 Dual-band impedance matching

Impedance matching at two frequencies can be done using another pair of inductors. Since inductors occupy a lot of chip area, this is unwanted. A design which reuses the previously designed inductors for both frequencies, is described in [7] and is depicted in Figure 3.2. In this design, the extra capacitor C2 is placed in parallel with the external capacitor C1 that is described in the previous section.

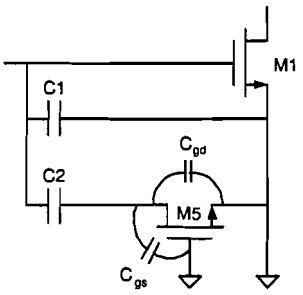


Figure 3.2: Dual-band switching components.

The switching transistor M3 is used in series with the extra capacitor C2. If the transistor is on (and it is well designed), it has virtually no effect on the total capacitance. If it is switched off however, the extra capacitor is situated in series with the combination of the drain-gate and drain-source parasitic capacitances. This affects the total capacitance so it should be considered when calculating the band-switching capacitor.

Also, the transconductance of the input transistor should be changed in order to be able to match at the other frequency. This transconductance can be adapted by changing its DC setting.

3.3 Gain

In principle, most gain parameters are the same as in the common-source amplifier so it is still proportional to R_d and g_m. However, the improvement in the output impedance by using a cascode stage, also influences the gain.

The DC voltage of the cascode transistor (V_{dc2}) is important to keep both transistors in saturation. If V_{dc2} is low, the source voltage of the cascode transistor is low as well. At the same time, this voltage is the drain voltage of the input transistor (M1 or M2). Therefore V_{dc2} also has to be large enough to keep it in saturation. The drain voltage of the cascode transistor is fixed because of the constant drain current. In Figure 3.3, this is illustrated by simulation results.

The drain voltage of the cascode transistor is constant because of the fixed current through the load resistor. As is stated before, the source voltage of this transistor increases for increasing V_{dc2}. This means a decrease in the drain-source voltage of the cascode transistor as well. So if V_{dc2} is too large the cascode transistor itself is no longer in saturation, which provides the upper limit to this voltage. This effect is visible in Figure 3.3, because the the output voltage is decreasing again for $V_{dc2} > 1.7$ V.

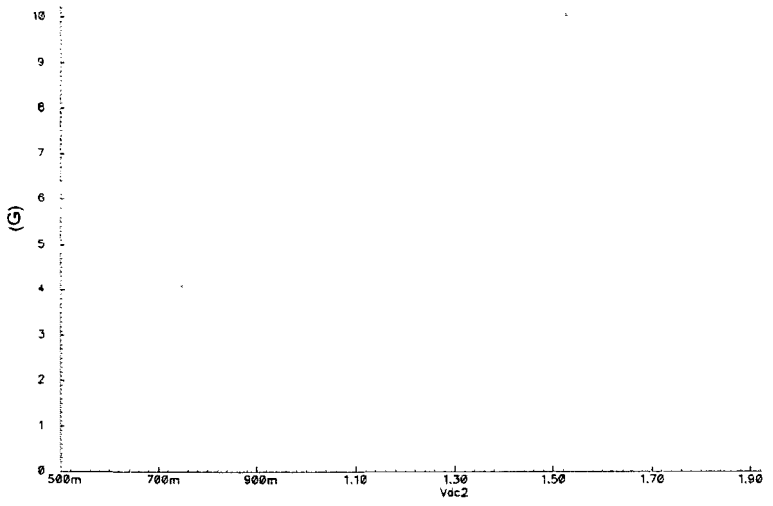


Figure 3.3: Gain as a function of the Cascode Transistor Voltage.

The width of the cascode transistor influences gain as well. This transistors (M3 and M4) should be large enough to keep the amplifying transistors (M1 and M2) in saturation. The upper limit to the transistor width is caused by the gain reduction due to parasitics. A larger transistor has a larger parasitic capacitance between gate and drain and between gate and source. Through these parasitics, signal leaks and therefore the gain is reduced.

3.4 Noise Figure

If the cascode-transistor is in saturation, it does not influence Noise Figure. The inductive degeneration however, does change the Noise Figure properties. In [7], the following general equation is explained:

$$NF = 10\log\left(1 + \frac{R_{L_g} + R_{L_s}}{R_s} + \gamma g_{d0} R_s \left(\frac{\omega C_{gs_t}}{g_m}\right)^2 + \frac{(\omega L_s)^2}{R_s R_d}\right) \tag{3.6}$$

R_{L_g} and R_{L_s} are the series resistances of the inductors, which are determined by inductor values and quality factors. Quality factors are dependent on the technology in which the inductors are implemented. g_{d0} is the zero bias drain conductance and γ is the coefficient of channel thermal noise. R_s is the fixed source resistance.

Using the matching conditions, it is possible to calculate NF when matching is achieved. This yields the following expression for the Noise Figure at matching frequency:

$$\begin{aligned} NF = & 10\log(1 + \sqrt{\frac{1}{g_m R_s}}\left(\frac{n}{\sqrt{n+1}Q_{L_g}} + \frac{1}{\sqrt{n+1}Q_{L_s}}\right) + \\ & \gamma\frac{g_{d0}}{g_m}\frac{1}{n+1} + \frac{1}{(n+1)g_m R_d}) \end{aligned} \tag{3.7}$$

It is important to notice that NF no longer depends on the individual inductor values, but on the ratio $n = \frac{L_g}{L_s}$. The expected influence of n on the Noise Figure is verified with simulations (see Figure 3.4).

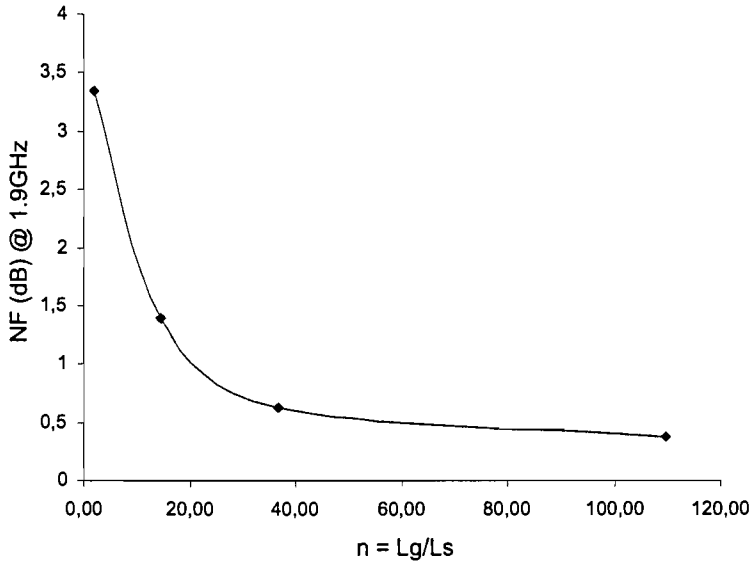


Figure 3.4: *NF* as a function of n ($n = L_g/L_s$).

Furthermore, the Noise Figure depends on the transconductance g_m of the input transistor. Figure 3.5 illustrates the relation between *NF* and the input transistor width ($W0$). This behavior practically is the same as for the common-source amplifier (see section 2.3).

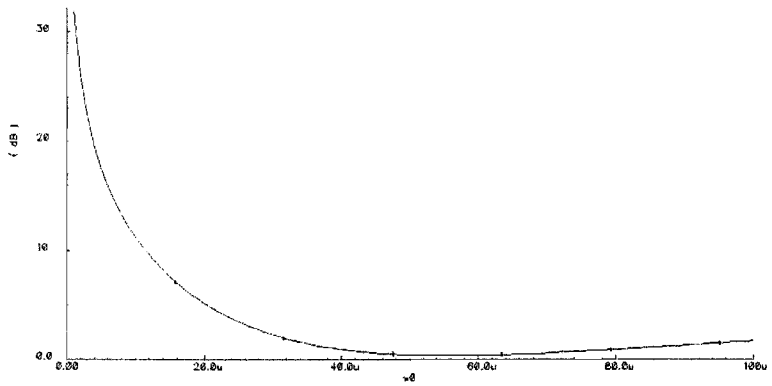


Figure 3.5: *NF* as a function of the width of transistor M1.

3.5 Linearity

The influence of the gate-source voltage of transistor M1 (V_{gs}) on linearity is simulated in order to compare this amplifier with the common-source amplifier. Figure 3.6 shows the simulation results for *IIP3*. It can be concluded that this is significantly less, but still proportional to V_{gs}.

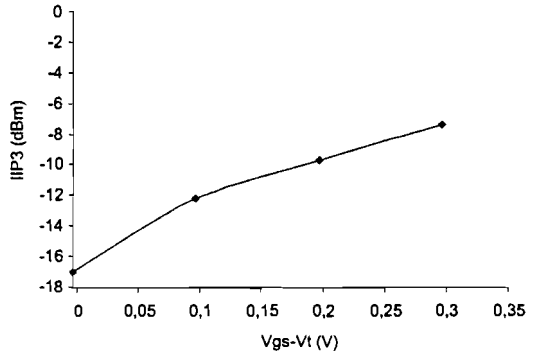


Figure 3.6: *IIP3* as a function of $V_{gs} - V_t$.

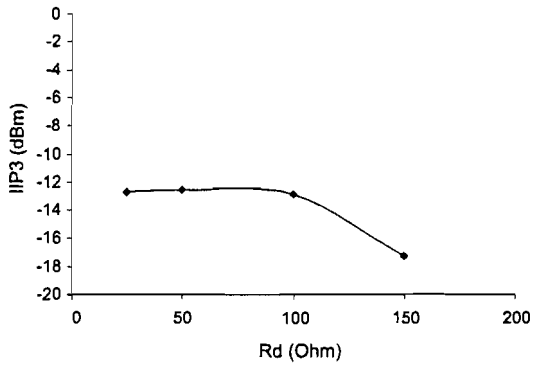


Figure 3.7: *IIP3* as a function of R_d.

As is stated in section 2.4, R_d has an impact on linearity as well. Linearity simulations are carried out for different values of R_d to investigate whether this still is the case for the inductively degenerated LNA. The results of these simulations are depicted in Figure 3.7. From this picture, it is clear that the

linearity is virtually constant for different load resistances. The linearity decreases dramatically only when the resistance value is too high to keep both transistors in saturation.

3.6 Implementation considerations

In the design of the LNA, the physical size of the layout of the inductors must be taken into account. The inductors in the design described in the previous chapter, occupy large amounts of chip area. Therefore, it is beneficial to implement an inductor as bondwire. Unfortunately, this is only possible for the gate inductance, because this is the only inductor that will be connected to a bondpad. Furthermore, the size of a bondwire is limited, which is discussed in section 3.6.1.
The source inductor will be implemented as planar on-chip inductor. This kind of inductances suffer from very limited quality factors. The design of planar on-chip inductors will be explained in 3.6.2. Also, packaging of the chip introduces unwanted capacitances and inductances. This will be discussed in section 3.6.3. With this knowledge a layout is constructed, which reveals some more difficulties. At the end of this chapter, the consequences of this research are used to suggest some directions for further research.

3.6.1 Bondwire inductance size limitation

On-chip inductors of about 1 nH already occupy very large amounts of chip area. As the largest inductor (L_g) is implemented as bondwire, a lot of chip area is saved. An extra advantage lies in the relatively high quality factor of bondwires. Unfortunately, the size of a bondwire is limited to 3 mm because of production considerations. Assuming that the average inductance of a bondwire is 1 nH/mm, the gate inductor is limited to 3 nH. This inductor is significantly smaller than calculated for minimal Noise Figure (see section 3.4). For this reason, the design is reviewed for a gate inductor of 3 nH.

A smaller gate inductor has the drawback that the source inductor is significantly larger to achieve impedance matching. Unfortunately, this has two negative consequences. Firstly, the ratio n becomes smaller, which deteriorates the Noise Figure. Secondly, body-effect turns out to be significant for source inductor values of 1-3 nH.

In order to include the body-effect in the calculations, the small-signal equivalent of the transistor is extended. In the new small-signal equivalent of the amplifier, the body-effect is modeled by an additional current source parallel to $g_m V_{gs}$ (see Figure 3.8).

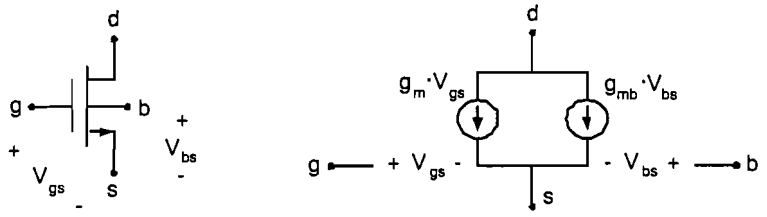


Figure 3.8: Transistor with extended small-signal equivalent.

With this improvement, the body-effect is now taken into account in the calculation of gain, L_s, and L_g. The size of this current source is $g_{mb}V_{bs}$. This yields the following Kirchoff equations:

$$\frac{V_g - V_{in}}{j\omega L_g} + j\omega C_{gs}(V_g - V_s) = 0 \tag{3.8}$$

$$j\omega C_{gs}(V_g - V_s) + \frac{V_s}{j\omega L_s} - g_m V_g + (g_m + g_{mb})V_s = 0 \tag{3.9}$$

$$\frac{V_{out}}{R_d} + g_m V_g - (g_m + g_{mb})V_s = 0 \tag{3.10}$$

Which easily provide the relation between V_{gs} and V_{in}.

$$V_{gs} = \frac{V_{in}}{1 - \omega^2 C_{gs} L_g + \frac{j\omega L_s(g_m + j\omega C_{gs})}{1 + j\omega L_s g_{mb}}} \tag{3.11}$$

This results in an expression for the input impedance of this amplifier stage:

$$\begin{aligned} Z_{in} &= \frac{V_{in}}{I_{in}} \\ &= \frac{V_{in}}{V_{gs} \cdot j\omega C_{gs}} \\ &= \frac{V_{in}}{j\omega C_{gs}} \cdot \frac{1 - \omega^2 C_{gs} L_g + \frac{j\omega L_s (g_m + j\omega C_{gs})}{1 + j\omega L_s g_{mb}}}{V_{in}} \\ &= \frac{1}{j\omega C_{gs}} + j\omega L_g + \frac{g_m \frac{L_s}{C_{gs}} + j\omega L_s}{1 + j\omega L_s g_{mb}} \end{aligned} \tag{3.12}$$

To obtain an expression for the Gain at the matching frequency, equations (3.8) and (3.10) are combined:

$$\frac{V_{out}}{R_d} + g_m \left(\frac{\frac{V_{in}}{j\omega L_g} + V_s j\omega C_{gs}}{\frac{1}{j\omega L_g} + j\omega C_{gs}} \right) - (g_m + g_{mb}) V_s = 0 \tag{3.13}$$

Furthermore, taking into account (3.9), the relation between V_s and V_{in} is determined:

$$\frac{V_s}{V_{in}} = \frac{j\omega C_{gs} + g_m}{\frac{1}{j\omega L_s} + g_m + g_{mb} + \left(\frac{L_g}{L_s} + 1 \right) j\omega C_{gs} - g_{mb} \omega^2 C_{gs} L_g} \tag{3.14}$$

Combining these relations (3.13) and (3.14), the gain (at the matching frequency) can be determined:

$$Gain = \frac{(g_{mb} j\omega L_s - \frac{g_m}{j\omega C_{gs}})(1 - \omega^2 C_{gs} L_g)}{\frac{1}{j\omega C_{gs}} + g_m \frac{L_s}{C_{gs}} + j\omega (L_s + L_g) + g_{mb} \left(\frac{L_s}{C_{gs}} - \omega^2 L_s L_g \right)} \cdot R_d \tag{3.15}$$

Assuming that the LNA impedance should be matched for the source resistance R_s. Therefore the following 2 equations can be written:

$$\mathrm{Re}(Z_{in}) = R_s = \frac{g_m \frac{L_s}{C_{gs}} + \omega^2 L_s^2 g_{mb}}{1 + (\omega L_s g_{mb})^2} \tag{3.16}$$

$$\mathrm{Im}(Z_{in}) = 0 = \omega L_g - \frac{1}{\omega C_{gs}} + \frac{\omega L_s - \omega g_m g_{mb} \frac{L_s^2}{C_{gs}}}{1 + (\omega L_s g_{mb})^2} \tag{3.17}$$

Using $n = \frac{L_g}{L_s}$, this results in the following expressions.

$$L_s = \sqrt{\frac{R_s}{g_m\omega^2\left(n+1+g_{mb}\left(\frac{1-R_s}{g_m}-R_s\right)\right)}} \tag{3.18}$$

$$C_{gs} = \frac{\sqrt{\frac{g_m^3}{R_s\omega^2}\left(n+1+g_{mb}\left(\frac{1-R_s}{g_m}-R_s\right)\right)}}{g_m(n+1)+g_{mb}\left(R_s g_{mb}-1+g_m\left(\frac{1-R_s}{g_m}-R_s\right)\right)} \tag{3.19}$$

As body-effect is now taken into account, new component sizes will be used to obtain impedance matching. The simulation results in Figure 3.9 illustrate the advantage in matching in this new approach.
In calculations without body-effect parameters, the component sizes are: $L_g = 3$ nH, $C_{gs,ext} = 1.2$ pF, $L_s = 1.9$ nH. These values are different when body-effect is introduced in the calculations: $L_g = 3$ nH, $C_{gs,ext} = 1.5$ pF, $L_s = 2.2$ nH.

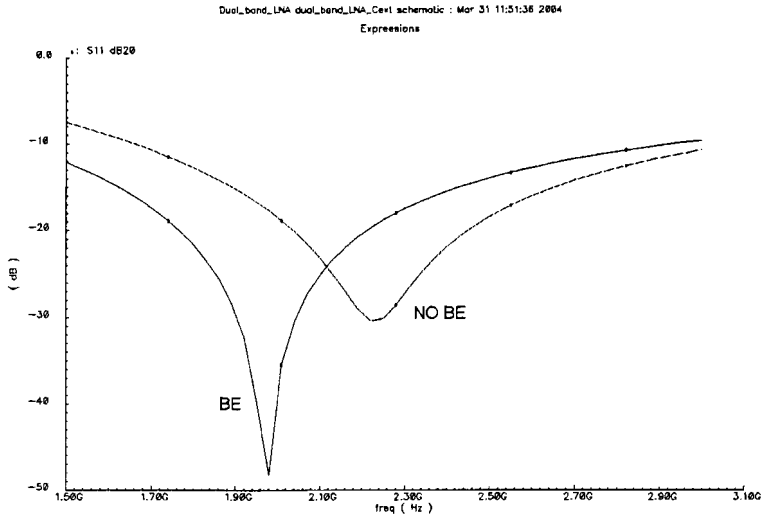


Figure 3.9: "**NO BE**": S11 when body effect is not taken into account. "**BE**": S11 when body effect is taken into account.

The improvement in impedance matching is at the cost of making gain and Noise Figure worse. The differences in gain and Noise Figure are illustrated in Figure 3.10 and Figure 3.11, respectively.

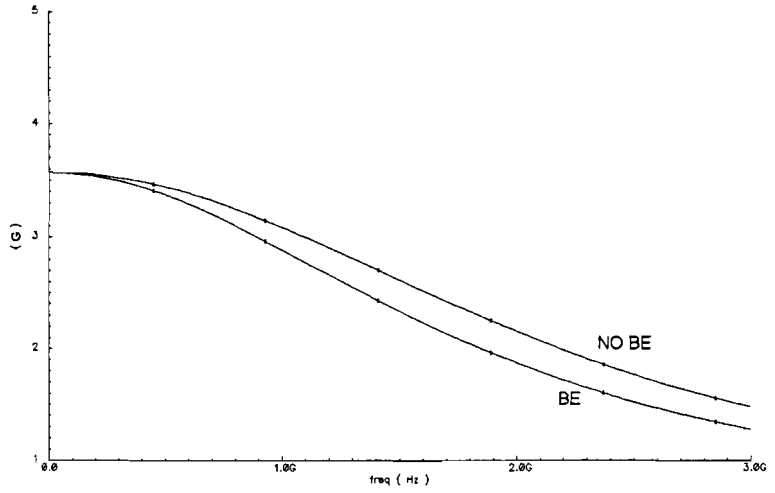


Figure 3.10: Difference in gain when body effect is not taken into account ('NO BE') when body effect is taken into account ('BE').

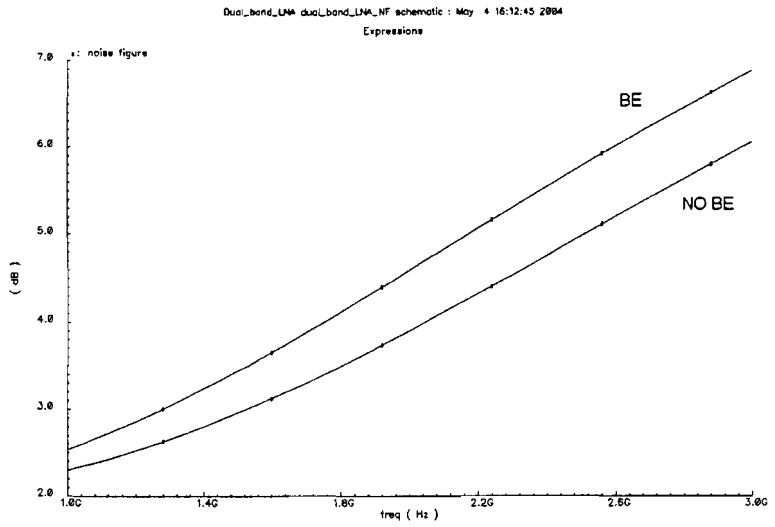


Figure 3.11: Difference in Noise Figure when body effect is not taken into account ('NO BE') when body effect is taken into account ('BE').

3.6.2 Planar inductor limitations

In [1], CMOS planar inductor design is explained. The geometric programming model is used to model an octagonal inductor. The model is depicted

in Figure 3.12.

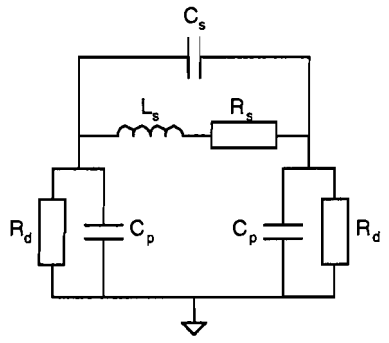


Figure 3.12: Inductor model representation.

The values of the components in the model schematic are described in the following equations:

$$L_s = \beta \cdot {D_{out}}^{\alpha 1} \cdot w^{\alpha 2} \cdot {D_{avg}}^{\alpha 3} \cdot n^{\alpha 4} \cdot s^{\alpha 5} \tag{3.20}$$

$$R_s = \frac{l}{\sigma \cdot w \cdot \delta \cdot (1 - e^{-\frac{t}{\delta}})} \tag{3.21}$$

$$C_s = \frac{\epsilon_{ox} \cdot n \cdot w^2}{t_{oxM1-M2}} \tag{3.22}$$

$$R_p = \frac{1 + [\omega \cdot R_{si} \cdot (C_{si} + C_{ox})]^2}{\omega^2 \cdot R_{si} \cdot {C_{ox}}^2} \tag{3.23}$$

$$C_p = \frac{C_{ox} + \omega^2 \cdot R_{si} \cdot (C_{si} + C_{ox}) \cdot C_{si} \cdot C_{ox}}{1 + [\omega \cdot R_{si} \cdot (C_{si} + C_{ox})]^2} \tag{3.24}$$

In this model, the layout parameters from Table 3.1 are used. Furthermore, the values R_{si}, C_{si}, and C_{ox} can be obtained by the following formulas:

$$R_{si} = \frac{2}{G_{sub} \cdot l \cdot w} \tag{3.25}$$

$$C_{si} = \frac{C_{sub} \cdot l \cdot w}{2} \tag{3.26}$$

Table 3.1: Layout parameters of the octagonal inductor model

Parameter	Description
β	$1.62 \cdot 10^{-3}$
$\alpha 1$	-1.21
$\alpha 2$	-0.163
$\alpha 3$	2.43
$\alpha 4$	1.75
$\alpha 5$	-0.049
D_{out}	Outer diameter
D_{in}	Inner diameter
D_{avg}	Average of outer and inner diameter
w	Spiral track width
n	Number of turns
s	Spacing between adjacent tracks
σ	Conductivity of the metal (typical $3.33 \cdot 10^7$ S)
δ	$\sqrt{2/(\omega \cdot \mu_0 \cdot \sigma)}$ where ω is the frequency
μ_0	$4\pi \cdot 10^{-7}$ H/m (Magnetic permeability of free space)
t	Turn thickness (typical $1.52 \cdot 10^{-6}$ m)
l	$4 \cdot n \cdot D_{avg}$
$t_{oxM1-M2}$	Oxide thickness between spiral and under-pass

$$C_{ox} = \frac{\epsilon_{ox} \cdot l \cdot w}{2 \cdot t_{ox}} \tag{3.27}$$

With the model introduced in this section, the following formula for the quality factor of the inductor can be derived:

$$Q = \frac{\omega L_s}{R_s} \cdot \frac{R_p}{R_p + R_s[(\omega L_s/R_s)^2 + 1]} \cdot \left[1 - (C_s + C_p)\frac{{R_s}^2 + (\omega L_s)^2}{L_s}\right] \tag{3.28}$$

This means the quality factor of the source inductor will be about 5 at 1.9 GHz. To illustrate the consequences of a lower quality of the inductor on NF, gain and S11, new simulations are carried out (see Figures 3.13, 3.14, and 3.15). In these simulations, the quality factor of a bondwire is assumed to be 10.

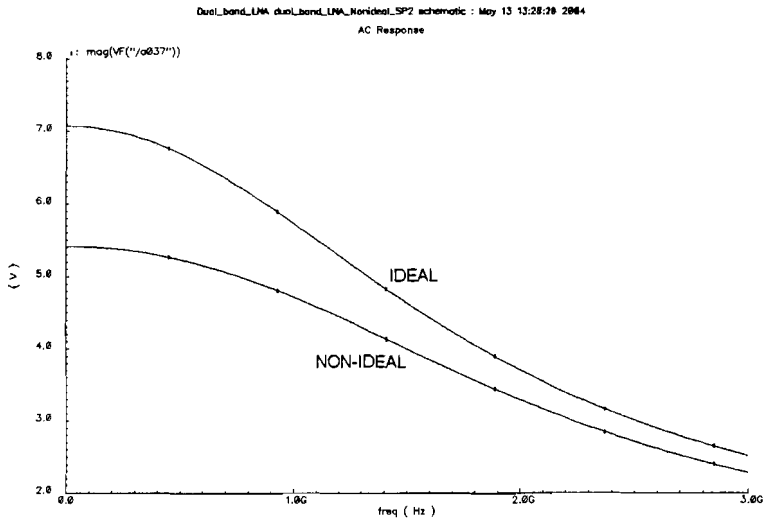


Figure 3.13: "**IDEAL**": Gain for infinite quality factors. "**NON-IDEAL**": Gain for $Q_{L_g} = 10$ and $Q_{L_s} = 5$.

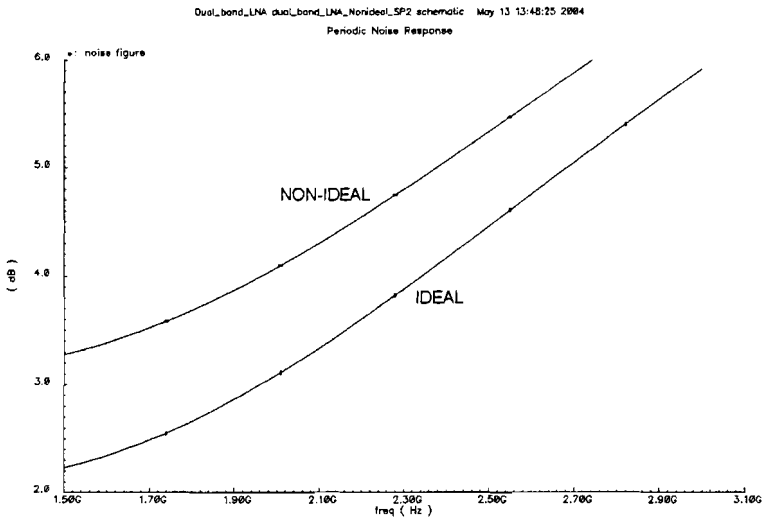


Figure 3.14: "**IDEAL**": Noise Figure for infinite quality factors. "**NON-IDEAL**": Noise Figure for $Q_{L_g} = 10$ and $Q_{L_s} = 5$.

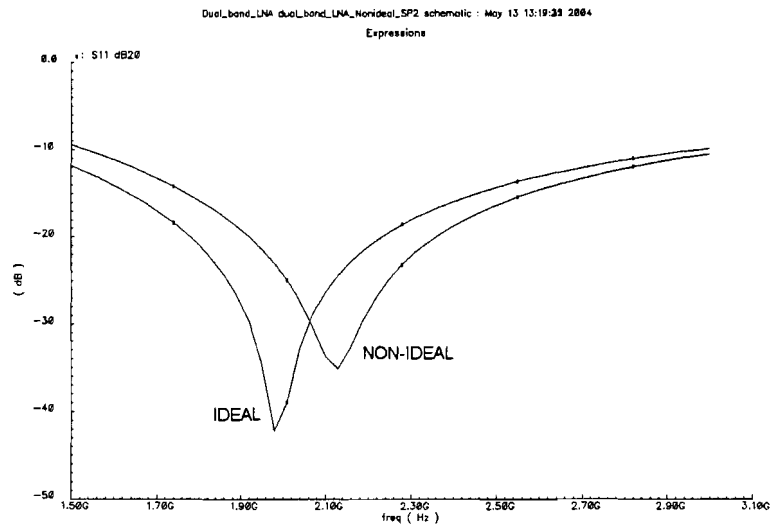


Figure 3.15: "**IDEAL**": S11 for infinite quality factors. "**NON-IDEAL**": S11 for $Q_{L_g} = 10$ and $Q_{L_s} = 5$.

3.6.3 Influence of package, bondpads and ESD diodes

For practical use, the LNA is placed in a package and an electrostatic discharge (ESD) protection ring is added. This has an influence on the input impedance. In this section, these consequences are explained. Figure 3.16 provides an insight in the physical position of the different peripherals.

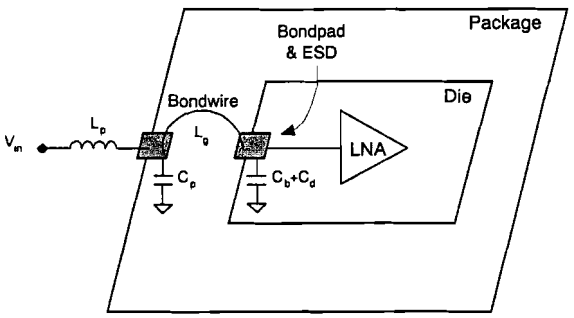


Figure 3.16: Modeled LNA package, bondwire, bondpad and ESD Diodes.

Package model

In the package, the bondwire is connected to the input- and output pins. As this is also the case for the RF input pin of the LNA package, the input impedance of the LNA is affected. From simulations, it turned out that the package can be modeled by a simple LC network (L_p and C_p in Figure 3.16). The experimentally retrieved values for L_p and C_p are 0.692 nH and 140.6 fF, respectively, for a National LLP44 package model.

Bondpad model

The bondpad is part of the chip die and enables connection of the bondwire. Because of its size it behaves as a capacitance and therefore influences the input impedance of the LNA. The capacitance naturally depends on the technology and physical size. It is very common to implement a bondpad in 2 layers simultaneously (e.g., Metal layer 5 and 6), interconnected by many vias. This gives the bondpad some physical strength which is needed during the process of wiring them to the package.

Dedicated bondpad modelers are available (e.g., Affirma), which can calculate the value of a simple capacitor model. For the design and technology under investigation, the bondpad can be modeled by a capacitor. From simulations using the bondpad model of National, a capacitance of 32.9 fF is obtained.

ESD Diodes model

To avoid damage from electrostatic discharge from outside sources, a so-called ESD ring is implemented in this layout. This ESD protection consists of 2 diodes connected to the bondpad. One of these diodes is connected to V_{dd} and the other one to ground. This enables large positive charges to be discharged via the positive supply voltage ring and negative charges via the ground ring.

In general, these diodes behave like capacitors. Simulations are carried out on the ESD model of National, which result in a total capacitance of 17.7 fF.

Influence on input impedance

The total influence yields the following new equation for the input impedance.

$$
\begin{aligned}
Z_{in,total} &= sL_p + \frac{sL_g + (Z_b \parallel Z_d \parallel Z_{in,LNA})}{1 + sC_p \cdot (sL_g + (Z_b \parallel Z_d \parallel Z_{in,LNA}))} \\
&= sL_p \\
&+ \frac{sL_g + \left(\frac{1+s^2C_{gs}(L_g+L_s)+g_m \cdot sL_s}{sC_{gs}+s(C_b+C_d)(1+sC_{gs}(L_g+L_s)+g_m \cdot sL_s)}\right)}{1 + s^2C_pL_g + sC_p\left(\frac{1+s^2C_{gs}(L_g+L_s)+g_m \cdot sL_s}{sC_{gs}+s(C_b+C_d)(1+sC_{gs}(L_g+L_s)+g_m \cdot sL_s)}\right)}
\end{aligned}
\tag{3.29}
$$

3.6.4 Layout considerations

The previous sections describe the implications of implementing this LNA. They also provide some measures to decrease its negative consequences. Despite this, the on-chip inductors still occupy very much chip area. Figure 3.17 shows the layout of the LNA when it is implemented differentially.

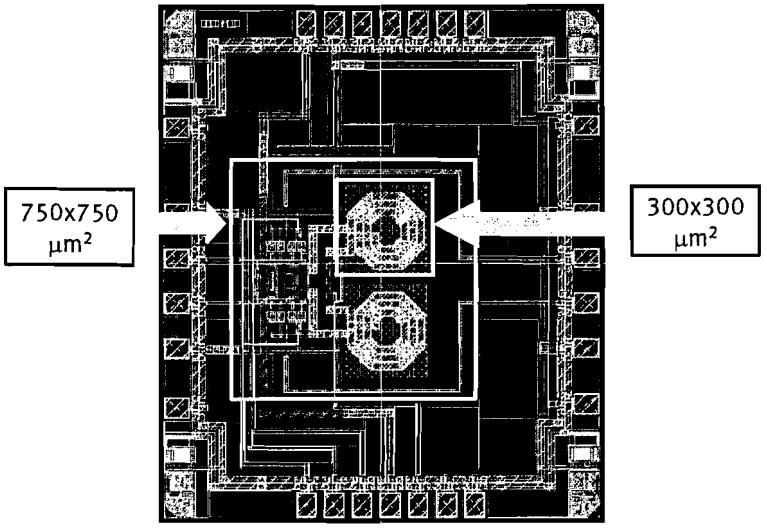


Figure 3.17: LNA layout with an indication of the inductor sizes.

3.7 Design flow

A clear and successful design procedure for this LNA topology is described in [7]. This design approach will be discussed briefly.

First, a starting value for the overdrive voltage ($V_{gs}-V_t$) should be chosen. For linearity purposes, this should be more than 150 mV. Then, select the width and transconductance of the input transistor on the basis of the power budget. The optimal ratio between L_g and L_s that yields the minimum Noise Figure, can be calculated with the following equation:

$$n_{opt} = (4Q_{L_g}^2 \gamma^2 g_m R_s)^{\frac{1}{3}} \tag{3.30}$$

Then, L_s (and therefore L_g) can be calculated using equation (3.18). From equation (3.19), the total gate-source capacity C_{gs} can be obtained. By simulations, the intrinsic gate-source capacitance of the input transistor can be determined. If this is less than the total needed capacitance, $C_{gs,ext}$ will be added to compensate this.

The load resistance R_d can now be chosen to achieve the desired voltage gain while keeping the cascode transistor in its saturation region. The input transistor can then be kept in saturation by tuning the cascode transistor width.

The next step in this process is checking if the performance (noise, gain, linearity) is sufficient with acceptable DC operating points for both transistors. If this is not satisfactory, some design steps could be repeated for better performance. After these performance requirements are met, the maximum size of the bondwire at the gate of the input transistor should be known. This determines the ratio between L_g and L_s that is no longer optimal, which means that the Noise Figure deteriorates for the sake of chip area.

3.8 Final simulation results

In this section, the final design of the inductively degenerated, cascoded LNA is illustrated and simulation results are presented. The simulations are performed in Cadence 4.4.6. The transistors are modeled by the BSIM3 models that are provided by National Semiconductors for the CMOS9T process. Figure 3.18 shows the schematic of the design inclusive the modeled package, bondpads, ESD diodes and a 3 nH bondwire. Table 3.2 shows the simulation results for this schematic.

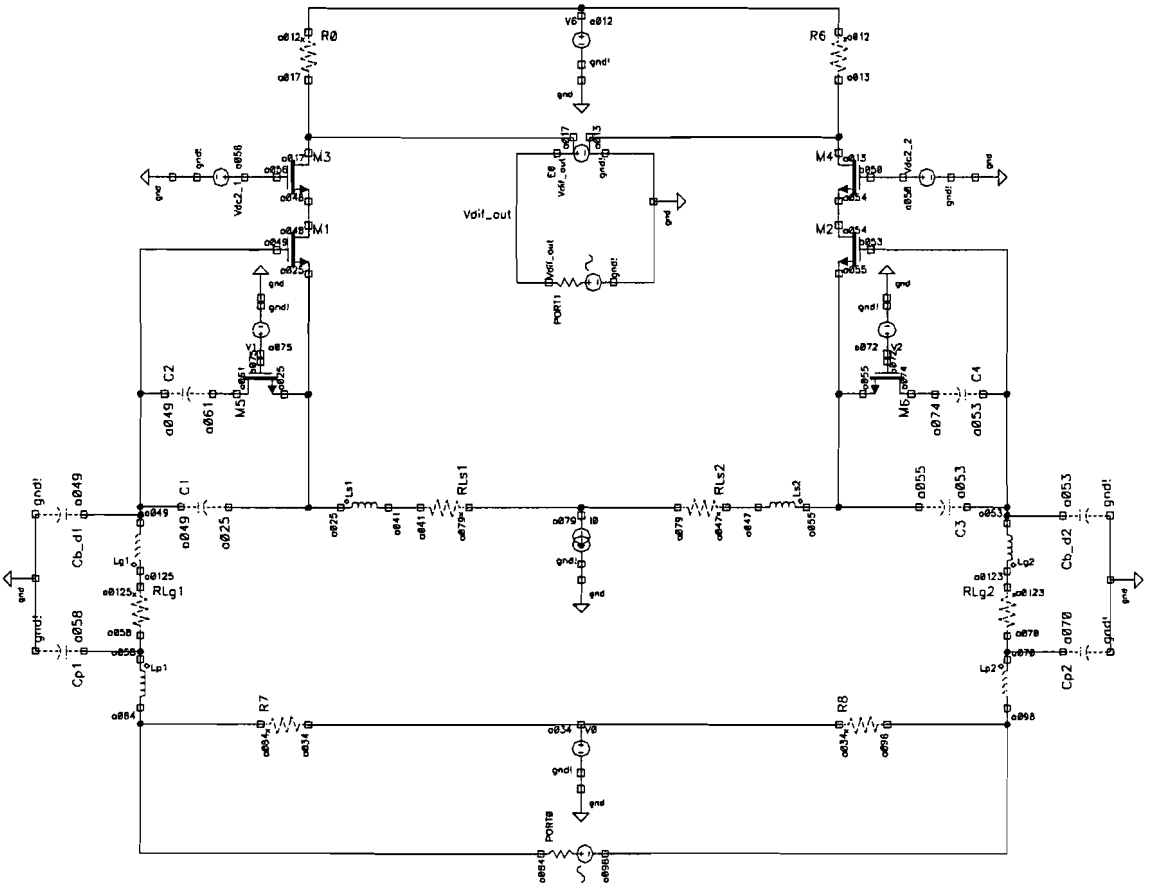


Figure 3.18: Schematic of the dual-band LNA.

Table 3.2: Simulation results of the differential dual-band LNA.

Band	NF(dB)	G(dB)	IIP3(dBm)	S11(dB)	I(mA)
DECT (1.9 GHz)	2.5	17	0.5	-16	16
BT (2.4 GHz)	2.3	15	3	-14	8

3.9 Summary

From the final simulation results, it can be concluded that the performance of this topologies is satisfactory. Noise, gain and linearity are good for the given power budget. A big advantage of the on-chip matching topology, is the fact that it is fully integrated and a simple and clear design procedure is available. Therefore almost no effort is needed to implement the chip in a system.

Mainly due to the size of on-chip inductors, this chip is relatively cost ineffective because of the total chip area it occupies. In an overall view at system level this size is unacceptable, which justifies the need for an alternative LNA topology. One specific alternative LNA topology will be discussed in the following chapter.

Chapter 4

Cascoded LNA with off-chip matching

4.1 Introduction

As proposed in the previous section, a lot of chip area can be saved when no on-chip impedance matching circuitry is needed. However, the LNA input impedance should still be matched to the source impedance. It is possible to do this using off-chip matching circuitry. A suitable way to achieve off-chip matching is by using transmission lines. In this chapter, the LNA again will consist of a cascoded common-source amplifier.

Microstrip lines on PCB will be used for the off-chip matching. A Microstrip line is, by definition, a transmission line consisting of a strip conductor and a ground plane separated by a dielectric medium [2]. The choice for this kind of transmission lines is based on technology availability and it is beyond the scope of this document.

In this chapter, a design procedure for Microstrip matching circuits is presented. Impedance matching is the first priority, as it was in the previous chapter when on-chip matching is applied. The matching circuit then will be optimized in order to reduce the total NF and the physical size of the matching network.

4.2 Impedance matching

When designing a suitable matching circuit, it is important to determine the load impedance. This load impedance (Z_L) is the input impedance of the LNA, which mainly depends on its input transistor (i.e. M1 in Figure 3.1).

There are numerous ways to match the load impedance to the source impedance using transmission lines. These options are limited by the technology and production process of the PCB, because not all physical structures might be possible. In this stage, also some effort will be put into optimizing the physical size.

Every load can be matched to a desired source resistance by a very simple transmission line network [2]. It consists of a series Microstrip line and a shunt stub (see Figure 4.1). The way this matching network transforms the load impedance, can be seen in Smith charts, e.g. Figure 4.2 (which will be discussed later).

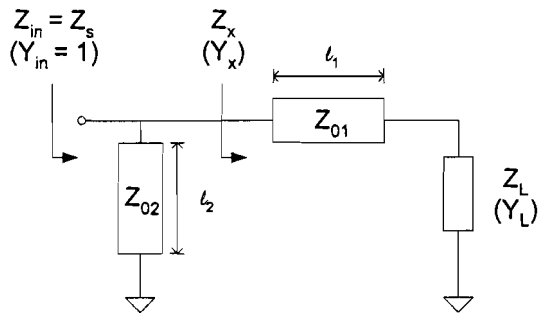
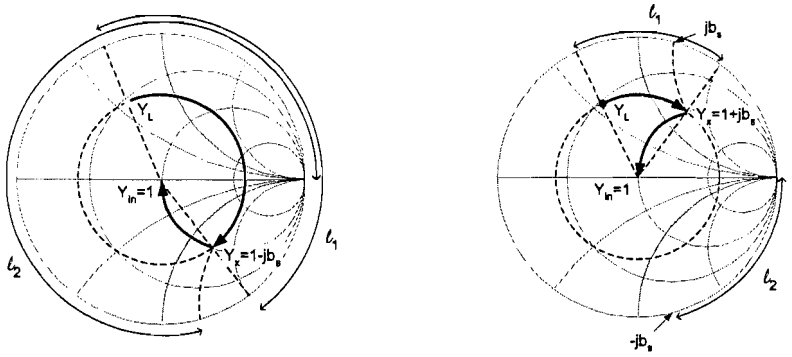


Figure 4.1: A simple Microstrip line matching network with a serial stub (Z_{01}) and a short-circuited shunt stub (Z_{02}).

In this example the load impedance is matched to a 50 Ω source, by using transmission lines with a characteristic impedance of 50 Ω. This enables quite easy matching with Smith charts that also use a 50 Ω reference. In this section Y Smith charts will be used (Figure 4.2), but Z Smith charts are suitable as well.



(a) Matching via $Y_x = 1 - jb_s$. (b) Matching via $Y_x = 1 + jb_s$.

Figure 4.2: Y Smith charts for the simple matching network.

4.2.1 Matching using Smith charts

The serial stub shifts the input impedance along the constant $|\Gamma|$ circle over a distance l_1, which yields the new input admittance Y_x. The shunt stub only influences the imaginary admittance component and can therefore shift the input admittance to the desired value of Y_{in}.

In this case, this means that the real part of Y_x should equal Y_{in}. Therefore, there are two possible values for Y_x. They are $Y_x = 1 + jb_s$ and $Y_x = 1 - jb_s$. Choosing between these values can be based on the size of the serial stub, except when DC limitations occur (which will be discussed later in this section).

The imaginary part is compensated by the shunt stub. Generally, this shunt stub can either be short-circuited (SC) or open-circuited (OC). A short-circuited shunt stub of size l_2 has the same effect as an open-circuited shunt stub of size $\lambda/4 + l_2$. Depending on whether the imaginary part of Y_x is positive or negative, the short-circuit may be shorter than the open-circuit or vice versa. Figure 4.2 shows the difference between using a short-circuited shunt stub when Y_x has a negative or a positive imaginary part, respectively.

In Figure 4.2(a), the shunt stub length (l_2) corresponds to $\lambda/4$ plus the distance between jb_s (the imaginary part of Y_x) and $\Gamma = 0$. In Figure 4.2(b), l_2 corresponds to the distance between $-jb_s$ and $\Gamma = \infty$.

When choosing between a short-circuited or an open-circuited shunt stub, also the DC behavior should be taken into account. A short-circuit cannot be applied at the input of a common-source amplifier, because this disables DC biasing of the input transistor.

When using lumped components, the short-circuit can be avoided by adding a large series capacitance. This capacitor would then behave as an open circuit for DC settings and as a short for higher frequencies. A capacitor of 1 nF has almost no effect on the impedance matching and increases the Noise Figure only about 0.2 dB.

If lumped components are not an option, the length of the shunt stub might increase dramatically. Then, choosing the shortest one of the short-circuit or the open-circuit is not possible, so the shunt stub is not necessarily the shortest possible. Therefore, this limitation also requires reconsidering the choice between either a positive or a negative imaginary part of Y_x. This choice is now a matter of the total length of both stubs, instead of just the serial stub length itself.

4.2.2 Size minimization

For the operation frequency and the transistor size and technology under investigation, a Microstrip matching network would be a few centimeters in size. Therefore some effort will be put in minimizing the size of the matching circuit.

First of all, the bondwire of the LNA chip can be used to reduce the total size of the transmission lines. As described in section 3.6.3, this influences the input impedance for the LNA. From simulations it appeared that the new impedance (incl. package, bondwire, bondpad and ESD ring) is easier to match to. This will be explained in section 4.4.

Secondly, adding an external capacitor between gate and source of the LNA's input transistor can decrease the size. Because of losses (see section 4.4.2) in the Microstrips, the matching circuit size also influences the noise performance. Therefore adding this external capacitor in parallel with the LNA also improves the overall Noise Figure.

A third way to decrease the size of the Microstrip lines is by applying discontinuities. Namely, transmission line discontinuities have an impact on the impedance. The discontinuities that will be used are bends. Apply-

ing several bends results in a meandering Microstrip. Of course there are other discontinuities possible, but these are less practical in terms of layout, production and complexity of the design process of the matching.

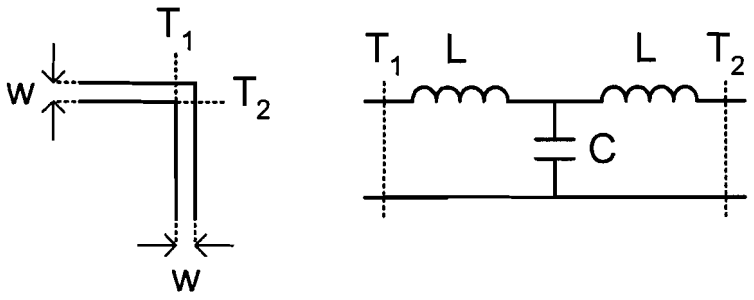


Figure 4.3: Microstrip line abrupt bend and the equivalent model (right).

The impact of the discontinuities is modeled extensively and described in [8]. The model of an abrupt bend in a Microstrip line is depicted in Figure 4.3. In this figure,

$$L = 100 \cdot h \cdot (4\sqrt{W/h} - 4.21) \quad [\text{nH/m}] \tag{4.1}$$

and for $W/h < 1$:

$$C = w \cdot \left(\frac{(14\epsilon_r + 12.5)(W/h) - (1.83\epsilon_r - 2.25)}{\sqrt{W/h}} + \frac{0.02\epsilon_r}{W/h} \right) \quad [\text{pF/m}] \tag{4.2}$$

or for $W/h \geq 1$:

$$C = w \cdot ((9.3\epsilon_r + 1.25)(W/h) + 5.2\epsilon_r + 7)) \quad [\text{pF/m}] \tag{4.3}$$

There also are techniques to compensate the discontinuity, which makes it equivalent to a straight transmission line. This is depicted in Figure 4.4, where the following values apply.

$$L = W \cdot \left(\sqrt{2} \cdot [1.04 + 1.3e^{-1.35W/h}] \right) \tag{4.4}$$

$$d - x = \sqrt{2} \cdot W - \frac{L}{2} \tag{4.5}$$

This approach does not effectively decrease the size of the total transmission line network. However, it does provide the opportunity to fit the network into a physical shape that might be more suitable than long straight lines.

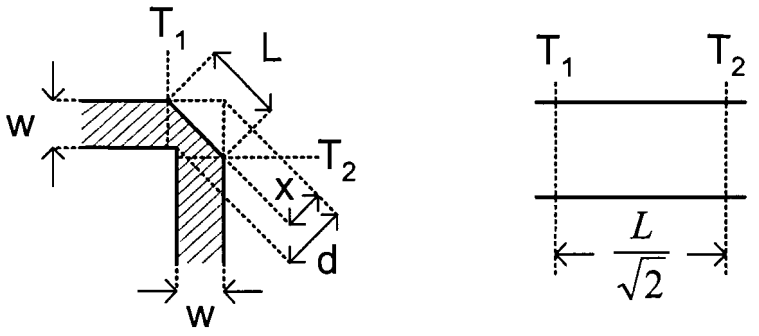


Figure 4.4: Optimal Microstrip line mitered bend and the equivalent model (right).

4.2.3 Dual-band impedance matching

Naturally, this LNA topology should be able to be dual-band. As was the case in the previous chapter, it would be very convenient if this could be possible without adding another matching circuit with the same size.

To investigate this possibility, the output impedance of the matching network is determined for other frequencies. Of course, this output impedance changes drastically.

Also, the input impedance of the common-source amplifier is simulated for different frequencies. As this input impedance is mainly capacitive, the real part remains virtually the same. By adding a capacitor or an inductor parallel to the input transistor, the input impedance could be shifted to a more suitable value.

The imaginary part of the LNA input impedance (Z_{LNA}) will now be shifted to a value that is the conjugate of the imaginary part of the matching circuit's output impedance (see Figure 4.5). This achieves a conjugate match of the imaginary parts, allowing the mismatch of the real parts. This mismatch of the real impedance parts turns out to be acceptable.

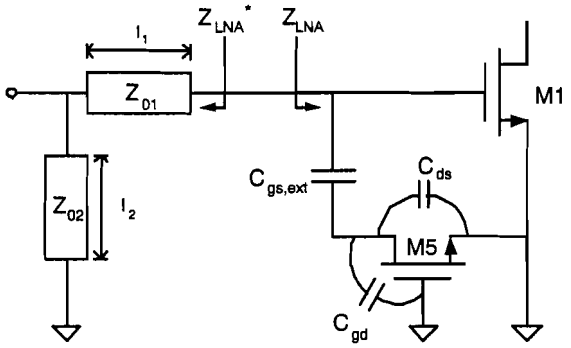


Figure 4.5: External Matching.

A capacitor is more suitable for integration than an inductor, so it is convenient to be able to place a capacitor parallel to the input transistor. A matching circuit that is designed for 1.9 GHz needs an inductor parallel to the input transistor in order to achieve conjugate match at 2.4 GHz. However, a matching circuit for 2.4 GHz can achieve a conjugate match at 1.9 GHz by using a capacitor in parallel ($C_{gs,ext}$, see Figure 4.5). The value for this capacitor can be calculated fairly easily (see Appendix A).

By enabling and disabling this capacitor with a transistor switch, a 2.4 GHz matching circuit can be used for 1.9 GHz matching as well.

4.3 Noise matching

Noise performance strongly depends on the impedance (R_m) that is seen by the LNA at its input. In this case, the output impedance of the matching network is very important for the LNA Noise Figure. To illustrate this, first the input referred noise of the LNA is described as follows (based upon [6], p. 39 etc.).

$$\overline{V_n^2} = \frac{8kT}{3g_m} \tag{4.6}$$

$$\overline{I_n^2} = \frac{8kT}{3g_m|Z_{in}|^2} \tag{4.7}$$

With this, the following description for the Noise Figure is constructed.

$$NF = 10\log\left(\frac{4kTR_m + \overline{(V_n + I_n R_m)^2}}{4kTR_m}\right) \tag{4.8}$$

This equation shows that there is a value for R_m for which the Noise Figure is minimal. This situation is called noise match. The noise matching impedance can be determined by simulations on the common-source amplifier that is introduced in chapter 2. In this particular case, the optimal source impedance (R_{opt}) for this LNA is measured to be 233 Ω.

As can be seen from (4.8), the Noise Figure can be tuned by changing the amplifier's transconductance. It would be convenient to choose the value for R_m close to the optimal source impedance of the LNA. However, the output impedance ($Z_m = R_m + jX_m$) of an ideal matching network is the complex conjugate of the LNA's input impedance. In practice, the values for R_{opt} and R_m are not the same.

Also, the available power gain P_a of the matching network influences the overall Noise Figure, which is illustrated by the following equation:

$$NF_{\text{tot}} = -10\log(P_a) + NF_{\text{LNA}} \tag{4.9}$$

In the practical case of this LNA, the noise matching can only be improved by applying less strict constraints concerning the impedance matching. Unfortunately, in the practical implementation of this LNA there is no room left for this tradeoff. This means, the impedance matching can not be decreased within the requirements. Because these input reflection requirements have to be met, no noise matching tradeoff can be made.

4.4 Implementation considerations

This section describes the influence of several implementation issues for the LNA with its Microstrip matching network. First, the difference between ideal transmission lines and Microstrip transmission lines, will be discussed. Also, losses in Microstrip lines, the chip package and the physical placement of the Microstrips have an effect and will be discussed in this section.

4.4.1 Microstrip implementation

In previous sections, the matching network is assumed to consist of ideal transmission lines. When using Microstrip transmission lines, characteristic impedance, the wavelength in the Microstrip and loss effects should be determined. These depend on the physical properties of the PCB, which are depicted in Figure 4.6.

t and W are the Microstrip thickness and width, respectively. Between the Microstrip (signal conductor) and the ground plane (ground conductor), there is a dielectric with height h and relative dielectric constant ϵ_r.

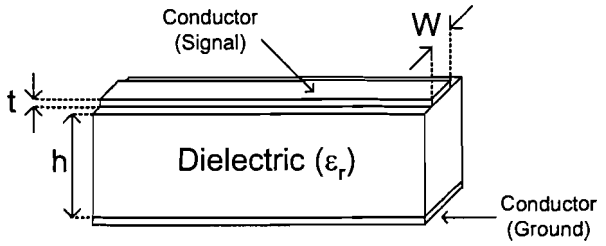


Figure 4.6: Physical properties of the Microstrip transmission lines and the PCB.

Both characteristic impedance and wavelength can be determined using the practical results presented in [2] en [8]. They provide fairly accurate analytical calculations for wavelengths in Microstrips and the Microstrip width for achieving some characteristic impedance.

For $W/h \leq 1$:

$$Z_0 = \frac{60}{\sqrt{\epsilon_{ff}}} \cdot \ln\left(8\frac{h}{W} + 0.25\frac{W}{h}\right) \tag{4.10}$$

where

$$\epsilon_{ff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}\left[\left(1 + 12\frac{h}{W}\right)^{-1/2} + 0.04\left(1 - \frac{W}{h}\right)^2\right] \tag{4.11}$$

For $W/h \geq 1$:

$$Z_0 = \frac{120\pi/\sqrt{\epsilon_{ff}}}{W/h + 1.393 + 0.667 \cdot \ln(W/h + 1.444)} \tag{4.12}$$

where

$$\epsilon_{ff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}\left(1 + 12\frac{h}{W}\right)^{-1/2} \tag{4.13}$$

The wavelength inside the Microstrip transmission lines is given by the next equations, where λ_0 is the wavelength in vacuum.

For $W/h \geq 0.6$**:**

$$\lambda = \frac{\lambda_0}{\sqrt{\epsilon_r}}\sqrt{\frac{\epsilon_r}{1 + 0.63(\epsilon_r - 1)(W/h)^{0.1255}}} \tag{4.14}$$

For $W/h \leq 0.6$**:**

$$\lambda = \frac{\lambda_0}{\sqrt{\epsilon_r}}\sqrt{\frac{\epsilon_r}{1 + 0.6(\epsilon_r - 1)(W/h)^{0.0297}}} \tag{4.15}$$

These equations are valid for a zero or negligible Microstrip thickness. If the thickness is not negligible ($t/h > 0.005$), then W in the previous equations should be replaced by the effective width:

For $W/h \geq 1/2\pi$**:**

$$W_{eff} = W + \frac{t}{\pi}\left(1 + \ln\frac{2h}{t}\right) \tag{4.16}$$

For $W/h \leq 1/2\pi$**:**

$$W_{eff} = W + \frac{t}{\pi}\left(1 + \ln\frac{4\pi W}{t}\right) \tag{4.17}$$

When the right characteristic impedance and wavelength are obtained from these calculations, the normal matching procedure can be executed using Smith charts.

4.4.2 Lossy Microstrips

The Microstrip matching network also is assumed to be lossless. Unfortunately, practical Microstrip transmission lines are lossy. The losses are expressed in a loss in the dielectric and a finite conductance of the Microstrip and the ground plane.

The losses cause a dispersion in the effective width and the characteristic impedance of the transmission lines and in the ϵ_{ff} of the dielectric. In the example, this mainly means that the real part of the input impedance is not as predicted, which results in less satisfying reflection performance.

Because of these losses, long Microstrip transmission lines have a dramatic effect on the noise performance. It appears from simulations that the size of the shunt stub is only acceptable when it is a short-circuited stub. As discussed before, this is impossible due to DC setting requirements. Therefore, the solution of adding a series capacitor is needed in this context.

In the current application, the size of the series transmission line is also very large. This again deteriorates the overall noise performance. Especially the series stub size can be reduced significantly, as is discussed in section 4.2.2.

4.4.3 Influence of package, bondpads and ESD diodes

As stated before, the package of the LNA chip also influences the performance of the total matched system. Simulations are carried out with influence of the package, the bondwire, the bondpads and the ESD ring. As the bondwire size can be chosen between 1 nH and 3 nH, the simulations are repeated for different bondwire sizes. Table 4.1 shows these simulation results.

Table 4.1: Microstrip sizes for LNA with package and different values of bondwire inductance

Microstrips	Serial stub	Shunt stub	Total size
Without bondwire	13.8849 mm	3.5912 mm	17.4761 mm
Package with 1 nH bondwire	11.4764 mm	3.9083 mm	15.3848 mm
Package with 2 nH bondwire	10.6707 mm	4.4140 mm	15.0848 mm
Package with 3 nH bondwire	9.7108 mm	4.8597 mm	14.5705 mm

4.4.4 Physical Microstrip placement

To limit the PCB area consequences, it may be beneficial to place the matching network under the footprint of the chip. It is possible to bend the Microstrip transmission lines in such a way that it fits best under the chip footprint. Of course, this has to be practically possible under the PCB constraints.

If two bends with the same orientation are applied close to each other, parts of the lines could behave as coupled lines. To limit the complexity of the Microstrip structure, effort will be put in avoiding significant coupling. From [4], it appears that coupling is limited when the straight line between two bends is at least 5 times the line width. This is illustrated in Figure 4.7.

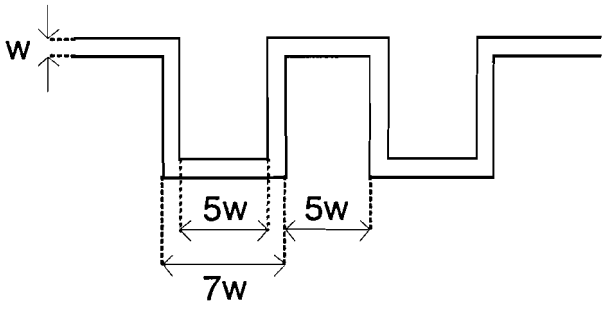


Figure 4.7: Meander line with less coupling.

4.5 Design flow

The design flow of this amplifier topology starts with the design of the common-source amplifier that is discussed in section 2.5. After that, the input impedance of the common-source amplifier should be determined by simulations.

Then, a matching circuit can be designed for 2.4 GHz by using the presented formulas for Microstrip transmission lines. This design process is fairly easy using Smith charts and even easier using its analytical equivalent (see Appendix B). The output impedance of this matching network at 1.9 GHz can then be determined directly. Appendix A yields the value of the capaci-

tor $C_{gs,ext}$ (see Figure 4.5) for switching between bands.

A suitable switching transistor has very little influence on the impedance matching when it is on. When it is off however, the switch itself influences the input impedance of the common source-amplifier. The combination of the drain-source and drain-gate parasitic capacitors of the switching transistor is then positioned in series with $C_{gs,ext}$. This was not anticipated upon when designing the matching network, so this design flow should be repeated with the new input impedance.

The new value for $C_{gs,ext}$ already yields acceptable results. While this process could be repeated several times, improvement is less because the new value of $C_{gs,ext}$ differs less from the anticipated value in each iteration.

4.6 Final simulation results

The most suitable simulator for Microstrip transmission line circuits is ADS. Unfortunately, the transistor models are not available for this simulator. Therefore, part of the simulations is done in ADS and the other part in Cadence.

This makes it harder to obtain NF, gain, S11 and linearity from the simulations. The common-source amplifier is simulated in Cadence to obtain the input impedance. This input impedance is used to design and simulate the matching network in ADS. The parameters for the Microstrip transmission lines are depicted in Figure 4.8. These simulations yield the S11 parameter and the gain (V_T/V_{in}) and output impedance (Z_T) of the matching network.

Then the common-source simulations can be resumed with a Thévenin equivalent of the matching network (see Figure 4.9). The impedance of the Thévenin source is the output impedance of the matching network. With this, the total gain and the output noise can be simulated.

Now, the total NF can be calculated using the following equation:

$$NF = 10\log\left(\frac{\overline{V_{n,out}^2}}{4kTR_s \cdot |G|^2}\right) \tag{4.18}$$

In this equation, G is the total gain, which is the product of the gain of the matching network and the gain of the LNA.

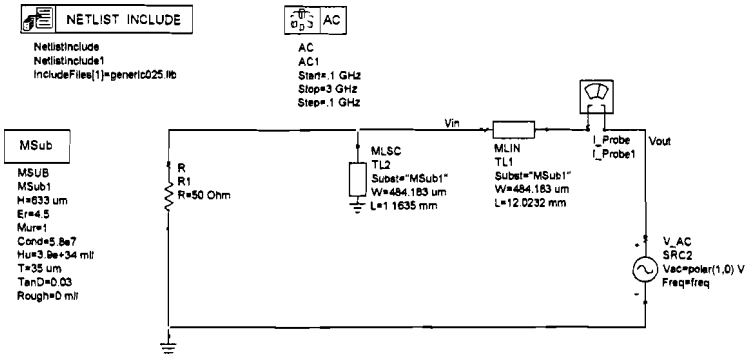


Figure 4.8: Microstrip parameters in ADS.

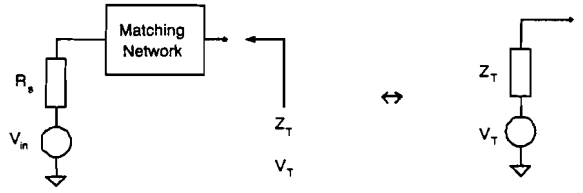


Figure 4.9: The matching circuit and its Thévenin equivalent.

The overall results of these simulations and the calculations are shown in Table 4.2.

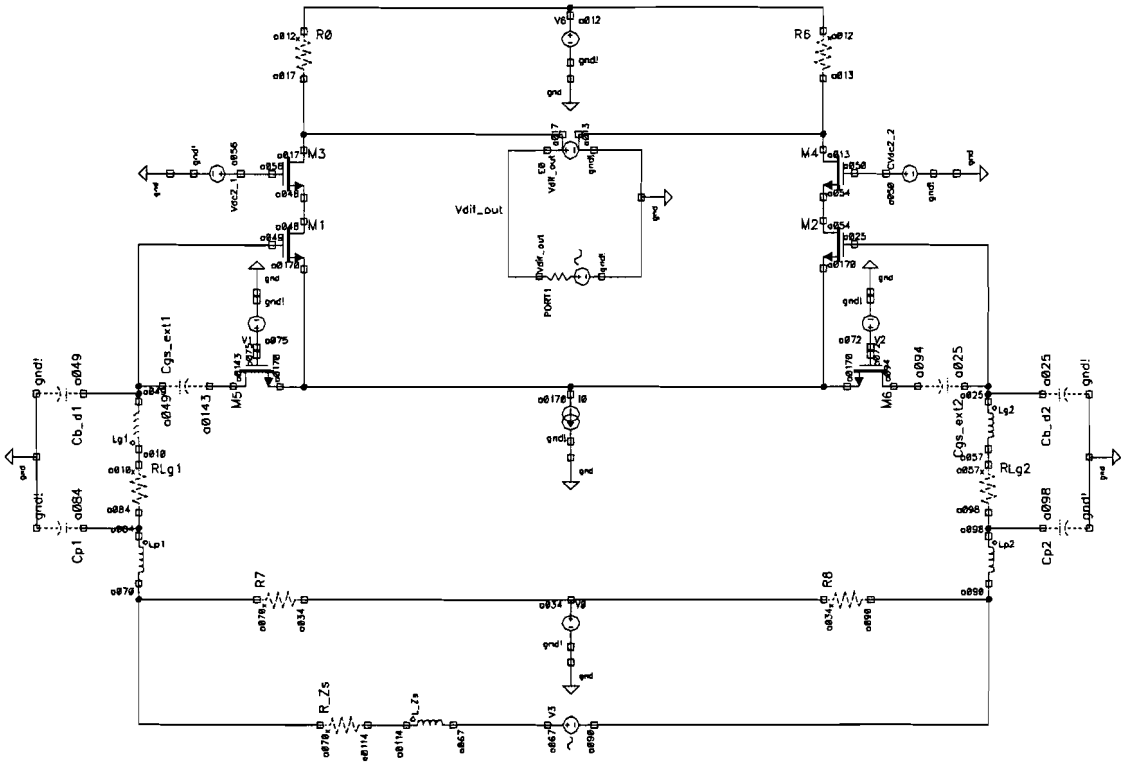


Figure 4.10: Cadence schematic of the common-source LNA.

Table 4.2: Simulation results of the differential dual-band LNA.

Band	NF(dB)	G(dB)	IIP3(dBm)	S11(dB)	I(mA)
DECT (1.9 GHz)	3.2	16	5	-11	16
BT (2.4 GHz)	2.0	19	5	-12	8

4.7 Summary

This LNA design achieves good results for dual-band operation. Its main advantage is the small area that it occupies on a chip. This has positive consequences for the cost effectiveness. The design procedure that is developed, is suitable for fast and clear designing of this LNA.

However, the small chip size is at the cost of a large transmission line

matching network on the PCB. Furthermore, the actual implementation of this matching network can not done by the LNA chip designer, which decreases the cost effectiveness in that stage.

Chapter 5

Conclusions and recommendations

5.1 On- and off-chip matching comparison and conclusions

There are two ways to compare the LNA topologies that are described in this document. Naturally, a performance comparison is very useful. However, it is also important to compare the design procedures. In the case of external matching, part of the design process will have to be carried out by the RF engineer that assembles the LNA chip in a system on a PCB. Therefore, it is of high importance to have a straightforward and unambiguous design process.

From the final simulation results, it can be concluded that the performance of both topologies is satisfactory. However, NF, gain and linearity are worse for the off-chip matched LNA, when using the same power budget. A big advantage of the on-chip matching topology, is the fact that it is fully integrated and therefore almost no effort is needed to assemble the chip on a PCB. Mainly due to the size of on-chip inductors, this chip is relatively cost ineffective because of the total chip area that is occupied. At a frequency of 1.9 GHz, this LNA design achieves a Noise Figure (NF) of 2.5 dB, an IIP3 of 0.5 dBm, an S11 of -16 dB and a gain of 17 dB, using a current of 16 mA. At a frequency of 2.4 GHz, it achieves a NF of 2.3 dB, an IIP3 of 3 dBm, a gain of 15 dB and an S11 of -14 dB for a current of only 8 mA.

In the LNA topology with the external matching circuit, the chip itself

is more cost effective. Unfortunately, the effort and experience needed to use this LNA in a system and designing the PCB is cost consuming as well. Furthermore, the matching network uses a large PCB area, which also decreases cost effectiveness and practical applicability. For this LNA design, the following overall performance is achieved at 1.9 GHz: NF is 3.2 dB, IIP3 is 5 dBm, S11 is -11 dB and the gain is 16 dB for a current of 16 mA. At a frequency of 2.4 GHz, it achieves a NF of 2.0 dB, an IIP3 of 5 dBm, a gain of 19 dB and an S11 of -12 dB, but this is achieved with a current of only 8 mA.

When comparing the design procedures, also some important differences arise. The design process for the LNA with on-chip matching is straightforward and simulations can be done in one CAD tool. For example, in this case Cadence/spectreRF is used. In the case of the externally matched LNA, not all simulations can be done in the same simulator. Cadence/spectreRF does not have advanced tools for working with transmission lines, so the matching network is designed in ADS. The transistor models are available in Cadence/spectreRF, so this tool is used for design of the active part of the LNA. The interfacing issues between these simulators complicate the way to determine the overall LNA performance.

5.2 Original contributions

Part of this document is comparable to or based on previous research that is carried out by others. Therefore, the main original contributions from this Master Thesis project are pointed out here.

The design equations of the on-chip matched LNA are extended by using an extended transistor model. This model also includes the body-effect that is significant in this application. Therefore improvement in the matching is achieved. The design procedure of the Microstrip matching circuit is investigated and described thoroughly. Also, techniques for performance improvement and a dual-band matching are introduced.

Furthermore, these two LNA designs are compared considering cost effectiveness, design process and performance.

5.3 Recommendations

In [8], a lot of different techniques are modeled to physically implement transmission lines with or without coupling and discontinuities. These techniques are less straightforward and not all of them are applicable on the PCB that is available. However, the implementation techniques could improve the performance of the matching network because of size and loss improvements.

It might also be interesting to investigate whether the second LNA design would be suitable for other frequencies as well. The trend of the performance versus the frequency would be very useful information about this design.

Appendix A

Matlab script: External capacitor for band switching

```
f = 1.9e9;
Zl = 21.722-141.77i;
Zout = 0.92621+81.158i;

%Zout' = 1/(i*2*pi*f*C + 1/Zl)
C = (1/(-i*imag(Zout)) - 1/(i*imag(Zl)))/(i*2*pi*f)

%If we would be switching to a higher frequency
f = 2.4e9;
%Zout' = 1/(1/(i*2*pi*f*L) + 1/Zl)
L = 1/((1/(-i*imag(Zout)) - 1/(i*imag(Zl))) * i*2*pi*f)
```

Appendix B

Matlab script: Analytical impedance matching

```
format long e;

c = 299792458;
f = 2.4e9;

er = 4.5;
W = 484.183e-6;
h = 633e-6;
t = 35e-6;

if W/h >= pi/2
Weff = W + (t/pi)*(1+log(2*h/t));
else
Weff = W + (t/pi)*(1+log(4*pi*W/t));
end
W = Weff

if W/h <= 0.6
lambda = ((c / f)/sqrt(er))*sqrt(er/(1 + 0.6*(er - 1)*((W/h)^0.0297)));
% For W/h <= 0.6
else
lambda = ((c / f)/sqrt(er))*sqrt(er/(1 + 0.63*(er - 1)*((W/h)^0.1255)));%
For W/h >= 0.6
```

```
end

if W/h <= 1
eff = ((er + 1)/2) + ((er - 1)/2)*(((1 + 12*(h/W))^(-0.5)) + 0.04*((1
- (W/h))^2)); % For W/h <= 1
Z0 = (60/sqrt(eff)) * log((8*h/W) + (0.25*W/h)); % For W/h <= 1
else
eff = ((er + 1)/2) + ((er - 1)/2)/sqrt(1 + 12*(h/W)); % For W/h >=
1
Z0 = (120*pi/sqrt(eff))/((W/h) + 1.393 + 0.667*log((W/h)+1.444));
% For W/h >= 1
end
Z0

yl = 1/(2.0596e+000 -1.1270e+002i);
y0 = 1/Z0;
Gamma = (yl - y0)/(yl + y0) % Because we use a Y Smith chart

GammaAbs = abs(Gamma)

b = [1-GammaAbs^2,0,4*y0^2-8*y0^2*GammaAbs^2,0,-16*GammaAbs^2*y0^4];
c = (i*real(roots(b)))';
d = y0 + c; % Be careful to have only the real solutions of b
GammaX = (d - y0)./(d + y0);
GammaXAbs = abs(GammaX);
Degrees = (angle(Gamma)-angle(GammaX))*360/(2*pi);
serial = (lambda/2).*(Degrees/360)

Gammajb = (c - y0)./(c + y0);
GammajbAbs = abs(Gammajb);
DegreesToGammaInf = angle(Gammajb)*360/(2*pi);
shunt = (lambda/2).*(DegreesToGammaInf/360)

lambda/4 + shunt
```

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