Analysis and design of automatic discrete frequency control for high-frequency oscillators

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Analysis and Design of Automatic Discrete Frequency Control for High-Frequency Oscillators

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Abstract

This thesis presents an analysis and design of automatic discrete frequency control systems for band-switched oscillators: An automatic frequency control (AFC) system must select the appropriate frequency band of an oscillator with several frequency bands. Automatic frequency control systems are divided into two types of systems: course frequency control (CFC) and frequency spread calibration (FSC) systems. In brief, CFC systems change frequency bands during operation and FSC systems select the appropriate frequency band at start-up. The main aim of this thesis are systems without any interference on sensitive analog points within the phase-locked loop (PLL).

Literature study has proven that *all digital AFC systems*, which rely on the reference clock and (digital) feedback signal in the PLL, are the most promising option. Furthermore, most presented systems use an open-loop and closed-loop step of the PLL. Therefore, two additional methods setting the phase-locked loop in an open-loop condition by means of switches in the digital part of the PLL are introduced.

The class of all digital AFC systems is subdivided into architectures using a variable divider ratio and architectures using a constant divider ratio. In addition, two types of digital frequency detectors are discussed: based on a counter or a digital logic quadricorrelator (DLQ). In particular, the DLQ combines minimum complexity with minimized measurement time per frequency measurement cycle.

In order to select the appropriate frequency band, generic frequency band requirements and selection criterions are developed for various detection scenarios. The selection criterions are illustrated with an example of a linear search algorithm, that uses these criterions.

The concept of a reduced division ratio in a variable divider CFC architecture is introduced. In this report, the reduction of the divider ratio decreases the necessary measurement time roughly by a factor of 7. A settling-time of less than $16\mu s$ can be achieved by combining the reduced division ratio with the digital frequency difference detector based on the DLQ.

Three CFC systems and one FSC system are designed with Verilog behavioral models in Cadence. This work shows that all digital AFC systems, which are not interfering with sensitive points within the PLL can be realized. No major problems are expected by conversion of the simulated AFC systems into actual implementations with digital circuits, as long as the frequency bands of the VCO meet the necessary frequency band requirements.

Contents

Introduction

The frequency range of integrated oscillators is subject to variation. This variation can be caused by temperature variations, power supply variations, aging and, for example, process-spread (in IC-technology the value of devices like capacitors, resistors, transistors vary a certain amount depending on their standard deviation). A standard way of dealing with process spread is increasing the nominal tuning range, such that the required tuning range is covered under worst-case conditions.

Increment of the tuning range of an oscillator to compensate process spread has, without special measures, a number of unwanted effects. A major drawback is an increase of the tuning constant of the oscillator. A high tuning constant means a high sensitivity for noise on the tuning input of the oscillator. Another drawback is that, for LC oscillators it may be impossible to meet the required tuning range with a single varactor.

Discrete tuning

A method to alleviate some of the problems associated with high tuning constants of oscillators, is adding a discrete tuning input. This added discrete tuning divides the total tuning range into several smaller, but overlapping frequency bands. An *automatic frequency control* (AFC) system must control this discrete tuning input and must select the appropriate frequency band. In addition to the discrete tuning, the analog fine-tune input is used to cover all the frequencies within one band. Since the tuning range of the analog fine-tune input is reduced significantly, this input is less sensitive for noise. Two types of automatic frequency control systems can be distinguished:

- *Coarse frequency control (CFC)*: This system works together with the phase-locked loop (PLL), which controls the fine-tune input of the voltage controlled oscillator (VCO). Every time a new frequency is selected, this CFC system selects the appropriate frequency band, followed by normal PLL operations which establishes phase-lock at the desired frequency.

- *Frequency spread calibration (FSC)*: This calibration system selects the proper frequency band at start-up and then disables further control of the discrete tuning input of the oscillator. Therefore, the required frequency range must be covered by the selected frequency band, during normal operation, taking into account external variations, like temperature effects and aging.

Project description

The main aim of this Master Thesis project is to give insight in automatic frequency control (AFC) systems for band-switched oscillators. Especially AFC systems working in the digital domain with minimum interaction with the PLL. And, if possible, no interference with the sensitive analog points within the PLL. The concept of a PLL with automatic frequency control of the VCO is illustrated in figure 1. This figure shows a PLL with an actuator (ACT), partially in the analog domain and partially in the digital domain. Furthermore, the AFC system with detector (DET) is completely in the digital domain.

A 4.5-7GHz LC oscillator with 16 frequency bands [4] will be used to demonstrate the concept of coarse frequency control (CFC). From this oscillator, another oscillator model can be derived, which fits the frequency band requirements for frequency spread calibration systems. This oscillator will be used for verification of the concept of frequency spread calibration (FSC). After that, the differences between CFC and FSC will be discussed.

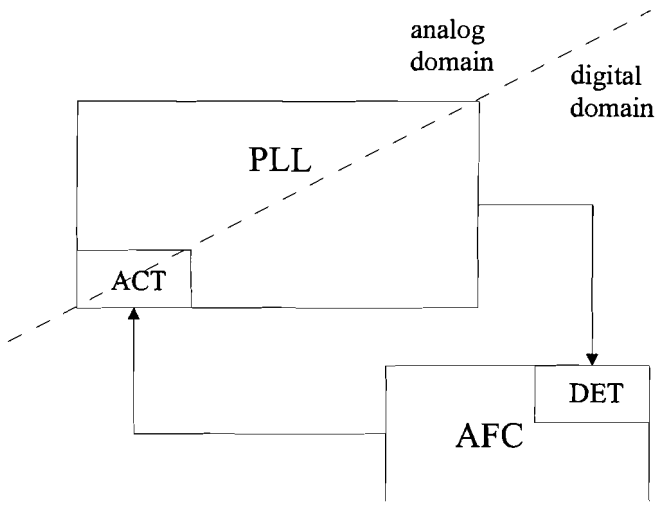

Figure 1: PLL with automatic frequency control in the digital domain

Problem definition

The following questions serve as the problem definition

- What are the differences between coarse frequency control (CFC) and the frequency spread calibration (FSC) systems?
- What do automatic frequency control systems assume from the VCO design (exact requirements for frequency bands):

  Number of frequency bands?

  Amount of span of the frequency bands?

  Amount of band overlap?

  Amount of variation due to external variables, like process spread?
- What are the actual band selection criterions?
- How is complexity growing with N (number of switches)?
- What kind of interaction with the PLL?

  Interaction on sensitive analog VCO control input?

  Possible unwanted frequency jumps?

  Possibility to shift the actuator and detector (see figure 1) into the digital domain?

New contributions

This work contributes to the classification of automatic frequency control (AFC) systems for oscillators with discrete tuning inputs. The existing AFC systems are divided into two types of systems: *coarse frequency control* and *frequency spread calibration.* After that, the all digital dual-loop architectures are subdivided into systems using a *variable* or *constant* division ratio. Furthermore, two (known) conditions of the VCO are introduced, which can be used during selection of the proper frequency band. These conditions, in combination with the type of system and the choice of a variable or constant division ratio, are called *detection scenarios.*

Several detection scenarios are discussed in chapter 4. For each detection scenario, generic frequency band requirements are given, resulting in relationships between necessary detector accuracy and band overlap or band spacing. These requirements are optimized for speed (minimized settling-time) and illustrated by means of examples. Furthermore, necessary band selection criterions are derived from the generic band requirements. Some are illustrated with an example of a linear search algorithm using these selection criterions.

In chapter 3, the basic all-digital AFC system is divided into four functionalities. The relationships between the main parameters of these functionalities are derived. Furthermore, the difference between asymmetric and symmetric detection for the case of a frequency counter is made (for example, asymmetric detection is used in [11]). This work suggests using the

symmetric detection, because the absolute frequency error is less than in the case of using asymmetric detection. The remaining part of this chapter shows the properties of the frequency difference detector based on a digital logic quadricorrelator[9] (DLQ), which is a very good alternative for a frequency counter.

Most AFC systems use an open-loop step, followed by a closed-loop step of the PLL. In chapter 2, two additional methods are presented, setting the PLL in an open-loop condition and the VCO in a known condition (e.g. at the start of each frequency band). These methods use switches in the digital part of the PLL and *do not interfere with the sensitive analog part.* One of these methods (the fastest), is the preferred method for course frequency control systems.

In chapter 5, the concept of reducing the division ratio is introduced: the reduced division ratio decreases the settling-time of the search algorithm. Furthermore, the conversion of the band requirements for a frequency counter to a frequency difference detector based on the DLQ is described.

Chapter 5 and 6 show examples of all-digital AFC systems that are implemented by means of behavioral models in a Verilog/Cadence simulator environment. These simulations verify the theory presented in chapter 3 and 4, by means of testing of worst-case scenarios. Therefore, no major problems are expected by the actual implementation of these AFC systems with digital circuits, as long as the frequency bands of the VCO meet the band requirements that are introduced in chapter 4.

Answers to the questions

- What are the differences between CFC and FSC systems? *Although both systems use the same digital dual-loop topology, the major difference between the CFC and FSC systems is the frequency band parameter to be detected: band overlap and band spacing for CFC and FSC, respectively. Furthermore, the preferred detection scenario (see chapter 4) is different for both systems.*

- What do automatic frequency control systems assume from the VCO design (exact requirements for frequency bands)? *The requirements for the frequency bands of the oscillator are dependent on the type of system (CFC or FSC) in combination with the used detection scenario; generic requirements are derived in chapter 4 for each discussed detection scenario.*

- What are the actual band selection criterions? *The band selection criterions are optimized for speed (minimized settling-time) and are derived in chapter 4 for each described detection scenario.*

- How is complexity growing with N (number of switches)? *In the case that the AFC system uses a separate band selector, without a sophisticated search algorithm (which is not needed due to the application of the digital quadricorrelator), then the amount of hardware will not increase to a great extend for increasing N.*

- What kind of interaction with the PLL? *Every AFC system must be enabled before it will select a new frequency band. Therefore, no unwanted frequency jumps are possible. Furthermore, the interaction on sensitive analog VCO control input can be minimized by using switches in the digital part of the PLL; two possible methods are introduced in chapter 2.*
- Possibility to shift the actuator and detector into the digital domain? *This thesis shows that all digital AFC systems can be realized, having the actuator and detector completely in the digital domain.*

Structure of this Thesis

In the first chapter, basic properties of voltage controlled oscillators are described. After that, the concept of frequency bands in an oscillator is introduced. Finally, the chapter is concluded with two examples of band-switched LC oscillators. Both oscillators will be used in a design of an automatic frequency control system.

The second chapter discusses a phase-locked loop, with the emphasis on the commonly used integer-N charge-pump PLL. Each building block is briefly reviewed and behavioral models are developed. The remaining part of this chapter deals with several methods setting the PLL into an open-loop condition, which is used by most automatic discrete frequency control systems.

Then this work proceeds with chapter three about discrete frequency control. First of all, the difference between the two types, *coarse frequency control* and *frequency spread control*, is discussed. After that, an overview of state-of-the-art systems will be given. The remaining part of this chapter focusses on all digital discrete frequency control systems and a subdivision of these systems is introduced as well as digital frequency detection.

Chapter four deals with requirements for oscillator frequency bands, which are dependent on the type of discrete frequency control system. Throughout this chapter generic band selection criterions are developed, which ensure selection of the appropriate frequency band. In addition, most mentioned band detection scenarios are illustrated by means of an simple example.

The fifth chapter deals with three designs of CFC systems. The main aim of making these designs is to verify the band requirements and selection criterions, introduced in chapter four. Furthermore, the settling-times and complexity of these systems will be compared.

In chapter six, a design of an FSC system is described. This system is used to verify the frequency band and selection criterions for FSC systems. In appendix F, a more complex predecessor of this system is described.

The final chapter summarizes the conclusions that are made throughout this report.

Chapter 1

Voltage controlled oscillator

As illustrated in figure 1.1, a voltage-controlled oscillator (VCO) generates an output signal, depending on a control input. The frequency of this output signal is a function of the voltage at the control input. The relationship between the output frequency (f_{out}) and the control voltage (V_{ctrl}) is given by

$$f_{out} = f_0 + K_{vco}(V_{ctrl})V_{ctrl} \tag{1.1}$$

where f_0 is the output frequency when the control voltage is 0V and $K_{vco}(V_{ctrl})$ is the tuning function [Hz/V] of the VCO.

The output frequency, given in equation 1.1, of integrated oscillators is subject to variation, due to changes in external variables, like: process-spread, supply voltage, temperature and aging. For example, process-spread in IC-technology causes that the value of devices like capacitors, resistors, transistors varies a certain amount depending on their standard deviation. Therefore, the spread in center frequency can easily be as large as 30% for ring oscillators and more than 15% for LC oscillators [1].

This chapter deals with some basic oscillator properties, like center frequency, tuning range, tuning constant and finally phase noise. After that the concept of a VCO with frequency bands will be discussed, for narrow-band and wide-band systems. Subsequently LC oscillators which use band-switching will be considered. Finally, two examples of band-switched VCOs will be presented in combination with an approximation of the process-spread, because behavioral models of these two VCOs will be used in simulations of automatic frequency control systems.

Figure 1.1: The block diagram of a VCO

Table 1.1: Center frequency, absolute tuning range and relative tuning range of several standards [1]

Standard	Center frequency [MHz]	Absolute tuning range [MHz]	Relative tuning range [%]
FM radio front-end	97.75	87.5 - 108	21
TV receiver	500.5	41 - 960	184
GSM transmitter	902.5	890 - 915	2.8
GSM receiver	942.5	925 - 960	3.7
Satellite TV front-end	1550	950 - 2150	77
DECT transceiver	1900	1880 - 1920	2.1
UMTS transmitter (FDD)	1950	1920 - 1980	3.1
UMTS receiver (FDD)	2140	2110 - 2170	2.8
Bluetooth	2441.5	2400 - 2483	3.4

1.1 Oscillator properties

Some basic oscillator properties will be discussed in the following paragraphs

Center frequency
The center frequency (f_c), or mid-range output frequency, is determined by the application in which the VCO is used. Table 1.1 shows the center frequencies of a number of RF standards.

Absolute tuning range
The absolute tuning range is defined by the minimum and maximum output frequencies (f_{min} and f_{max}) that an oscillator can reach. Table 1.1 also gives the minimum absolute tuning range for the given standards.
Especially the specified tuning range must be met under worst-case conditions. Therefore *frequency deviations* due to process-spread, supply voltage variations, temperature changes and aging should be *added* to the actual tuning range of a VCO.

Relative tuning range
The relative tuning range is defined by $(f_{max} - f_{min})/f_c * 100\%$ and roughly divides the given systems into two categories: *wide-band* and *narrow-band* systems. For example, FM radio, television and satellite TV are wide-band systems and telecom systems like GSM, UMTS, DECT and Bluetooth are narrow-band systems.

VCO tuning function
The VCO tuning function is dependent of the control voltage at the input of the VCO. It is a non-linear function and the characteristic typically exhibits a high gain region in the middle of the range and a low gain region at the two extremes [3]. Very often this function is approximated by a linear function,

and then this is called a VCO tuning constant (K_{vco}), which is defined as the ratio of the output frequency over the input control voltage

$$K_{vco} = \frac{f_{max} - f_{min}}{dV_{ctrl}} \tag{1.2}$$

This constant will become larger if the tuning range is increased, to cover process-spread for example. If the supply voltage decreases, in case of a redesign using a newer technology for example, the maximum control voltage swing will also decrease and thus K_{vco} will increase [1].

Phase noise
Phase noise is undesired energy spread continuously in the vicinity of the output frequency, possessing a higher power density at frequencies closer to the fundamental of the output frequency [2]. Furthermore, phase noise is often the most damaging of all noise contributions to the spectral purity of the output signal of an oscillator. A concern in the design of oscillators is the phase noise as a result of the noise on the VCO control input. The noise in the output frequency is proportional to K_{vco} and the noise voltage on the control input, see equation 1.1. Thus for low noise applications, it is advantageous to implement a VCO with a minimized tuning constant and this can be in conflict with the required tuning range.

1.2 Frequency Bands

In general, increasing the nominal tuning range of an oscillator, such that the required tuning range is covered under worst-case conditions, could be used. But, a wider tuning range results in a higher K_{vco} and therefore a higher noise sensitivity of the VCO control input. A way to achieve a large tuning range and a small K_{vco} simultaneously, is by breaking a single wide-range tuning curve into several narrower-range sections with some frequency overlap [3]. This leads to the concept of switch-selected tuning elements in a VCO.

1.2.1 Switch-selected tuning

Three types of switch-selected tuning will be discussed in the following paragraphs.

Switched capacitors
An LC oscillator may be tuned by connecting some combination of MOS capacitors selected from an array. The challenge here is to build a satisfactory RF switch, which will select the capacitors. The switch resistance must be sufficiently low to not degrade the capacitor Q. This implies a MOSFET with a large W/L ratio, whose large junction capacitance will now parasitically load the capacitor array when the MOSFET is turned OFF, and compresses the available spread in capacitance [3].

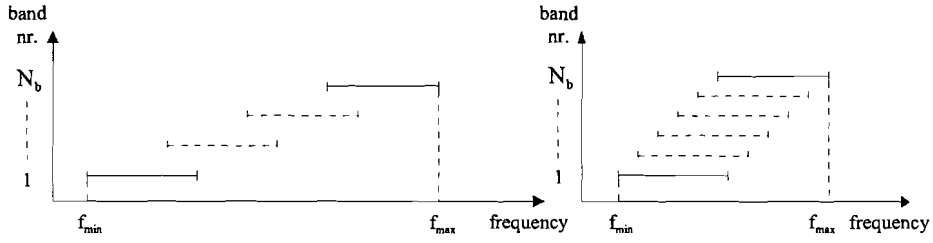

Figure 1.2: Frequency bands in a wide-band and a narrow-band system.

Switched inductors / switched oscillators
While a series MOSFET is able to select a capacitor without heavily degrading the resonator Q, when used in series with an inductor it adds a much larger relative loss. However, one of an array of independent oscillators may be selected with a MOSFET switch [3].

Switched current sources
One way to change the operating frequency in a ring oscillator is to change the current through an amplifier stage (varying g_m). An array of switched current sources can be used to achieve a piecewise frequency-current characteristic.

1.2.2 Band positioning

The partially overlapping frequency bands of an oscillator should be positioned differently in narrow-band and wide-band systems. Figure 1.2 shows an example of the frequency bands for a narrow-band system and a wide-band system.

Wide-band systems
In wide-band systems the desired frequency range is large. As mentioned earlier, a way to achieve a large tuning range and a small K_{vco} simultaneously, is by using several narrower-range sections with some (small) frequency overlap. Every time a new frequency is selected in the system, an automatic frequency control system must select the appropriate frequency band, after that the PLL locks on the (exact) desired frequency. In this report, this will be called *course frequency control.*

Narrow-band systems
In narrow-band systems the desired relative tuning range (<5%) is small in comparison with the total relative tuning range ($\approx$ 30%), which must be implemented to compensate for external variations. An automatic frequency control loop must select the proper frequency band at startup, this will be referred to as *frequency spread calibration.* Therefore, the minimum frequency overlap between two adjacent frequency bands is at least the required absolute frequency range of the given standard (see table 1.1). This will guarantee that at least one frequency band can cover the whole required frequency range. Obviously, each frequency band must still be able to compensate for external variations during operation (e.g. temperature changes).

1.3 LC oscillator

First of all, the frequency of oscillation of a LC oscillator will be discussed. Then the principle of band-switches is described and finally, two examples of LC oscillators with frequency bands will be given.

1.3.1 Frequency of oscillation

In order to calculate the frequency of oscillation a single-ended linear behavioral model of an ideal LC oscillator is introduced in figure 1.3. The (noiseless) resistor R represents all the losses that are present in the oscillator. These are compensated by the negative resistance amplifier with small-signal gain g_m. The LC tank inductance has a value L and the capacitance consists of several contributions: a parasitic capacitance C_p, a varactor capacitance C_v and a switched-capacitor array capacitance C_a. Sometimes some extra fixed capacitance C_f could be added. The frequency of oscillation can be derived easily

$$f_{osc} = \frac{1}{2\pi\sqrt{L(C_p + C_v + C_a)}} \tag{1.3}$$

The most common method of varying the frequency of oscillation is to vary the total capacitance. Therefore the varactor capacitance is a continuously tunable capacitance which varies from $C_{v_{min}}$ to $C_{v_{max}}$. Furthermore, the switched-capacitor array capacitance is a discretely changeable capacity, which can vary from the minimum array capacitance $C_{a_{min}}$ to the maximum array capacitance $C_{a_{max}}$.

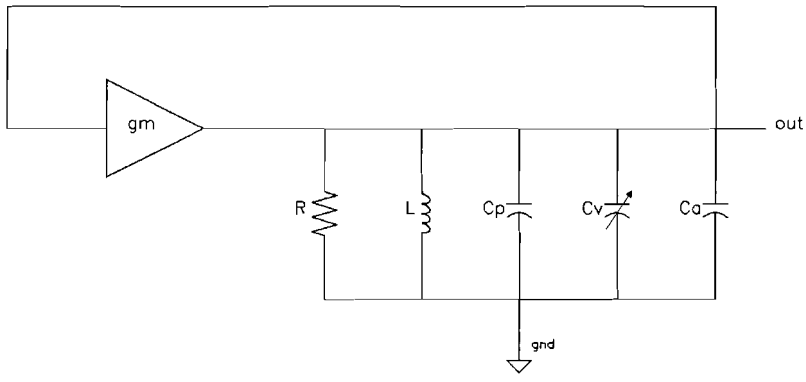

Figure 1.3: Single-ended linear behavioral model of a ideal LC oscillator [1]

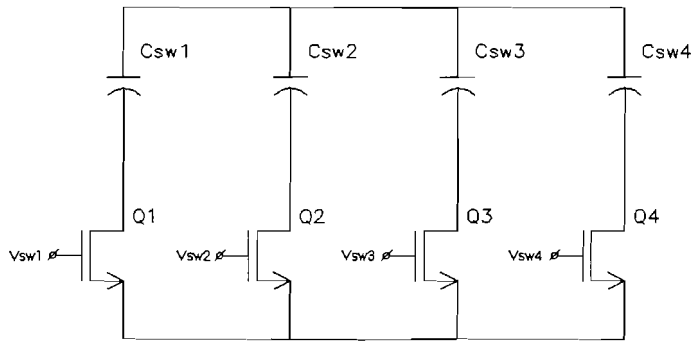

Figure 1.4: A capacitor array implementation

1.3.2 Band-switches

As mentioned before, a large tuning range combined with a good phase noise performance can be achieved if band-switching is used. A LC oscillator may be tuned by connecting some combination of capacitors selected from an array [3]. The capacitors can be sized equal, binary-weighted or other weighting schemes are also possible. In the case of equal capacitors, N identical switches and capacitors divide the tuning range in N+1 bands. In case of binary weighted capacitors, N capacitors divide the tuning range into 2^N bands, which is more efficient in terms of the number of required control signals [1].

Simplified models for a MOS-switch ($Q_1..Q_4$ in figure 1.4) in ON-state and OFF-state are a resistor R_Q and a capacitor C_Q, respectively. The switch ON-resistance must be sufficiently low, otherwise it will degrade the capacitor quality factor. The total capacitance in OFF-state of one branch is: $C_{off} = (C_{sw}^{-1} + C_Q^{-1})^{-1}$.

1.3.3 4.5-7GHz LC oscillator for course frequency control

An example of a LC oscillator using band-switching is a 4.5-7 GHz oscillator in CMOS 0.18μm [4]. This VCO will be used in combination with the *course frequency control* system, as will be discussed in chapter 5. In this oscillator, improved-Q differential switches are applied, but the principle of adding capacity with MOS-switches is the same. The resonator in this oscillator consists of an inductor of approximately 1nH, a paracitic capacitance of around 80fF, varactor with $\alpha_{varactor} = 2$ ($C_{v_{min}} = 125$fF to $C_{v_{max}} = 250$fF) and four binary weighted band-switches. The first band-switch represents an on-capacitance of $C_{on} = 64$fF and an off-capacitance of $C_{off} = 15$fF. The frequency bands of this VCO are illustrated in figure 1.5.

Process-spread simulation
The simulator takes 500 trails with randomly selected values of L and C from the interval [-4σ, 4σ] around the nominal value. The first simulation

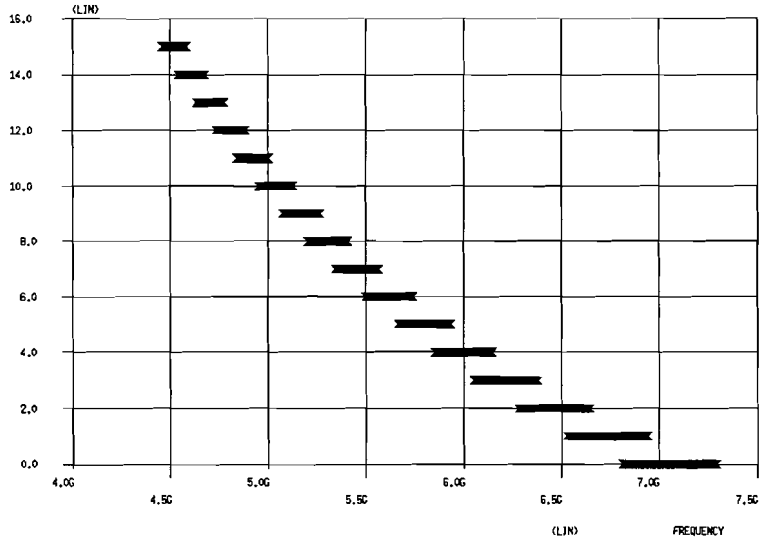

Figure 1.5: Frequency bands of the 4.5-7GHz LC oscillator

gives the spread of the minimum and maximum frequency of oscillation. The following values: σ_C=5% and σ_L=1% were used (absolute spread). The second effect occuring on a wafer is matching of the (nearby) capacitors. This can be simulated by means of a matching coefficient. These simulations are performed with the following values of σ_m: 0.25%, 0.5% and 1% (relative spread).

Both simulations were done separately. In the case of absolute component spread, the correlation between the (normal distributed) capacitor values is set to 1. In the case of the simulations for mismatch (relative spread), those values are completely uncorrelated.

The *absolute spread* on values of the inductor and the capacitors results in shifting the frequency bands upwards or downwards. The simulation results can be found in the appendix in table A.2 as well as illustrations of the shifted frequency bands. In brief, absolute spread causes the frequency bands to shift approximately 11% downwards and 14% upwards. If the frequency bands shift downwards, the frequency bands are compressed and if the frequency bands shift upwards, the frequency bands are extended. As a result the overlap between adjacent frequency bands is also approximately 11% less or 14% more in the case of shifting down or up, respectively

The *mismatch* of the capacitor values results in more or less frequency overlap between two adjacent frequency bands. The simulation results are given in the appendix in table A.3 for σ_m is 0.25%, 0.5% and 1% in the cases that the frequency bands are shifted down, up and in the nominal case. In brief, the frequency band overlap changes approximately 7% due to mismatch of the capacitor values.

1.3.4 5.1-6.7GHz LC oscillator for frequency spread calibration

The second example VCO is an oscillator model, which has similarities with the first VCO in inductor, capacitor and varactor values, but has 8 overlapping frequency band and will be used to demonstrate the *frequency spread calibration* system, as will be discussed in chapter 6.

The center frequency of the VCO in the first example will be the starting point for this model: $f_c = 5896\text{MHz} \approx 5900\text{MHz}$. The desired frequency band has a bandwidth of 100MHz and this band will be situated between: $f_b = 5850\text{MHz}$ and $f_e = 5950\text{MHz}$. Process-spread of $4\sigma_C = 20\%$ and $4\sigma_L = 4\%$ will shift the frequency bands to higher or lower frequencies. This sets the minimum and maximum operating frequency for the oscillator: $f_{min} \approx 5100\text{MHz}$ and $f_{max} \approx 6700\text{MHz}$. The calculation of the switched capacitor array values can be found in the appendix. Figure 1.6 shows the 8 overlapping frequency bands of this VCO.

Process-spread simulations were done with $\sigma_m = 1\%$ and the results are given in the appendix in table A.5 and A.6. As a result of the process-spread, the spacing between two adjacent frequency bands changes roughly by 4%.

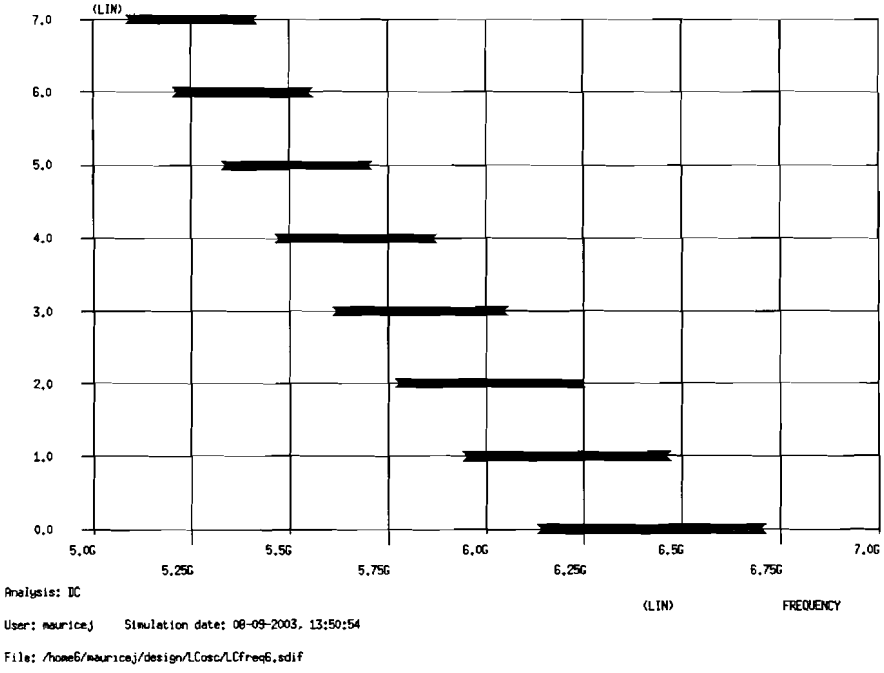

Figure 1.6: Frequency bands of the VCO for frequency spread calibration

1.4 Summary

Some basic oscillator properties were introduced, like center frequency, tuning range and phase noise. The center frequency of a VCO is the mid-range output frequency and absolute tuning range is defined by the minimum and maximum output frequencies. In general, the output frequency of a VCO is a function of the control voltage at the input and is subject to variation due to external variables (e.g. process-spread). Furthermore, phase noise is proportional to K_{vco} and the noise voltage on the control input. Thus, low noise applications require a VCO with a minimized tuning constant. However, a low tuning constant can be in conflict with the required tuning range.

A way to achieve a large tuning range and a small K_{vco} simultaneously, is by breaking a wide frequency band into several smaller, partially overlapping frequency bands. Therefore, switch-selected tuning elements are used in an oscillator. Then, an automatic frequency control system must select the appropriate frequency band.

The tuning range requirement will roughly divide the systems that use an oscillator into two categories: narrow-band and wide-band systems. The frequency bands of an oscillator should be positioned differently in narrow-band and wide-band systems. Therefore two example VCOs are presented in this chapter:

- The first example VCO will be used in a *course frequency control* system. Process-spread (assuming $4\sigma_C = 20\%$ and $4\sigma_L = 4\%$) will shift the frequency bands of this oscillator approximately 11% downwards and 14% upwards, this is also affecting the band overlap between two adjacent frequency bands by the same amount. In addition, the frequency band overlap changes approximately 7% due to mismatch ($\sigma_m = 1\%$) of the capacitor values in the capacitor array.
- The second example VCO has 8 overlapping frequency bands and will be used to demonstrate the *frequency spread calibration* system. In addition to the absolute spread, the frequency spacing between two adjacent frequency bands changes roughly by 4%, due to relative spread (mismatch, $\sigma_m = 1\%$).

Chapter 2

Phase-locked loop

Nowadays nearly all radio-frequency products rely on digital tuning functionality. The digital tuning systems use a voltage controlled oscillator which is incorporated in a feedback control loop, the phase-locked loop (PLL). This PLL achieves a very high absolute accuracy of the output frequency, which can be varied in small and precise steps.

This chapter deals with a commonly used integer-N architecture, followed by a brief review of the building blocks of a basic charge-pump PLL. After that, simulation results of a charge-pump behavioral model will be given. This model is used for simulations of the automatic frequency control systems. Finally, several methods to set the PLL in an open-loop condition are presented.

2.1 Integer-N PLL architecture

An integer-N PLL is illustrated in figure 2.1 and consists of a VCO, a frequency divider with divider ratio N, a phase detector and a loop filter. In addition, the architecture uses a reference divider with ratio M. The frequency divider (N) in the feedback loop will give a frequency multiplication of the input reference frequency. If the divider has value N, then the output frequency will be N times the input frequency. If the divider value is adjustable, the output frequency of a PLL is programmable. The output frequency produced is a function of the values selected for the input reference divider (M) and the feedback divider (N), such that

$$f_{out} = N(\frac{f_{ref}}{M}) \tag{2.1}$$

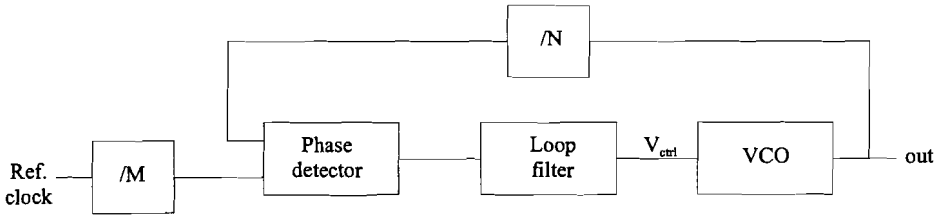

Figure 2.1: Standard integer-N architecture

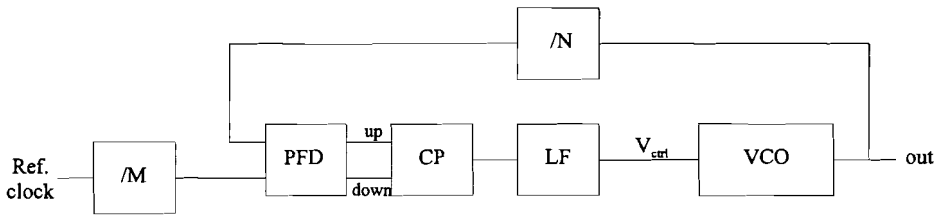

Figure 2.2: Charge-pump PLL

2.2 Charge-pump PLL

Figure 2.2 shows a charge-pump PLL, which consists of a phase/frequency Detector (PFD), charge pump (CP), loop filter (LF), voltage controlled oscillator (VCO), a feedback divider N and a reference divider M.

Phase-frequency detector: This part determines the phase difference between the input reference frequency and the output frequency. The two outputs, UP and DOWN drive the charge pump.

Charge-pump: This part sinkes or sources current from or into the loop filter, depending on the up and down input signals.

Loop filter: A low-pass filter is used to attenuate the high-frequency components produced by the PFD/CP combination and for stabilizing the loop.

Voltage controlled oscillator: This device generates a sinusoidal signal at a frequency which is a function of the control voltage. As mentioned earlier, a VCO has the following characteristic: $f_{out} = f_0 + K_{vco}(V_{ctrl})V_{ctrl}$. The first integrator in this loop is the VCO, the second integration is the result of the CP/LF combination, which results in a type II PLL.

Frequency dividers: The reference divider divides the reference frequency by M. The feedback divider divides the frequency at the input by a variable factor (N). With this variable N, the PLL is able to generate frequencies that are integer multiples of the (fixed) reference frequency, according to (2.1).

2.2.1 Phase-frequency detector

A phase-frequency detector (PFD) circuit can detect both phase and frequency differences, as illustrated in figure 2.3. The Q_A and Q_B outputs of the PFD are not complementary and are usually called "UP" and "DOWN" signals.
An example of the operation of a PFD: If the frequency of input A is greater than that of input B, than the PFD produces pulses at Q_A, while Q_B remains zero. Conversely, if $\omega_A < \omega_B$, then positive pulses appear at Q_B while $Q_A = 0$. If $\omega_A = \omega_B$, then the circuit generates pulses at either Q_A or Q_B with a width equal to the phase difference between the two inputs. Thus, the average value

of $Q_A - Q_B$ is an indication of the frequency or phase difference between A and B [5].

At least *three states* are required to create a circuit with the above mentioned behavior: $Q_A = Q_B = 0$; $Q_A = 0$, $Q_B = 1$; and $Q_A = 1$, $Q_B = 0$. The circuit could be implemented as an edge-triggered sequential state machine. The states can only change at the rising transitions of A and B. Figure 2.4 shows a state diagram of the operation of this PFD. If the PFD is in state "0", a transition on A will put the PFD in state "I". The circuit remains in this state until a transition occurs on B, then the PFD returns to state 0. The switching sequence between states "0" and "II" works similar [5].

Two extra points will be mentioned:

- If ω_{out} is far away from ω_{in} the PFD varies the control voltage such that ω_{out} approaches ω_{in}. When the input and output frequency are sufficiently close, the PFD operates as a phase detector, performing phase lock. In this case a linear model can describe the locking behavior, see appendix B.
- In practice, a PFD will produce narrow reset pulses on the outputs Q_A and Q_B, if the PLL is in lock.

PFD behavioral model
The behavioral model in Verilog is a three-state behavioral model and if the loop is in lock, this model simply produces $Q_A = Q_B = 0$ instead of the narrow reset pulses on the outputs.

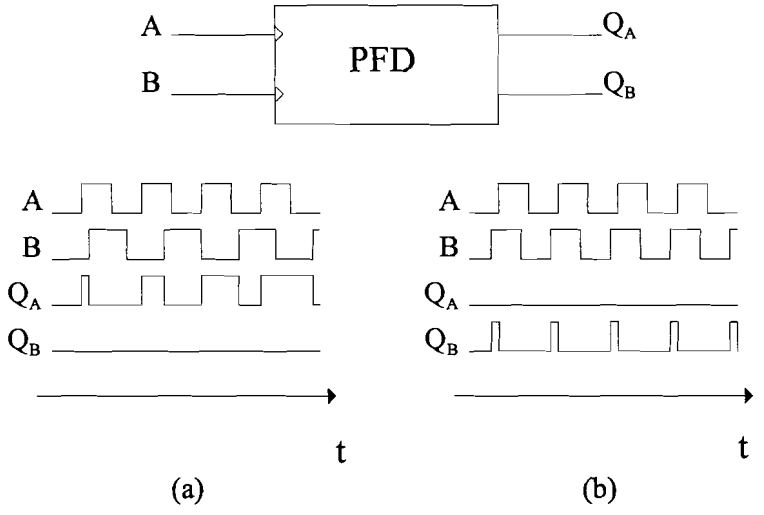

Figure 2.3: PFD response with (a) $\omega_A > \omega_B$, (b) A lagging B [5]

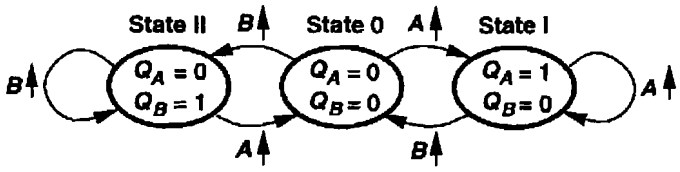

Figure 2.4: PFD state diagram [5]

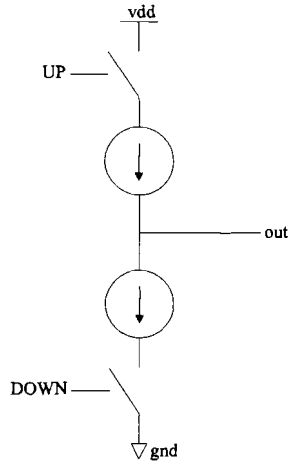

Figure 2.5: CP current sources

Table 2.1: Output table of the Charge-pump

UP	DOWN	Out
0	0	high imp.
0	1	$-I_{cp}$
1	0	$+I_{cp}$
1	1	0

2.2.2 Charge-pump

As illustrated in figure 2.5, a charge-pump (CP) consists of two switched current sources and has two inputs. The output of the CP drives the loop filter. The "UP" and "DOWN" inputs can be active or not active. Therefore, the output has four different states, which can be found in table 2.1.
In the case of two ideal switched current sources, the behavior of the CP can be described as follows: If the UP-input is active, the circuit acts as a current source, pumping current into the LF. In the case of an active DOWN-input, the CP circuit is a current sink, and the current flows from the LF into the CP. If both inputs are active, then both current sources are "ON" and this results in *zero* output current. If both inputs are not active, both current sources are switched "OFF" and therefore the output of the CP is high impedant.
In practice some mismatch will always be present between the UP and DOWN current sources. This will result in a mismatch output current ($I_{mismatch}$) in the case of two active inputs and in a small leak current (I_{leak}), if both inputs are not active.

Charge-pump behavioral model
Although a simple charge-pump model consists of two ideal switched current sources, this cannot be used in the behavioral model of the PLL. The *integration* of the CP/LF combination, together with ideal current sources, results in unrealistic values of the output voltage of the CP/LF combination. In practice the output voltage of the CP/LF combination is limited (between negative and positive power supply voltage) and therefore output current of the CP is also limited. Thus, the output current of a CP must be a function of the loop-filter voltage. A CP behavioral model has been derived from a charge-pump build with CMOS18 models and the results are given in appendix B.

The *advantages* of the charge-pump behavioral model are: The output current is easy changeable, the UP and DOWN currents are exactly matched (therefore the mismatch current will be *zero*), the leak current (when the output is high impedant) is also *zero*. Further explanation of the behavioral model and simulation results can be found in appendix B.

2.2.3 Loop filter

In [8] is shown that the output of the CP vanishes when the phase difference between the input signals of the PFD is zero. This is an ideal locking position for the loop: There is no current injection into the loop filter. Phase lock with zero phase error, for all possible output frequencies requires a loop filter with infinite DC gain. In other words, the loop filter must perform an integration operation on the CP output signal. A simple capacitor suffices to realize the integration function at the loop filter [8].

On the other hand, the loop already contains a perfect integrator: the VCO. So, the addition of another perfect integrator in the loop leads to instability, unless further measures are taken to increase the phase margin. For that reason

a resistor (R_1) should be added in series with the capacitor (C_1), resulting in a first order filter, yielding a second-order PLL system [8].
Every time current is injected into the series combination of the capacitor and resistor, the control voltage makes a voltage step. As a consequence the minimum loop filter configuration found in practice includes an additional capacitor (C_2) in parallel to the R_1C_1-section. The purpose of this extra capacitor is to decrease the loop filter trans-impedance for higher frequencies and therefore suppress the (initial) voltage step. The loop filter is now a second order filter and the PLL a third-order system.

Second-order filter
A way to calculate a second-order loop filter for an CP-PLL can be found in appendix B. An example of a second-order filter, which gives a PLL loop with a phase margin of 55^0, with VCO band number 7 (5393MHz - 5582MHz, K_{vco} = 105MHz/V), reference frequency f_{ref}=1MHz, Divider ratio N = 5500 and charge-pump current $I_{CP} = 200\mu$A results in calculated loop-filter component values of: $R_1 = 183\text{k}\Omega$, $C_1 = 27.6$pF and $C_2 = 3.05$pF.

2.2.4 Simulation results

The complete behavioral model of a charge-pump PLL in Cadence is illustrated in figure 2.6. The PFD, CP, VCO and programmable divider N are build with Verilog models. The band-switched VCO has 16 frequency bands and further details about this VCO are given in chapter 1 and in appendix A. Furthermore, the divider ratio N, the charge-pump output current and LF component values can easily be changed.

A simulation result of normal locking behavior is given in figure 2.7, which shows that the PLL achieves phase-lock at the desired frequency of 5500 MHz: At marker A the output frequency is 5581 MHz and at marker B the output frequency 5500 MHz. In addition, the phase of the FB and REF signals is the same at marker B.

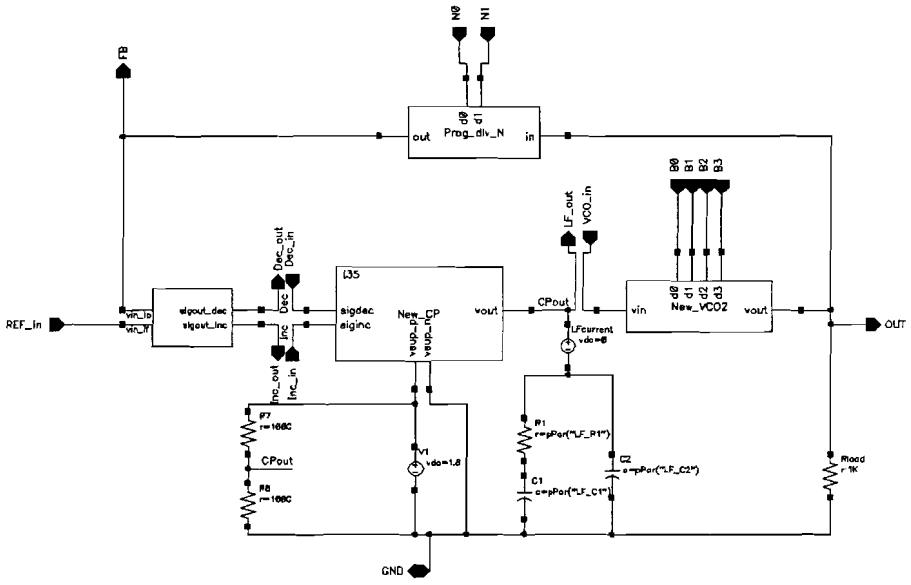

Figure 2.6: The PLL model in Cadence

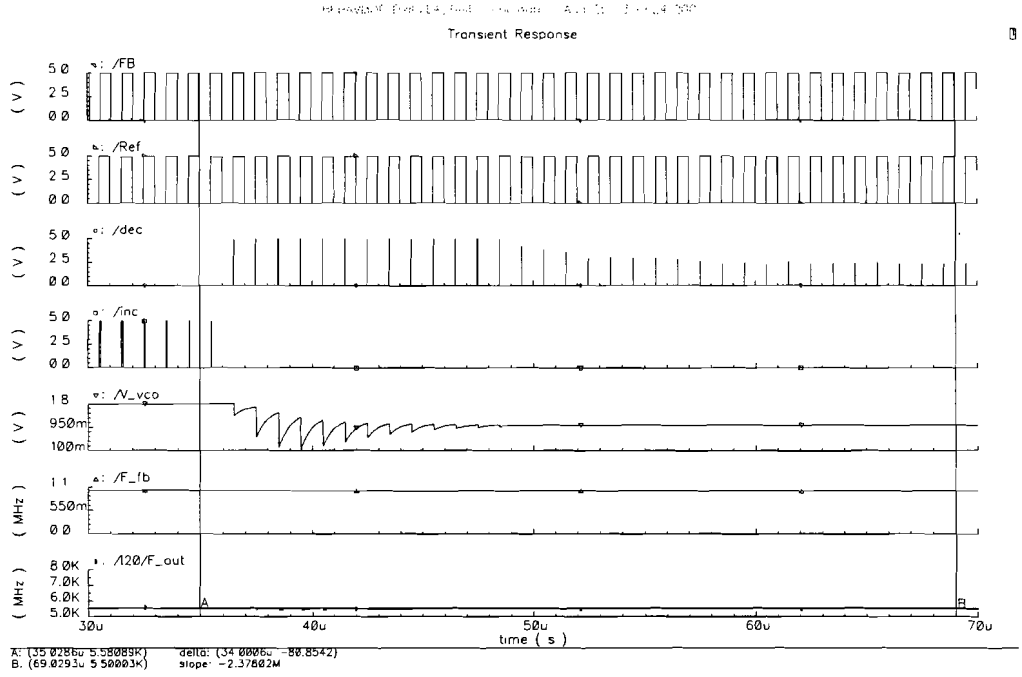

Figure 2.7: A simulation result of the PLL: f_{REF} = 1MHz, FB = feedback signal, inc = UP and dec = DOWN output of the PFD, V_vco = loop filter voltage, F_out = output frequency.

2.2.5 Open-loop condition

A commonly used method, in automatic frequency control systems, is setting the PLL in an open-loop condition, during selection of the appropriate frequency band of the oscillator. After that, the PLL is returned into normal closed-loop operation and the PLL locks on the desired output frequency. This section gives four possibilities to set the phase-locked loop in an open-loop condition.

The first two methods are reported in the literature and use a reference voltage at the input of the VCO, which can be defined at any level between V_{ss} and V_{dd}. Therefore, the center frequency of each frequency band can be selected during automatic frequency control. In some cases, which are discussed in chapter 4, the VCO output frequency can be set at the start (or end) of each frequency band. Then, the third or fourth method can be used.

Switches between LF and VCO (no. 1)
The first method to open the fine-tune loop is illustrated in figure 2.8. To set the PLL in an open-loop condition, switch SW1 is opened and a reference voltage is connected to the VCO control input (by means of switch SW2). For example, this method can be used to set the VCO at the center output frequency, during automatic frequency control. After selection of the desired frequency band of the VCO, the reference voltage is disconnected and the fine-tune loop is closed. In practice, the switches are implemented with (noisy) MOS-switches, therefore a drawback of this method is the interference with the noise sensitive analog control input of the VCO.

Switches before CP and between LF and VCO (no. 2)
The second way to open the fine-tune loop is given in figure 2.9. The principle is same as the first method: During open-loop condition, a reference voltage is applied to the control input of the VCO. But, instead of using a switch between the LF and the VCO, the inputs of the CP are disconnected from the PFD. This results in a high impedance output of the CP and therefore the loop-filter voltage can be controlled by the reference voltage source. An advantage in comparison with the first mentioned method is the absence of the MOS-switch between the LF and the VCO input. The switching is partially moved to the digital inputs of the CP, which are less sensitive to noise than analog tuning input of the VCO.

It must be noted that the loop-filter capacitors will be (dis)charged to a level equal to the reference voltage. In the case that the reference voltage is at mid-range voltage, the loop-filter voltage is at mid-range voltage and the initial VCO output frequency will be around the center frequency when the fine-tune loop is closed. Therefore, this method can be used to achieve a fast settling time of the closed-loop step.

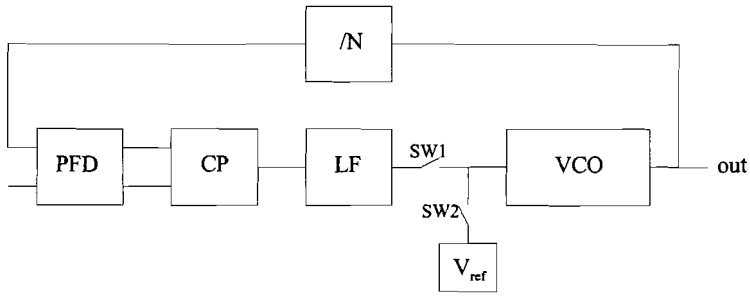

Figure 2.8: Open-loop condition will be established by opening SW1 and closing SW2 (method 1).

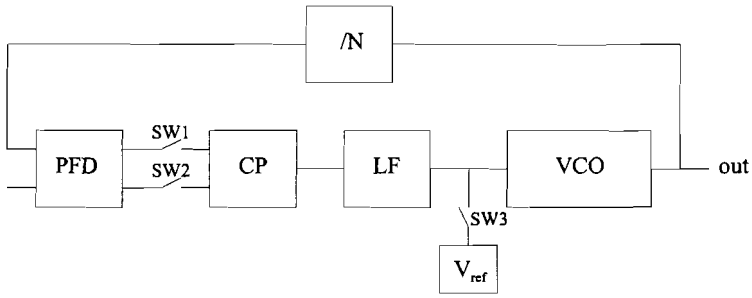

Figure 2.9: Open-loop condition will be established by opening switches SW1 and SW2 and closing SW3 (method 2).

Switches controlling the PFD (no. 3)
The third method uses switches at the digital inputs of the PFD and is illustrated in figure 2.10. While the PLL is in normal operation, switch SW1 is closed and the reference clock is connected to the input of the PFD. In open-loop condition, this input of the PFD is at a constant level, either V_{ss} or V_{dd}. Therefore, the loop-filter voltage will settle at V_{ss} after a certain time. On the other hand, if the switching would be applied in the feedback line of the PLL, then the loop-filter voltage would settle at V_{dd}.

To demonstrate a *drawback* of this method, the state-machine behavior of the PFD will be recalled: The PFD has three states. In the case that the PFD is in the "UP" state, two rising edges at the feedback input (FB) of the PFD are required, to set the PFD into the "DOWN" state. If the PLL is lock (before opening the loop), the frequency of the FB-signal is the same as the frequency of the reference clock and the delay time can be calculated as follows:

Example: If the reference frequency f_{ref} = 1MHz, then the worst-case delay time is 2μs, see simulation result in appendix B. One way to decrease this delay time is by decreasing the divider ratio in the feedback loop, another way is to use of the next mentioned method.

Switches controlling the CP (no. 4)
The switches, directly controlling the charge-pump of the PLL, are illustrated in figure 2.11. During normal operation, the switches SW1 and SW2 are closed. In open-loop condition, these switches are open and V_{dd} will be connected to the DOWN or UP input of the CP. This will result in a loop-filter voltage of V_{ss} or V_{dd}, respectively.

The settling-time of the loop-filter voltage to V_{ss} or V_{dd} depends on the charge-pump output current (I_{CP}) and the value of capacitor C_2 in the loop-filter and can be approximated with

$$I_{CP} = C_2 \frac{dV}{dt} \tag{2.2}$$

Example: The charge-pump output current is 200μA and the value of C_2 is 3pF. Then the worst-case settling-time is approximately 30ns, which is much faster than the previous mentioned 2μs of method three. Simulation results of the settling-time of the third and fourth system can be found in appendix B.

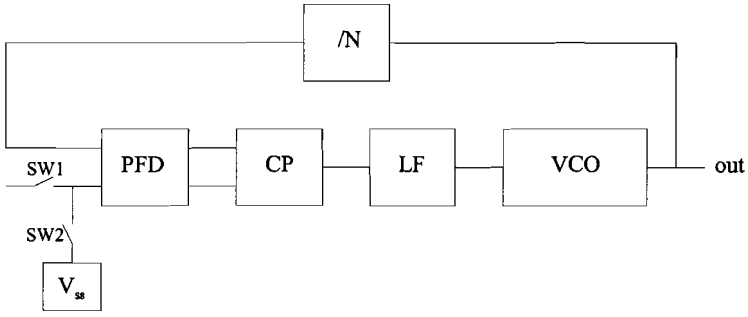

Figure 2.10: In open-loop condition, one input of the PFD will be at a constant level, driving the loop filter voltage to either V_{ss} or V_{dd} (method 3).

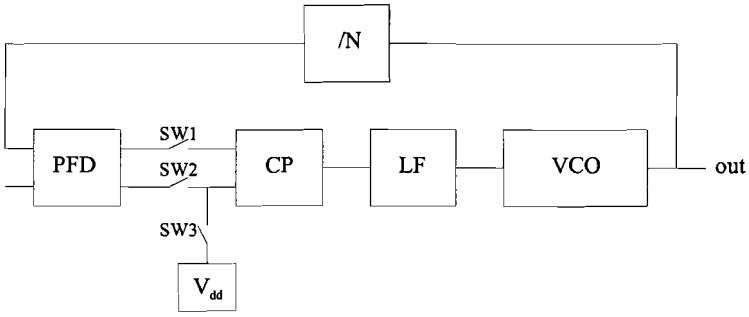

Figure 2.11: In open-loop condition, switches SW1 and SW2 are open and the CP will be set in the UP or DOWN state (method 4).

2.3 Summary

A commonly used PLL architecture is the integer-N charge-pump PLL architecture. This PLL consists of a PFD, CP, LF, VCO, a feedback divider and a reference divider.

The frequency divider in the feedback loop will give a frequency multiplication of the input reference frequency. If the divider is adjustable, the output frequency of a PLL becomes programmable.

A PFD can detect both phase and frequency differences. The outputs of the PFD are not complementary and are usually called "UP" and "DOWN". Therefore, the behavioral model in Verilog is a three-state model, see figure 2.4.

A CP consists of two switched current sources and has two inputs. The output of the CP drives the loop filter and the output current of a CP must be a function of the loop-filter voltage. A CP behavioral model has been derived from a charge-pump build in CMOS18. Three advantages of the behavioral model are: The output current is easy changeable, the UP and DOWN currents are exactly matched and the leak output current is zero.

The minimum LF configuration found in practice consists of a capacitor (C_2) in parallel to a R_1C_1-section. The capacitor C_2 decreases the loop filter trans-impedance for higher frequencies, yielding a second order filter and a third-order PLL system.

The complete behavioral model for a charge-pump PLL has been made in Verilog. In brief, the divider ratio N, the charge-pump output current and LF component values can be changed. Simulation of this charge-pump PLL model, in combination with a behavioral model of the first example VCO (see chapter 1), shows phase-lock exactly at the desired frequency.

Four methods setting a PLL in an open-loop condition have been presented. Whereas the first two mentioned methods use switches in the sensitive analog part of the PLL, the third and fourth method use switches in the digital part of the PLL. Therefore, these methods *do not interfere with the sensitive analog part of the PLL.* But, these methods (using switches in the digital part of the PLL) can only set the VCO at the start (or end) of each frequency band. Especially the fourth method, controlling the CP inputs directly, drives the loop-filter voltage to V_{ss} or V_{dd} with a minimized settling-time. Therefore, this method will be used in the design automatic frequency control systems given in chapter 5 and 6.

Chapter 3

Discrete frequency control

Automatic frequency control (AFC) systems can be classified into two types of systems: *coarse frequency control* and *frequency spread calibration*, both systems will be discussed in the next two sections. After that, the state-of-the-art AFC systems will be classified into four main architectures. In particular, the all digital AFC system is the most promising solution; in addition to the four main architectures, the all digital *dual-loop* systems will be subdivided into two subclasses: variable divider and constant divider architectures. Finally, two types of digital frequency detectors will be discussed.

3.1 Coarse frequency control

Course frequency control (CFC) is often used in wide-band systems, where the required frequency range is large. As mentioned earlier, a way to achieve a large tuning range and a small K_{vco} simultaneously, is by using several narrow-range sections with some (small) frequency overlap. Every time a new frequency is selected in the system, a CFC system must select the appropriate frequency band. After that, the PLL can lock on the (exact) desired frequency. In general, each frequency band must be able to compensate for the quantization error of the discrete CFC system.

3.2 Frequency spread calibration

In narrow-band systems the desired relative tuning range (<5%) is small in comparison with the implemented relative tuning range ($\approx$ 30%), to compensate for external variations. As mentioned before, a number of overlapping frequency bands can be used instead of one broad frequency band covering the whole desired frequency range. Then, a frequency spread calibration (FSC) system must select the proper frequency band at power-up. After that, further control of the discrete tuning is disabled. Therefore, the minimum frequency overlap between two adjacent frequency bands is at least the required absolute frequency range of the given standard (for examples, see table 1.1). This guarantees that at least one frequency band can cover the whole required frequency range.

Obviously, each frequency band must still be able to compensate for external variations (e.g. temperature changes) during operation, which are assumed to be relatively small in comparison to the process spread variation.

3.3 State-of-the-art

This section roughly divides the AFC systems, found in the literature, into four main architectures, which are described below. After that, the used algorithms are briefly described, followed by some implementation examples. Finally, an overview of the state-of-the-art AFC systems will be given.

3.3.1 Used architectures

The AFC systems can be divided into four main architectures and the most important properties of these architectures are described below.

AFC relies on V_{LF} architecture (no. 1)
The first automatic frequency control architecture is given in figure 3.1. In this topology, the automatic frequency calibration (AFC) system uses the phase detector and the charge-pump of the PLL. A major drawback of this architecture is interference with the sensitive analog part of the PLL.

The automatic frequency tuning works in the following way: Switch SW1 is opened and SW2 is closed. Then, a reference voltage (V_{ref}) is applied to the VCO and this reference voltage could be the center of the voltage range, e.g. at mid-range voltage. The loop filter voltage (V_{LF}) is applied to the AFC through a high-input impedance amplifier. The AFC system applies a sequence of digital control values to the N discrete tuning inputs of the VCO, selecting different operating curves. For each VCO operating curve an output signal (*out*) is generated. The charge pump will drive the loop-filter voltage V_{LF} either to the negative supply voltage or to the positive. This depends on whether the frequency of the feedback signal (FB) is greater than or less than the frequency of the reference signal divided by the input divider (M). Each digital control input value N in the sequence is applied for a period of time, and the AFC system can eventually identify two VCO operating curves that have center frequencies just above and just below the frequency of the reference signal. One of these two operating curves is be selected for use during normal PLL operations. After automatic tuning, switch SW1 is closed and switch SW2 is opened to enable normal PLL operations.

Lock-up time of the selection of the appropriate frequency band, can be minimized by setting the feedback frequency to its maximum by adjusting the divider ratio N to the minimum. Especially, in combination with a maximized frequency of the reference signal, by adjusting the divider ratio of divider M to the minimum.

AFC includes separate PFD/CP architecture (no. 2)
The second architecture (see figure 3.2) uses two separate PLL loops, one for automatic frequency control and one for fine-tuning. This results in a higher complexity, because the PFD and CP are implemented twice. On the other hand, this results in less interaction with the sensitive loop filter voltage in the fine-tuning loop. Furthermore, the settling-time of the additional loop can be made much faster than the settling-time of the normal PLL.

The PFD in the automatic tuning loop generates up and down error signals and therefore, the CP generates an "UP" or "DOWN" current into the capacitor C. This affects the input voltage of the automatic frequency control system. In most cases, an additional comparator is needed to convert the capacitor voltage into digital signals for AFC system. For further explanation of the automatic frequency tuning is referred to the explanation of the first architecture.

Digital AFC architecture (no. 3)
The architecture given in figure 3.3 uses a digital frequency detector or frequency difference detector, instead of the PFD/CP combination in the second architecture. Therefore, the AFC system can be realized completely in the digital domain.

The concept of the digital frequency difference detector (FDD) is analogous to the PFD/CP combination, except that the FDD detects a difference in frequency rather than phase. The FDD also generates up/down error signals and the automatic frequency control system can use different algorithms (see section 4.3.2) to find the appropriate VCO frequency band. In the case of using an frequency detector, the detected frequency can be truncated into an up/down error signal, or the output of the frequency detector can directly be used to select the appropriate frequency band.

Also digital AFC systems can use an open-loop step, followed by a closed-loop step. In the open-loop step, the appropriate frequency band of the VCO is selected by the digital AFC system. After that, the PLL is returned into closed-loop operation and the PLL exactly tunes at the desired output frequency. The digital AFC system can use one of the four methods given in section 2.2.5. to set the PLL in an open-loop condition.

Digital AFC with automatic gain control (no. 4)
AFC systems that correct the VCO gain (K_{VCO}) as well as the VCO center frequency, have been reported by [12, 23]. After the first iteration of VCO center frequency calibration is completed, the VCO gain is calibrated. The VCO center frequency control word, N, is provided to a VCO gain detection/control block. This block can use a lookup table to determine the value K for the correct VCO gain curve. After the gain correction, the VCO center frequency calibration is repeated. (This architecture is not illustrated in a figure.)

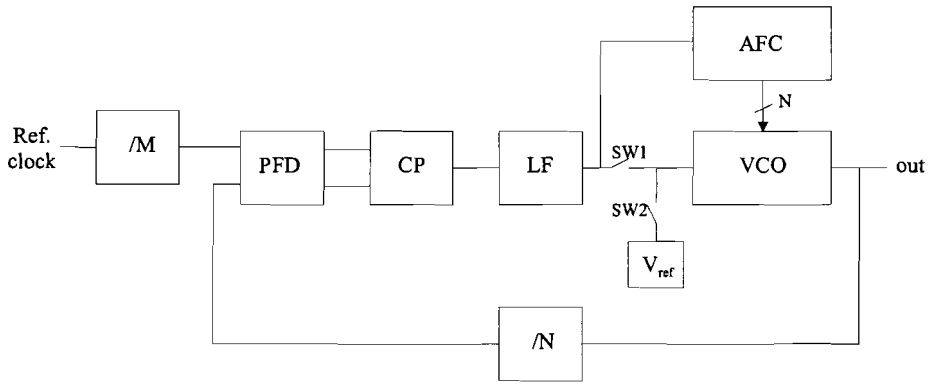

Figure 3.1: PLL with AFC that relies on V_{LF} [19]

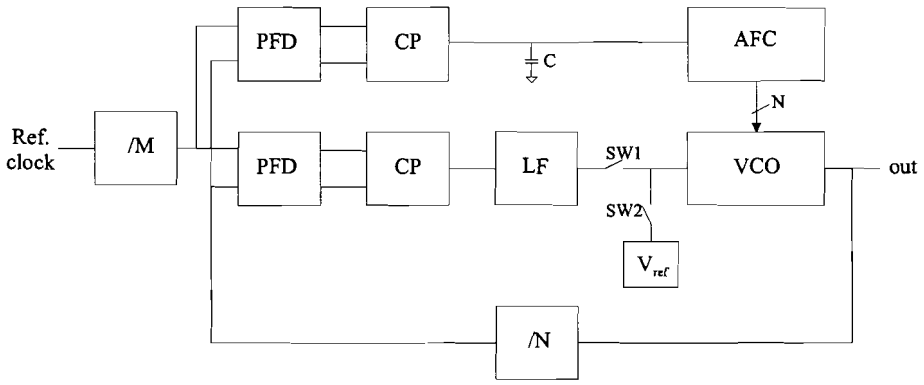

Figure 3.2: PLL with separate AFC loop [19]

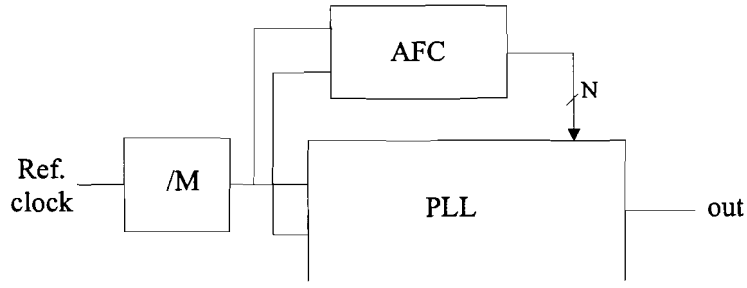

Figure 3.3: PLL with all digital AFC loop

3.3.2 Band search algorithms

A state machine can select a VCO center frequency with the discrete VCO tuning. This state machine may identify two VCO operation curves that have, for example, center frequencies just above and just below the desired frequency. One of these two must be selected for use during normal PLL operations.

Linear search algorithm
The state machine can perform a linear search algorithm in which the values of the center frequency control value are selected linearly, starting at one end of the range of possible values (e.g. 0) and proceeding to the other end of the range until the error signal provided by the FDD changes polarity.

Binary search algorithm
If the state machine is using a binary search algorithm each new value of N is selected midway between two previously selected values that yielded opposing error signal values [24]. The binary search stops when two consecutive values are detected that yield opposing error signals.

Linear interpolation search algorithm
Another method is a linear interpolation search algorithm. This algorithm estimates the frequency of the VCO and converts this into a certain change of the digital VCO codeword N. For example, in [15] this is done by referring to a conversion table.

Combination algorithm
A combination of the previous mentioned algorithms is also a possibility: e.g. the VCO has a discrete tuning input of 7 bits; linear interpolation principle is used to set the 4 MSBs and the 3 LSBs are set by using a 3 bit linear search algorithm.

Power-up measurement algorithm
The AFC algorithm can also rely on power-up measurement of the frequency coverage for each frequency band of the VCO and store these measurements into a lookup table. The lookup table is then used in normal operation to select and appropriate band of the VCO such that the PLL can lock on the desired frequency [17].

3.3.3 Example implementations

This section gives some information about example implementations of all digital AFC systems.

Frequency detection based on two counters
In [11] an automatic frequency control system based on two counters is introduced. The digital AFC centers the VCO frequency, thereby reducing the voltage swing needed from the analog control and increasing the pulling range of the VCO. This is an all digital AFC architecture. The AFC system

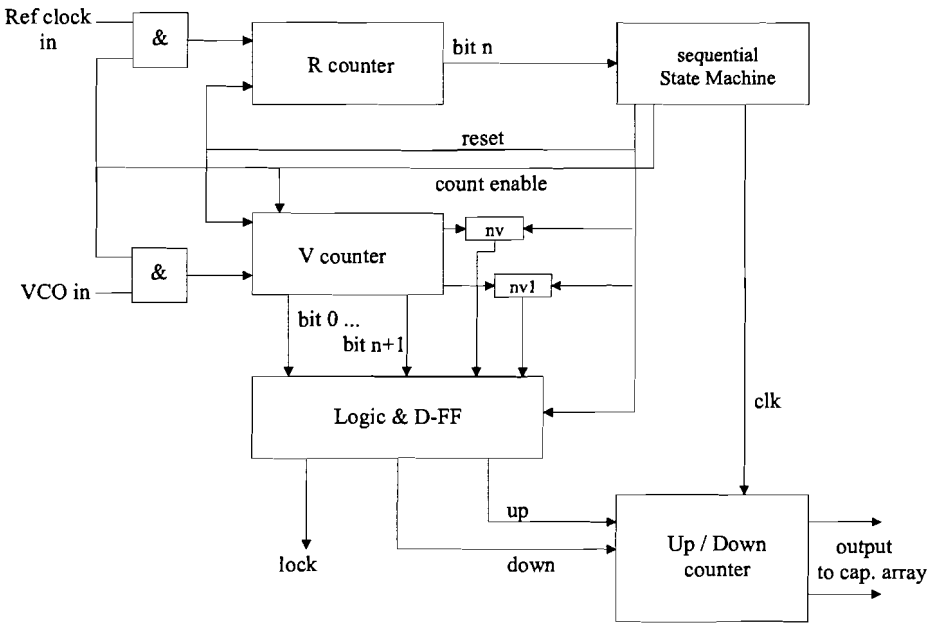

Figure 3.4: AFC system with two counter FDD [11]

generates a frequency difference indication, using a digital frequency difference detector (FDD), and uses this to increment or decrement the capacitance value of the VCO.

Figure 3.4 shows the digital FDD with two counters (R and V), reported in [11]. These two binary counters, with reset and enable, increment on every edge of the input and are used to count the cycles of the reference and VCO clocks. Counter R counts cycles of the reference clock and is a binary counter of n bits. Counter V counts cycles of the signal generated by the VCO and is at least n+1 bits long. Two one bit latches nv and nv1 are used to remember any overflows. When the R counter bit n is set, which means overflow of n-1 into bit n, the counting of R and V will be stopped.

The contents of the R and V counter is used to determine the relative frequency difference between the reference clock and the VCO. The relative frequency difference is used to set 3 latches, indicating whether the VCO is too fast, too slow or in the appropriate frequency band. The controlling state machine then generates a clock for an up/down counter. Each of the bits of this counter controls one of the MOS switches in the capacitor array in the VCO. The measurement is used to increment or decrement this counter to correct the center frequency of the VCO. The direction of the change for the counter is dependent on the relation between band number and center frequency of the VCO.

The calibration system in [10] also uses two counters that race side by side. If the counter R counts faster and finishes the race before the node V, the N-bit

control is incremented to speed up the VCO. The counter length determines the limited accuracy of the frequency comparison. The initial phase offset between R and V will have a minimal influence on the accuracy of the comparison, provided that the length of the counters is long enough. Once the node V wins the race, the N-bits are frozen for the normal operation of the PLL and the calibration circuit is disabled until the reset/calibrate signal is reactivated by power-up.

Frequency detection based on a digital logic quadricorrelator
In [27][1] a frequency calibration circuit that uses a digital logic quadricorrelator [9] is presented. Furthermore, it seems that the circuit makes use of method 4 (directly controlling the CP, see chapter 2) to set the PLL in an open-loop condition.

A frequency calibration circuit based a digital logic quadricorrelator (DLQ) determines the course tuning settings for the required channel. The direction of rotation of the in-phase and quadrature samples determines the polarity of the frequency difference. Initially, the PLL is disabled, the counter is reset and the counter is incremented or decremented with the quadricorrelator UP/DOWN outputs. A state machine determines convergence and freezes its state and re-enables the PLL for final phase-locking.

Digital center frequency and VCO tuning constant calibration
In [12] an automatic frequency control system is presented that also corrects the VCO tuning constant. The control circuit consists of a decoder and a state machine. It extracts the frequency and gain message from the output bits of the counter and generates a K bit signal to trim the VCO tuning constant. This system makes use of method 2, presented in chapter 2, to set the PLL into an open-loop state: Both up and down charge pump switches are opened and the switch between the reference voltage source and the VCO is closed in order to place a fixed reference voltage (e.g. mid-level) at the VCO control input.

After finding the appropriate frequency band and tuning constant, the digital auto-trimming circuit sets a *start level* on the VCO control input through a simple digital to analog converter, to achieve the desired frequency within a tolerance of 10%, which ensures a fast settling time of the closed-loop step. Then, the calibration circuit is de-activated and the PLL can operate in conventional mode.

[1] This article has been published in June 2003, after I had been working on the AFC systems using the DLQ.

3.3.4 Overview

Table 3.1 gives the results of the comparison of automatic frequency control systems presented in the references: First of all, the type of oscillator is given, together with the frequency range or operating frequency of the oscillator. Next, the architecture number (see section 3.3.1) is listed in the table as well as the method setting the PLL in open-loop condition, which were introduced in section 2.2.5. If no method number is given in the table, then the way of setting the PLL into an open-loop condition is not known. Finally, the division into two types of automatic frequency control systems is made.

Many published systems use switches in the analog part of the PLL to set the PLL in an open-loop condition and the VCO, for example, in the middle of each frequency band. Even in digital automatic frequency control systems. An all digital AFC system in combination with switches in the digital part of the PLL, which directly control the charge-pump to set the PLL in open-loop seems to be a promising solution.

As mentioned before, [27] uses an all digital AFC system, which controls the CP directly. This system is an calibration system, but it has similarities with the variable divider CFC system with digital quadricorrelator, that will be discussed in chapter 5.

Table 3.1: Comparison of references (CFC = Coarse Frequency Control, FSC = Frequency Spread Calibration)

Reference	Type of oscillator	Frequency [MHz]	Architecture no. / Method no.	Type of system
[10]	CCO, Ring	80-1000	3 / 1	FSC
[11]	VCO	1020-1270	3	CFC
[12]	Ring	1250-2850	4 / 2	CFC
[13]	LC	821-1000	2	FSC
[14]	Ring		1	CFC
[15]	LC	1910-2340	3 / 1	FSC
[16]	Ring	111-290	1 /1	CFC
[17]	LC	3330-4000	3	FSC
[18]	LC	760-980		CFC
[19]	VCO		1,2,3 / 1	
[20]	VCO		3 / 2	
[21]	Ring		1 / 1	
[22]	LC		1 / 1	
[23]	VCO		4 / 1	FSC
[24]	VCO		3 / 1	CFC
[26]	LC	158-232	3	FSC
[27]	LC	10000	3 / 4	FSC

3.4 All digital dual-loop topology

In the previous section, the state-of-the-art systems have been subdivided into four main architectures. The AFC system can use an open-loop step to select the proper frequency band, followed by the normal closed-loop operation of the PLL to achieve phase-lock at the desired frequency. The *all digital automatic frequency control system* is the most promising architecture, especially in combination with method 4, which directly controls the CP to set the PLL in open-loop condition, see section 2.2.5.

The generic dual-loop topology for all digital AFC systems is illustrated in figure 3.5. A digital frequency detector measures the frequency of the divided VCO signal. The frequency bands of the VCO can be selected by means of discrete tuning with a N bits digital signal. The two different *reference clocks*, in figure 3.5, make the system more flexible. Practical AFC systems might use the same reference frequency or, for example, use a frequency divider between the first and second reference clock. In addition, the AFC system selects the appropriate frequency band according to the desired frequency. The way of dealing with the desired frequency in digital AFC systems depends on the used architecture and will be explained in the next paragraph.

All digital automatic discrete frequency control systems can be classified into two types of architectures: in the first architecture, see figure 3.6(a), the output signal of the VCO is divided by a constant division ratio, whereas in the second architecture the division ratio is variable and depends on the desired frequency, see figure 3.6(b). In the constant divider architecture, the value of the discrete tuning outputs of the AFC system is directly dependent on the choice of $f_{desired}$. On the other hand, in the variable divider architecture, the division ratio is changed according to the desired frequency. Therefore, the frequency difference between the reference frequency (or a multiple of the reference frequency) and the frequency of the divided VCO signal is used to select the appropriate frequency band.

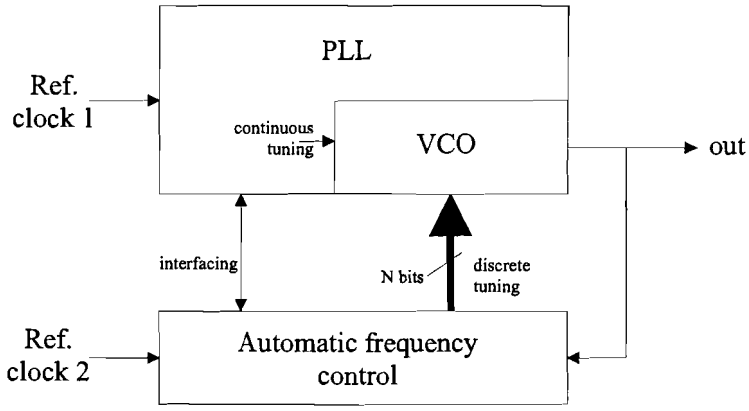

Figure 3.5: Dual-loop topology

Figure 3.7 gives a block diagram of the AFC system, which consists of four main parts: a time measurement block, a frequency counter (FC) or frequency difference detector (FDD), a band selector and a sequential state machine. In brief, this state machine controls all the actions in the AFC system and in particular it determents convergence of the frequency band selection algorithm. The time measurement block is used to set a certain measurement time (t_m), which defines the accuracy of the frequency measurement. The band selector selects the frequency band of the VCO. Furthermore, a FC or FDD detects pulses from the divided VCO signal, during a specified measurement period and gives the state-machine information about the measured frequency or frequency difference.

3.5 Frequency detection

In this report, the digital frequency counter (FC) is based on a VCO pulse counter and the digital frequency difference detector (FDD) can be based on either a pulse counter or a digital logic quadricorrelator. First of all, the principle of a frequency detector based on a counter will be discussed, followed by the explanation of the FDD based on the digital logic quadricorrelator.

The pulse counter can be used as frequency counter or, with some additional logic, as a frequency difference detector. In FDD operation, the counter result will be truncated into an up/down error signal instead of a counter value representing a measured frequency.

3.5.1 Frequency counter

The measured frequency, f_m, is directly related to the value V of the VCO pulse counter. The linear relationship between f_m and V also depends on the measurement time, t_m, and the division ratio N of the divider. This section gives the relationship between the measurement time and the detector accuracy, followed by the relationship between the detected pulses and the measured frequency. Finally, the frequency error will be discussed.

Measurement time
The AFC system needs a time indication to detect an absolute frequency with a certain accuracy. In other words, the minimum detectable frequency differences are directly related to the measurement time.

The time measurement block can, for example, be implemented with a counter, which counts a specified number of reference periods (R) from the reference clock. Although numerous other possibilities could be used to generate a measurement time indication for the frequency detector, an implementation with a counter is flexible, and for further discussion it is assumed that a reference counter is used.

A possible count cycle of the reference clock counter is illustrated in figure 3.8. The counter is enabled by the controlling state machine. During enable, it

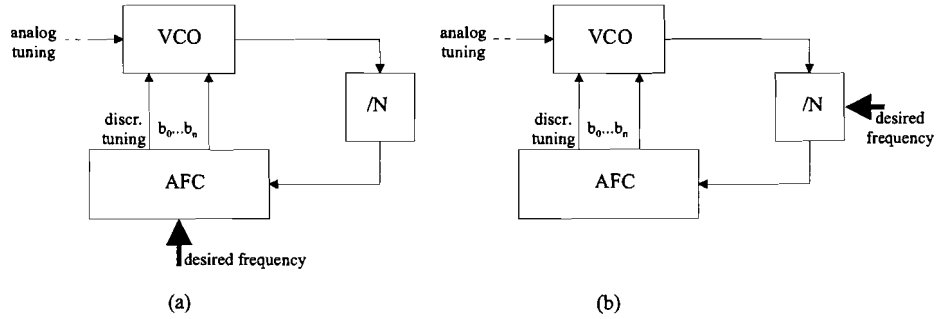

Figure 3.6: (a) Constant divider architecture, (b) Variable divider architecture.

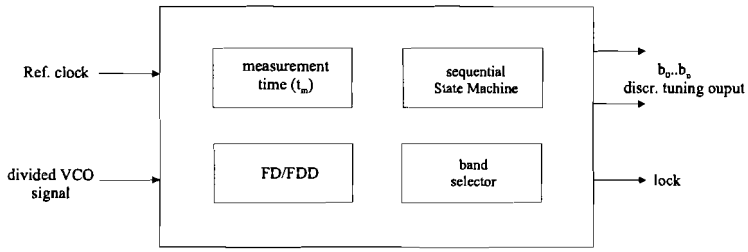

Figure 3.7: General block diagram of an AFC system

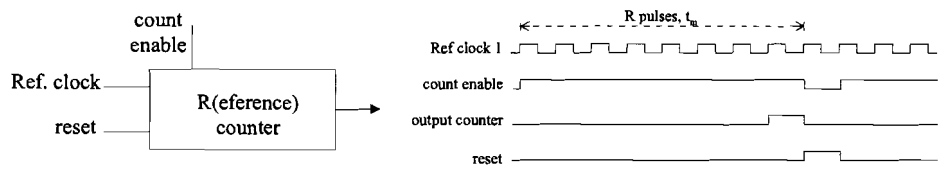

Figure 3.8: Realisation of the measurement time (t_m).

counts R pulses and then the output becomes active. Now, the counter is reset and the measurement cycle can start again.

In general, every value of R can be used to indicate the end of the measurement period. Thus, the reference clock generates R pulses during the measurement period and the measurement time t_m is given by

$$t_m = \frac{R}{f_{ref}} \tag{3.1}$$

where f_{ref} is the frequency of the reference clock. The number of bits necessary for the reference counter can be calculated with

$$n_r = \left\lceil \frac{\log R}{\log 2} \right\rceil \tag{3.2}$$

where $\lceil x \rceil$ denotes the ceil function, that is the smallest integer greater than or equal to x.

Detector accuracy

To calculate the detectable frequency difference, two cases will be considered: During the measurement period, the divided VCO signal generates n or $(n-1)$ pulses. The frequency of the divided VCO signal can be calculated for these two situations.

$$f_{vco1} = \frac{t_m}{n}^{-1} = n f_{ref} \tag{3.3}$$

$$f_{vco2} = \frac{t_m}{n-1}^{-1} = (n-1) f_{ref} \tag{3.4}$$

Subtraction of f_{vco2} from f_{vco1} gives the detectable frequency difference

$$\begin{aligned} \Delta f_{det} &= f_{vco2} - f_{vco1} \\ &= n f_{ref} - (n-1) f_{ref} = f_{ref} = \frac{1}{t_m} \end{aligned} \tag{3.5}$$

Whenever the detectable frequency difference is known, the minimum necessary measurement time $t_{m,min}$ can be calculated.

$$t_{m,min} = \frac{1}{\Delta f_{det}} \tag{3.6}$$

Example: An AFC system needs a frequency detector with a detectable frequency difference of $\Delta f_{det} = 1\text{MHz}$, then the minimum necessary measurement time will be $t_{m,min} = 1\mu s$.

Measured frequency and measurement speed

This part deals with the design of the digital frequency detector, in combination with the divider, which divides the VCO output signal.

Equation 3.5 shows that the frequency resolution of the frequency detector, Δf_{det}, is dependent on the measurement time t_m. In addition, the actual frequency resolution, F, of the frequency measurement of the output frequency of

the VCO depends on the Δf_{det} and the divider ratio N and can be expressed as

$$F = N\Delta f_{det} \tag{3.7}$$

The measured frequency, f_m, is depended on the actual counter value V, the measurement time t_m and the divider ratio N.

$$f_m = \frac{V}{t_m}N \tag{3.8}$$

A combination of (3.1) and (4.9) gives

$$f_m = \frac{VN}{R}f_{ref} \tag{3.9}$$

Furthermore, a combination of (3.5), (3.1) and (3.7) gives

$$\frac{N}{R} = \frac{F}{f_{ref}} \tag{3.10}$$

This equation shows that the measurement time (speed) is independent of the choice of reference frequency, but dependent on the divider ratio N in combination with the necessary accuracy F of the detector.

Example: Assume F = 25 MHz, and f_{ref} = 10MHz or f_{ref} = 100MHz.

$$f_{ref} = 10\text{MHz}, \frac{N}{R} = 2.5$$

$$f_{ref} = 100\text{MHz}, \frac{N}{R} = \frac{F}{f_{ref}} = \frac{1}{4}$$

Two different divider ratios will be chosen and together with the two reference frequencies, this results in four different cases. The results are given in table 3.2 and show that the measurement time is independent of the reference frequency, but dependent of the choice of the divider ratio N.

Table 3.2: Measurement time t_m and the number of reference periods R as function of divider ratio N and the reference frequency f_{ref}.

N	f_{ref} [MHz]	R	t_m [ns]
10	100	40	400
10	10	4	400
40	100	160	1600
40	10	16	1600

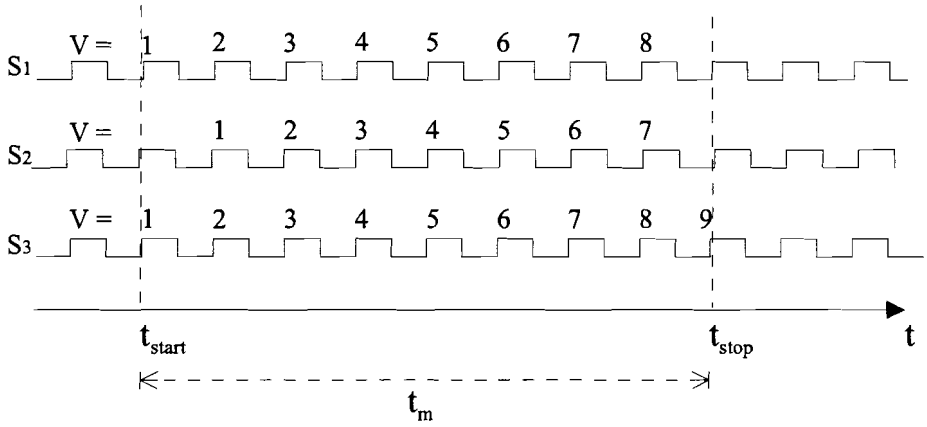

Figure 3.9: Square waves and V counter values.

Frequency error
While using a simple VCO pulse counter, two implementations in the frequency detector block are possible: the counter either *increments* or *does not increment* the counter value, when the input of the counter is active (HIGH) at the start of the measurement period. This depends on the exact implementation of the count enable of the counter. In the text throughout this report, the case that the counter *never increments* exactly at the start of the measurement period will be called *symmetric detection.* The case that the counter *increments*, when the counter input is active at the start of the measurement period, will be called *asymmetric detection.*

Symmetric detection
During the measurement period t_m, a counter counts pulses from the divided VCO signal. This counter makes a *count error* due to the occurring phase differences between the VCO signal and the reference clock (an example of this count error will be given in the next paragraph). Every counted pulse represents a frequency difference of Δf_{det}. Thus, the count error results in a frequency error in the measured frequency, called f_{err}.

An example of the count error, mentioned in the previous paragraph, is illustrated in figure 3.9. This figure shows three signals together with the counter values V. The counter starts counting at t_{start}, stops at t_{stop} and the measurement time is t_m. The frequency of the second signal, S_2, is slightly lower than the frequency of the first signal, S_1, and the frequency of the third signal, S_3 is slightly higher than the first signal. Furthermore, S_2 has a rising edge just before t_{start} and a rising edge just after t_{stop}. S_3 has a rising edge just after t_{start} and a rising edge just before t_{stop}. These three signals result in three different values for counter V. The first signal results in V=8, whereas S_2 results in V=7 and S_3 results in V=9.

In the limit case, the frequency difference between S_1, S_2 and S_3 goes to *zero.* Then, S_2 still has a rising edge just before t_{start} and one just after t_{stop} and the

counter will still produce V=7. But, a very small phase change in S_2 will cause S_2 to shift to the left or right, see figure 3.9, and this results in a counter value of V=8. A phase change for S_3 also results in V=8. Therefore the worst-case count error will be ± 1 count. Thus, the frequency error can be expressed as

$$-\Delta f_{det} \leq f_{err} \leq +\Delta f_{det} \tag{3.11}$$

Asymmetric detection

In the previous case, the pulse counter never increments the value of V exactly at at the start of the measurement period. In the case that the counter increments the value of V, when the input is HIGH, exactly at the start of the measurement period, see signal S_2 in figure 3.9. This will result in V=8 for signal S_2 in figure 3.9.

In the limit case, a signal with 6.5 pulses between t_{start} and t_{stop} can generate V=8. Also a signal with 8.5 pulses within the measurement period can generate V=8. Therefore the frequency error can now be expressed as

$$-1.5\Delta f_{det} \leq f_{err} \leq +0.5\Delta f_{det} \tag{3.12}$$

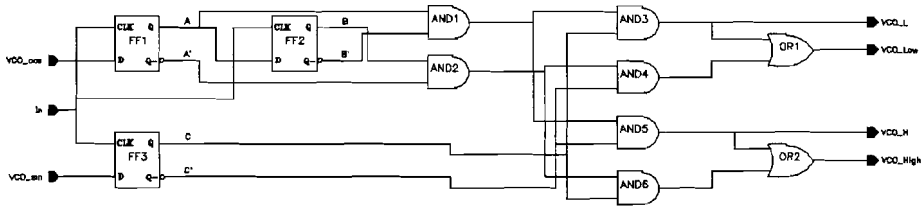

Figure 3.10: Schematic of the DLQ[9]

3.5.2 FDD based on digital logic quadicorrelator

Another way to implement a FDD is by means of a Digital Logic Quadricorrelator (DLQ). The configuration of DLQ1 is given in figure 3.10. This DLQ1 consists of three D flip-flops, four AND-gates and two OR-gates. The operation of this DLQ1 will be considered for three different cases [9]:

Case 1: when $\omega_{in} = \omega_{VCO}$
If the input frequency is equal to the VCO frequency, the outputs of FF1,2 are always "1" or "0". As the output of AND1,2 is always "0", the output of OR1,2 is always "0", regardless of the (C,C') ports' states. This FDD does not produce any spurious output when no frequency difference does exist.

Case 2: when $\omega_{in} < \omega_{VCO}$
If the input frequency is lower than the VCO frequency, (A, A') ports produce a square wave which has the frequency component of the input frequency error. (C, C') ports give a 90° delayed version of the (A, A'), AND1,2 deliver the rising and falling edge differentiation output respectively. AND5,6 produce the one clock width "1" pulses. The "1" pulses from OR2 (VCO-HIGH) mean the CO frequency is higher than the input frequency. The VCO-LOW port remains to be "0" states.

Case 3: when $\omega_{in} > \omega_{VCO}$
If the input frequency is higher than the VCO frequency, the VCO-LOW port delivers "1" pulses which mean the VCO frequency is lower than the input frequency. The VCO-HIGH port keeps silence.

Balanced digital logic quadricorrelator

The balanced digital logic quadricorrelator (DLQ2) works similar to the DLQ1 described above, but it consists of four flip-flops and requires some additional AND-gates, see appendix C. The frequency detector gain is doubled, but its linear discrimination range is reduced by half [9].

Simulation result

The simulation result, given in figure 3.11, shows the response of the DLQ1 outputs: VCO_high1 (normal output) and VCO_h1 (output of AND-gate number 5) and the outputs of DLQ2: VCO_high2. The input signals are a reference clock and a (divided) VCO signal. The frequency of the reference clock is f_{REF}=5MHz and the frequency of the VCO signal is f_{VCO}=5.35MHz.

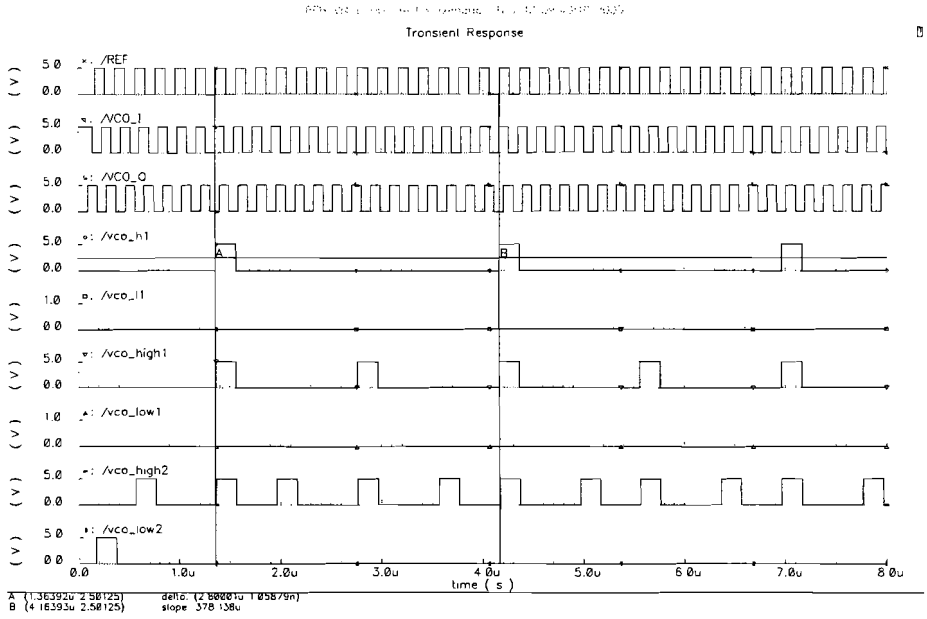

Figure 3.11: A simulation result of the DLQ1, with f_{REF}=5MHz and f_{VCO}=5.35MHz.

The DLQ1 produces pulses on the VCO_high1 and VCO_h1 output, indicating that the frequency of the VCO signal is higher than the frequency of the reference clock. Another conclusion can be drawn from the simulation result: the detector gain of the VCO_high1 output is twice as high as the detector gain offered by output VCO_h1. It must be noted that the output of the balanced DLQ2: VCO_high2 has twice the detector gain of the DLQ1.

The frequency difference between both input signals is 350kHz. In the case of one complete period difference between the two input signals, the minimum necessary detection time is: 2.857μs. The output VCO_h1 reacts on a difference of one period, but due to the discrete sampling character of the DLQ (with a sample frequency of f_{REF}), the minimum detection time is rounded off to a integer multiple of the reference clock period (200ns). Therefore, the time difference between the markers A and B is 2.8 μs.

The output VCO_high1 has twice the detector gain than VCO_h1. Therefore, the output VCO_high1 reacts on a half period difference between the two input signals. In this case: 1.428μs. The balanced DLQ2 reacts on one quarter period difference, which is 714ns in this case. Due to the discrete character, the output of the DLQ1 becomes active after 1.4μs or 1.6μs and the output of the balanced DLQ2 becomes active after 600ns or 800ns.

3.6 Summary

Automatic frequency control (AFC) systems can be divided into two types of systems: course frequency control (CFC) systems and frequency spread calibration (FSC) systems. In general, course frequency control is used in wide-band systems and frequency spread calibration is narrow-band systems. The main difference between course control and calibration is: in course control systems, the AFC selects an appropriate frequency band every time a new frequency is selected and in a calibration system the AFC selects the proper frequency band at start-up.

The frequency bands in FSC systems must at least cover the whole required frequency range and must be able to compensate for external variations during operation, whereas in CFC systems each frequency band can be smaller than the complete required frequency range, as long as the frequency bands together are able to cover the required frequency range, even under worst-case conditions. Furthermore, the overlap between two adjacent frequency bands can be small, as long as the bands are able to compensate for the quantization error of the AFC system.

The state-of-the-art systems are subdivided into four main architectures. Especially, the all digital AFC system is a promising option, therefore some important digital example implementations are given in this chapter. The band search algorithms reported in the literature are: linear, binary, interpolation as well as power-up measurement. Nearly all AFC architectures use an open-loop step to select the appropriate frequency band followed by a closed-loop step of the PLL to achieve phase-lock. Furthermore, most systems described in the literature rely on a reference voltage (e.g. mid-level) that is connected to the VCO tuning input during the band selection.

We think that the most promising solution is an *all digital* AFC system, which uses the charge-pump to set the PLL in open-loop condition (the VCO is then at the start of each frequency band), instead of interfering with the sensitive loop-filter voltage by connecting a reference voltage to the VCO. The next step is the subdivision of these dual-loop all-digital AFC systems into variable divider and constant divider architectures.

Two ways of digital frequency detection are discussed: A frequency counter and a frequency difference detector. A pulse counter can be used as frequency counter or as frequency difference detector, by truncating the counter value into an up/down error signal. The digital logic quadricorrelator (DLQ) can only be used as FDD. The necessary measurement time of the frequency counter is inversely dependent on the necessary detectable frequency difference ($t_m = \frac{1}{\Delta f_{det}}$) and the frequency error of this detector varies between $\pm\Delta f_{det}$. The measurement time of the normal DLQ to detect a frequency difference of Δf_{det} is $t_m = \frac{1}{2\Delta f_{det}}$ and in the case of a balanced DLQ: $t_m = \frac{1}{4\Delta f_{det}}$.
The DLQ is a FDD building block, which combines an attractive measurement time with minimized circuit complexity!

Chapter 4

Frequency band requirements

This chapter deals with generic frequency band requirements in combination with band selection criterions. First of all, an overview of detection scenarios will be given, followed by a section about band requirements and selection criteria for coarse frequency control (CFC) and a section for frequency spread calibration (FSC). Finally, a summary will be given. The definitions given in the next list are used in the remaining part of this Thesis.

Definitions

f_{ref}	Reference frequency of the digital system
f_{out}	Output frequency of the VCO
f_{lock}	Frequency to 'lock on' *desired output frequency*
f_m	Measured frequency
t_m	Measurement time
f_{err}	Frequency error of the detector
Δf_{det}	Frequency resolution of the digital frequency detector
F	Frequency resolution of the digital freq. detector after multiplication
F_s	Frequency spacing between two adjacent frequency bands
F_{ov}	Frequency overlap between two adjacent frequency bands
F_{span}	Frequency span of a frequency band
$F_{desired}$	Desired frequency range, which must be covered by a frequency band
U	Process spread margin

4.1 Overview of frequency band detection scenarios

This section gives an overview of all band detection scenarios described in this chapter. The overview is illustrated in figure 4.1. First of all, the division into CFC and FSC systems is made. In brief, in CFC systems the frequency overlap (F_{ov}) beween two adjacent frequency bands is the most important parameter, whereas in FSC the frequency spacing (F_s) between two adjacent frequency bands is more important.

After that, coarse frequency control systems are subdivided into two kinds of architectures: *constant divider ratio* and *variable divider ratio* architectures. Next, the difference between systems that set the frequency of the VCO "at the start of each frequency band" or "in the middle of each

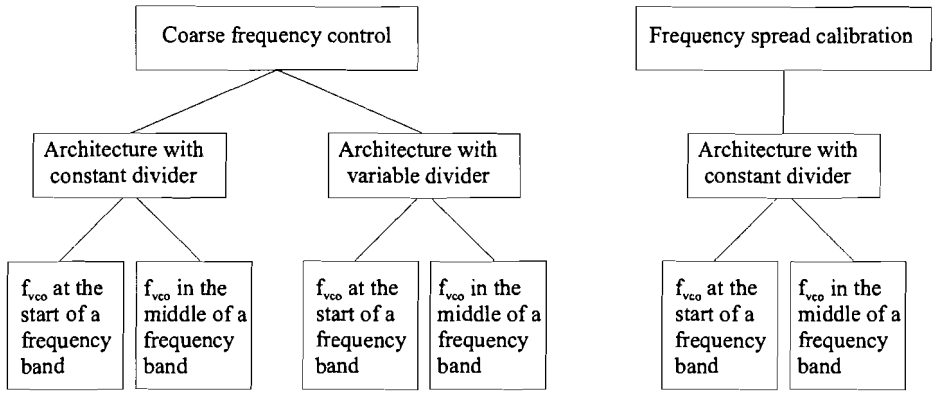

Figure 4.1: Overview of frequency band detection scenarios.

frequency band", during frequency band selection, is made. The principle of setting f_{vco} at the start of each frequency band is the same as setting f_{vco} at the end of each frequency band, therefore only f_{vco} at the start the frequency bands is discussed. With *in the middle* is meant: the VCO is set at the center frequency of the operating frequency band. In practice this may introduce some frequency error, but this is not further discussed in this report.

In general, in frequency spread calibration systems, the desired frequency band has a fixed frequency range and therefore only architectures with a constant divider ratio are considered. It must be noted that systems that use calibration at power-up in combination with a variable divider ratio could exist, for example in multi-band systems, but these systems are not further discussed.

4.2 Coarse frequency control

Figure 4.2 shows two overlapping frequency bands of a VCO. The begin, center and end of frequency band number 1 are indicated with f_{b1}, f_{c1} and f_{e1}. The begin, center and end of band number 2 are indicated with f_{b1}, f_{c1} and f_{e1}. The amount of band overlap is called X.

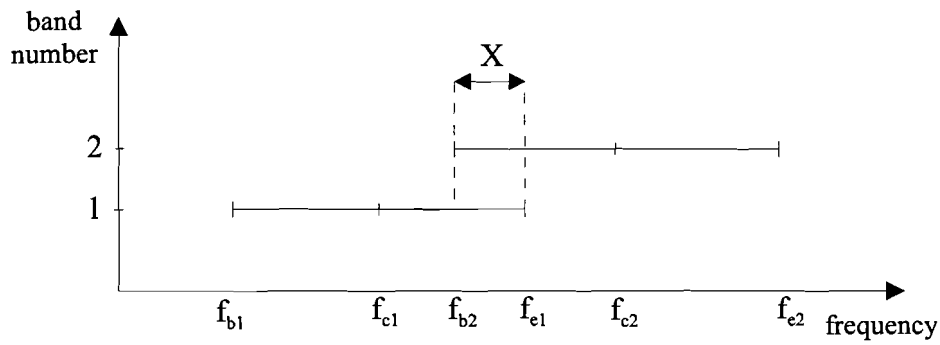

Figure 4.2: Two overlapping frequency bands a VCO.

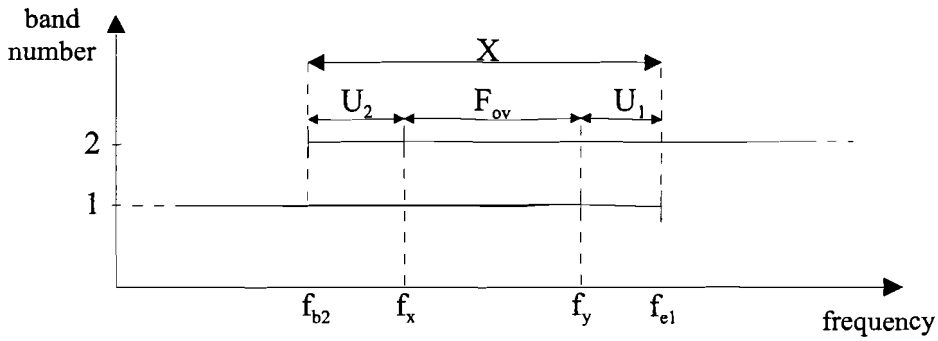

Figure 4.3: Frequency overlap between two adjacent frequency bands a VCO, the total overlap X consists of U_1, U_2 and F_{ov}.

The amount of band overlap changes due to external variations, like: temperature, supply voltage, aging and process spread. Therefore, the amount of band overlap X will be subdivided into U_1, U_2 and F_{ov}, which is illustrated in figure 4.3. U_1 and U_2 are the band margins of band 1 and 2, respectively. Furthermore, F_{ov} is the (worst-case) minimum frequency overlap between band 1 and 2. In other words, f_{b2} and f_{e1} change due to external variations, therefore U_1 and U_2 change, but F_{ov} is constant. In the worst case, f_{b2} goes to f_x and f_{e1} goes to f_y. Thus, U_1 and U_2 both go to *zero* and the amount of overlap band between is still F_{ov}.

The amount of band overlap, F_{ov}, between the frequencies f_x and f_y is the necessary margin needed for the AFC system to function properly. For further discussion the following assumption will be made: if the desired frequency is lower than f_x, band number one must be selected and if the desired frequency is higher than f_y, band number two. In the region between f_x and f_y both bands can be selected.

The question, which must be answered: What is the minimum band overlap (F_{ov}) that is needed for the discrete frequency control loop to select the proper frequency band. The answer is dependent on the detection scenario, therefore four scenarios will be described.

4.2.1 Two-band VCO example

This section gives a simple example of a VCO, which will be used illustrate the coarse tuning detection scenarios. This VCO has minimum complexity: only two frequency bands. Furthermore, the frequency bands of this VCO have similarities with band number 4 and 5 of the previous mentioned 4.5-7GHz VCO (see chapter 1).

Process spread causes the frequency bands, drawn in figure 4.2 and 4.3, to shift to lower or higher frequencies. In addition the values for F_{span} and F_{ov} change: if the bands shift down, to lower frequencies, the frequency ranges of the bands will be compressed and F_{span} and F_{ov} will decrease. In the same

Table 4.1: Two frequency bands of the VCO example

band number	Frequency [MHz] f_b	f_e	F_{span} [MHz] min.	nom.	max.
1	5725	5950	200	225	257
2	5900	6175	250	275	315

way, if the bands shift up, to higher frequencies, the ranges will be extended and F_{span} and F_{ov} will increase.

The nominal frequency range of frequency band number 1 is 5725 - 5950 MHz and of band number 2 is 5900 - 6175 MHz. The nominal band overlap between these two frequency bands is 50 MHz. The worst-case minimum frequency overlap between band number 1 and 2 is 35 MHz, which is caused only by frequency spread in the oscillator, other variations in external variables are not taken into account. The operating frequencies are summarized in table 4.1. In addition, the span of both frequency bands is given in this table.

4.2.2 Constant divider detection

Whenever an architecture with a constant division ratio is used, the frequency detector can only detect discrete frequencies with a frequency distance of $F = N\Delta f_{det}$. Figure 4.4 gives an example of these discrete frequencies, which are marked with 'x', together with two frequency bands.

Some discrete detectable frequency marks are named with a letter, e.g. 'b'. This letter corresponds to a certain value of the counter, which is used in the frequency detector circuit. It also corresponds to the measured frequency: e.g. detection of 'b' corresponds to a measured frequency of f_b.

This section describes two band detection scenarios, both using a constant division ratio and a symmetric frequency detector. The first is with "f_{vco} at the start of each frequency band" and the second with "f_{vco} in the middle of each frequency band".

f_{vco} is at the start of a frequency band

During the coarse frequency tuning, the output frequency of the VCO will be set at the start of each (selected) frequency band. Furthermore, the divider ratio will be constant. In that case, the minimum frequency band overlap between two adjacent frequency bands of a VCO is drawn in figure 4.4. The total band overlap X consists of: Two margins U_1 and U_2 and the frequency overlap, F_{ov}, which is necessary for the digital control loop to function properly. The frequency overlap F_{ov} must be larger than two times the frequency detector resolution F, which can be expressed as

$$F_{ov} \geq 2N\Delta f_{det} \tag{4.1}$$

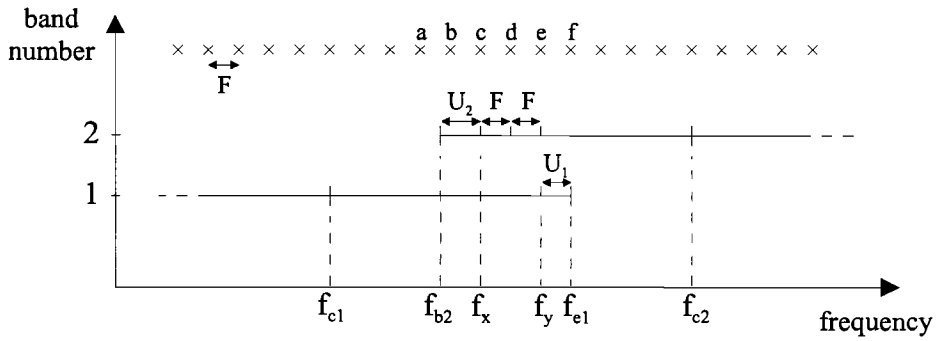

Figure 4.4: Two frequency bands and discrete detectable frequencies marks ('x') on equal frequency distances of F = $N\Delta f_{det}$.

The explanation for this minimum overlap is as follows: Assume $U_1 = 0$ and $U_2 = 0$, then the start frequency of band number 2 of the VCO is f_x. In addition, f_x lays exactly on f_c (this is not always the case, because the frequency bands, in figure 4.4, can shift to the left or right). Detection of f_x with a *symmetric* detector can result in a measured frequency of: f_b, f_c or f_d.

It must be noted that in the case of $U_2 = 0$ the frequency f_b, see figure 4.4, is not covered by band number 2 (this band starts at $f_x = f_c$). Furthermore, the frequencies higher than the measured frequency f_m plus the detector resolution F are always covered by band number 2. This leads to the following band selection criterion:

Band number 1 must be selected if $f_d \leq f_m + F$

Band number 2 must be selected if $f_d \geq f_m + F$

Now assume that detection of the start-frequency of band number 2 results in a measured frequency of f_d. In that case, band number 1 must be able to cover all frequencies less than $f_d + F = f_e$. Therefore the minimum value for F_{ov} will be $2F$. The minimum band overlap is: $X = U_1 + U_2 + 2N\Delta f_{det}$.

Example: The previous mentioned two-band VCO in combination with a constant division ratio of N=100 will be used: The minimum band overlap is 35 MHz. Therefore, the detector resolution F=17.5 MHz. The division ratio sets the maximum Δf_{det} = 175kHz and the minimum necessary measurement time $t_m = 5.7\mu$s.

f_{vco} is in the middle of a frequency band

Now the output frequency of the VCO is in the middle of the frequency band, e.g. mid-range, during coarse frequency tuning. In this case, figure 4.5 illustrates the overlap of two frequency bands. In the case that band number 1 is selected, the frequency f_{c1} will be generated and in the case of band 2,

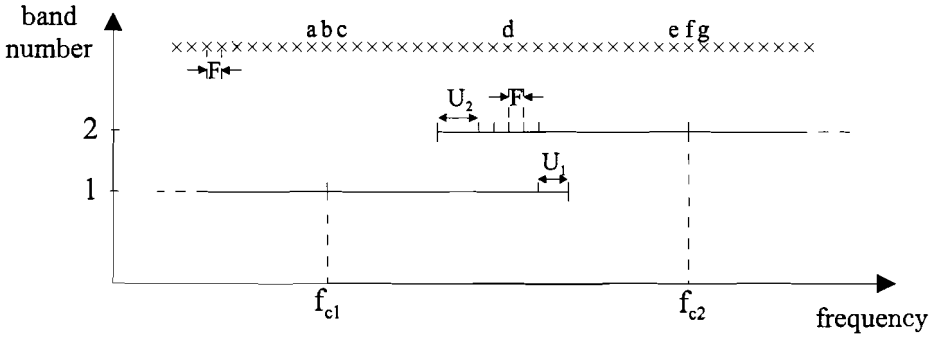

Figure 4.5: Two overlapping frequency bands and the discrete detectable frequencies.

f_{c2}. The *symmetric* frequency detector can detect point 'a', 'b' or 'c' when band 1 is selected and point 'e', 'f' or 'g' when band 2 is selected. A problem arises if the desired frequency is f_d: Which band should now be selected?

Selecting the proper frequency band for the desired frequencies around f_d can only be done properly if the span of the frequency bands is known. The span of each frequency band can be stored in, for example, a lookup table, but these values are dependent on process, voltage and temperature variables. Therefore, the worst-case smallest frequency span must be stored. The frequency span margins U_1 and U_2 (which represent the difference between the normal span and the worst-case smallest span) are also illustrated in figure 4.5.
If f_{c1} is generated by the VCO, the measured frequency can be f_a, f_b or f_c. In the case of generation of f_{c2}: f_e, f_f or f_g. Both measured frequencies can have an absolute measurement error of $2N\Delta f_{det}$, therefore the minimum band overlap can be expressed as $F_{ov} = 4N\Delta f_{det}$.

The necessary band overlap between band 1 and 2 is: $U_1 + U_2 + 4N\Delta f_{det}$. This results in a larger necessary band overlap than in the previous mentioned case, where the output frequency of the VCO is at the start of each frequency band during coarse tuning. If the band overlap is kept the same for both cases, than the frequency detector of must be more accurate, than in the previous mentioned case. This means that the measurement time becomes longer and this will be illustrated with the next example.

Example: The two-band VCO and a constant division ratio N=100 will be used in combination with the output frequency of the VCO in the middle of the frequency band during coarse tuning. The center frequency of band number 1 is 5837.5MHz and of band number 2 is 6037.5MHz. Furthermore, the nominal span of band 1 is 225MHz and of band 2 is 275MHz.
The minimum frequency span of band number 1 is 200 MHz and of band number 2 is 250 MHz. The frequency overlap F_{ov} can now be calculated and is 25MHz. Followed by $F = F_{ov}/4 = 6.25$MHz. Finally, $\Delta f_{det} = 62.5$kHz and the necessary measurement time $t_m = 16$us.

4.2.3 Variable divider detection

This section describes two band detection scenarios, both using a variable division ratio and a symmetric frequency detector. The first is with "f_{vco} at the start of each frequency band" and the second with "f_{vco} in the middle of each frequency band".

f_{vco} is at the start of a frequency band

The minimum frequency overlap F_{ov} is situated between two frequencies f_x and f_y, which are on a distance U_2 and U_1 from f_{b2} and f_{e1}, respectively (see figure 4.3). Assume $U_1 = U_2 = U$, then f_x and f_y can be expressed as

$$\begin{aligned} f_x &= f_{b2} + U \\ f_y &= f_{b2} + X - U \end{aligned} \tag{4.2}$$

Due to the divider with the variable divider ratio, the output frequency will be divided with different divider ratios. So, if frequency f_x or f_y is selected, this divider ratio has value N_x or N_y, respectively. N_x and N_y can be calculated with

$$N_x = \frac{f_x}{f_{ref}}, \qquad N_y = \frac{f_y}{f_{ref}} \tag{4.3}$$

During the digital selection of the desired frequency band the output frequency of the VCO is at the start of the frequency range: The VCO generates f_{b2}. In the case that the selected frequency is f_x, the selected division ratio is N_x. The output frequency of the divider will be called f_x'. In other words, band number 2 is selected and therefore the VCO generates f_{b2}. Furthermore, the division ratio is N_x, which 'points' to f_x and the output frequency of the divider is f_x'

$$f_x{}' = \frac{f_{b2}}{N_x} = \frac{f_{b2}}{f_x} f_{ref} \tag{4.4}$$

The division results in a projection of f_x around the reference frequency, and this projection is called f_x'. The projection of f_y is called f_y' and can be expressed similarly.

$$f_y{}' = \frac{f_{b2}}{f_y} f_{ref} \tag{4.5}$$

The frequency difference between f_x' and f_y' is called $\Delta f_{xy}{}'$ and can be calculated in the following way

$$\begin{aligned} \Delta f_{xy}{}' &= \left| \frac{f_{b2}}{f_x} - \frac{f_{b2}}{f_y} \right| f_{ref} \\ &= \left| \frac{f_y - f_x}{f_x f_y} \right| f_{b2} f_{ref} \\ &= \frac{X - 2U}{f_{b2}^2 + X f_{b2} + UX - U^2} f_{b2} f_{ref} \end{aligned} \tag{4.6}$$

Assume $U = 0$, then equation 4.7 becomes

$$\Delta f_{xy}{}' = \frac{X f_{ref}}{f_{b2} + X} \tag{4.7}$$

Obviously the frequency difference between f_x and f_y after division (with a variable division ratio) will be larger if X becomes larger. It also becomes larger if the reference frequency will becomes larger, because the division ratio will then be less. Furthermore, $\Delta f_{xy}{}'$ will also become larger if the start frequency will be lower, also caused by the fact that the division ratio will be less.

The frequency distance $\Delta f_{xy}{}'$ is the minimum frequency overlap, after division, that is needed for the digital coarse tuning loop to function properly. In general $\Delta f_{xy}{}'$ is a band dependent variable and will be called $\Delta f_{xy}{}'(x)$, where x is the band number. Furthermore, in equation 4.7, $f_{b2} + X$ is the same frequency as f_{e1}, which is the end frequency of the previous frequency band, $f_{e(x-1)}$. Thus, $\Delta f_{xy}{}'(x)$ can be expressed as

$$\Delta f_{xy}{}'(x) = \frac{X_x f_{ref}}{f_{e(x-1)}} = \frac{X_x}{N_{e(x-1)}} \tag{4.8}$$

where X_x is the band overlap between band number x and the previous frequency band, $f_{e(x-1)}$ is the end of the previous frequency band (band number x-1) and $N_{e(x-1)}$ is the division ratio, which selects $f_{e(x-1)}$.

Now the measurement frequencies will be calculated. The maximum accuracy of the discrete detectable frequency differences is Δf_{det}. This results in detectable frequencies ($f_m{}'$) around the reference frequency.

$$f_m{}'(n) = f_{ref} + n\Delta f_{det} \qquad n = \ldots, -2, -1, 0, 1, 2, \ldots \tag{4.9}$$

These frequencies ($f_m{}'$) are multiplied with a variable division ratio and this results in measurable frequencies, f_m in the normal frequency range of the VCO, which depend on the selected frequency band. For example frequency band number 2 is selected and then f_m will be

$$f_m(n) = \frac{f_{ref} f_{b2}}{f'_m(n)} \tag{4.10}$$

The measurable frequencies exhibits a very nice property, $f_m(0)$ will always lay exactly on the start frequency of the selected frequency band.

Figure 4.6 illustrates two overlapping frequency bands of a VCO together with the discrete measurable frequencies, which are dependent on the selected frequency band (the U margins are not drawn). The detectable frequencies that are drawn near frequency band number 1, give information about the frequencies in comparison with f_{b1} and the marks near frequency band number 2 in comparison with f_{b2}.

The detector works as following: Assume f_c is selected by the divider and band number 2 of the VCO is selected. Thus f_{b2} will be generated by the VCO and this will be divided by a divider ratio of N_c. In that case, the output frequency of the divider will be lower than the reference frequency and f'_c will be detected, which corresponds to a measured frequency of f_c. That means that detected frequencies lower than the reference frequency result in

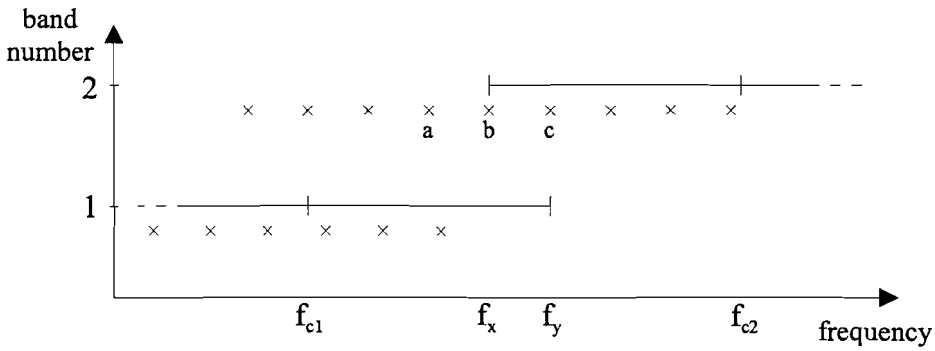

Figure 4.6: Two overlapping frequency bands a VCO, together with discrete, band dependent, detectable frequencies centered around the start of each frequency band.

measured frequencies higher than f_{b2}. Furthermore, frequencies higher than the reference frequency indicate that a lower frequency than f_{b2} is selected.

Assume $U_2 = 0$, a *symmetric* detector will be used, and the output frequency of the VCO is f_{b2}. Depending on the selected division ratio, a marked point below frequency band 2 will be detected, see figure 4.6. Divider ratios, which select frequencies between f_a and f_b, can result in a measured frequency of f_a or f_b. Furthermore, divider ratios, which select frequencies between f_b and f_c, can result in a measured frequency of f_b or f_c.

Desired frequencies lower than f_b are not covered by band number 2, thus band number 1 should be selected. But, frequencies lower than f_b can result in a measured frequency of f_b. Therefore the following criterion will be used to select the right frequency band.

Band number 1 must be selected if $f_{desired} \leq f_b$

Band number 2 must be selected if $f_{desired} \geq f_c$

The frequencies between f_b and f_c must be covered by both frequency bands, therefore the minimum frequency band overlap, F_{ov}, must be greater than the frequency distance between f_b and f_c and can be expressed as.

$$F_{ov(x)} \geq N_{e(x-1)} \Delta f_{det} \tag{4.11}$$

Where $N_{e(x-1)}$ is the division ratio, which selects $f_{e(x-1)}$, the end of the previous frequency band (band number x-1).

The total band overlap for a symmetric and an asymmetric detector will be given by

- Symmetric detector: The minimum band overlap is $U_1 + U_2 + N_{e(x-1)}\Delta f_{det}$.
- Asymmetric detector: The measurement fault is distributed asymmetrically around the selected frequency. Therefore the minimum band overlap is $U_1 + U_2 + 1.5N_{e(x-1)}\Delta f_{det}$.

In figure 4.7 linear search algorithm for the variable divider coarse frequency control architecture is introduced. $f_{d(esired)}$ is the desired frequency and divider ratio N_d selects this frequency. f_L is a discrete lock frequency, which is band dependant. For example, f_L lays exactly on f_c in band number 2 in figure 4.6. It must be noted that the desired frequency f_d is different from the measured frequency f_m: if f_d is lower than f_L the measured frequency will be higher than f_L. In the case that f_d is higher than f_L the measured frequency will be lower than f_L.

The frequency band search algorithm, given in figure 4.7, ensures lock in the appropriate frequency band, as long as the minimum frequency band overlap criterion is met. The following example shows a calculation of the maximum frequency accuracy of the frequency detector, together with the minimum necessary measurement time.

Example: The two-band VCO example has a minimum frequency overlap of 35MHz between frequency band number 1 and 2. Assume that the divider ratio to select f_{e1} will be $N = 100$. Furthermore, a symmetric detector will be used. Then the $\Delta f_{det} = 350$kHz and the minimum measurement time is $t_m = 2.85\mu$s.

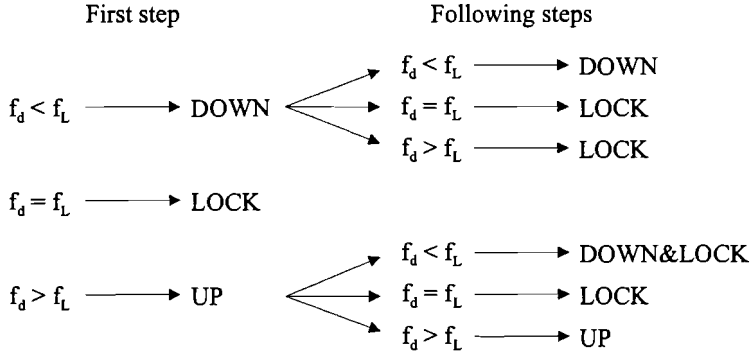

Figure 4.7: Frequency band selection: Linear search algorithm for the variable divider system as function of the lock frequency f_L and the desired frequency $f_{d(esired)}$.

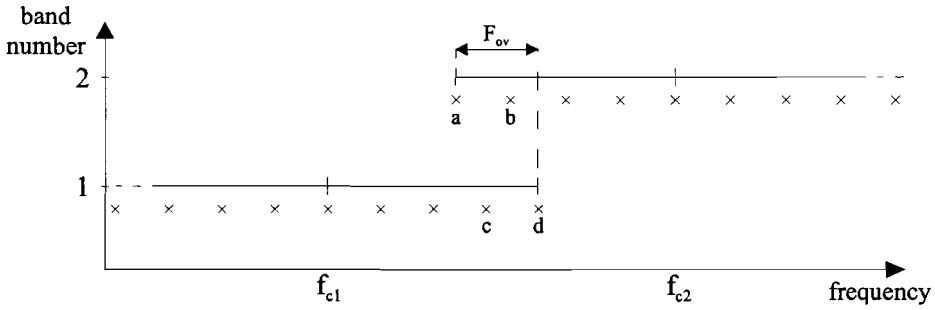

Figure 4.8: Two overlapping frequency bands a VCO, together with discrete, band dependent, detectable frequencies centered around the mid-range frequency of each frequency band.

f_{vco} is in the middle of a frequency band

What was shown in formula 4.9 and 4.10, works similar for the case that the f_{vco} is in the middle of the frequency band. But, now the discrete detectable frequencies are centered around the mid-range output frequency of the frequency bands. Figure 4.8 gives the minimum necessary band overlap in the case that four discrete detection frequencies f_a, f_b, f_c and f_d in the necessary band overlap (F_{ov}). (3 Frequencies are really necessary, e.g. f_a, f_b and f_c)

Assume $U_2 = 0$, a *symmetric* detector will be used, and the output frequency of the VCO is f_{c2}. Depending on the selected division ratio, a marked point below frequency band 2 will be detected, see figure 4.8. Divider ratios, which select frequencies between f_a and f_b, can result in a measured frequency of f_a or f_b. Furthermore, divider ratios, which select frequencies between f_c and f_d, can result in a measured frequency of f_c or f_d.
Desired frequencies lower than $f_a = f_{b2}$ and higher than $f_d = f_{e1}$ are not covered by band number 2 and band number 1, respectively. But, frequencies lower than f_a can result in a measured frequency of f_a, or frequency higher than f_d can result in a measured frequency of f_d. Therefore the following criterion will be used to select the right frequency band.

> Band number 1 is selected during the measurement:
> If $f_{desired} \geq f_d$ then band number 2 must be selected, otherwise band number 1.
>
> Band number 2 is selected during the measurement:
> If $f_{desired} \leq f_a$ then band number 1 must be selected, otherwise band number 2.

The frequencies between f_a, f_b and f_c must be covered by both frequency bands, therefore the minimum frequency band overlap, F_{ov}, must be greater than the frequency distance between f_a and f_b and can be expressed as

$$F_{ov(x)} \geq N_{e(x-1)} \Delta f_{det} \tag{4.12}$$

Which is the minimum necessary band overlap in the case that a *symmetric* detector will be used. Furthermore, x is the band number.

The total band overlap between two adjacent frequency bands will become now: $U_1 + U_2 + N_{e(x-1)}\Delta f_{det}$.

Example: The two-band VCO will be used in combination with the output frequency of the VCO in the middle of the frequency band during coarse tuning. The center frequency of band number 1 is 5837.5MHz and of band number 2 is 6037.5MHz. Furthermore, the nominal span of band 1 is 225MHz and of band 2 is 275MHz.
The minimum frequency span of band number 1 is 200 MHz and of band number 2 is 250 MHz. The minimum frequency overlap F_{ov} can now be calculated and is 25MHz. Assume that the divider ratio will be N=100. Then, Δf_{det} = 250kHz and the necessary measurement time $t_m = 4\mu$s.

4.2.4 Comparison between coarse control scenarios

Table 4.2 shows the results of the examples given for the mentioned band detection scenarios for coarse frequency control. The first conclusion that can be drawn is: for coarse frequency control "f_{vco} at the start of the frequency band" is the preferred method, especially in the case of small frequency band overlap between adjacent frequency bands.
The second conclusion that can be drawn from the results of the examples is that variable divider ratio systems have a faster settling time than constant divider ratio systems. *The second conclusion is only valid if the divider ratio of both systems is in the same order.* In practical systems, the limited accuracy of the variable divider ratio (for example integer values) of the variable divider sets a divider ratio range which is much higher than the divider ratio which can be used in the constant divider architecture.

The final conclusion is: The constant divider ratio system can be made much faster than the variable one, by decreasing the used divider ratio. But, in the case that the divider ratio of both systems is in the same order, the variable divider system is faster.

Table 4.2: Comparison of coarse control band detection scenarios, for N=100 and symmetric detector

Divider ratio	f_{vco}	Δf_{det} [kHz]	t_m [μs]
Constant	start	175	5.7
	middle	62.5	16
Variable	start	350	2.85
	middle	250	4

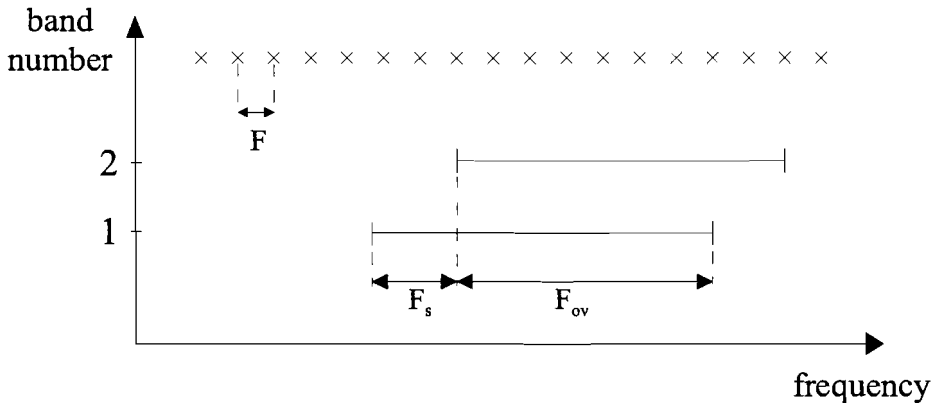

Figure 4.9: Two frequency bands of an oscillator with (discrete) detectable frequencies, marked with 'x'.

4.3 Frequency spread calibration

This section deals with some general definitions for discrete frequency calibration, like band overlap and band spacing.

Figure 4.9 shows two frequency bands of a band-switched oscillator in combination with the discrete detectable frequencies of a digital frequency detector. The distance F between two detectable frequencies is defined by $N\Delta f_{det}$. The frequency spacing between two adjacent frequency bands is called F_s and the overlap F_{ov}. Furthermore the frequency span of a frequency band, F_{span} is defined by $F_s + F_{ov}$.

Process spread causes the frequency bands, drawn in figure 4.9, to shift to lower or higher frequencies. In addition, the values for F_s and F_{span} change: if the bands shift down, to lower frequencies, the frequency ranges of the bands will be compressed and F_s and F_{span} will decrease. In the same way, if the bands shift up, to higher frequencies, the ranges will be extended and F_s and F_{span} will increase.

It must be noted that for proper behavior of the digital calibration system, the frequency overlap between the frequency bands must at least cover the desired frequency range ($F_{desired}$), see figure 4.11. Otherwise certain values of process spread result in two frequency bands that cannot cover the desired frequency range.

4.3.1 f_{vco} is at the start of a frequency band

This section describes two lock methods, the first lock method sets an upper boundary for F_s and therefore, the algorithm and lock method is band dependent. The second method does not set an upper boundary for F_s and has no band dependance and therefore it is the preferred method.

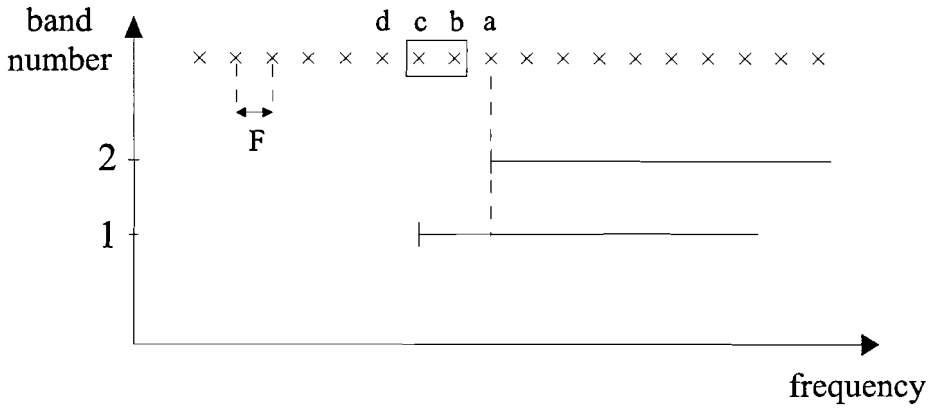

Figure 4.10: Two frequency bands of an oscillator and a lock range between marked points 'b' and 'c'.

Lock method with upper boundary for F_s

Figure 4.10 shows an example, where the desired frequency range starts at f_a (the detectable frequency marked with 'a') and a lock range is defined between f_b and f_c. Different actions will be taken according to the measured frequency, while the output frequency of the VCO is at the start of the frequency band.

Detection of f_a results in DOWN and LOCK

If f_m is between f_c and f_d that results in LOCK

Detection of f_d results in DOWN and LOCK

One of the advantages of this lock method is: the above mentioned actions can easily be translated into a simple logical function as function of the counter value V. Furthermore, in the case of equally spaced frequency bands with equal frequency span, the center frequency of the frequency bands is also calibrated.

The boundaries for F_s and F_{span} will be derived as following: Assume that the symmetric detector will be used and the measurement error is $\pm N\Delta f_{det}$. If the start of frequency band 1 is slightly lower than f_c, point 'd' can be detected and this results in an UP and LOCK action. So, band 2 can be selected and this band must cover the desired frequency range. Therefore the upper boundary for the frequency band spacing between band 1 and 2, F_s, is given by

$$F_s \leq 2N\Delta f_{det} \tag{4.13}$$

If the start of frequency band 1 is slightly higher than f_d, point 'c' can be detected, which results in a lock. Therefore the frequency span that band 1 must cover is

$$F_{span} \geq 3N\Delta f_{det} + F_{desired} \tag{4.14}$$

In addition, if the start of frequency band 2 is slightly higher than f_b, point 'a' can be detected and this results in a DOWN and LOCK action. Thus, band

1 must cover the desired frequency range. Therefore a second requirement for the frequency span of the frequency bands is drawn up

$$F_{span} \geq N\Delta f_{det} + F_s + F_{desired} \tag{4.15}$$

Which is always true if F_s satisfies the given boundary in equation F.1 and F_{span} satisfies equation F.2.

In practice, the frequency bands of a VCO are not spaced equally and therefore four similar lock methods are introduced in the appendix. These methods have a larger lock range and therefore a higher upper boundary for F_s. The upper boundary for F_s is a restriction for the VCO frequency bands. Therefore the band dependance must be programmed in the band selection function, which is a drawback for the system that uses these lock methods.

Lock method without upper boundary for F_s

The upper boundary for F_s of the previous mentioned method is caused by the "UP and LOCK" action if f_d is detected. Now a slightly different definition of the lock frequency will be used. This is illustrated in figure 4.11. The desired frequency range ($F_{desired}$) is situated between f_x and f_y. The margins U_1 and U_2 are the necessary margins to cope with external variations. Furthermore, the lock frequency f_L, which will be used in the algorithm, is drawn on a distance f_{err} from the left side of U_1. f_{err} is the measurement error of the detector, which is dependent on the measurement time. This definition sets a new minimum frequency span requirement, which is given by

$$F_{span} \geq U_1 + U_2 + F_{desired} + f_{err} + F_s \tag{4.16}$$

Under condition that

$$F_{err} \leq \frac{F_s}{2} \tag{4.17}$$

The band selection algorithm, illustrated in figure 4.12, works as follows: if the first measured frequency is less than f_L than the frequency band number must be increased. After that, the decision scheme will be changed to guarantee convergence of the band lock procedure. In the case that the first measured frequency is higher than f_L then the decision scheme will be different, see 4.12. It must be noted that only the lower frequency band can be selected in case of detection of two alternating measurements.

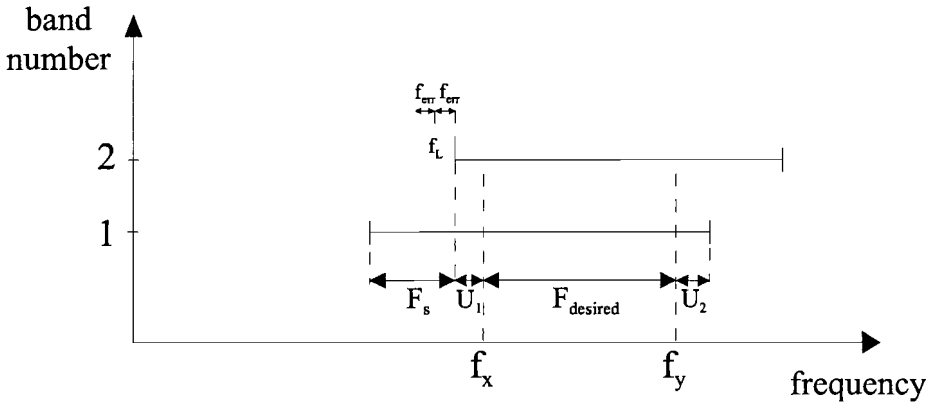

Figure 4.11: Two frequency bands with definition of the discrete lock frequency, f_L

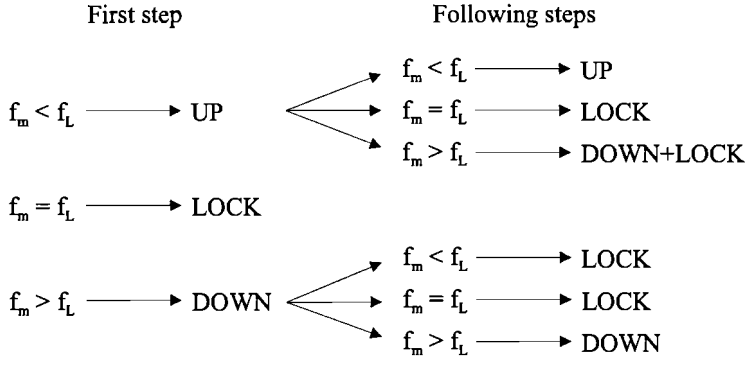

Figure 4.12: Frequency band selection: linear search algorithm for calibration systems as function of f_L and f_m.

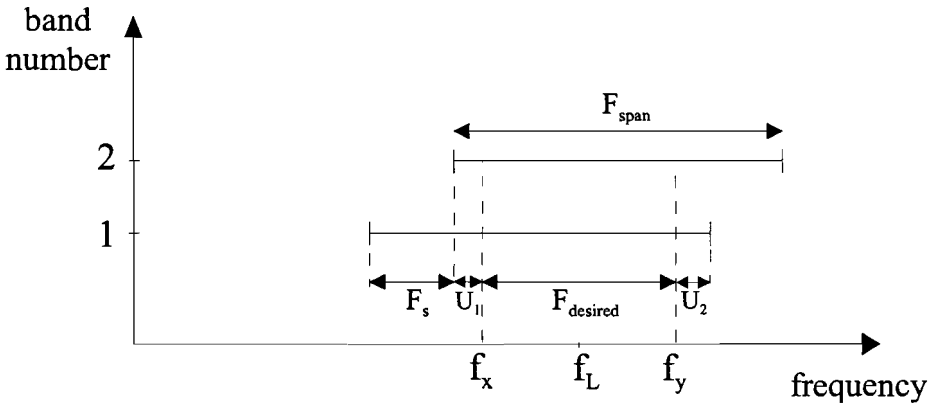

Figure 4.13: Two frequency bands with definition of the lock frequency f_L in the middle of the frequency bands.

4.3.2 f_{vco} is in the middle of a frequency band

In the case that f_{vco} is in the middle of a frequency band, the lock frequency, f_L will be defined differently from the previous case. f_L is now positioned exactly in the middle of the desired frequency span, this is illustrated in figure 4.13. A new frequency span requirement can be drawn up.

$$F_{span} \geq U_1 + U_2 + F_{desired} + 2F_s \tag{4.18}$$

It must be noted that both frequency bands can be selected at the detection of two alternating measurements.

An advantage of this method in comparison to the before mentioned method, is that the center frequency of the frequency bands is also calibrated.

4.3.3 Comparison between scenarios

The main difference between "f_{vco} is at the start of a frequency band" and "f_{vco} is in the middle of a frequency band" is center frequency calibration. In the case that f_{vco} is in the middle of a frequency band, the center frequency of the selected frequency is automatically the closest to the desired center frequency of the required frequency range. In the case that f_{vco} is at the start of the frequency band, the only requirement that can be fulfilled is selection of the frequency band that covers the required frequency band (under condition that the selected frequency band fulfills the requirement given in equation 4.16).

4.4 Summary

In this chapter, generic frequency band requirements and selection criterions were introduced for coarse frequency control (CFC) and frequency spread calibration (FSC) systems. The coarse control systems are further subdivided into constant divider and variable divider architectures. In the case of frequency spread calibration systems, one fixed required frequency range is considered, resulting in a constant divider architecture.

For the above mentioned cases, two different detection scenarios are considered: "f_{vco} is at the start of a frequency band" and "f_{vco} is in the middle of a frequency band". The resulting band selection criteria and frequency band requirements can be found throughout this chapter, but the most important conclusions are briefly summarized (see also table 4.3):

In CFC systems, especially with small frequency overlap between two adjacent frequency bands, "f_{vco} is at the start of a frequency band" is the preferred method.

In CFC systems, the "f_{vco} is in the middle of a frequency band" detection method needs (additional) information about the span of the frequency bands to select the proper frequency band.

In CFC systems, a small and constant divider ratio results in the fastest settling time.

In the case that the divider ratio of the constant and variable divider architecture is in the same order, the variable divider ratio system needs the smallest measurement time.

In CFC systems, a variable divider architecture results in minimum complexity.

In FSC systems, "f_{vco} is in the middle of a frequency band" results in center frequency calibration.

In FSC systems, "f_{vco} is at the start of the frequency band" fulfills the requirement of selecting the frequency band that covers the required frequency range, but cannot calibrate the center frequency of the VCO.

Table 4.3: Comparison of frequency band detection scenarios

Type of control	f_{VCO} at the start of a freq. band	f_{VCO} in the middle of a freq. band
Coarse	+	-
Calibration	-	+

Chapter 5

Coarse frequency control

This chapter deals with the design of three coarse frequency control (CFC) systems. The first uses a constant divider architecture, whereas the second and third system use a variable divider architecture. One variable divider system is based on a pulse counter and the other one uses a digital logic quadricorrelator (DLQ) as a frequency difference detector. Furthermore, the section about the variable divider system based on a pulse counter introduces a system that uses a truncated divider ratio, which decreases the settling time.

The main aim of making these designs (with behavioral models) is to verify the band selection criteria and band requirements, introduced in chapter 4, by means of simulation. Therefore, only the linear search algorithm is implemented, but conclusions about other search algorithms can be drawn up as well. Furthermore, conclusions about complexity and settling time can be drawn up and finally, every section gives a design procedure of the discussed system.

All described systems use the architecture given in figure 5.1. In this architecture, the feedback divider in the PLL will be re-used. In case of the constant divider ratio architecture, the divider ratio is set to the appropriate constant value during the open-loop step.

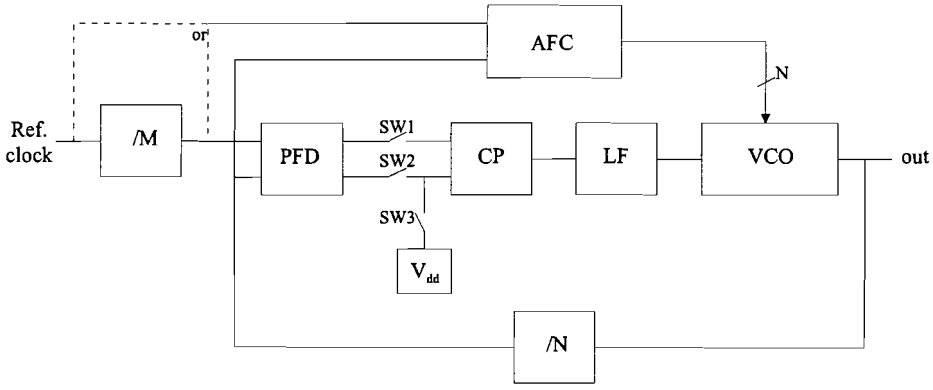

Figure 5.1: Discrete course control architecture

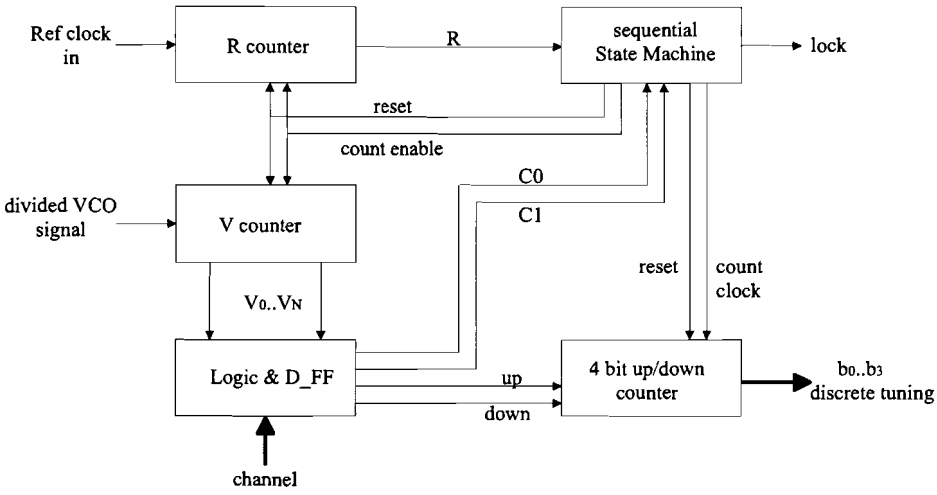

Figure 5.2: Block diagram of the AFC system used in a constant divider architecture.

5.1 Constant divider architecture with counter

This section describes a design of a constant divider course control system, followed by the simulation results and conclusions about settling time. Finally, a design procedure will be given.

5.1.1 Design

The coarse frequency control system uses the 4.5-7GHz VCO that is introduced in chapter 1. The block diagram of the CFC system in a constant divider architecture is illustrated in figure 5.2. The reference clock cycles are counted by the R counter, which triggers the sequential state-machine at the end of R cycles of the reference clock. This sets an exact measurement time, as discussed in chapter 3. The number of cycles of the divided VCO signal are counted with the V counter. The logic[1] and D-flip-flop block generates an UP or DOWN signal, depending on the value of the V counter and the desired channel. The 4 bit UP/DOWN counter sets the discrete tuning inputs of the VCO, like the implementation given in [11].

It must be noted that the desired channel (or desired frequency) must be converted into a corresponding value of the V counter, which can be done by means of additional logic or for example by means of a few lines of DSP code.

Assume that the constant divider ratio is 100 and the worst-case minimum frequency overlap between band number 14 and 15 is assumed to be 30 MHz. Now, the Δf_{det} and minimum necessary measurement time can be calculated.

$$\Delta f_{det} = \frac{30\text{MHz}}{2 * 100} = 150\text{kHz}, \qquad t_{m,min} = 6.66\mu\text{s}$$

[1]The exact functionality of this logical block will be discussed in the next section about the variable divider architecture

While using a reference clock of 10MHz and a value for R=66, the measurement time is 6.7μs (in this system, the reference counter always starts 1 reference clock period later then the V counter). This yields F = $N\Delta f_{det}$=14.9MHz. The lock value of V can be derived from the band selection criterion given in chapter 4 and can be calculated as follows

$$V_{lock} = \frac{f_d}{F} - 1 \tag{5.1}$$

where V_{lock} is the lock value of V, which is used in a lock scheme similar to the one given in the next section, in figure 5.6.

Simulation result
The general test-bench for course control systems is given in figure 5.3. During course control, this test-bench sets the output frequency of the VCO at the start of each frequency band and at the end of the discrete course tuning cycle, the output frequency of the VCO is set at the end of the frequency band. This gives the opportunity to check whether the VCO covers the desired frequency or not.

A simulation result of the constant divider system is given in figure 5.4, which shows a lock sequence of three measurement cycles of 6.7μs. At the end of the course tuning cycle, band number 7 is selected and the desired frequency of 5500MHz is covered by this frequency band. Further simulations have been conducted to check lock behavior in frequency band overlap regions, resulting in verification of the frequency band requirement and selection criterion given in chapter 4.

Settling time
The worst-case settling time of the linear search algorithm in combination with the 16 band oscillator is approximately 8 times 6.6μs, which yields approximately 53μs. This settling time can be reduced by using a binary search algorithm, which needs at least 4 measurement cycles to select one of the 16 frequency bands of the VCO. Then, the settling time is 4*6.6μs$\approx$27μs.

An implementation using the *interpolation search algorithm* requires a slightly different architecture; the value of the V counter and the desired channel are than also inputs of the sequential state machine, which directly determents the discrete tuning bits (b_0...b_3). A condition for a proper interpolation search algorithm: the span of the VCO frequency bands must be stored in for example a lookup table. The worst-case settling time of the interpolation search algorithm is estimated by 3 measurement cycles, yielding 3*6.6μs$\approx$19.8μs.

The constant divider architecture is also suitable for the application of a *power-up measurement algorithm*, storing all the start frequencies of the VCO frequency bands in for example a lookup table. This algorithm can directly determine the desired frequency band of the VCO and therefore the open-loop step is only required during the storage of the start frequencies of the frequency bands. Therefore the settling time, during normal operation, of this algorithm is estimated by 0μs. Although using stored values of the start frequencies of

the frequency bands, the minimum necessary measurement time of the measurement of the start frequency of the frequency bands and the band selection criterions stay the same as discussed before.

5.1.2 Design procedure

- Determine worst-case value for F_{OV}.
- Determine maximum settling time and then the constant divider ratio.
- Than, the maximum Δf_{det} and the minimum necessary measurement time can be calculated.
- Now the reference frequency can be chosen, which determines the length of the R counter and the specific value for R to indicate the end of the measurement period.
- Determine the minimum size of the V counter, consider using flip-flops to remember any counter overflow, like the implementation given in [11].
- Determine the type of channel to counter value conversion: e.g. logic or DSP.

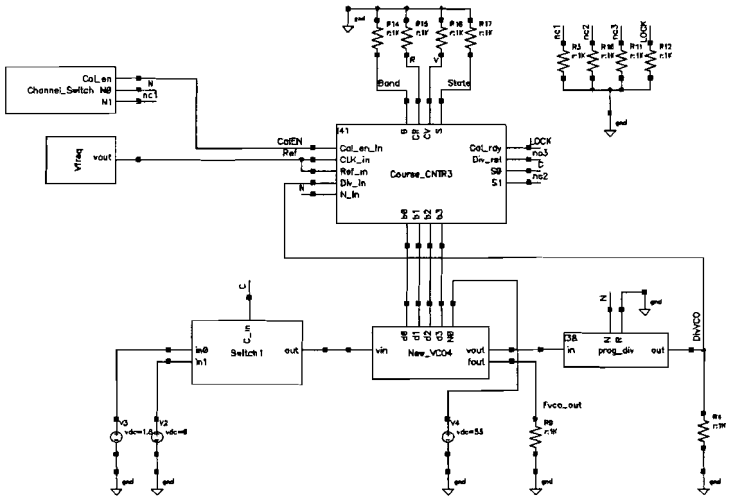

Figure 5.3: Course frequency control systems test-bench (no. 1): After the course tuning cycle, the start and end frequency of the selected frequency band of the VCO ban be checked, because the input voltage of the VCO is changed from one end of the range to the other one (0V to 1.8V).

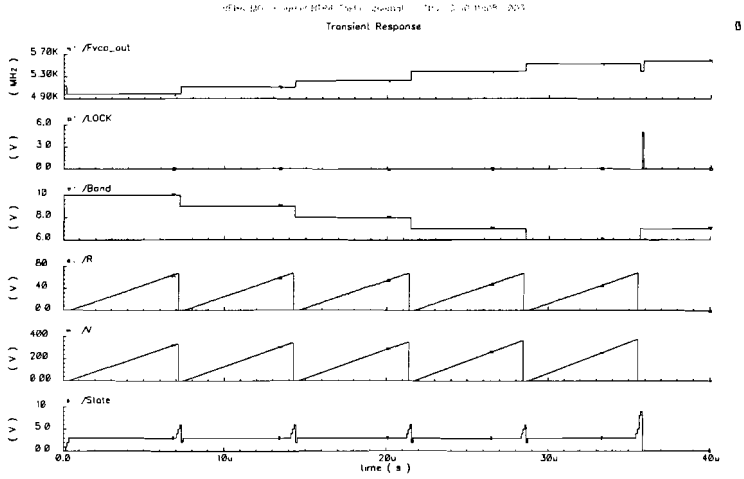

Figure 5.4: Simulation result of the constant divider system (in test-bench no. 1), starting in band number 10: The desired frequency is 5500MHz, signal Fvco_out gives the output frequency of the VCO, after 5 measurement cycles band number 7 is selected (Lock signal), the values of the R and V counters and the State of the state-machine are also shown.

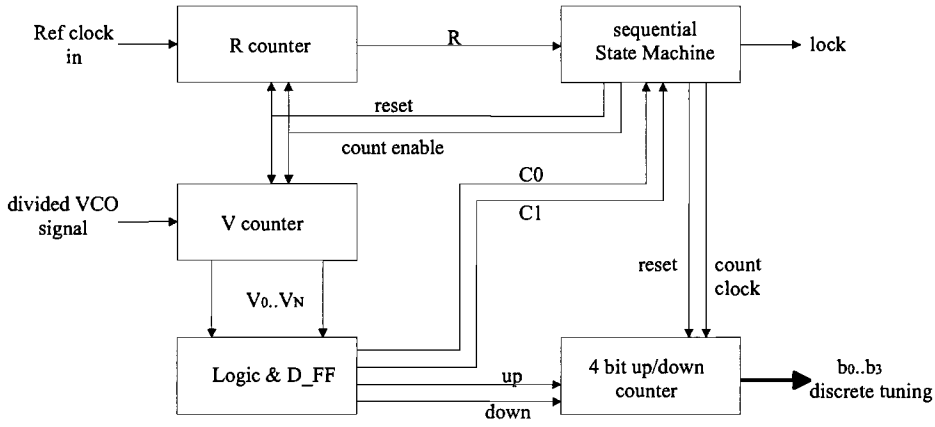

Figure 5.5: Block diagram of the AFC system, used in a variable divider architecture.

5.2 Variable divider architecture with counter

This section deals with the design of a coarse frequency control system based on a VCO pulse counter, used in a variable divider ratio architecture. The block diagram of this AFC system is given in figure 5.5. First of all, a straight forward system is designed, followed by a system that reduces the division ratio and therefore reduces the required measurement time. Finally, a design procedure will be given.

5.2.1 Design

The coarse frequency control system uses the 4.5-7GHz VCO that is introduced in chapter 1. This VCO is incorporated in a integer-N charge-pump PLL system which is introduced in chapter 2. The channel spacing of this PLL is assumed to be 1MHz, thus the feedback divider ratio can be varied between 5093 to 6556 (due to process spread, the frequency range of the VCO is reduced).
In this example design, the reference frequency of the digital course tuning loop will be chosen 1MHz[2]. Than, the divider ratio can be varied between 5093 and 6556. The worst-case minimum frequency overlap between band number 14 and 15 is assumed to be 30 MHz. The next step is to estimate the worst-case value for N_{e14}, which will be estimated by 4562*1.15=5246 (4562MHz is the nominal end frequency of band number 14 and in worst-case this value is 15% higher). Now, the minimum Δf_{det} and measurement time can be calculated.

$$\Delta f_{det} = \frac{30\text{MHz}}{5246} = 5.7\text{kHz}, \qquad t_{m,min} = 175\mu\text{s}$$

As calculated above, the minimum measurement time is 175μs and will be implemented by means of a 1MHz clock in combination with a counter, which has to count 175 clock periods (R is set to the value: R=175-1=174 ,because

[2]This reference frequency does not specify the clock frequency of the AFC system, but sets the limits and necessary accuracy of the feedback divider.

the reference counter always starts 1 reference clock period later then the V counter). The lock value of the V counter can be calculated as follows

$$V = t_{m,min} f_{ref} - 1 = 175\mu s * 1\text{MHz} - 1 = 175 - 1 = 174$$

As mentioned before, a selection of a higher divider ratio (which means that the desired frequency is also higher) results in lower detected frequencies. Therefore the frequency f_c, given in figure 4.6, is represented here by the value of V=174.

The linear search algorithm lock scheme is presented in figure 5.6. According to this lock scheme, the actions of the logic are given in table 5.1.

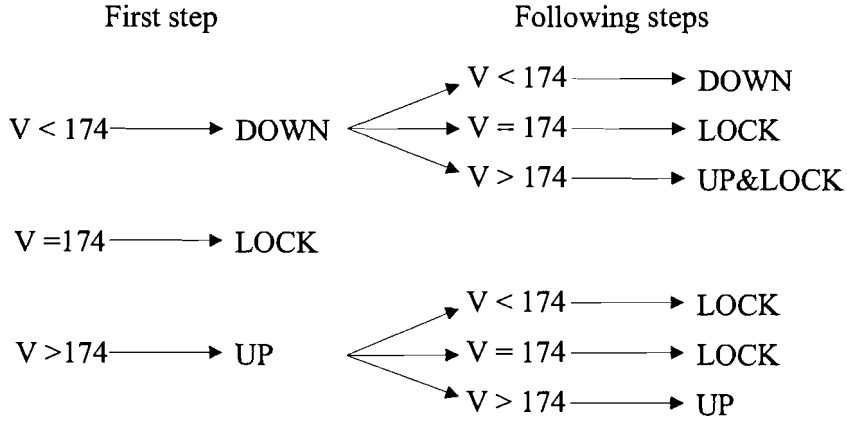

Figure 5.6: Implemented linear search lock scheme

Table 5.1: Logic table: Action and outputs (C0, C1, UP and DOWN) as function of *previous action* and counter value

Counter value (V)	Previous action	Action	C_1 C_0	UP DOWN
< 174	none	DOWN	0 0	0 1
< 174	UP	LOCK	1 1	0 0
174		LOCK	1 1	0 0
> 174	none	UP	0 0	1 0
> 174	DOWN	UP&LOCK	1 0	1 0

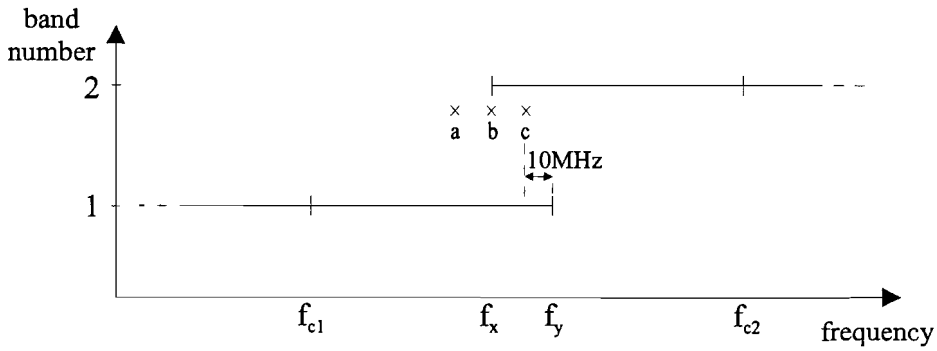

Figure 5.7: Reduced division ratio: Frequency band overlap incorporates 10MHz frequency selection error.

5.2.2 Reduced division ratio

As mentioned before, the measurement time directly depends on the amount of band overlap and the divider ratio. By dividing the divider ratio by a factor of 10 (then the divider ratio varies between 513 and 637), the measurement time can be reduced by approximately 7 times!

All divider values will be rounded off to the lower integer value. Therefore the worst-case frequency error in selecting the desired frequency with the variable divider will be maximal 10MHz. This error must be incorporated in the frequency overlap between the frequency bands, see figure 5.7.

The worst-case minimum frequency overlap between band number 14 and 15 is assumed to be 30 MHz. The next step is to estimate the worst-case value for N_{e14}, which is estimated by 525. Now, the minimum Δf_{det} and measurement time can be calculated.

$$\Delta f_{det} = \frac{30\text{MHz} - 10\text{MHz}}{525} = 38.1\text{kHz}, \qquad t_{m,min} = 26.25\mu\text{s}$$

In principle, the reference frequency of the automatic coarse frequency control is now 10MHz. As discussed earlier, the choice of the reference frequency is independent of the clock frequency. The minimum measurement time of 26.25μs, is realized by a means of a 1MHz clock, in combination with a value of R=27-1=26, which yields a measurement time of exactly 27μs.

The measurement time is 27μs, therefore the lock value for V is 269 (270-1). The linear search lock scheme, presented in figure 5.6, and the actions of the logic, given in table 5.1, stay the same. But, the lock value for V changes into 269.

Simulation result

Figure 5.8 shows a lock sequence of three measurement cycles each of 27μs. At the end of the course tuning cycle, band number 7 is selected and the desired frequency of 5500MHz is covered by this frequency band. Figure 5.9

shows the second test-bench using the PLL model (see chapter 2). in combination with the second test-bench: this test-bench includes the developed behavioral model of the PLL. A drawback of this test-bench is the much longer simulation times than the first test-bench. A three cycle lock sequence from the opposite direction (than the first shown simulation result), followed by a closed-loop step of the PLL, resulting in phase-lock at a frequency of 5500MHz is given in figure 5.10. Further simulations have been conducted to check lock behavior in frequency band overlap regions, resulting in verification of the frequency band requirements and selection criterions given in chapter 4.

Settling time
The worst-case settling time of the linear search algorithm in combination with the 16 band oscillator is approximately 8 times 27μs, which yields 216μs. This settling time can be reduced by using a binary search algorithm, which needs at least 4 measurement cycles to select one of the 16 frequency bands of the VCO. Then, the settling time is 4*27μs=108μs.

An implementation using the interpolation search algorithm is not recommended, because the variable divider ratio changes the total frequency detector accuracy (F). Therefore, the variable divider architecture is also not suitable for a power-up measurement algorithm.

5.2.3 Design procedure

- Determine worst-case value for F_{OV}.
- Determine maximum amount of divider ratio truncation and worst-case value for $N_{e(x-1)}$.
- Than the minimum necessary Δf_{det} and the minimum measurement time can be calculated.
- Now the reference frequency can be chosen, which determines the length of the R counter and the specific value for R to indicate the end of the measurement period.
- Determine the minimum size of the V counter, consider using flip-flops to remember any counter overflow, like the implementation given in [11].

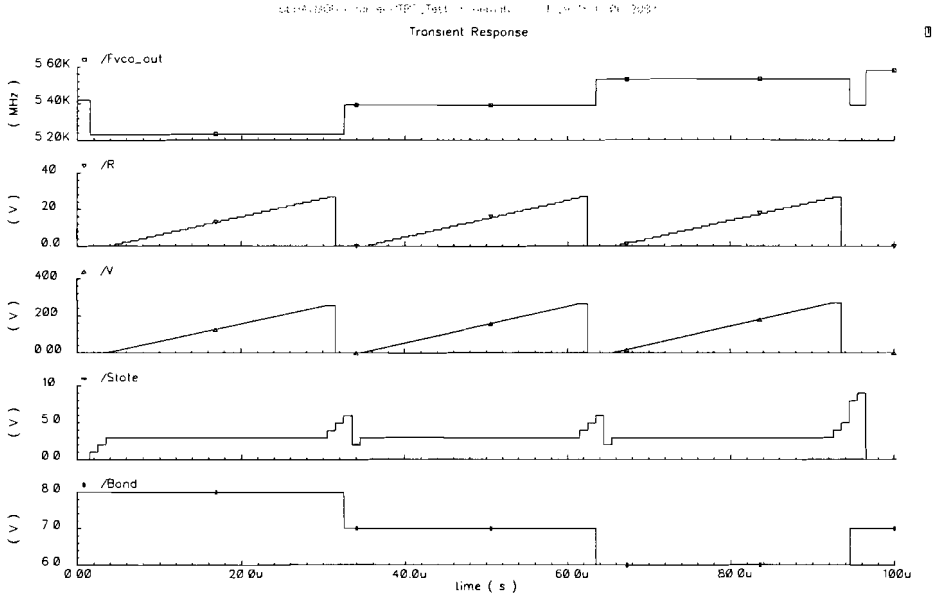

Figure 5.8: Simulation result of the variable divider system (in text-bench no. 1), starting in band 8: The desired frequency is 5500MHz. Signal Fvco_out gives the output frequency of the VCO, after 3 measurement cycles (approximately 94μs) locks the state-machine in band number 7 (Band), the values of the R and V counters and the State of the state-machine are also shown.

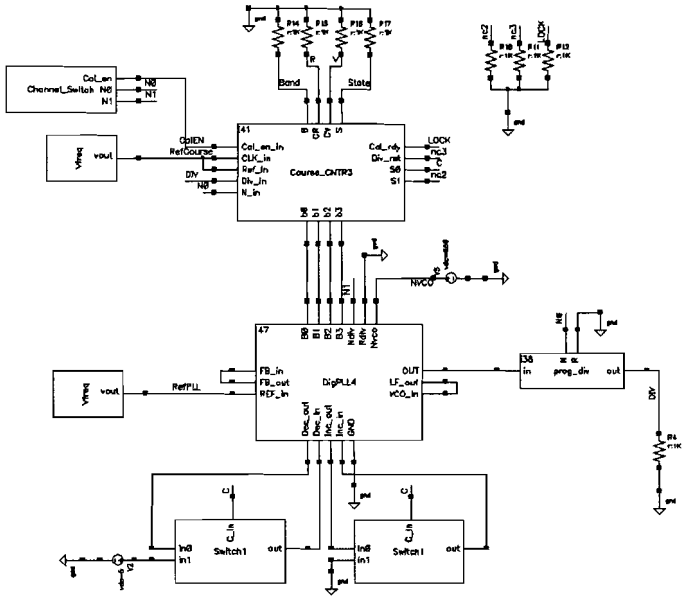

Figure 5.9: Course frequency control systems test-bench with PLL (no. 2): After the course tuning cycle, normal PLL operations start (closed-loop operation) and phase-lock at the desired frequency will follow.

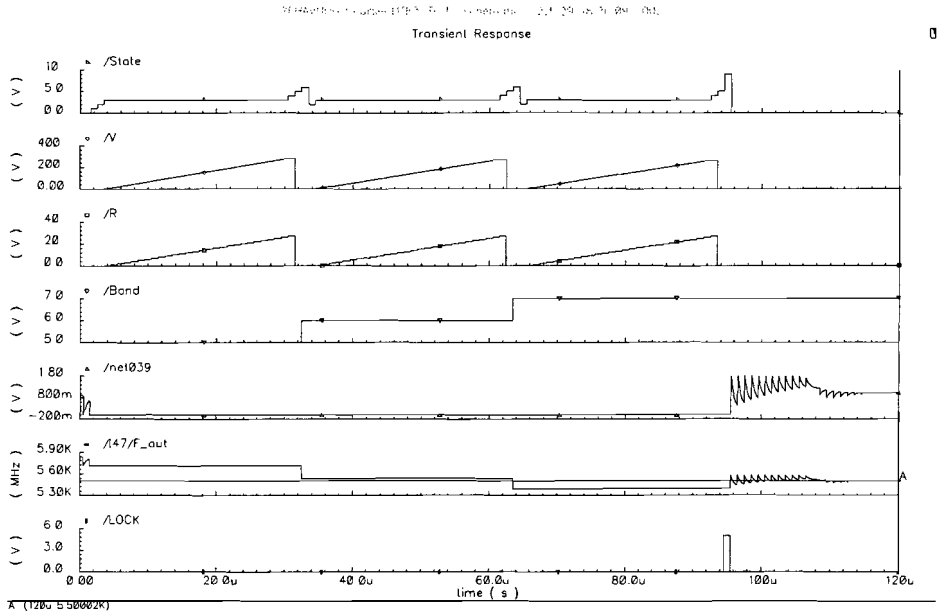

Figure 5.10: Simulation result of the variable divider system (in text-bench no. 2), starting in band 5: The desired frequency is 5500MHz. Signal Fvco_out gives the output frequency of the VCO, after 3 measurement cycles (approximately 94μs) locks (Lock) the state-machine in band number 7 (Band), the values of the R and V counters and the State of the state-machine are also shown. Then the PLL returns with normal closed-loop operation. Finally, the PLL locks at the frequency of 5500MHz.

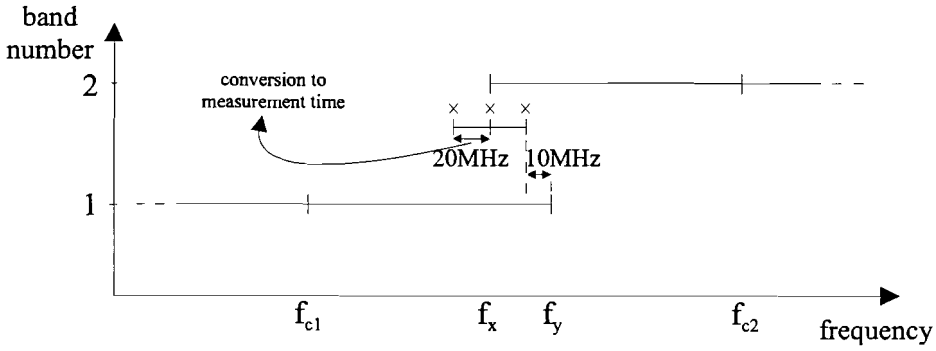

Figure 5.11: Frequency band overlap to measurement time conversion.

5.3 Variable divider architecture with DLQ

This section describes a design of a coarse frequency control system based on a digital logic quadricorrelator, used in a variable divider ratio architecture (also using a reduced division ratio). Followed by the simulation results and conclusions about the settling-time. Finally, a design procedure will be given.

5.3.1 Design

The coarse frequency control system uses the 4.5-7GHz VCO that is introduced in chapter 1. This VCO is incorporated in a integer-N charge-pump PLL system, which is introduced in chapter 2. The channel spacing of this PLL is assumed to be 1MHz, thus the feedback divider ratio in the PLL can be varied between 5093 to 6556 (due to process spread, the frequency range of the VCO is reduced).

The design of the CFC system based on the DLQ can also use the truncated divider ratio, which reduces the maximum measurement time of one measurement cycle. In this case, the divider ratio during course tuning is a factor 10 less than the normal divider ratio used in the PLL (then the divider ratio varies between 513 and 637 and the reference frequency at the input of the DLQ is 10MHz[3]). In addition to the division of 10, the divider ratio is also rounded off to the lower integer value. Then, the error in frequency selection by the divider (of 10MHz) must be incorporated in the frequency overlap between the frequency bands, see figure 5.11.

The next step is to convert the band selection criterions, given in chapter 4, into criterions for a CFC system using a DLQ. As discussed before, the amount of output pulses of a DLQ have and inverse relationship with the frequency difference of the signals at the input of the DLQ. Therefore, frequency distance between the discrete detectable frequencies, for CFC systems using a counter, must be converted into a maximum measurement time requirement, see figure 5.11.

[3]In the system with the DLQ, the chosen divider ratio sets the reference frequency for the DLQ frequency difference detector.

The worst-case minimum frequency overlap between band number 14 and 15 is again assumed to be 30 MHz. The next step is to estimate the worst-case value for N_{e14}, which will be estimated by 525. Now, the minimum Δf_{det} (or frequency difference between discrete detectable frequencies) and measurement time of a CFC system with counter can be calculated.

$$\Delta f_{det} = \frac{30\text{MHz} - 10\text{MHz}}{525} = 38.1\text{kHz}, \qquad t_{m,counter} = 26.25\mu\text{s}$$

As mentioned before, the maximum measurement time of a (balanced) DLQ2 to detect a frequency difference of Δf_{det} is 4 times less than the above calculated value for t_m, therefore

$$t_{m,DLQ2} = \frac{t_{m,counter}}{4} = \frac{26.25\mu\text{s}}{4} = 6.56\mu\text{s} \approx 6.6\mu\text{s} \tag{5.2}$$

In the case that the desired frequency is close to the start of frequency band number 2 and within the 20MHz frequency range, indicated in figure 5.11, then the frequency difference between the reference frequency and the divided VCO signal will become so small that the DLQ2 will not give any frequency difference indication within 6.56μs (as calculated above). Then frequency band number 1 must be selected.

It must be noted that the time between two pulses at the output of the DLQ2, is only valid in a stable situation. Therefore, after switching frequency bands, the CFC systems waits for a pulse of the DLQ2 and then the R counter starts counting. If the R counter times out before any output of the DLQ is received, the frequency difference is less than the calculated 20MHz frequency range above (and below) and frequency band number 1 must be selected, see 5.11.

At this point the frequency error due to discrete sampling behavior of the DLQ2 detector must be calculated, resulting in a slightly higher measurement time (or value for R) and therefore the CFC with DLQ can never select the wrong frequency band. Assume the measurement time is 6.6μs then the detectable frequency difference within this measurement period is

$$f_{diff1} = \frac{1}{6.6\mu\text{s} * 4} * 525 = 19.89\text{MHz}$$

The maximum absolute time error is 1 period of the reference clock: 100ns. Therefore, the next calculated frequency difference, f_{diff2}, represents the maximum detectable frequency difference that the DLQ can detect during the measurement period of 6.6μs.

$$f_{diff2} = \frac{1}{6.5\mu\text{s} * 4} * 525 = 20.19\text{MHz}$$

Now the frequency error can be calculated

$$f_{err} = f_{diff2} - f_{diff1} = 0.3\text{MHz}$$

Due to this frequency difference measurement error, the actual measurement time must be 100ns longer than the before calculated 6.6μs and becomes 6.7μs.

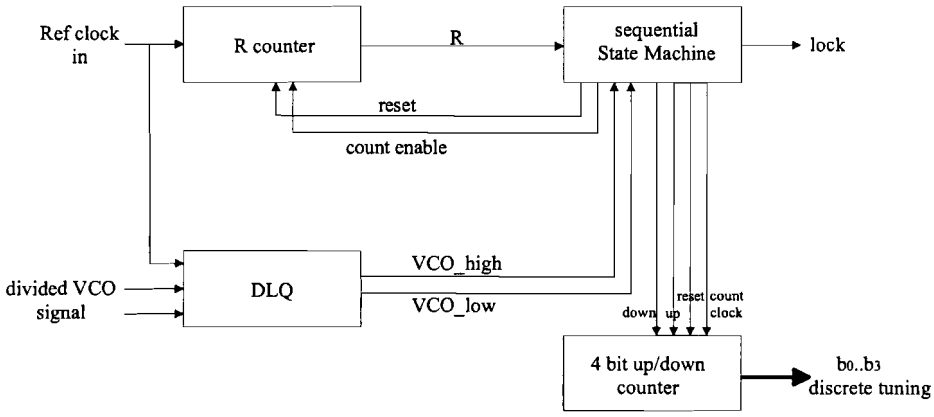

Figure 5.12: Block diagram of the CFC system with DLQ, used in a variable divider architecture.

The next step is to calculate the value of R for the reference counter

$$R = \frac{t_m}{t_{ref}} = \frac{6.7\mu s}{100ns} - 1 = 66 \tag{5.3}$$

In this system, the reference clock counter starts 1 clock period later than the actual measurement starts, therefore the contribution of -1 in the calculation of R, resulting in a measurement time of $t_{m,DLQ2} = 6.7\mu s$.

The complete block diagram of the CFC system with DLQ2 is given in figure 5.12. In brief, the DLQ2 indicates whether the frequency of the divided VCO signal is higher than the reference frequency or lower. Furthermore, the reference counter counts R pulses to indicate that the maximum measurement time is over. The sequential state-machine controls the 4 bit up/down counter and the lock output indicates the selection of the appropriate frequency band. The 4 bit up/down counter is used to control the discrete tuning inputs of the VCO and therefore this CFC system uses a linear search algorithm.

Simulation result

Figure 5.13 shows a lock sequence of the course control with the DLQ2, starting in band number 15. At the end of the course tuning cycle, band number 7 is selected and the desired frequency of 5500MHz is covered by this frequency band. Figure 5.14 shows a lock sequence from the opposite direction, starting in band number 0. Also resulting in the selection of the appropriate frequency band.

For the next simulation, the output frequencies of the VCO are slightly shifted upwards (absolute spread). Therefore the frequency overlap between frequency band 7 and 8 of the VCO is now situated above the desired frequency of 5500Mhz. Furthermore, the desired frequency of 5500MHz lays within the 20MHz range of the start of frequency band 7 (thus frequency band number 8 must be selected). The simulation result, given in figure 5.15, shows lock in band number 8 after timeout due to the reference counter.

Settling time

The worst-case settling time of the CFC system with DLQ, using a linear search algorithm in combination with the 16 band oscillator is approximately 16μs, which is very fast for the used divider ratio of 513 to 637.

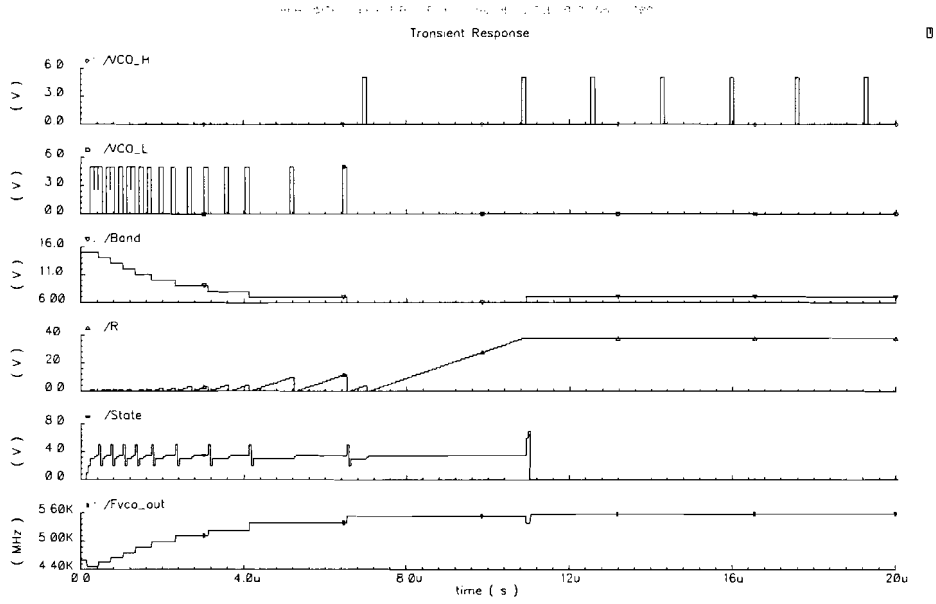

Figure 5.13: Simulation result of the variable divider system with DLQ (in text-bench no. 1), starting in band 15: The desired frequency is 5500MHz. VCO_H and VCO_L are the outputs of DLQ2. Signal Fvco_out gives the output frequency of the VCO, after approximately 11μs lock the state-machine in band number 7 (Band), due to the change from pulses from VCO_L to pulses from VCO_H.

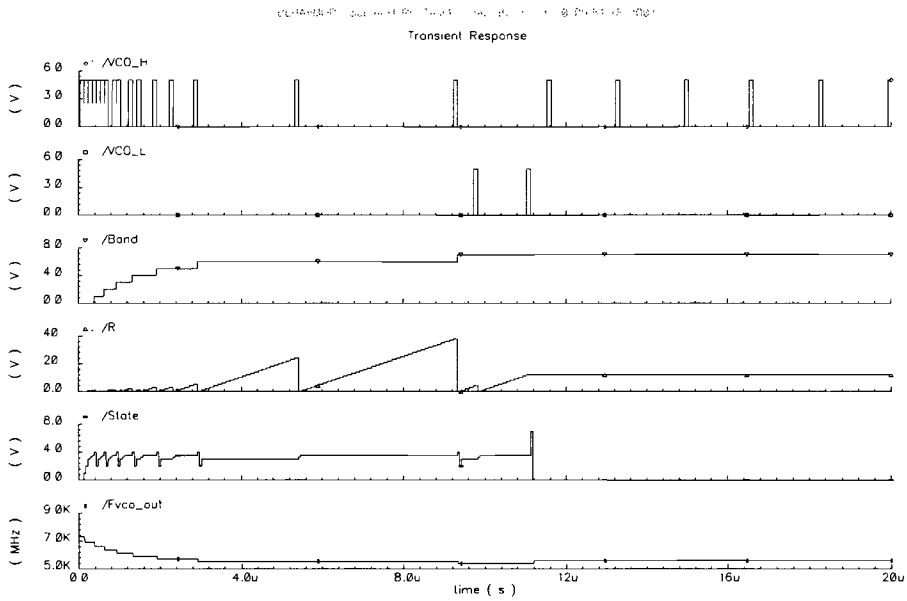

Figure 5.14: Simulation result of the variable divider system with DLQ (in text-bench no. 1), starting in band 0: The desired frequency is 5500MHz. VCO_H and VCO_L are the outputs of DLQ2. Signal Fvco_out gives the output frequency of the VCO, after approximately 11μs lock the state-machine in band number 7 (Band), due to the change from pulses from VCO_H to pulses from VCO_L.

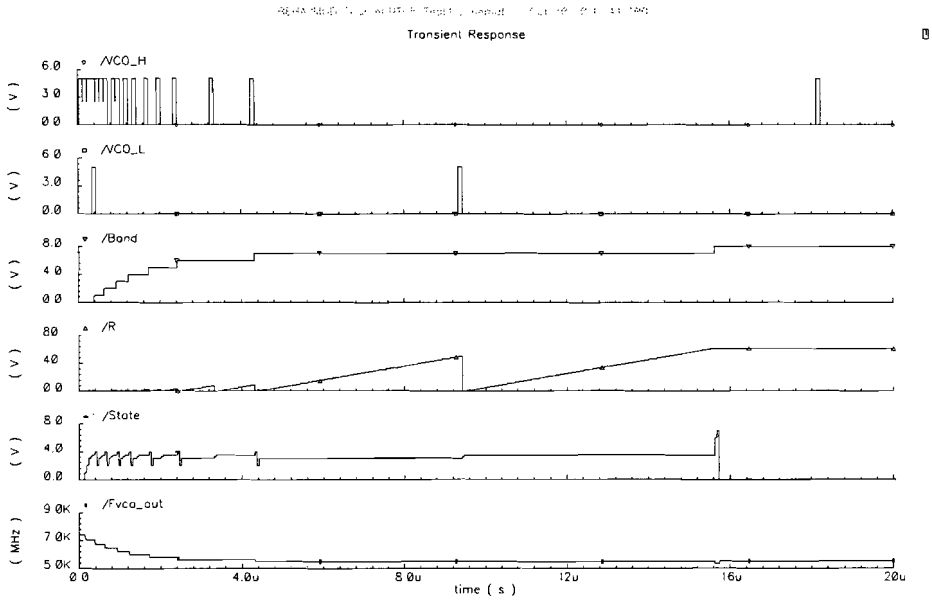

Figure 5.15: Simulation result of the variable divider system with DLQ (in text-bench no. 1), starting in band 0: The desired frequency is 5500MHz. Signal Fvco_out gives the output frequency of the VCO. After approximately $9\mu s$ the output pulses on VCO_H change into pulses on VCO_L, then the time measurement with the R counter starts. After timeout of the R counter, the state-machine decides to lock in band number 8 (Band). Finally, coverage of the selected frequency band (in this case 8, because VCO is shifted up in frequency) can be checked.

5.4 Comparison of CFC systems

In this chapter, three CFC are designed: one constant divider and two variable divider systems. The first variable divider system uses a pulse counter and the second is based on digital logic quadricorrelator. The simulated behavioral model systems verify the band requirements and selection criterions given in chapter 4. Furthermore, the most important conclusions for these CFC systems are briefly summarized:

The smallest settling time can be realized with a constant divider architecture, however this leads to increased complexity due to the desired frequency to corresponding counter value conversion (see table 5.2), in combination with the need for high frequency counters.

The constant divider architecture is also suitable for very fast search algorithms, like the interpolation and power-up measurement algorithm. Both algorithms result in increased complexity.

The variable divider architecture is more suitable for the linear and binary search algorithms (see table 5.3).

In the presented variable divider architecture; divider ratio reduction by a factor of 10 decreases the measurement time roughly by a factor of 7!

Especially, the system with DLQ results in a very fast settling time ($< 16\mu s$), while using the minimum complexity variable divider architecture.

Table 5.2: Design parameters as function of each architecture

Design parameters	Constant divider	Variable divider	
		Counter	DLQ
Complexity	-	+	++
Settling time (speed)	++	-	+

Table 5.3: Applicability of the search algorithms for each architecture

Search algorithm	Constant divider	Variable divider	
		Counter	DLQ
linear	+	+	+
binary	+	+	+
interpolation	+	-	-
power-up measurement	+	-	-

Chapter 6

Frequency spread calibration

This chapter gives a description of a frequency spread calibration (FSC) system with a digital pulse counter, which counts rising edges of the divided VCO signal. Simulation results can be found in appendix E. Appendix F gives a brief description of the predecessor of the presented FSC system. Although the system, given in appendix F, works properly, the band dependance in that system is not a practical property. Therefore the FSC system presented in this chapter is recommended for use. The next section deals with the design of a FSC system and the remaining of this chapter describes a general design procedure.

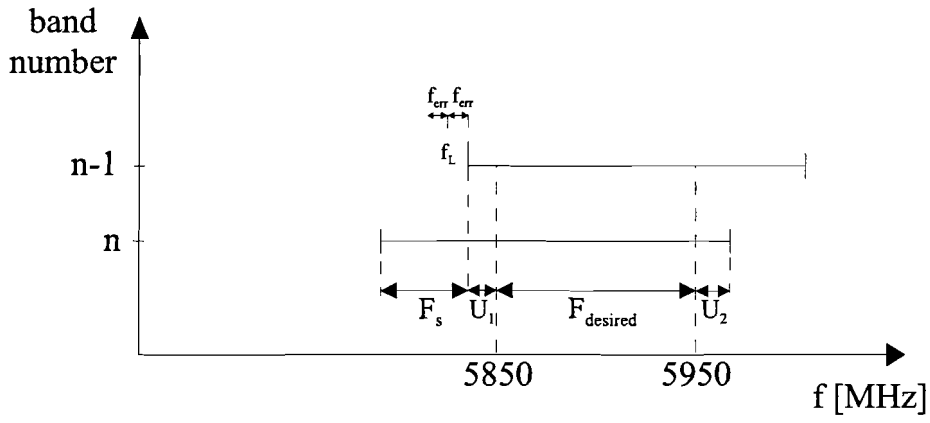

Figure 6.1: Definition of the discrete lock frequency f_L, the desired frequency band, U margins, frequency error of the detector (f_{err}, frequency spacing F_s and the desired frequency range $F_{desired}$.

Table 6.1: f_b, F_s and F_{span} and as a function band number 1 to 7 (n) under condition that the previous frequency band (n-1) starts at 5830MHz.

n	Condition [MHz]	Absolute spread	f_{b_n} [MHz]	F_{s_n} [MHz]	F_{span_n} [MHz]
1	$f_{b_0} = 5830$	0.949	5650	179	483
2	$f_{b_1} = 5830$	0.980	5661	168	453
3	$f_{b_2} = 5830$	1.009	5670	159	426
4	$f_{b_3} = 5830$	1.037	5685	150	399
5	$f_{b_4} = 5830$	1.064	5705	144	381
6	$f_{b_5} = 5830$	1.091	5692	137	363
7	$f_{b_6} = 5830$	1.118	5700	129	346

6.1 Design

The FSC system calibrates the second example VCO, given in chapter 1. Details about this VCO, with 8 overlapping frequency bands, can be found in appendix A.2. As illustrated in figure 6.1, the desired frequency band in the FSC system has a bandwidth of 100MHz and this band will be situated between: $f_b = 5850$MHz and $f_e = 5950$MHz. Furthermore, the next assumptions will be made: the reference frequency is 10MHz (f_{ref}) and the used division ratio N is 10[1]. The U_1 and U_2 margins are assumed to be 20MHz, resulting in a lock frequency of f_L=5850MHz-20MHz-f_{err}=5830MHz-f_{err}.

Absolute and relative process spread change the values of the frequency band spacing (F_s), frequency band overlap (F_{ov}) and the span of the frequency bands (F_{span}), therefore these parameters are dependent on the band number and amount of spread. In general, if absolute spread shifts the frequency bands up, to higher frequencies, the ranges are extended and F_s and F_{span} increase. Similarly, in the case that the bands shift down, the frequency ranges of the bands are compressed and F_s and F_{span} decrease. Furthermore, it has been shown that mismatch faults (relative spread), changes the range of each frequency band and the frequency spacing between two adjacent frequency bands. Thus, the values for F_s, F_{ov} and F_{span} are dependent on the band number and as well on the amount of absolute and relative spread. First of all, the influence of absolute spread will be considered, followed by relative spread.

Absolute spread greatly influences the operating frequency of the VCO and, for example, span of the frequency bands. Therefore table 6.1 shows the values for the start frequency f_b, F_s and F_{span} of band number 1 to 7 under condition that the previous frequency band starts at $5850 - U = 5830$MHz, see figure 6.1. The condition that the previous frequency band exactly starts at 5830MHz defines a *certain amount of absolute spread*, which is also given

[1]As mentioned before, the division ratio has an inverse relationship with the necessary measurement time. A division ratio of 10 shows the possibility to create a system with a very fast settling-time. Practical implementations may also use higher division ratios.

in table 6.1. The given values for f_b, F_s and F_{span} are only the result of absolute spread.

Relative spread introduces an extra error of approximately 4% in the frequency band spacing and the span of the frequency bands (see results of statistical simulations in chapter 1), this error is not incorporated in the values given in table 6.1.

Figure 6.2 shows the block diagram of the FSC system. The divider VCO signal is counted by the V counter, the logic and D-flip-flop block compares the output of the V counter with the discrete lock frequency and gives either an UP or DOWN output signal to the 3 bit UP/DOWN counter, which controls the discrete control inputs of the VCO. The state-machine controls the actions of the FSC system and determents convergence of the linear search algorithm according to the outputs of the logic&D_FF block. In this particular design, the reference clock counter R is not used. Instead of this counter the state-machine waits a couple of clock cycles to establish a certain measurement time.

In practice, f_L must be an integer multiple of F and is given by

$$f_L = xF \tag{6.1}$$

where x can be any positive integer value. In the case that $\Delta f_{det} = 5\text{MHz}$ (exactly two reference cycles), than $F = N\Delta f_{det} = 50\text{MHz}$ and the frequency for f_L can be calculated with

$$f_{L,max} = f_{desired,start} - U_1 = 5850\text{MHz} - 20\text{MHz} = 5830\text{MHz}$$

The closest integer multiple of F, lower than 5830MHz is $f_L = 5800\text{MHz}$. Than the U_1 margin is 50MHz. Therefore, the minimum frequency span requirement is

$$\begin{aligned} F_{span} &\geq U_1 + U_2 + F_{desired} + f_{err} + F_s \\ F_{span} &\geq 50 + 20 + 100 + 50 + 130\text{MHz} = 350\text{MHz} \end{aligned} \tag{6.2}$$

which is definitely not true for band number 7, therefore Δf_{det} will be set by three reference cycles (instead of 2), which yields $\Delta f_{det} = 3.333\text{MHz}$ and $F = 33.33\text{MHz}$. Now f_L will be 174 times F, which gives f_L = 174*33.33MHz= 5800MHz. The minimum frequency span requirement is

$$F_{span} \geq 20 + 20 + 100 + 33.33 + 130 \approx 303\text{MHz}$$

which is true for all frequency bands, even in the case of an additional error of 4% due to relative spread.

The actions of the logic&D_FF block are dependent on the previous action and the current output value of the counter V, see table 6.2.

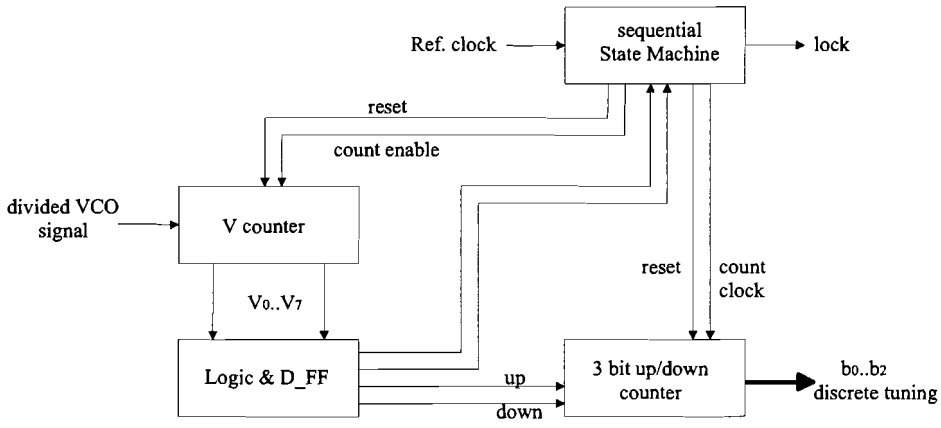

Figure 6.2: Block diagram of the FSC system

Table 6.2: Logic table: Action and outputs (C0, C1, UP and DOWN) as function of *previous action* and counter value

Counter value (V)	Previous action	Action	C_1 C_0	UP DOWN
< 174	none	DOWN	0 0	0 1
< 174	UP	LOCK	1 1	0 0
174		LOCK	1 1	0 0
> 174	none	UP	0 0	1 0
> 174	DOWN	UP&LOCK	1 0	1 0

Simulation result
Figure 6.3 shows the test-bench for FSC systems and figure 6.4 shows the block diagram of the implemented FSC system. Figure 6.5 shows a simulation result of the FSC system, starting in band number 0 and finally selecting band number 2 for normal PLL operation.

Settling time
The worst-case settling time of this FSC system, using a constant divider ratio of 10 and a linear search algorithm in combination with the 8 band oscillator is approximately 2.5μs. But, by decreasing the used divider ratio, the settling-time will become longer.

6.2 Design procedure

- Determine worst-case values for F_s and F_{span}, which are band dependent.
- Determine maximum settling-time and then the constant divider ratio.
- Than, the maximum Δf_{det} and the minimum necessary measurement time can be calculated.
- Now the reference frequency can be chosen, which determines the length of the R counter and the specific value for R to indicate the end of the measurement period (or in this design, a specified number of reference cycles that the state-machine waits).
- Calculate the value of f_L, which is an integer multiple of F.
- Check whether the frequency span of all the frequency bands satisfies the frequency span requirement, given in equation 6.2.
- Determine the minimum size of the V counter, consider using flip-flops to remember any counter overflow, like the implementation given in [11].

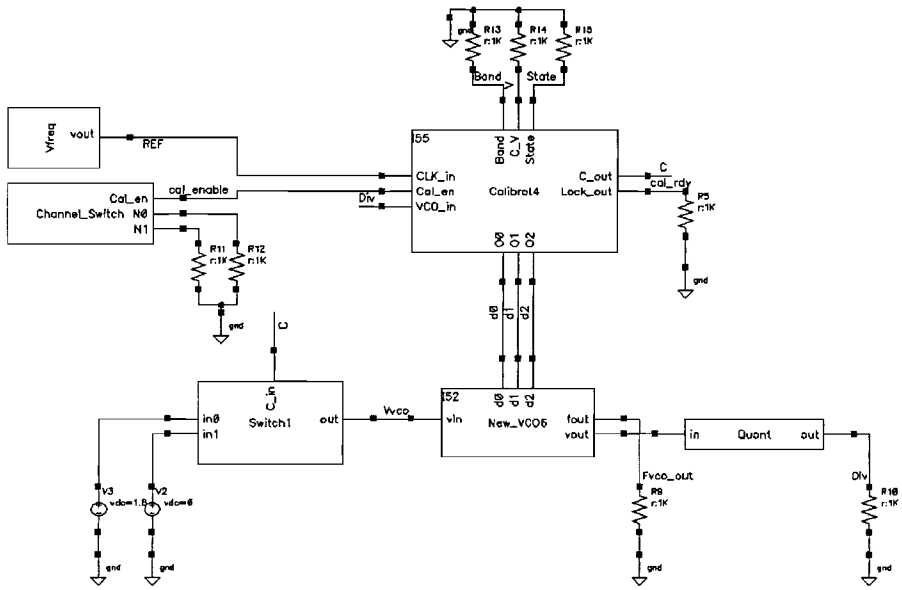

Figure 6.3: FSC system test-bench: After the calibration cycle, the start and end frequency of the selected frequency band of the VCO ban be checked, because the input voltage of the VCO is changed from one end of the range to the other one (0V to 1.8V).

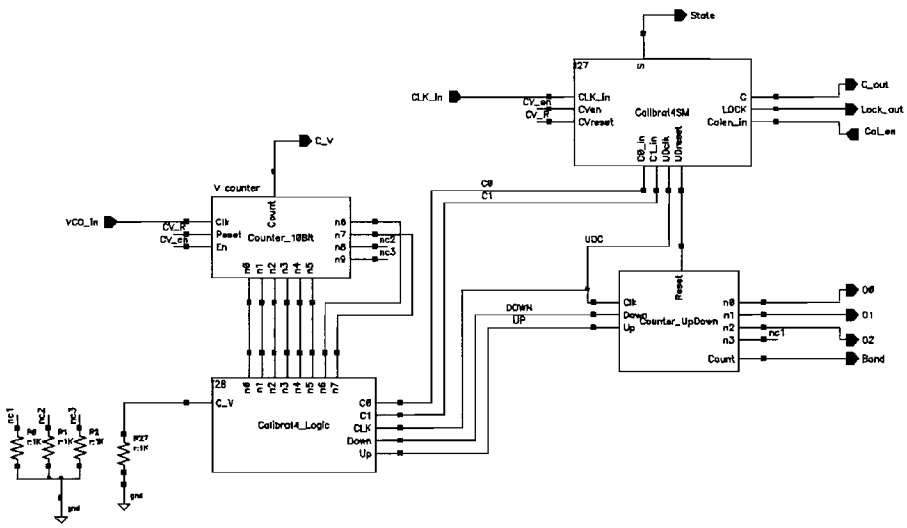

Figure 6.4: Implemented FSC system in Verilog/Cadence

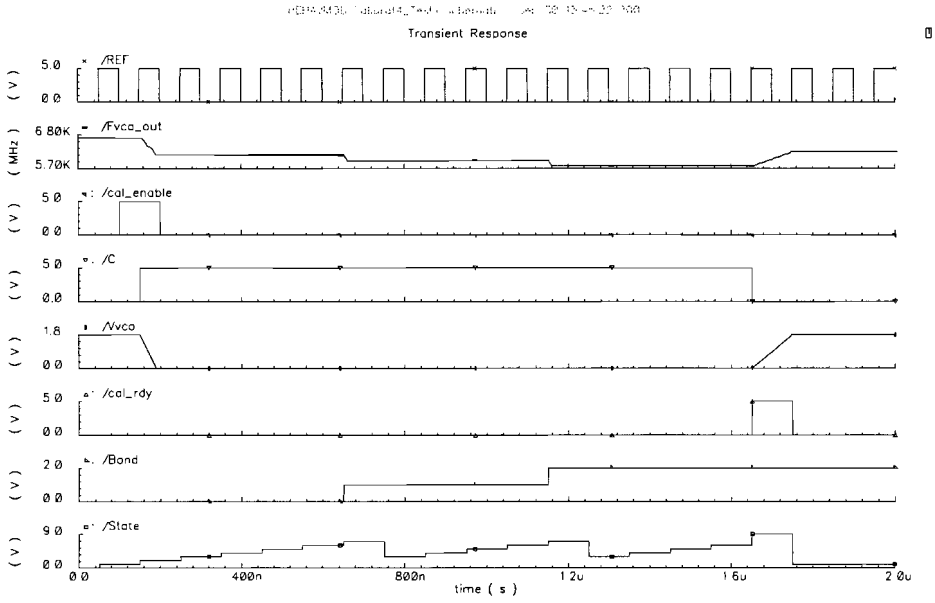

Figure 6.5: Simulation result of the FSC system: The lock frequency is 5830MHz, signal Fvco_out gives the output frequency of the VCO. The calibration starts with the Cal_enable signal, after approximately 1.6μs shows the Cal_RDY signal that the calibration is ready. Finally, coverage of the selected frequency band can be checked and the desired frequency is covered by band number 2.

Chapter 7

Conclusion

In general, the output frequency of an oscillator is a function of the control voltage at the input and is subject to variation due to external variables (e.g. process-spread). Furthermore, phase noise is proportional to K_{vco} and the noise voltage on the control input of the VCO. Thus, low noise applications require a VCO with a minimized tuning constant. However, a low tuning constant can be in conflict with the required tuning range. A way to achieve a large tuning range and a small K_{vco} simultaneously, is by using several partially overlapping frequency bands. Therefore, switch-selected tuning elements are used in an oscillator. An automatic frequency control (AFC) system must select the appropriate frequency band, followed by normal PLL operations, resulting in phase-lock at the desired output frequency.

The tuning range requirement roughly divides the systems that use a VCO into two categories: wide-band and narrow-band systems. Therefore, automatic frequency control (AFC) systems can be divided into two types of systems: course frequency control (CFC) systems and frequency spread calibration (FSC) systems. The main difference between both systems is: in a course control system the AFC selects an appropriate frequency band every time a new frequency is selected and in a calibration system the AFC selects the proper frequency band at start-up.

The frequency bands in a calibration system must at least cover the whole required frequency range and must be able to compensate for external variations during operation, whereas in a course frequency control system each frequency band can be smaller than the complete required frequency range, as long as the frequency bands together are able to cover the required frequency range, even under worst-case conditions. Furthermore, the overlap between two adjacent frequency bands can be small, as long as the bands are able to compensate for the quantization error of the AFC system.

The VCO is incorporated in a commonly used integer-N charge-pump PLL. A charge-pump PLL consists of a PFD, CP, LF, VCO, a feedback divider and a reference divider. Simulations of the developed behavioral model of the charge-pump PLL show phase-lock at the desired output frequency.

Nearly all AFC architectures use an open-loop step to select the appropriate frequency band followed by a closed-loop step to achieve phase-lock. Most systems described in the literature rely on a reference voltage (e.g. mid-level) that is connected to the VCO tuning input during the open-loop step. Four methods setting the PLL in a open-loop condition have been presented: The first two set the control voltage of the VCO at a certain level, thereby interfering with an sensitive analog part in the PLL. The third and fourth presented method use switches in the digital part of the PLL, driving the loop-filter voltage to V_{ss} (or V_{dd}). The fourth method controls the CP directly and has a much faster settling time than the third method. Therefore, the fourth method will be used in the further design automatic frequency control systems.

The all digital AFC system is the most promising architecture, found in the literature. Especially combined with the before mentioned method to set the PLL in open-loop by controlling the CP directly. This method sets the control voltage of the VCO at V_{ss}, resulting that during calibration, the output frequency is always at the start of each frequency band.

Two ways of digital frequency detection are discussed: the frequency counter (FC) and the frequency difference detector (FDD). A pulse counter can be used as a frequency counter, when it counts during a specified measurement period. The pulse counter can also be used as a frequency difference detector when it is combined with some additional logic, which truncates the resulting counter value in an up/down error signal. The DLQ can only be used as a frequency difference detector. *Minimum complexity is offered by the DLQ in combination with a very attractive measurement-time.*

The generic frequency band requirements and selection criterions were introduced for coarse frequency control and frequency spread calibration systems. The all digital coarse control systems are further subdivided into constant divider and variable divider architectures. In the case of frequency spread calibration systems the case of one fixed required frequency range is considered, resulting in a constant divider architecture.

For the above mentioned cases, two different detection scenarios were considered: "f_{vco} is at the start of a frequency band" and "f_{vco} is in the middle of a frequency band". The most important conclusions will be briefly summarized:

- In course control systems with small band overlap between two adjacent frequency bands, "f_{vco} is at the start of a frequency band" is the preferred method.
- In CFC systems, the "f_{vco} is in the middle of a frequency band" detection method needs (additional) information about the span of the frequency bands to select the appropriate frequency band.
- In CFC systems, a small and constant divider ratio will result in the fastest settling time.

- In the case that the divider ratio of the constant and variable divider architecture is in the same order, the variable divider ratio system needs the smallest measurement time.
- In CFC systems, a variable divider architecture results in minimum complexity.
- In FSC systems, "f_{vco} is in the middle of a frequency band" results in center frequency calibration.
- In FSC systems, "f_{vco} is at the start of the frequency band" only fulfills the requirement that the selected frequency band covers the required frequency range and the center frequency of the VCO is not calibrated.

Three CFC systems are designed: one constant divider and two variable divider systems. The first variable divider system uses a pulse counter and the second is based on digital logic quadricorrelator. The most important conclusions for these CFC systems are briefly summarized:

- The frequency band requirements and selection criterions, given in chapter 4, are valid for the tested systems.
- The smallest settling time can be realized with a constant divider architecture, however this leads to increased complexity due to the desired frequency to corresponding counter value conversion (see table 5.2), in combination with the need for high frequency counters.
- The constant divider architecture is also suitable for very fast search algorithms, like the interpolation and power-up measurement algorithm. Both algorithms result in increased complexity.
- The variable divider architecture is more suitable for the linear and binary search algorithms (see table 5.3).
- In the presented variable divider architecture, division ratio reduction by a factor of 10 decreases the measurement time roughly by a factor of 7!
- *Especially, the CFC system using the balanced DLQ in combination with a reduced division ratio results in a fast settling time ($< 16\mu s$), while using the minimum complexity variable divider architecture and the minimum complexity DLQ frequency difference detector.*

One FSC system is designed, mainly to verify the band requirements and selections criterions introduced in chapter 4. This design shows the possibility to make a FSC system in which the PLL is set in open-loop by controlling the CP directly. Therefore, the output frequency of the VCO is always at the start of each frequency band during calibration. After that, the PLL is set in closed-loop condition and normal PLL operations follows. The simulation results show that the appropriate frequency band is selected, but the center frequency of the VCO is not calibrated.

Chapter 8

Future research

In the future, more and more low noise oscillators covering a large frequency range are needed. Especially for multi-standard systems sharing the front-end part. In addition, the supply voltage decreases due to migration to newer technology, therefore the VCO tuning constant (K_{vco}) will increase. To achieve a large tuning range and a small K_{vco} at the same time, oscillators with discrete tuning inputs are introduced. Therefore automatic frequency control (AFC) systems are needed and the presented systems could be further improved by:

- First of all, the AFC systems based on Verilog behavioral models can be converted into a digital implementation in a FPGA, which controls the frequency bands of the 4.5-7GHz oscillator. By adding a down-convertor followed by a programmable (digital) frequency divider; the frequency band requirements presented in chapter 4 can be verified by means of measurements.

- The generic frequency band requirements, introduced in chapter 4 are optimized for speed. Therefore reliable estimations of the frequency band margins of the frequency bands are necessary. Further research on the used VCO is needed to estimate of these margins with respect to external variations, like: process spread and temperature.

- Furthermore, the generic frequency band requirements that are introduced in chapter 4 can also be optimized for robustness of the system. This will of course result in a longer settling-time. A remaining question is: in what ways can the system be made more robust, without knowing any information of the VCO frequency bands? A possibility could be measuring the start and end frequency of the bands of interest, followed by selection of the 'best' frequency band for operation.

- Nowadays many systems use fractional PLL architectures. The applicability of the suggested reduced division ratio method must be proven for application in systems using fractional-N PLLs.

- The AFC system, using the digital logic quadricorrelator can be made faster by using a simple interpolation search algorithm, based on the value of the reference counter. Further increase of speed can be achieved by phase-alignment by resetting the digital dividers.

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Appendices

Appendix A

VCO

A.1 Frequency bands of the first example VCO: 4.5-7 GHz

Table A.1 gives the nominal operating frequencies of the 16 frequency bands of the first example VCO [4]. The figures A.1, A.2 and A.3 on the next page give the frequency bands of the VCO for the cases that the bands are shifted down, up as well as the nominal case.

Table A.1: Frequencies of the frquency bands of VCO example 1

Band number	f_b [MHz]	f_c [MHz]	f_e [MHz]	K_{vco} [MHz/V]
0	6919	7123	7326	226.1
1	6616	6793	6970	196.7
2	6364	6517	6670	170.0
3	6121	6266	6411	161.1
4	5905	6035	6165	144.4
5	5713	5833	5952	132.8
6	5536	5647	5757	122.8
7	5393	5488	5582	105.0
8	5233	5327	5420	103.9
9	5118	5196	5274	86.70
10	4986	5062	5138	84.40
11	4869	4941	5013	80.00
12	4753	4826	4899	81.10
13	4653	4722	4790	76.10
14	4562	4630	4697	75.00
15	4465	4536	4606	78.30

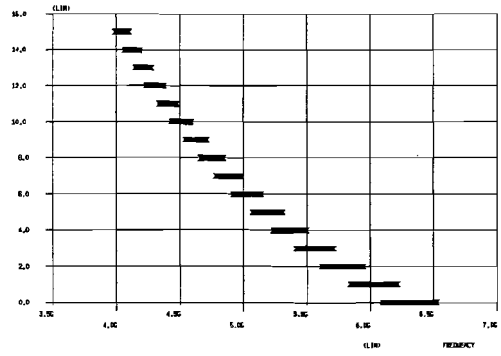

Figure A.1: Frequency bands of VCO 1 shifted to lower frequencies

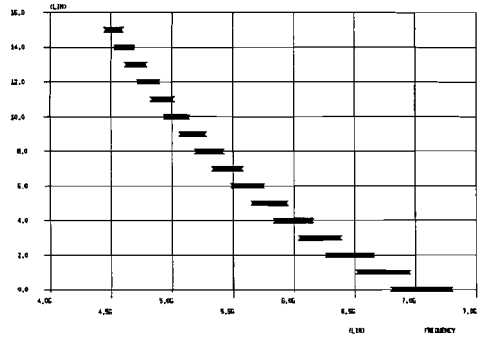

Figure A.2: Original frequency bands of VCO 1

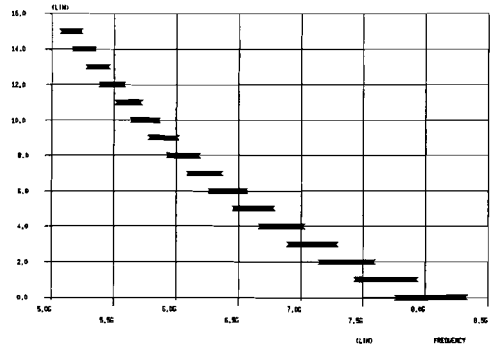

Figure A.3: Frequency bands of VCO 1 shifted to higher frequencies

Table A.2: Process spread absolute values

Shift direction	Frequency [MHz]		Overlap [MHz]	
	f_{b15}	f_{e0}	$F_{ov_{0,1}}$	$F_{ov_{14,15}}$
down	3993	6556	120	34.6
nominal	4465	7330	134	38.7
up	5093	8362	153	44.2

Table A.3: Band overlap

shift direction	σ_m [%]	Overlap [MHz]			
		$F_{ov_{0,1}}$		$F_{ov_{14,15}}$	
		min	max	min	max
down	0.25	118	122	34.1	35.2
	0.5	116	124	33.6	35.8
	1	113	127	32.5	37.1
nominal	0.25	132	136	38.1	39.4
	0.5	130	138	37.5	40.1
	1	126	143	36.3	41.4
up	0.25	151	155	43.5	45.0
	0.5	148	158	42.8	45.7
	1	144	163	41.5	47.3

$f_{b_{15}}$ is the start frequency of band number 15 and f_{e_0} is the end frequency of band number 0. The frequency overlap between band 0 and 1 is referred to as $F_{OV_{0,1}}$ and the overlap between band 14 and 15 as $F_{OV_{14,15}}$.

A.2 Frequency bands of the second example VCO

Calculation of capacitor array of second example VCO:

$$f_{min} = \frac{5850.10^6}{(\sqrt{0.8 * 0.96})^{-1}} \approx 5100\text{MHz} \tag{A.1}$$

$$f_{max} = \frac{5950.10^6}{(\sqrt{1.2 * 1.04})^{-1}} \approx 6700\text{MHz} \tag{A.2}$$

Assume $C_p + C_f \geq 80\text{fF}$, $L = 1.08nH$. Furthermore, $N = 3$ with binary weighted capacitors, which results in 8 frequency bands.

$$C_{min,tot} = \frac{1}{(2\pi f_{max})^2 L} \approx 522fF, \qquad C_{max,tot} = \approx 902fF \tag{A.3}$$

$$C_{min,tot} = C_p + C_{a,min} + C_{v,min} \tag{A.4}$$

$$C_{max,tot} = C_p + C_{a,max} + C_{v,max} \tag{A.5}$$

$$C_{a,min} = C_{sw,off}(2^N - 1), \qquad C_{a,max} = C_{sw,on}(2^N - 1) \tag{A.6}$$

Now we choose: $C_{sw,off} = 15\text{fF}$ and $C_{sw,on} = 55\text{fF}$. Then $C_{v,min} = 100\text{fF}$ and $C_{v,max} = 200\text{fF}$. Now the residual capacitance can be calculated: $C_f + C_p = 317\text{fF}$.

Table A.4 gives the nominal operating frequencies of the 16 frequency bands of the first example VCO [4]. The figures A.4, A.5 and A.6 on the next page give the frequency bands of the VCO for the cases that the bands are shifted down, up as well as the nominal case. Table A.5 and A.6 give the results of performed statistical simulations.

Table A.4: Frequencies of the frquency bands of VCO example 2

Band number	f_b [MHz]	f_c [MHz]	f_e [MHz]	Span [MHz]	K_{vco} [MHz/V]
0	6141	6422	6703	563	313
1	5952	6206	6468	508	282
2	5780	6011	6242	462	257
3	5622	5833	6044	422	234
4	5477	5671	5864	384	213
5	5342	5521	5700	358	199
6	5216	5382	5548	332	184
7	5099	5254	5408	309	172

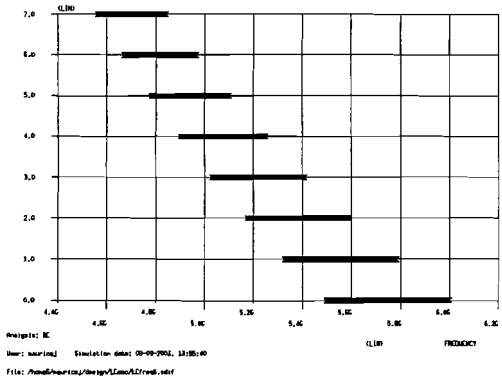

Figure A.4: Frequency bands of VCO 2 shifted to lower frequencies

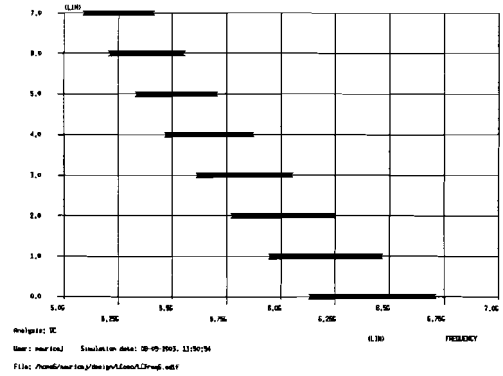

Figure A.5: Original frequency bands of VCO 2

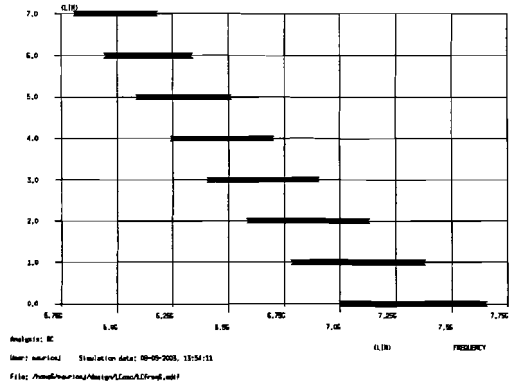

Figure A.6: Frequency bands of VCO 2 shifted to higher frequencies

Table A.5: Start frequency of the frequency bands of interest (absolute spread)

shift direction	Frequency band number	Start frequency [MHz] min	max
down	0	5473	5520
	1	5306	5349
up	6	5929	5978
	7	5797	5843

Table A.6: Frequency band spacing, with $\sigma_m = 1\%$ (absolute+relative spread)

shift direction	Frequency spacing [MHz] $F_{s_{0,1}}$ min	max	$F_{s_{6,7}}$ min	max
down	165	172		
up			131	136

Appendix B

PLL model

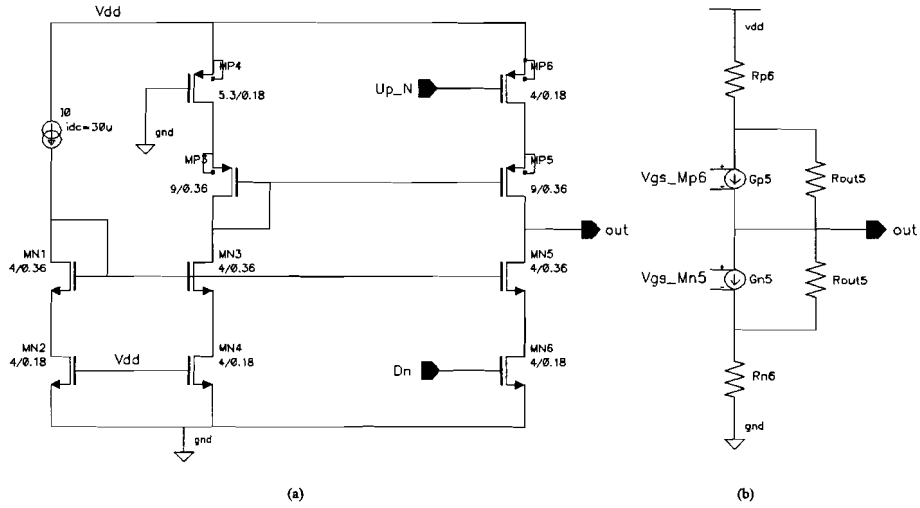

Figure B.1: (a) A charge-pump in CMOS18, (b) equivalent circuit model of the output stage

B.1 Charge-pump model

B.1.1 Realization in CMOS18

Figure B.1(a) shows a charge-pump with source-switched MOS current sources together with the bias circuitry [7]. MN6 and MP6 operate in deep triode region and behave like a resistor. When the current sources (MN5 and MP5) are switched on, they operate in triode or saturation region, depending on the output voltage of the CP (= V_{LF}). If the MOS current source operates in triode region, the output current will be limited. Figure B.1(b) shows a simple equivalent circuit model of the output stage of the CP.

B.1.2 Behavioral model

The behavioral model of the CP is derived from the charge-pump output stage model and will consist of two controlled current sources. One pumping current and the other sinking current, depending on the "UP" and "DOWN" input signals. Both current sources are matched. So, the the mismatch output current will be *zero*. In the CMOS18 model, the transistors exhibit triode, saturation and off regions of operation. The Verilog behavioral model will approximate the off-region with an open circuit, therefore the leak output current of this CP will also be *zero*. Furthermore, the triode and saturation region are modelled using the following formulas.
If the MOS operates in the triode region, the following equation will be used [6]:

$$I_{d_{triode}} = \beta_1 \left[(V_{gs} - V_{th}) V_{ds} - \frac{1}{2} V_{ds}^2 \right] \tag{B.1}$$

If the MOS operates in saturation region, the following equation will be used [6]:

$$I_{d_{saturation}} = \beta_2 \left(V_{gs} - V_{th} \right)^2 (1 + \lambda V_{ds}) \tag{B.2}$$

Assume V_{gs} is independent of V_{out} and $V_{gs} - V_{th} = V_x$, then V_x is the output voltage at which the MOST goes from triode region to saturation region or opposite. At this point: $V_{ds} = V_x$ and $I_{d_{triode}} = I_{d_{saturation}}$, therefore

$$I_{out}\big|_{V_{ds}=V_x} = I_d \tag{B.3}$$

$$\beta_1 = \frac{2I_d}{V_x^2} \qquad \beta_2 = \frac{I_d}{V_x^2 + \lambda V_x^3} \tag{B.4}$$

In the Verilog CP model the parameters I_d (CP output current, I_{CP}) and V_x can be changed.

B.1.3 Simulation results

This section will give the simulation results of the charge-pump model in CMOS18 and the behavioral model. Figure B.2 gives the UP current as a function of output voltage, for the CMOS18 and Verilog model. Figure B.3 gives the DOWN current as a function of the output voltage and figure B.4 gives the the leak current when the output is high impedant, also for CMOS18 and the behavioral model. Figure B.5 gives a transient response of the output current, when the loop-filter voltage is constant and figure B.6 gives a transient of the output current and loop-filter voltage of the Verilog behavioral model.

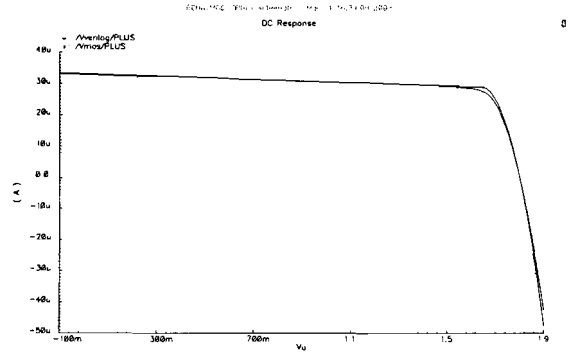

Figure B.2: UP current as a function of output voltage, for the CMOS18 and Verilog model

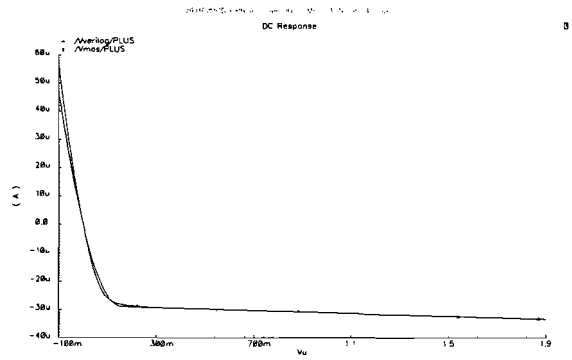

Figure B.3: DOWN current as function of the output voltage, for the CMOS18 and Verilog model

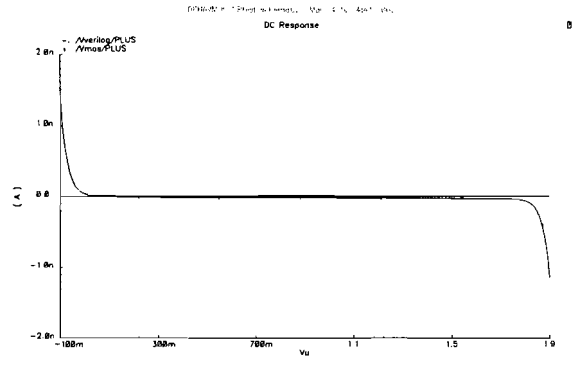

Figure B.4: Leak current when both inputs are not active, for the CMOS18 and Verilog model (= *zero*)

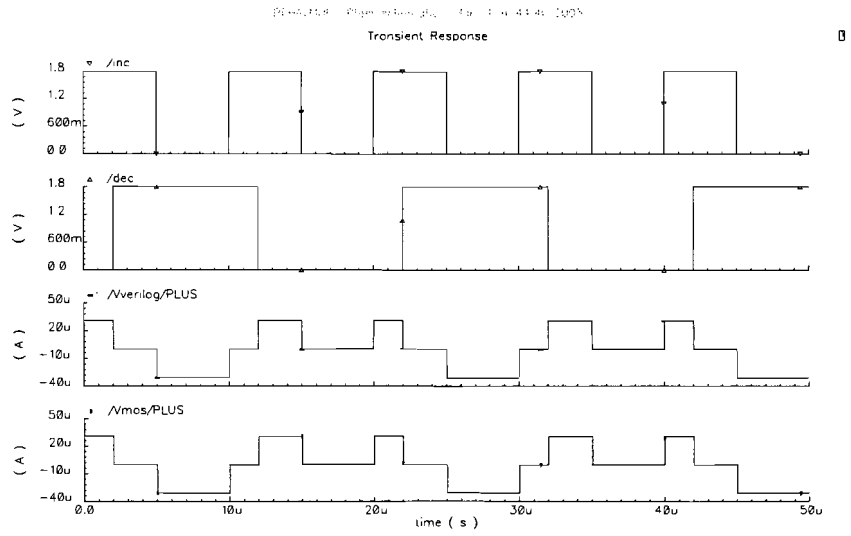

Figure B.5: Transient response: Output current as function of inputs: inc=UP and dec=DOWN, for CMOS18 (Vmos/PLUS) and Verilog model (Verilog/PLUS)

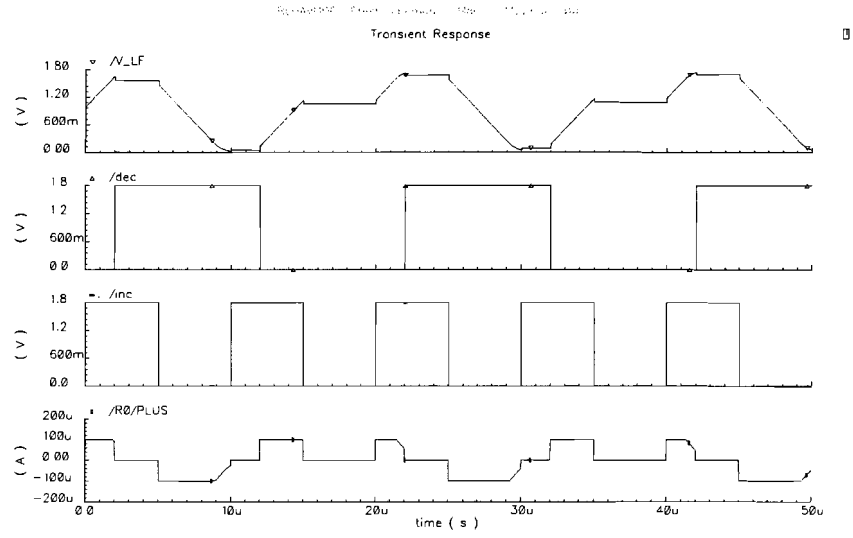

Figure B.6: Transient response: Output current (R0/PLUS) and LF voltage (V_LF) as function of inputs: inc and dec. The used loop-filter consists of a RC combination, therefore V_{LF} exhibits voltage jumps at changes of the CP output current

B.2 Loop filter calculation

This section describes the way to calculate the values of the loop-filter components for the PLL used in the simulation (all formulas from [8]).

The PLL model in Verilog and Cadence uses a second-order loop-filter. The transfer function of this loop filter can be written as

$$Z_{lf}(s) = \frac{k}{s}\frac{1+s\tau_2}{1+s\tau_3} \tag{B.5}$$

where k is a gain factor, τ_2 is the time constant for the stabilizing zero and τ_3 is the time constant of the pole which is used to attenuate the reference frequency and its harmonics. The relationship between the component values in the filter and the design parameters can be found in tabel B.1.

The open- and closed-loop transfer functions G(s) and H(s) can be derived with the linear phase domain model of a PLL, wich is shown in figure B.7. The loop consists of a VCO with a gain K_{vco} [Hz/V], a programmable frequency divider with a divider ratio N, a phase-frequency detector / single ended charge-pump combination (PFD/CP) with a combined gain $K_{pfd} = I_{cp}/2\pi$, and a loop-filter with a trans-impedance transfer function Z_{lf}. The open-loop transfer function is expressed as

$$\begin{aligned} G(s) &= K_{pfd}Z_{lf}(s)\frac{2\pi K_{vco}}{s}\frac{1}{N} \\ &= \frac{I_{cp}}{2\pi}Z_{lf}(s)\frac{2\pi Kvco}{s}\frac{1}{N} \end{aligned} \tag{B.6}$$

Table B.1: Relationship design parameters and component values [8]

Parameter	Loop filter components
τ_2	R_1C_1
τ_3	$R_1\frac{C_1C_2}{C_1+C_2}$
k	$\frac{1}{C_1+C_2}$

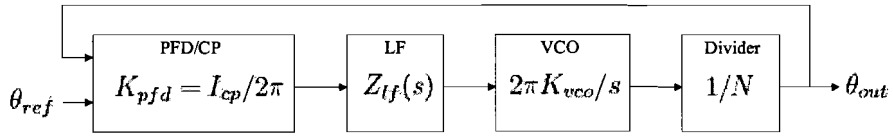

Figure B.7: Linear model of a PLL[8]

The closed loop gain can be expressed as

$$\begin{aligned} H(s) &= \frac{G(s)}{1+G(s)} \\ &= \frac{2\pi K_{pfd} Z_{lf}(s) K_{vco}/N}{s + 2\pi K_{pfd} Z_{lf}(s) K_{vco}/N} \end{aligned} \tag{B.7}$$

The open loop bandwidth f_c is defined by the condition: $|G(j2\pi f_c)| = 1$ and phase margin: $\phi_m = arg(G(j2\pi f_c)) + \pi$. Now the open-loop gain equation for $G(j\omega)$ can be written as

$$\begin{aligned} G(j\omega) &= -\frac{I_{cp} K_{vco} k}{N\omega^2} \frac{1+j\omega\tau_2}{1+j\omega\tau 3} \\ &= -\frac{I_{cp} K_{vco} k}{N\omega^2} \frac{1+j\omega\tau_2}{1+j\omega\tau_2/b} \end{aligned} \tag{B.8}$$

where b is

$$b = \frac{\tau_2}{\tau_3} = 1 + \frac{C_1}{C_2} \tag{B.9}$$

The phase of the transfer function $G(j\omega)$ from B.12 will be denoted as $\Psi(j\omega)$

$$\begin{aligned} \Psi(j\omega) &= -\pi arg(1+j\omega\tau_2) - arg(1+j\omega\tau_3) \\ &= -\pi + arctan(\omega\tau_2) - arctan(\omega\tau_3) \end{aligned} \tag{B.10}$$

and the point of the of zero derivative of the phase response will be called ω_{max}. This gives

$$\omega_{max} = \sqrt{\frac{1}{\tau_2\tau_3}} \tag{B.11}$$

So, the frequency of maximum phase advance lies at the geometrical average of the inverse of time constants τ_2 and τ_3. The value of the maximum phase advance $\phi_{max} + \pi$ at $\omega = \omega_{max}$ can be calculated as a function of τ_2, τ_3 and $b = \tau_2/\tau_3$ by inserting in B.10 and B.11

$$\begin{aligned} \phi_{max} &= arctan\frac{\tau_2 - \tau_3}{2\sqrt{\tau_2\tau_3}} \\ &= arctan\frac{b-1}{2\sqrt{b}} \end{aligned} \tag{B.12}$$

Solving B.12 for b as a function of ϕ_{max} yields

$$b = \frac{1}{(-tan\phi_{max} + 1/cos\phi_{max})^2} \tag{B.13}$$

Which results in

$$\tau_2 = \frac{\sqrt{b}}{\omega_c} \tag{B.14}$$

$$\tau_3 = \frac{1}{\sqrt{b}\omega_c} \tag{B.15}$$

And therefore the values of the loop-filter components can be calculated

$$R_1 = \frac{N\omega_c}{I_{cp}K_{vco}}\frac{b}{b-1} \tag{B.16}$$

$$C_1 = \frac{\tau_2}{R_1} \tag{B.17}$$

$$C_2 = \frac{1}{R_1}\frac{\tau_2\tau_3}{\tau_2 - \tau_3} \tag{B.18}$$

B.3 Open-loop simulation results

Figure B.8 shows the drawback of the architecture given in figure 2.10, the delay time for the loop-filter voltage to go to V_{ss} is approximately 2μs. Figure B.9 gives the transient response of the architecture given in figure 2.11. Figure B.10 shows the discharge time of the loop-filter. The worst case delay time is approximately 30ns.

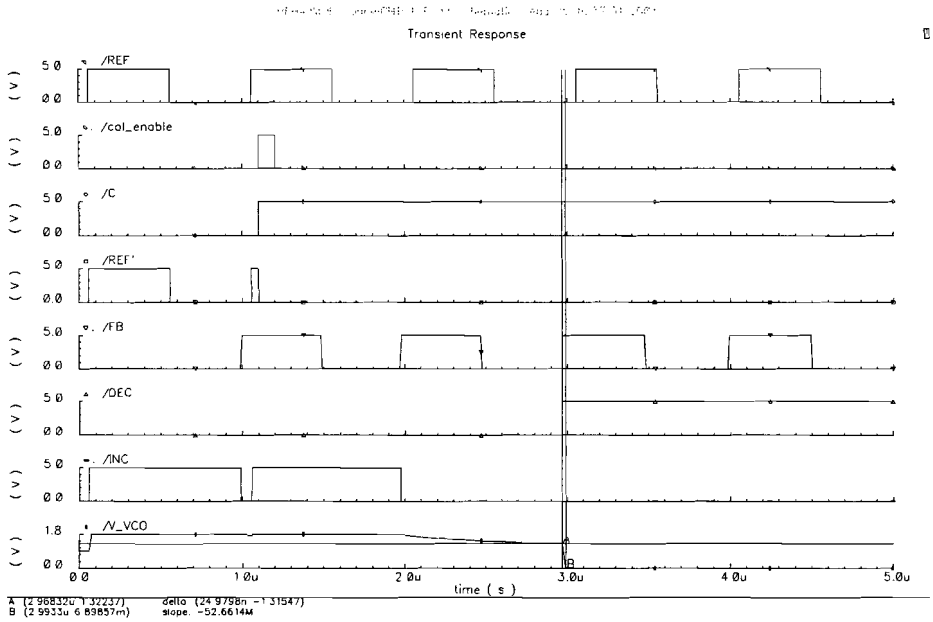

Figure B.8: Transient response: The frequency of REF is 1MHz and REF' is the signal after the switch, which is controlled by signal C, the frequency of the feedback signal (FB) is also 1MHz. The delay time for the loop-filter voltage (V_VCO) to go to V_{ss} is approximately 2μs. Marker A and B show the discharge time of capacitor C_2 in the loop-filter.

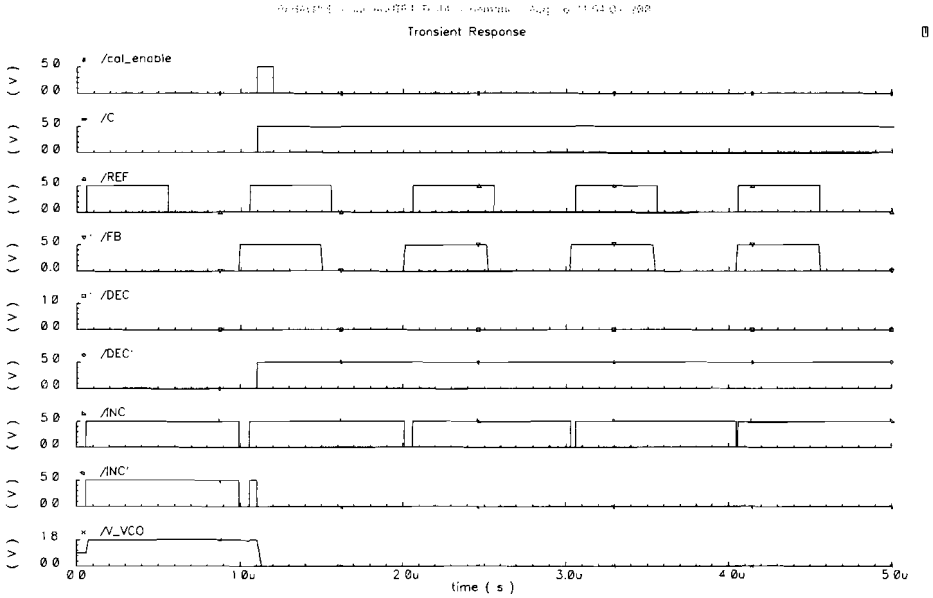

Figure B.9: Transient response: The frequency of REF and FB is 1MHz. Control signal C switches signal DEC to V_{dd} and INC to V_{ss}. The delay time for the loop-filter voltage (V_VCO) to go to V_{ss} is approximately 30ns.

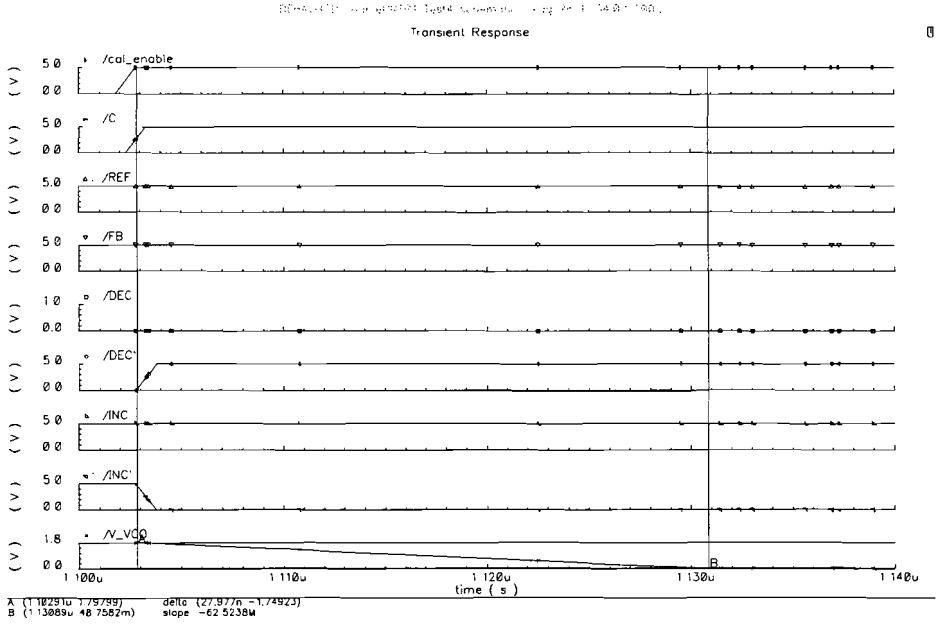

Figure B.10: Transient response: Marker A and B show the discharge time of capacitor C_2 in the loop-filter.

Appendix C

DLQ

This appendix shows some additional simulation results of the digital logic quadricorrelator. First of all, the schematic of the balanced quadricorrelator is given. Figure C.2 gives a simulation result for the case that $f_{VCO} > f_{REF}$. In figure C.3, $f_{VCO} > f_{REF}$ is also the case, but the frequency difference between the VCO signal and the reference signal is less than in the previous case. Finally, $f_{VCO} < f_{REF}$ and the DLQ is out of its operating range, therefore generating spurious output signals (illustrated in figure C.4).

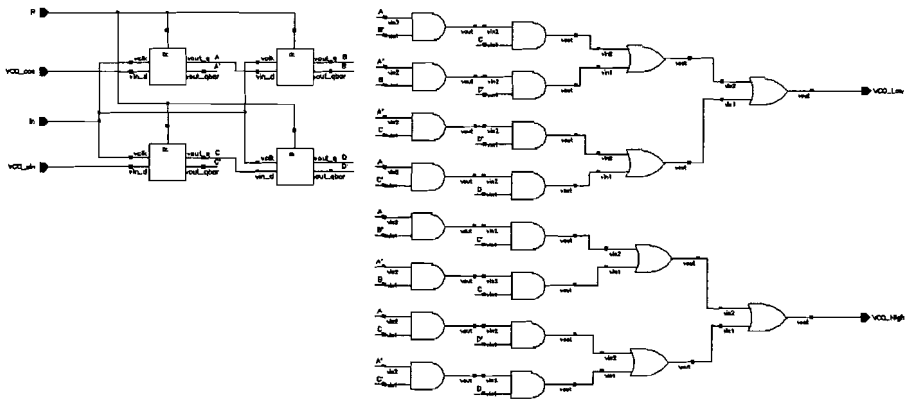

Figure C.1: Schematic of balanced digital quadricorrelator [9]

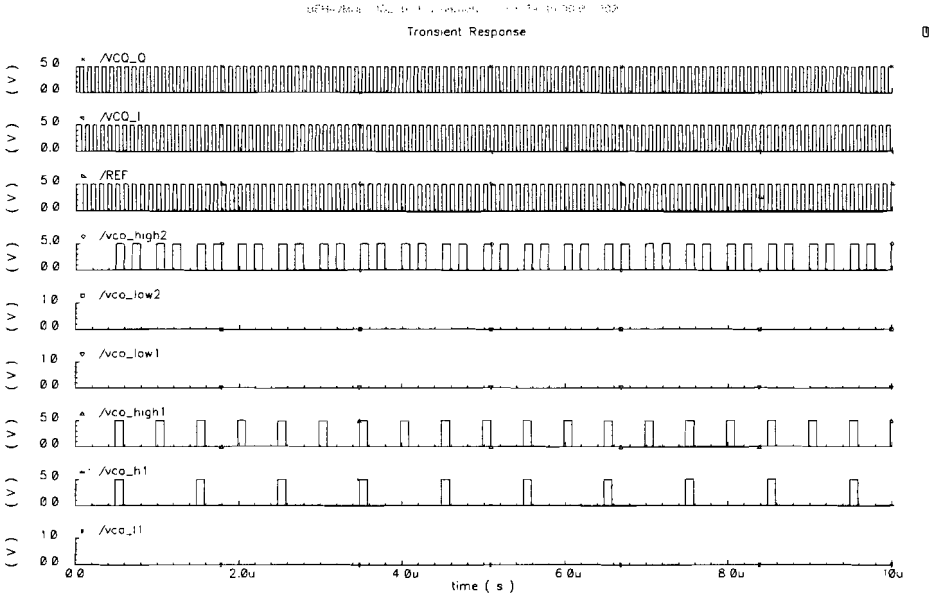

Figure C.2: Simulation result of the DLQ: $f_{VCO} > f_{REF}$, VCO_high2 is the output of the balanced DLQ(2), VCO_high1 is the output of the "normal" DLQ and VCO_h1 is the output of AND-gate no. 5 (see figure 3.10). Conclusion: the detector gain of DLQ2 is twice the gain of DLQ1.

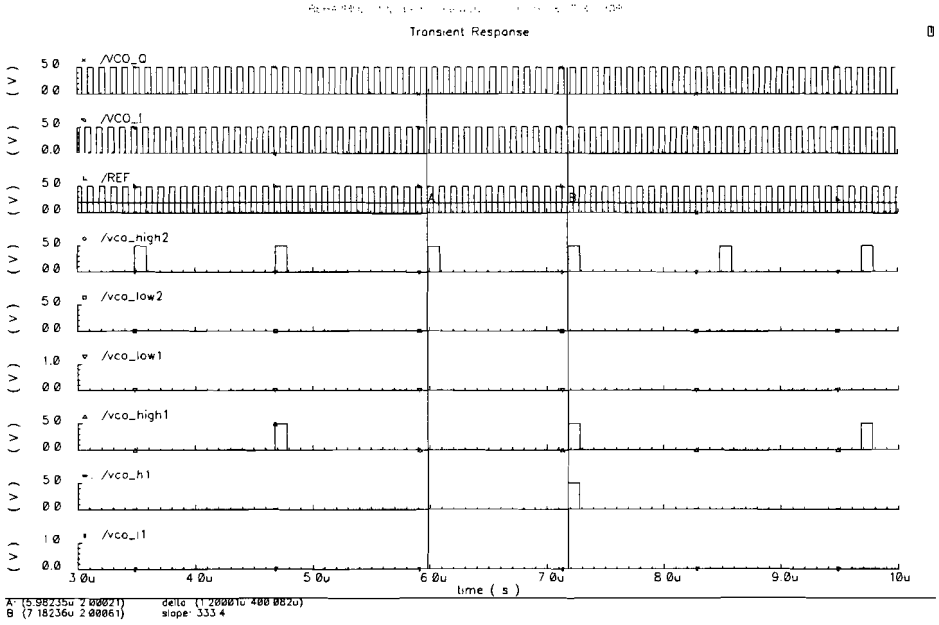

Figure C.3: Simulation result of the DLQ: f_{VCO} = 10.2MHz and f_{REF} = 10.0MHz, the frequency difference is 200kHz. The expected time between two output pulses of the balanced DLQ2 is: $\frac{1}{4*200k} = 1.25\mu s$, but the measured time is $1.2\mu s$ due to the discrete sampling character of the DLQ.

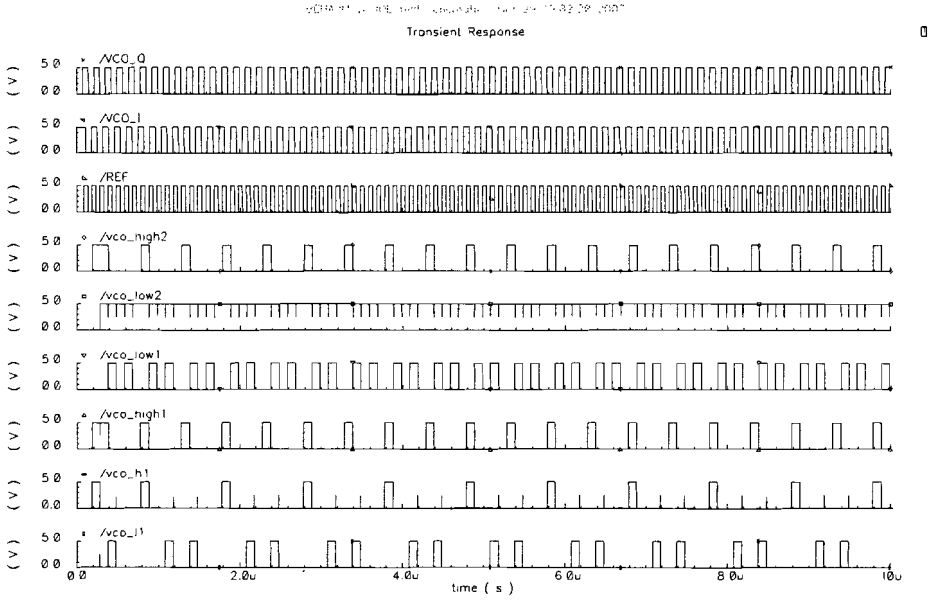

Figure C.4: Simulation result of the DLQ: $f_{VCO} < f_{REF}$, but the frequency difference is to large, resulting in spurious output on the "high" outputs of the DLQ

Appendix D

Coarse frequency control

D.1 States of the state-machine in the variable divider system with counter

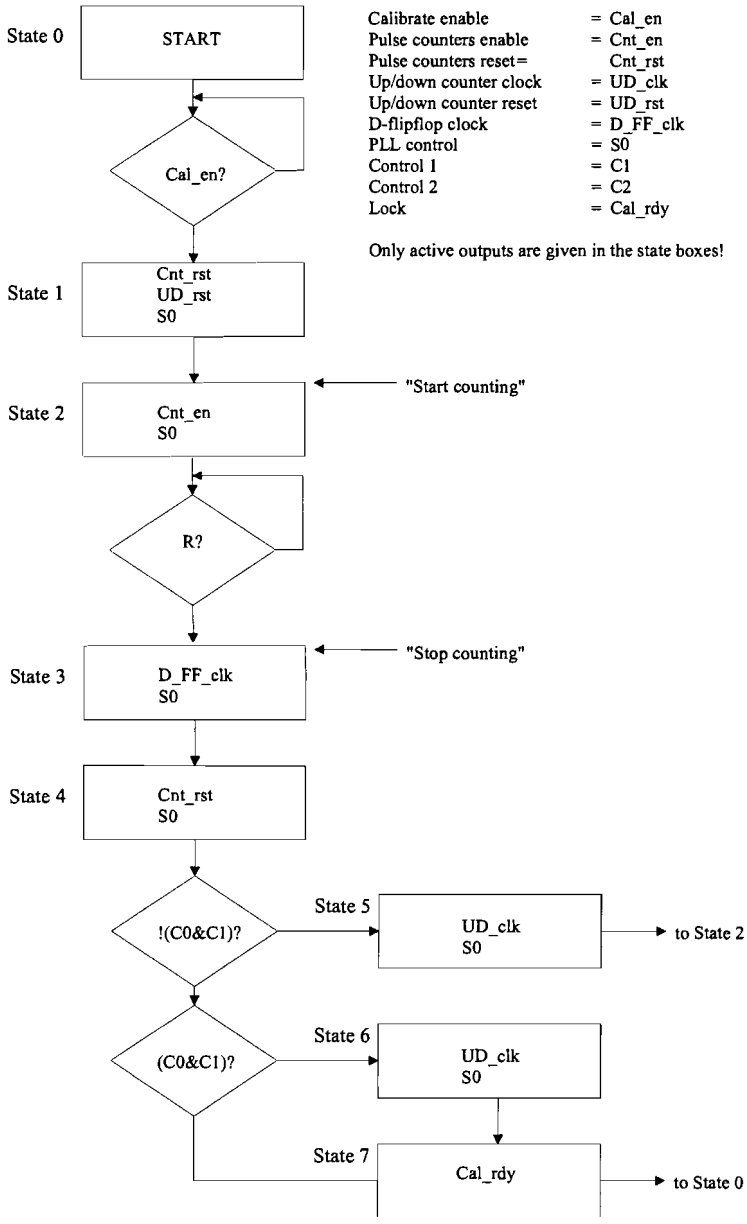

Figure D.1: States of the state-machine in the variable divider system with counter

Appendix E

Frequency spread calibration

E.1 States of the state-machine in the FSC

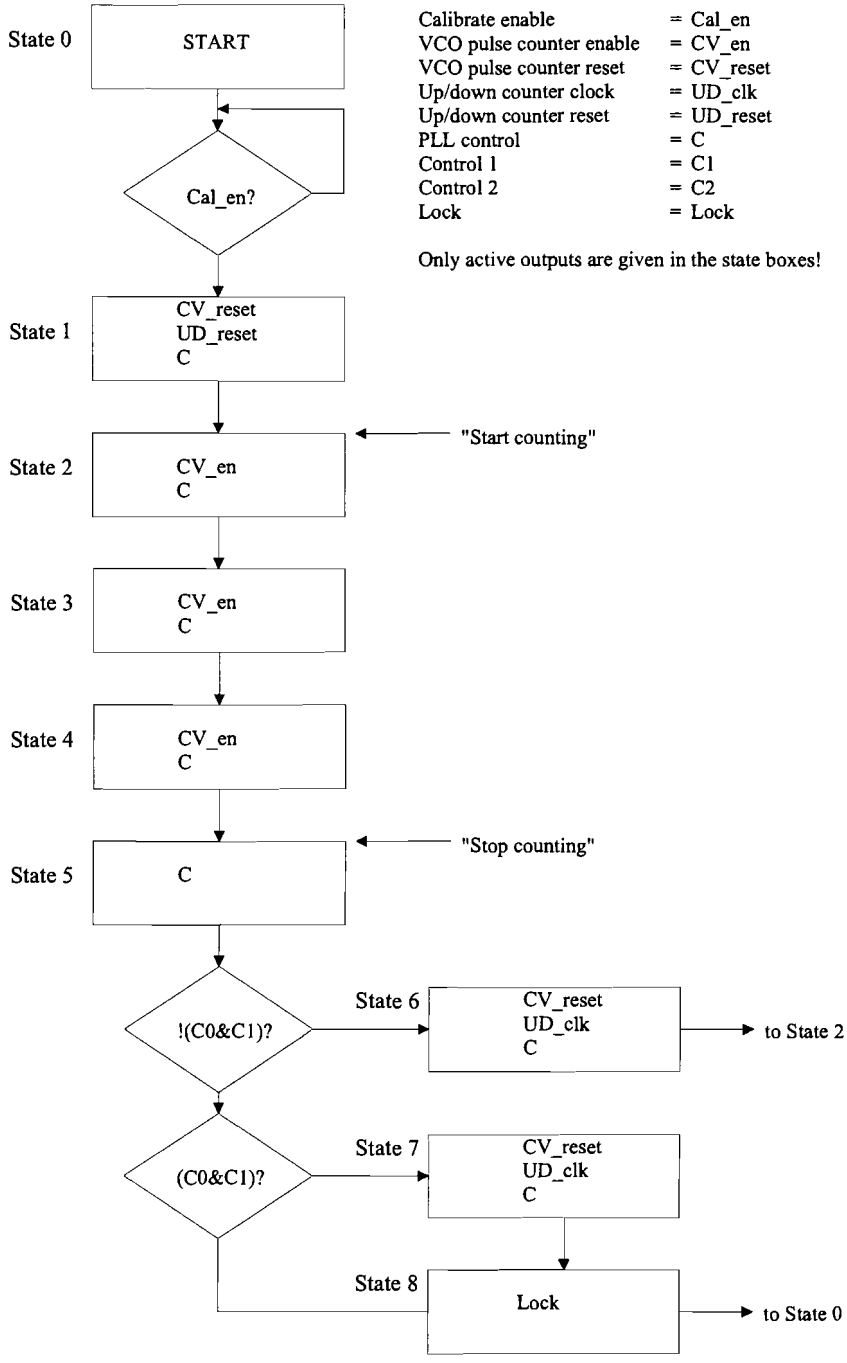

Figure E.1: State diagram of the state-machine

Appendix F

Predecessor FSC system

F.1 Five Lock methods

The next sections describe five different lock methods, while the factor $F = N\Delta f_{det}$ is kept the same. Furthermore the assumption is made that F_s and F_r is constant for the frequency bands, even if the frequency bands shift up or down due to process spread.

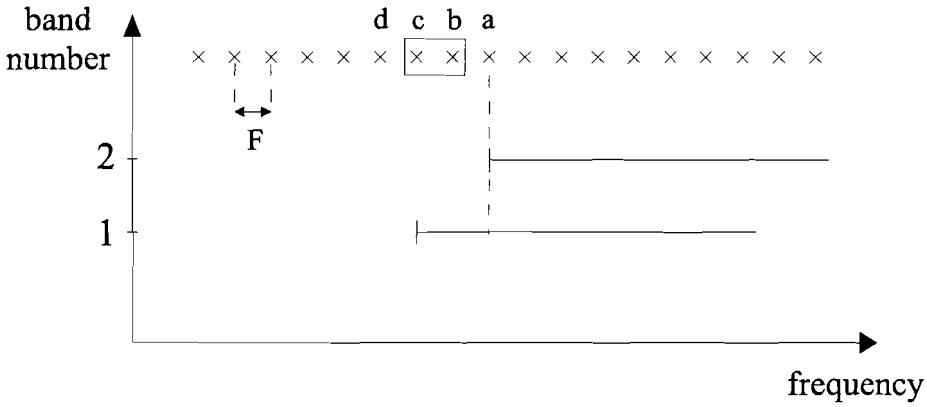

Figure F.1: Method 1: two frequency bands of an oscillator in combination with the desired frequency range and the lock range between marked points 'b' and 'c'.

Method 1: Lock between f_b and f_c
Figure F.1 shows the first method: The desired frequency range starts at the detectable frequency marked with a (this frequency will be called f_a). The lock range is situated between the points marked with 'b' and 'c' or between f_b and f_c. Detection of f_a results in up&lock and detection of f_d results in down&lock, see table F.1.
If the start of frequency band 1 is slightly lower than f_c, point 'd' can be detected and this results in an up&lock action. So, band 2 can be selected and this band must cover the desired frequency range.

Therefore the upper boundary for the frequency band spacing between band 1 and 2, F_s, is given by

$$F_s \leq 2N\Delta f_{det} \tag{F.1}$$

If the start of frequency band 1 is slightly higher than f_d, point 'c' can be detected, which results in a lock. Therefore the frequency range that band 1 must cover is

$$F_r \geq 3N\Delta f_{det} + F_{desired} \tag{F.2}$$

In addition, if the start of frequency band 2 is slightly higher than f_b, point 'a' can be detected and this results in a down&lock action. Thus, band 1 must cover the desired frequency range. Therefore a second requirement for the frequency range of the frequency bands is drawn up

$$F_r \geq N\Delta f_{det} + F_s + F_{desired} \tag{F.3}$$

The frequency band spacing F_s must satisfy the given boundary in equation F.1, therefore F_s is always smaller than $2N\Delta f_{det}$. Thus, the minimum frequency range requirement given in F.3 is always true if F_r satisfies equation F.2. The band requirements given in equation F.1 and F.2 can also be found in table F.2, which gives an overview of the five mentioned lock methods together with the requirements for the frequency bands.

Method 2: Lock between f_c and f_d
The second method is illustrated in figure F.2(a). The desired frequency range starts at f_a and the lock range is between f_c and f_d. Detection of f_b results in down&lock and f_e results in up&lock, see table F.1. The upper boundary for F_s can be derived in a way similar to the first method, this results in

$$F_s \leq 3N\Delta f_{det} \tag{F.4}$$

Another way of looking at the upper boundary for F_s is: whenever a start of a frequency band lays in the range between f_b and f_e the digital control loop will get into lock. Therefore the F_s may never be bigger than $f_b - f_e$. This sets an upper boundary of $3N\Delta f_{det}$, which is accidentally the same as the boundary in (F.1).

The requirements for the frequency range of the frequency bands can be derived in a way similar to method 1, this results in

$$F_r \geq 4N\Delta f_{det} + F_{desired} \tag{F.5}$$

$$F_r \geq 2N\Delta f_{det} + F_s + F_{desired} \tag{F.6}$$

The band requirements given in equation F.4, F.5 and F.6 can also be found in table F.2.

Method 3: Lock between f_b and f_d
The third case is shown in figure F.2(b). The desired frequency range starts at

f_a and the lock range is between f_c and f_e. Detection of f_b results in down&lock and f_f results in up&lock, see table F.1. The upper boundary for F_s is given by

$$F_s \leq 3N\Delta f_{det} \tag{F.7}$$

The frequency range requirements are given by

$$F_r \geq 4N\Delta f_{det} + F_{desired} \tag{F.8}$$

$$F_r \geq N\Delta f_{det} + F_s + F_{desired} \tag{F.9}$$

The frequency band spacing F_s must satisfy the given boundary in equation F.7, therefore F_s is always smaller than $3N\Delta f_{det}$. Thus, the minimum frequency range requirement given in F.9 is always true, in the case that F_r satisfies equation F.8. The band requirements given in equation F.7 and F.8 can also be found in table F.2.

Method 4: Lock between f_c and f_e
The fourth case is shown in figure F.2(c). The desired frequency range starts at f_a and the lock range is between f_c and f_e. Detection of f_b results in down&lock and f_f results in up&lock, see table F.1. The upper boundary for F_s is given by

$$F_s \leq 4N\Delta f_{det} \tag{F.10}$$

The minimum frequency range requirements are given by

$$F_r \geq 5N\Delta f_{det} + F_{desired} \tag{F.11}$$

$$F_r \geq 2N\Delta f_{det} + F_s + F_{desired} \tag{F.12}$$

The band requirements given in equation F.4, F.5 and F.6 can also be found in table F.2.

Method 5: Lock between f_b and f_e
The fifth case is shown in figure F.2(d). The desired frequency range starts at f_a and the lock range is between f_b and f_e. Detection of f_a results in down&lock and f_f results in up&lock, see table F.1. The upper boundary for F_s is given by

$$F_s \leq 4N\Delta f_{det} \tag{F.13}$$

The minimum frequency range requirements are given by

$$F_r \geq 5N\Delta f_{det} + F_{desired} \tag{F.14}$$

$$F_r \geq N\Delta f_{det} + F_s + F_{desired} \tag{F.15}$$

The frequency band spacing F_s must satisfy the given boundary in equation F.13, therefore F_s is always smaller than $4N\Delta f_{det}$. Thus, the minimum frequency range requirement given in F.9 is always true, in the case that F_r satisfies equation F.8. The band requirements given in equation F.7 and F.8 can also be found in table F.2, which gives a summary of the band requirements for F_s and F_r for the five mentioned lock methods.

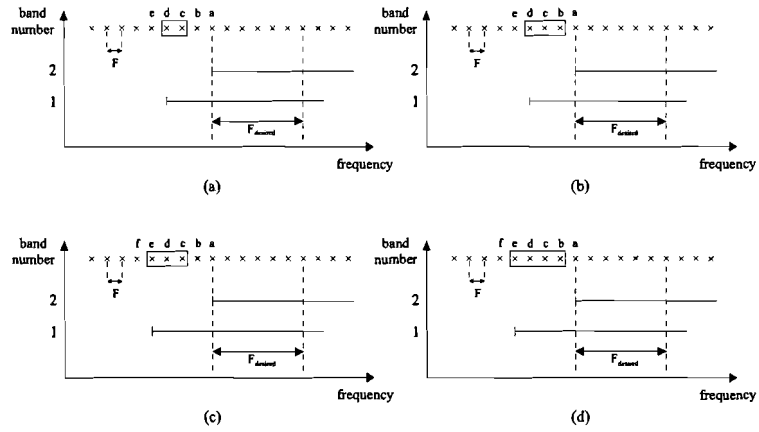

Figure F.2: Four different lock methods: (a) Method 2: the lock range is situated between marked points 'c' and 'd' (b) Method 3: lock range between 'b' and 'd' (c) Method 4: lock range between 'c' and 'e' (d) Method 5: lock range between 'b' and 'e'.

Table F.1: Actions for the five lock methods

	Detected point					
Method	a	b	c	d	e	f
1	D+L	L	L	U+L	U	U
2	D	D+L	L	L	U+L	U
3	D+L	L	L	L	U+L	U
4	D	D+L	L	L	L	U+L
5	D+L	L	L	L	L	U+L
Action	D = band down, L = lock and U = band up					

Table F.2: Band requirements for the five different lock methods

Method	$F_s \leq$	$F_r \geq$	$F_r \geq$
1	$2N\Delta f_{det}$	$3N\Delta f_{det} + F_{desired}$	
2	$3N\Delta f_{det}$	$4N\Delta f_{det} + F_{desired}$	$2N\Delta f_{det} + F_s + F_{desired}$
3	$3N\Delta f_{det}$	$4N\Delta f_{det} + F_{desired}$	
4	$4N\Delta f_{det}$	$5N\Delta f_{det} + F_{desired}$	$2N\Delta f_{det} + F_s + F_{desired}$
5	$4N\Delta f_{det}$	$5N\Delta f_{det} + F_{desired}$	

F.2 Design of predecessor FSC system

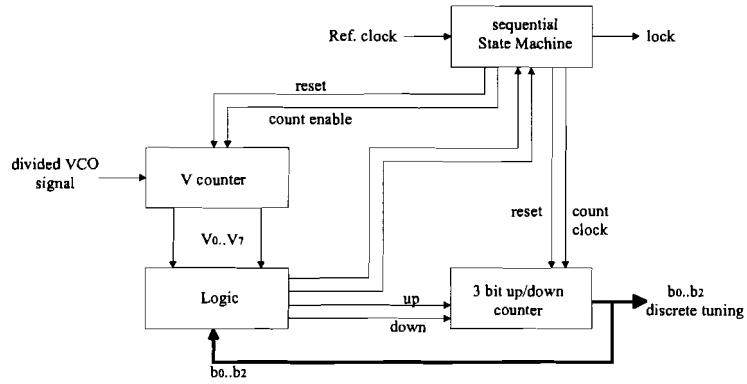

Figure F.3: Block schematic of FSC system, with band dependance

Table F.3: Logic table: Action and outputs (C0, C1, UP and DOWN) as function of *band number* and counter value

Band	Counter value	Action	C_1 C_0	UP DOWN
0	≤ 116	Lock	11	00
	117	Counter up + Lock	10	10
	≥ 118	Counter up	00	10
1-5	≤ 111	Counter down	00	01
	112	Counter down + Lock	01	01
	113-116	Lock	11	00
	117	Counter up + Lock	10	10
	≥ 118	Counter up	00	10
6	≤ 112	Counter down	00	01
	113	Counter down + Lock	01	01
	114-116	Lock	11	00
	117	Counter up + Lock	10	10
	≥ 118	Counter up	00	10
7	≤ 112	Counter down	00	01
	113	Counter down + Lock	01	01
	≥ 114	Lock	11	00

The safety margin M = $\pm$ 10MHz, reference frequency f_{ref} = 10MHz, divider ratio N = 10 and Δf_{det} = 5MHz. Tables F.4 and F.5 show that for band number 6 and 7 method 3 will be used and for band number 0 to 5 method 5.

Table F.4: F_r, Method conditions and possible method as function of band number X: 1 to 7

X	$F_{r_X} - F_D$ [MHz]	$F_{r_X} - F_D - M$	$\geq$	Method
1	384	374	$5\Delta f_{det}$	1,2,3,4,5
2	354	344	$5\Delta f_{det}$	1,2,3,4,5
3	327	317	$5\Delta f_{det}$	1,2,3,4,5
4	300	290	$5\Delta f_{det}$	1,2,3,4,5
5	282	272	$5\Delta f_{det}$	1,2,3,4,5
6	264	252	$5\Delta f_{det}$	1,2,3,4,5
7	247	237	$4\Delta f_{det}$	1,2,3

Table F.5: F_s, Method conditions and possible method as function of band number X: 1 to 7

X	F_{s_X} [MHz]	$F_{s_X} + M$	$\leq$	Method
1	180	190	$4\Delta f_{det}$	4,5
2	169	179	$4\Delta f_{det}$	4,5
3	160	170	$4\Delta f_{det}$	4,5
4	151	161	$4\Delta f_{det}$	4,5
5	145	155	$4\Delta f_{det}$	4,5
6	138	148	$3\Delta f_{det}$	2,3
7	130	140	$3\Delta f_{det}$	2,3