Design of a 10 bit 1 Gsample/s Track- and- Hold Circuit

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Report of the graduation project
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Company supervisors:Ir. P. Vorenkamp and Dr. ir. R. Roovers

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Eindhoven, August 1996,

Maurits Storms.

Abstract

In this report the design of a 10 bit 1 GHz sample rate track-and-hold circuit with a 2 V peak-to-peak signal amplitude is described. The architecture on which the design is based is a single channel differential configuration in order to meet several design specifications. The choice between an interleaved and a single channel configuration is discussed. A new double-poly production process (OBIC) is used and treated, differences between the new and former processes are discussed.

The track-and-hold circuit consists of five subcircuits: an input buffer, a switch with a hold capacitor, an output buffer, a clock buffer and a bias voltage circuit. All these circuits are analyzed and designed by means of simulation. The total circuit has been designed with a distortion below -72 dB over a 500 MHz full-Nyquist bandwidth in order to meet process matching and other non-idealities. Also noise is taken into account. Measurement setup has been proposed and implemented in the layout of the design.

Contents

1 Introduction

In the past few years track-and-hold circuits are widely used in data acquisition and data distribution systems. Due to the rapid increase of the use of digital techniques, the track-and-hold circuit together with the analog-to-digital and digital-to-analog converter are designed for high performance or flexibility. The most important features of these devices are conversion speed and accuracy. Often there is a trade off between speed and resolution, depending on the intended application. The high speed track-and-hold circuits are mostly designed for measuring equipment and video applications.

The basic function of the track-and-hold circuit is to convert a continuous time, continuous amplitude signal into a discrete time, continuous amplitude signal. If the circuit is used as a presampler in front of an analog-to-digital converter, the high frequency performance of the converter can be improved. The track-and-hold circuit can also be used in multiplexed systems and as a deglitcher behind a digital-to-analog converter.

The track-and-hold circuit to be designed here has strict specifications. The device must operate at a 1 GHz sample rate with a 10 bit resolution and handle a 2 V peak-to-peak input signal amplitude. This results in a 500 MHz full-Nyquist bandwidth and overall distortion below -62 dB. To meet these specifications a differential architecture is used in a bipolar IC technology.

Designing a track-and-hold circuit with high performance in several specifications is a difficult task. Precision Monolithic Inc's (PMI) Steve Sockolov said it best: "Designing a track-and-hold is like trying to flatten a waterbed by pushing on it in different places."

As already said there is a trade off between speed and accuracy, but also between speed and power consumption. Not to forget the trade off between speed and circuit complexity, speed and die area or die area and accuracy. All these factors should be seriously taken into account in the design of a track-and-hold circuit.

This report represents the design of the 10 bit resolution, 1 GHz sample rate track-and-hold circuit in a new double-poly bipolar production process (OBIC). First the circuit configuration is treated, after that the new process is described. Then a theoretical analysis of several subcircuits is done whereupon the circuits are verified by simulation and the results are presented. Next the total circuit is designed and tested by means of simulation. At last a test configuration is treated and a layout design is given. Finally some conclusions are drawn.

2 The Track-and-Hold Circuit

2.1 Properties of a Track-and-Hold Circuit

2.1.1 Basic Track-and-Hold Configuration

A track-and-hold circuit is an important part in analog-to-digital converter systems. This circuit converts a continuous time, continuous amplitude signal into a discrete time, continuous amplitude signal. In a track-and-hold circuit two different modes exist, track and hold. In the track mode the output of the circuit "tracks" the input signal which is also the output of the circuit. In the hold mode the output signal is held on the value of the input at the instant the hold instruction was given. This process is periodic as illustrated in Figure 1.

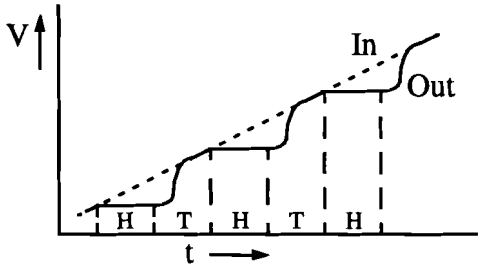


Figure 1 Track-and-hold signals

This function can be realized with a switch and a capacitor as illustrated in Figure 2, in which S is the switch, R is the on-resistance of the switch and C_h is the hold capacitor.

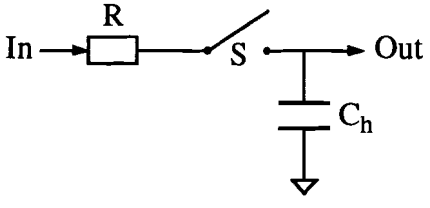


Figure 2 Basic track-and-hold circuit

In order to realize a configuration as in Figure 2 in a practical circuit it is necessary to buffer the circuit with an input and an output buffer. This is done to reduce the influence of external signals on the signals of the track-and-hold circuit and vice versa, which may deteriorate the functioning of the track-and-hold circuit. The circuit with the two unity gain amplifiers is shown in Figure 3.

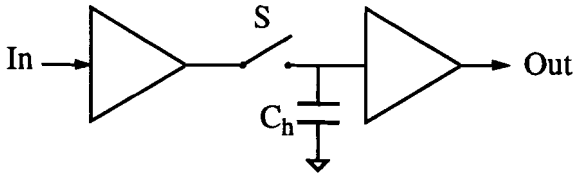


Figure 3 Buffered track-and-hold circuit

2.1.2 Performance Limitations and Artifacts of a Track-and-Hold Circuit

Track-and-hold circuits suffer from several performance limitations and artifacts due to design issues and process technology. The most important issues are listed here:

- signal bandwidth
- acquisition time
- aperture time uncertainty
- noise
- charge injection
- droop
- hold mode feedthrough.

For more information on these issues is referred to [1]. Eventually not all these issues are valid for every track-and-hold circuit configuration. The issues which are valid for the track-and-hold circuit to be designed will be covered later on.

2.2 Design Specifications and Configuration Options

2.2.1 Design Specifications

The track-and-hold circuit to be designed must be able to operate at a sample rate of 1 giga sample per second with a 10 bit accuracy, which is close to -62 dB for the overall distortion. This means that the input signal has a 500 MHz full-Nyquist bandwidth. The input range is 2 V peak-to-peak. The supply voltage is 5 V and the process is a bipolar double-poly process which will be described in the next chapter. For the design of the track-and-hold circuit two options are available:

1. a configuration in which two or more identical track-and-hold circuits are interleaved,

2. a single channel configuration as in Figure 3.

2.2.2 An Interleaved Track-and-Hold Circuit

The sample rate of 1 Gsample/s for the total track-and-hold circuit can be divided over two, in phase shifted, track-and-hold circuits each operating at 500 Msample/s of which the hold modes are merged in a multiplexer [2]. The block diagram of such a circuit is illustrated in Figure 4. The last block is the multiplexer which switches alternating between the two hold modes of the two track-and-hold circuits. This leads to a sample rate that is twice the sample rate of the single channel track-and-hold circuits.

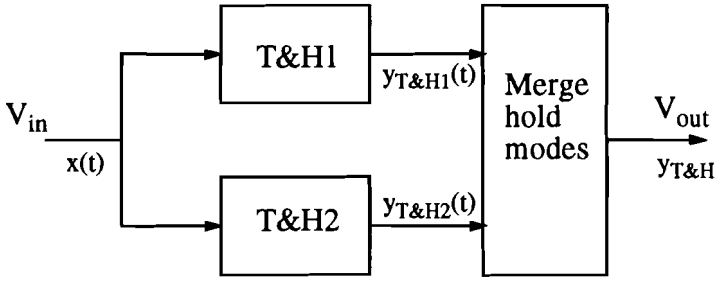


Figure 4 Block diagram of an interleaved track-and-hold circuit

A circuit configuration like this has certain advantages. First the track-and-hold circuits do not need to operate (switch) at 1 GHz sample rate. Second, due to the lower sample rate, the hold capacitors can be larger as a result of a larger acquisition time. This leads to higher accuracy and lower noise, due to a lower droop rate, less influence of charge injection and larger signal power.

Only the hold modes of the track-and-hold circuits are alternating valid at the output of the total circuit. For this reason only the hold modes of the track-and-hold circuits need to be described considering an ideal track mode. The samples are determined by multiplying an input signal $x(t)$ by a periodic train of impulses $\delta(t-kT_s)$ [3]. The hold mode is only a sample convolved with a rectangle function $\Pi(2t/T_s)$. This leads to the following signal equations for the two track-and-hold circuits in time and frequency domain:

$$y_{T\&H1}(t) = \left[x(t) \cdot \sum_{k=-\infty}^{\infty} \delta(t - kT_s)\right] * \prod\left(\frac{2t}{T_s}\right), \tag{1}$$

$$y_{T\&H2}(t) = \left[x(t) \cdot \sum_{k=-\infty}^{\infty} \delta\left(t - kT_s - \frac{1}{2}T_s\right)\right] * \prod\left(\frac{2t}{T_s}\right), \tag{2}$$

$$Y_{T\&H1}(f) = \frac{\sin\left(\pi f \frac{T_s}{2}\right)}{\pi f T_s} \sum_{n=-\infty}^{\infty} X\left(f - \frac{n}{T_s}\right), \tag{3}$$

$$Y_{T\&H2}(f) = \frac{\sin\left(\pi f \frac{T_s}{2}\right)}{\pi f T_s} \sum_{n=-\infty}^{\infty} X\left(f - \frac{n}{T_s}\right) e^{-jn\pi}. \quad (4)$$

From the equations in frequency domain, (3) and (4), it is seen that, in an ideal situation, certain spectral components cancel due to sampling. This is illustrated in Figure 5. In Figure 5(a) the frequency spectrum of a signal with f_{sig} as signal frequency with respect to (3) is shown and in Figure 5(b) the frequency spectrum of f_{sig} with respect to (4) is shown in which the phase shifted peaks are caused by the extra phase shift $e^{-jn\pi}$. In Figure 5(c) the sum of the frequency spectra is shown from which it is concluded that the sample rate is multiplied by two.

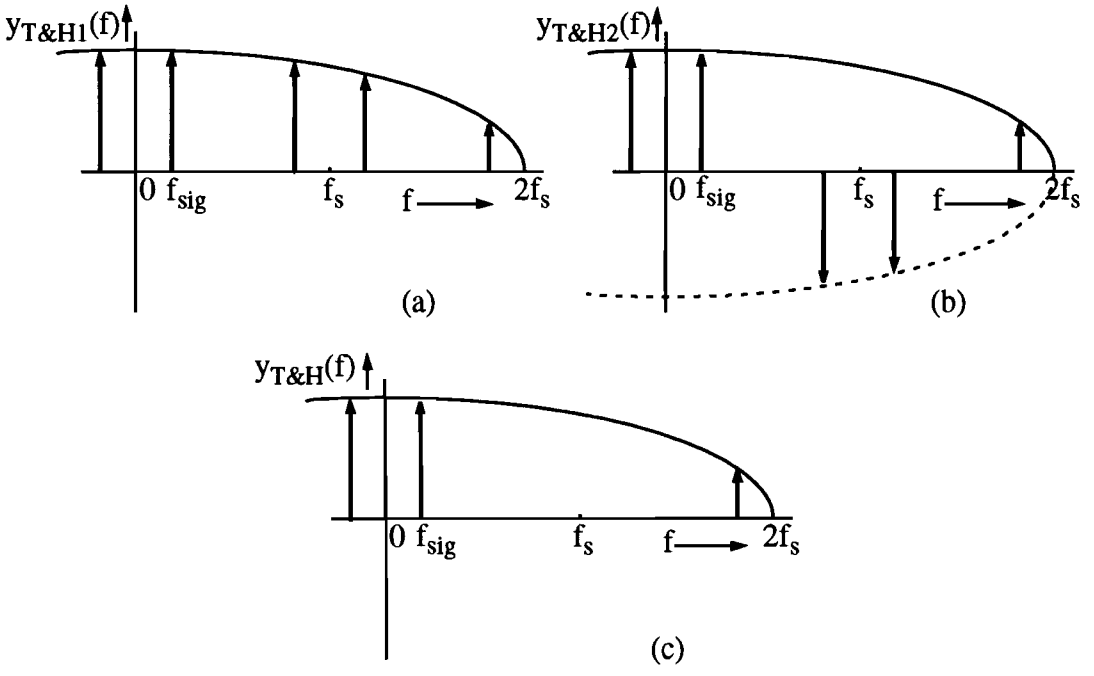


Figure 5 Frequency spectrum of the interleaved signals

The above described theory is only valid in an ideal situation. In order to get more insight into non-idealities some errors are introduced such as (1) different gain between the two track-and-hold circuits, (2) no 50% duty-cycle in the multiplexer, (3) an offset voltage between the two track-and-hold circuits and (4) a combination of the before mentioned errors.

1. Gain error: For the calculation of the influence of a gain error a worst case analysis has been done with the help of the equations (3) and (4). Due to gain error, the frequency components around f_s do not cancel completely, leading to distortion. The maximum allowable gain error in a 10 bit system has been calculated at 1.02‰ (see Appendix A). From the calculation it is concluded that very high requirements are put on the IC technology (e.g. matching).

2. Duty-cycle: The duty-cycle of the multiplexer circuit is defined at 50%. Some calculations have been done in order to determine the maximum allowable duty-cycle error (see Appendix B). Here also the error leads to incomplete canceling of the frequency components around f_s leading to distortion. The maximum error in the duty-cycle is calculated at 0.508‰, this is also a very high demand made on the process technology.

3. Offset voltage: An offset voltage in one of the track-and-hold circuits, will cause no distortion. This can easily be calculated because an offset voltage in the time domain will only lead to a Dirac pulse $\delta(f)$ at f=0 in the frequency spectrum.

4. Gain error and duty-cycle error: If it is possible to process a circuit which is as accurate as demanded in 1. and 2. then it is still not sure that a 10 bit resolution will be reached because a combination of gain error and duty-cycle error will lead to an even larger distortion. To guarantee a 10 bit resolution a domain, in which the sum of the two errors is smaller than -61.96 dB, must be marked (for more information see Appendix C).

The calculations show that only in process technologies with more than 1‰ accuracy in a buffer circuit, the results of the interleaved track-and-hold are conform the specifications. This demand is too high for todays IC technology, reasonable values are within 1% accuracy for a buffer circuit which leads to -42 dB distortion for a 1% gain error and -36 dB for a 1% duty-cycle error. From this it is concluded that this configuration is not suitable for a 10 bit 1 Gsample/s track-and-hold circuit.

2.2.3 A Stand Alone Track-and-Hold Configuration

In a stand alone configuration of a track-and-hold circuit as in Figure 3 the circuit needs to operate at 1 GHz sample rate which, as a result of a small acquisition time, directly results in a small hold capacitor leading to less accuracy and more noise. The approach is fully differential in order to meet some of the specifications of Paragraph 2.1.2. The differential configuration is shown in Figure 6.

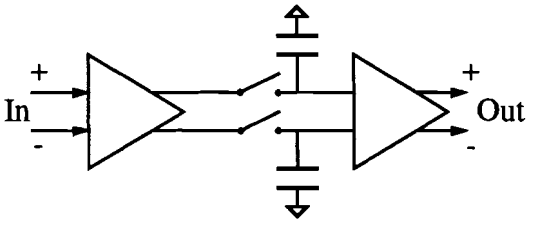


Figure 6 Differential track-and-hold circuit

Firstly, the second order harmonic distortion is canceled. Secondly, the track-to-hold step will virtually vanish because both switches will cause an identical charge injection into the hold capacitors. Finally, the droop rate reduces to a common mode effect. This results in the following artifacts: signal bandwidth, acquisition time, aperture time uncertainty, noise and hold mode feedthrough. Because of the poor results of the interleaved track-and-hold circuit, the single channel, differential configuration of Figure 6 will be used for the design of the 10 bit 1 Gsample/s track-and-hold circuit.

3 IC Technology and Transistor Parameters

The process in which the track-and-hold circuit will be realized, is a double-poly bipolar IC technology with a polysilicon deposited base. The choice for a bipolar process may be clear if high speed is required. The double-poly process results in several advantages over single-poly processes. These advantages will become clear after studying the process technology.

3.1 The Double-Poly IC Technology

In this double-poly process it is not only the emitter junction that is formed by a doped polysilicon layer (as in the QUBIC1 process [4]) but also the base contacting layer. This is done because selectively grown bases provide a better control over the active base profile of bipolar transistors, which lead to an improved trade-off between cut-off frequency f_T and base resistance. In addition, the base-collector capacitance is strongly reduced, due to inherently lower perimeter contribution [5]. In order to make the differences between the former process and the new OBIC double-poly process clear, the cross-sections of the transistors are illustrated and compared.

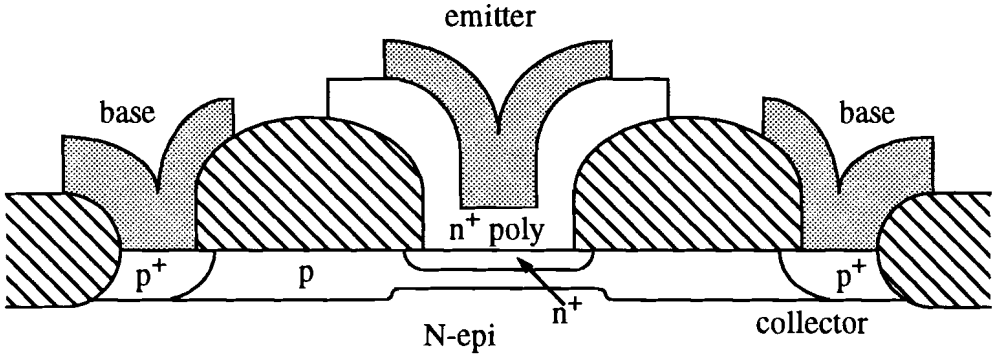


Figure 7 Former QUBIC1 NPN-transistor cross-section

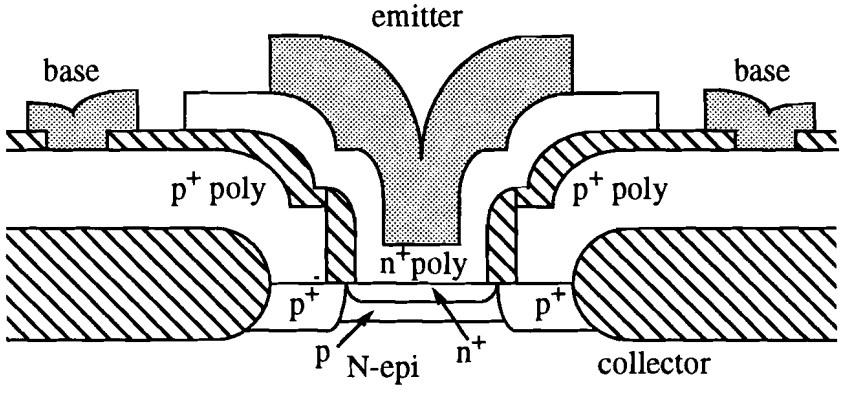


Figure 8 OBIC double-poly NPN-transistor cross-section

The base resistance of the transistor from the QUBIC1 process, Figure 7, is determined by the long p-type silicon path. In Figure 8 the base resistance is determined by a p^+-type polysilicon path with a lower resistivity, which leads to a lower base resistance and a smaller p-type silicon base area. With this polysilicon contacting layer the lateral dimensions of the transistor are minimized. Thus not only the base resistance but also the base-collector capacitance has been minimized, due to a smaller overlap between base and collector. This results in an improved circuit speed at the same current density, or reduced power consumption at the same speed.

3.2 Transistor Parameters

The transistor operation is the most important factor in the performance of high speed circuits. This high speed performance is limited by several device aspects which are determined by the transistor parameters. The formulas defining these aspects in terms of transistor parameters are included in Appendix D. The transistor parameters and its aspects of the double-poly process, OBIC (Monroe layout), and the former process, QUBIC1, are summarized in Table 1. Now a good comparison between the processes is possible.

Table 1 Transistor parameter sets

Parameter	QUBIC1	OBIC
R_{bc}	50	114.1
R_{bv}	700	359.7
R_e	30	14.8
V_{de}	0.9	0.92
Q_{B0}	9.4f	4.5f
C_{je}	4.7f	7.8f
C_{jc}	7.1f	9.4f
C_{js}	32f	29.7f
f_T	9.9G	27.4G
I_{cp}	250µ	560µ
g_m	10m	22.4m
R_b	532	252.7
C_d	160f	130f
F_v	1.6G	4.2G
F_{out}	1.2G	3G
g_{meff}/g_m	77%	75.1%
$F_{0.5}$	1.1G	2.2G

For the transistors of both processes the emitter size is 1µmx2µm. Comparing the QUBIC1 process with the OBIC process results in a multiplication of f_T, F_v and F_{out} by a factor three. This means that the bandwidth has been increased which leads to circuits operating at higher speed than the circuits in the QUBIC1 process. But the collector cur-

rent I_{cp} at peak f_T has been increased to, so there is a trade-off between speed and power. The f_T and its collector current are variable with the transistor size. In order to get some insight into the emitter area dependency, f_T and I_{cp} are shown in Figure 9 for several transistor sizes of the OBIC process. Here W_e is the emitter width, the emitter length is 2µm. The emitter width can only vary between 0.8µm and 1.2µm according to the double-poly process block, the emitter length can vary between 2µm and 10µm. The trend of f_T and I_{cp} is for larger emitter lengths the same as in Figure 9. The value of f_T may improve with 1 GHz by increasing the emitter size to 1.2µmx10µm. The value of I_{cp} increases almost linearly with the emitter size which pleads for an equal current density for all f_T.

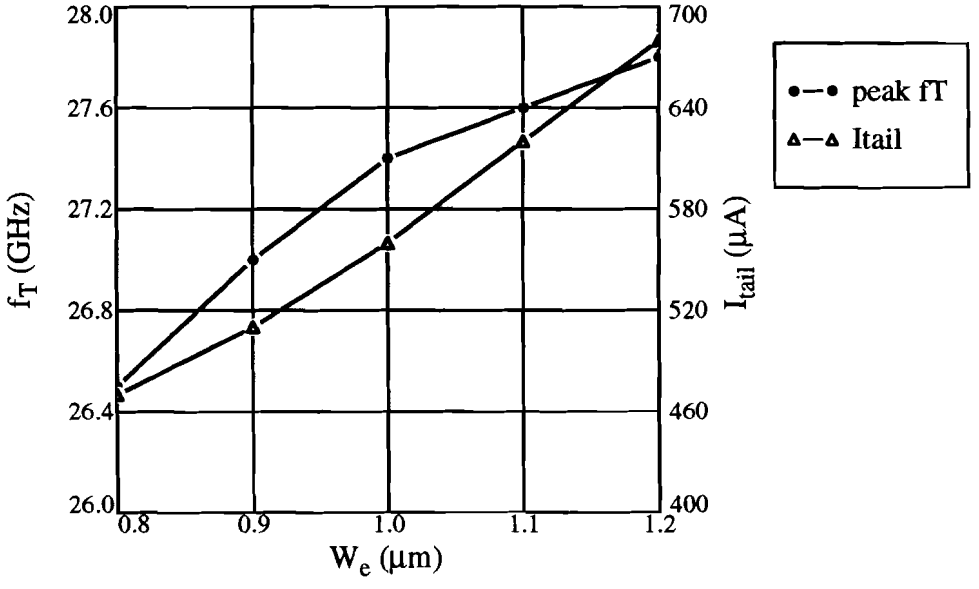


Figure 9 f_T and I_{tail} (I_{cp}) as a function of W_e

From Table 1 it is seen that the depletion capacitances C_{je} and C_{jc} haven not been reduced compared to the QUBIC1 process. This is in contrast with the before mentioned theory. Investigation on this subject has shown that the capacitances measured on the wafer at zero bias are smaller in agreement with the theory. But due to curve fitting of many measurements on transistors of all sizes, the zero bias capacitance could have been shifted over a certain range, resulting in this contradiction.

4 Analysis and Design of the Building Blocks of a Track-and-Hold Circuit

In this chapter all the building blocks of a track-and-hold circuit are described. Theory, specifications and design are covered. The subcircuits are designed for a fully differential 10 bit 1 Gsample/s track-and-hold circuit.

4.1 Noise Specifications

For a 10 bit 1 Gsample/s circuit the overall distortion must be below -62 dB in order to meet the 10 bit effective resolution. The noise power in a circuit generated by a resistor, the thermal noise, can easily be calculated using:

$$\bar{e}^2_{noise} = 4kTR\delta f. \tag{5}$$

The noise rms voltage $\bar{e}$ of a 10 bit system should not be larger than the quantization error voltage of a 10 bit system, this leads to:

$$\bar{e}_{noise,\,rms} = \sqrt{4kTR\delta f} \leq \bar{e}_{qns} = \frac{LSB}{\sqrt{12}}, \tag{6}$$

in which LSB is the value of the least significant bit in the 10 bit system. With 2 V peak-to-peak input range and a 10 bit system, $\bar{e}_{noise}$ may not exceed 564 µV rms.

However in a track-and-hold circuit due to sampling of the input signal all input frequencies that are in the aliasing signal bands are folded back into the baseband. This is also valid for the noise on the input signal. The total noise, according to [1], can now be described as

$$\bar{e}_{total} = \bar{e}_{noise} \cdot \sqrt{\frac{2f_{noise}}{f_s}}, \tag{7}$$

in which f_s is the sampling frequency and f_{noise} the noise bandwidth ($\frac{\pi}{2}f_{-3dB}$).From this it is concluded that the thermal noise generated at the input, before sampling, should be bandwidth limited in order to reduce fold-back noise due to sampling.

For a 1 GHz sample rate a 500 MHz signal bandwidth is available. Signals with frequencies below 500 MHz should be attenuated as little as possible. If an attenuation of 1 dB at 500 MHz is allowed, then the total bandwidth f_{-3dB} of the system is 983 MHz. With this system bandwidth and maximum noise signal, the maximum allowable resistor value in a circuit can be calculated. For a 1 GHz sample rate, the maximum allowable resistor value in the circuit, has been calculated at 2000 Ω. The actual resistance value should be corrected because of the signal attenuation of 1 dB at 500 MHz, this results in a maximum resistor value of 1600 Ω.

4.2 Buffers in the Track-and-Hold Circuit

As mentioned in Chapter 2, the track-and-hold circuit contains an input buffer and an output buffer. These buffers must meet the distortion specification of -62 dB over a 500 MHz input signal bandwidth and the specification made in Paragraph 4.1. Other design issues which should be taken into account are low power and chip area. Several buffer topologies will be discussed.

4.2.1 Linearized Differential Buffer

The linearized differential buffer [6] consists of a degenerated differential pair loaded with a series connection of a diode and a resistor, as illustrated in Figure 10.

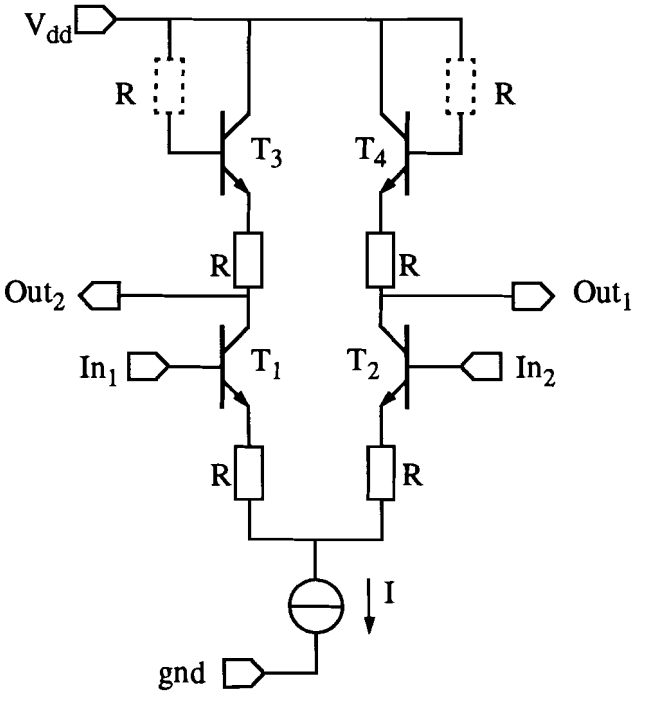


Figure 10 Linearized differential buffer

Due to base-emitter modulation effects, the voltage-to-current conversion performed by the differential input pair, T_1 and T_2, will be nonlinear. However due to an almost identical current-to-voltage conversion performed by the load a highly linear overall voltage transfer will be established. The dashed resistors contribute also to a higher linear conversion, now the base voltage of the diodes is not set at V_{dd} but it can fluctuate as the base voltage of the input transistors. The circuit has been simulated with maximum size transistors 1.2μmx10μm with I_{cp}=3.3 mA, R=400 Ω and I=3 mA, with respect to noise generation and power dissipation. The bias current I is not chosen higher in order to set the bias current at least a factor two below I_{cp}. The input signals, In_1 and In_2 are sine waves with a 0.5 V amplitude with a 180° phase shift. The results are illustrated in Figure 11. As can be seen the third harmonic, in this case the worst one, is only -47 dB down

at 500 MHz input frequency, which is not enough for a 10 bit system. From this it is concluded that this buffer is not appropriate for use as an input buffer in the track-and-hold circuit. This distortion caused by the parasitic capacitances can also be calculated.

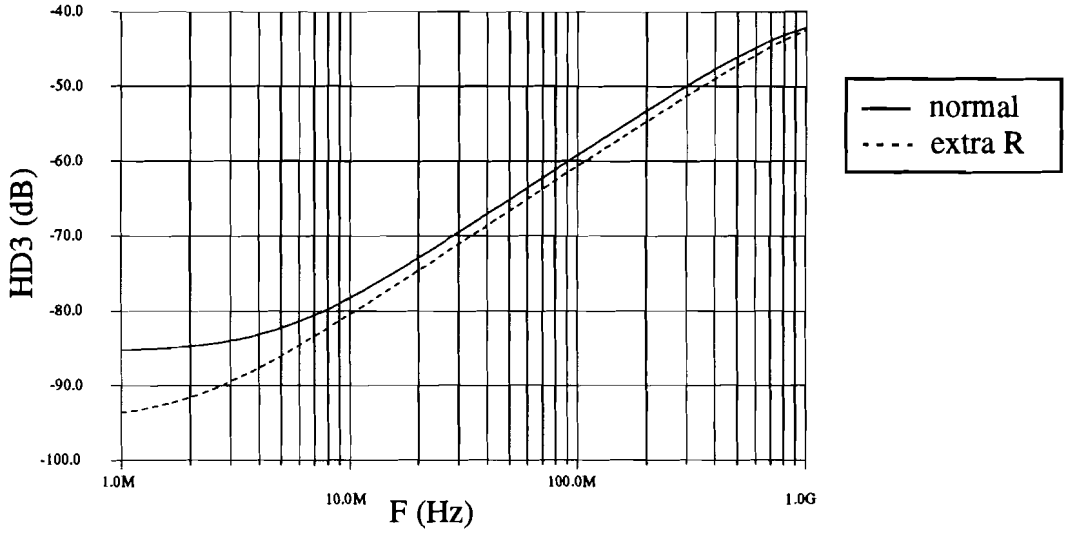


Figure 11 Third harmonic distortion of the linearized differential buffer

The parasitic capacitances causing the distortion are junction capacitances C_j, the main parasitics are the base-emitter junction capacitance C_{je} and the base-collector junction capacitance C_{jc} which are expressed as:

$$C_j = \frac{C_{j0}}{\left(1 - \frac{v}{\phi_0}\right)^m}, \tag{8}$$

in which C_{j0} is the capacitance at equilibrium (V=0 V), ϕ_0 the built-in potential and m the grading coefficient.

In the circuit of Figure 10 C_{je0} is 47.4 fF, C_{jc0} is 28.9 fF, m_c is 0.47, m_e is 0.32, ϕ_{c0} is 0.75 V, ϕ_{e0} is 0.92 V. The distortion term is calculated using:

$$v_{out} = i \cdot R = C_j \cdot \frac{dv}{dt} \cdot R. \tag{9}$$

If now for C_j a Taylor series is developed, then a third order harmonic will appear in (9). The Taylor series for C_{jc} has to be developed around -1 because this junction is reversed biased with 1 V. This leads to:

$$C_{jc} = C_{jc0}\left(\frac{1}{\left(1 + \frac{1}{\phi_{c0}}\right)^{m_c}} + \frac{m_c(1+v)}{\left(1 + \frac{1}{\phi_{c0}}\right)^{m_c}(1+\phi_{c0})} \cdots\right.$$

$$\left. \ldots + \frac{m_c(1+m_c)(1+v)^2}{2\left(1+\frac{1}{\phi_{c0}}\right)^{m_c}(1+\phi_{c0})^2} + \frac{m_c(1+m_c)(2+m_c)(1+v)^3}{6\left(1+\frac{1}{\phi_{c0}}\right)^{m_c}(1+\phi_{c0})^3} + \ldots \right). \quad (10)$$

The actual voltage v over the junction capacitance is -1+sin(2πft) because the base voltage of the input transistor is 2.5+0.5*sin(2πft) and the collector voltage is 3.5-0.5*sin(2πft). But now, because of the series developed around -1, only sin(2πft) has to be applied for v. The series has to be developed to the fourth order to obtain an accurate value for the distortion. This third order distortion has also been calculated at -47 dB for a 500 MHz input signal. From this it is concluded that the influence of the junction capacitance C_{jc} has been modeled by developing a Taylor series of its characteristic equation.

In order to obtain a better circuit performance the capacitance should be reduced. To give some insight into the maximum capacitance value allowed for a certain performance the third order distortion is illustrated in Figure 12 as a function of the junction capacitance C_{jc} for several signal frequencies.

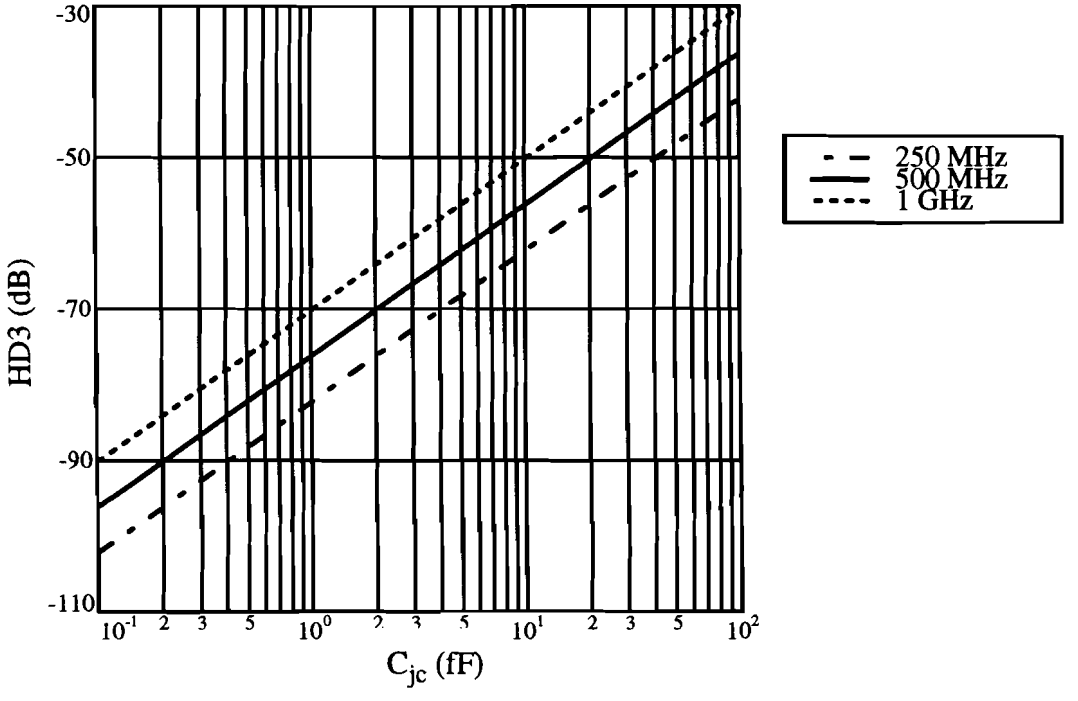


Figure 12 Third harmonic distortion vs. C_{jc} for several signal frequencies

For the influence of C_{je} an identical calculation can be done with the use of (8) and (9). Only now the junction voltage is determined by:

$$v = V_T \ln\left(\frac{I_{bias} + i_{sig}}{I_{sat}}\right), \quad (11)$$

where I_{sat} is the saturation current of the transistor in reverse bias and i_{sig} the signal cur-

rent. The Taylor series results in:

$$v = V_T\left[\ln\left(\frac{I_{bias}}{I_{sat}}\right)+\frac{i_{sig}}{I_{bias}}-\frac{1}{2}\left(\frac{i_{sig}}{I_{bias}}\right)^2+\frac{1}{3}\left(\frac{i_{sig}}{I_{bias}}\right)^3-\frac{1}{4}\left(\frac{i_{sig}}{I_{bias}}\right)^4+....\right] \quad (12)$$

With I_{bias}=1.5 mA and I_{sat}=9.6 aA, the Taylor series of (8) has to be developed around 0.875 V, the DC forward bias voltage of the base-emitter junction. The substitution of all the Taylor series in (9) results in a function including all the distortion terms, from this the third order harmonic distortion is determined, it is calculated at -62dB. However simulations have shown that for distortion due to C_{je} the third order harmonic is set at -56 dB. The mismatch between theory and simulations might be caused the very simple model used to calculate the distortion. In the simulation the complete transistor model is taken into account. If the Taylor series here is developed around zero volt then a better matching is found, the reason for this is that series around zero matches better with the used model than the series developed around 0.875 V.

From the calculations and simulations of the linearized differential buffer it is concluded that this buffer is not suited for a 10 bit 500 MHz input buffer with a 2 V peak-to-peak differential input voltage. As can be seen in the distortion equations, the buffer has a better performance operating with smaller input signal amplitudes. Simulations have been done in order to find out for which amplitude the buffer reaches the desired performance. The results are given in Figure 13. From this it is concluded that with less than 0.3 V amplitude single-ended the 10 bit 500 MHz performance is achieved.

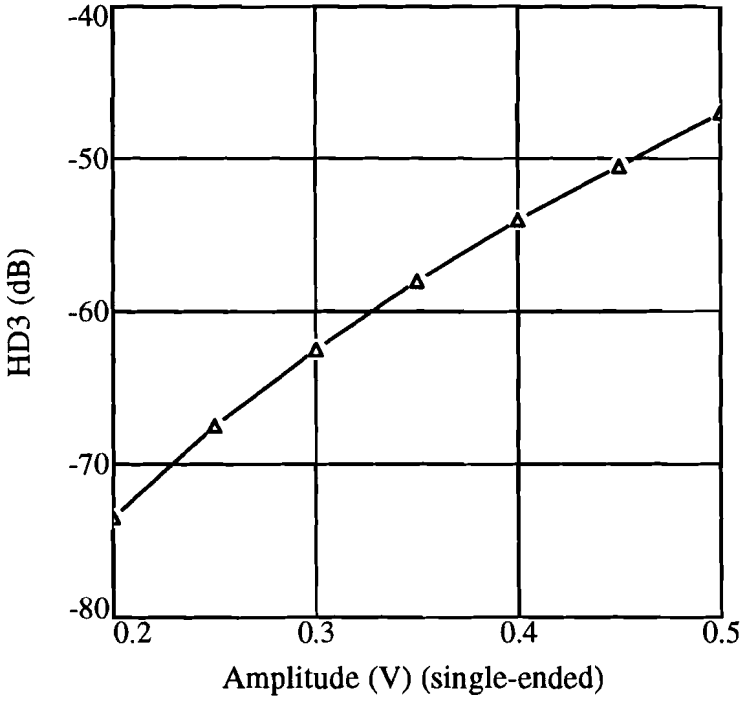


Figure 13 Third order distortion vs. signal amplitude

4.2.2 Translinear Buffer with Base Current Compensation

The translinear principle [7] is a well-known circuit topology for realizing wide-band buffers. Modifications by increasing the input window and improving the high frequency linearity have already been proposed [8]. This resulted in a trans-linear buffer as illustrated in Figure 14.

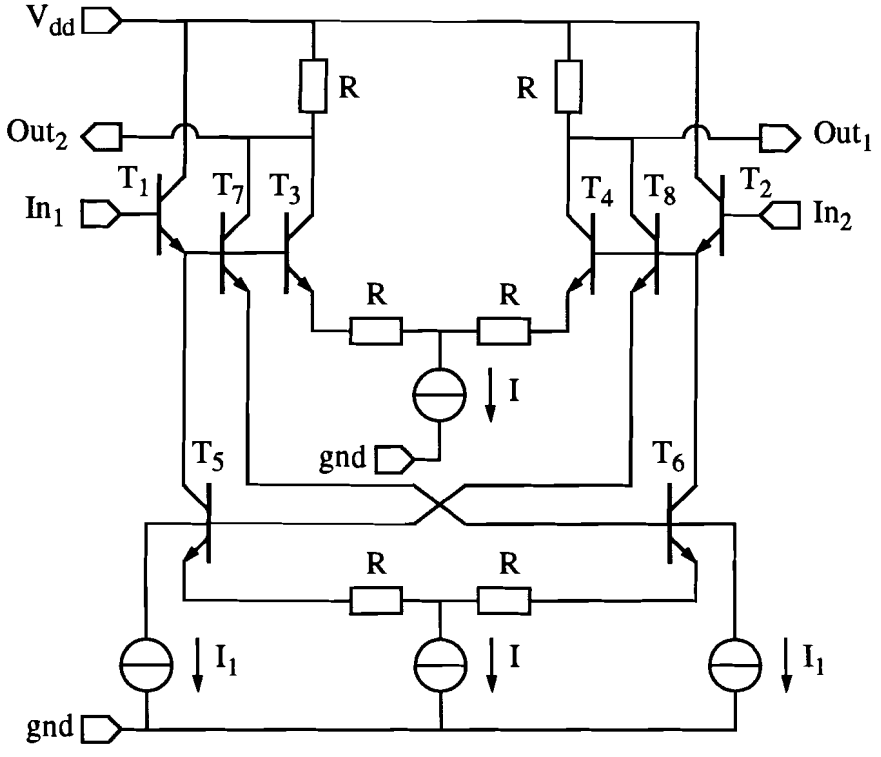


Figure 14 Translinear buffer with base current compensation

Assuming equal transistor sizes and resistor values, the voltage difference between T_3 and T_4 is a copy of the differential input signal. This should lead to a high linearity. But for high frequencies the linearity is limited by non-linear base currents of T_3 and T_4. For this reason the same base currents of T_5 and T_6 are connected to the output terminals by the use of T_7 and T_8. Now the circuit has a non-linear base current compensation which leads to high linearity beyond the beta cut-off frequency f_β. The circuit has been simulated with maximum size transistors 1.2µmx10µm with I_{cp}=3.3 mA, R=400 Ω, I_1=100 µA and I=3 mA. The input signals, In_1 and In_2, are sine waves with a 0.5 V amplitude with a 180° phase shift. The results are illustrated in Figure 15. As can be seen the third order harmonic is set at -55 dB for 500 MHz which is not enough to meet the specifications for the track-and-hold to be designed. This high frequency distortion is also due to the parasitic capacitances as mentioned in Paragraph 4.2.1. Another problem is that the performance at low frequencies is below the 10 bit resolution, this will be tackled further on.

From the results of the simulations of the translinear buffer it is concluded that this buffer in this configuration is not suited for a 10 bit 500 MHz input buffer with a 2 V peak-to-peak differential input voltage. Just like the linearized differential buffer, the translinear buffer has a better performance operating with smaller amplitudes. Some simulations have been done in order to find out for which amplitude the buffer reaches it desired performance. The results are given in Figure 16. From this it is concluded that with less than 0.4 V amplitude single-ended the 10 bit 500 MHz performance is reached.

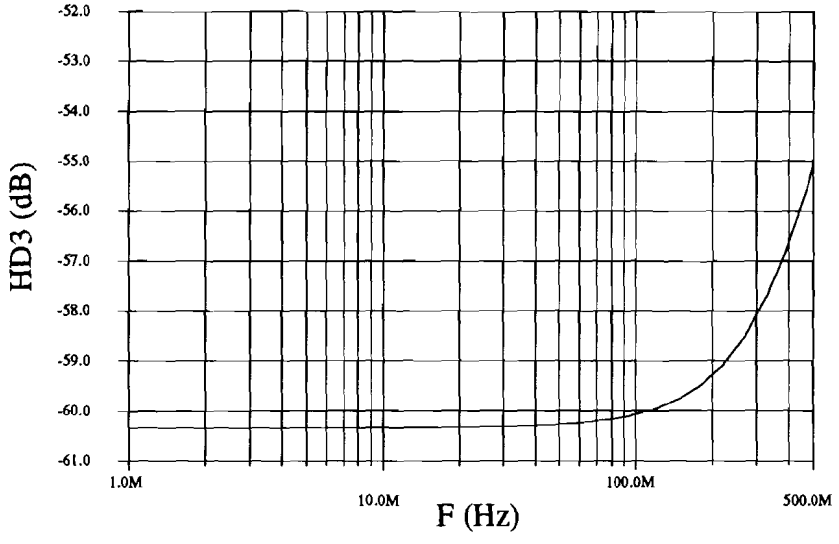


Figure 15 Third harmonic distortion of the translinear buffer

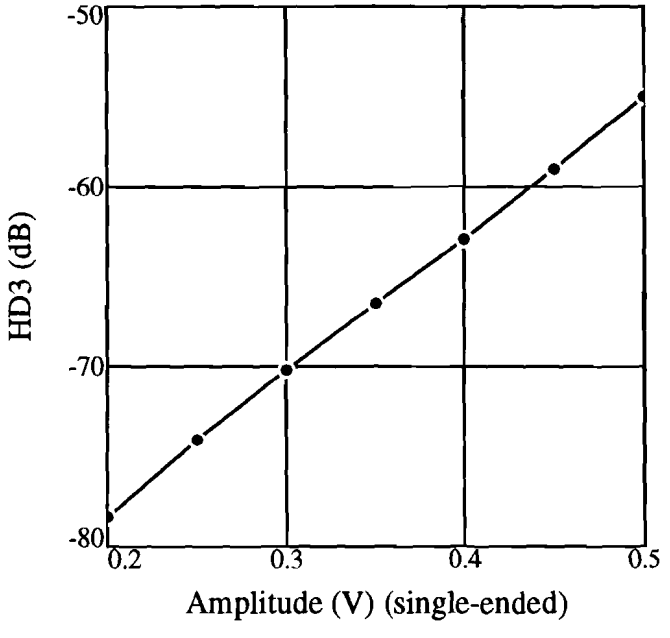


Figure 16 Third order distortion vs. signal amplitude

The reason why the low frequency performance is not good, is that there is a difference between the emitter currents of T_1 and T_3. If the circuit is analyzed exactly then it is found that the emitter currents differ twice the base current. With low beta (β) the base current is relatively large. In this process β is approximately 65. This base current loss disturbs the translinear principle, because now the base-emitter modulation is not canceled completely. The base-emitter modulation can now be expressed as follows:

$$\Delta v_{be1} = V_T \ln\left(\frac{I + i_{sig}}{I - i_{sig}}\right), \tag{13}$$

for the transistor pair T_3 and T_4 and

$$\Delta v_{be2} = V_T \ln\left(\frac{I - i_{sig} + \frac{2I}{\beta} + \frac{2i_{sig}}{\beta}}{I + i_{sig} + \frac{2I}{\beta} - \frac{2i_{sig}}{\beta}}\right), \tag{14}$$

for the transistor pair T_1 and T_2. Equations (13) and (14) can be developed in Taylor series of the form:

$$\Delta v_{be} = -2V_T I \cdot i_{sig} + \frac{2V_T I}{3} \cdot i_{sig}^3 + \frac{2V_T I}{5} \cdot i_{sig}^5 + \ldots. \tag{15}$$

The distortion is now calculated with

$$v = \Delta v_{be1} + \Delta v_{be2}. \tag{16}$$

After applying the right values for the signals, the distortion was calculated at -60 dB for the third harmonic, which is very close to the simulated result of Figure 15.
Since now the artifact of this circuit is known a solution is found. As concluded from Figure 14 there is a current difference of twice the base current. This is reduced to a difference of one base current by connecting the base of T_3 to the emitter of T_7. Now there is only one base current difference, an extra base-emitter modulation and an extra base compensation current. This circuit, as shown in Figure 17, has also been simulated. The results are given in Figure 18. As can be seen the low frequency distortion is reduced from -60 dB to -80 dB. This means that not only the reduction of the base current loss but also the extra base-emitter modulation and the extra base compensation current have a positive effect on the circuit functioning. A disadvantage of this new circuit geometry is the extra base-emitter voltage due to which the DC bias voltage has to be raised. The high frequency distortion has increased. This can be easily explained, due to the raising of the DC voltage the depletion capacitances of transistors T_1, T_2, T_7 and T_8 are less reverse biased than in the former circuit.

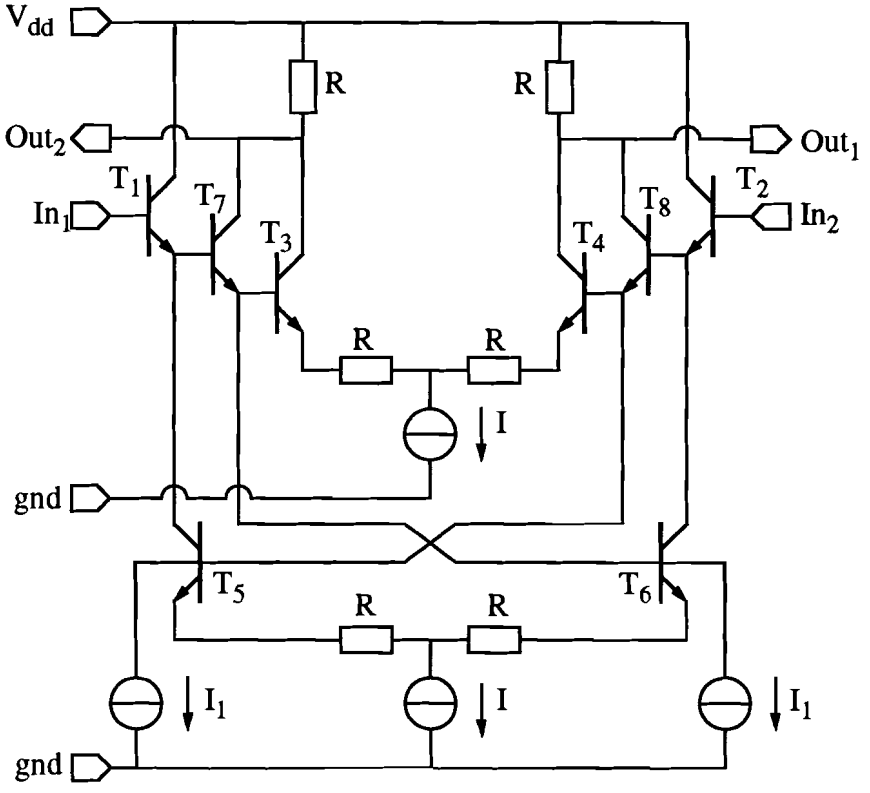


Figure 17 Extra compensated translinear buffer

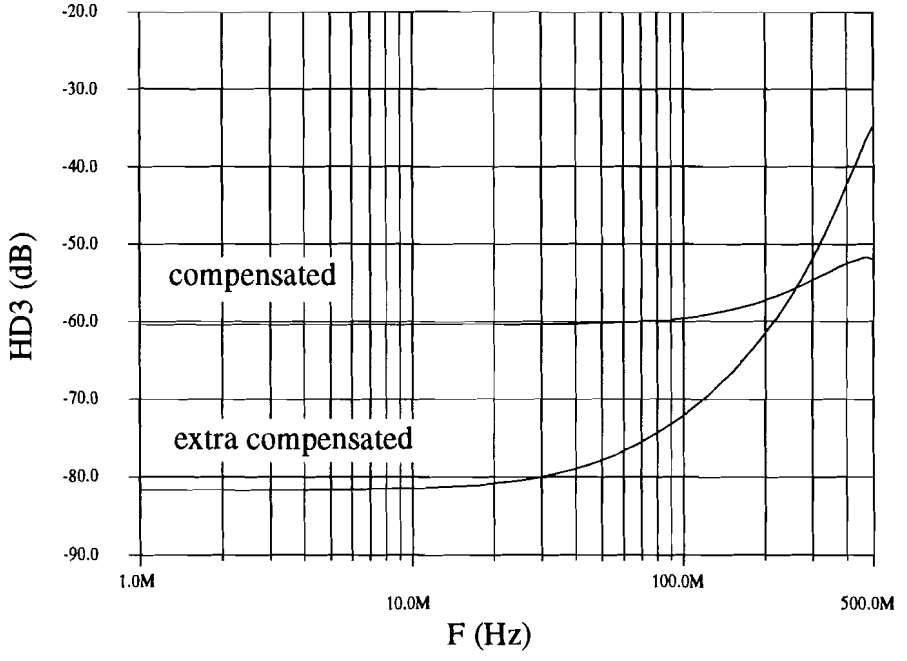


Figure 18 HD3 of the extra compensated translinear buffer

4.2.3 Unity Gain Buffer

The buffer which will be described now is a unity gain buffer with unity feedback. As this buffer is single-ended, two are needed in the differential configuration. The basic circuit is illustrated in Figure 19. This circuit has certain advantages compared to the other circuits: it is small which means fast and the resistor *R* is in the amplification which means that the thermal noise generated by the resistor can be divided with the gain. Thus a larger resistor value than in Paragraph 4.1 is calculated, is allowed.

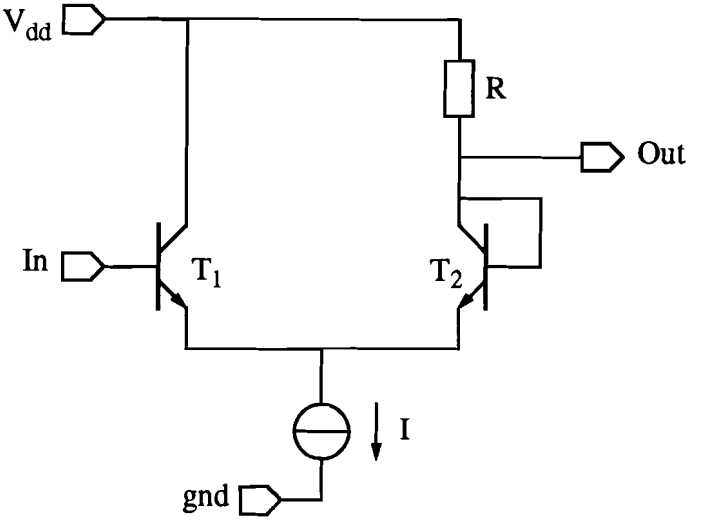


Figure 19 Basic unity gain buffer

The circuit has been simulated with maximum size transistors 1.2µmx10µm with I_{cp}=3.3 mA, R=800 Ω and I=3 mA. The input signal *In* is a sine wave with a 0.5 V amplitude. The third order harmonic is set at -64 dB over a full 500 MHz range which is enough to meet the specifications for the track-and-hold to be designed. Also for this buffer a distortion as function of the input signal amplitude is given. The results are illustrated in Figure 20. The distortion results can be checked easily with the following equation:

$$v = V_T \ln\left(\frac{I_{bias,T1} + i_{sig}}{I_{bias,T2} - i_{sig}}\right) \quad (17)$$

Proper DC voltage biasing, the bias currents through transistors T_1 and T_2 are identical. By developing a Taylor series the third order harmonic is found, the calculated value is found to be -63 dB. From this it is seen that with a simple calculation the distortion can be predicted reasonably accurate. The distortion of the parasitic capacitances, the junction capacitances, which determined that the previous buffers were not suitable is now canceled because of the short-circuit over the base-collector depletion capacitance of transistor T_2. The distortion of the base-collector capacitance of T1 can be kept low if the output resistance of the previous circuit is small.

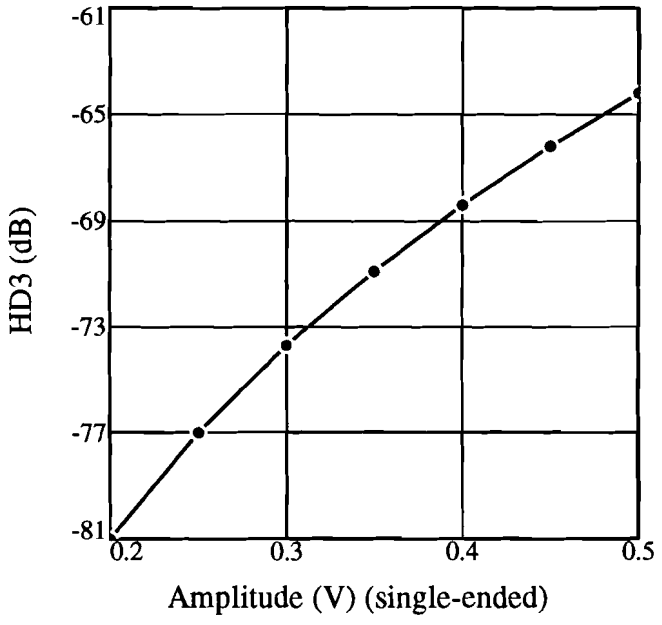


Figure 20 Third order distortion vs. signal amplitude

However the safety margin is too small if process matching is taken into account. This will be shown with the help of some DC voltage and resistor deviations. First the distortion is given with the same DC settings as before but now the resistor has been varied slightly as with matching problems. The results in Figure 21 are the simulation results, but these results can also be calculated with the help of (17).

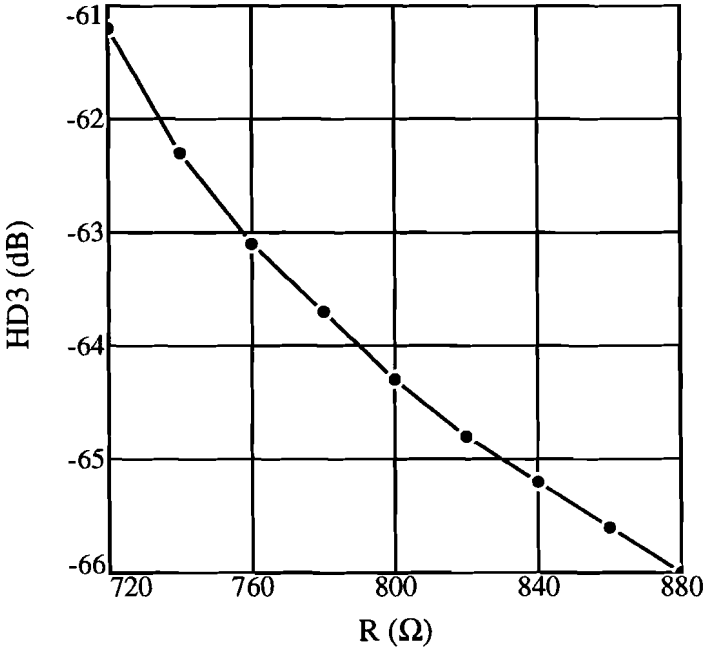


Figure 21 HD3 vs. resistance variation (0.5 V amplitude)

As can be seen from Figure 21 a smaller resistance deteriorates the distortion of the circuit, which can lead to a performance lower than 10 bit. A larger resistance however improves the distortion, because the signal current decreases. But the signal current must be kept large enough to be able to drive a following circuit.
Also the influence of the DC bias voltage at the input of the circuit has been investigated. The bias voltage has been varied but the resistance of R has been kept constant. This leads to different bias currents of the transistors, which results in extra harmonic distortion. The results at 500 MHz are illustrated in Figure 22, calculating the distortion with (17) gives the same results.

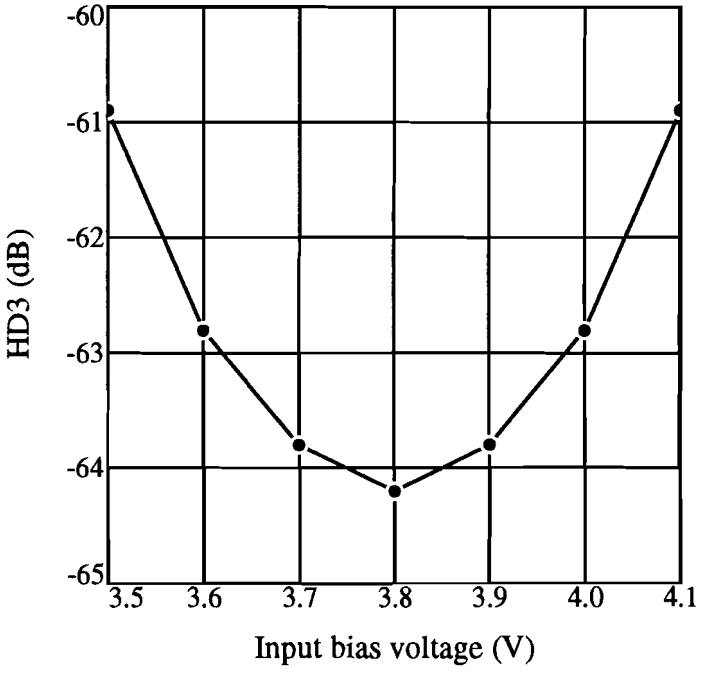


Figure 22 HD3 vs. bias voltage variation (0.5 V amplitude)

It is concluded that a high frequency linear buffer is found but its overall distortion is just a few decibels too high. If the buffer could be linearized a little bit more then it would be suitable for the 10 bit 1 Gsample/s track-and-hold circuit. The buffer can be linearized by putting two stages in parallel. But now the DC input voltage and output voltage is lowered, this is not desirable if the buffer has to drive following stages. Another option is to put two complementary stages in parallel in which an emitter ratio 'n' or a DC voltage source is applied [9]. The circuit configuration is given in Figure 23. In order to explain the functioning of the circuit, some calculations are given.
Transforming of the normal differential pair equation (17) results in

$$i_{sig} = I_{bias} \tanh\left(\frac{v}{2V_T}\right). \tag{18}$$

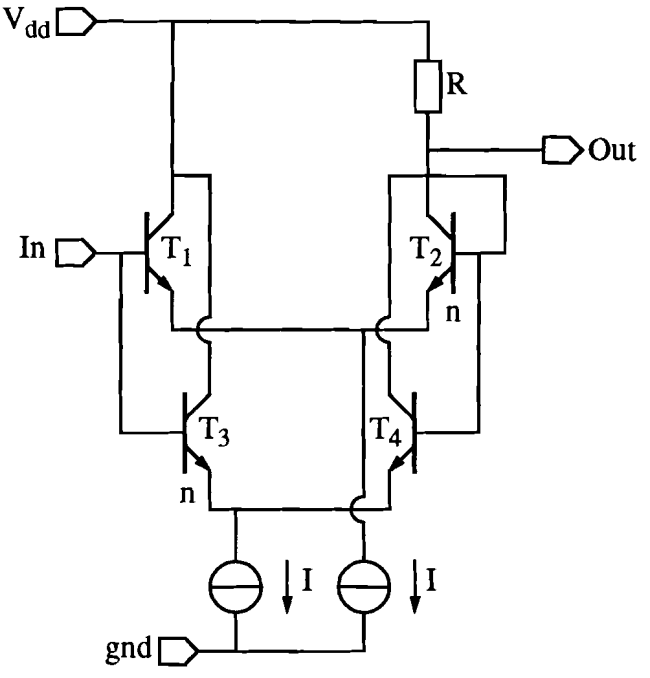


Figure 23 Linearized unity gain buffer (emitter ratio)

The transconductance g_m of the differential pair which determines the linearity is given by:

$$g_m = \frac{di_{sig}}{dv} = \frac{I_{bias}}{2V_T} sech^2\left(\frac{v}{2V_T}\right). \tag{19}$$

The transconductance has been simulated for a differential pair (see Figure 24), the simulation results match with the calculation of (19).

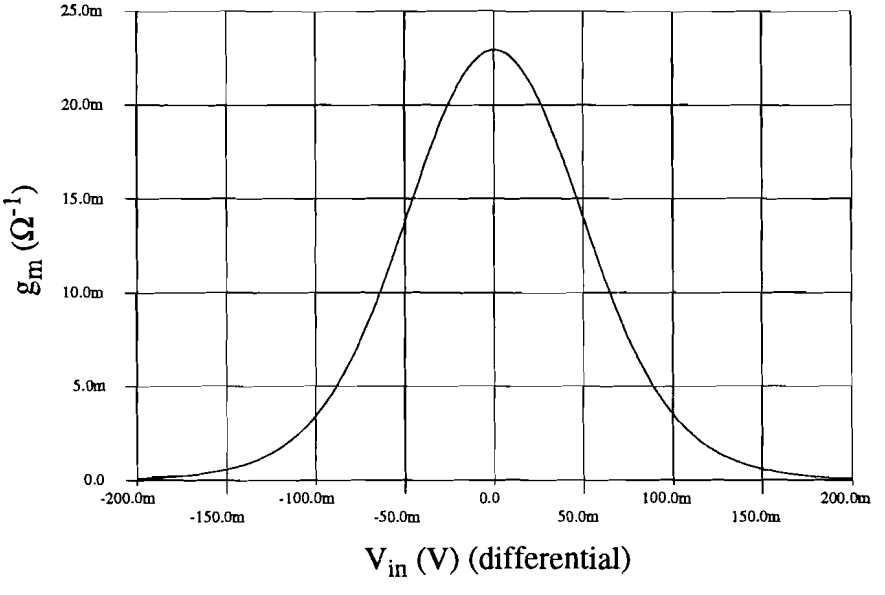


Figure 24 Transconductance vs. differential input voltage

For the circuit configuration of Figure 23 equation (18) turns into

$$i_{sig} = I_{bias}\left[\tanh\left(\frac{v - V_{offset}}{2V_T}\right) + \tanh\left(\frac{v + V_{offset}}{2V_T}\right)\right], \tag{20}$$

in which V_{offset} is an offset voltage generated by the emitter ratio 'n' which is equal to

$$V_{offset} = V_T \ln(n). \tag{21}$$

The third harmonic distortion is calculated by developing a Taylor series of (20), the Taylor series has to be developed further than the third order as in [10] this leads to

$$i_{sig} = I_{bias}\left(v \cdot \frac{sech^2\left(\frac{V_{offset}}{2V_T}\right)}{V_T} + v^3 \cdot \frac{\left(-2 + cosh\left(\frac{V_{offset}}{V_T}\right)\right) sech^4\left(\frac{V_{offset}}{2V_T}\right)}{12V_T^3} \ldots \right.$$
$$\left. \ldots + v^5 \cdot \frac{\left(33 - 26cosh\left(\frac{V_{offset}}{V_T}\right) + cosh\left(\frac{2V_{offset}}{V_T}\right)\right) sech^6\left(\frac{V_{offset}}{2V_T}\right)}{960V_T^5} + \ldots \right). \tag{22}$$

The fifth order component and further of (22) also contribute to the third order harmonic distortion. The optimal offset voltage to reduce the third order harmonic distortion can now be calculated and is found to be 39 mV. This calculation results in a 5 mV difference with the values calculated in [9] and [10]. Using (21) this leads to an emitter ratio of 0.22. The smallest transistor is now chosen to have a 1.2µmx2.2µm emitter size and the largest 1.2µmx10µm.

The circuit of Figure 23 has now been simulated with the calculated emitter ratio. As expected the transconductance g_m is now more linear around zero. The transconductance of the differential pairs and the total transconductance are given in Figure 25.

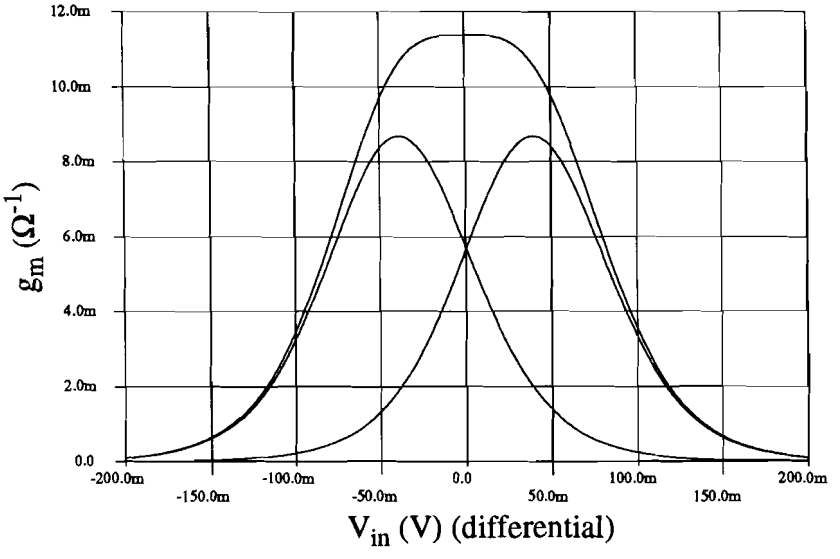


Figure 25 Linearized transconductance vs. differential input voltage

In Figure 25 the current I from Figure 23 is set at 1 mA and the resistance in the actual buffer is set to 1000 Ω which leads to a DC input voltage of 4 V. This current reduction is done to decrease the influence of the emitter resistance on the offset voltage. The resistance R has been increased in order to reduce the signal current together with the bias current. Now an AC analysis is done on the circuit of Figure 23, in which the above mentioned values are used. From Figure 26 it is seen that the overall performance has increased.

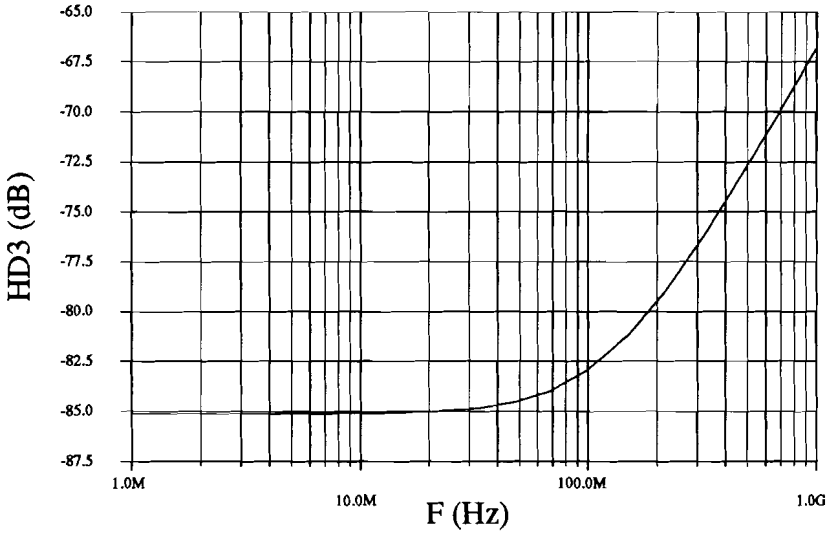


Figure 26 HD3 vs. input frequency of the linearized unity gain buffer

From Figure 26 it can also be seen that at high frequencies the performance reduces, probably due to the parasitic capacitance C_{je}. This influence is calculated in the same way as in Paragraph 4.2.1, but now a detailed description of the signal currents is needed in order to determine a good value for the base-emitter voltage. From Figure 23 it is seen that at the node *Out* two base-emitter capacitances of T_2 and T_4 are connected, with different capacitance values and different base-emitter voltages. The distortion can now be calculated with

$$v_{out} = C_{je,\mathrm{T2}} \cdot \frac{dv_{be,\mathrm{T2}}}{dt} \cdot R + C_{je,\mathrm{T4}} \cdot \frac{dv_{be,\mathrm{T4}}}{dt} \cdot R. \qquad (23)$$

For the calculation of the parasitic capacitances equation (8) is used in which v has to be substituted, once by $v_{be,T2}$ and once by $v_{be,T4}$. For the capacitances at equilibrium the values $C_{je0,T2}$= 11 fF and $C_{je0,T4}$= 47 fF are applied. Now a detailed description of the base-emitter voltage has to be found. Due to the emitter ratio, the signal current through the transistors is no sine wave anymore. The signal current can be divided in a DC component, due to biasing, a positive and a negative signal component. The problem is that due to the emitter ratio the amplitude of the positive and negative signal component are not equal. The sine wave is now split into a positive and a negative part, which can be scaled by different amplitudes.

The positive part of the sine wave can be described with

$$i_{sig+} = A \cdot \left[\frac{1}{\pi} + \frac{1}{2}\sin(2\pi ft) - \frac{2}{\pi}\left(\frac{\cos(4\pi ft)}{3} + \frac{\cos(8\pi ft)}{15} + \frac{\cos(12\pi ft)}{35}\right) + \ldots\right], \quad (24)$$

and the negative part with

$$i_{sig-} = B \cdot \left[-\frac{1}{\pi} + \frac{1}{2}\sin(2\pi ft) + \frac{2}{\pi}\left(\frac{\cos(4\pi ft)}{3} + \frac{\cos(8\pi ft)}{15} + \frac{\cos(12\pi ft)}{35}\right) + \ldots\right]. \quad (25)$$

The base-emitter voltages can now be calculated if the scaling factors A and B are known for the transistors T_2 and T_4, these are extracted from previous simulations. This results in

$$v_{be,T2} = V_T \ln\left(\frac{i_{sig+,T2} + i_{sig-,T2} + I_{bias,T2}}{I_{sat,T2}}\right), \quad (26)$$

and

$$v_{be,T4} = V_T \ln\left(\frac{i_{sig+,T4} + i_{sig-,T4} + I_{bias,T4}}{I_{sat,T4}}\right). \quad (27)$$

The saturation currents are given by $I_{sat,T2}$=2 aA and $I_{sat,T4}$=9.6 aA. By developing Taylor series of the base-emitter voltages, calculating their derivative, developing Taylor series of the parasitic capacitances, substituting all the variables in (23) leads to a third order harmonic distortion of -73 dB at 500 MHz, which is very close to the simulated result from Figure 26.

4.3 Switch Design

The switch and the hold function are combined in one circuit. This circuit consists basically of three transistors and a hold capacitor. The basic circuit is shown in Figure 27. Transistor T_1 is the switch itself, T_2 and T_3 perform the switching function.

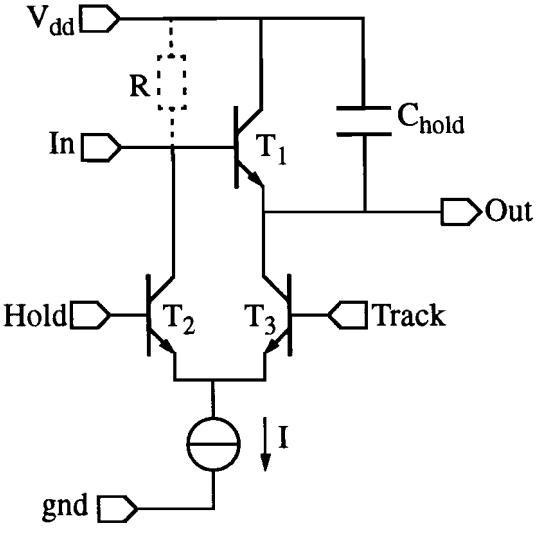


Figure 27 Basic switch configuration

If the circuit is in track mode then the voltage on the track node is higher than the voltage on the hold node. This implies that current I is sustained by T_1 and T_3, which means that the switch is closed resulting in $\Delta v_{out} = \Delta v_{in} - \Delta v_{be,T1}$. By switching from track to hold mode, the voltage at the input is lowered due to the current I through the resistor R, which is the load resistor of the previous buffer. The hold capacitor memorizes the input voltage at the output in the hold mode. If now the input voltage during hold mode is low enough then the switch is opened.
Due to base-emitter modulation $\Delta v_{be,T1}$ in the track mode, the output signal will suffer from distortion. This distortion is calculated by developing a Taylor series of this base-emitter modulation, like

$$\Delta v_{be,T1} = V_T \ln\left(\frac{I + i_c}{I}\right) = V_T\left[\frac{i_c}{I} - \frac{1}{2}\left(\frac{i_c}{I}\right)^2 + \frac{1}{3}\left(\frac{i_c}{I}\right)^3 - \frac{1}{4}\left(\frac{i_c}{I}\right)^4 + \ldots\right], \tag{28}$$

in which i_c is the current to (dis)charge the capacitor, given by

$$i_c = C_{hold} \cdot \frac{dv_{out}}{dt}. \tag{29}$$

By taking more components than only the third order component, an accurate third order harmonic distortion component is calculated. Now a value for the capacitor and the tail current have to be chosen. The capacitor must not be very large, otherwise the tail current has to be very large also resulting in high power dissipation. The calculations show that for a 1 pF hold capacitor a tail current of 3 mA is required to obtain an exact 10 bit resolution at 500 MHz. To build in a safety margin, the capacitor C_{hold} is chosen to be 1 pF and the tail current I is 4 mA resulting in a -70.6 dB third order harmonic distortion at 500 MHz signal frequency. The switch distortion has also been simulated in a AC analysis, the above mentioned values are used in the simulation. The results are shown in Figure 28.

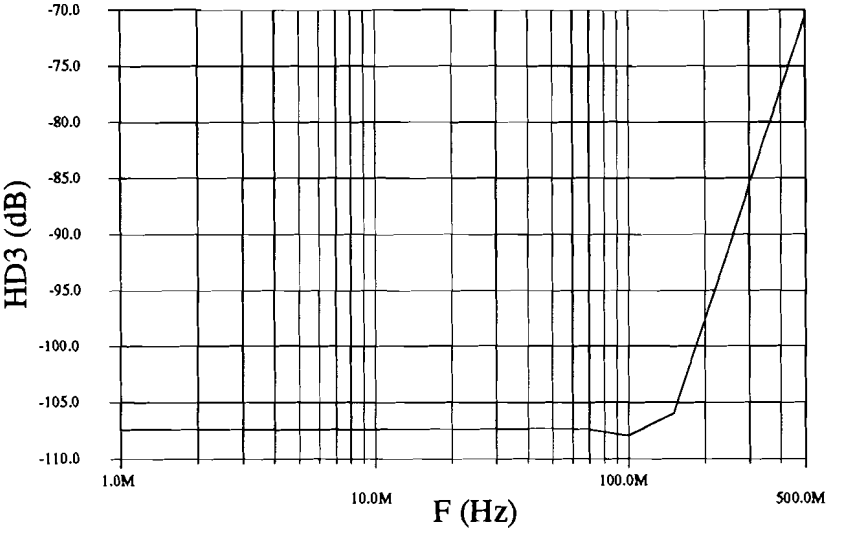


Figure 28 Switch distortion vs. signal frequency

The 4 mA tail current in the switch can result in distortion due to a non-linear base current at high frequencies, because the current is larger than the I_{cp} of the largest transistor. This problem can be solved by connecting two transistors in parallel.

Now the switching characteristics have to be investigated. This is done by alternating applying a pulse signal on transistors T_2 and T_3 between 1.2 V and 1.5 V. Transient simulations have shown that an oscillation occurs due to switching. At the first sight an oscillation should not be possible because only one capacitor is used in the circuit. And in previous track-and-hold circuits such an oscillation due to switching was already damped because of the long settling times allowed at lower speed. In this circuit this oscillation is not allowed because there is only 0.5 nanosecond in a track period. For this reason some research is done on frequency response of a transistor used as an emitter follower. The response can be described best by using a small-signal equivalent circuit [11]. The used small-signal equivalent circuit is given in Figure 29.
In this circuit R_b is the base resistance of the transistor lumped with the source resistance, C_π is the junction diffusion capacitance (given in Appendix D) and r_π the junction diffusion resistance ($=\beta_0/g_m$).

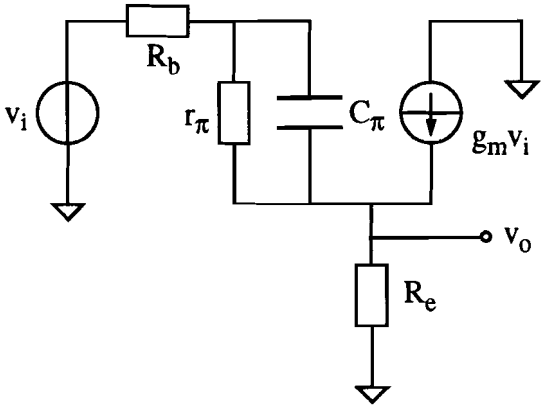


Figure 29 Small equivalent circuit of the switching transistor

From this the input and output impedances can be calculated, resulting in an input impedance given

$$z_i = R_b + z_\pi + (g_m z_\pi + 1)R_e, \tag{30}$$

an output impedance resulting in

$$z_o = \frac{z_\pi + R_b}{1 + g_m z_\pi}, \tag{31}$$

in which

$$z_\pi = \frac{r_\pi}{1 + sC_\pi r_\pi}. \tag{32}$$

By examining the input impedance z_i of (30) it is found that this impedance can be represented as a parallel R-C circuit in series with R_b and R_e. The effective input capacitance is $C_\pi/(1+g_mR_e)$ and less than C_π for typical values of g_mR_e. Thus at very high frequencies the input impedance of the emitter follower becomes capacitive.
The emitter follower output impedance z_o can best be split into a high and low frequency calculation. At low frequencies, where $z_\pi=r_\pi$, this results in

$$z_o\Big|_{\omega=0} \cong \frac{1}{g_m} = \frac{R_b}{\beta_0}. \tag{33}$$

For high frequencies, where $z_\pi \to 0$ because C_π becomes a short circuit, the following equation is valid

$$z_o\Big|_{\omega=\infty} = R_b. \tag{34}$$

From this it is concluded that at very low and very high frequencies, z_o is resistive. In between its behavior depends on parameter values. It is also concluded that with increasing frequency the impedance z_o increases, this represents inductive behavior. This inductive behavior can have a major influence on the circuit behavior, particularly when the emitter follower drives capacitive loads, as in the track-and-hold circuit. For this circuit with inductive behavior an equivalent circuit can be postulated as in Figure 30.

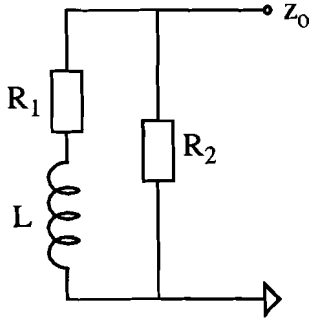


Figure 30 Equivalent circuit of the emitter follower output impedance

For low frequencies the inductor is a short circuit, which results in an output impedance of the parallel resistance of R_1 and R_2. For high frequencies the inductor is an open circuit, which results in an output impedance of R_2. Assuming that $R_1<<R_2$, then the impedance of Figure 30 can be expressed as

$$z_o = \frac{(R_1+sL)R_2}{R_1+R_2+sL} \cong \frac{(R_1+sL)R_2}{R_2+sL}. \tag{35}$$

Comparing (31) with (35), the following expressions for the components of Figure 30

can be found:

$$R_1 = \frac{1}{g_m} + \frac{R_b}{\beta_0}, \tag{36}$$

$$R_2 = R_b, \tag{37}$$

$$L = C_\pi r_\pi \frac{R_b}{\beta_0}. \tag{38}$$

By driving a capacitive load, a L-C resonance circuit is formed which leads to oscillations. The oscillations can be damped by connecting a resistor in series with the capacitor. Figure 30 now changes into Figure 31, due to the capacitive load with its damping resistor.

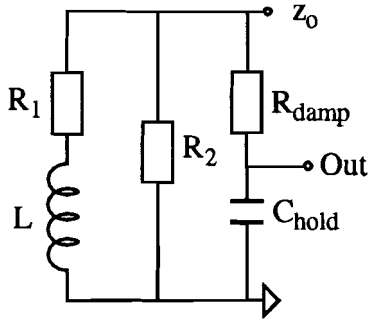


Figure 31 Small-signal equivalent circuit of the basic switch configuration

The influence of a switching current at node z_0 on the node *Out* is calculated with the Kirchhoff current equations. The response results in

$$v_{out} = i \cdot \frac{sLR_2 + R_1R_2}{s^2(LR_dC + LR_2C) + s(CR_1R_2 + CR_1R_d + CR_2R_d + L) + R_1 + R_2}. \tag{39}$$

The step response of this function is transformed into the time domain by applying an inverse Laplace transform. This transform leads to a difficult time function due to the occurring oscillation. Therefore it is more convenient only to observe the envelope exponential which is calculated at

$$oscillation\ envelope = e^{\left(-\frac{(R_1R_2C + R_1R_dC + R_2R_dC + L)t}{2(LR_2C + LR_dC)}\right)}. \tag{40}$$

For a -80 dB distortion due to acquisition time a R-C time constant of 9.2 is required [1]. This acquisition time distortion is calculated at -80 dB in order to ensure the 10 bit specifications, because the used model is very simplified. The track mode period is only 0.5 ns valid for a 1 GHz sample rate. This means that the time constant of (40) must be around $9.2/0.5*10^{-9}=1.84*10^{10}$. Evaluating equation (40) has led to a smaller hold

capacitor of 0.1 pF, a smaller switching current of 0.6 mA and a smaller transistor of 1μmx2μm in order to meet the calculated specifications. The resistor R_{damp} is now calculated at 170 Ω. With this implementation the influence of the oscillation has been reduced below -80 dB. The distortion, due to the earlier mentioned base-emitter modulation, is calculated at -82 dB for the new component values. Simulations, AC and transient with FFT, of all this have shown equal results. But now with the small capacitor, droop, noise and charge injection can deteriorate the circuit functioning heavily. This effect will be observed with circuit implementation in a following chapter.

The mentioned inductor L consists of several transistor parameters. An exact analysis leads to an equation for the inductor as given

$$L = C_\pi r_\pi \frac{R_b}{\beta_0} = \frac{g_m}{2\pi f_T} \cdot \frac{\beta_0}{g_m} \cdot \frac{R_b}{\beta_0} = \frac{R_b}{2\pi f_T}. \tag{41}$$

As can be seen, the inductance changes with the value of f_T which on its turn depends on the tail current. In order to get some insight in these values a plot of the f_T and L as a function of the tail current is given in Figure 32.

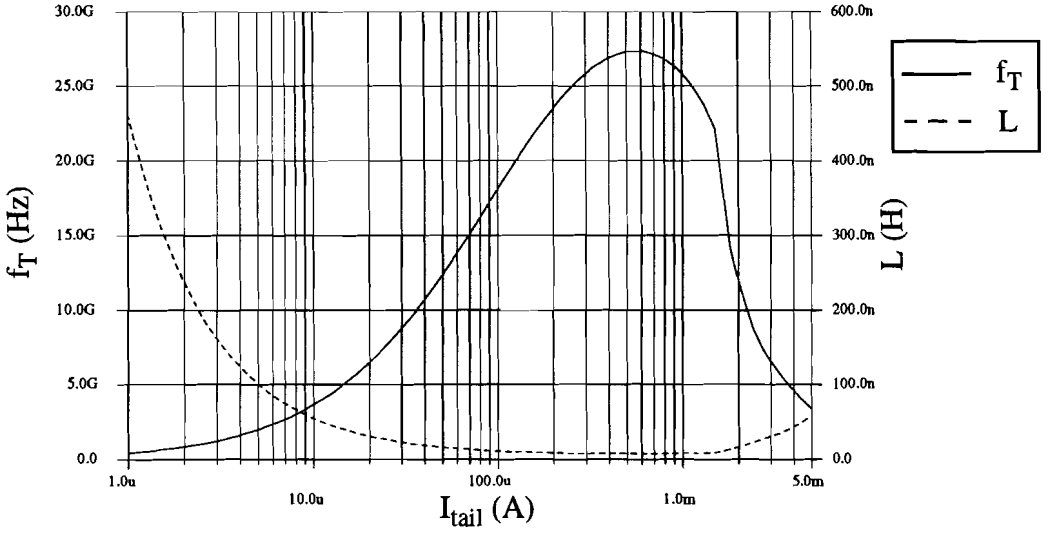


Figure 32 Inductance and f_T of the switching transistor vs. tail current

As can be seen from this figure there is an optimum inductance between 0.5 mA and 1 mA, in this domain is the switch operating. Also can be seen that the inductance is a function of f_T and R_b. If R_b is smaller than f_T is larger as mentioned before, this will lead to a double reduction of the inductance. If this could be accomplished the circuit operation would improve.

4.4 Clock Buffer Design

The clock buffer decides whether the circuit is in track or hold mode. The input signal of the clock buffer is an external sine wave with a frequency equal to the desired sample

rate. The sine wave is superposed on a DC voltage. The buffer circuit [12] is illustrated in Figure 33. The first part of the circuit consists out of two levelshifts, T_1 with T_3 and T_2 with T_4, which are integrated for the case that the clock buffer is controlled with an ECL buffer. If now the input signals are applied directly to the clock buffer then a DC voltage of 3 V is required to obtain a suitable input voltage for the differential pair T_8 and T_9. The amplitude of the sine wave does not have to be large, 0.15 V amplitude is enough to switch the differential pair, T_8 and T_9.

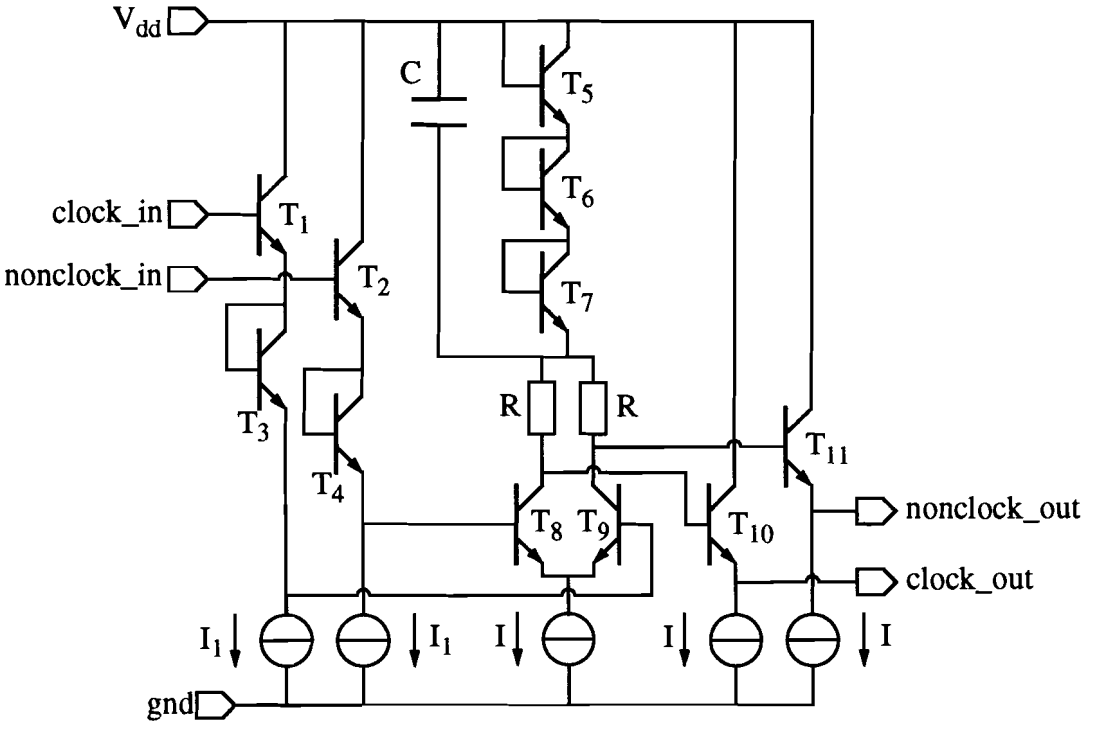


Figure 33 Clock buffer configuration

The tail current I_1 for the levelshifts can also be small, a value of 100 µA is chosen. The emitter size of these levelshifts can be small, here 0.8µmx2µm. As mentioned before the switching transistors are driven with voltages between 1.2 V and 1.5 V. This means that the output buffer must have output voltages switching between these values. Also the emitter followers T_{10} and T_{11} are needed at the output in order to reduce the influence of the switch transistors on the clock buffer (signal). Counting backwards, it is concluded that the base voltages of T_{10} and T_{11} must have a value switching between 2.075 V and 2.375 V with a base emitter voltage of 0.875 V. If the 0.3 V switching voltage is realized with the resistors R then a gap of 2.625 V has to be filled between the resistors and the supply voltage V_{dd}. This gap can perfectly be filled with a diode string of three base-emitter voltages of T_5, T_6 and T_7, size 1µmx4µm. The differential pair has also a 1µmx4µm emitter size.The capacitor C is set at 2 pF and is integrated in order to sustain the DV voltage better at this point. The tail current I is set at 1 mA and the resistors R are

chosen to be 350 Ω. This leads to a slightly larger switching voltage for which is chosen to compensate for internal losses. The emitter size of the output emitter followers has been set at 1.2μmx10μm in order to create a strong buffer. The circuit has been simulated at a 1 GHz input frequency, the results, given in Figure 34, are satisfying.

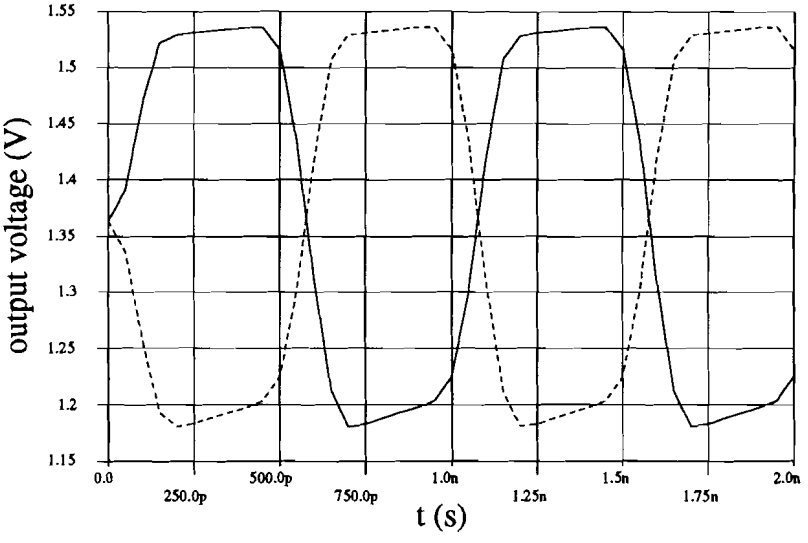


Figure 34 Clock buffer output signals vs. time

4.5 Bias Voltage Circuit Design

In the total track-and-hold circuit several current sources are used. These current sources are controlled with a bias reference voltage. In order to guarantee a proper functioning of the circuit this bias reference voltage needs to be constant with respect to temperature and supply voltage variations. This bias voltage has to be realized without external signals, excluding the ground and the supply voltage. In order to realize a constant reference voltage, temperature and supply voltage variations must be taken into account. The bias voltage circuit [12] is shown in Figure 35. This circuit configuration is chosen because it has proven its reliability in the past. In order to get some insight into the operation of the circuit, some calculations will be done. Applying the Kirchhoff potential equations for the loop, in which T_{10}, R_2, T_9, R_3, T_6 and T_{13} are included, leads to the following equation:

$$V_{be,\mathrm{T10}} + I_{R2} \cdot R_2 + V_{be,\mathrm{T9}} + I_{R3} \cdot R_3 - V_{be,\mathrm{T6}} - V_{be,\mathrm{T13}} = 0. \tag{42}$$

If base current loss is neglected and the transistors are assumed to be identical 1μmx4μm then the follwing equation is valid due to the parallel connection of T_{10}, T_{11} and T_{12}:

$$V_{be,\mathrm{T6}} = V_{be,\mathrm{T10}} + \frac{kT}{q}\ln(3), \tag{43}$$

which is also valid for T_9 and T_{13}. If R_2 and R_3 are identical and $I_{R2} \approx I_{R3}$, controlled by R_3, the circuit is almost independent of the supply voltage. The capacitor C_1=8 pF is

implemented in order to reduce the effects of spikes on the supply voltage.
The above mentioned results in

$$I_{R2}R_2 + I_{R3} \cdot R_3 = \frac{kT}{q}\ln(9). \tag{44}$$

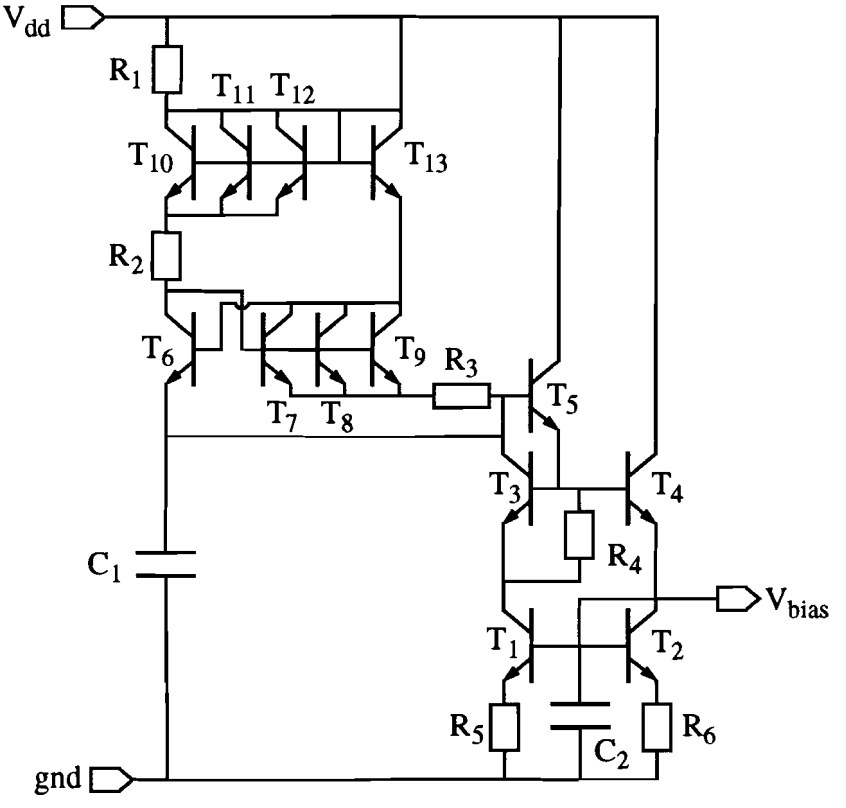


Figure 35 Bias reference voltage configuration

Now the temperature dependency of the bias voltage in this circuit must be investigated. The current flowing through a bipolar transistor is described with

$$I = I_0 \cdot \left(e^{\frac{qV_{be}}{kT}} - 1 \right), \tag{45}$$

in which

$$I_0 = CT^{\alpha} e^{-\frac{qV_g}{kT}}. \tag{46}$$

In (46) C is a constant depending on the transistor size, V_g=1.2 V is the bandgap voltage of silicon and T^{α} represents the temperature dependence of I_0 with α is 1.8 according to [13]. Neglecting the -1 term in (45) because the diode is forward biased, results in the following derivative of the current I with respect to the temperature:

$$\frac{dI}{dT} = I\left(\frac{\alpha}{T} - \frac{q(V_{be} - V_g)}{kT^2} + \frac{q}{kT}\frac{dV_{be}}{dT}\right). \tag{47}$$

From (47) the temperature dependence of V_{be} is derived, resulting in

$$\frac{dV_{be}}{dT} = \frac{k}{q}(1-\alpha) + \frac{V_{be} - V_g}{T}. \tag{48}$$

This leads to $\left.\frac{dV_{be}}{dT}\right|_{T=298K} = -1.3$ mV/K, if R_2 and R_3 are set at 180 Ω. Now the temperature dependence of V_{be} is known, the influence on the collector current of T_1 has to be investigated. The collector current through T_1 is described with

$$I_{c,T1} = I_{R2} + I_{R3} + \frac{V_{be,T3}}{R_4}, \tag{49}$$

which can be replaced by

$$I_{c,T1} = \frac{kT}{qR_2}\ln(9) + \frac{V_g - 1.3 \cdot 10^{-3}T}{R_4}. \tag{50}$$

Eliminating all terms of (50) except V_g, results in a resistance ratio R_4/R_2 of 6.9 and now the collector current can be expressed as

$$I_{c,T1} = \frac{V_g}{R_4}, \tag{51}$$

which should be independent of the temperature. In practice (simulation) a resistance ratio of 6.5 showed better performance, resulting in R_4 is 1175 Ω. Simulations with these values and R_1= 6300 Ω and R_5=R_6=210 Ω, have shown an almost constant current.This collector current is given in Figure 36.

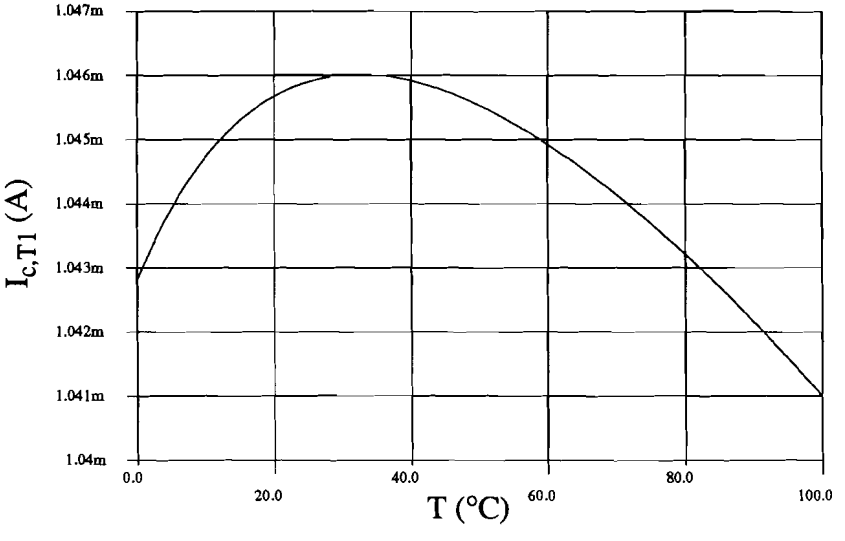


Figure 36 Collector current of a bias circuit vs. temperature

As can be seen the collector current is not fully independent of the temperature, but the accuracy is within 1% over a large temperature range. Simulations have shown that this is enough for the 10 bit track-and-hold circuit. The supply voltage dependence of the collector current is also 1% for voltages above 4.9 V. For a supply voltage below 4.9 V the

accuracy decreases rapidly because of the piling of several base-emitter voltages. The capacitor C_2=5 pF has been integrated in order to reduce the influence of internal voltage peaks due to switching.

5 Circuit Configuration of the Total Track-and-Hold

At first sight, for the total track-and-hold circuit several configurations are possible. Some of these architectures are treated in this chapter. All the building blocks are explained in Chapter 4.

5.1 Basic Track-and-Hold Configuration

As before mentioned, the basic track-and-hold circuit consists of an input and output buffer with a switch in between and of course the bias voltage circuit and the clock buffer. As described in Chapter 4, a suitable input buffer is the linearized unity gain buffer of paragraph 4.2.3. In this configuration, shown in Figure 37, this buffer is also used as output buffer. It may be clear that the actual design is a differential circuit of which now only one side is illustrated.

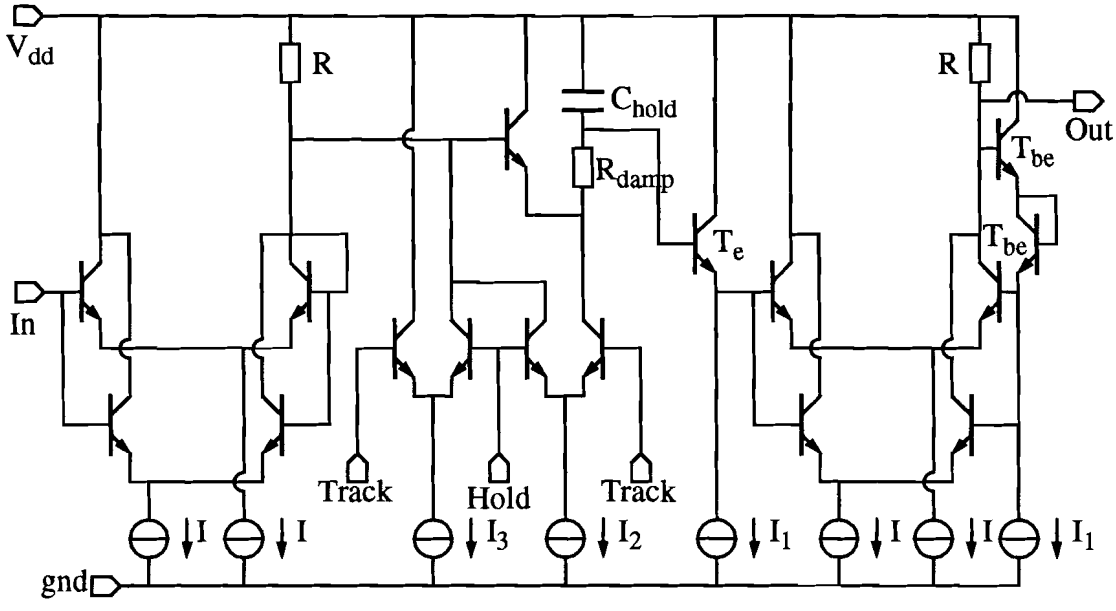


Figure 37 First track-and-hold configuration

In this circuit, after the hold capacitor an emitter follower T_e is integrated in order to reduce the single-ended droop rate, due to the relatively large base current of the output buffer. Due to the switch and the emitter follower, the DC level decreases twice the base-emitter voltage. In Chapter 4 it was made clear that the, in Figure 37 used, buffer was dependent of the DC voltage. Thus the DC output voltage of the output buffer has to be corrected with two base-emitter voltages T_{be}, as in Figure 37. The switch has been realized with an extra current for the hold mode in order to reduce the switch input voltage enough in the hold mode. The distortion is determined by taking samples of a certain width at the end of the hold periods. These samples are Fourier transformed resulting in the desired frequency spectrum.
Unfortunately, this circuit does not meet the device specifications. The reason for this is

charge injection due to unequal and signal dependent voltage drops in the transient from track to hold mode. The charge injection is due to the voltage drop over the base-emitter capacitance, resulting in a voltage drop over the hold capacitance.

5.2 Basic Track-and-Hold Configuration with Feedback

In order to make the charge injection signal independent a feedback has been applied to the circuit of Figure 37 resulting in the circuit of Figure 38. As can be seen, the output of the total circuit is fed back to the input of the switch with the help of a transistor T_f.

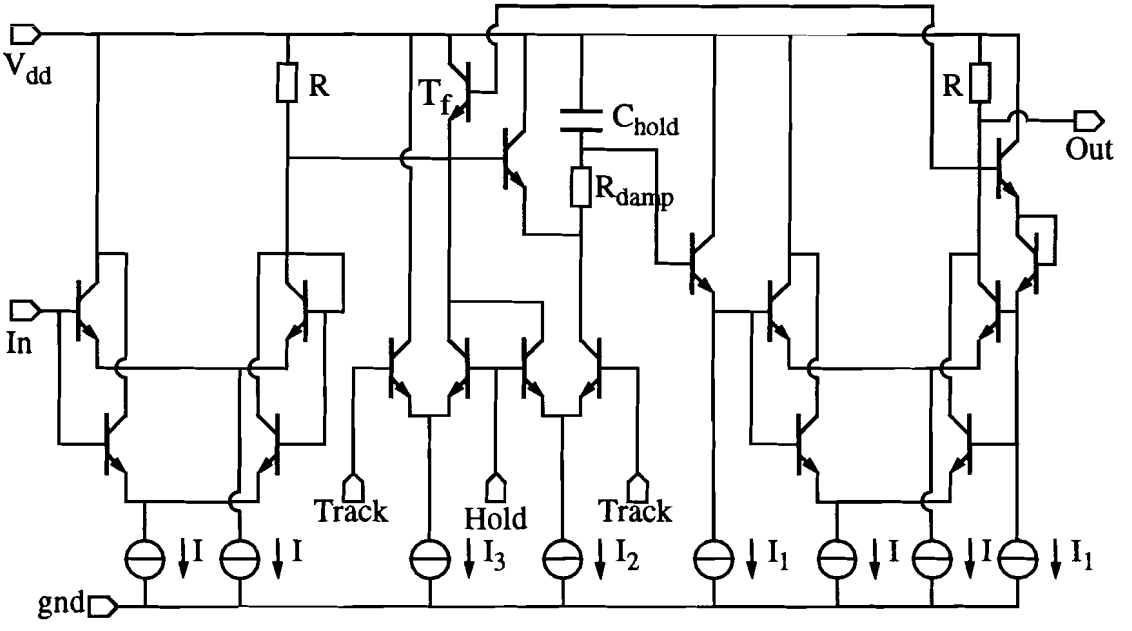


Figure 38 Second track-and-hold configuration with feedback

In track mode the feedback transistor T_f is off and the circuit operates the same as the previous circuit. But in hold mode, the large hold current pulls the switch input voltage down to exactly one base emitter voltage below the output voltage. Now, in hold mode, the switch input voltage is equal to the switch output voltage resulting in an opened switch. The circuit operation is kept the same as before, but now the voltage drop over the base- emitter capacitance of the switch is set at one base-emitter voltage resulting in a signal independent charge injection.
However this transistor feedback results in an oscillation as treated in Paragraph 4.3, because the feedback transistor also operates as a switch. The capacitive load is formed by all the parasitic capacitances connected with the emitter of the feedback transistor. Also the levelshift at the end of the output buffer appears to be oscillating. Damping all the oscillations would lead to a complex web of damping resistors. Therefore another solution has to be found.

5.3 Upgraded Track-and-Hold Circuit

In the previous track-and-hold circuits the output buffer caused oscillations due to levelshifts. These buffers were also very linear for high frequencies. But after sampling, in the hold mode, the frequency of the information holding signal is very low, it is determined by the single-ended droop rate. So actually the output buffer does not have to meet the specifications demanded on the input buffer. By integrating another output buffer the problem of the levelshift is solved. The buffer of Paragraph 4.2.1 is very linear for low frequencies and therefore suited for this circuit.

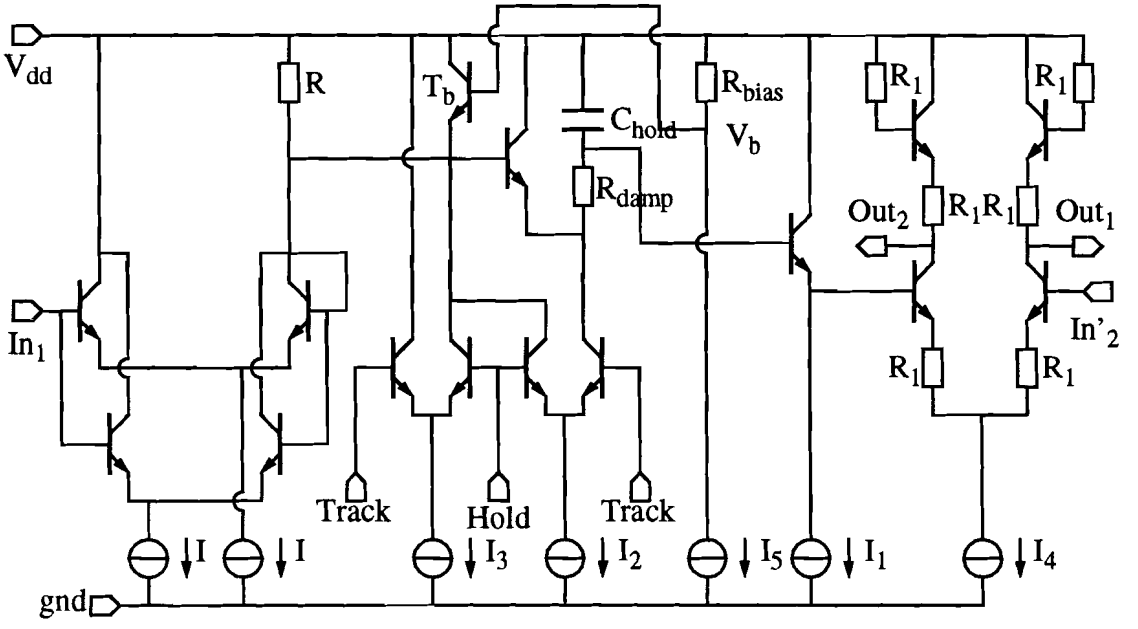


Figure 39 Upgraded track-and-hold circuit

The charge injection is now controlled with a switching transistor T_b of which the base is connected to a bias voltage V_b. In the hold mode the input voltage always drops to a voltage set at the bias voltage minus the base-emitter voltage of the switching transistor. The voltage drop is not signal independent as in Paragraph 5.2 but the voltage at the input of the switch is constant for and during all hold modes in contrast with the circuit from Paragraph 5.1. With this the distortion due to charge injection is limited below the specifications of the 10 bit resolution 1 GHz sample rate track-and-hold circuit. By choosing a minimum size transistor for the hold mode bias function, oscillations have been reduced to a minimum. The simulation results of this circuit meet the specifications. The differential output of the total system (see Appendix E) and the sample moments at the end of the hold periods are given in Figure 40. In this figure the track period and the hold period can clearly be seen. Also a small voltage drop due to charge injection can be observed. The total differential peak-to-peak output is not exactly 2 V, this can be ascribed to the gain in the buffers which is smaller than one.

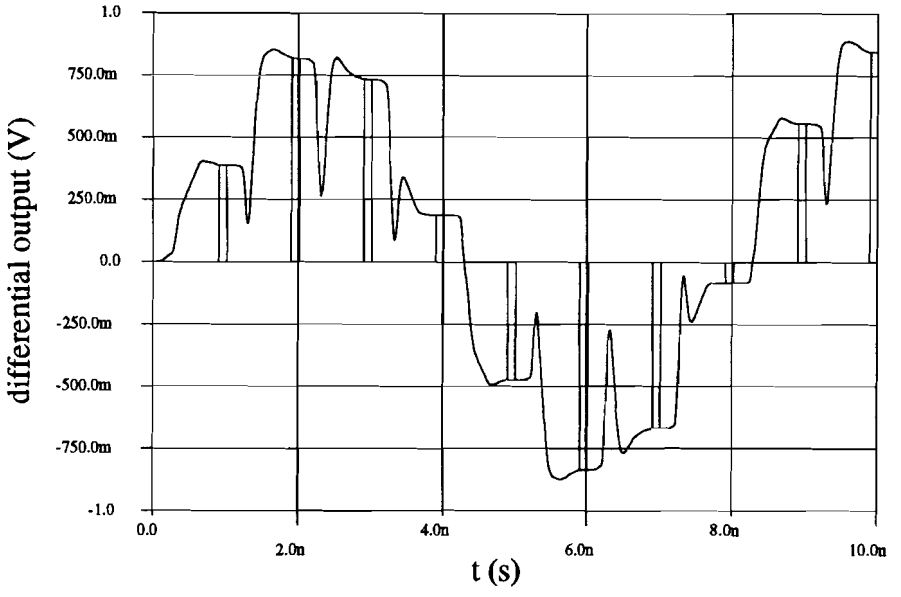


Figure 40 Differential output of the total track-and-hold circuit

For several signal frequencies the distortion is measured by means of simulation. These results are given in Table 2.

Table 2 Simulation results of the track-and-hold operated at 1 GHz sampling frequency

f (MHz)	HD2 (dB)	HD3 (dB)	HD5 (dB)
30	-95	-80	-83
50	-103	-79	-83
110	-114	-79	-82
230	-102	-77	-81
490	-107	-73	-77

From Table 2 it is concluded that the circuit design meets the distortion specifications. The distortion is even less than required for a 10 bit resolution, this was done in order to build in a safety margin for process matching. Now the distortion results are satisfying, the noise specifications have to be checked. For this, an AC noise analysis is done by means of simulation. The results of the circuit noise density and noise voltage on the hold capacitor are given in Figure 41. Only the noise on the hold capacitor cannot be removed after sampling, the noise of the output buffer can be filtered off at the input of a following circuit for example an analog-to-digital converter. As can be seen from this figure the noise voltage does not exceed 500 μV rms which is below the demanded specification of 564μV rms from Paragraph 4.1. From the above it is concluded that the designed track-and-hold does meet the specifications.

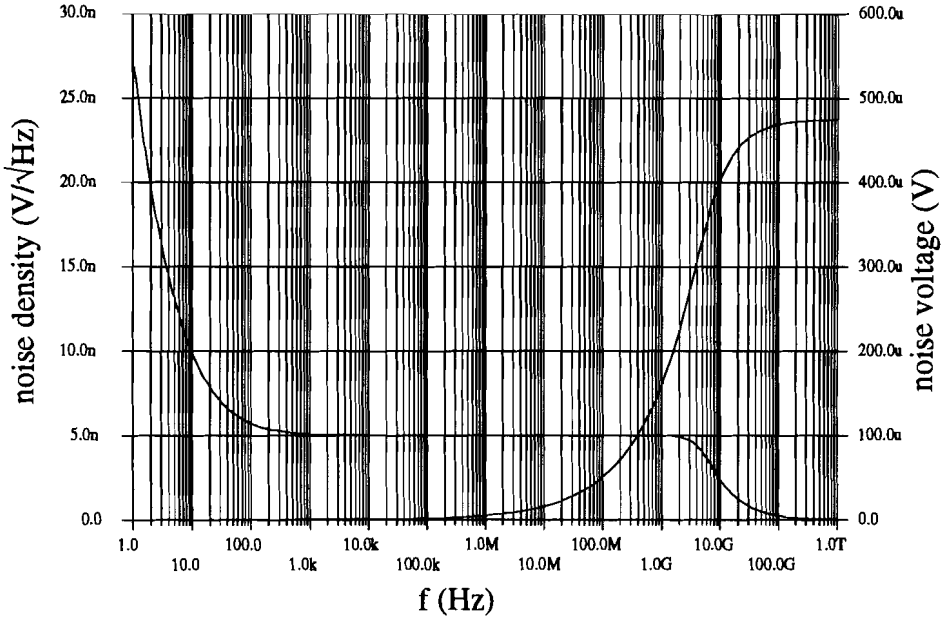


Figure 41 Noise results of the track-and-hold circuit

6 Testing the Track-and-Hold Circuit

Testing of this high speed track-and-hold circuit is done with the use of a cascade of two track-and-hold circuits. Accurate information about the sampled (hold) signal is obtained if the two circuits are operated with different clock signals. This information in the hold mode is important for an application in which the next circuit block is an analog-to-digital converter. Also an output buffer with a 50 Ω output resistance is needed in order to make good measurement possible and in order to drive the capacitances of the bonding pads. Such a 50 Ω buffer could also be used if the track-and-hold circuit is connected to another stand alone IC with respect to the bonding pad capacitances. The signal to be measured must be single ended, so a differential-to-single transformation has to be done. This can be done with the help of a transformer. The measurement setup is illustrated in Figure 42.

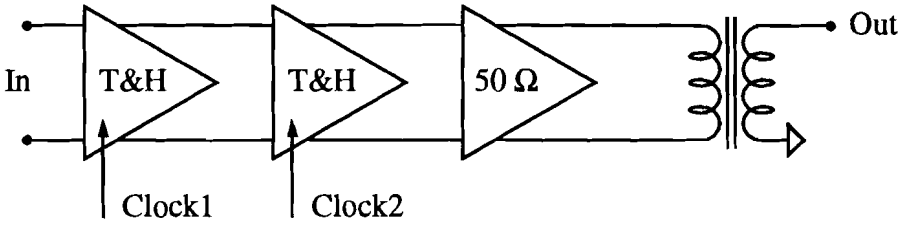


Figure 42 Measurement setup

For low frequency measurements, the 50 Ω buffer could also be replaced by emitter followers with a relative large bias current in order to drive the capacitances of the bonding pads.
The measurement is based on sub-sampling of the output of the first track-and-hold circuit. This is done by the second track-and-hold circuit, which has a 180° phase shifted clock signal with a lower frequency. The clock signals are illustrated in Figure 43.

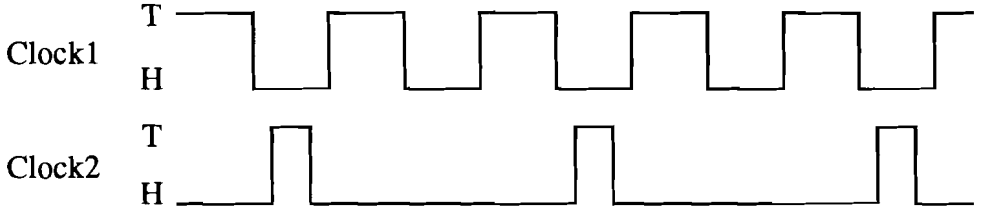


Figure 43 Clock signals in the measurement setup

By clocking the circuit like this, the signal information is not lost but the frequency at the output has changed into $f_{out}=f_{clock2}-f_{in}$. If the input frequency f_{in} is 495 MHz and the frequency of *Clock2* 500 MHz, then the signal information of the input signal is found back in a 5 MHz signal. Given this low frequency output, the 50 Ω buffer only needs to be

very linear in that frequency range. The problem with this 50 Ω buffer is to realize it in a 5 V process. A buffer which might meet the 10 bit resolution specification is the translinear buffer of Paragraph 4.2.1, with a few modifications. The modified translinear buffer is given in Figure 44.

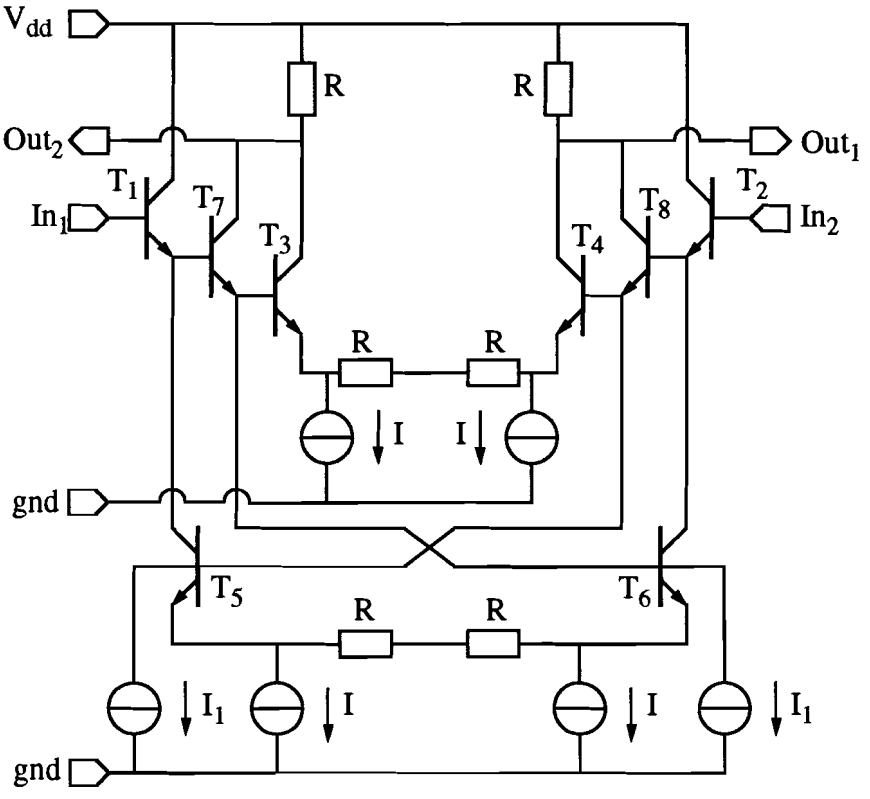


Figure 44 Translinear 50 Ω buffer

As can be seen from Figure 44, the tail currents *I* here are not flowing through the degeneration resistors. With this an extra voltage drop is saved. The resistors *R* are chosen to be 100 Ω in order to establish the 50 Ω output impedance. The tail currents *I* are set at 8 mA and the current I_1 is set at 400 µA. The transistors are all maximum size, 1.2µmx10µm, and the transistors T_1, T_2, T_3, T_4, T_5 and T_6 are set four times in parallel in order to minimize base current modulation. The results, given in Figure 45, are satisfying. But in these simulations the buffer is operated at a 3.9 V DC voltage and with large currents resulting in large base currents. These large base currents may not affect the output buffer of the second track-and-hold circuit. For this reason, two emitter followers are integrated in front of the buffer. The DC output voltage of the second track-and-hold is 3.6 V minus to emitter followers resulting in 1.9 V. The DC voltage to control the 50 Ω buffer is now too low. This can be solved by adjusting the supply voltage of the buffer with -2 V. Inherently, the applied substrate voltage is also set at -2 V. This measure is not necessary if the output is formed by emitter followers only. The integrated emitter followers do not have any effect on the circuit functioning. However the voltage adjustment does lead to two extra voltage pins at 3 V and -2 V, but this is of no concern because this

implementation is only needed on the test chip. Because of the large currents and the voltage adjustment in the 50 Ω buffer, an extra bias voltage circuit should be implemented with this buffer in order to control the large current sources.

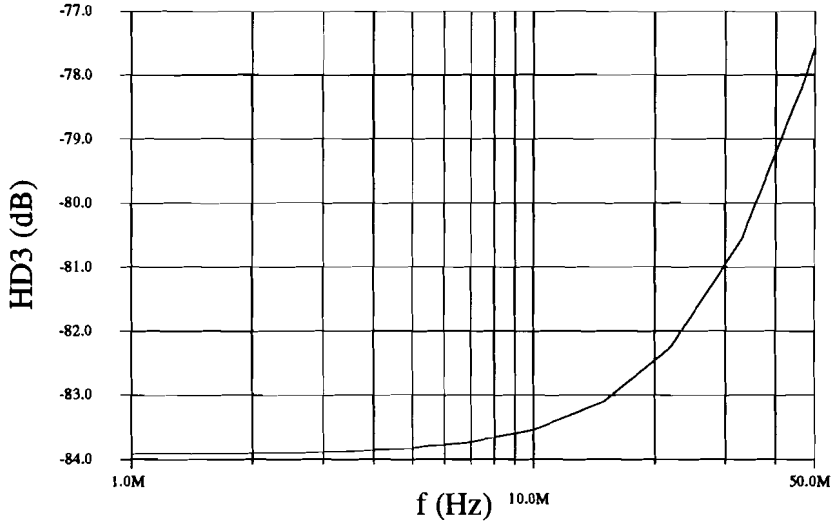
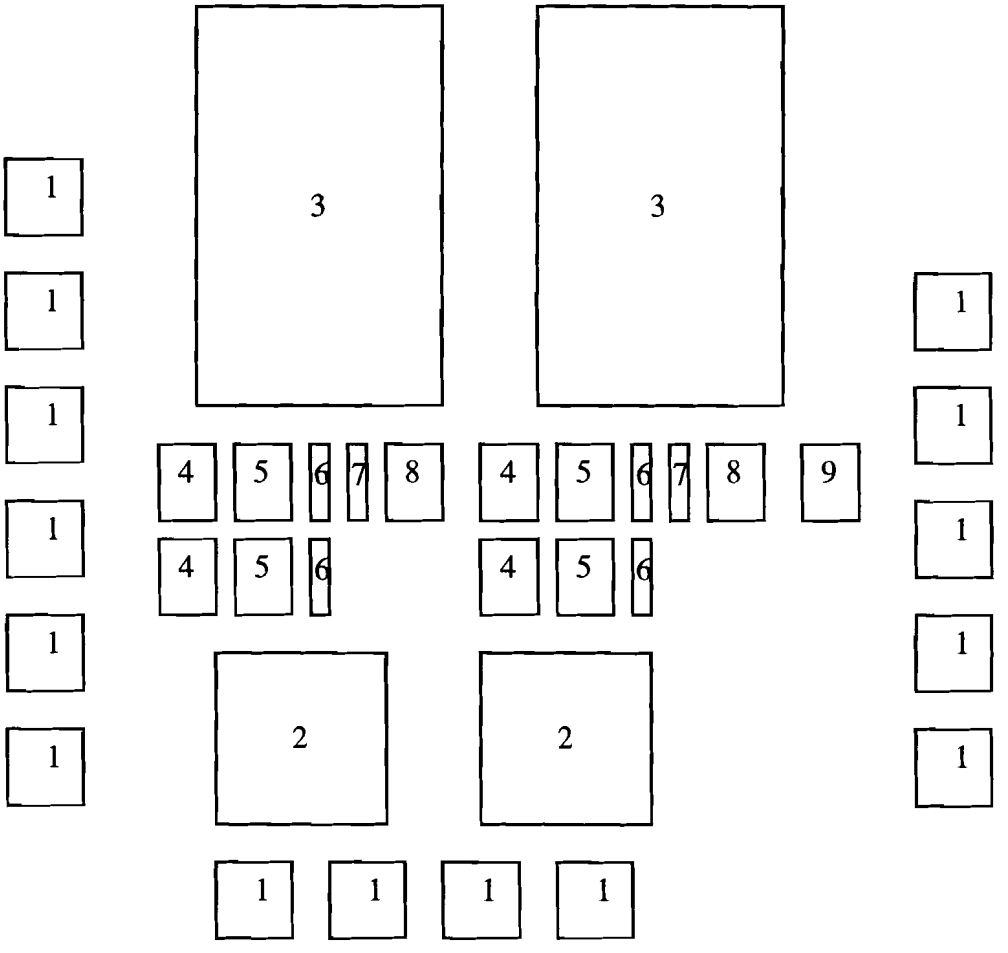


Figure 45 HD3 of the 50 Ω buffer for low frequencies

In the test configuration some adjustments in the second track-and-hold were needed also. The DC output voltage of the first track-and-hold circuit is 3.6 V.
For this reason the DC voltage of the input buffer of the second track-and-hold circuit had to be adjusted from 4 V to 3.6 V. This is done by increasing the resistor from 1000 Ω to 1400 Ω. In order to speed up the track mode a little bit, the tail current has been increased from 1 mA to 2 mA. The resistor must now be reduced to 700 Ω. These changes have been implemented and checked, they did not affect the circuit operation with respect to distortion and noise.

7 Layout

The performance of the track-and-hold circuit is not only determined by the used components and their parameters together with their implementation, but also by the circuit layout. Matching of components is determined by the process matching. From this point of view the components with very high acquired matching accuracy should be placed side by side in order to reduce mismatch. To meet this mismatch reduction, the circuit has been designed using a mirror between the differential subcircuits. To give some insight into the layout of the track-and-hold circuit a block diagram is given in Figure 46.



1. bonding pad
2. clock buffer
3. bias voltage circuit
4. input buffer
5. switch
6. emitter follower
7. DC feedback
8. output buffer
9. 50 Ω buffer/emitter followers

Figure 46 Block diagram of the IC layout

The layout of the block diagram of Figure 46 has been established and is illustrated in Figure 47. The total die area is 1.4mmx1.6 mm. The die area of the actual track-and-hold circuit without bonding pads, measurement circuit, clock buffer and bias voltage circuit is only 0.3mmx0.3mm. The chip area of this track-and-hold ($0.09mm^2$) has been improved compared to the chip area used in [6] ($0.25mm^2$).

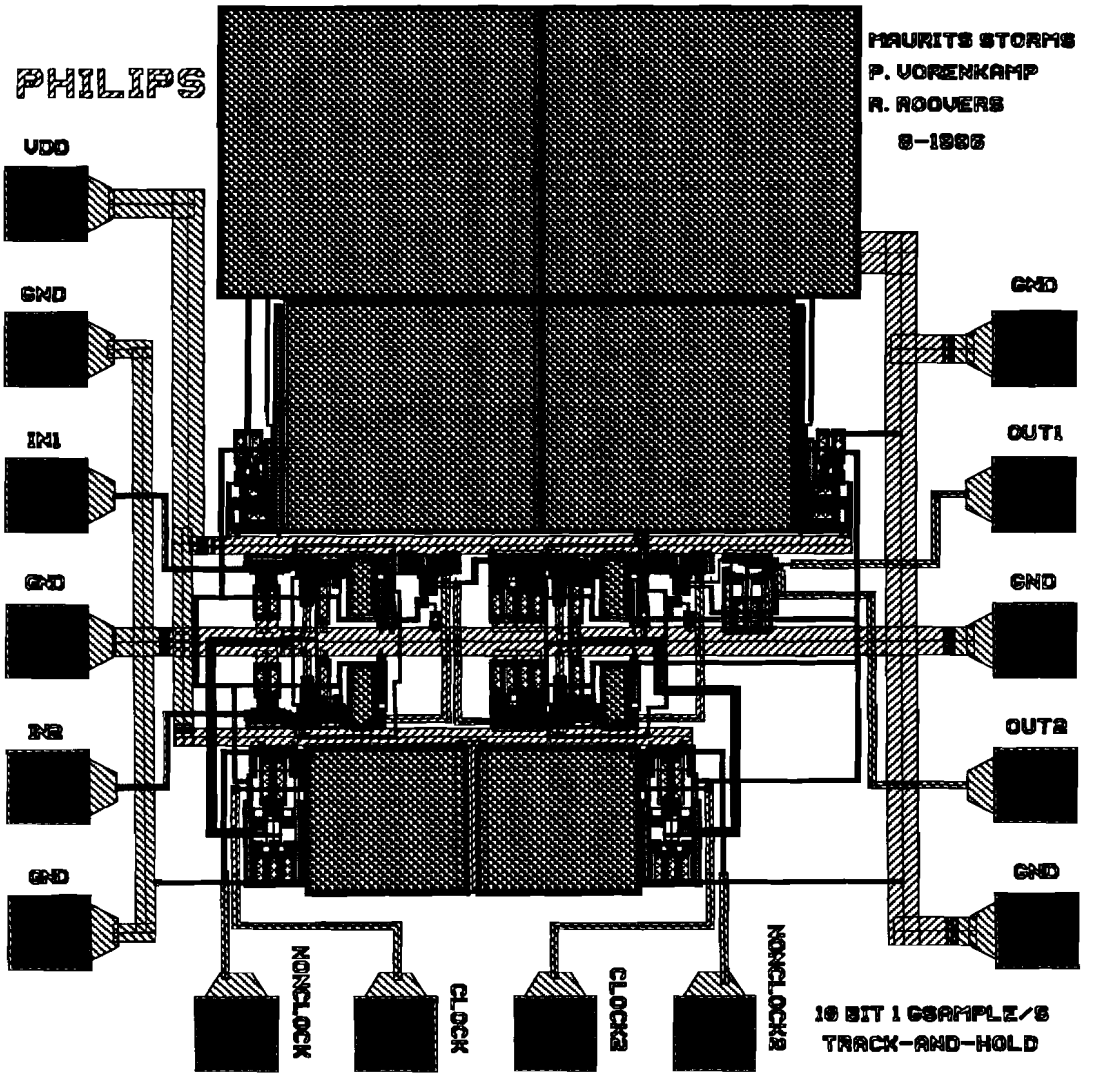


Figure 47 Total IC layout of the track-and-hold and measurement circuit

Conclusions

The analysis and design of the track-and-hold circuit with high speed and high resolution have been performed. The simulations of the subcircuits and the total design have shown satisfying results. A measurement setup has been proposed and a circuit layout has been designed. About the design and implementation of a track-and-hold circuit, the following conclusions can be stated:

- A differential single channel track-and-hold configuration is preferred to a differential interleaved track-and-hold configuration. With respect to an interleaved circuit the demand for process matching is too high for todays technology.
- For a track-and-hold circuit with a large bandwidth, noise contribution must seriously be taken into account.
- Parasitic capacitances and base-emitter modulation are the dominating distortion effects in the several buffers which were treated. Analysis has shown that the distortion can be calculated by developing a few Taylor series far enough. The distortion is modeled with a few small equations.
- The smallest and simplest circuit has proven to be the fastest and most linear circuit. The linearity has been established by the sum of two shifted transconductances, which leads to a more linear transconductance around zero.
- If a transistor is used as a switch and operated at high frequencies, then it shows inductive behavior. Connecting a capacitor to this switch leads to oscillations. In order to damp the oscillations a damping resistor must be implemented. Due to these oscillations the capacitance must have a small value.
- The small hold capacitor value leads to large voltage drops due to charge injection and hold mode feedthrough. To reduce the influence of these artifacts the off-voltage must be set at a constant value.
- Testing the high speed track-and-hold circuit with todays measuring devices is not possible without the help of a second track-and-hold and the use of subsampling.
- The total design has a distortion below -72 dB over a 500 MHz full-Nyquist bandwidth. Because process matching is taken into account, there is a margin of 10 dB.

Reviewing the conclusions and the simulation results, it is concluded that the design of this track-and-hold circuit appears to be a promising approach to further design of high performance track-and-hold circuits. Measurements will have to confirm the obtained simulation results.

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Appendix A Gain Error Calculation

In order to calculate the maximum allowable gain error between the two interleaved tack-and-hold circuits a worst case analysis is needed. With the help of (A.1) and (A.2), which give insight into the behavior in the frequency domain, this calculation can be done.

$$Y_{T\&H1}(f) = \frac{\sin\left(\pi f \frac{T_s}{2}\right)}{\pi f T_s} \sum_{n=-\infty}^{\infty} X\left(f - \frac{n}{T_s}\right), \tag{A.1}$$

$$Y_{T\&H2}(f) = \frac{\sin\left(\pi f \frac{T_s}{2}\right)}{\pi f T_s} \sum_{n=-\infty}^{\infty} X\left(f - \frac{n}{T_s}\right) e^{-jn\pi}. \tag{A.2}$$

In the calculation the distortion between the input signal f_x and the signal f_s-f_x, where f_s is the sample rate. The worst case is determined by choosing a high signal frequency which results in a low frequency signal f_s-f_x. The gain is introduced as a constant B. The distortion is calculated as follows:

$$D = 20\log\left(\frac{B \cdot Y_{T\&H1}(f_s - f_x) + Y_{T\&H2}(f_s - f_x)}{B \cdot Y_{T\&H1}(f_x) + Y_{T\&H2}(f_x)}\right), \tag{A.3}$$

which results in

$$D = 20\log\left(\frac{B \cdot \frac{\sin\left(\pi(f_s - f_x)\frac{T_s}{2}\right)}{\pi(f_s - f_x)T_s} - \frac{\sin\left(\pi(f_s - f_x)\frac{T_s}{2}\right)}{\pi(f_s - f_x)T_s}}{B \cdot \frac{\sin\left(\pi f_x \frac{T_s}{2}\right)}{\pi f_x T_s} + \frac{\sin\left(\pi f_x \frac{T_s}{2}\right)}{\pi f_x T_s}}\right). \tag{A.4}$$

For a 10 bit resolution, D=-61.96 dB, f_x=499 Mhz and f_s=500 Mhz, the gain constant has been calculated at B=1.00102. This means that for the proposed circuit a maximum gain error of 1.02‰ between the two interleaved track-and hold circuits may occur.

N.B.: If the track-and-hold circuit is used in front of an analog-to-digital converter, then the sinc-function can be neglected, (A.4) results in (A.5)

$$D = 20\log\left(\frac{B-1}{B+1}\right), \tag{A.5}$$

in which B=1.0016 for a 10 bit system, so the maximum allowable gain error is 1.6‰.

Appendix B Duty-Cycle Error Calculation

In order to calculate the maximum allowable duty-cycle error in the multiplexer of the interleaved track-and-hold circuit a duty-cycle error x has been introduced together with the worst case analysis from Appendix A. The duty-cycle for the track-and-hold circuits is as illustrated in Figure B.1.

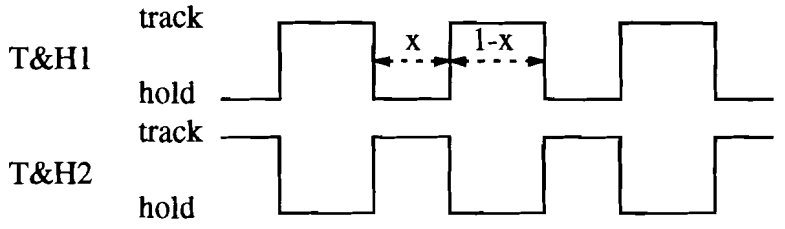

Figure B.1 Duty-cycle configuration

For calculation of the duty-cycle error (A.1) and (A.2) are used, but they are changed into:

$$Y_{T\&H1}(f) = \frac{\sin(\pi f T_s x)}{\pi f T_s} \sum_{n=-\infty}^{\infty} X\left(f - \frac{n}{T_s}\right), \tag{B.1}$$

$$Y_{T\&H2}(f) = \frac{\sin(\pi f T_s (1-x))}{\pi f T_s} \sum_{n=-\infty}^{\infty} X\left(f - \frac{n}{T_s}\right) e^{-jn\pi}. \tag{B.2}$$

The total distortion calculation results in:

$$D = 20\log\left(\frac{\dfrac{\sin(\pi(f_s - f_x)T_s x)}{\pi(f_s - f_x)T_s} - \dfrac{\sin(\pi(f_s - f_x)T_s(1-x))}{\pi(f_s - f_x)T_s}}{\dfrac{\sin(\pi f_x T_s x)}{\pi f_x T_s} + \dfrac{\sin(\pi f_x T_s(1-x))}{\pi f_x T_s}}\right). \tag{B.3}$$

For a 10 bit resolution, D=-61.96 dB, f_x=499 Mhz and f_s=500 Mhz, the duty-cycle error has been calculated at x=0.499746. This means that for the proposed circuit a maximum duty-cycle error of 0.508‰ in the multiplexer may occur.

Appendix C Gain and Duty-Cycle Error

In order to calculate the maximum allowable gain error B between the two interleaved track-and-hold circuits combined with the maximum duty-cycle error x in the multiplexer, a worst case analysis is needed. With the help of (A.1) and (A.2), which give insight into the behavior in the frequency domain, this calculation can be done.
The gain error (see Appendix A) and the duty-cycle error (see Appendix B) are combined into one distortion calculation as in (C.1).

$$D = 20\log\left(\frac{B\cdot\frac{\sin(\pi(f_s-f_x)T_sx)}{\pi(f_s-f_x)T_s}-\frac{\sin(\pi(f_s-f_x)T_s(1-x))}{\pi(f_s-f_x)T_s}}{B\cdot\frac{\sin(\pi f_xT_sx)}{\pi f_xT_s}+\frac{\sin(\pi f_xT_s(1-x))}{\pi f_xT_s}}\right) \qquad \text{(C.1)}$$

Here also a worst case analysis is done with respect to the frequency. For a 10 bit resolution, D=-61.96 dB, f_x=499 Mhz and f_s=500 Mhz, a domain is marked in which the combination of the two errors is small enough. This is illustrated in Figure C.1.

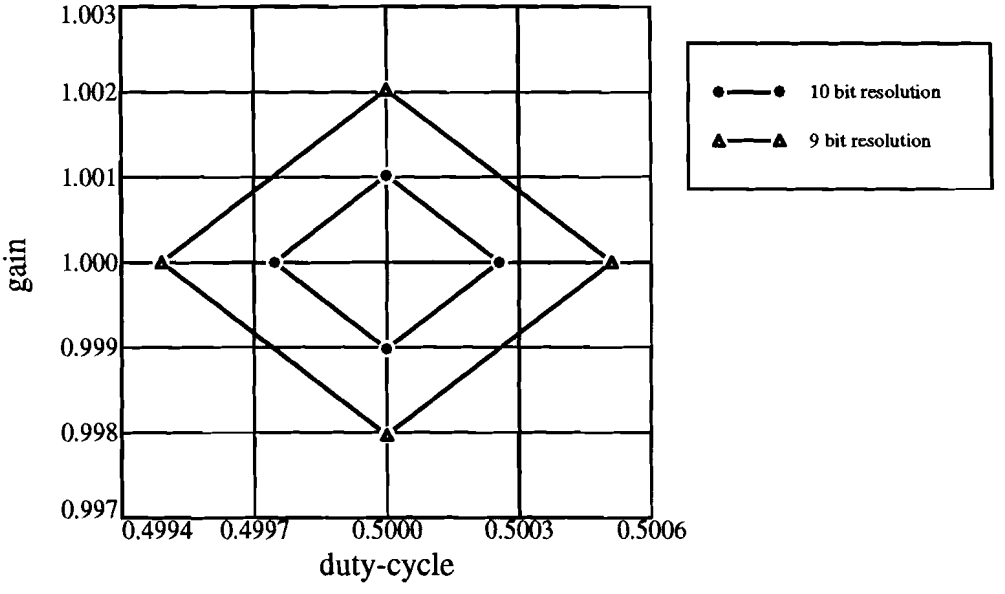

Figure C.1 Combined gain and duty-cycle error

Appendix D Bipolar Transistor Formulas

Here f_T is defined as the frequency at which beta is reduced to 1, with V_{bc}=0.

Effective base resistance near peak f_T:

$$R_b = R_{bc} + \frac{R_{bv}}{1 + \frac{V_{de}C_{je}}{Q_{b0}}} \tag{D.1}$$

Base-emitter diffusion capacitance:

$$C_d = \frac{g_m}{2\pi f_T} \tag{D.2}$$

Extrinsic input bandwidth:

$$F_v = \frac{1}{2\pi R_b(2C_{jc} + C_{je} + C_d)} \tag{D.3}$$

Extrinsic output bandwidth (for 1 V_{pp} output swing):

$$F_{out} = \frac{I_{cp}}{2\pi C_{js}} \tag{D.4}$$

Ratio of effective and theoretical transconductance:

$$\frac{g_{meff}}{g_m} = \frac{1}{1 + g_m R_e} \tag{D.5}$$

Frequency at which noise figure starts increasing:

$$F_{0.5} = 0.1\sqrt{\frac{f_T}{4\pi R_b(C_{jc} + C_{je})}} \tag{D.6}$$

Appendix E Total Track-and-Hold Circuit