MASTER

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Award date:
2001

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13th August 2001

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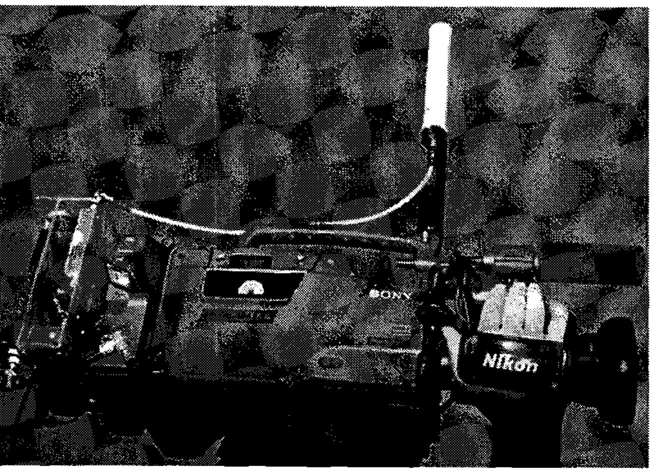
DVCpro video codec interface for digital radio cameras

D.J.F. van Kemenade

Abstract—**The design of an interface for a DVCpro video oder/decoder in a digital radio camera system is discussed. he compressed video data is split and transmitted via two VB-T channels. Emphasis is on some high-speed hardware esign considerations and problems encountered in interfacng with the codec. Improvements in the field of error protecion and concealment for a second-generation DVCpro system re proposed.**

I. Introduction

THIS report describes the work that has been carried out during my graduation project at the Research & Develpment department of the British Broadcasting Corporation BBC) in Kingswood Warren, Surrey, UK. BBC R&D caries out strategic research in order to give competitive adantage to the BBC.



ig. 1. MPEG prototype digital radio camera

1.1. Background of the project

BBC R&D is developing a digital radio camera for use in roduction of live television programmes. Essentially a raio camera is a regular television camera in which the ideo cable has been replaced by a radio link in order to ive the cameraman more freedom of movement.

Until recently only analogue radio cameras were availble. The main problem is that multipath reception derades their performance. Generally directional antennas ith steering personnel are needed to avoid this, which is ostly and prevents wider acceptance of radio cameras in elevision production. A digital transmitter can overcome hese problems because its digital modulation scheme can erform much better in multipath conditions. The project ision is that eventually virtually all television cameras will e cordless. The BBC has successfully built and demonstrated a first-generation digital radio camera prototype (Fig. 1) [1]. It has been shown that the system can be used outdoors as well as indoors, which was previously difficult using analogue radio cameras. The project has given the BBC the desired competitive advantage in this field. To date no publications about similar systems from others have been found.

1.2. Need for a low-delay video coder

An essential part of a digital radio camera is the video coder. It compresses the digital video signal so that the data rate is reduced to a level that can be handled by the digital radio link. In the first prototype, an MPEG-2 video coder was used. The main disadvantage of this coder is that it introduces a delay of 18 frames. In many television production applications this is impractical. In general radio cameras, external microphones and fixed (zero-delay) cameras are used together. Delays also pose a problem for director-camera interaction and when radio cameras are used on an outside broadcast location when they contribute to a studio programme. For example, when a person filmed on location with a radio camera is being interviewed from the studio, there will be a long pause before the interviewee starts answering a question. As a result, a low coding delay is an important constraint. No specific maximum acceptable value for the coding delay was given for this project.

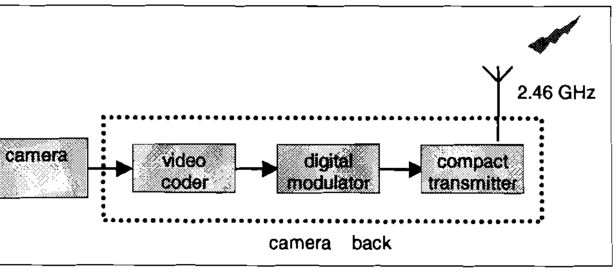
BBC programme makers started to like using the prototype digital radio cameras and there was increasing pressure on BBC R&D to quickly develop a new prototype with a small coding delay. An existing compact low-delay DVCpro codec card from Panasonic was made available to the BBC and so it was decided to base the new prototype on this codec. This report describes the design of a DVCpro interface that is used to connect the codec with the rest of the system.

1.3. Guide to this report

Chapter II describes the main elements of a digital radio camera system and the constraints for each of them. Obviously the choice for the video coder is the most important one in this report. It turns out that DVCpro is a suitable choice. In Chapter III some important design parameters for the DVCpro interface are chosen. They determine the hardware design (Chapter IV) and logic design (Chapter V). As the first generation of the system was built in a hurry, there are improvements that could be made in a second-generation system. They are described in Chapter VI. The most important one is improved error protection. In Chapter VII conclusions are drawn.

II. SYSTEM OVERVIEW

ig. 2 shows a block diagram of the entire digital radio iera. It consists of an existing television camera on ch a camera back unit is mounted. This unit contains video coder, the digital modulator and the transmitter. requirements for each part of the system will be dissed. As this report deals with the video coder, this part l be covered extensively.



2. Block diagram of the digital radio camera

2.1. Camera

n principle any video camera can be used in the system, long as a digital video output is available. In the first EG-2-based prototype, a prototype video coder made by y was used, which had to be used with a Sony SX camder. During operational trials the size and weight of this icorder including the camera back unit have proven to a disadvantage. Also, the recorder unit in the camera is dom used but still consumes power. This is why the BBC chosen for a smaller and lighter dockable camera for second-generation prototype.

2.2. Video coder

This is an essential part of the digital radio camera. It es the uncompressed ITU-601 [2] digital video data from camera and outputs compressed video data with a conerably lower rate to the digital modulator. This is necesy because the data rate of the uncompressed video is 270 it/s, which is too much to be carried on any practical io channel.

There are many considerations that need to be taken into ount when choosing a video coder.

icture quality. For video compression to be effective, e compression scheme will need to be lossy. This means at some picture information will be discarded, potenally leading to a noticeable deterioration of the picture uality. As the BBC wants to produce high-quality televion programmes, the compressed picture quality should pproach the original uncompressed picture quality as uch as possible.

ata rate. The compressed video data rate should ideally as low as possible. This minimises radio spectrum use nd simplifies the design of the radio link. The data rate hould also be constant, as the capacity of the radio chanel is constant and cannot be exceeded.

oding delay. The process of compressing and decomressing one or more video frames introduces a delay beween the uncompressed input picture in the camera and e decoded output picture from the receiver. Too large a delay poses severe difficulties in a television production environment. Typically a radio camera is used together with several cabled cameras and independent microphones with zero delay. The only way to make sure that all incoming sources are time synchronous would be to delay all other sources by the same amount as the digital radio camera. But even in this case there would still be many practical problems as pointed out in Chapter I. For this reason, it is essential that coding delay does not exceed a couple of frames at the most.

- **Availability.** As the BBC wants to start using digital radio cameras as soon as possible, availability of video coders also plays a role. An optimal coder that will take many man-years to develop may not be as attractive as a suboptimal one that is immediately available.

Possible video compression schemes are described in Appendix A.

An existing MPEG-2 coder was used in the first-generation prototype. The main reason was that this was the only compact video coder available at the time (1999). Its picture quality was acceptable. The data rate was around 11 Mbit/s, which is an input rate that can be handled by practical transmitters. The main disadvantage of this coder, however, was the long fixed coding delay of 18 frames (720 ms). Unfortunately it was not possible to modify the Group of Pictures (GOP) structure of the MPEG-2 coder to limit the delay. Programme trials showed clearly that the long delay posed many difficulties, which is why the BBC decided to develop a second-generation digital radio camera with a shorter video delay.

The advantage of a new MPEG-2 encoder would be that many parameters could be changed freely in order to optimise the picture quality/data rate trade-off for the digital radio camera application. The coding delay could be kept within acceptable limits by using I (intra) frame only or a short GOP structure. However, the main problem is that such an MPEG-2 encoder is not yet available as a compact unit so this could only be a long-term solution.

DV does not offer the flexibility to change the data rate according to the application, which is a serious disadvantage. The 50 Mbit/s data rate of DVCpro50 is too high for practical radio channels, but DVCpro25 is just acceptable. On the positive side, compression decisions are optimised for each block so that the overall picture quality is maximised within the 25 Mbit/s limit as a result of the extra features of DV. The coding delay is low (approximately 2.5 frames coding/decoding) because only I frame compression is used. Another significant advantage is that a compact DVCpro codec was readily available for use by the BBC in mid-2000.

For this reason, the BBC decided to choose DVCpro25 video coding for the second-generation digital radio camera (short to medium term). But at the same time, the BBC is working on a new MPEG-2 video coder for a third-generation digital radio camera (longer term) that will be fully configurable according to application-specific needs.

From this point onwards, DVCpro25 will be referred to as DVCpro.

2.3. Digital modulator

A digital modulation scheme is needed for transmission f the video data over the radio channel. The main reuirement for the digital radio link is that it is rugged, even n severe multipath environments. The COFDM (Coded)rthogonal Frequency Division Multiplex) modulation cheme was specifically designed for operation in multipath ituations. It is used in the DAB (Digital Audio Broadcastng) and DVB (Digital Video Broadcasting) standards.

When the BBC's digital radio camera project started in 998, it was decided to use the DVB-T standard [3]. This vas expedient, as there was much DVB-T experience vithin the BBC as it had just launched the first digital terestrial television service worldwide. Another advantage vas that DVB-T receivers were readily available, so that ne project could concentrate on the digital radio camera ransmitter.

DVB-T has many modes with various channel capacities. 'hey range from 4.98 Mbit/s (QPSK rate ½ with ¼ guard nterval) to 31.67 Mbit/s (64-QAM rate ⅞ with $^{1}/_{32}$ guard nterval). This will be discussed further in Section 3.3.

2.4. Compact transmitter

The baseband COFDM signal needs to be up-converted ɔ an RF frequency for transmission. The requirements for ne transmitter is that its size and power consumption hould be as small as possible. The power consumption eeds be limited to avoid excessive thermal dissipation in ne camera back and to maximise battery life.

The BBC has chosen for direct I/Q up-conversion. This voids the need for one or more IF stages. As a result, there re no additional frequency components close to the 'OFDM spectrum so that the output filter does not need to ave tight specifications. Not only does this allow the ansmitter to be smaller, it is also possible to retune the ansmission frequency within a large range.

The power amplifier needs to have a high linearity beause of the modulation scheme that is used. This is a disdvantage because linear amplifiers are less efficient in erms of power. On the other hand, the required output ower for the digital radio camera is much lower than for n analogue one so that overall power consumption remains vithin acceptable limits.

The digital radio camera operates in the 2.45 GHz band, ne lowest allocated band in the UK for video links. These ɔwer frequencies are preferred for mobile links because of ne better propagation in difficult environments.

III. DVCPRO PARAMETERS

Now that the choice for DVCpro video compression has een made, it is useful to take a closer look at the DVCpro lata structure. Information from this chapter will be used to etermine constraints for the hardware (Chapter 4) and ɔgic design (Chapter 5) of the DVCpro video coder.

It will become clear that certain parts of the DVCpro ata do not need to be transmitted. After the net data rate as been determined, an appropriate DVB-T mode will be hosen. Then the data stream will need to be divided into ackets for transmission over the radio link.

3.1. DVCpro data structure

Figure 3 shows the DVCpro data structure. [4].

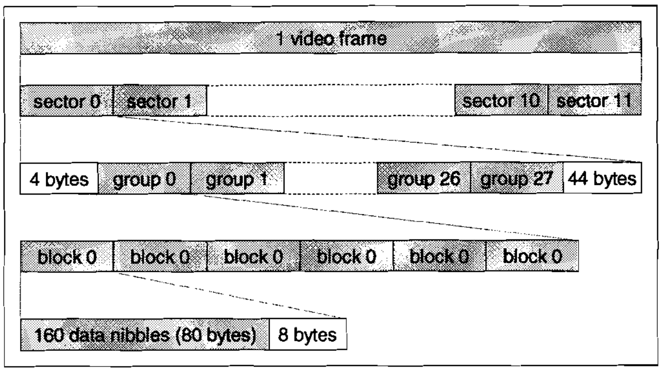


Fig. 3. DVCpro data structure

Each video frame is divided into 12 sectors. Each sector consists of 28 groups and some padding, a number of clocks during which no data is conveyed. Each group is divided into 6 blocks. At the lowest level, each block contains 80 bytes of data. Of those, 77 bytes contain the data of one DCT macro block and 3 bytes contain framing information. The 80 bytes are followed by 8 bytes of padding.

It is no surprise that there are similarities between the DV coding process and the DVCpro data structure. An 8-8 DCT block contains 64 pixels and 8-bit video sampling is used, so a DCT block is 64 bytes when uncompressed. One macro block contains 6 DCT blocks or 384 bytes. One video segment consists of 5 macro blocks or 1920 bytes. Quantisation is now applied to this video segment with an upper limit of 385 bytes after compression. As each block contains 77 data bytes, five blocks are needed to contain one compressed video segment. The sixth one carries audio information or remains unused.

The total number of sectors and groups can be explained as follows. One video frame contains 720 by 576 pixels. Per luminance DCT block there are 64 pixels, so there are 720×576/64 = 6480 luminance DCT blocks. DVCpro uses 4:1:1 colour sampling, so that the total number of DCT blocks is 1.5×6480 = 9720. These make up 1620 macro blocks or 324 video segments. Each segment occupies one block, and there are 12×28 = 336 groups in one frame. This means that there are 12 spare blocks. In every sector, the first block is used for header information.

3.2. Data rate considerations

The rate of the entire DVCpro data stream is 35.5968 Mbit/s. But there are some data categories that can be discarded while retaining the core video data. This is necessary for reliable transmission over the DVB-T channel (see Section 3.3).

First of all, it seems sensible to discard the padding bytes. One should keep in mind that DVCpro is not a transmission standard but a digital videotape standard. The data played back from a tape will always have some jitter, as the tape transport velocity cannot always be perfectly constant for mechanical reasons. The padding bytes allow compensation for data overflows or underflows. In the digital radio camera system, the transmission medium is not tape but a io channel, so the padding bytes can be discarded with- problems. The remaining data rate in that case is 8 bits byte × 80 bytes per block × 6 blocks per group × 28 ups per sector × 12 sectors per frame × 25 frames per ond = 32.256 Mbit/s.

\ further data reduction is possible because not all 168 cks contain audio or video data. 135 blocks contain eo, 9 blocks contain audio and 6 blocks contain header ormation. The remaining 18 are so-called dummy blocks t are not needed in this application, so only 150 groups d to be transmitted. This leads to a data rate of 30×150×12×25 = 28.8 Mbit/s.

n DVCpro the audio signal (48 kHz, 16 bits, stereo) is compressed. The data rate of the DVCpro-audio is 30×9×12×25 = 1.728 Mbit/s. One could decide for alter- ive means to transmit audio information, using a sepa- e compression scheme. In that case the DVCpro data rate uld be reduced to 27.072 Mbit/s.

_astly, the 6 header blocks and the three framing bytes in h block could also be discarded once it is known how to roduce the data they contain at the decoder side of the tem. This would lead to the lowest possible data rate of 77×135×12×25 = 24.948 Mbit/s. This explains why this npression scheme is called DVCpro25.

The BBC decided to use the 32.256 Mbit/s option, carding the padding bytes. This seemed to be the easiest y to get a significant data rate reduction while avoiding ra efforts in distinguishing video, audio, dummy and der blocks, processing audio data and regenerating ning information. At a later stage, it will be recom- nded to make a different choice to accommodate addi- nal error protection for the system.

3.3. DVB-T mode

\s pointed out in Section 2.3, the DVB-T standard is d for transmission of the DVCpro data. DVB-T has ny modes, each with its own data capacity. They depend the modulation system, the code rate and the guard in- val that is used.

The modulation system determines the number of points the constellation: 4 (QPSK), 16 (16-QAM) or 64 (64- M). Higher-order modulation means that there are more sible symbols, which increases the data capacity. How- r, this higher capacity comes at the price of a higher or probability because it is more likely that constellation nts get confused, which leads to transmission errors.

The code rate determines which fraction of the physical io channel capacity is actually used for data transmis- n. The remaining capacity is used to add error protection a. A lower code rate implies less available capacity for nsmission but more error resilience in the system. This is cussed further in Section 6.2.1.

The number of carriers in DVB-T is either 6817 (8K de) or 1705 (2K mode). The 8K mode is suitable for gle frequency transmitter networks as it offers longer so- led guard intervals. The guard interval is the fraction of symbol period where the demodulator waits for all ech- to die away before decoding the symbol. This avoids er-symbol interference (ISI) in multipath transmission situations. A larger guard interval allows for longer echoes to be received without causing ISI. In digital radio camera applications, though, very long echoes do not occur. That is why the 2K mode with a 1/32 guard interval (7 µs) is always sufficient for the radio camera. The 2K mode is also preferred because it has a higher immunity to Doppler multipath than the 8K mode in the microwave bands.

The available net data rates for each mode are listed in Appendix B. It is clear that the data rates of the QPSK and 16-QAM modes are not sufficient to carry the DVCpro data, not even when only the core video data is retained. Some of the 64-QAM modes do have sufficient data rates, but only at high code rates. In fact, only modes with code rate ½ are sufficiently rugged in difficult radio channels. Higher, so-called punctured code rates are achieved by discarding some error-coded information. If at the receiver even more information is lost due to the properties of the channel, only little data is left for reliable reception.

Taking all this into account, 64-QAM with r = ½ and $g = {}^{1}/_{32}$ in 2K-mode is the best choice for the radio camera application. However, in order to carry the 32.256 Mbit/s data rate that was chosen in Section 3.2 *two* DVB-T channels are needed.

3.4. Packet structure

In the DVB-T system, data is sent in 188-byte packets. It is convenient to map the data of one DVCpro sector onto an integer number of packets. For the 32.256 Mbit/s option, 74 packets are needed. The last packet is not filled completely; 0x00 bytes are added.

The following packet structure was chosen by the BBC:

- **Byte 0:** sync word (47hex). This is required by DVB-T.
- **Byte 1-3:** reserved for MPEG interoperability.
- **Byte 4:** validity flag (1 bit) and packet address (7 bits). Sometimes no DVCpro data is available when a packet is sent. In this case the validity flag is set to indicate that this is a dummy packet. The packet address is necessary to identify the packet at the decoder side. Two packet streams will need to be combined and there is a variable delay between them because two receivers are used.
- **Byte 5:** sector address (5 bits) and multiplexing mode (3 bits). The sector address is used again for synchronisation purposes. The multiplexing mode indicates the chosen data rate option from Section 3.2 and the DVB-T mode.
- **B6 – B187:** DVCpro data (182 bytes).

Sending a packet is prompted by a packet clock. The data rate for a 64-QAM r = ½ channel is 18.096257 Mbit/s, so the byte clock is 2.262032 MHz. With 188 bytes per packet, the packet clock needs to be 12.032 kHz. Note that there are two of these channels, so in total 24064 packets are sent per second.

IV. Hardware design

Now that the exact constraints of the system are known, we can start designing a hardware platform that can carry out the required tasks.

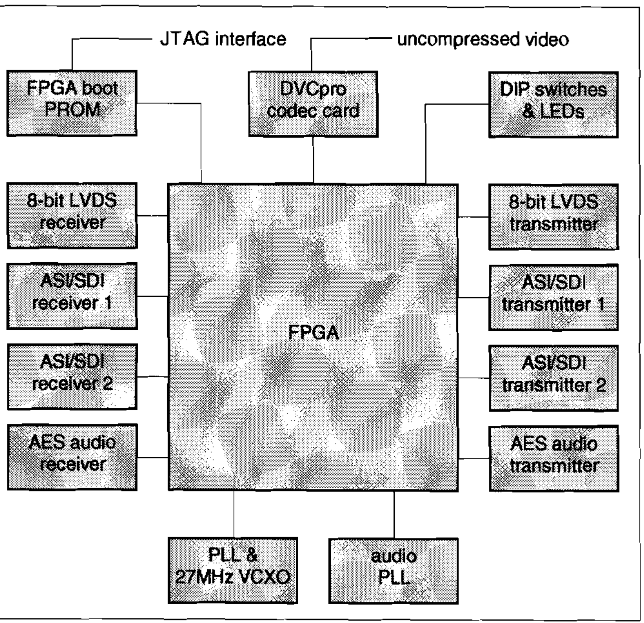
4.1. Hardware overview

The overall function of the hardware is to provide an interface between the existing Panasonic DVCpro codec and he rest of the digital radio camera system. In the transmitter, the interface takes an ITU-601 serial digital video signal and an AES/EBU digital audio signal and puts them nto a suitable format for the DVCpro coder. The comressed DVCpro data is split into two data streams and put nto packets to be transmitted via the two DVB-T modulaors. In the receiver, the DVCpro interface facilitates the nverse process.

The similarity between the interfacing requirements in ransmitter and receiver prompted us to build one hardware latform that can perform both functions. This saved valuble time in the first stage of the development process.)nce the basic system was working, separate and more ompact versions of the two interfaces could be built.

4.2. Design

Fig. 4 is a block diagram of the DVCpro interface card. ll signal processing is carried out in a Field Programmale Gate Array (FPGA) that is connected to many interaces. The FPGA's configuration data is stored in an inystem programmable PROM. There are separate configuations for coder and decoder modes. The FPGA used is a (ilinx Spartan-XL XCS40XL [5].



'ig. 4. Hardware overview

There are two interfaces with the Panasonic DVCpro coec: an uncompressed video bus (8 bits) and a DVCpro data us (4 bits) with some auxiliary signals. The direction of hese two busses can be configured on the codec card acording to the use. The uncompressed video bus is supposed o comply with ITU-601 according to Panasonic's specificaions [4]. The uncompressed parallel video clock frequency s 27 MHz and the DVCpro data clock frequency is 18 ЛHz.

There are three video input interfaces: one LVDS (Low-/oltage Dual Signalling) parallel input and two ASI (Asynhronous Serial Interface) inputs, which can also be configred as SDI (Serial Digital Interface, ITU-601) video nputs. The LVDS input is primarily intended to connect irectly to camera heads with a parallel output. The ASI/SDI inputs can take signals from any digital video source. In decoder mode, they connect to the two DVB-T receivers via the ASI interface. The clock frequency of the ASI or serial ITU-601 signal is 270 MHz.

There is also an LVDS parallel output and two ASI/SDI outputs. In coder mode, the LVDS output sends the DVB-T packets to the modulators. A multiplex signal determines to which of the two modulators the packet is sent. Alternatively, the two ASI outputs can be used to send the packets to external standard DVB-T modulators. In decoder mode, the SDI outputs carry the decoded uncompressed video signal.

Furthermore there are AES/EBU audio input and output interfaces for coder and decoder modes respectively. A specialised PLL IC generates a 24.576 MHz audio clock that is locked to the 27 MHz video clock. The phase of the incoming audio clock is arbitrary and generally not locked in any way to the video clock. Therefore an asynchronous sample rate converter is integrated into the digital audio receiver. The serial audio data is read out from the IC with the audio clock using the audio clock generated on the DVCpro interface card.

There is also a second PLL and a 27 MHz oscillator. In decoder mode, it locks the internal 27 MHz clock to the sync bytes from the received packets.

Functions implemented in the FPGA can be controlled by some DIP switches. For debugging purposes, some LEDs and logic test ports are connected to the FPGA.

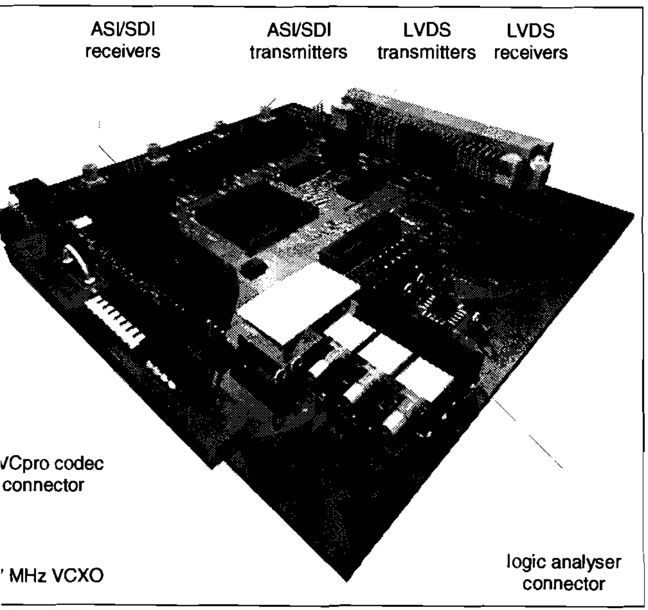
A disadvantage of using the same interface board for both coding and decoding is that in a given mode, many parts of the circuit will not be used. Especially in coder mode this is a problem, because it is a requirement that the radio camera power consumption is kept to a minimum, as seen in Section 2.4. To achieve this, the circuits that are not used in coder mode are powered through FETs. Their gates are connected to the FPGA, from where they are controlled.

4.3. High-speed design considerations

The clock speeds of the signals that are processed on the card are high. Therefore careful hardware layout design is required.

All high-speed signals come together in the FPGA. Therefore it is placed in the middle of the board (see Fig. 5), so that all PCB tracks are as short as possible. This minimises crosstalk between signals and avoids signal reflections. Termination of TTL signal tracks is not needed.

Apart from the track length, it is also important that track crossings are kept to a minimum. This not only limits interference, it also minimises the number of PCB layers that is required, saving PCB cost. Luckily the approximately 220 signal I/O pins on the FPGA can be chosen freely, apart from incoming clock signals. They should be connected through dedicated Global Clock (GCK) pins that are internally connected to short delay, small skew buffers and nets. Incoming signals are likely to be distributed over many Configurable Logic Blocks (CLBs) that contain the logic gates.



5. DVCpro interface board without codec card

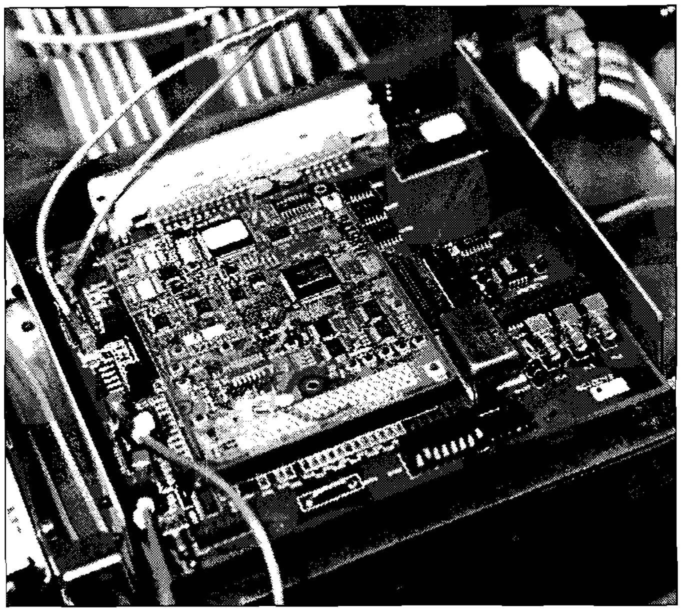


Fig. 6. DVCpro interface card with codec card

The four 270 Mbit/s ASI/SDI interfaces require special
ntion because of the high frequencies involved. The
rfaces use Cypress Hotlink serial-to-parallel and paral-
to-serial converters [6]. To avoid electromagnetic inter-
nce, the input/output connectors are placed as close to
se chips as possible. Furthermore, pulse transformers are
d for cable-chip coupling. They provide isolation be-
en the cable and the circuit, have good common-mode
se rejection and they are a balanced-to-unbalanced con-
ter: the chip connections are balanced, but a normal 75
ms BNC cable is used to interface to other equipment.

The other video interfaces use parallel LVDS [7]. This is
efficient way to transmit high-speed signals over short
ances, in this case from camera to video coder and from
eo coder to DVB-T modem. Because LVDS uses differ-
ial signalling it provides good common-mode noise re-
ion. However, to ensure this, the pairs of differential
ks must be routed as close together as possible and they
st be equally long. As LVDS offers good protection
inst noise, it can use low voltage swings. This enables
h signalling speeds (more than 400 Mbit/s), but more
ortantly for this application the power consumption is
remely low. The two differential signal tracks at the
DS receiver need to be terminated to their characteristic
erential impedance, as close to the receiver as possible.
s is necessary to close the current loop, and prevents
nal reflection that interferes with succeeding pulses.
per termination also reduces electromagnetic interfer-
e with other signal tracks. Normally 100 Ohms termina-
n is used. The differential track pair should be designed
uch a way that its characteristic impedance is 100 Ohms
well. This is achieved by choosing suitable dimensions
the tracks as a function of the distance between them,
PCB height and the relative dielectric permittivity of the
B material.

V. Logic design

Now suitable interfaces are in place to connect the external signals to the FPGA, where the processing is carried out. In this Chapter we will see what processing is needed in coder and decoder modes.

5.1. Overview

5.1.1. Coder mode

Fig. 7 shows the block diagram of the logic when the DVCpro interface is used in coder mode.

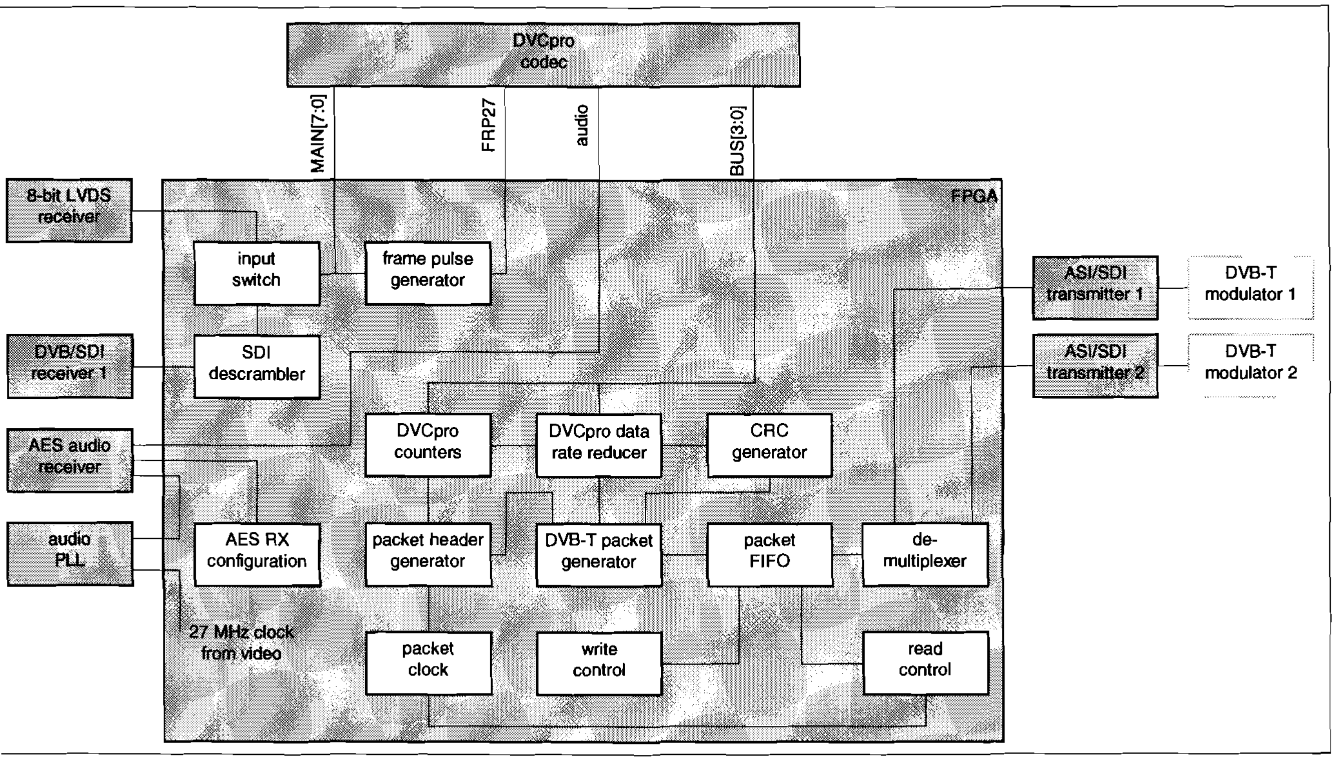
If the parallel LVDS input is used, the digital video signal is sent directly to the DVCpro codec. If the ASI/SDI serial video input is used, the signal must be descrambled first. An additional signal that indicates the start of the video frame needs to be generated. This is discussed further in Section 5.2.1.

The AES receiver/rate converter requires a master clock with frequency $512F_s$ = 24.576 MHz, with sample frequency F_s = 48 kHz. This clock is generated by the audio PLL IC from the 27 MHz video clock. A simple configuration block sends a serial control data stream to the IC to put it into a mode in which it generates right-justified serial audio data. This is the format required by the DVCpro codec. This configuration happens only once.

The compressed DVCpro data is used by a set of counters to keep track of the current sector, group, block and data nibble within the block. This is needed to determine which data nibbles are transmitted and which are discarded, according to the chosen data rate option (see Section 3.2).

The sector counter is also used by the packet header generator, together with a packet clock counter. The packet header followed by the DVCpro data and the two CRC (Cyclic redundancy check, see Section 6.3.1) bytes that have been generated from this data are formatted into DVB-T packets and stored in a FIFO memory.

The FIFO is read out using the packet clock. If no valid packets are available at any moment, a dummy packet is sent instead. The packet de-multiplexer sends the packets from the FIFO to the two DVB-T modulators alternately.



'ig. 7. Logic block diagram (coder mode)

5.1.2. Decoder mode

Fig. 8 shows the block diagram of the logic when the)VCpro interface is used in decoder mode.

The signals from the two DVB-T receivers are fed in usng the ASI/SDI inputs. There will be a variable delay beween the two packet streams. To compensate for this, the ackets are stored in two FIFOs. Then they are read out in he right order using the decoded packet headers, so that ıe two streams can be recombined.

However, some data was discarded to save bandwidth. It ; reconstructed in the DVCpro framer, with the help of a et of DVCpro counters that keep track of the current secor, group, block and data nibble. The data stream and)VCpro counters are also used by the CRC checker to drive n indicator that signals whether the data have been reeived and recombined correctly.

The packet clock is retrieved from one of the streams and sed in a PLL to generate the 27 MHz system clock.

The serial digital audio signal from the DVCpro codec oes not need any processing as it is sent to the AES transnitter. The codec board sends a right-justified audio stream nd this is accepted by the AES transmitter. The video sigal from the codec, however, is not readily usable. The TRS enerator ensures that the video output is ITU-601 complint. This is discussed further in Section 5.2.2. The data is crambled before it goes to the serial AES/SDI video output.

5.2. Design

5.2.1. FRP27 generator (coder)

'he DVCpro coder requires a rising signal at the start of a ideo frame, or a frame pulse, called FRP27. This function ; achieved by decoding the TRS (Time Reference Signal) equences that are multiplexed into the ITU-601 signal [2]. ι TRS sequence consists of four hexadecimal words:

FF 00 00 XY

The system works with 8-bit video signals. In this case the TRS consists of the following bytes:

FF = 11111111
00 = 00000000
00 = 00000000
$XY = 1\ F\ V\ H\ (V \oplus H)\ (F \oplus H)\ (F \oplus V)\ (F \oplus V \oplus H)$

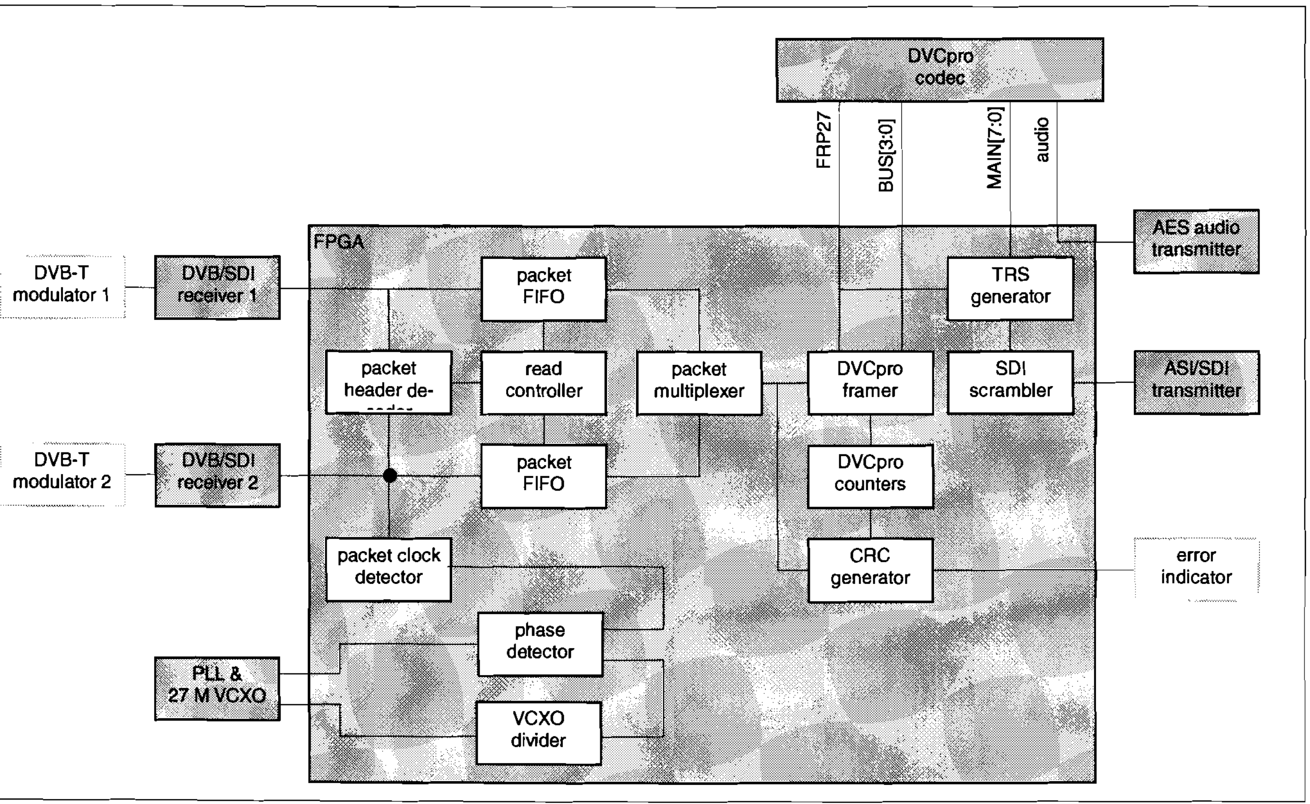
F is "0" during the first field, V is "1" during the field-blanking interval and H is "1" at the start of the line-blanking interval. The four least significant bits provide some Hamming error-protection for the F, V and H bits.

Each line contains two TRS sequences: the SAV (Start of Active Video) TRS is multiplexed into the video stream immediately before the active line data, the EAV (End of Active Video) TRS immediately follows the active line data. There are 1440 bytes in the active line data (720 pixels, 4:2:2 sampling) and 288 bytes in the line-blanking.

It is clear that the start of a frame coincides with a rising edge in the F (field) bit. The FRP27 (coder) generation function can be implemented using a four-byte pipeline in which the three previous bytes are stored. If the previous bytes are FF, 00 and 00 respectively, bit 6 of the current byte contains F. This is the required FRP27 (coder) signal.

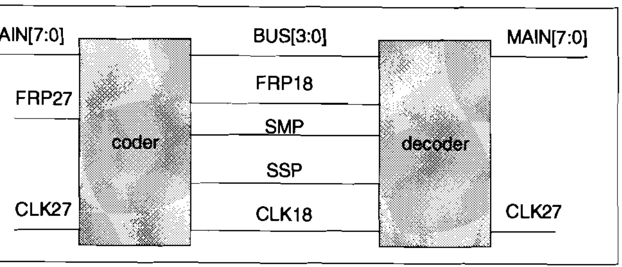
5.2.2. Panasonic interfacing issues

When design on the DVCpro started, only little was known about the details of the interfaces on the Panasonic codec. This board was originally designed for internal use by Panasonic in its DVCpro equipment so there was no extensive information for other users. Obviously there are many things that can go wrong in the whole chain between the DVCpro coder output and the DVCpro decoder input,

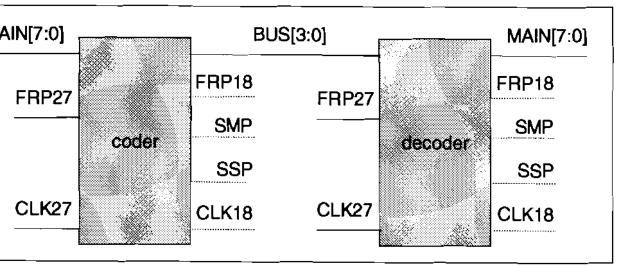


. **8.** Logic block diagram (decoder mode)

›efore work on all that started it seemed useful to first try coder and decoder "back-to-back". This turned out to be ambitious project in itself.



9: Back-to-back test: expected situation



10: Back-to-back test: actual situation

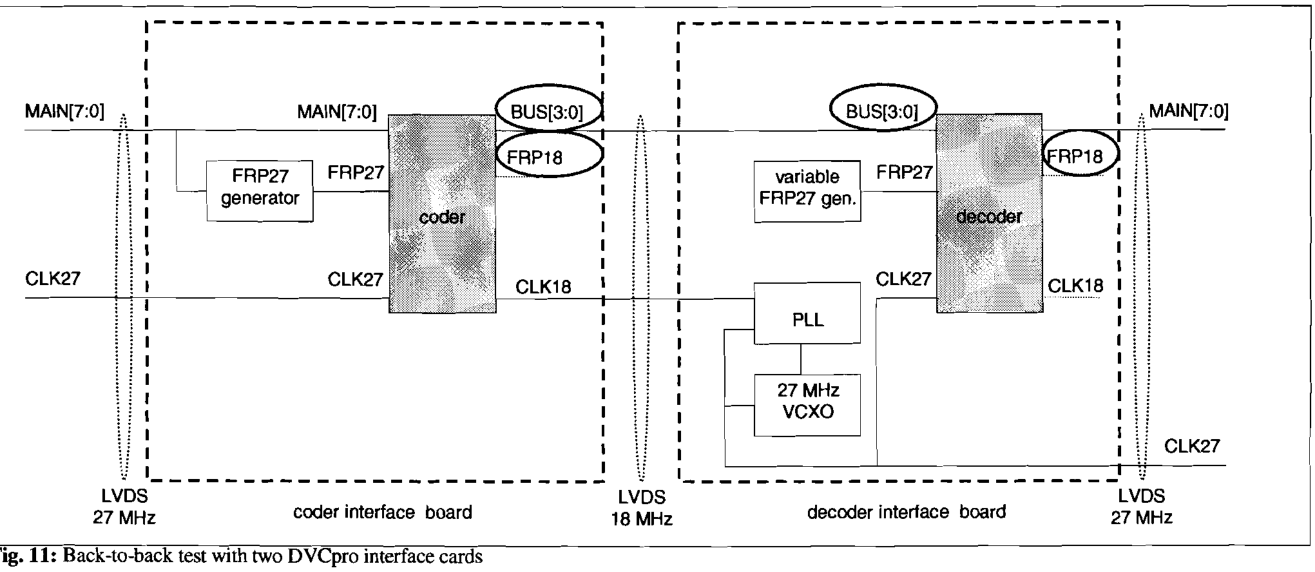
Dne would expect that a back-to-back test of the two les would be as simple as shown in Fig. 9. The incoming eo source is MAIN[7:0] with its associated clock K27. The FRP27 frame pulse has been discussed in Sec- 1 5.2.1. The DVCpro compressed data appears on 'S[3:0] and is associated with an 18 MHz clock, CLK18. P18 is a frame pulse aligned with the compressed frame. IP (Start Mark Pulse) signals the start of a DVCpro block 1 SSP (Sector Start Pulse) is self-explanatory. It would 'e been easy if these coder-generated signals could be fed ıight into a decoder, and that 8 bits of uncompressed video together with a clock signal would appear at its output.

Unfortunately, this was not the case. In fact the directionality of only the MAIN[7:0] and BUS[3:0] busses changes according to the codec function, all the others remain the same. The actual situation is displayed in Fig. 10.

At the decoder, it is obviously confusing to have an 18 MHz-based BUS[3:0] that is clocked in using a CLK18 that the decoder itself generates, while we have to supply a 27 MHz clock. It was even more unclear how FRP27 should be generated on the decoder side. Presumably this arrangement has been designed for use in DVCpro video recorders and camcorders, but for our non-standard application a solution had to be found.

A series of tests was carried out to acquire the necessary information. The test setup is shown in Fig. 11. Only BUS[3:0] and CLK18 were sent from the coder to the decoder interface card. It would have been impossible to send the CLK27 across from the coder card, as the coder card output bus and the decoder card input bus both needed to be clocked at 18 MHz. However, in the wireless application this would not have been impossible anyway. Instead, the internal 27 MHz VCXO on the decoder card was used in conjunction with the PLL to lock it to the incoming 18 MHz clock. This VCXO-generated 27 MHz clock was connected to CLK27 on the decoder. Then it was ensured that the resulting CLK18, generated by the decoder, was in phase with the CLK18 from the coder. As a result, the BUS[3:0] was known to be fed into the decoder reliably. In the real decoder design, the 18 MHz clock is not available but the same result can be achieved by using the received packet clock as the reference instead.

Regarding the frame pulse, a logic block was created that allowed to generate a FRP27 signal with a delay that could



'ig. 11: Back-to-back test with two DVCpro interface cards

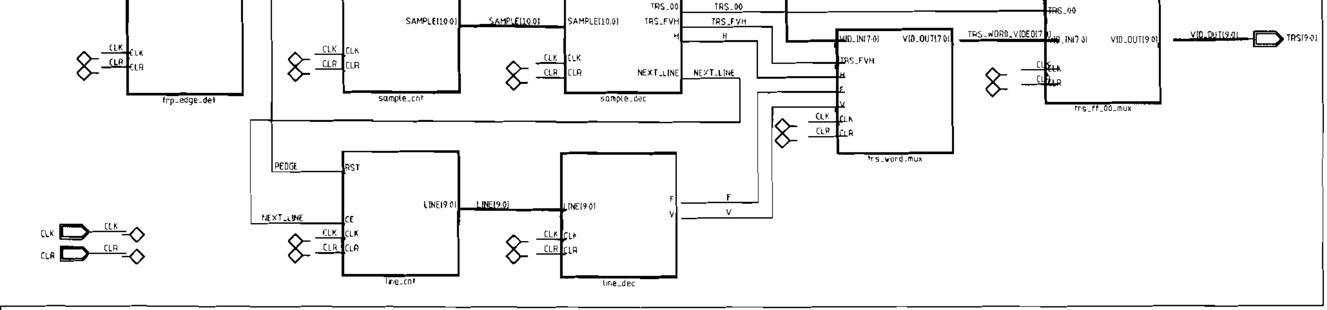
e chosen freely. The uncompressed video output of the ecoder was connected to a monitor. The FRP27 phase was hosen in such a way that the FRP18-BUS[3:0] timing relaionship at the decoder corresponded with the one at the oder. It was expected that this would make the test picture ppear on the monitor, but there was nothing there. Shiftng FRP27 some clock periods backwards or forwards via ne DIP switches did not seem to make any difference.

It was difficult to solve this problem that was supposed to e the easiest one to start off with, before the really difficult rork of splitting and recombining data streams began. 'hings were made more difficult because a large chain of ubsystems was tested at once. It consisted of a video test ard generator followed by several converters to obtain a arallel LVDS video source, on the coder card: input interaces, the coder itself and output interfaces, on the decoder ard: input interfaces, the decoder itself and output interaces, and a second string of converters to go from parallel .VDS video to the SDI-compatible monitor. The series of xternal video converters was checked and found to work vhen the two DVCpro interface cards were taken out of the ystem. However, there could still be interfacing problems n the inputs and outputs of both cards. It was impossible to reak the system down into smaller parts; there was no refrence coder or decoder available.

The only option left to narrow the problem down was to se only one DVCpro codec card and one interface card for coding *and* decoding, so that connection difficulties between two interface cards were excluded. In principle this was possible, as the Panasonic codec card can be configured as a combined coder/decoder in DVCpro25 mode. However, some hardware modifications were necessary to facilitate this. But it was worthwhile. In the two-card setup, the uncompressed video output on the decoder did not show any coherent pattern. In the one-card test, ITU-601-like video data could be seen on the output. Only the TRS bytes were missing. This explained why the monitor had not shown any pictures previously.

So the video interface on the Panasonic card was not ITU-601-compliant as promised in the data sheet. The only solution to this was to build a TRS generator (see Section 5.2.3) to overlay the TRS bytes onto the uncompressed video data. Again the phase of the FRP27 signal going into the decoder was chosen such that the BUS[3:0]-CLK18 relationships at the coder and decoder, on the same card this time, corresponded with each other. Now the back-to-back test finally worked. It turned out that the FRP27 phase could be varied over a couple of clock periods around the initial value while the system kept working. However, outside this range the uncompressed video data looked as unfamiliar as it had done in the two-card test.

Still it was necessary to return to the two-card setup, as this resembles the actual application in which the coder and decoder will be used. This time it worked, with the TRS



'ig. 12. TRS generator

ıerator in place. It turned out that there had been an uniced delay in one of the signals, so that the BUS[3:0]-P18 comparison at the coder and decoder side had not ːn accurate. As a result, the range of tested values had t fallen outside the acceptable range and this had caused incoherent uncompressed video data at the decoder out-.

Now the small acceptable range of FRP27 phases is ɔwn and the medium value is chosen as the preferred ː. It can be generated easily by decoding a certain value the DVCpro counters. For specific values of the sector, ck, group and nibble counters FRP27 is high, for all oth- it is low.

5.2.3. *TRS generator*

we have seen in Section 5.2.1, decoding the TRS seːnce is not difficult. Creating TRS sequences to be over-l onto the uncompressed video signal from the decoder uires more FPGA resources. Fig. 12 shows the block gram of the TRS generator.

The input signals are CLK27 and FRP27. The latter is d to synchronise the TRS sequence with the video ːam. FRP27 enters the circuit via an edge detector. The ulting signal is high during the first clock period of the v video frame. At this point, the sample counter and line ınter are reset to values that are specific to the Panasonic 'Cpro decoder (sample 552 in the first line). When there no rising FRP27 edge, the sample counter continually ps counting from 0 to 1727 as there are 1728 bytes with or C_R/C_B samples in a digital video line. After sample ?7 a new line starts, so a NEXT_LINE signal is sent to line counter to increase the line count. The line counter ıtinually counts from 0 to 624 as there are 625 lines in a L TV picture.

The sample and line counter values are decoded to create V and F signals according to the ITU-601 specification. ː TRS_FF, TRS_00 and TRS_FVH signals determine en the FF, 00 and XY TRS bytes are overlaid onto the oming video data. This is done in consecutive stages to ıimise the use of CLBs in the FPGA and to avoid timing ɔrs.

VI. Improvements

So far, all the work that has been carried out has been ɔlementing the BBC's original proposals. Most of them l been made in a hurry because of time pressure on the ject. This section contains three proposals to improve ıre versions of the DVCpro system. First a new packet ıcture is proposed that maximises the amount of error tection data that can be added. This is then used in an litional error protection scheme with time interleaving to ther improve transmission ruggedness. Lastly some error ıcealment strategies are discussed.

5.1. *Packet structure*

The packet structure can be improved in two completely ferent ways, depending on the goal that needs to be ieved. Initially, it was important to minimise memory ge in the original system (Section 6.1.1). In the proposed new system, memory is not the prime concern and it is more important to maximise the amount of error protection data that can accommodated in each packet (Section 6.1.2).

6.1.1. *Minimising FIFO length*

There is one packet FIFO in the coder and two in the decoder. In the coder, the FIFO stores DVCpro data until it is ready to be transmitted in packets. In the decoder, the FIFOs compensate for delays between the two incoming packet streams. They also allow for fluctuations in the incoming data that occur because padding is discarded at some points.

Ideally, the FIFO in the coder is 2 packets deep. While the first packet is read out and sent to be a DVB-T modulator to be transmitted, the second packet is being written with data arriving from the DVCpro coder. When the DVCpro interface design first started, it was assumed that both decoder FIFOs would be 2 packets deep as well. However, it turned out that all FIFOs needed to be 3 packets deep. This meant that in the decoder there was a memory requirement for 6 packets (6×188 = 1128 bytes), which consumes 36% of the FPGA resources. As a result, there would not be enough room for all other decoder logic.

This problem occurs because of the packet structure that had been chosen by the BBC. All packets were filled completely, except for the last packet in a sector. This last packet is only partially filled. This causes a significant fluctuation in the data rate, which needs to be compensated for by deeper FIFOs.

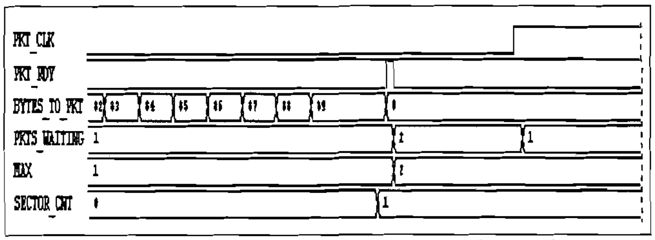


Fig. 13. Timing diagram of original packet structure at the end of a sector

A computer simulation was carried out to illustrate this situation. The timing diagram is shown in Fig. 13. The number of data bytes that is sent to a packet is counted in BYTES_TO_PKT. Once it has counted from 0 to 181, the packet is full. The number of packets waiting to be transmitted, PKTS_WAITING, is increased and the next data byte will be the first in a new packet. On a rising packet clock (PKT_CLK) edge, a packet is sent and PKTS_WAITING is decreased. The variable MAX contains the maximum number of PKTS_WAITING that has occurred. This means that the required FIFO depth is MAX+1, as data that is currently arriving from the coder must be written to a new packet that is not yet waiting for transmission. When a new DVCpro sector starts, the current packet is padded with zeroes regardless of the present BYTES_TO_PKT count and put into the queue. Fig. 13 shows that this is wasteful in this case. At this specific moment MAX could have been limited to 1 if sending the last (incomplete) packet had been postponed for a small number of clock periods, but this is not the general case because the

KT_CLK timing with respect to the start of a new sector aries over time.

A better packet strategy in this case would be to divide ıe number of bytes per sector more equally over all the ackets that are sent within a sector period ($^{1}/_{12}{}^{\text{th}}$ video ·ame). Dividing the data equally over all packets is generlly not possible when a small FIFO is used, as after disarding some of the DVCpro data according to Section 3.2 ıe incoming data rate is not constant. During "busy" perids within the sector, when little or no data nibbles are disarded, the available packet payload will not be sufficient to eep up with the data rate. As a result, MAX will increase uickly. So if MAX is to be minimised, a balance between qual-length and maximum-length packets needs to be ound.

The optimal number of bytes per packet depends on the educed DVCpro data rate that is chosen. Computer simulaons were carried out to find the optimal payload for each ossible reduced DVCpro data rate. In each case, the numer of bytes per sector divided by the number of packets per ector was chosen as the initial value. Then MAX was deermined after a 1-second simulation. The simulation was epeated with the number of bytes per packet increased by ne until a minimum value for MAX was found. The reults are summarised in Table I.

TABLE I: SIMULATION RESULTS FOR THE MINIMUM FIFO LENGTH PACKET STRATEGY

Reduced DVCpro data rate	Average bytes per packet	Optimal bytes per packet	MAX
32.256 Mbit/s	168	168	1
28.800 Mbit/s	150	170	1
27.072 Mbit/s	141	167	1
24.948 Mbit/s	130	167	1

From Table I we see that MAX can be limited to 1 in all ases, so that the required FIFO length is now only 2. All ackets are padded with zeroes. This packet structure is seful to adopt in the present DVCpro system where only imited memory is available.

6.1.2. *Equalising payload*

If memory availability is not a problem in the second-;eneration DVCpro system then the strategy in which the ıumber of bytes per sector is equally divided over all packts per sector is the best one. It will be shown in Section 6.2 hat the unused portion of a packet can be used to add errorırotecting bytes. The more of these bytes can be added, the nore powerful the error protection will be.

Therefore a new reduced DVCpro data rate option is ıroposed. We have seen in Section 3.2 that the video-only ıption data rate is 24.948 Mbit/s, while the audio portion of he DVCpro data amounts to 1.728 Mbit/s. A new reduced lata rate option in which only video and audio data are etained and all padding and control data is discarded will ıave a data rate of 26.676 Mbit/s.

It is clear that the control data will need to be regener.ted in the decoder. Since the original DVCpro interface ıroposals were adopted, more information about the)VCpro data interface details has been obtained [8]. First f all, the Control group at the start of each sector contains so-called header, subcode and VAUX information. However, according to the datasheet the codec ignores this data altogether. Hence this group can safely be replaced by a dummy block. The three ID bytes at the start of each block do need to be regenerated by the decoder, but this is not difficult. It contains the following information:

- **Section type:** header, subcode, VAUX, audio, video. The sequence of 168 blocks in every DVCpro sector is always the same, so it is easy to determine the type of each block using the DVCpro counters that are already available in the design.
- **DIF sequence number**. This is in fact the sector number that is readily available from the DVCpro counters.
- **DIF block number**. This numbers the blocks of a certain type. In our application, this number ranges from 0 to 8 (9 audio blocks) or 0 to 134 (135 video blocks).

The data rate for this option is 26.676 Mbit/s = 3,334,500 bytes/s. They are equally divided over all packets, so there will be 3334500/24064 = 139 bytes of DVCpro data per packet. The validity flag (1 bit), packet address (7 bits), sector address (5 bits) and multiplexing mode (3 bits) from the original packet structure are retained and they will occupy 2 further bytes. The three bytes that had originally been reserved for MPEG interoperability are not longer used, as it is unlikely that MPEG-specific equipment will be used with the DVCpro system. The first byte of a DVB-T packet is still reserved for the sync byte, so there will be 188–1–139–2 = 46 bytes per packet available for error protection.

Computer simulation has shown that MAX=6 for this number of bytes per packet, so the FIFOs will be 7 packets deep.

6.2. *Error protection*

Two ways to add error protection will be discussed: turbo coding and time interleaving. The latter will turn out to be the preferred option.

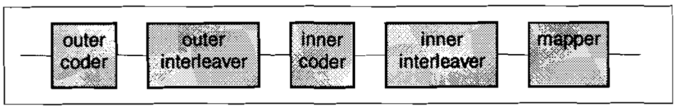


Fig. 14. FEC mechanism in DVB-T

6.2.1. *Existing error coding in DVB-T*

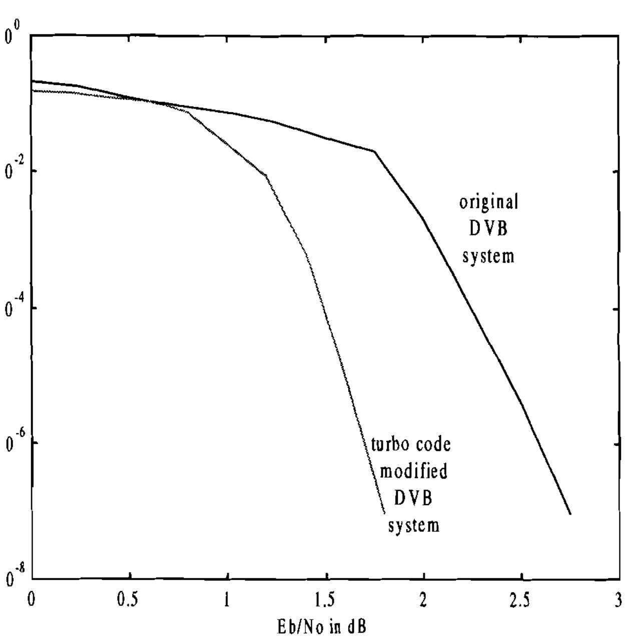
As a result of noise there will be errors when transmitting information over a radio channel. For digital video systems a reliable transmission system is necessary, so transmission errors should be avoided. There are two error control strategies to suppress transmission errors: automatic repeat request (ARQ) and forward error correction (FEC) [9]. ARQ requires a two-way system. When errors are detected at the receiver, it sends a request to repeat the message. This is not practical in real-time applications like digital video transmission systems. For this reason, those systems always use FEC. The FEC scheme used in DVB-T is based on concatenated Reed-Solomon (RS) and convolutional coding (CC), which has proven to be very efficient. The scheme is illustrated in Fig. 14 [3].

The data is organised in packets that are 188 bytes long (1 sync byte followed by 187 data bytes). Then RS

4,188,8) Reed-Solomon block coding is applied to the kets. The error-protected packet is 204 bytes long and tains 16 parity bytes. The RS-code is capable of correct- 8 random erroneous bytes. The inner coder is a 3,171) convolutional code. The outer byte-wise interver between the RS and CC matches the error correction perties of the both codes so that the performance of the catenated coding is optimal. The mother CC has rate ½, it can be punctured for the other code rates that DVB-T ws for. In the inner interleaver, the data is distributed r the 1512 active OFDM carriers by bit-wise followed by nbol-wise interleaving. This process is called frequency erleaving.

5.2.2. Turbo coding

Although RS-CC concatenated coding is very powerful, or coding performance could be improved even further using turbo coding instead of convolutional coding. bo codes are extremely energy efficient for error correc- n [10]. Several authors have proposed to replace convoonal codes by turbo codes in DVB [11], [12]. In Fig. 15 s shown that for a typical bit error rate (BER) of 10^{-6} to ^{7} the required power per bit is reduced by approximately lB. Conversely, by maintaining the existing power level BER decreases, and the system becomes more rugged.



. 15. BER v power per bit using convolutional inner code (original DVB em) and turbo inner code (modified DVB system). Both systems use a RS 1,188,8) outer code, a rate ½ inner code and a depth 12 convolutional rleaver between inner and outer code [11]

However, this 1 dB coding gain comes at the cost of a destly increased decoder complexity. But a more severe blem is that the replacement of the convolutional coder not possible within the DVB-T standard. An important vantage of the current digital radio camera, which is that an work with any DVB-T receiver, does not longer exist that case. So at present, using turbo coding is not a vie option, although it should be considered for future ra- camera generations if it is decided to use an alternative nsmission standard optimised for this particular applican.

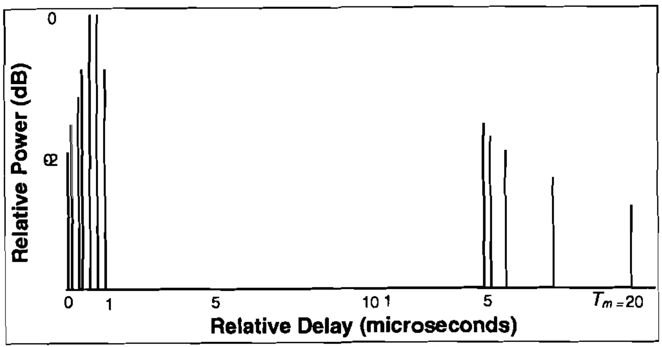


Fig. 16. Delay profile for a typical hilly terrain environment

6.2.3. Time interleaving

It would be preferable to find a way to make transmission more rugged in such a way that the DVB-T layer of the communication channel is preserved. This ruggedness is required especially in fading channel conditions.

As a result of reflections, there will generally be multipath reception. The several paths from transmitter to receiver are associated with different delays, leading to dispersion of the signal in time. Those different delays are displayed in a delay profile, as shown in Fig. 16.

From the delay profile, the multipath spread of the channel, T_m, can be determined. From T_m we can calculate the coherence bandwidth [13]:

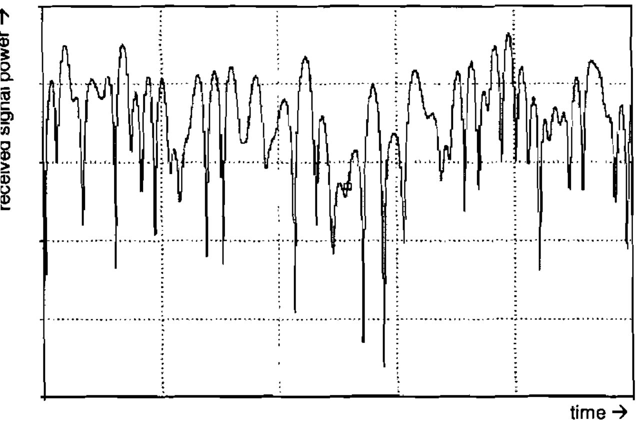
$$(\Delta f)_c \approx \frac{1}{T_m} \quad (1)$$

If the coherence bandwidth is small compared to the bandwidth of the transmitted signal, *frequency-selective fading* occurs. There will be notches in the spectrum of the received signal. As a result, not all COFDM carriers can be received because they are attenuated too much. The DVB-T standard offers protection against this, as it employs *frequency interleaving*. Even if a large proportion of the carriers cannot be received properly, the original data can still be reconstructed from the remaining carriers.

This is no longer possible in the event of *flat fading*, also called frequency-nonselective fading, when all carriers are severely attenuated. This occurs when the coherence bandwidth is large in comparison with the signal bandwidth, so when T_m is small. This happens when a number of signal paths arrive at the receive antenna at the same time or with only short delay. Their sum may add up constructively or destructively, sometimes leading to total cancellation or fading. Fig. 17 depicts the received signal power after transmission over a flat fading channel.

The depth, number and duration of the dips in Fig. 17 are a function of the maximum Doppler frequency, which in turn depends on the carrier frequency and the speed of the mobile transmitter. The distance between two local amplitude maximums in Fig. 17 is approximately equal to the coherence time of the channel [14], which can be calculated from the maximum Doppler frequency:

$$(\Delta t)_c \approx \frac{1}{2f_{dop,\max}} \quad (2)$$



'ig. 17. Power envelope of a typical flat fade signal

For high transmitter speeds, the maximum Doppler fre-uency will be high, so the distance between maximums nd hence the length of deep fades will be short. In this ase, flat fading can be overcome with *time interleaving* 15]. Just as frequency interleaving allows erroneous data to ›e corrected from information obtained from carriers with ifferent frequencies, time interleaving allows recovering ata from information transmitted before or after the flat ading event.

The DVB-T standard does not offer time interleaving, as : was primarily designed for stationary receivers. However, adio cameras are used for the very reason that they offer ıobility. So we are going to extend the DVB-T system with n additional layer that provides time interleaving.

As we have seen in Section 6.1, in the newly proposed ›acket structure, only 141 data bytes are sent per packet. 'he first byte is still reserved for the sync symbol and the ›acket consists of 188 bytes. This leaves us with 46 unused ›ytes that can be used for error protection. As the 141-byte)VCpro packets arrive, they are first RS (187,141,23) oded. In this way, 46 parity bytes are added to the DVCpro ›ytes.

1	2	...	22	23	24	... packet 1 ...	186	187
1	2	...	22	23	24	... packet 2 ...	186	187
1	2	...	22	23	24	... packet 3 ...	186	187
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	2	...	22	23	24	... packet *N*-2 ...	186	187
1	2	...	22	23	24	... packet *N*-1 ...	186	187
1	2	...	22	23	24	... packet *N* ...	186	187

'ig. 18. Modified packet order for time interleaving. The first bytes of all ackets are transmitted, followed by the second bytes of all packets, etc. Cor-ıpted bytes are shaded.

The error-protected DVCpro packets are not transmitted mmediately, but *N* 187-byte packets are stored in rows of a nemory. The memory is then read out in columns, as illus-rated in Fig. 18. The 188-byte DVB-T packet is formed by he sync byte followed by 187 bytes from the memory col-ımn. In the event of a deep fade, a number of packets will ıot be received correctly. Assume that the 23*N* bytes shown n grey are corrupted, which corresponds with 23*N*/187)VB-T packets. The time it takes to transmit this portion of he data is

$$\frac{23N}{187}T_{packet} \quad (3)$$

with

$$T_{packet} = \frac{1}{f_{packet}} = \frac{1}{12032} = 83.11\ \mu\text{s} \quad (4)$$

In the time de-interleaver in the receiver, the data is written into memory columns and read out in rows, so that we have 187-byte error-coded DVCpro packets again. Each of these received DVCpro packets contains 23 corrupted bytes. However, up to 23 bytes can be corrected by the RS-code so the original packet can be reconstructed. So as long as the duration of the correctable portion in Formula 3 exceeds the maximum error burst time T_{burst} caused by the deep fade, the video data can be received correctly:

$$\frac{23N}{187}\cdot T_{packet} > T_{burst} \quad (5)$$

So the interleaving depth N needs to be:

$$N = \left\lceil \frac{T_{burst}}{T_{packet}}\frac{187}{23} \right\rceil \quad (6)$$

Now we need to know T_{burst}, the length of the bursts we want to overcome with time interleaving. The fading channel can be simulated using a band limited white Gaussian noise model, which has a Rayleigh probability distribution [16]. A computer simulation has been carried out. A deep fade was assumed to occur every time the envelope of the channel transfer function was more than 20 dB below the average value. The result is a probability density function for the length of deep fades. From this we can derive the cumulative density function, shown in Fig. 19. This allows us to choose the desired degree of reliability and derive the corresponding maximum burst length.

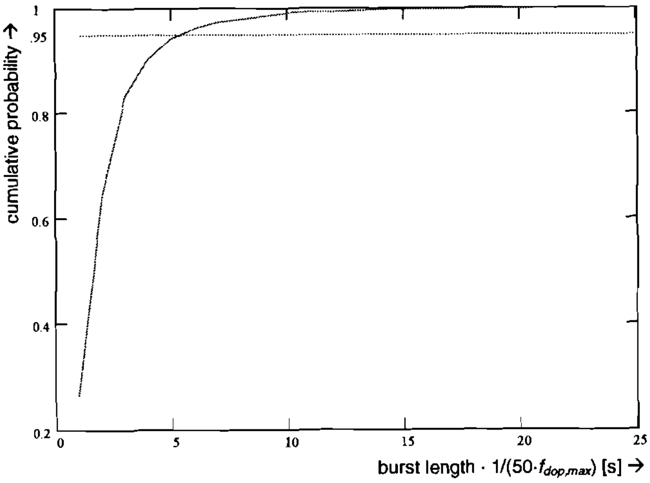
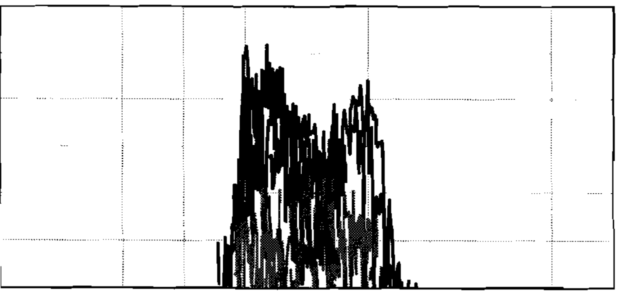


Fig. 19. Cumulative probability function of the length of deep fades

The timescale depends on the maximum Doppler frequency, as pointed out before. The BBC has carried out Doppler spectrum measurements with its microwave channel sounder. Fig. 20 shows a typical Doppler spectrum. It was measured in a corner of a large room in Kingswood Warren while moving around the channel sounder in a circle. This is a typical movement a cameraman could make in a studio.



20. Doppler spectrum for typical indoor radio camera usage

The maximum Doppler frequency $f_{dop,max}$ is 15 Hz in this e. Applying this to Fig. 19 and choosing 95% reliability, see that the maximum burst length equals 5.66 / (50·15) 7.55 ms. So only 5% of deep fades will be longer than 5 ms. We choose

T_{burst} = 7.55 ms

nd hence, according to (6),

$$N=\left\lceil \frac{7.55\cdot 10^{-3}}{82.11\cdot 10^{-6}}\cdot\frac{187}{23}\right\rceil = 748 \text{ packets.}$$

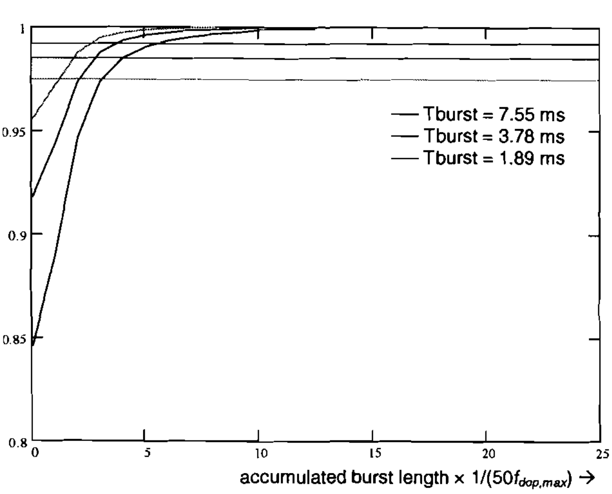
So far it has been assumed tacitly that after the 23N corited bytes in the N-packet block from Fig. 18 there are no ther corrupted packets in the time span corresponding h this block:

T_{block} = 748T_{packet} = 61.4 ms

However, if there are any more error bursts, then data nnot be restored anymore, because the error-rectingcapabilities of the RS code have already fully n used.

To check the time interleaving performance, another nulation was carried out. This time the test data was died into 22,500 intervals of 61.4 ms. For each interval, sum of all deep fades within it was expressed in time. e RS (187,141,23) code can correct up to

23/187×T_{packet} = 7.55 ms of accumulated burst errors.



21. Cumulative density function of the length of accumulated errors per rval

Fig. 21 shows the cumulative density function of the total st length per interval. In 99% of the intervals, the error recting capabilities of the RS code turns out to be suffint for the burst errors caused by the deep fades in the nnel. Note that this assumption is only valid if the disution of burst errors within the N-packet block is such that the number of corrupted bytes per row does not exceed 23.

It is clear that time interleaving can be used to make the digital radio camera system much more rugged. It matches the mobile radio camera application to the DVB-T standard that was primarily intended for static use.

However, there are serious disadvantages as well. First of all, time interleaving introduces a significant additional coding delay. In Fig. 22 an overview of the required hardware is given. For each DVB-T channel, N rows of data are written into a time interleaving block first. As soon as this block is complete, it can be read out in columns. The inverse process takes place in the receiver. Note that the block that is read out column-wise in the transmitter and the block that is filled column-wise in the receiver are separate memory blocks, but the reading and writing takes place simultaneously. Hence, the overall delay introduced by time interleaving is

$T_{delay} = 3T_{block}$ = 185 ms ≈ 4.6 frames

This is a dramatic increase compared with the 2-frame delay in the DVCpro codec and clashes with one of the main system requirements set out in Section 2.2.

Therefore the delay increase should be limited. There is a trade-off between interleaving depth and the amount of burst errors that can be corrected. To keep the delay down, more errors will need to be accepted. Initially, Fig. 19 was used to choose the time interleaving depth. Then Fig. 21 was used to check whether the choice was reasonable. The first one gives an indication as to how long the error burst is *when one occurs*, while the second one takes into account that most of the time there is no burst at all. The second method is more suitable to make the trade-off when the average reliability is most important rather than the worst case.

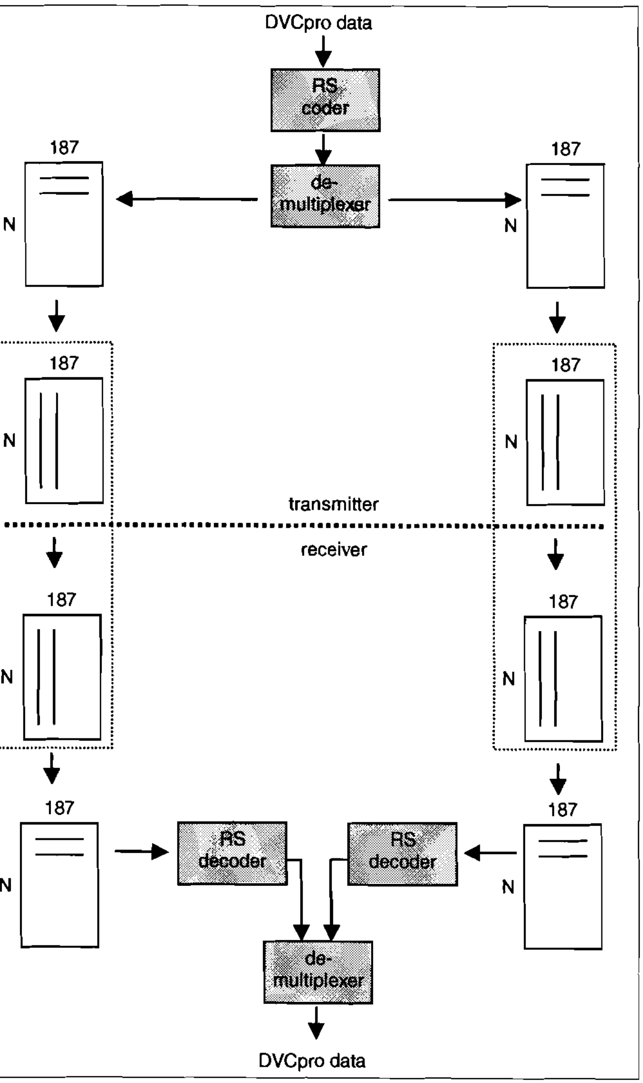
Previously, we had 99% reliability. If we accept 98.5%, the required interleaving depth is halved to 2.3 frames. It can be halved once more to 1.2 frames. In this case, the reliability drops slightly to 98%. This means that a small sacrifice as far as reliability is concerned leads to a large reduction of the required time interleaving depth.

The preferred option is to use a time interleaver with variable depth, with N=748 (as before) chosen as the upper limit. The degree of ruggedness of the system can then be traded off against delay according to the specific application it is used for.

The second problem of time interleaving is the necessary larger hardware size. The major components are memory and the RS encoder and decoder. This is illustrated in Fig. 22. In the transmitter as well as the receiver, four memory blocks of 187N bytes are needed with N=748. Hence the total memory requirement is approximately 600,000 bytes. This is considerably more than the hundreds of bytes needed in the first version of the DVCpro interface and it cannot longer be implemented in the FPGA, so external memory will be necessary.

The RS encoder and decoder can be implemented in a Xilinx FPGA. They are even readily available as “logic cores” from Xilinx and other providers [17], [18]. The amount of FPGA logic that is needed is proportional to (n-

) in the RS (n,k,t) code. As we use RS (187,141,23), $(n\text{-}k)$ s relatively large so many resources are needed. The RS ecoder is more complex than the encoder. As a result, high values cause long processing delays in the decoder. For ur particular RS code this means that the decoder requires pause between RS blocks, which is not acceptable for the)VCpro decoder. This could be overcome by increasing the umber of clock periods per symbol, but this would lead to n extremely high clock frequency as the symbol rate is lready high. The only alternative is to use two RS decoders n parallel, one after each time de-interleaver. As a conseuence, it is likely that at least one large additional FPGA s required for the receiver.



'ig. 22. Time interleaving hardware overview

6.3. *Error detection*

Even though much effort has been put into avoiding unecoverable errors in the receiver, they still can occur under ertain circumstances. In that case they need to be detected o that we can attempt to conceal them, as we will see in ection 6.4.

6.3.1. *CRC codes*

CRC codes are Cyclic Redundancy Check codes. They do ot have error correcting capability and are therefore norally used in ARQ systems [19]. They are an application of shortened cyclic codes. In the transmitter, the syndrome is calculated as usual using a generator polynomial $g(x)$ and added to the message that is to be checked. In the receiver, the syndrome of the message concatenated with the transmitter syndrome is calculated. If the receiver syndrome is zero, no error has been detected.

There are several CRC standards that differ in terms of the generator polynomial that is used and the initial state of the register that is used for syndrome calculation. The BBC had chosen to use the CCITT polynomial, with $g(x) = 1 + x^5 + x^{12} + x^{16}$ and zero as the initial register state. Using this polynomial, the probability that a message with a burst of errors is incorrectly interpreted as being correct is 1/65536.

CRC error detection has already been implemented in the present DVCpro system, where it is only used to drive an indicator. This is useful for troubleshooting the system. In this case, the message consists of the data in all 74 DVCpro packets in one sector. The CRC code consists of two bytes, which are appended to the data in the last packet of the sector. This is possible because this packet is not fully used.

6.3.2. *RS decoding failure signal*

In the proposed system with time interleaving, CRC error detection could still be used. However, the RS error protection that is used by the time interleaving mechanism can also be used for error detection. It is easy to equip the RS decoders with outputs that indicate whether the decoding process has been successful. If there are more than 23 erroneous bytes in the packet, they cannot longer be corrected and this will be flagged on the outputs.

This error detection method is more sophisticated than CRC error detection, because it applies to much smaller data sequences: 141 RS-coded bytes (almost 2 macro blocks) versus many thousands of bytes in the CRC code applied to complete sectors (135 macro blocks). It is clear the more localised the error detection is, the better it can be used for error concealment.

6.4. *Error concealment*

Although many efforts have been made now to prevent uncorrectable errors from happening, there will still be occasions when errors will occur. In those cases it is important to try to limit the damage to the picture by concealing the errors as much as possible.

6.4.1. *Fail to black*

If the present DVCpro system fails, all or part of the picture turns bright green or magenta. This makes the error very obvious. It would be better if the picture, or preferably a small number of macro blocks, turn black instead.

Errors can be detected per packet, which contains the contents of almost 2 compressed macro blocks. It is practical to apply error concealment on a macro block-by-macro block basis. If the current DVB-T packet turns out to be uncorrectable, it is likely that the current compressed macro block has already started in the previous error-free packet. This would mean that it is too late to start replacing this macro block by a black one. Therefore the incoming

Cpro data stream should be delayed by one block. Then two macro block errors that will occur in the next ket can be substituted instantly by black ones. This reres 77 bytes of memory.

5.4.2. Copy adjacent macro blocks

\ more advanced way to conceal errors is to copy the tents of an adjacent macro block to the current one ıer than make it black. In order to understand how this be done, some knowledge about the way the macro :ks are organised is required.

3roups of 27 macro blocks form so-called super blocks. :y correspond with the DVCpro groups in Fig. 3. The y the super blocks and macro blocks are organised is wn in Figs. 23 and 24. From Fig. 24 it follows that in st cases the previous macro block is adjacent either verılly or horizontally. Exceptions are macro blocks 0 in er blocks $S_{i,0}$, $S_{i,2}$ and $S_{i,4}$. When those macro blocks are rupted, the next one should be copied. To achieve this, a ı-block delay is needed which costs 154 bytes.

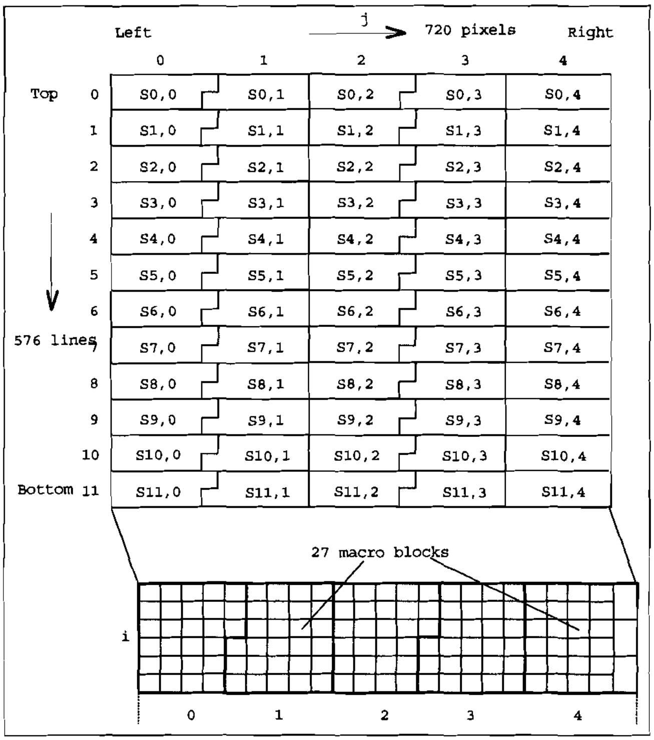
Note that this can only be done if the next macro block is corrupted. Otherwise, more complicated arrangements :d to be made that will cost more memory and delay.

5.4.3. Copy same macro block from previous frame

The optimal error concealment method is to replace corted macro blocks in the current frame by the correspondmacro blocks from the previous frame. The downside is t a significant amount of memory is required. There are 5 video blocks per sector and 12 sectors per frame. So : frame of compressed video can be stored in 135×12×77 24,740 bytes of memory. Like in Section 6.4.1, the sec1 part of the current macro block is stored in the next 'B-T packet, which may be corrupted. To be able to look :ad, an additional delay of one block is needed. This ngs the total memory requirement for this error conlment method to 124,817 bytes.

Note that it is not possible to re-use the memory that has :ady been allocated for time interleaving. The four 187*N* mory blocks contain RS-encoded packets, so an addiıal RS decoding step would be necessary to retrieve cro blocks.

However, there is less concern about the size of the rever than the transmitter because the receiver is at a fixed ation.



	0	1	2	3	4
0	S0,0	S0,1	S0,2	S0,3	S0,4
1	S1,0	S1,1	S1,2	S1,3	S1,4
2	S2,0	S2,1	S2,2	S2,3	S2,4
3	S3,0	S3,1	S3,2	S3,3	S3,4
4	S4,0	S4,1	S4,2	S4,3	S4,4
5	S5,0	S5,1	S5,2	S5,3	S5,4
6	S6,0	S6,1	S6,2	S6,3	S6,4
7	S7,0	S7,1	S7,2	S7,3	S7,4
8	S8,0	S8,1	S8,2	S8,3	S8,4
9	S9,0	S9,1	S9,2	S9,3	S9,4
10	S10,0	S10,1	S10,2	S10,3	S10,4
11	S11,0	S11,1	S11,2	S11,3	S11,4

Fig. 23. Super blocks and macro blocks in one frame [8]

Super block S i, 0, S i, 2 (i = 0, ..., 11)

0	11	12	23	24
1	10	13	22	25
2	9	14	21	26
3	8	15	20	
4	7	16	19	
5	6	17	18	

Super block S i, 1, S i, 3 (i = 0, ..., 11)

	8	9	20	21
	7	10	19	22
	6	11	18	23
0	5	12	17	24
1	4	13	16	25
2	3	14	15	26

Super block S i, 4 (i = 0, ..., 11)

0	11	12	23	24
1	10	13	22	
2	9	14	21	25
3	8	15	20	
4	7	16	19	26
5	6	17	18	

Fig. 24. Macro block order in a super block [8]

VII. Conclusions

DVCpro is a usable alternative for the MPEG-2 video compression scheme for use in a digital radio camera. A disadvantage is the fact that two DVB-T channels are needed for transmission, but DVCpro's low coding delay is a significant advantage.

It has been shown how the requirements for the DVCpro codec interface have been translated into hardware and logic design.

Some aspects that must be taken into account in a hardware design that processes high-speed signals have been discussed.

During the logic design stage of the project, there were severe difficulties with interfacing to the Panasonic DVCpro codec. This was mainly due to inaccuracies in its documentation. The way to solving the problems was paved once it was known that the codec did not comply with the ITU-601 standard as expected.

A proposed new packet structure allows for a maximum amount of error protection data to be added to the transmitted data.

This makes it possible to extend the DVB-T transmission channel with time interleaving, which is a powerful error protection mechanism in digital radio camera environments. This improved ruggedness is achieved while standard DVB-T receivers and modulators can still be used.

Despite all efforts that have been made to make transmission more reliable, it is never possible to guarantee that it is error-free. Therefore three strategies to conceal the effects of transmission errors on the video picture have been discussed. The best option is to replace corrupted macro blocks by the same macro blocks from the previous frame. Howecer, this is the most expensive option in terms of memory that is required.

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IX. Acknowledgements

I would like to thank the Eindhoven University of Technology and the BBC for making it possible for me to carry out my graduation project at BBC R&D. Thanks to John Zubrzycki and prof. Van Roermund for supervising my project, and to Thomas Davies, Peter Moss, Jonathan Rosser and Mark Waddell at the BBC for their help.

Appendix A: Video compression schemes

Γhere are three main video coding families to choose n:

IPEG

›V

'avelet-based coding

Γhe latter is relatively new. It is still being developed inly in software and there are problems with handling erlaced, full-resolution, real-time SDTV video. Hence a dware realisation of wavelet coding would be impossible the short term. Below MPEG and DV are investigated ther.

. Intra-frame compression

Γhe two remaining compression families are both based DCT (Discrete Cosine Transform). With DCT the video nal is transformed from the spatial domain to the freency domain. This is done in block of 8 by 8 pixels (8-8 'T). Then the DCT coefficients are weighted according heir significance to the human visual system. This is the called quantisation step, which is the lossy step in the npression process. Here the compressed data rate is demined. Fine quantisation leads to good quality pictures l a high bit rate, coarse quantisation to lower quality and ower bit rate. In the spatial domain, all pixel intensity els are equiprobable. This is not longer the case in the tial domain after quantisation. As a result, compression ı take place. This last step is variable-length coding .C) in which more probable levels are given shorter les than less probable ones.

. Inter-frame compression

Γhe process described above is called intra-frame (I me) compression as it takes place in the two-dimensional tial domain of one frame. To compress the video signal n further, it is possible to exploit redundancies in the nporal domain, between successive frames. This leads to ee types of frames in MPEG:

frames, as described above

' frames: pictures coded differentially with reference to a revious or subsequent I or P frame

3 frames: pictures coded differentially with reference to oth previous and subsequent I or P frames.

Typically consecutive frames do not differ very much, so t B and P frames will become very small. Hence a large a rate reduction can be obtained.

MPEG uses a Group Of Pictures (GOP) that is a particu- sequence of I, P and B frames. A GOP is typically 12 mes long. Using GOPs introduces a larger coding delay, ich contradicts the low delay requirement mentioned in ction 1.2. So there is a trade-off between the reduction in a rate that can be achieved for a certain picture quality l the coding delay.

A.3. Data rate control

There are three mechanisms to control the data rate of the compressed video output.

- **Constant quantisation table**. If quantisation is carried out using weighting factors, the data rate will vary according to the picture content but picture quality will be constant.
- **Feedback buffer control**. If the data rate is getting too high, a coarser quantisation table is used for subsequent blocks. If there is a buffer underflow, a finer quantisation table is used. Still the data rate is not exactly constant, bit stuffing is needed to achieve a constant byte count per frame. The picture quality is variable.
- **Feed-forward quantisation control.** Several quantisation operations are carried out on each block simultaneously. The quantisation table that yields the bit rate closest to but not greater than the desired rate is used for that particular block. In this way the picture quality is maximised while maintaining an almost constant data rate. However, this technique is computationally expensive and the picture quality is still variable.

A.4. MPEG

MPEG (Motion Picture Expert Group) is a family of compression schemes. There are numerous Profiles and Layers, offering different trade-offs between picture quality and data rate. MPEG-1 picture size is limited to 354x240 pixel picture sizes. M-JPEG (Joint Pictures Expert Group still image standard applied to moving pictures) uses I frame coding only and has a variable data rate in order to keep picture quality constant. Most MPEG-2 schemes use GOPs to achieve higher compression ratios due to temporal compression. Feedback buffer control is used to limit data rate variation. Feed-forward quantisation control would be more optimal, but it is impractical because every possible quantisation table would need to be applied to every frame in the GOP. This requires too many computations. MPEG-4 is aimed at low bit rate object-based video coding and interactivity, which is not as suitable for the radio camera as MPEG-2.

A.5. DV

DV (Digital Video) compression offers some additional features [20].

- **Interlaced images**. Most compression schemes use frame-based processing. The video pictures are deinterlaced before compression. If there is no or little motion between the two fields of one frame, frame-based compression performs well. However, if there is significant motion, there will be little correlation between the pixels on alternate lines. This reduces the redundancy, hence limiting the effectiveness of the compression. In this case, field-based processing would perform better.

V combines the advantages of both techniques. Dependng on the difference between the two fields in a frame, DV nooses for frame processing (8-8 DCT) or field processing 2-4-8 DCT, 2 halve blocks each containing 4 by 8 pixels om one field). This is done on a block-by-block basis, so nat optimal decisions are made for each small area in the icture.

- **DCT block shuffling**. Four adjacent luminance DCT blocks and two luminance DCT blocks with the corresponding colour information are grouped into a macro block. Shuffling means that five macro blocks from different locations in the picture are combined into one so-called video segment. Quantisation is applied per video segment. The advantage of doing this is that video segments always contain an average amount of redundancy, so that the effects of compression are equally distributed within an image.
- **DCT blocks pre-analysis**. There are 64 possible quantisation tables in DV. These are organised in four groups of 16 tables, each optimised for a certain level of spatial detail. The measured power of the AC coefficients within the DCT blocks is used to choose one of the four groups. The pre-analysis is executed per video segment. Then each of the 16 remaining quantisation tables is applied to the DCT blocks. A selection is made in such a way that the final byte count is closest to, but not exceeding, the desired byte count that is linked to the desired data rate.

The main difference between DV and MPEG-2 is that the data rate in DV cannot be freely configured as in MPEG-2. For standard definition TV (SDTV), there are only two data rates. DVCpro25 is a professional tape format that uses DV at 25 Mbit/s, DVCpro50 is 50 Mbit/s.

Appendix B: Useful bitrate (Mbit/s) for all non-hierarchical DVB-T modes

Modulation	Code rate	Guard interval			
		1/4	1/8	1/16	1/32
QPSK	1/2	4,98	5,53	5,85	6,03
	2/3	6,64	7,37	7,81	8,04
	3/4	7,46	8,29	8,78	9,05
	5/6	8,29	9,22	9,76	10,05
	7/8	8,71	9,68	10,25	10,56
16-QAM	1/2	9,95	11,06	11,71	12,06
	2/3	13,27	14,75	15,61	16,09
	3/4	14,93	16,59	17,56	18,10
	5/6	16,59	18,43	19,52	20,11
	7/8	17,42	19,35	20,49	21,11
64-QAM	1/2	14,93	16,59	17,56	18,10
	2/3	19,91	22,12	23,42	24,13
	3/4	22,39	24,88	26,35	27,14
	5/6	24,88	27,65	29,27	30,16
	7/8	26,13	29,03	30,74	31,67