A controlled ballast based on 80C166 for 32 Watt DC HID lamp

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THESIS

A Controlled Ballast based on 80C166 for 32 Watt DC HID lamp

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SUMMARY

The control circuit of electronic power supplies for a High Intensity Discharge (HID) lamp is relatively complicated. The development of a ballast for a new lamp is usually a trial and error activity. Following this development method, an optimum design is never possible. The current development in microelectronics opens the possibility to digitize a big part of the HID lamp ballast control circuit. Digitalization based on a microcontroller is expensive (short instalment). Also the microcontroller application gives some advantages, such as better performance and faster development method, more flexibility for complex algorithm implementation, and expansion possibility for the user-interface (communication).

In this thesis a controlled ballast based on 80C166 is presented for a 32Watt DC HID lamp. This ballast is divided into 4 blocks: preconditioner (preliminary a 400Volt power supply), high efficiency (95%) 200kHz/32Watt Buck converter based on ZVS-QSC (Zero-Voltage-Switch Quasi-Square wave-Converter), ignitor (fly-back converter, 1.6kV DC), and control circuit (Current Mode Controller and 80C166). With the Current Mode Controller (CMC), the Buck converter can operate in open circuit, short circuit, and normal state. The control algorithm is implemented in the 80C166 microcontroller. This control algorithm consists of three states: initialization, ignition, and power regulation.

The controlled ballast based on 80C166 is able to feed the 32 Watt DC HID lamp correctly. The power regulation is based on the small signal p-i characteristic of the lamp, which is derived from a system identification. By a good approximation the power variation only depends on the current variation. The lamp power is directly controlled according to the multiplication $P_{la}=V_{la}*I_{la}$ (where in the conventional controller $S=V_{la}+\beta I_{la}$ is used). The optimum integrator time constant of the power controller is 0.3 s. The feedback power control system has a settling time of 0.1 s to 5% tolerance.

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1. INTRODUCTION

The present and future generation control circuits of electronic power supplies for the High Intensity Discharge (HID) lamp are relatively complicated. The interface between the mains and the lamp demands an accurate specification: the mains current distortion must be minimized to reduce the mains-pollution (maximizing the power factor), the ripple current of the lamp must be small (typically 5%) to obviate the acoustic resonance effect, an high efficiency ballast is required to save the energy consumption, and economically the product must be cheap and have a small size. In the future a user-interface could be added (remote control, dimming, etc).

Currently, the control circuit of a ballast is based on analogue circuits such as opamps, integrators, timers, comparators, etc. There are many tasks, sometimes quite complex, and mostly lamp-type dependent. Thus it is visible that in practice the number of analogue components for the ballast application rises up to a very high number. The development of a ballast for a new lamp is usually a trial and error activity. This gives an extra complication in the design process because the specification can be made only after all development has finished. Following this development method, an optimum design is never possible.

The current development in microelectronics makes it possible to digitize a big part of the HID-lamp ballast analogue circuit. A single chip microcontroller, such as SAB 80C166, promises a dramatic reduction of analogue components. A ballast circuit with switch frequency of 20kHz can be directly controlled by the SAB 80C166. In this case the control mode is a Pulse Width Modulation (PWM) with 7-bit resolution (accuracy of 0.8%). To control a ballast with a very high switching frequency, for instance 200kHz, extra hardware must be added. The PWM mode must be replaced by a Current Mode Control (CMC).

Digitalization opens a new method of development with some advantages:

- Low-cost software modifications will replace high-cost hardware modifications,
- Interactive system development by using an interactive high level language software, such as FORTH, will replace time wasting analogue modifications,
- Possibility for implementation of control algorithms such as I-, PI-, PID- controller, or a more complex controller such us adaptive - or self tuning controller,
- Expansion for the user-interface (communication) in the same microcontroller.

The purpose of this research is designing a DC HID-lamp ballast and creating a universal HID-lamp ballast control circuit based on SAB 80C166. The type of the control circuit is a power controller. This ballast will be applied as experimental power-supply.

The ballast consists of:

a. Preconditioner,
b. Down converter,
c. Ignitor, and
d. Control circuit.

A DC HID lamp compared to an AC HID lamp has a dramatic component reduction on its ballast. A commutator is not needed to supply a DC HID lamp. This saves space and cost of a DC HID lamp ballast. The small signal impedance of a 32Watt DC HID lamp (HALARC Metal Halide) is not very dominant in comparation with the property of a 32Watt AC HID lamp (Phillips White Son). Power regulation of a DC HID lamp will be easier and faster than a AC HID lamp. This is the second advantage of DC HID lamp.

The plan of this research is as follows:

a. Realization of an interactive development board based on 80C166,
b. System identification of a DC HID-lamp,
c. Derivation of a new strategy of the power control algorithm.
d. Design of a high efficiency, 200kHz/32Watt Forward Converter,
e. Design of a Current Mode Control for the Forward Converter (ForCe), which could control the ForCe in open circuit -, short circuit - , and normal state,
f. Building of a prototype Ignitor, a Fly-back Converter,
g. Implementation of the power controller in 80C166 and completing the ballast system as an experimental power supply.

Design of an electronic ballast for a lamp is always based on lamp properties. The power circuit of the electronic ballast depends on the large signal properties of the lamp, such as nominal lamp voltage, nominal lamp current, ignition voltage, etc. Some information about small signal properties of the lamp is needed, to control the lamp power at its nominal level. The regulation algorithm of the control circuit is based on these small signal characteristics, such as small signal impedance characteristic (v-i characteristic), small signal p-i characteristic, etc.

Chapter 2 describes a system identification of a 32 Watt DC HID-lamp. A pascal program is developed to determinate an electrical model of the DC HID-lamp. This model is useful to derive a small signal p-i characteristic. The power controller type is based on this p-i characteristic.

Chapter 3 illustrates the complete schematic of a HID-lamp ballast and gives its specifications. Further this chapter describes: a design of a 200kHz/32Watt ForCe inclusive the CMC, completing a closed-loop system of the ForCe. The principle of a prototype ignitor (a fly-back Converter) is also shown.

In chapter 4 the capabilities of the SAB 80C166 are investigated. A FORTH SYSTEM is implemented in EPROMs. Together with 80C166, this FORTH SYSTEM creates an interactive program development system. This chapter also describes possible tasks inventory which could be handled by a microcontroller for controlling a HID-lamp ballast.

Chapter 5 gives a realization of an experimental power supply based on 80C166, and discusses the result of the power measurement.

Chapter 6 discusses conclusions and recommendations of the research.

2. SMALL SIGNAL CHARACTERISTIC OF DC H.I.D. LAMP

The controller type of the ballast is a power controller. The power controller will keep the lamp power constant. To design an optimum power controller, a small signal characteristic of the controlled lamp is needed. Therefore a system identification of a 32 Watt DC HID lamp must be done.

The system identification is based on a model. Parameters of this model are determined from measurement data.

2.1. THE NATURE OF DC H.I.D LAMP

It is well known that a HID lamp has a non minimum phase (NMP) characteristic in its small signal v-i characteristic. In this case, NMP means: A positive step excitation in the lamp current, will give an undershoot in the lamp voltage response. This undershoot increases the settling time. If this characteristic is very dominant, it will give difficulty if one tries to design a fast feedback system for this lamp.

In term of control system engineering, a system is called NMP if that system has, at least, one zero in the right half s-plane (RHP).

2.1.1. N.M.P. System: A Simple Model 1 RHP Zero and 2 Poles

A system identification of an AC HID lamp (White Son, 32 Watt) has been done[1]. A relative simple model is applied to characterize the behavior of a AC lamp. The small signal impedance model of an AC HID lamp is given by the next relation:

$$Z_l(s) = \frac{v(s)}{i(s)} = K \frac{(s-\omega_z)}{(s+\omega_{p1})(s+\omega_{p2})} . \qquad (2.1)$$

The impedance $Z_l(s)$ has one RHP zero (ω_z) and two poles (ω_{p1} and ω_{p2}). $K<0$ is a constant with dimension [Ohm.rad/s]. We can rewrite that relation in partial fractions as:

$$Z_l(s) = Z_{l1}(s) + Z_{l2}(s) = Z_{l1} \frac{\omega_{p1}}{(s+\omega_{p1})} + Z_{l2} \frac{\omega_{p2}}{(s+\omega_{p2})} . \qquad (2.2)$$

Where

$$K = Z_{l1}\omega_{p1} + Z_{l2}\omega_{p2} < 0 \quad and \quad \omega_z = -\frac{(Z_{l1}+Z_{l2})\omega_{p1}\omega_{p2}}{(Z_{l1}\omega_{p1}+Z_{l2}\omega_{p2})} > 0 . \qquad (2.3)$$

Now the impedance characteristic becomes much easier to understand. The impedance is the sum of two first-order systems, $Z_{l1}(s)$ and $Z_{l2}(s)$. It holds that $Z_{l1}>0$, $Z_{l2}<0$, and $Z_{l1}+Z_{l2}>0$. Assume $\omega_{p1}<\omega_{p2}$. It is clear that $Z_{l2}(s)$ has a faster response than $Z_{l1}(s)$.

If we apply a current step excitation $\Delta i>0$ to this impedance, $Z_{1i}(s)$ (i=1,2) will give an exponential voltage response. $Z_{11}(s)$ causes a positive exponential response ($Z_{11}>0$) and $Z_{12}(s)$ causes a negative exponential response ($Z_{12}<0$). At first the response of $Z_{12}(s)$ is dominant, and it is negative. At that time, the sum of these responses will give an undershoot (a NMP characteristic). At the end of the response ($t\rightarrow\infty$ or $s\rightarrow 0$) the small voltage deviation will become $(Z_{11}+Z_{12})\Delta i>0$.

This model is also valid for a DC HID lamp. We will use this model to characterize the small signal impedance of the 32 Watt DC HID lamp.

2.1.2. System Identification

To identify the lamp characteristic, we need a current source. First the lamp must be ignited, and then the current source will bring the lamp into its nominal operating state, where the lamp voltage $V_{la}=V_0$, the lamp current $I_{la}=I_0$, the lamp power $P_{la}=P_0$ and the lamp impedance $Z_0=V_0/I_0$. The characteristic measurement are done at this nominal point. The measurement schematic is depicted in figure 2.1. A current source will excite the lamp with a small step current i(t), and the lamp voltage will respond according to its impedance characteristic. Measurement data of i(t) and v(t) are saved into files. A 100 hours old lamp is used during the system identification.

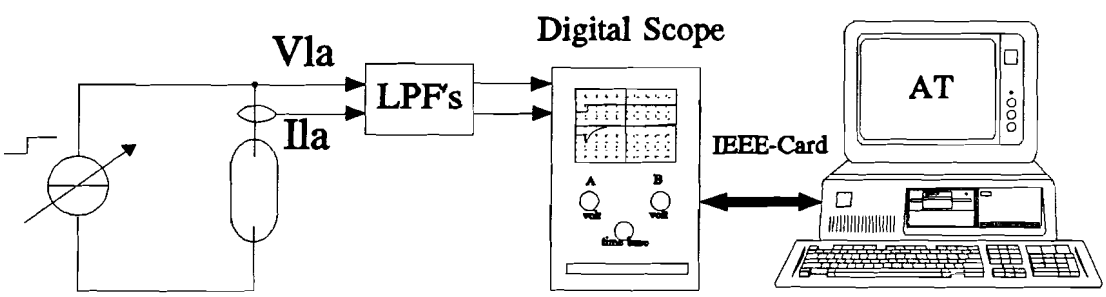


Figure 2.1. System identification scheme of A DC HID lamp parameters

The current source is a down converter based on current mode control. The range of the switch frequency of this converter is 20kHz-80kHz. The ripple current of this converter is about 20%. Low pass Filters are used to achieve noise-free measurements of the lamp current and the lamp voltage variations.

A pascal program has been developed for the calculation of the lamp parameters Z_{l1}, Z_{l2}, ω_{p1}, and ω_{p2}. This program is based on the minimum variance squared method. For more detail see appendix A. Table A.1. gives the result of the system identification.

Example results of the system identification are shown in figure 2.2. and figure 2.3. The calculation of those lamp parameters is based on formula 2.2.

Conclusion of the system identification:

a). The largest time constant $\tau_{p1}=1/\omega_{p1}$ is about 10 s, and the other time constant $\tau_{p2}=1/\omega_{p2}$ is smaller than 1 ms. This second time constant is faster than the measurement accuracy (limited by those low pass filters), so an exact value of this time constant can not be given.

b). The small signal impedance of the lamp is a non-linear system. The parameters of the lamp are changing with the current direction. Figure 3.2. and figure 3.3. give different parameters, although the current step variation for both case is the same (20% from the nominal value).

In other words: the poles and the zero of the lamp impedance shift, depending on the mean value of the current lamp.

c). In term of percentage, the voltage variation is much smaller than the variation in the current. It means $|Z_{l1}(s)+Z_{l2}(s)| \ll Z_0$. It will have certain consequences for the control power strategy (see chapter 2.2).

d). The model in formula 2 can be reduced to:

$$Z_l(s) = Z_{l1} \frac{\omega_{p1}}{(s+\omega_{p1})} + Z_{l2} \,. \qquad (2.4)$$

This is the consequence of conclusion a). This reduction is allowed if the time constant of the lamp power regulation much slower than 1 ms. The small signal impedance of the lamp in formula 2.4 will be used for the next purpose.

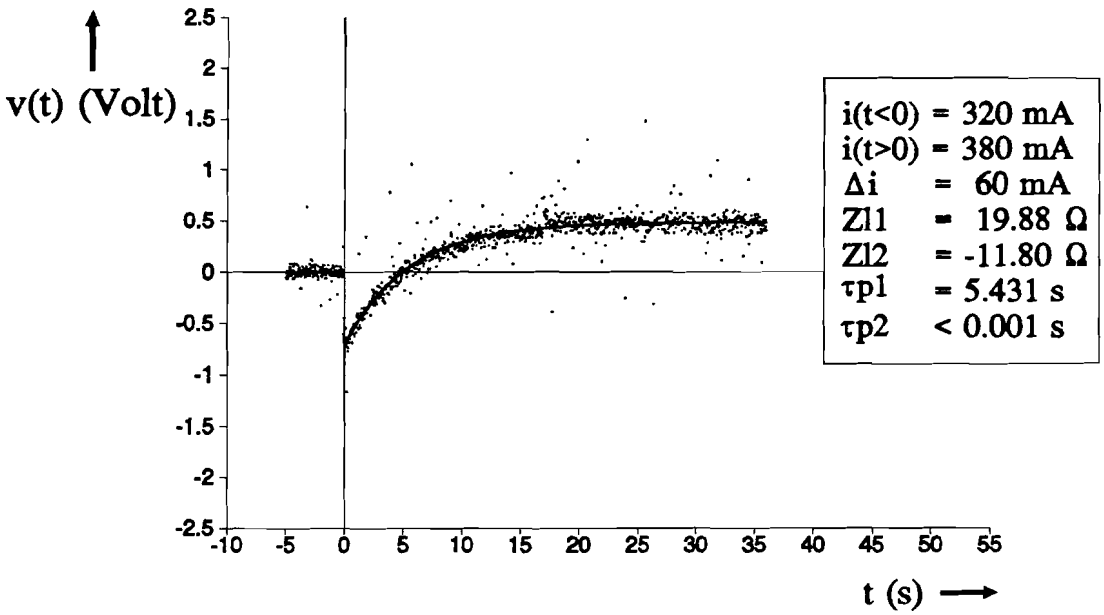


Figure 2.2. A positive step response ($\Delta i>0$) of a DC HID lamp

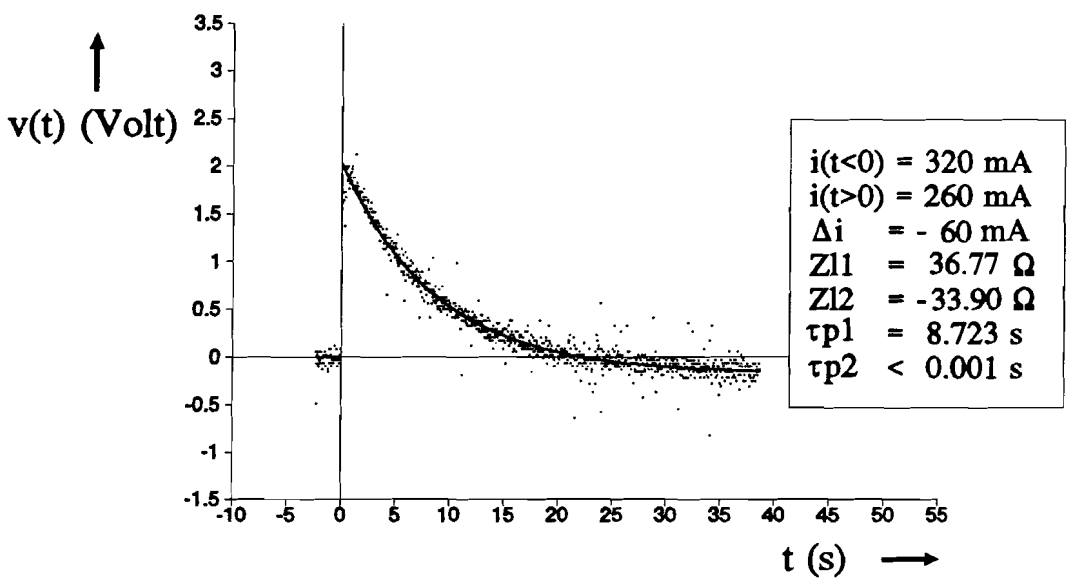


Figure 2.3. A negative step response ($\Delta i<0$) of a DC HID lamp

2.2. CONTROL STRATEGY OF POWER REGULATION FOR DC H.I.D. LAMP

In the ballast application the type of the controller is a power controller. By definition, power is voltage multiplied by current, and it is a non-linear relation. It is very complex to design a controller for a non-linear system.

The power controller must keep the lamp power constant, that is the nominal power. It has been observed at the nominal point the variation of the lamp current and the lamp voltage are small, so the variation in power will be small too. In this condition a linearization in the power relation is allowed. By linearization, the design of an optimum power controller will be much easier.

2.2.1. Linearization of Power-Current Relation

Once again, in DC system, power by definition is:

$$P_{la}(t) = V_{la}(t)\, I_{la}(t) \ . \tag{2.5}$$

Linearization is done by assuming that in the nominal state the lamp has a small disturbance,

$$P_{la}(t) = V_{la}(t)\, I_{la}(t) = (V_0 + v(t))\, (I_0 + i(t)) \ . \tag{2.6}$$

The second order term is neglectable, so:

$$P_{la}(t) - P_0 = p(t) = I_0 i(t) \left(\frac{V_0}{I_0} + \frac{v(t)}{i(t)} \right) , \tag{2.7}$$

with $Z_0=V_0/I_0$ and $Z_l(s)=v(s)/i(s)$, the linearization of the small signal power is completed (s-domain):

$$p(s) = I_0 i(s)\, (Z_0 + Z_l(s)) = I_0 i(s) Z_p(s) \ . \tag{2.8}$$

$Z_p(s)=Z_0+Z_l(s)$ represents the small signal p-i characteristic of a HID lamp.

For the 32 Watt DC HID lamp Z_0 is much larger than $Z_l(s)$. In this case the p-i characteristic will be a minimum phase system (no RHP zero in the $Z_p(s)$). Because $Z_p(s) \approx Z_0$, the variation in the lamp power will only depend on the variation in the lamp current. So a fast power regulation can be realized just by using an integrator as the power controller. The time constant of this integrator depends on the D/A converter bandwidth of the microcontroller. See chapter 5.

2.2.2. Power Control Algorithm

The control algorithm will be implemented in a microcontroller, so normalization is necessary. The controller must keep the power lamp at the nominal level. Thus it is trivial that the normalization will be based on those nominal magnitudes. p(s) is normalized with P_0, i(s) with I_0, and Zp(s) with Z_0. After normalization formula 2.8 becomes,

$$[p(s)] = \frac{p(s)}{P_0} = \frac{I_0}{I_0}\,\frac{i(s)}{I_0}\,\frac{Z_p(s)}{Z_0} = [i(s)]\,[Z_p(s)]\ . \qquad (2.9)$$

Now [p(s)], [i(s)], and $[Z_p(s)]$ are dimension less. From now on brackets means a scaled magnitude. The feedback control system for the lamp power regulation is shown in figure 2.4 (for the realization see chapter 5).

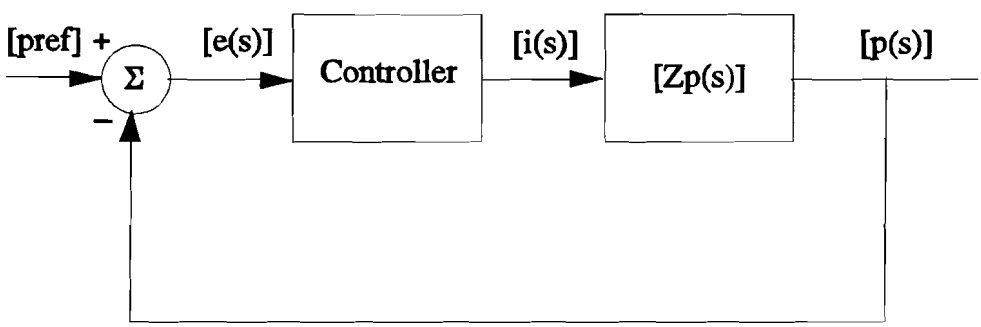


Figure 2.4. Control strategy of the power regulation of a DC HID lamp

The power of the lamp must be kept constant. The control strategy is as follows: The lamp voltage $[V_{la}(t)]$ and the current voltage $[I_{la}(t)]$ are measured. Multiplication of those two parameters results in a lamp power, so $[P_{la}(t)]=[V_{la}(t)]*[I_{la}(t)]$. This large-signal power is subtracted from a reference power (the nominal power $[P_0]$), and it will present as a small signal power [p(t)]. It is clear that the small signal power reference $[p_{ref}(t)]=0$, so the power error $[e(t)]= -[p(t)] = [P_0]-[P_{la}(t)]$. The controller, in this case an integrator, will compensate this power error by controlling the small signal current [i(t)].

3. H.I.D. LAMP BALLAST

The DC HID (High Intensity Discharge) lamp family is a high pressure lamp. Compared to a low pressure lamp, a high pressure lamp has some differences and advantages such as more compact and high power. High power means high light output, good quality, accompanies high efficacy v.v.

A DC HID lamp compared to an AC HID lamp gives a dramatic component reduction in the ballast. A commutator is not needed to supply a DC HID lamp. This saves space and lowers cost of a DC HID lamp ballast.

The specification of an electronic ballast depends on the lamp properties (for instance, a different kind of lamp asks a different method of ignition). In this research we will design a ballast for a 32 Watt HALARC Metal Halide lamp.

3.1. SPECIFICATION OF 32 WATT HALARC METAL HALIDE LAMP

Information about the lamp specifications is very important for ballast design. For instance lamp temperature, light color, acoustic resonance, steady state lamp voltage, steady state lamp current, ignition voltage and waveform (pulse or DC), ripple voltage, small signal impedance characteristic.

A 32 Watt metal Halide lamp is operated vertically, base up ± 15° in open or enclosed fixtures. This type of lighting is well known as 'down lighting'.

Traditionally, Metal halide ballast design only focused on steady-state operation, with the exception of sustaining voltages due to reignitation spikes. This is not the case for ballast design for the 32 Watt HALARC. Starting and the transition from glow to arc are critical modes of operation and must be designed correctly.

Electrical characteristics :

High performance metal halide lamp for use on General Electric Ballast E-MX32-277 (nominal switching frequency 30kHz) has following specifications[2],

Normal state:

a. Nominal lamp power : P_{nom} = 32Watt,
b. Nominal lamp voltage: V_{nom} = 90Volt,
c. Nominal lamp current: I_{nom} = 360mA.

Ignition state:

d. Minimal open circuit voltage (DC) for starting: V_{ign} = 1kV.

Pulse starting for the 32 Watt HALARC is not recommended (all parameters are DC, the lamp is a DC lamp). For more detail about the lamp specification see[2].

Starting and transition states

Figure 3.1. gives some fundamental modes of the lamp operation[2].

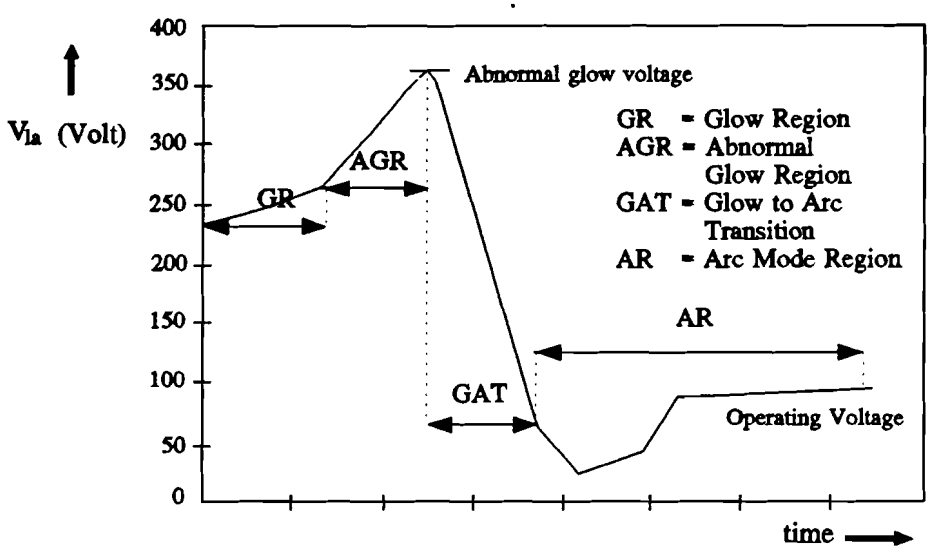


Figure 3.1. 32 Watt HALARC Lamp, Lamp Operating Modes

The first mode of the operation is the breakdown mode. In this mode the fill gas is ionized by the voltage placed across the lamp terminals.

The second mode of operation is the glow mode. The lamp travels to this mode from the breakdown mode. In this region the lamp voltage, (approx. 180-200 Vdc), rises slightly with increasing current. This is the positive resistance region. The lamp voltage may continue to increase more rapidly through a secondary glow region referred to as the abnormal glow region. The lamp voltage will peak to a value higher than the initial glow voltage. The abnormal glow voltage may reach 360-380 Vdc, dependent on the instantaneous current supplied by the ballast. It is important that the ballast has a compliance voltage greater than the abnormal glow voltage during this region. Insufficient compliance will cause the lamp to stay in glow.

The time between the peak of the abnormal glow voltage and the arc mode is referred to as the glow to arc transition region. During this period the discharge has a negative resistance and a rapidly decreasing lamp voltage.

The lamp voltage will continue to decrease to a minimum voltage of 15 to 35 Vdc. The lamp is now in the arc mode. During the first minutes of operation the lamp voltage will begin to rise to the operating voltage of the lamp as the mercury pressure increases. The time required to come up to operating voltage and the operating power is dependent on the ballast current.

3.2. A DC H.I.D. LAMP BALLAST CONFIGURATION

Figure 3.2. illustrates an electronic ballast configuration for a 32 Watt Metal Halide lamp. This configuration is based on specifications and conditions in preceding chapter.

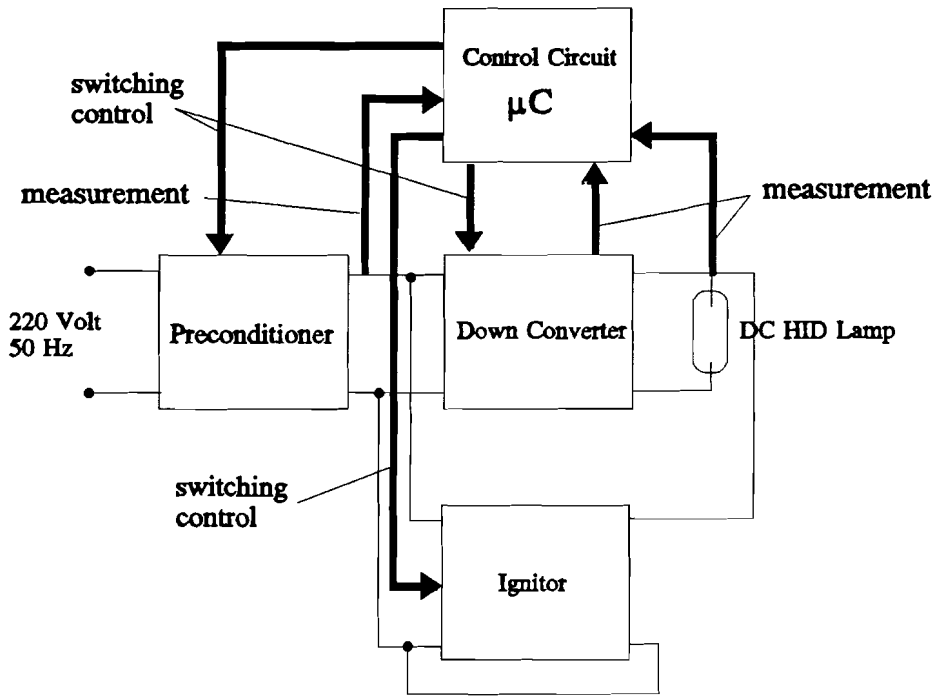


Figure 3.2. A DC HID lamp ballast configuration

The ballast is divided into 4 blocks:

a. Preconditioner,
b. Down converter,
c. Ignitor,
d. Control circuit.

The Preconditioner converts the sinusoidal voltage from the mains (rms 220 Volt, 50 Hz) into a DC level 385 Volt. The Preconditioner is designed so that the input current to the mains guarantees an optimum power-factor and keeps the mains distortion minimum.

Assume, the preconditioner is an ideal power supply with a constant output voltage 385 Volt. There are three transition states to be crossed, to bring the lamp into its normal operating state.

Initialization

Initialization is completed, if the following conditions are valid:

The output of the preconditioner is 385 Volt. The lamp is in the off state, and the lamp is not yet ignited (the lamp is an infinitely high impedance). The down converter supplies an open voltage about 385 Volt over the lamp (this voltage has a function as a compliance voltage in the abnormal glow voltage, see chapter 3.1.).

If the initialization is completed, the lamp is ready to ignite.

Ignition

If the lamp is ready to ignite, the control circuit will set the ignitor high. A high voltage of ca. 1.6kV is then placed over the terminals of the lamp. The output voltage of the ignitor is still high until the lamp is ignited or if the maximum ignition period is reached. More about the ignitor in chapter 3.5.

If the lamp is ignited, then the lamp voltage will travel in several modes (see chapter 3.1.).

In the very beginning of the arc mode, the lamp voltage is very low, about 15 Volt. It means the down converter will be shortcircuited. Protection (current limiter) is needed to avoid the overcurrent. This problem is simply solved when a current mode controller is applied to control the down converter. More about down converter and current mode control in chapter 3.3. and 3.4.

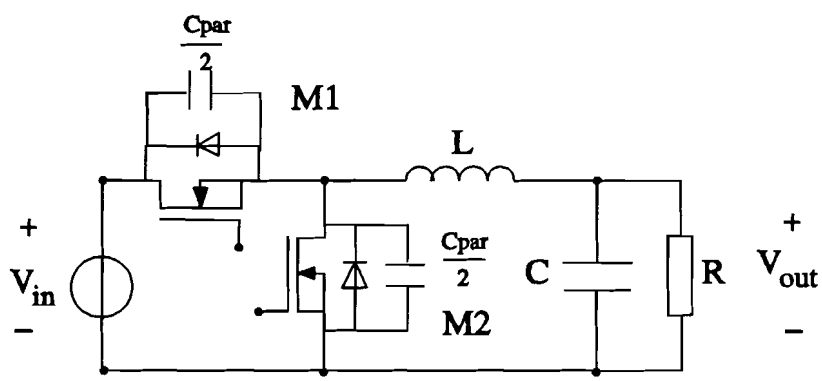
Control

When the lamp is on, the control circuit will control the power of the lamp. So the controller will bring the lamp into its operating state. The lamp power will be kept constant at 32 Watt. It is clear that the control circuit takes care of the coordination in the ballast according to required conditions. Practically, it means controlling power MOSFETs.

3.3. ForCe

Ballast design in this research will focus on the design of a down converter called ForCe (Forward Converter), which will controlled by a microcontroller (in this context the term "Forward Converter" is not related to a type of down converter which uses a transformer as a galvanic coupling between the input and the output of the converter).

ForCe has a very high switching frequency, 200kHz. The microcontroller can not directly control the ForCe (those power switches), caused by its speed limitation and control accuracy. An convenient interface between µ-controller and the ForCe is then required. That is a Voltage Controlled Current Mode Controller. The schematic of the ForCe and its operation modes are depicted in figure 3.3 and 3.4. The inductor current in every mode is given in figure 3.5.



Forward Converter = ForCe

Figure 3.3. ForCe

V_{in} = DC input voltage of the ForCe (385 Volt),
V_{out} = Output voltage of the ForCe,
L = Inductor,
C = Output capacitance,
R = Resistor (simulates the lamp in normal state),
C_{par} = Total parasitic capacitance of the MOSFETs,
I_{plus} = Maximum of the inductor current i_L,
I_{min} = Minimum of the inductor current i_L,
T_s = Switching frequency,
δ = Duty cycle,
τ_1 = Charge time of the parasitic capacitance,
τ_2 = Discharge time of the parasitic capacitance,

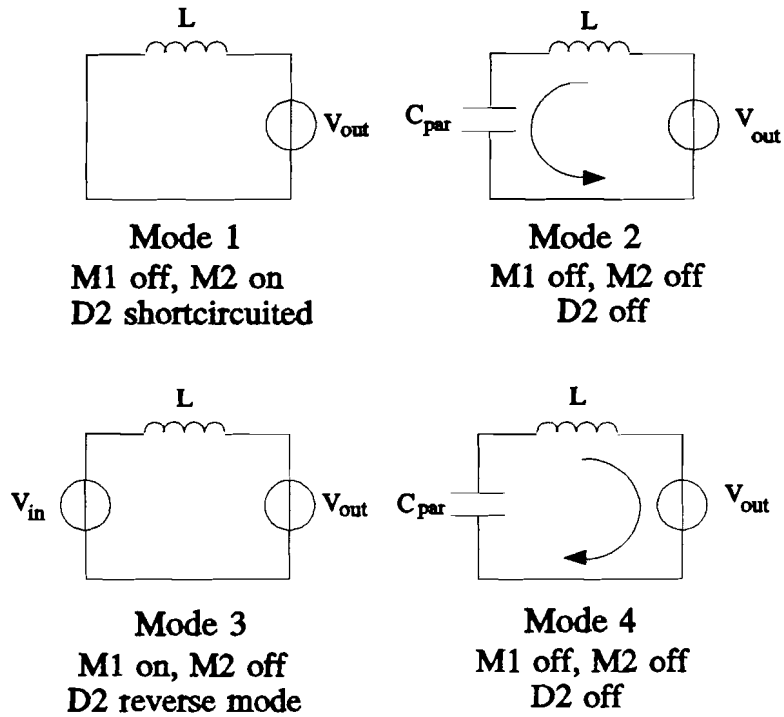


Figure 3.4. ForCe and its operating modes

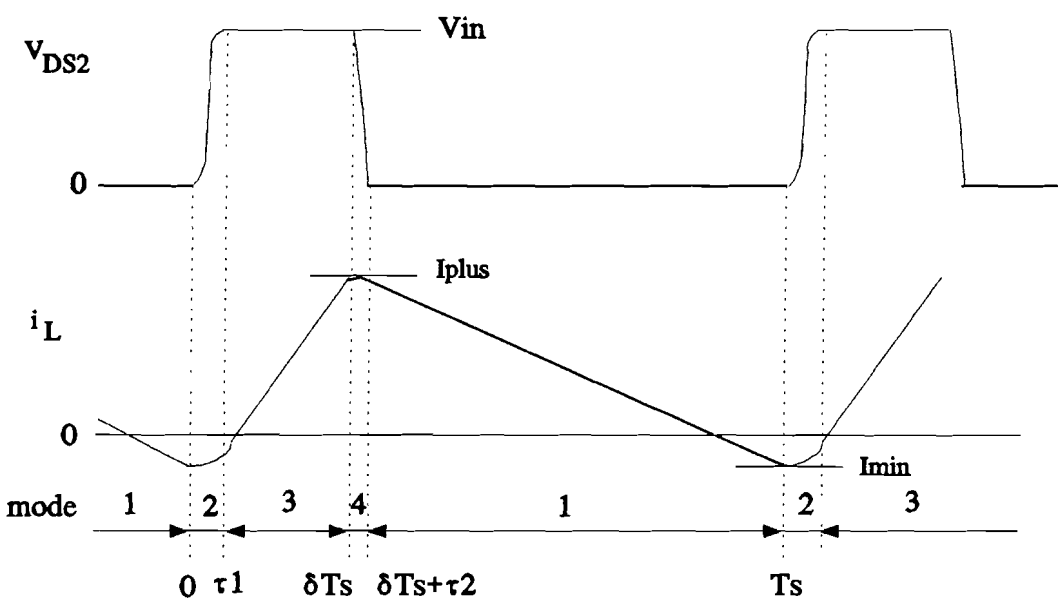


Figure 3.5. Inductor current i_L and V_{DS2} in several modes

M1 = Main MOSFET
M2 = Second MOSFET
D1 = Parasitic diode of the main MOSFET,
D2 = Parasitic diode of the second MOSFET.

Assumed the ForCe is in steady state, so V_{out} is about δV_{in}.

Mode 1: M1 is off, M2 is on, and D2 is shortcircuited. The inductor voltage $V_L=-V_{out}<0$, so i_L decreases linearly. If I_{min} is reached ($I_{min}<0$), then M2 is switched off. The converter is then in Mode 2.

Mode 2: M1 is still off, M2 is off, and D2 is off. The parasitic capacitance C_{par} then will be charged with an energy of $\frac{1}{2}LI_{min}^2$. So the voltage over C_{par}, is also equal to V_{DS2}, will increase. In other words the inductive energy is converted into a capacitive energy $\frac{1}{2}C_{par}V_{DS2}^2$. We can design so that V_{DS2} is equal to V_{in}, when at that moment (τ_1) the main MOSFET is switched on. So Zero Voltage Switching (ZVS) is achieved[3,4]. Therefore the switching loss is reduced.

Mode 3: M1 is on, M2 is off, and D2 is in reverse mode. The inductor voltage $V_L=V_{in}-V_{out}>0$. So the inductor current will increase linearly. When I_{plus} is reached M1 will switch off.

Mode 4: M1 is off, M2 is off, and D2 is off. C_{par} will be discharged. V_{DS2} will decrease very rapidly (τ_2). When V_{DS2} becomes zero M2 is switched on (ZVS)[4].

A conventional down converter has just 2 modes. They are Mode 1 and Mode 3 of the ForCe. It is clear that the ForCe is a down converter, where the diode of this conventional converter is replaced by a MOSFET. By using this extra MOSFET, a negative inductor current can be applied. In this way reduction in the switching losses is achieved (Mode 2 and Mode 4). Experimentally an efficiency of 90-95% is reached.

In the literature, the ForCe is known as a Buck converter based on ZVS-QSC (Zero-Voltage-Switch Quasi-Square wave-Converter) technique[4].

3.3.1. Design of Filter (R,L,C) of the ForCe

The resistor R

The resistor design is easy,

$$R = R_{la} = \frac{V_{la}}{I_{la}} . \tag{3.1}$$

Assume V_{la}=100Volt and I_{la}=320mA, then R is equal to 312.5Ω.

The Inductor L

The design of the inductor is based on ZVS (Zero Voltage Switching), where the energy balance of the inductive energy $\frac{1}{2}LI_{min}^2$ and the capacitive energy $\frac{1}{2}C_{par}V_{in}^2$ is used. More detail see in appendix B. The negative peak current I_{min} as function of the parasitic capacitance C_{par} is given in the next relation, and depicted in figure 3.6.

$$I_{min} = -I_{par}\left[1 + \sqrt{1 + 2\left(\frac{I_{la}}{I_{par}}\right)}\right], \tag{3.2}$$

$$I_{par} = \frac{C_{par}V_{in}}{\delta(1-\delta)T_s} .$$

I_{par} has a dimension of Ampere, and it can not be measured.

The value of L follows from the relation,

$$L = \frac{\delta(1-\delta)V_{in}T_s}{2(I_{la}-I_{min})} . \tag{3.3}$$

L as function of C_{par} is given in figure 3.7. If C_{par} is 150pF, δ=0.256, T_s=5μs and V_{in}=385Volt, then I_{min} is about -275mA. So the inductor L is about 320μH.

We see I_{min} is in the range of the I_{la}. This is the consequence of a design in low power converter. The value of C_{par} depends on the type of the used MOSFET. If C_{par} could be smaller, I_{min} would be smaller, but L becomes larger.

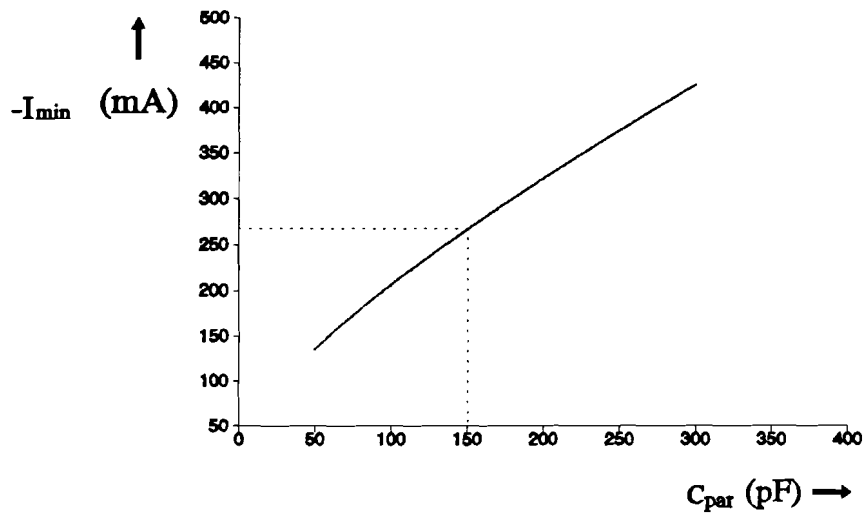


Figure 3.6. I_{min} versus C_{par}, with V_{in}=385V, δ=0.256, T_s=5μs, and I_{la}=320mA.

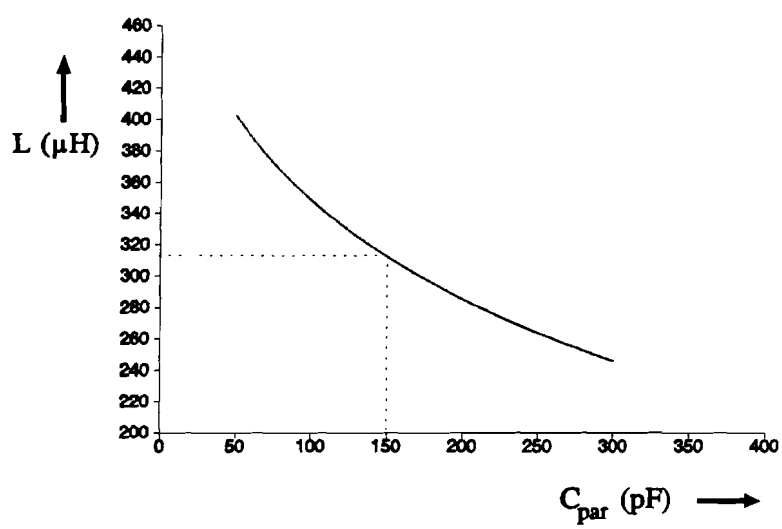


Figure 3.7. L versus C_{par}, where V_{in}=385 V, δ=0.256, T_s=5μs, and I_{la}=320mA.

The output capacitance C

The design of the output capacitance is based on the value of the allowed ripple output voltage. A ripple of 5% is a typical design value. From experience the acoustic resonance effect is in this case avoided.

A relation between the ripple voltage and filter parameters is given in the next relation (derivation see in appendix C):

$$\left[\frac{\Delta V_{out}}{V_{out}}\right] = 4\,\frac{\sin(\pi\delta)}{\pi\delta}\,\frac{\frac{1}{LC}}{\sqrt{(\frac{1}{LC}-\omega_s^{\,2})^2+(\frac{\omega_s}{RC})^2}}\,, \qquad (3.4)$$

where $\omega_s=2\pi/T_s$. Figure 3.8. gives the relation between C and the related ripple.

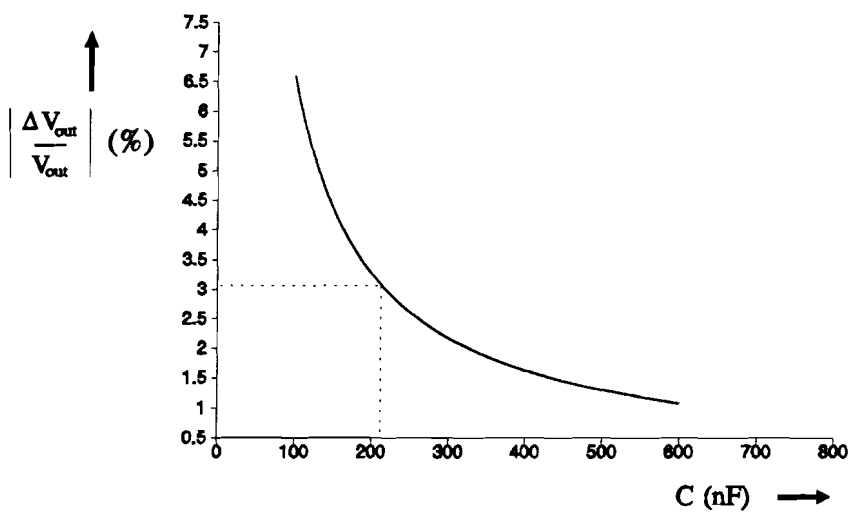


Figure 3.8. Relative ripple versus C, with L=350μH, δ=0.256, and T_s=5μs.

We see in figure 3.8. a large capacitance is related to a small ripple. For our ForCe, the value of the output capacitance C is chosen equal to 0.22μF, thus the relative ripple in nominal state is about 3%.

3.3.2 Level Shifter

The switching state of the main MOSFET is complementary with the switching state of the second MOSFET. The gate of the second MOSFET can be controlled directly by a low voltage pulse (+12 Volt). For the main MOSFET a level shifter is needed. The level shifter causes delay in the on-state of the main MOSFET. This is not a disadvantage. Actually, the trick of the second mode is valid during this delay period, which will improve the efficiency of the converter. The complete schematic of the ForCe is depicted in appendix D.

3.4. CURRENT MODE CONTROL (C.M.C.)

Unlike PWM direct duty ratio, where to control the inductor current (the duty ratio) a fixed frequency sawtooth waveform is compared with a control voltage is applied, current mode control directly controls the output inductor current that feeds the output-stage. Current Mode Controlled effectively eliminates the phase lag of a control function associated with the output filter inductor or the energy-storage inductor. CMC is far superior to the commonly used PWM duty-ratio controllers. Figure 3.9. illustrates the ForCe and CMC configuration.

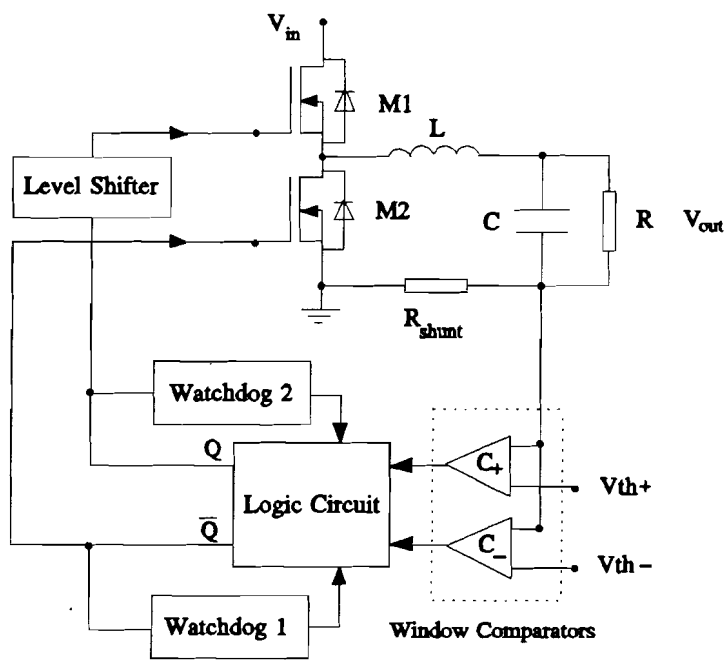


Figure 3.9. ForCe based on Current Mode Control

R_{shunt} = Sensor of the inductor current i_L,
V_{TH+} = Control voltage which is proportional to the maximum of i_L (I_{plus}),
V_{TH-} = Control voltage which is proportional to the minimum of i_L (I_{min}),
C+ = Comparator which detects the maximum of i_L (I_{plus}),
C- = Comparator which detects the minimum of i_L (I_{min}),
$\bar{Q}$ = The output of the logic circuit which controls the switch state of M1.

The ForCe controlled by CMC creates a current source, which is required for the ballast application. Those control voltages, V_{TH+} and V_{TH-}, are controlled by a compensator. The type of the compensator depends on the type of controlled system. It could be a voltage-, current-, or power regulation. Here a power regulation is required.

3.4.1. Principle of C.M.C.

Normal state

Assume the ForCe is in the steady state of normal operation. The main MOSFET is on, so the inductor current increases linearly. If i_L becomes equal to I_{plus}, the main MOSFET is then switched off. Now the second MOSFET is switched on (with a small delay τ_2). The inductor current then decreases linearly. If i_L becomes equal to I_{min}, the second MOSFET is switched off, and the main MOSFET switches on (with a natural delay τ_1, caused by the level shifter). And so on.

Figure 3.10. depicts the inductor current in the normal state. Those modes of the ForCe are not described in detail anymore. In stead of those modes, figure 3.10. marks the component (C_+, C_-, Watchdog1=WD1, or Watchdog2=WD2) which force the logic circuit to control the state of those MOSFETs.

In this way the inductor current will be limited in a band (I_{plus},I_{min}). So overcurrent is avoided. To realize this principe, the inductor current must be measured. This signal then is compared with two reference voltages (V_{TH+} and V_{TH-}) which are proportional with I_{plus} and I_{min}. The outputs of these comparators are inputs to a logic circuit, which decides the state of the main- and the second MOSFET.

The relation $|Z_l(s)| \ll Z_0$ is valid for the 32Watt DC HID lamp in the normal state. It means the power variation p(s) depends only on the current variation i(s), and the lamp voltage $V_{la}=V_0$ is constant. Assumed V_{in} is also constant, so the duty cycle of the M1 gate pulse must be constant too ($V_0=\delta V_{in}$). I_{min} is also a fixed magnitude. I_{plus} can be written as:

$$I_{plus} = \frac{V_{in} - V_{la}}{L} \delta T_s + I_{min} \qquad (3.5)$$

Now I_{plus} depends only on the switching period T_s. Summary: $\partial P_{la} \sim \partial I_a \sim \partial I_{plus} \sim \partial T_s$. So the lamp power is variable proportionally to the variation of the switching period of the ForCe T_s ($T_s=1/f_s$). In this case CMC operates as a VCO (Voltage Controlled Oscillator).

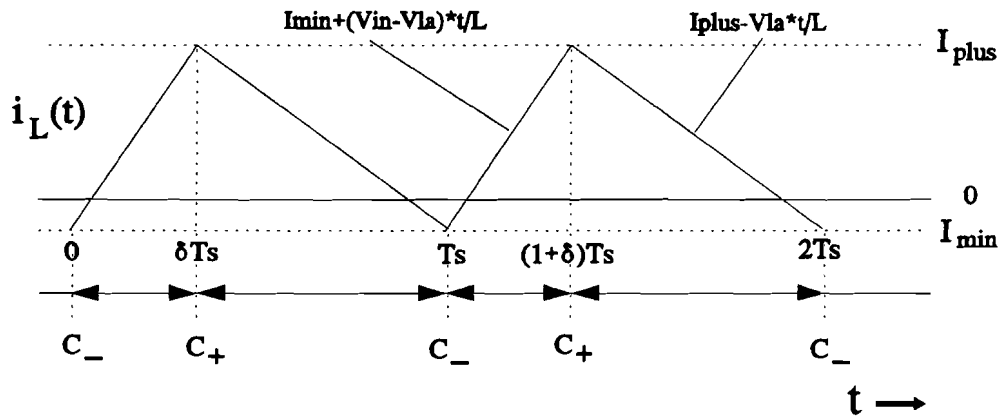


Figure 3.10. The inductor current i_L in normal state

Open circuit

In the start-up phase, our ForCe must be able to supply a compliance voltage in open circuit (lamp is not ignited yet). Therefore in steady state the mean value of the inductor current is almost zero. If our CMC is only based in normal state, there will be a problem. This is because i_L will never reach I_{plus}. It means the main MOSFET will be always on. If the main MOSFET is on too long, it will damage the MOSFET (the level shifter does not work anymore). Therefore a timer or a watchdog is needed. So if a certain wait time is passing this watchdog will switch off the main MOSFET. If the main MOSFET is switched off, then the inductor current will rapidly decrease. If i_L becomes equal to I_{min}, C_- will switch the main MOSFET on.

The mean value of the inductor current is almost zero, so the positive peak of the inductor current must be about $-I_{min}$. This information tells, how long the watchdog should wait. See figure 3.11. The switching frequency in the open-circuit is much lower than in the normal state.

$T_{open}=-2LI_{min}(V_{in}/(V_{in}-\Delta V))/\Delta V > T_s$, where ΔV is about 5Volt (V_{in}=385Volt).

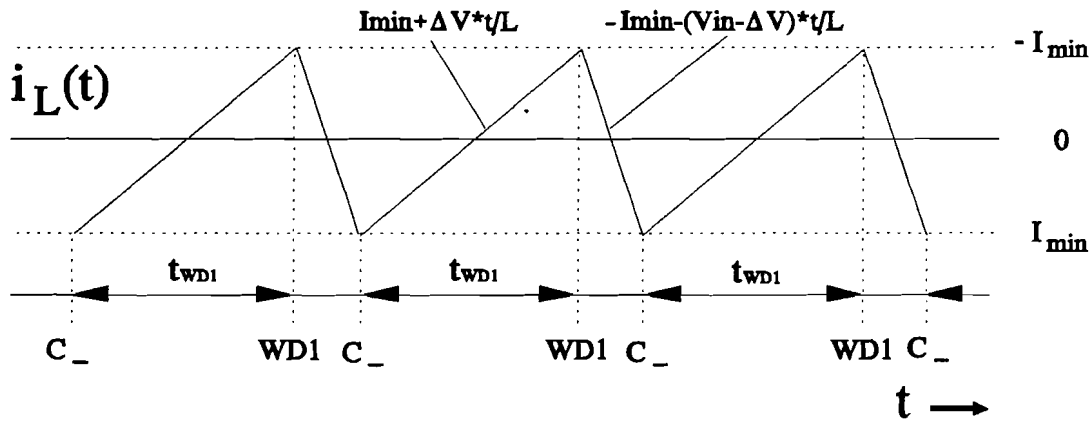


Figure 3.11. The inductor current i_L in the opencircuit state

Short circuit

After ignition, the lamp voltage will decrease to a low level voltage (typically 15 Volt), so the ForCe will be short-circuited. The inductor current will increase very fast, but when the I_{plus} is reached the main MOSFET will be switched off. Because the output voltage is very low, the inductor current will decrease very slowly (approximately exponential). The decay time of this current depends on the shunt resistor R_{shunt} and the inductor L. The inductor current will never reach I_{min}, so a second watchdog is introduced. By choosing a relative large wait time, the main MOSFET will be switched on again when the inductor current is almost zero. The mean value of the inductor current then has the same range as in the normal state. See figure 3.12. The switching frequency in the short-circuit is also much lower than in the normal state.

$T_{short}=(I_{plus}-\Delta I)L/V_{in}+(L/R)\ln(I_{plus}/\Delta I)>T_s$, where ΔI is very small (see figure 3.12).

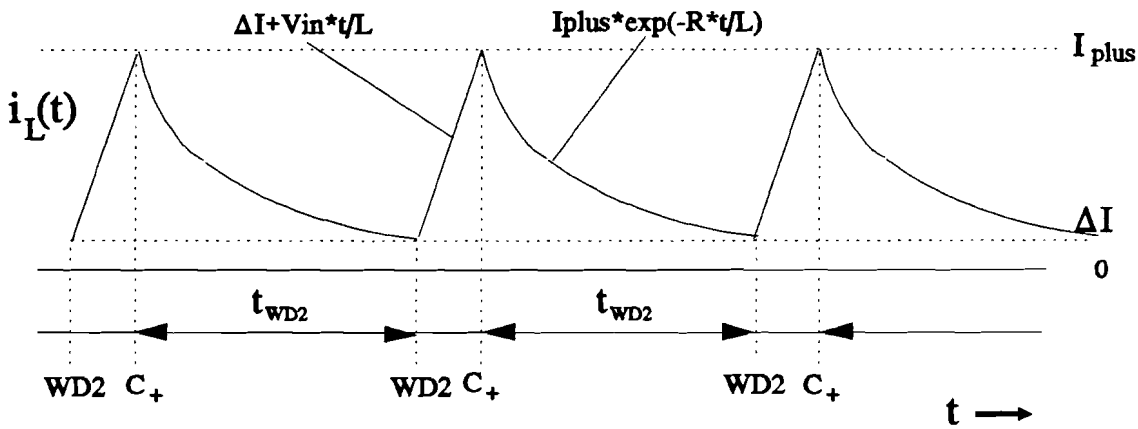


Figure 3.12. The inductor current in the shortcircuit state

3.4.2. Design of C.M.C.

So the CMC is divided into 4 blocks:

a. Current sensor R_{shunt},
b. Two window comparators (C_+ and C_-),
c. Logic circuit,
d. Two watchdogs.

Current sensor

R_{shunt} is supposed to be small to keep losses minimal. R_{shunt} is placed between the low side of the output capacitance and ground, so the signal can be used directly for the next purpose:

Window comparators

There are two window comparators. The first comparator, C_+, compares i_L*R_{shunt} to the required positive level ($V_{TH+}=I_{plus}*R_{shunt}$). The second one, C_-, compares i_L*R_{shunt} to the required negative level ($V_{TH-}=I_{min}*R_{shunt}$).

For this purpose fast comparators must be applied. Delays will cause imperfection in the control loop.

Logic Circuit

In normal state there are three parameters which decide the state of the M1 gate pulse (Q_{new}). They are C_+ (output of the first comparator), C_- (output of the second comparator), and Q_{old} (the previous state of the M1 gate pulse). So we can design a flip-flop circuit with memory, according to a new- and old state of those three parameters C_+,C_-, and Q. The result of this logic circuit is quite amazing, it is a SR Flip-Flop.

The preliminary result of the control circuit is given in figure 3.13, where this relation is valid:

$$\overline{Q}_{new} = C_+ + C_- \overline{Q}_{old} \tag{3.6}$$

Check it out!, if C_+ is high Q is always low.

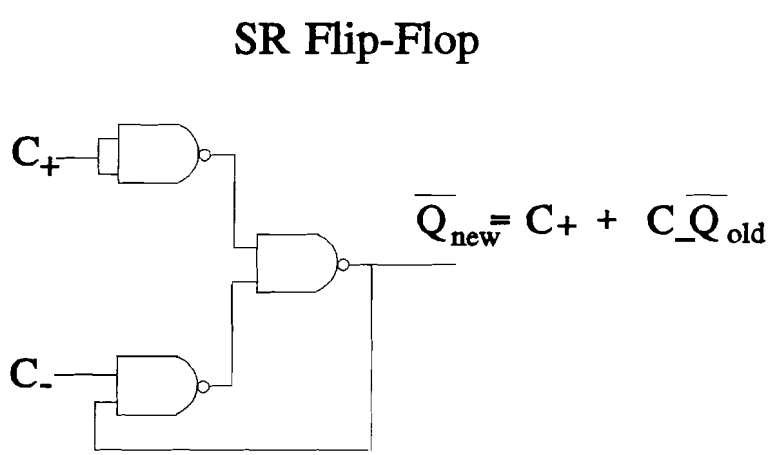


Figure 3.13. SR flip-flop

Watchdogs

According to 3.4.1., a current mode controller based on the normal state only is not enough to control the ForCe. To operate the ForCe in open- and short-circuit, watchdogs are needed. The principle and the realization of a watchdog for this ForCe is relatively simple. The schematic of the watchdog is given in figure 3.14.

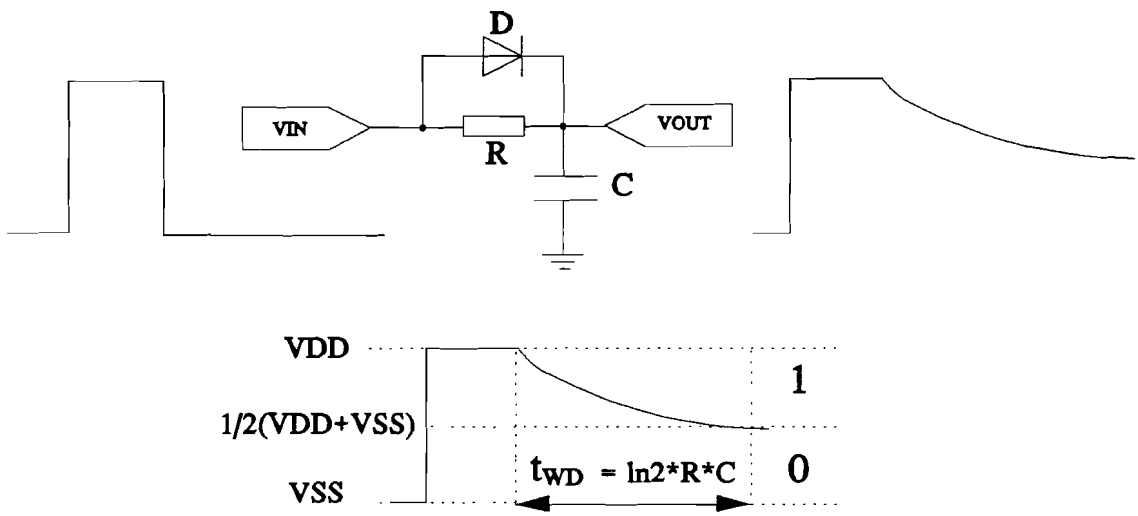


Figure 3.14. The principle of the watchdog

Assumed Q is high, the main MOSFET is on, then the output of the first watchdog WD2 is also high (the watchdog diode is conducting so the capacitance is rapidly charged). But if Q becomes low, the main MOSFET is off, the output of WD2 will decay according to a RC time. Logically (digital) speaking, as long as the analog output of the watchdog is greater than $\frac{1}{2}(V_{DD}+V_{SS})$, the logic circuit will handle this level as a high logic level. If the output of WD2 is lower than the half of the high logic level it will be treated as a low logic level. Now, $\bar{C}$ becomes low then Q is high. If $\bar{C}$ is not low (I_{min} is not reached yet) until the wait time of the second watchdog t_{WD2} is equal to $\ln 2 * R_{WD2} * C_{WD2}$ is passed, the logic level of WD2 will become low. WD2 will force the output logic circuit Q high, so the main MOSFET will be switched on.

An extra extension to the logic circuit is needed. This extra component (gating to the SR flip-flop) will make a decision who switches the main MOSFET on, $\bar{C}$ or WD2. Note $\bar{C}$ is dominant to WD2.

The working of WD1 is analogous to WD2. The complementary of Q will operate as the input of WD1. An extra gating is also needed. The complete diagram of the CMC is given in figure 3.15. (see also appendix E).

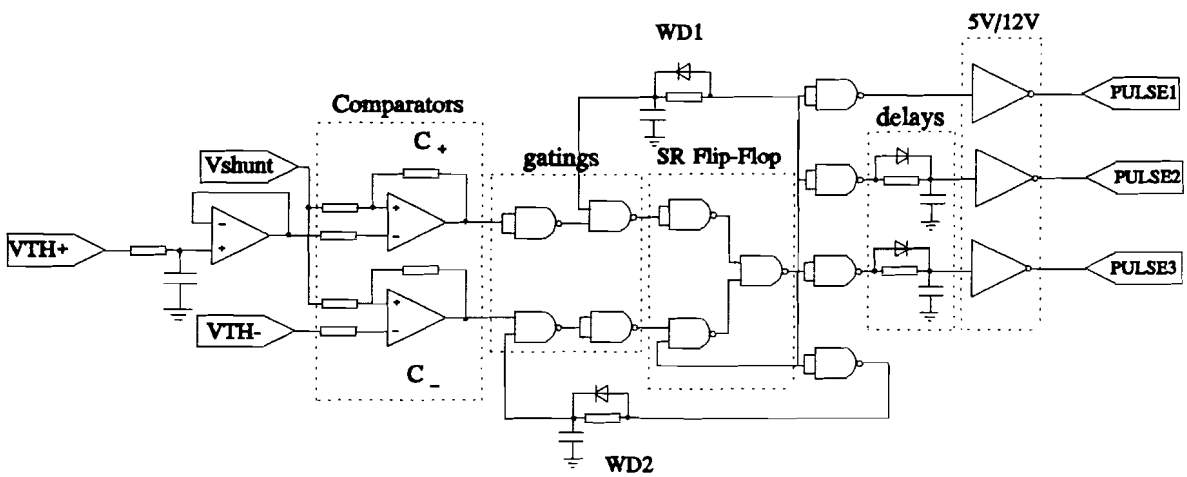


Figure 3.15. Complete diagram of the current mode controller

PULSE1 is connected to the gate of the level shifter MOSFET M3. It is clear that the gate pulse of M3 is the complementary with the gate pulse of M1.

PULSE2 is connected to the basis of the level shifter BIPOLAR B_{ls}. Assumed, M1 is being switched off. The drain of M3 can have a certain voltage (supplied by a divider, R_2 and R_3, from $V_{cc}=+12V$, see appendix E). It is possible that this voltage is greater than the threshold voltage of M1. So M1 is not really switched off. But if the level shifter BIPOLAR is switched on, R_3 will be shortcircuited, so the drain voltage of M3 becomes zero. Now M1 is really switched off.

PULSE3 is connected to the gate of the second MOSFET.

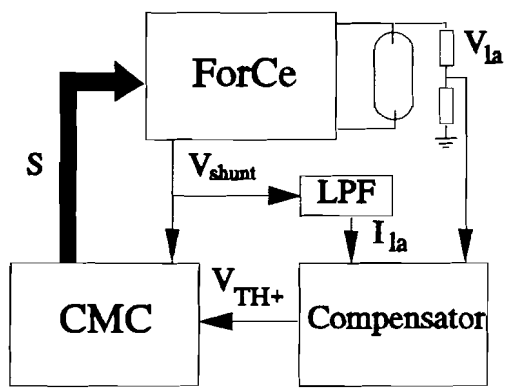
3.4.3. Voltage Controlled C.M.C.

ForCe plus CMC creates a variable current source. The output current I_{la} is variable with V_{TH+}. By first order approximation, I_{la} is equal to $\frac{1}{2}(I_{plus}+I_{min})$. Assumed I_{min} is constant, then I_{plus} has a linear relation with I_{la}.

The requirement is to control the load power. There are two important parameters that must be measured to control the output power, they are the output current I_{la}, and the output voltage V_{la}. The output power P_{la} is then $V_{la}*I_{la}$. The P_{la} is compared with the reference power P_{ref}, which results in a power error. This power error will be compensated by a controller (compensator). The output of this compensator will control I_{la} via i_L, in this case by variation of the control signal V_{TH+}.

The feedback system regulates the output power in such a manner that the error power tends to be equal to zero, thus $P_{la} \rightarrow P_{ref}$.

V_{la} is measured via a divider, and I_{la} is measured by filtering V_{shunt}. The simplified presentation of ForCe inclusive CMC and the compensator is depicted in figure 3.16.



LPF = Low Pass Filter,
S = Switch Pulses to M1 and M2.

Figure 3.16. Simplified schematic of the power regulation

3.5. IGNITOR

To bring the lamp in on state, first the lamp must be ignited. The schematic of the ignitor is given in figure 3.17.

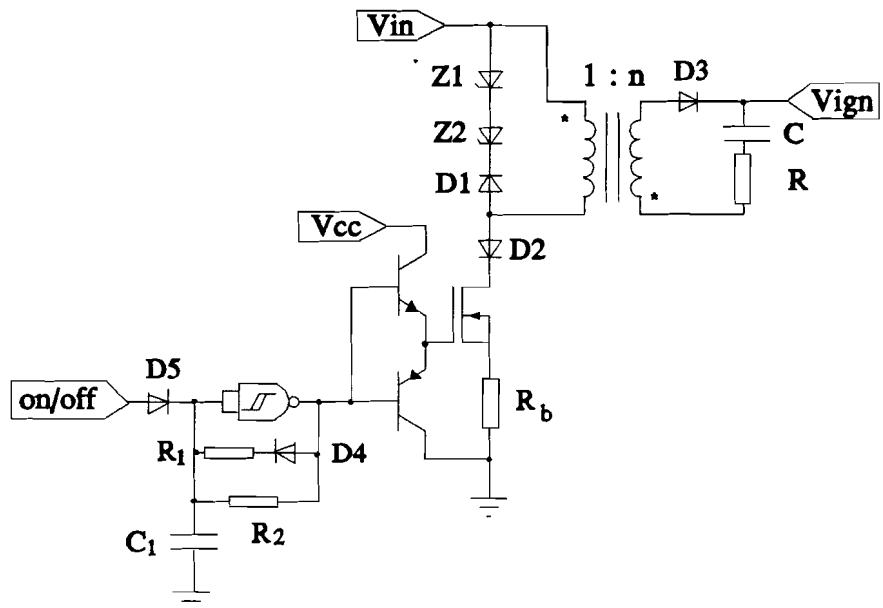


Figure 3.17. Ignitor

The ignitor is a fly-back converter. The input voltage of this converter is 385 Volt. The switch frequency of the MOSFET is about 200kHz, with a duty cycle of 0.1. The transformation ratio n is 4. So in open circuit the ignitor output will be about 4*385V≈1.6kV. This DC voltage is enough to ignite the DC HID lamp.

If the lamp is ignited the pulse to the gate of MOSFET will be set off. This occurs when the lamp voltage becomes low, ca. 100Volt (the lamp is in glow to arc transition, see figure 3.1.). After that the ForCe will feed the lamp.

Assume the ballast is in ignition state. When the lamp is not on, after a certain ignition time has passed (typically 60s for a 32Watt DC HID lamp), the gate pulse of the MOSFET will be set off. So temporary the ignition action is canceled. After a certain waiting time the ignitor will set on again. If the lamp is still not on after several tries (for instance 5 times), the ignition will be canceled. In this case the lamp is probably defect. If the lamp is replaced by a new one, the ballast has to be reset first.

4. MICROCONTROLLER 80C166, FORTH AND TASK INVENTORY

A research on a universal microprocessor (μP) or microcontroller (μC) for ballast application has been done[5]. The evaluation of the research is based on an optimum controller for a 400kHz, 250Watt Forward Converter (ForCe). In this context optimum is in terms of capacity, interactivity, and price. The possibility of DSP (Digital Signal Processor), RISC (Reduced Instruction Set Computer), and some microcontrollers have been investigated. For more detail see[5].

There is no fast processor which can control the ForCe directly. So an interface between the processor card and the ForCe is needed. This interface is a voltage controlled current mode controller (see chapter 3.4). In this way a relative slow μ-processor/μ-controller is applicable.

A moduNORM 80C166 is chosen as a universal μC-card for ballast application. Currently, the 80C166 microcontroller is the state of the art in embedded control. Compared to some other cards (DSP- and RISC cards) this 80C166 card has some great advantages such as low cost, large number of ADC channels, large number of PWM channels, flexible I/O facility, and feasibility for programming in a high level language (HLL). Combination of a HLL such as FORTH and this 80C166 card results an interactive program development system. Interactive here means changes to an algorithm can be made at any time, by using a simple terminal emulator program on PC. This system can be realized because FORTH is not only a compiled language, but also an interpreter.

4.1. ModuNORM 80C166

The Siemens 16-bit 80C166 is a RISC-like μ-controller. It utilizes a 4-stage pipeline and has a dual-ported register file. The device includes a branch-target cache, with caches the last branch target address to minimize branch delays during looping. And like later RISC chips, the 166 has multiply and divide instructions[6].

80C166 differs from classic RISC CPUs. First, it has no data or instruction caches. Instead, the μ-controller holds 8 kbytes of ROM or PROM and 1 kbyte of RAM on chip and addresses as much as 64 kbytes of external memory. Second, unlike RISC processors, the 166 is not a load/store machine in which all accesses to memory are loads and stores and all data manipulation is between registers. In the 166, one can add a register to a memory location. More about 80C166 architecture see[6].

ModuNORM 80C166 is a card based on 80C166. The technical data of ModuNORM 80C166[7]:

- Central Processing Unit Siemens SAB 80C166,
- Quartz oscillator 40MHz,
- 1 kbyte fast static dual ported RAM on the µ-controller chip,
- 64 kbyte RAM, 70ns for running with 0 wait states,
- 2*bytewide sockets, for up to 192 kbyte EPROM,
- 2 serial channels, TTL/CMOS levels,
- 100ns instruction cycle time,
- watchdog timer,
- 5 general purpose timer/counter with a resolution of 200/400ns,
- 56 I/O lines in the multiplexed version or 40 in the non-multiplexed version,
- 10 channels 10-bit A/D converter with conversion time 9.75 µs,
- 16 channels PWM,
- Power supply 5V/200mA,
- Mechanical dimensions 50X80 mm^2.

An A/D converter can be realized by filtering a PWM output with a simple RC network (only the DC component of the PWM is passed). By variation of the PWM duty cycle, the DC output voltage of the RC filter can be varied proportionally.

The ModuNORM 80C166 will be used as the controller of the ballast system.

4.2. 80C66 + FORTH = INTERACTIVE SYSTEM

The software will be written in FORTH. The main argument is that FORTH has a dual nature. In one sense it is an interpreted language, but it can also be thought of as a compiled language. In development and test state of an algorithm implementation such an HLL is very handy to use.

Relative to other HLLs such as BASIC and PASCAL, FORTH programs tend to be shorter. In term of memory usage, FORTH is also smaller. That means a compiled FORTH program will run faster.

On the 80C166 card no BASIC/PASCAL are available. If they were, they don't allow access to the hardware. Compiled languages are not interactive, meaning hardware emulators (ICE) must be used, adding cost and complexity. With an interpreter, changes to the algorithm can be made at any time, using a simple terminal emulator program on a PC. Therefore, interaction between a designer and the processor card is very simple.

Diagram of the interactive development board is depicted in figure 4.1. First a FORTH KERNEL is programmed into EPROM's (2*bytewide). It results a FORTH SYSTEM on those EPROM's. At the every beginning of the card operation, the FORTH SYSTEM in the EPROM's is downloaded to the RAM of the µ-controller. So after the download the µ-controller can speak FORTH.

A terminal emulator is used as a medium to develop the software. A new WORD (program) is built from WORDS (programs) which are already exist in the FORTH SYSTEM Library.

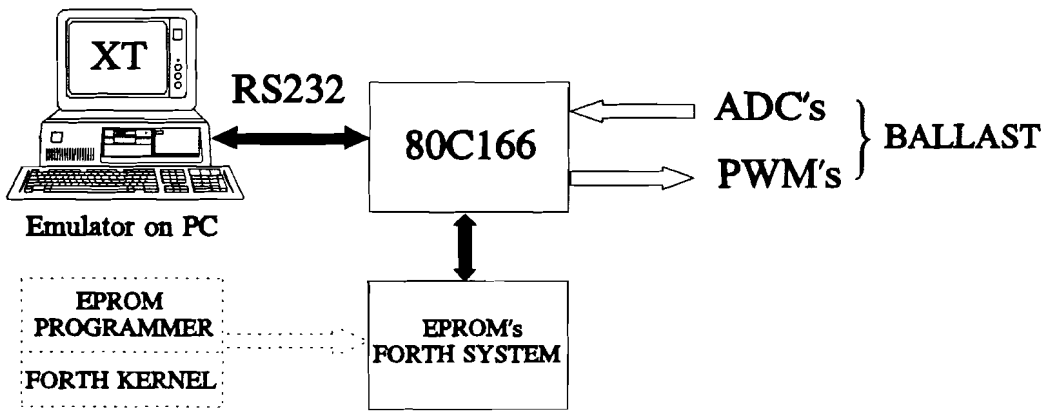


Figure 4.1. Diagram of the interactive development board based on 80C166

A designer on the PC communicates with the microcontroller via a standard RS232 serial line. A program can be send to the microcontroller at every time. In this case the CPU of the microcontroller will act as an interpreter. The microcontroller then will execute those program instructions. It could be an integer arithmetic calculation, reading an A/D converter channel, timing/counting, or generating of a PWM pulse with a certain duty cycle and frequency, etc. A program can be saved into a file on PC.

Program development in FORTH SYSTEM is in fact just building those advanced WORDS from basic WORDS.

4.3. TASK INVENTORY

The 80C166 card will used as the controller of the DC HID lamp ballast. There are two general important tasks of the μ-controller:

1. Measure

- Measurement of a scaled DC signal or a scaled relative slow varying signal (AD converter),
- Measurement of time interval (timer/counter),
- Measurement of a digital level (AD converter), etc.

2. Control

- Control of a voltage (DA converter),
- Control of switching pulse; duty cycle, or frequency (PWM),
- Control of logic level; on/off (Capture and Compare), etc.

The tasks that will be handled by the microcontroller to control the DC HID lamp ballast are collected in the next section.

4.3.1. Preconditioner: Possible Tasks for the μ-controller

A brief explanation about the operation of the preconditioner is given in chapter 4.1. For more detail see[8].

a. Gate Pulse

The μ-controller could control the gate pulse of the preconditioner MOSFET directly. The frequency sweep of the gate pulses lies between 20kHz-200kHz[8].

Assume a feedback system will be applied in this preconditioner to keep the output voltage constant. In this case, a directly controlled gate pulse of the MOSFET for the 80C166 is not possible. The accuracy of a PWM pulse of 80C166 becomes worst with a higher frequencies. To realize a feedback control system of this converter, an interface between the microcontroller and the preconditioner is needed. This is a indirect switch control method and has a relative slow time constant.

b. Compensator

The output of the preconditioner must be kept constant, 385 Volt. A controller is needed. An integrator is a solution of this requirement. This algorithm can be implemented in the microcontroller. A timer is needed to realize a certain sample time.

c. Measurement

To control the output voltage, the output voltage must be measured. This magnitude is compared with a reference value, resulting in an error voltage. Following an algorithm this error will be compensated for. An A/D converter is needed to measure this controlled magnitude.

d. Generating a Control Voltage V_c

In an indirect switch control method, a control voltage is used to control the gate pulse of the MOSFET. A D/A converter is needed to generate a control voltage. The variation of this control signal depends on the compensator algorithm.

e. Overcurrent Detector

The inductor current of the preconditioner will be limited by the overcurrent detector. In this way a saturation in the inductor current is avoided. An A/D converter can be programmed to generate a logic level (software).

Figure 4.2. shows a controlled preconditoner based on 80C166. The zero detector is connected to the switching control interface (SCI). The zero detector gives an interrupt to the SCI if the mains voltage crosses zero. This information is needed to synchronize the working of the SCI. More about the control principle see[7].

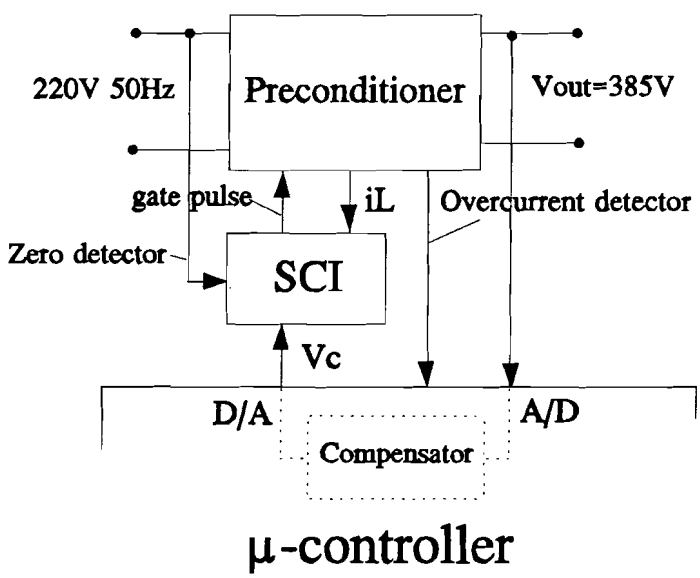


Figure 4.2. A controlled preconditioner based on 80C166

4.3.2. ForCe: Possible Tasks for the µ-controller

The explanation about the operation of the ForCe is described in chapter 3.3.

a. Gate Pulses

The nominal switch frequency of the ForCe is 200kHz. The µ-controller can not control those gate pulses of the MOSFETs directly. So an interface is used, to create a relative slow control system. A Current Mode controller will take care of the switching pattern.

If one designs a ForCe with a switch frequency of 20kHz, a directly control can be applied. In this case, those gate pulses have a 7-bit resolution.

b. Compensator

The lamp power will be kept constant. So the lamp voltage V_{la} of about 100 Volt and the lamp current I_{la} must be measured (2 channel A/D converter). A compensator algorithm can be implemented in the microcontroller. A timer is also needed to realize a certain sample time.

c. Measurements

Beside the measurement of the lamp voltage and the lamp current, a special measurement of the ForCe output voltage V_{FORCE} of about 400 Volt must be done (1 additional A/D converter channel). This extra magnitude is needed for the realization of a state machine controller. For more detail see chapter 5.1.

d. Generating a Control Voltage V_c

The current Mode Controller is controlled by a control voltage $V_c=V_{TH+}$ (1 channel D/A converter). The variation of V_{TH+} depends on the compensator algorithm.

e. Current Limiter

The inductor current can not higher than 2 A. If the inductor current exceeds that limit, the inductor of the ForCe will be in saturation. The current will increase sharper (non linear relation), and if this current increase too high it will damage the ForCe. So a maximum current limiter is needed. Also, in normal state the lamp current may not be too low. A minimum limit must be defined, and it is the half of the nominal current. A software limiter can be implemented in the microcontroller. It is clear that V_{TH+} will have a maximum and a minimum. Figure 4.3. depicts a controlled ForCe based on 80C166.

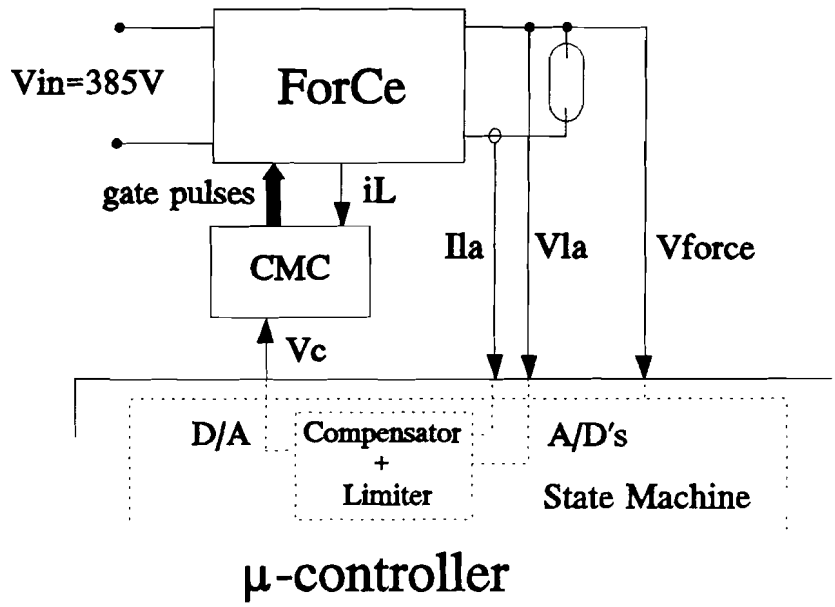


Figure 4.3. A controlled ForCe based on 80C166

4.3.3. Ignitor: Possible Tasks for the µ-controler

a. Gate Pulse

The switching frequency of the ignitor is 200kHz, with duty cycle of 0.1. This pulse can be simply realized by using a PWM channel of the µ-controller. Unfortunately, this PWM has only 3 bit resolution (see 80C166 databook[6]). In the first phase of the ballast development, an additional oscillator is used, because an optimum ignitor must be further investigated.

b. ON-OFF Pulse

ON-OFF pulse is needed to set or reset the ignitor (see chapter 4.6.). If the initialization is completed, the ignitor will set on, and when the ignition has succeeded the ignitor will reset. A capture/compare port (CCP) of the µ-controller can be programmed as a logic pulse (0 or 1), to create an ON-OFF pulse. If the PWM is used to control the gate pulse of the MOSFET, an ON-OFF pulse is not needed.

Figure 4.4. gives two alternatives of a controlled ignitor based on 80C166.

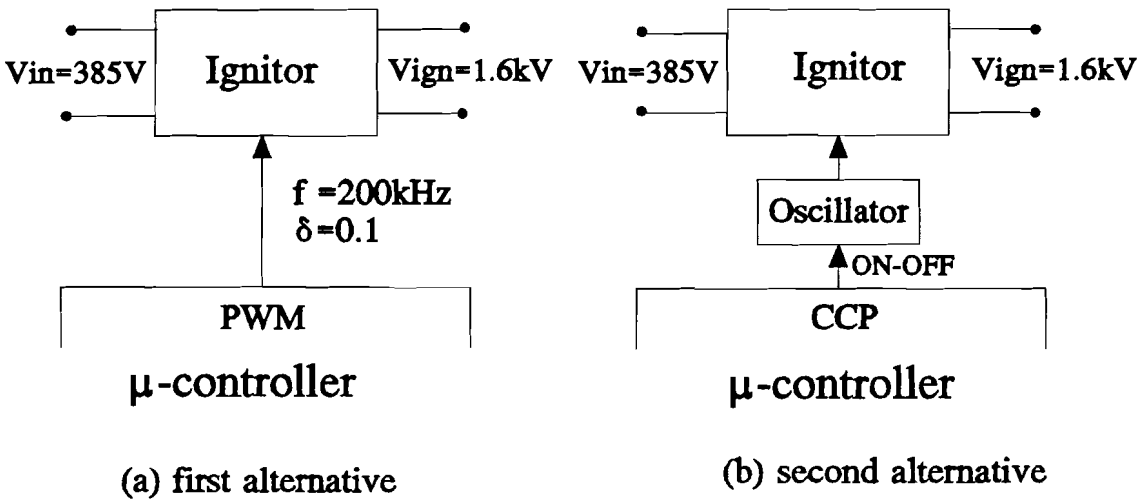


Figure 4.4. A controlled ignitor based on 80C166

According to the preliminary tasks inventory, there are needed:
- 5 channel A/D converters,
- 2 channel D/A converters (PWM+RC-network),
- 1 digital port (capture/compare port),
- 2 timers,

to realize a control circuit for a DC HID lamp ballast.

The available facilities of 80C166 are not fully used (see the 80C166 technical data on page 30). So the function of 80C166 can still be expanded for other purposes, such as for the realization of the communication with the user.

5. REALIZATION OF A CONTROLLED BALLAST BASED ON 80C166 FOR DC HID LAMP

Chapter 3.2. describes a DC HID lamp ballast based on a μ-controller. The realization of this ballast is the subject of this chapter. First, development phases of the ballast control circuit are presented. Here the process of implementing the control algorithm is planned to reach an optimum program development process. Second, the realization of a digital power controller will be explained comprehensively. And last but not least, the experiment results and the agreement between theory and experiment will be discussed.

5.1. DEVELOPMENT PHASES

As mentioned in chapter 3.2., to feed the lamp correctly, there are three important states to be crossed. Those are initialization, ignition, and power regulation. In the first development phase, those state programs will be built separately as blocks. In the second development phase these blocks will be integrated as a complete control program. This integration is made by using a state machine method.

Development phase I: DPI

Those state programs are implemented in FORTH (see appendix F). The flow chart of those states is given in figure 5.1. up to 5.3.

a. Initialization (figure 5.1.)

First V_{TH+} must be set to the nominal value. The lamp is READY to ignite, if the output voltage of the preconditioner V_{in}=385V and if the output of the ForCe V_{FORCE}=385V.

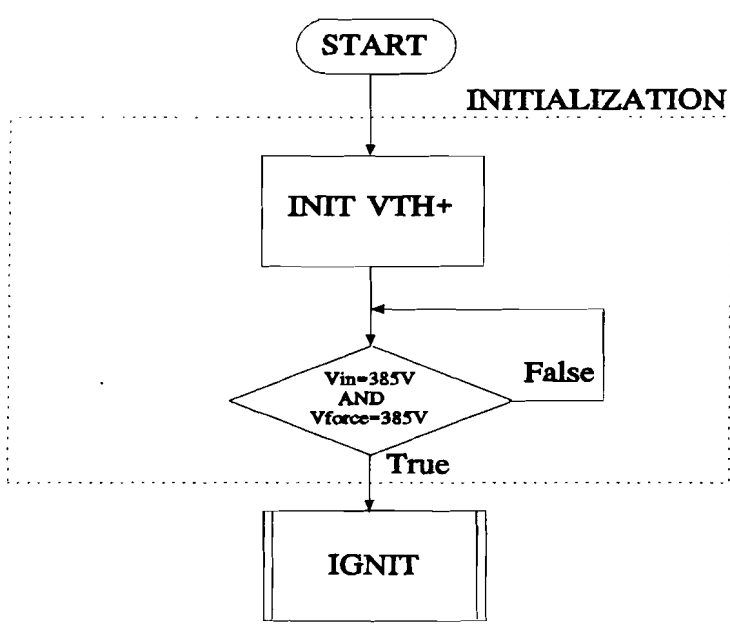


Figure 5.1. Initialization flow diagram

b. Ignition (Figure 5.2.)

When the initialization is completed, the ignitor will set on. The ignition will end if the V_{FORCE} becomes 100 Volt (that means the lamp is ignited successfully) or if the maximum ignition time T_{ign} is reached. If the lamp is not ignited until T_{ign} is TRUE, then the ballast will wait for T_{wait} seconds. After T_{wait} the ignition will be run again. If the number of ignition efforts is equal to the maximum number N_{max}, the ignition will be canceled. Probably the lamp is defect.

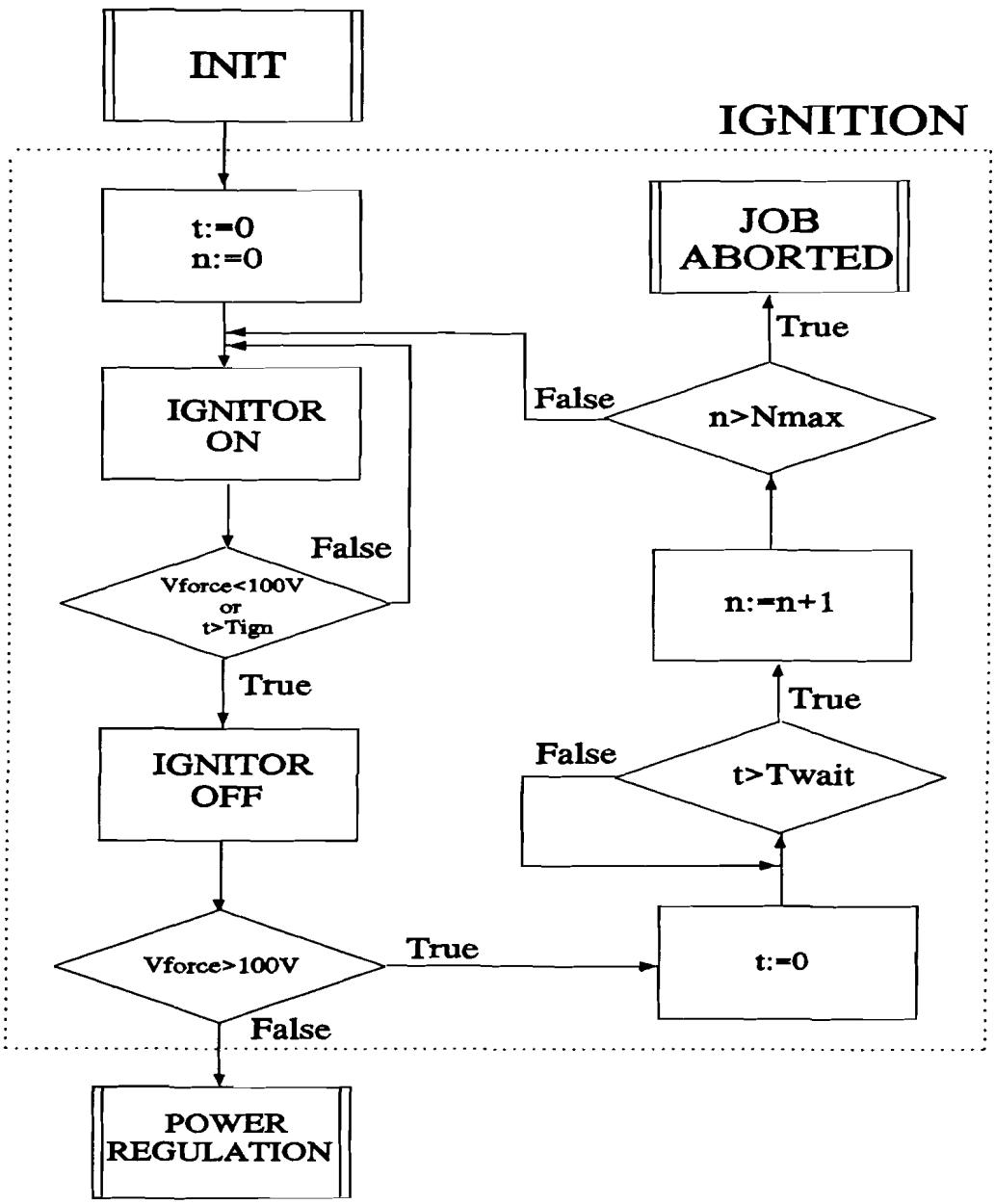


Figure 5.2. Ignition flow diagram

c. Power regulation (figure 5.3.)

If the ignition is successful, the power regulator will be active. The lamp current and the lamp voltage will be measured. According to the control algorithm, the lamp power will be kept constant at the nominal level (32 Watt).

The lamp can be switched off by entering $V_{TH+}=0$.

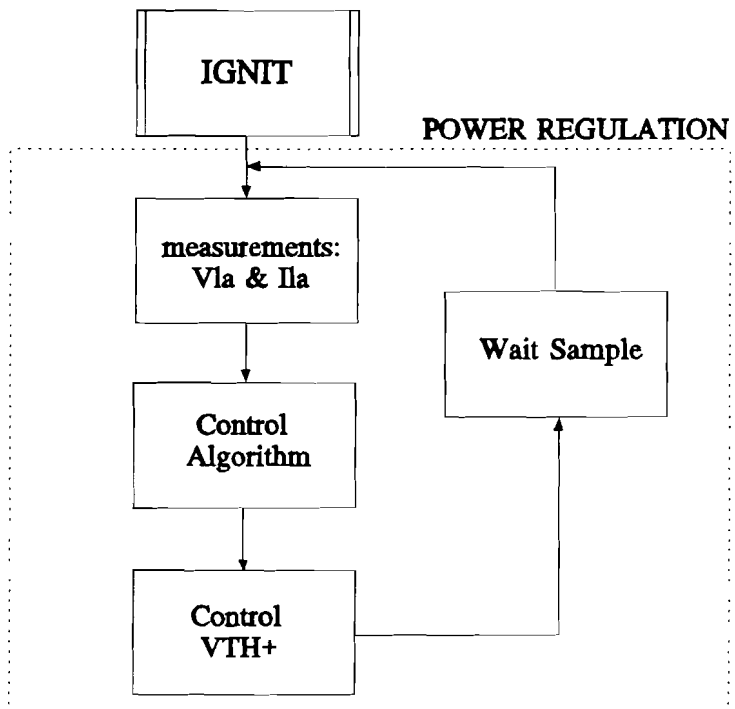


Figure 5.3. Power regulation flow diagram

Development Phase II: DPII

We can integrate those blocks from DPI with IF THEN ELSE statements. But this method is not so elegant. The STATE MACHINE method compared to the IF THEN ELSE method has two advantages. First, the STATE MACHINE method is better organized, so every modification is relatively simple to be done. Second by using the STATE MACHINE method, the program tends to be shorter.

In this DPII, we will use STATE MACHINE to build the complete automatic control program. This state machine is divided in to 4 states:

a. INIT = Initialization,
b. IGNIT = Ignition,
c. CONTR = Power regulation,
d. MESS = Messages.

There are at least two parameters needed to characterize a state. Those very logical choices are V_{la} and I_{la}. For a practical reason (see appendix F), V_{FORCE} is introduced to take over the job of V_{la} in the STATE MACHINE. For the symmetry we will call I_{la} as I_{FORCE}. So every state changing will be characterized by V_{FORCE} and I_{FORCE}.

The range of V_{FORCE} is from 0 to 385V. When V_{FORCE}=385V (ForCe is in open circuit), the ballast is initialized. Then the ignition is active. If V_{FORCE}=15V (ForCe is in short circuit), the lamp is ignited. After that, the lamp voltage will rise, until the lamp voltage V_{FORCE} becomes about 100V. Now the lamp is in its normal state. The lamp power will be kept constant (power regulation). Based on those states, V_{FORCE} can be encoded into three sub-states. These sub-states are symbolized with integers, see Table 5.1. Of course these choices are a little bit FUZZY.

Table 5.1. Sub-states of V_{FORCE}

Range of V_{FORCE}	**Sub-state**
$0V<V_{FORCE}<100V$	0
$100V<V_{FORCE}<385V$	1
$V_{FORCE}>385V$	2

Also I_{FORCE}, there are sub-states too. See Table 5.2.

Table 5.2. Sub-states of I_{FORCE}

Range of I_{FORCE}	**Sub-state**
$0<I_{FORCE}<160mA$	0
$I_{FORCE}>160mA$	1

It is clear that the variation of those sub-states of V_{FORCE} and I_{FORCE}, will cause a progression from one state to another state. Figure 5.4. shows the STATE MACHINE flow chart, where the bit sequence is (V_{FORCE},I_{FORCE}).

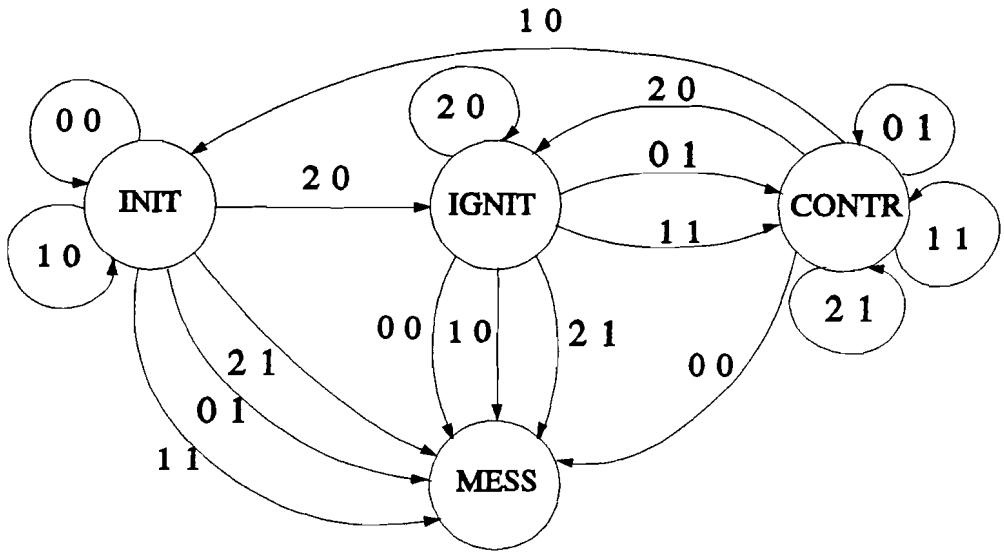


Figure 5.4. State Machine

The state begins with INIT. If V_{FORCE}=2 and I_{FORCE}=0, it means the initialization is completed, then the new state becomes IGNIT. So the ignitor is set on. If V_{FORCE}=1 and I_{FORCE}=1 (the lamp is ignited), the new state becomes CONTR. Here the power regulation is active.

The above procedure path is the right method to feed and control the DC HID lamp. If the ballast system deviates from this procedure, there is something wrong happen. Serious deviation will cause cancellation in the whole ballast system (the state will fall in MESS). The microcontroller will give a message to the user what is wrong in the system. In this way, the control circuit will also have some intelligence. For more detail see in appendix F (implementation of the state machine).

5.2. DIGITALIZATION OF THE POWER CONTROLLER

Chapter 2.2.2. gives a power control strategy for the 32 Watt DC HID lamp. This control algorithm will be implemented in the 80C166 μ-controller. Digitalization is thus necessary.

According to the system identification, an integrator is enough to control the lamp power. The time constant of the integrator depends on the whole feedback system characteristic. Of course the choice of this time constant must guarantee the stability of the feedback system.

5.2.1. Digitalization of Integrator

According to figure 2.4. the power error [e(t)] is the input of the integrator. The output of the integrator is [i(t)]. We can write this relation as,

$$[i(t)] = \frac{1}{T_i} \int_{t_0}^{t} [e(\tau)]\, d\tau \ , \tag{5.1}$$

T_i is the integrator time constant. Differentiation of [i(t)] gives,

$$\frac{d[i(t)]}{dt} = \frac{[e(t)]}{T_i} \ . \tag{5.2}$$

Digitalization is done by approximation of d[i(t)]/dt,

$$\frac{d[i(t)]}{dt} = \frac{[i(t)] - [i(t-T_{sample})]}{T_{sample}} \ , \tag{5.3}$$

where T_{sample} is the sample time. So we can write formula 5.3 as,

$$[i(t)] = \frac{T_{sample}}{T_i} [e(t)] + [i(t-T_{sample})] \ . \tag{5.4}$$

With $t/T_{sample}=n$ the sample number and $T_{sample}/T_i=KINT$ the integrator constant, the digitalization is completed,

$$[i(n)] = KINT*[e(n)] + [i(n-1)] \ . \tag{5.5}$$

A much simpler notation,

$$i[n] = KINT*e[n] + i[n-1] \ . \tag{5.6}$$

So the changing in the small signal current i[n] is equal to the changing in the error e[n] multiplied with an integrator constant KINT, plus the old current i[n-1]. If the error e[n] is equal to zero, i[n]=i[n-1].

5.2.2. Low Pass Filter for D/A Converter Application

As mentioned in chapter 4.1. a D/A converter can be built from a PWM channel of the 80C166, by using a low pass filter (for instance a simple RC-network).

According to the 80C166 data book[6], the maximum accuracy of the PWM is 16-bit, with a counter time unit 400ns.

The principle of the PWM is as follows (see figure 5.5.): a sawtooth wave is compared with a control value CV from a register. The duty cycle of PWM depends on this control value. The resolution of the sawtooth is variable with a relative value T0REL.

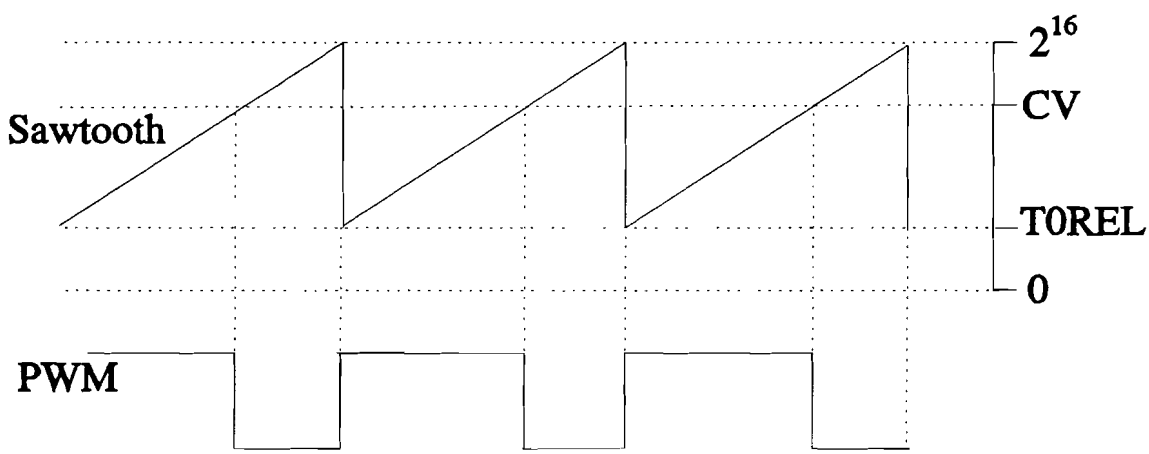


Figure 5.5. The principle of Pulse Width Modulation (PWM)

The content of T0REL must be 0 for a 16-bit PWM resolution. According to this boundary, the sawtooth frequency f_{16} will be $((2^{16}-1)*400ns)^{-1} \approx 40Hz$. A large RC time constant (low pass filter) is needed, to realize a D/A converter with a 16-bit accuracy.

A resolution of 10-bit is chosen for the ballast application. The only reason for this choice is that the A/D converter is also 10-bit. In this case, the frequency of the PWM is $f_{10}=((2^{10}-1)*400ns)^{-1} \approx 2.4kHz$. The content of T0REL must be $(2^{16}-2^{10})$, 10-bit. And the range of the control value will be, $(2^{16}-2^{10}) \leq CV \leq 2^{16}$. The RC time constant of the LPF must be greater than $2^{10}/(\pi f_{10}) \approx 0.13$ s, to maintain the 10-bit resolution (the relative ripple of the LPF output is smaller than 2^{-11}). R=200 kOhm and C=680nF are chosen for the RC network. This RC-filter will cause delay in the control algorithm, and it will also fix the choice of the integrator time constant T_i.

5.2.3. Complete Schematic of Power Controller Realization

Figure 5.6. gives the complete schematic of the power control system.

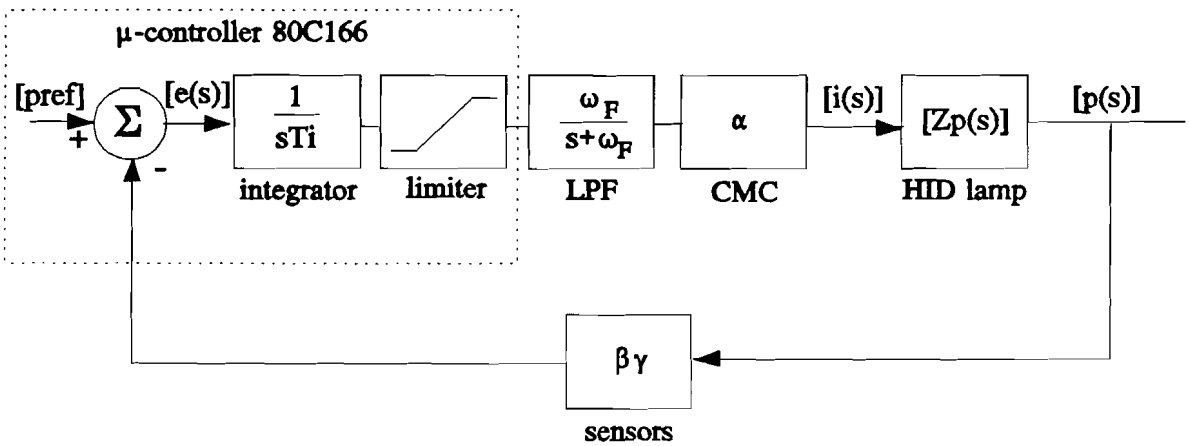


Figure 5.6. The realization of the power controller diagram

The output of the integrator is related to the control value CV, which determines the duty cycle of the PWM. After filtering (LPF) of the PWM signal, the small signal current [i(s)] results. As long as the output of the integrator is not saturated ($[i(s)]_{max}$ or $[i(s)]_{min}$ of the limiter) the feedback system is linear.

α = the gain of the CMC,
β = the gain of the lamp current sensor,
γ = the gain of the lamp voltage sensor.

In ideal case, α,β, and γ are unity. If α,β, and γ are not unity, the optimum integrator time constant depends on α,β, and γ, and in steady state $P_{la}(t\rightarrow\infty)=P_{ref}/(\beta\gamma)$.

Feedback transfer functions

Assumed the feedback system is linear and $\alpha,\beta,\gamma \neq 1$. There are three important transfer functions. The first transfer function gives how the lamp power changes with the power reference variation,

$$\frac{[p(s)]}{[p_{ref}]} = \frac{1/\beta\gamma}{\frac{T_i}{\alpha\beta\gamma\ \omega_F\ [Z_p(s)]}\ s^2 + \frac{T_i}{\alpha\beta\gamma\ [Z_p(s)]}\ s + 1} \quad . \tag{5.7}$$

The second transfer function describes how the lamp current is controlled by changes the power reference,

$$\frac{[i(s)]}{[p_{ref}]} = \frac{1}{[Z_p(s)]\ (\frac{T_i}{\alpha\beta\gamma\ \omega_F\ [Z_p(s)]}\ s^2 + \frac{T_i}{\alpha\beta\gamma\ [Z_p(s)]}\ s + 1)} \quad . \tag{5.8}$$

And the last transfer function illustrates how the lamp voltage behaves by a variation in the power reference,

$$\frac{[v(s)]}{[p_{ref}]} = \frac{[Z_l(s)]}{[Z_p(s)]} \frac{1}{(\frac{T_i}{\alpha\beta\gamma\ \omega_F\ [Z_p(s)]}\ s^2 + \frac{T_i}{\alpha\beta\gamma\ [Z_p(s)]}\ s + 1)} \quad . \tag{5.9}$$

Stability and Performance

Assumed that the sample frequency f_{sample} is much larger than the bandwidth of the feedback system. Z-transformation is then not necessary. We can still use s-domain transfer functions to analyze the stability of the system.

We know for the 32 Watt DC HID lamp the approximation $[Z_p(s)] \approx [Z_0] = 1$ is valid. In this case, the power control system has the characteristic polynomial,

$$\frac{T_i}{\alpha\beta\gamma\ \omega_F}\ s^2 + \frac{T_i}{\alpha\beta\gamma}\ s + 1 \quad . \tag{5.10}$$

A second order system is stable, if all roots of the characteristic polynomial lie in the left half of the complex plane (LHP). And a second order polynomial has all roots in the left half of the complex plane (LHP) if and only if all polynomial coefficients have the same algebraic sign. This condition is valid for the power control characteristic polynomial in formula 5.10. The polynomial has two LHP roots,

$$s_{1,2} = -\frac{\omega_F}{2}\ (1 \pm \sqrt{1 - \frac{4\ \alpha\beta\gamma}{\omega_F\ T_i}}) \quad . \tag{5.11}$$

Optimum integration time constant

The first transfer function (formula 5.7) is equal to the second transfer function (formula 5.8), when the approximation $[Z_p(s)]=1$ is applied. This transfer function is a second-order system. The bandwidth of this transfer function depends on the choice of the integrator time constant. This transfer function can also be written as,

$$[T(s)] = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \qquad (5.12)$$

The natural frequency $\omega_n=(\alpha\beta\gamma\omega_F/T_i)^{1/2}$, and the damping ratio $\zeta=1/2(\omega_F T_i/\alpha\beta\gamma)^{1/2}$. Assumed $\alpha\beta\gamma=1$, the feedback system is optimum when $\zeta=0.707$ (where the poles of the feedback system are complex). The step response of this transfer function will have a fast settling time and a small overshoot, see figure 5.7. In this case, the optimum integrator time constant will be equal to,

$$T_i = \frac{2\ \alpha\beta\gamma}{\omega_F} \qquad (5.13)$$

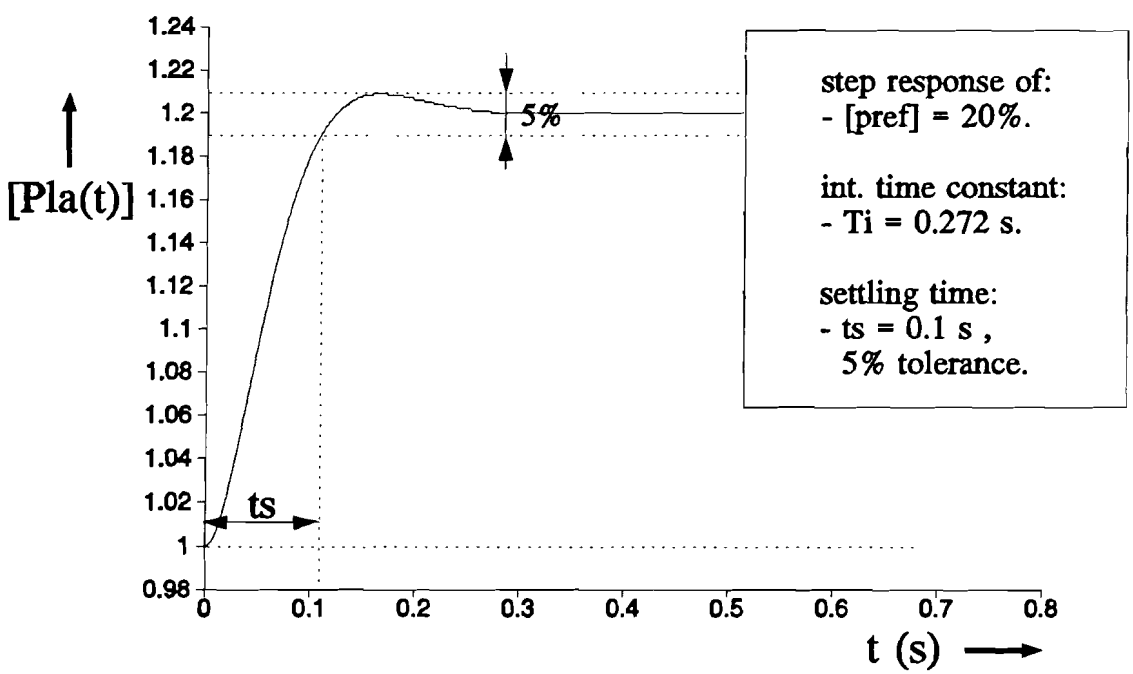


Figure 5.7. Optimum integrator time constant

Implementation in FORTH

The power control algorithm is implemented in FORTH. The diagram of the implementation is given in figure 5.8.

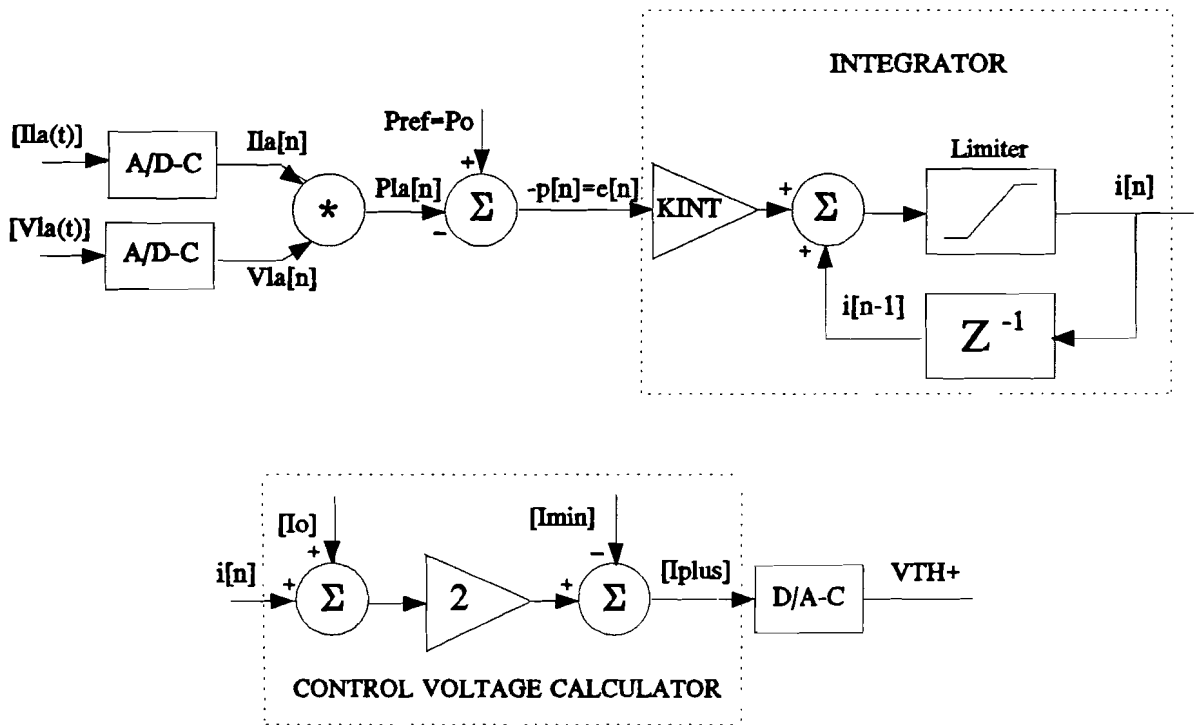


Figure 5.8. Implementation diagram of the power controller

The limiter is implemented internally in the integrator. This limiter has two functions:

a. to prevent the ForCe from overcurrent, when the inductor is saturated,
b. to avoid WIND-UP, when the power error e[n] becomes very large.

The control voltage calculator (+ D/A-converter) converts the variation of i[n] in V_{TH+}. This V_{TH+} is proportional with I_{plus}. The ForCe will convert this control voltage into i(t). The voltage control calculator is the inverse of the ForCe: $I_{la}(t)=½(I_{plus}+I_{min})$.

5.3. RESULT: POWER MEASUREMENT

Some measurements are done to check the validity of the theory (for more experiment results see appendix G). Figure 5.9. gives a comparation between experiment result and theory, by a step excitation in [pref]=44%. In this experiment the sample time T_{sample} is 1 ms, and the integrator time constant T_i=0.272 s. From the experiment, $\alpha\beta\gamma$=0.90 and $\beta\gamma$=1.05 are found, so the CMC gain factor becomes α=0.86 (see figure 5.6).

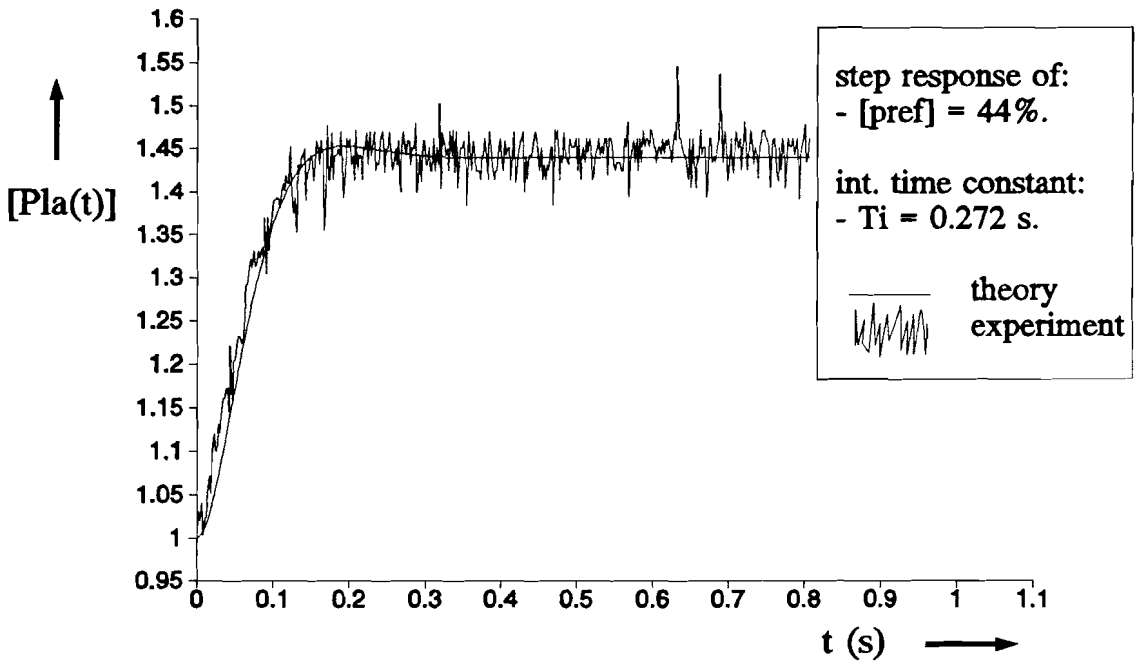


Figure 5.9. Comparison between theoretical and experimental power step response by an optimum integration time constant.

The experimental result shows a good agreement with the theory. The linearization and the approximation $[Z_p(s)]$=1, are good tools for design an optimum lamp power regulation. The system is not noise free. The model does not take this noise into account. But anyway, the integrator will always try to keep the power error equal to zero. The accuracy of the power controller will be limited by the noise level.

The power control is directly based on the relation $P_{la}=V_{la}*I_{la}$. This power controller differs from the conventional power control expression, $S = V_{la}+\beta_p I_{la}$, where S is a constant. In the conventional power controller, the lamp power is not really kept constant, but the lamp voltage plus an amount of the lamp current (β_p is typically 0.2). The integrator is also used in the conventional way, but relatively slow.

The new power controller can still be improved. The pole in the feedback system, caused by the LPF, can be canceled by using a PI-controller. The zero of this PI-controller should cancel the pole of the LPF. In this way a very fast integrator can be applied (by approximation the system becomes first order).

6. CONCLUSION AND RECOMMENDATION

Conclusion

A 80C166-based controlled ballast for a DC HID lamp is designed and realized. The ballast consists of: preconditioner (in this research, it is a power supply, 400Volt), down converter (ForCe), ignitor, control circuit (μ-controller), and a 32Watt DC HID lamp. A standard procedure of the ballast operation is as following (divided into 3 states):

1. Initialization,
2. Ignition, and
3. Power regulation.

These states are implemented in FORTH, as blocks. A ballast control circuit, based on this program, is tested. The lamp is fed correctly, and the lamp power is kept constant at 32 Watt.

A 200kHz/32Watt ForCe is designed and tested. It has an efficiency of 95%. ForCe operates according to Zero-Voltage-Switch Quasi-Square wave-Converter (ZVS-QSC) technique[4].

The 80C166 card can not control the ForCe directly. An interface between the ForCe and the 80C166 is needed, to create a feedback system. This interface is called current mode controller (CMC). This CMC has a control voltage input. The output current of the ForCe is proportional with this control voltage. ForCe + CMC results in a current source, which is able to operate in open circuit, short circuit, and normal state (feed the lamp).

The type of the controller is a power controller. A system identification is needed, to derive an optimum control strategy. Here the small-signal impedance $Z_l(s)$ of a 32 Watt DC HID lamp is determined. This v-i characteristic of the DC HID lamp is a non minimum phase system and it is not linear. The $Z_l(s)$ can be described as a sum of two first-order impedances ($Z_{l1}(s)$ and $Z_{l2}(s)$). The time constant of the first impedance τ_{p1} is about 10s, the second time constant τ_{p2} is smaller than 1ms, and $|Z_l(s)| \ll Z_0$.

The small signal p-i characteristic is found by linearization of the power $P_{la}(t)=V_{la}(t)*I_{la}(t)$ at the nominal point. By approximation, p(t) depends only on i(t), not on v(t). The consequence of this assumption: a integrator is enough to create a fast power control system. The time constant of this integrator is limited by the time constant of the D/A converter of the microcontroller. The optimum integrator time constant is about 0.3s.

By a 5% accuracy, the settling time of the power control system is about 0.1 s. A control system model is developed and compared with experiment results. Those measurement results show a good agreement with the theory.

Recommendation

A STATE MACHINE method is introduced to create an automatic and intelligent control system (development phase II). An alternative integrated program is implemented in FORTH. More research and development in this STATE MACHINE solution is recommended.

More study on the ignition state is needed. This state is the most critical phase in the ballast system. The system behavior during this state is also important for the design of the STATE MACHINE controller.

The power regulation has no trouble with the non minimum phase v-i characteristic of the DC HID lamp. Supposed one tried to control the lamp voltage, the voltage controller must take this NMP behavior into account. Beside the v-i characteristic of the 32 Watt DC lamp is not linear. A self-tuning controller, based on zero-pole cancellation is a solution of this problem. This option is very interesting.

The accuracy of the power controller is limited by noise level. A research for minimizing of the noise influence is necessary.

A single chip microcontroller can directly control the ballast (ForCe), if the applied switch operates at about 20kHz (7-bit resolution). A disadvantage of this solution is that the volume of the ForCe becomes larger, however the volume of the control circuit will be reduced. A research of this possibility positively will open better insight. As the µ-controller increases in speed this feature can be realized. The core volume will then not increase, but the CMC can be omitted.

During the research the preconditioner is a power supply 400 Volt. In the next development phase a controlled boost converter, based on the µ-controller can be applied as the preconditioner.

Those available facilities of 80C166 are not fully used (see the 80C166 technical data on page 30). So the function of 80C166 can still be expanded for other purposes, such as for the realization of the communication with the user.

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APPENDIX A. SYSTEM IDENTIFICATION

A.1. THEORY: MINIMUM VARIANCE SQUARED METHOD

Assumed the small signal impedance of the HID lamp is as given in formula 2.2. By a step excitation in the current $i(t)=i_{step}$, the small voltage variation, theoretically, will be:

$$v(t) = i_{step}\left[Z_{l1}(1-e^{-\frac{t}{\tau_{p1}}}) + Z_{l2}(1-e^{-\frac{t}{\tau_{p2}}})\right]. \qquad \textbf{(A.1)}$$

$v(t)$ is normalized with i_{step} and sampled at t_i resulting in $v^*(t_i)$:

$$v^*(t_i) = \frac{v(t_i)}{i_{step}} = \left[Z_{l1}(1-e^{-\frac{t_i}{\tau_{p1}}}) + Z_{l2}(1-e^{-\frac{t_i}{\tau_{p2}}})\right]. \qquad \textbf{(A.2)}$$

The normalized and measured voltage is $v^*_{exp}[i]$, where $i=t_i/t_{sample}$.

The minimum variance squared method is defined by,

$$S = \sum_{i=1}^{N} \left(v^*(t_i) - v^*_{exp}[i] \right)^2 . \qquad \textbf{(A.3)}$$

S must be minimum, to have a good approximation of $v^*(t) \approx v_{exp}(t)$. So in other words,

$$\frac{\partial S}{\partial Z_{lk}} = 0 \text{ and } \frac{\partial S}{\partial \tau_{pk}} = 0. \qquad \textbf{(A.4)}$$
$$k = 1,2 .$$

Formula A.4 gives 4 equations with 4 unknown parameters. These equations are non linear, and it is very hard to solve them. Another approach: we can choose $\partial S/\partial Z_{lk}=0$ for $k=1,2$ and let $\partial S/\partial \tau_{pk}$ smaller than 10^{-3} for $k=1,2$. In this alternative those τ_{pk}'s are estimated. From this boundary a matrix of 2x2 results with two unknown parameters Z_{lk}'s. The two equations are derived from:

$$\frac{\partial S}{\partial Z_{lk}} = \sum_{i=1}^{N} 2\left(v^*(t_i) - v^*_{exp}[i] \right)\left(1-e^{-\frac{t_i}{\tau_{pk}}}\right) = 0 . \qquad \textbf{(A.5)}$$
$$k = 1,2 .$$

Formula (A.5) gives:

$$\begin{aligned} A\ Z_{l1} + B\ Z_{l2} &= C \\ D\ Z_{l1} + E\ Z_{l2} &= F \end{aligned} \qquad \textbf{(A.6)}$$

A,B,C,D,E, en F are a function of τ_{p1}, τ_{p2}, and $v_{exp}[i]$'s. Now those Z_{lk}'s can be solved.

The accuracy indicators are:

$$\frac{\partial S}{\partial \tau_{pk}} = \sum_{n=1}^{N} -2(\ v*_t(t_i) - v*_e[i]\ )\ Z_{lk}\ \frac{t_i}{\tau_{pk}^2}\ e^{-\frac{t_i}{\tau_{pk}}} < 10^{-3}\ . \qquad \textbf{(A.6)}$$

$$k = 1,2\ .$$

The implementation of this method is given in the next section.

A.2. PASCAL PROGRAM

```
Program MVSM (Input,Output); { minimum variance squared method }

%include '/userdef/hendrix/units/header.pas';

var t, dt , t1, t2, Zl1, Zl2, Sigma1, Sigma2, dc, M, negscale, posscale, dummy: real;
    i, N, Ndc : integer;
    u: array [1 .. 1025] of real;
    data: text;

%include '/userdef/hendrix/units/agoodies.pas';

(* ------------------- *)
Procedure ReadData;

begin
readln(data,dt,N,Ndc);
  For i:=0 to (N-1) do
    begin
      readln(data,u[i]);
    end;
end;
(* ------------------- *)
Procedure Middeldc;

begin
i:=0; M:=0;
  While i<=Ndc do
  begin
    M:=u[i]+M;
    i:=i+1;
  end;
dc:=M/(Ndc+1);
end;
```

```
(* ---------------------- *)
Function HID(var ts,Zl1,Zl2,t1,t2 :real): real;

begin
   HID:=Zl1*(1-exp(-ts/t1))+Zl2*(1-exp(-ts/t2));
end;
(* ---------------------- *)
Procedure PlotFunc1;

var i: integer; ts,Z1,Z2: real;

begin
  Trace[1].Xoffs:=0;       Trace[1].Yoffs:=negscale;
  Trace[1].Xdiff:=40;  Trace[1].Ydiff:=posscale;
  Trace[2].Xoffs:=0;     Trace[2].Yoffs:=negscale;
  Trace[2].Xdiff:=40;  Trace[2].Ydiff:=posscale;
  GraphOutput('samples =>','Resp =>',Black,White);
  Wmove1(0,0); Wmove2(0,0);{Wmove3(0,0)};
  for i:=0 TO (N-1) DO Wplot1(i*dt,(u[i]-dc)*150);
  for i:=0 to Ndc-1 do Wplot2(i*dt,0);
  for i:=Ndc to (N-1) do
    begin
      ts:=dt*(i-Ndc);
      Wplot2(ts+(Ndc*dt),HID(ts,Zl1,Zl2,t1,t2));
    end;
end;
(* ---------------------- *)
Procedure ImpedanceCalculator;

{see Erwin Kreyzig page 395}

var s1, s2, e11, e12, e21, e22, DET: real;
    i: integer;

begin
i:=0;s1:=0;s2:=0;e11:=0;e22:=0;e12:=0;e21:=0;
While i+Ndc<=N do
  begin
    t:=dt*i;
    s1:=(u[i+Ndc]-dc)*(1-exp(-t/t1))+s1;
    s2:=(u[i+Ndc]-dc)*(1-exp(-t/t2))+s2;
    e11:=(1-exp(-t/t1))*(1-exp(-t/t1))+e11;
    e12:=(1-exp(-t/t1))*(1-exp(-t/t2))+e12;
    e21:=(1-exp(-t/t2))*(1-exp(-t/t1))+e21;
    e22:=(1-exp(-t/t2))*(1-exp(-t/t2))+e22;
    i:=i+1;
   end;

DET:=(e11*e22-e12*e21);
Zl1:=(s1*e22-s2*e12)*150/DET;
Zl2:=(s2*e11-s1*e21)*150/DET;
writeln('DET= ',DET);
writeln('e11*e22= ',e11*e22);
writeln('e12*e21= ',e12*e21);
end;
(* ---------------------- *)
```

```
(* ------------------------ *)
Procedure Accuracy (var Zl1, Zl2: real);

var st1, st2, et11, et12, et21, et22: real;
    i: integer ;

begin
i:=0;st1:=0;st2:=0;et11:=0;et12:=0;et21:=0;et22:=0;
while i+Ndc<=N do
  begin
    t:=dt*i;
    st1:=Zl1*(u[i+Ndc]-dc)*exp(-t/t1)*t/sqr(t1)*150+st1;
    st2:=Zl2*(u[i+Ndc]-dc)*exp(-t/t2)*t/sqr(t2)*150+st2;
    et11:=sqr(Zl1)*(1-exp(-t/t1))*exp(-t/t1)*t/sqr(t1)+et11;
    et22:=sqr(Zl2)*(1-exp(-t/t2))*exp(-t/t2)*t/sqr(t2)+et22;
    et12:=Zl1*Zl2*(1-exp(-t/t2))*exp(-t/t1)*t/sqr(t1)+et12;
    et21:=Zl1*Zl2*(1-exp(-t/t1))*exp(-t/t2)*t/sqr(t2)+et21;
    i:=i+1;
  end;
Sigma1:=-2*(st1-et11-et12);
Sigma2:=-2*(st2-et21-et22);

end;
(* ------------------------ *)
Procedure Showresults;

begin
writeln('t1 = ',t1:3:3);
writeln('t2 = ',t2:3:3);
writeln('Z1 = ',Zl1:3:3);
writeln('Z2 = ',Zl2:3:3);
writeln('S1 = ',Sigma1);
writeln('S2 = ',Sigma2);
writeln('dc = ',(dc*150):3:3);
readln;
negscale:=-1; posscale:=3;
InitGraphicsOutput;
repeat
  Plotfunc1;
  write('OldNegscale: ',negscale:2:1,'. Oldposscale : ',posscale:2:1,'. Type (1) 0 (not) to change the Y-scale: ');

  readln(dummy);
  If dummy=0 then
     begin
       write(' Type negscale and posscale: ');
       readln(negscale,posscale);
     end;
until dummy=1;
RestoreCrtMode;
end;
(* ------------------------ *)
```

```
(* ------------------------- *)
{MAIN}

BEGIN
writeln;
writeln('  ************************************************************');
writeln('  * This Program calculate the impedance of a DC HID lamp    *');
writeln('  * according to a 2-order model, with one zero in RHP        *');
writeln('  * and two stable poles. Here is assumed that t1 and t2      *');
writeln('  * are known.                                                *');
writeln('  * Measurement must be specified in a file, call *.txt.      *');
writeln('  *                                                          *');
writeln('  *            written by: Rizqa Defiora                     *');
writeln('  *                                                          *');
writeln('  ************************************************************');
writeln;


Assign(data,paramstr(1));
Reset(data);
ReadData;
Close(data);

Middeldc;

REPEAT

write('Type t1 and t2 in seconds: ');
read(t1,t2);

ImpedanceCalculator;

Accuracy(Zl1 ,Zl2);

Showresults;

UNTIL FALSE

END.
```

A.3. MEASUREMENT RESULTS

Tabel A.1.

$i(0^-)$ (mA)	$i(0^+)$ (mA)	Z_{11} (Ohm)	Z_{12} (Ohm)	τ_{p1} (s)	τ_{p2} (s)
300	340	28.675	-20.125	10.502	<0.001
340	300	33.625	-25.175	12.150	<0.001
300	360	26.433	-18.717	5.574	<0.001
360	300	29.550	-17.200	10.580	<0.001
300	390	24.044	-14.911	5.705	<0.001
390	300	22.733	-18.622	11.485	<0.001
320	350	37.400	-21.233	6.150	<0.001
350	320	48.500	-32.600	8.331	<0.001
320	380	19.833	-11.800	5.431	<0.001
380	320	23.250	-16.850	8.165	<0.001
320	420	19.830	-12.960	4.783	<0.001
420	320	21.410	-15.520	9.327	<0.001
280	310	34.667	-25.133	10.880	<0.001
310	280	48.733	-42.433	9.425	<0.001
260	320	36.333	-26.95	8.723	<0.001

APPENDIX B. DESIGN OF THE ForCe INDUCTOR L

The calculation of the inductor value is based on the semi resonant snubber. Energy balance says:

$$\frac{1}{2}LI_{min}^{2} \geq \frac{1}{2}C_{par}V_{in}^{2} \qquad \textbf{(B.1)}$$

The minimum inductive energy is chosen for the design of the inductor L. The equality sign is valid in formula B.1. If the inductive energy is greater than the capacitive energy, the diode of the main MOSFET D1 will be on. It means, an amount of the inductive energy goes to the mains, and ZVS is still valid. Assuming that after switch off of the main MOSFET the inductor current decreases linearly (first order approximation) according to,

$$i_L = I_{plus} - \frac{\delta V_{in}}{L}t \qquad \textbf{(B.2)}$$

until i_L is equal to I_{min} at $t=(1-\delta)T_s$. The value of L can be calculated as:

$$L = \frac{\delta(1-\delta)V_{in}T_s}{2(I_{out}-I_{min})} \qquad \textbf{(B.3)}$$

Where I_{out} is the DC current across the resistor:

$$I_{out} = \frac{I_{plus}+I_{min}}{2} \qquad \textbf{(B.4)}$$

Combination of B.2 and B.3, gives the value of I_{min}:

$$I_{min} = -I_{par}\left[1 + \sqrt{1 + 2\left(\frac{I_{out}}{I_{par}}\right)}\right] \qquad \textbf{(B.5)}$$

$$I_{par} = \frac{C_{par}V_{in}}{\delta(1-\delta)T_s}$$

C_{par}, V_{in}, δ, en T_s are known, so I_{min} can be calculated. Because now I_{min} is known, then the value of L and I_{plus} can be calculated too.

APPENDIX C. DESIGN OF OUTPUT ForCe CAPACITANCE C

C.1. ForCe = SWITCHES + FILTER

Assumed the switches are ideal. Then the voltage over the second MOSFET is a block signal. The rest of the circuit can be written as a second order system, see figure 4.7. The next relation is valid (Laplace):

$$\frac{V_{in}(s)}{V_{out}(s)} = \frac{\frac{1}{LC}}{s^2 + \frac{s}{RC} + \frac{1}{LC}} \qquad \text{(C.1)}$$

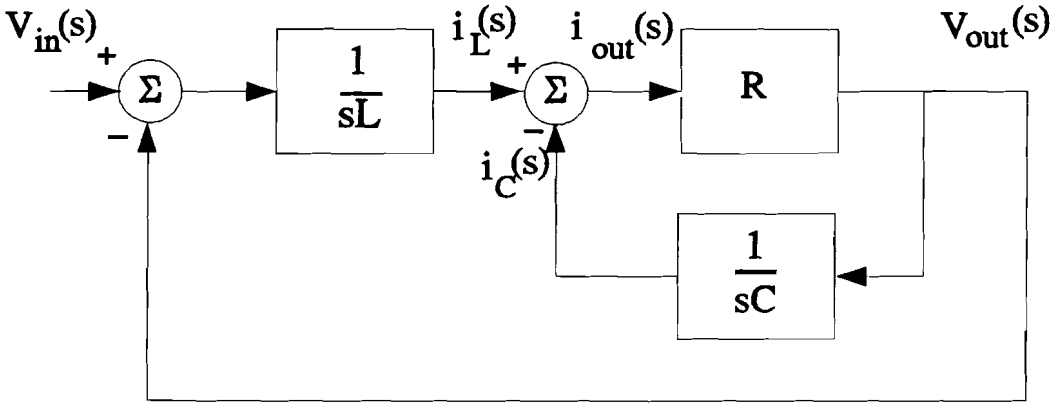


Figure 4.7. The block scheme of the filter part of ForCe

The ForCe is now described as a feedback system. There are two integrators. The first integrator integrates the error of $V_{in}(t)$-$V_{out}(t)$/L which results in the inductor current $i_L(t)$. After this the inductor current $i_L(t)$ will be filtered by a first other filter with time constant RC, multiplied with R which results in $V_{out}(t)$. The feedback system tries to control the error $V_{in}(t)$-$V_{out}(t)$ equal to zero. Therefore $V_{out}(t)$ will follow the DC-component of the block signal $V_{in}(t)$.

The second integrator lies in an intern loop. This intern feedback will pass the DC-component of the inductor current $i_L(t)$, results $i_{out}(t)$, and filtered AC components of $i_L(t)$. So that the capacitor current $i_C(t)$ is almost equal to the ripple of the inductor current $i_L(t)$.

C.2. OUTPUT CAPACITANCE

Assumed, $\tau 1$ and $\tau 2$ are very much smaller dan δT_s and $(1-\delta)T_s$ (the reactance of C_{par} is very much larger than the reactance of R-L-C filter). So the input Voltage of the Filter is a block signal with Fourier series:

$$V_{in}(t) = \delta V_{in} + V_{in} \sum_{n=1}^{\infty} c_n \sin\left(\frac{2n\pi t}{T_s} + \varphi_n\right) . \qquad \text{(C.2)}$$

Where

$$c_n = \sqrt{a_n^2 + b_n^2} , \qquad \text{(C.3)}$$

$$\varphi_n = \arctan\left(\frac{b_n}{a_n}\right) , \qquad \text{(C.4)}$$

$$\begin{aligned} a_n &= \frac{\sin(2n\pi\delta)}{n\pi} , \\ b_n &= \frac{(\,1 - \cos(2n\pi\delta)\,)}{n\pi} . \end{aligned} \qquad \text{(C.5)}$$

The second order (RLC) filter is:

$$F(j\omega) = \frac{\omega_{nat}^2}{\omega_{nat}^2 - \omega^2 + 2\,j\zeta\omega_{nat}\omega} . \qquad \text{(C.6)}$$

Where

$$\begin{aligned} \omega_{nat} &= \frac{1}{\sqrt{LC}} , \\ \zeta &= \frac{1}{2R}\sqrt{\frac{L}{C}} . \end{aligned} \qquad \text{(C.7)}$$

After Filtering the block signal becomes:

$$V_{out}(t) = \delta V_{in} + V_{in} \sum_{n=1}^{\infty} r_n \sin(\frac{2n\pi t}{T_s} + \chi_n) \ . \qquad \text{(C.8)}$$

Where

$$\begin{aligned} r_n &= c_n \ |F(j\omega_n)| \ , \\ |F(j\omega_n)| &= \frac{\omega_{nat}^{\ 2}}{\sqrt{(\omega_{nat}^{\ 2}-\omega_n^{\ 2})^2 + (2\zeta\omega_{nat}\omega_n)^2}} \ , \\ \omega_n &= \frac{2n\pi}{T_s} \ , \\ \chi_n &= \varphi_n + \psi_n \ , \ and \\ \psi_n &= - \arctan(\frac{2\zeta\omega_{nat}\omega_n}{\omega_{nat}^{\ 2}-\omega_n^{\ 2}}) \ . \end{aligned} \qquad \text{(C.9)}$$

To calculate the value of the output capacitance we will use the Fourier series of the output voltage. Assuming that after filtering those n-th harmonics (n>1) are very much smaller than the first harmonic, we have:

$$\begin{aligned} V_{out}(t) &= \delta V_{in} + r_1 \ V_{in} \sin(\frac{2\pi t}{T_s} + \varphi_1 + \psi_1) \ , \\ V_{out} &= \delta V_{in} \ . \end{aligned} \qquad \text{(C.10)}$$

The top-top ripple will be:

$$\Delta V_{out} = 2|V_{out}(t) - \delta V_{in}| = 2 \ r_1 \ Vin \ . \qquad \text{(C.11)}$$

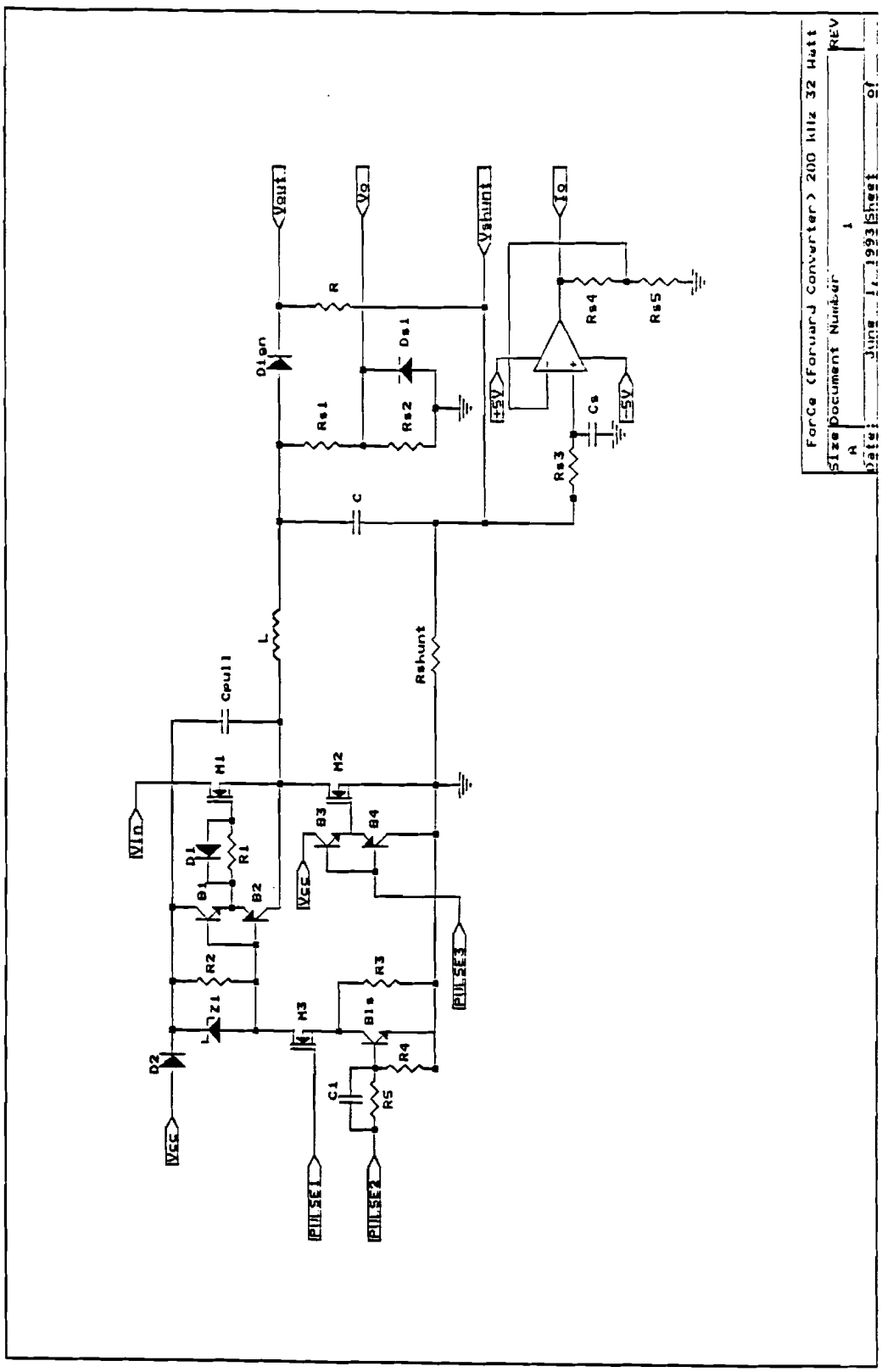
Or relative ripple to the DC output Voltage:

$$\left[\frac{\Delta V_{out}}{V_{out}}\right] = \frac{2 \ r_1}{\delta} = 4 \ \frac{\sin(\pi\delta)}{\pi\delta} \ \frac{\omega_{nat}^{\ 2}}{\sqrt{(\omega_{nat}^{\ 2}-\omega_s^{\ 2})^2+(2\zeta\omega_{nat}\omega_s)^2}} \ . \qquad \text{(C.12)}$$

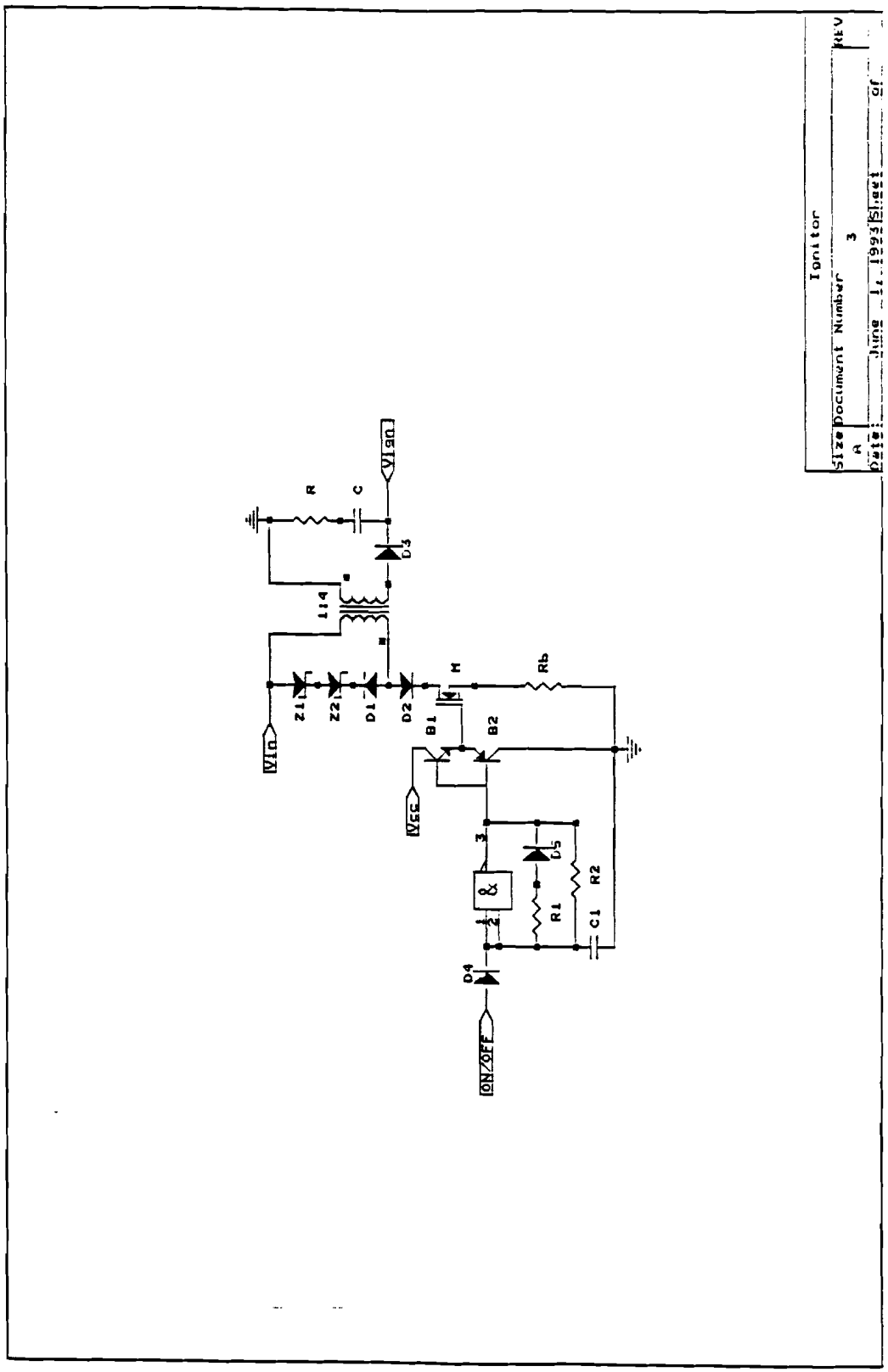
The relative ripple is a design parameter.

APPENDIX D. ForCe AND IGNITOR

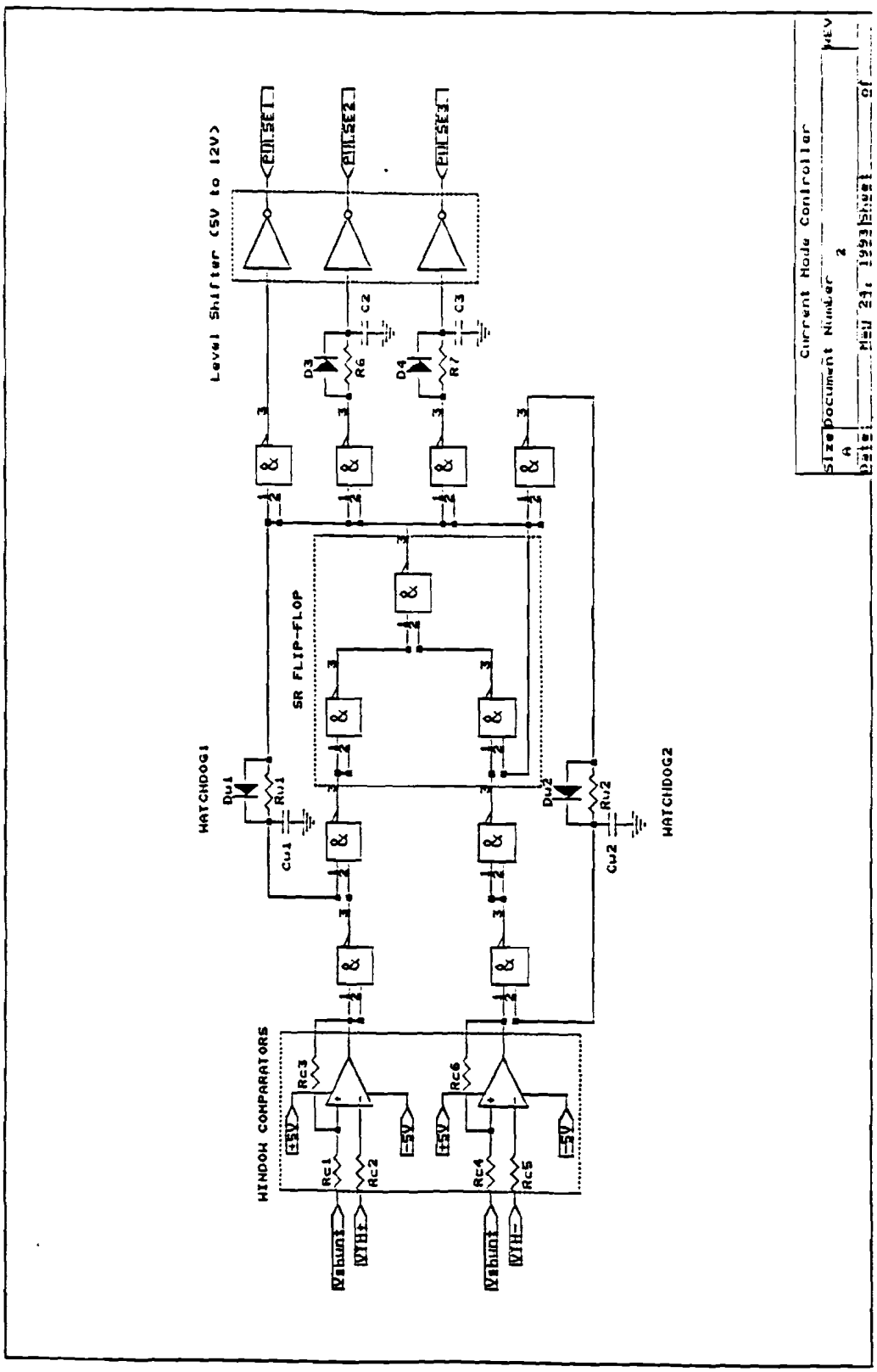
D.1. COMPLETE SCHEMATIC OF ForCe



D.2. COMPLETE SCHEMATIC OF IGNITOR



APPENDIX E. COMPLETE SCHEMATIC OF C.M.C.



```
Screen # 0
( POWERCONTROLLER                          RZQ 10:12 04/14/93)
( Last changed screen # 046                RZQ 04:10 03/23/93)
```

```
Screen # 1
(                                          RZQ 11:54 06/04/93)
EMPTY
22 46 THRU LOAD
```

```
Screen # 2
( BOUNDARY                                 RZQ 09:35 05/28/93)

   GRADUATION-PROJECT, RIZQA DERFIORA, DEC 1992 - MAY 1993
     HIGH INTENSITY DISCHARGE (HID) LAMP CONTROL CIRCUIT


BOUNDARY:
1. THE FORWARD CONVERTER IS ON CURRENT MODE CONTROL (CMC),
2. THE FORWARD CONVERTER IS ASSUMED AS A CURRENT SOURCE,
3. THE LAMP POWER WILL BE KEPT CONSTANT (POWER CONTROLLER),
4. THE LAM HAS A NON MINIMUM PHASE v-i CHARACTERISTIC,
5. BUT THE LAMP HAS A MINIMUM PHASE p-i CHARACTERISTIC ,
6. THE SYSTEM IS MULTI-INPUT SINGLE-OUTPUT (MISO).
```

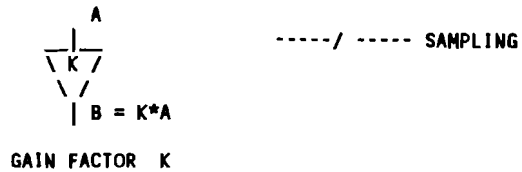
```
Screen # 3
( LAMP STATES                              RZQ 22:46 05/27/93)

              D E V E L O P M E N T   P H A S E   I

THERE ARE THREE LAMP STATES :
1. OPEN-CIRCUIT STATE,
2. SHORT-CIRCUIT STATE,
3. NORMAL STATE,

AD1. IN OPEN CIRCUIT STATE VTH+ MUST BE AS HIGH AS IN NOMINAL
     STATE. NO POWER REGULATION.
AD2. SHORT CIRCUIT STATE IDEM AD1. IN THIS WAY A SOFT START
     WILL BE GUARANTUEED.
AD3. IN THE NORMAL STATE THE REGULATION (THE CONTROLLER)
     MUST BE ACTIVED.
```

```
Screen # 4
( SPECIFICATIONS                           RZQ 22:45 05/27/93)

POWER CONTROLLER

THERE ARE TWO INPUTS:
1. OUTPUT VOLTAGE VOUT
2. OUTPUT CURRENT IOUT

THE CONTROLLER OUTPUT IS VH+ (TOP OF THE INDUCTOR CURRENT)

OTHERS IMPORTANT SPECIFICATIONS:
1. CONTROL SIGNAL LIMITER,
2. THE SPEED OF REGULATION (BAND-WIDTH),
3. DEFINITION OF HIGH & LOW FOR VOUT & IOUT (FUZZY),
4. TIMER TIME UNIT IS 200 ns FOR SINGEL LENGTH,
5. SAMPLE TIME (CHOOSEN 1 ms).
```

```
Screen # 5
( THE MEANING OF SYMBOLS                   RZQ 01:24 03/23/93)

                    M U L T I P L I E R



                A ----->
                        * ----> C = A*B
                B ----->
```

Screen # 6
(RZQ 15:01 04/15/93)

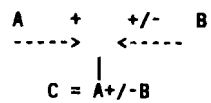
G A I N F A C T O R & S A M P L I N G



GAIN FACTOR K

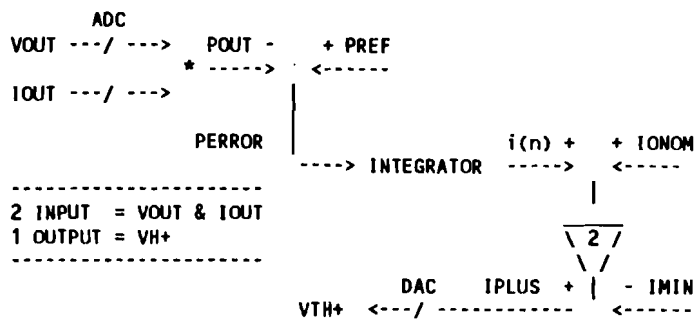
Screen # 7
(RZQ 15:01 04/15/93)

A D D E R & S U B T R A C T E R



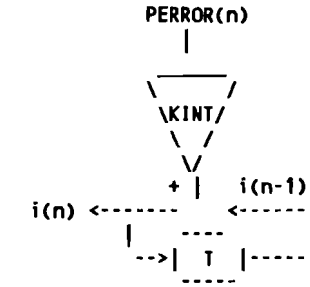
Screen # 8
(GENERAL SCHEME RZQ 01:24 03/23/93)

P O W E R C O N T R O L L E R



Screen # 9
(INTEGRATOR RZQ 10:06 05/07/93)

I N T E G R A T O R

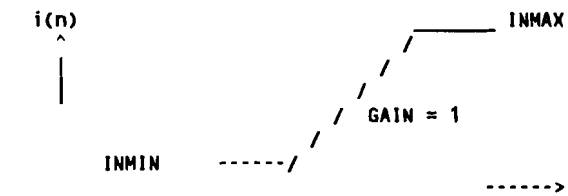


i(n) = i(n-1) + KINT*PERROR(n)

KINT = (K*Ts) / Ti
K = GAIN FACTOR
Ts = SAMPLE TIME
Ti = TIME CONSTANT

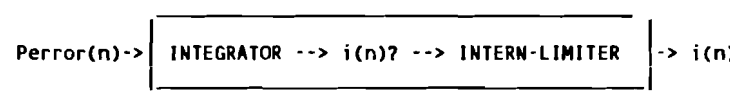
Screen # 10
(INTERN-LIMITER RZQ 08:26 05/17/93)

I N T E R N - L I M I T E R



Screen # 11
(INTEGRATOR WITH INTERN-LIMITER RZQ 14:27 05/11/93)

NON LINEAR INTEGRATOR



AFTER EXECUTION OF A CONTROL CYCLE i(n-1):=i(n), NOT i(n)?. SEE INTERN-LIMIT.

```
Screen # 12
( STRUCTURE                                    RZQ 12:02 05/28/93)

STRUCTURE OF THE POWER REGULATION IN NORMAL STATE:
1. VOUT & IOUT MEASUREMENTS (ALSO IN OTHER STATES),
2. POWER ERROR CALCULATION, PREF-VOUT*IOUT,
3. POWER ERROR AS INPUT OF THE CONTROLLER, WHICH RESULTS
   A CONTROL SIGNAL IPLUS, SOMEHOW IS RELATED TO VH+,
4. LIMITER TO ACCURE INDUCTOR (MAGNETIC) SATURATION,

POSSIBLE TYPE OF CONTROLLER:
1. A SIMPLE INTEGRATOR WITH A TIME CONSTANT (I CONTROLLER),
2. ZERO-POLE PLACEMENT CONTROLLER (LAMP MODEL AVAILABLE),
```

```
Screen # 13
( THE MAGIC OF *2^16 IN FORTH                  RZQ 16:14 05/06/93)

INTEGRATION:

            i(n) = i(n-1) + KINT*PERROR(n)

THE VALUE OF KINT  MUCH SMALLER THAN 1, DIVISION WILL GIVES BAD
ACCURACY IN THE CLOSED-LOOP. SO THE *2^16 TRICK IS APLLIED:

      2^16*i(n) = 2^16*i(n-1) + KINT*2^16 * PERROR(n)

BINARY, MULTIPLYING WITH 2^16 MEANS SIMPLY 'SHIFT' THE LOW WORD
16 BIT, SO IT BECAMES A HIGH WORD OF A 32 BIT WORD. IN FORTH:

  ( n*2^16 MEANS n 0 SWAP )   AND    ( d/2^16 MEANS  d NIP )
```

```
Screen # 14
( NUMBER CONSIDERATION                         RZQ 14:31 05/11/93)

IF:
d,max   = 2147483647          d,min   = -2147483647
IOUTNOM = 500   PREF  = 500   IOUTMAX =  1000   IOUTMIN = 250
VOUTNOM = 500   SCALE = 500   VOUTMAX =  1000

THEN:                    - PREF < PERROR < 3*PREF

LIMITATION 1:            3*PREF*KINT*2^16*  < d,max
(SIGN DOUBLE LENGTH)     -PREF*KINT2^16*    > d,min
                          KINT*2^16,max = 2^15
                          KINT*2^16,min = 2

LIMITATION 2:            IOUTMIN < IOUTNOM + i(n) < IOUTMAX
(INDUCTOR SATURATION)       INMIN   <  i(n)   < INMAX
```

```
Screen # 15
( STATES MACHINE                               RZQ 01:26 03/23/93)

       D E V E L O P M E N T   P H A S E  I I

DC HID LAMP MUST BE BALLASTED CORRECTLY. THE MOST CRITICAL
PERIOD IS DURING THE START-UP.

THE FORWARD CONVERTER (FORCE) TRAVEL IN SEVERAL MODES:
1. OPEN CIRCUIT = READY TO IGNITE,
   FORCE OUTPUT VOLTAGE IS ABOUT 400 VOLT,
2. IGNITION,
   IGNITION VOLTAGE IS ABOUT 1.6 kV,
3. SHORT CIRCUIT = LAMP IS ALREADY IGNITED,
   FORCE OUTPUT VOLTAGE IS ABOUT 15 VOLT,
4. NORMAL STATE = INTEGRATOR IS ACTIVED.
```

```
Screen # 16
( STATES, V-STATE                              RZQ 14:02 06/03/93)

VOUT IS LIMITED INTO 1024 (ZENER 5 VOLT), WHICH IS RELATED TO
THE REAL LAMP VOLTAGE 200 VOLT. IF THE REAL LAMP VOLTAGE IS
GREATER THAN 200 VOLT, VOUT IS STILL 1024. SO WE CAN NOT DEFINE
THE STATES OF THE OUPUT VOLTAGE OF FORCE, V-FORCE, WITH VOUT IN
ALL POSSIBLE VALUES (FOR INSTANCE IN OPEN CIRCUIT).

V-FORCE CAN MEASURE THE WHOLE RANGE: 0-400 VOLT,
SO WE CAN CLEARLY DEFINE THE STATE OF THE OUTPUT VOLTAGE OF THE
FORCE.

        0  < V-FORCE <  50 VOLT, V-STATE = 0
       50  < V-FORCE < 380 VOLT, V-STATE = 1
           V-FORCE > 380 VOLT, V-STATE = 2
```

```
Screen # 17
( I-STATE                                      RZQ 10:25 05/28/93)

I-STATE IS SYMPLY DERIVED FROM IOUT. AND IT HAS ONLY 2 STATES,
0 & 1.
          0 < I-LAMP < 150 mA, I-STATE = 0
              I-LAMP > 150 mA, I-STATE = 1

THE IMPORTANT STATES ARE:
1. PRE-IGNITED  = END OF "INIT"
        OPEN-CIRCUIT :   V-STATE=2  I-STATE=0
2. IGNITED      = END OF "IGNIT"
        SHORT-CIRCUIT:   V-STATE=0  I-STATE=1
3. POST-IGNITED = BEING "CONTR"
        NORMAL STATE:    V-STATE=1  I-STATE=1

MORE SEE Screen # 43
```

```
Screen # 18
( LISTING OF THE STATES MACHINE, INIT        RZQ 10:25 05/28/93)

OLD-STATE: 0 = INIT

      V-STATE I-STATE  NEW-STATE

         0       0       NOP        ; NO OPERATION
         0       1       MESS1      ; SHORT CIRCUIT
         1       0       NOP        ; NO OPERATION
         1       1       MESS2      ; ITS NOT A LAMP
         2       0       IGNIT      ; IGNITION
         2       1       MESS3      ; OVERLOAD

MORE SEE Screen # 43


Screen # 19
( IGNIT                                     RZQ 10:25 05/28/93)

OLD-STATE: 1 = IGNIT

      V-STATE I-STATE  NEW-STATE

         0       0       MESS4      ; CIRCUIT IS DEFECT
         0       1       CONTR      ; CONTROL THE POWER
         1       0       MESS4      ; CIRCUIT IS DEFECT
         1       1       CONTR      ; CONTROL THE POWER
         2       0       NOP        ; STIL BEING IGNITE
         2       1       MESS3      ; OVERLOAD

MORE SEE Screen # 43


Screen # 20
( CONTR, AND MESS                           RZQ 10:25 05/28/93)

OLD-STATE: 2 = CONTR

      V-STATE I-STATE  NEW-STATE

         0       0       MESS5      ; LAMP IS DEFECT
         0       1       CONTR      ; CONTROL THE POWER
         1       0       INIT       ; BACK TO INITIALIZE
         1       1       CONTR      ; CONTROL THE POWER
         2       0       IGNIT      ; LAMP OUT, IGNITE!
         2       1       NOP        ; NO OPERATION

MORE SEE Screen # 43


Screen # 21
( MESS                                      RZQ 10:25 05/28/93)

OLD-STATE: 3 = MESS

      V-STATE I-STATE  NEW-STATE

         0       0       NOP        ; NO OPERATION
         0       1       NOP        ; NO OPERATION
         1       0       NOP        ; NO OPERATION
         1       1       NOP        ; NO OPERATION
         2       0       NOP        ; NO OPERATION
         2       1       NOP        ; NO OPERATION

MORE SEE Screen # 43


Screen # 22
( VALUE, AND DVALUE                         RZQ 23:13 05/27/93)

: VALUE ( n -- ) CREATE , DOES> @ ;
: TO    ' >BODY
     STATE @ IF [COMPILE] LITERAL  COMPILE !
          ELSE !
          THEN ; IMMEDIATE

\ example usage:    3 VALUE foo    foo .   77 TO foo  foo .

: DVALUE ( d -- ) CREATE , , DOES> 2@ ;
: DTO    ' >BODY
     STATE @ IF [COMPILE] LITERAL  COMPILE 2!
          ELSE 2!
          THEN ; IMMEDIATE


Screen # 23
( LIST, FALSE, TRUE, AND WAIT-FOR           RZQ 23:05 05/27/93)

: LIST ( n -- ) CR ." Screen # " DUP .
  BLOCK
  16 0 DO CR I 2 .R SPACE
         DUP 64 TYPE  64 +
       LOOP DROP ;

                  0 CONSTANT FALSE
                  FALSE 0= CONSTANT TRUE

: WAIT-FOR  ( n -- )
  ?TERMINAL IF KEY = ELSE DROP FALSE THEN ;
```

```
Screen # 24
( ASCII, MENU, AND BEEP                          RZQ 12:12 06/04/93)

: ASCII BL WORD 1+ C@
  STATE @ IF [COMPILE] LITERAL THEN ; IMMEDIATE

: MENU
  ASCII E  WAIT-FOR ;

: BEEP 7 EMIT ;

VARIABLE AA  ' D< AA !

: D> [ AA @ ' D> AA ! ] LITERAL EXECUTE ;

: D< [ AA @ ] LITERAL EXECUTE ;
```

```
Screen # 25
( M/, *2^16, /2^16, DMIN, DMAX                   RZQ 00:05 03/23/93)

: M/ M/MOD NIP ; ( d n1 -- n2 )

: *2^16 ( n -- d ) 0 SWAP ;

: /2^16 ( d -- n ) NIP ;

: DMIN  ( d1 d2 -- dmin )
  2OVER 2OVER
  D> IF 2SWAP 2DROP ELSE 2DROP THEN ;

: DMAX ( d1 d2 -- dmax )
  2OVER 2OVER
  D< IF 2SWAP 2DROP ELSE 2DROP THEN ;
```

```
Screen # 26
( VALUES                                         RZQ 14:06 06/03/93)

     500 VALUE SCALE                  500 VALUE PREF
     500 VALUE IONOM                 -200 VALUE IMIN
       0 VALUE i(n-1)                1390 VALUE IPLUSNOM
    2340 VALUE IPLUSMAX               780 VALUE IPLUSMIN
     975 VALUE IOMAX                  175 VALUE IOMIN
     475 VALUE INMAX                 -350 VALUE INMIN
      40 VALUE INV-KINT              4456 VALUE KINT*2^16
    5000 VALUE SAMPLE-TIME              0 VALUE COUNT-ERROR
     100 VALUE VLOW                   800 VALUE VHIGH
     250 VALUE ILOW                     0 VALUE OLD-STATE
      0. DVALUE Di(n-1)                 0 VALUE <VFC>(n-1)
  340000. DVALUE DSAMPLE-TIME           0 VALUE <IOUT>(n-1)
                                        6 CONSTANT #COLUMNS
\ INV-KINT = 1/KINT
```

```
Screen # 27
( POWER ERROR CALCULATOR                         RZQ 14:05 06/03/93)

: IOUT 1 A/D ; \ IOUT IS MEASURED ON CHANNEL 1 (A/D)
: VOUT 2 A/D ; \ VOUT IS MEASURED ON CHANNEL 2 (A/D)
: VFC  3 A/D ; \ VIGN IS MEASURED ON CHANNEL 3 (A/D)

: PERROR ( -- n )
  PREF  IOUT VOUT SCALE */  - ;

: PROBE-I
  BEGIN CR IOUT . ?TERMINAL UNTIL ;

: PROBE-V
  BEGIN CR VOUT . ?TERMINAL UNTIL ;
```

```
Screen # 28
( <VFC>, <ILOW>, V-, AND I-STATE                 RZQ 16:34 06/03/93)

: <VFC> ( -- n2 )
  <VFC>(n-1) 80 100 */  VFC 20 100 */  + DUP TO <VFC>(n-1) ;

: <IOUT>
  <IOUT>(n-1) 80 100 */  IOUT 20 100 */  + DUP TO <IOUT>(n-1) ;

: V-STATE  ( <VFC> -- n )
  DUP VLOW  < IF DROP 0 ELSE
      VHIGH < IF      1 ELSE
                      2 THEN THEN ;

: I-STATE
  ILOW < IF 0 ELSE
            1 THEN ;
```

```
Screen # 29
( INTEGRATOR BASIC                               RZQ 11:43 05/10/93)

: INTERN-LIMIT ( n -- nmax or nmin )
  INMAX MIN  INMIN MAX ;

: INTEGRATES ( n1 -- n2 )
  INV-KINT /  i(n-1)  +   INTERN-LIMIT
  DUP TO i(n-1) ;
```

```
Screen # 30
( INTEGRATOR WITH *2^16 MANIPULATION          RZQ 09:28 05/10/93)

: INMAX*2^16 ( n -- d )
  INMAX *2^16 ; \ SHIFT 16 BIT LOW TO HIGH

: INMIN*2^16 ( n -- d )
  INMIN *2^16 ; \ SHIFT 16 BIT LOW TO HIGH

: INTERN-LIMIT*2^16  \ ( Di(n)? -- Di(n) )
  INMAX*2^16 DMIN  INMIN*2^16 DMAX ; \ LIMITER DOUBLE FUNCTION

: INTEGRATED ( n1 -- n2 )
  KINT*2^16 M* Di(n-1) D+  INTERN-LIMIT*2^16
  2DUP DTO Di(n-1) /2^16 ;


Screen # 31
( CHOOSE-INTEGRATOR, AND COUNT-ERROR          RZQ 23:11 05/27/93)

VARIABLE 'INT ' INTEGRATES 'INT !
: INTEGRATOR 'INT @ EXECUTE ;

: SHOW-ERROR  ( -- )
  COUNT-ERROR 1+ TO COUNT-ERROR
  COUNT-ERROR 5000 > IF 0 TO COUNT-ERROR BEEP CR PERROR . THEN
; \ PRINT THE ERROR EVERY 50*Ts


Screen # 32
( IPLUS                                       RZQ 23:06 05/27/93)

: IPLUS   ( -- n )
  PERROR
  INTEGRATED
  IONOM + 2* IMIN - ; \ IPLUS =2*( IONOM + i(n) ) - IMIN


Screen # 33
( COUNTER & PWM                               RZQ 23:33 03/22/93)

: TIMER0 ( -- )
  64 T01CON ! ; \ T0 IS SET INTO TIMER MODE
                \ SEE DATABOOK SAB 80C166 PAGE 8-5
: PWM1   ( -- )
  TIMER0
  112   CCM0   !
  3     DP2    ! ; \ CC0IO IS SET INTO CAMPARE MODE 3
                   \ SEE DATABOOK SAB 80C166 PAGE 8-10/20
: INITP2-0
  DP2 @ 1 OR  DP2 ! ;

: RESETP2-0  P2 @ 1 OR  P2 ! ;

: SETP2-0  P2 @ 1 NOT AND  P2 ! ;


Screen # 34
( DAC                                         RZQ 11:03 05/28/93)

: INIT-DAC  ( -- )
  PWM1
  -1024 TOREL !  \ SET PWM INTO 10 BIT ACCURACY
  -140 CC1    ! ; \ SET VH+ INTO A VALUE IN NORMAL STATE

: >DAC ( n -- ) NEGATE CC1 ! ; \ STORE TO DAC, COMPARE MODE
                                \ RELATED TO PWM1
: VTH+ ( -- n )
  IPLUS  129 1000 */ ; \ CALCULATE CC1 TO DAC

: TEST-DAC> PWM1 -1024 TOREL ! -400 CC1 ! ; \ POUT < PREF
: TEST-DAC< PWM1 -1024 TOREL ! -600 CC1 ! ; \ POUT > PREF


Screen # 35
( T?, AND WAIT-SAMPLE                         RZQ 18:36 03/22/93)

: T? T6 @ ; \ SHOW THE TIMER VALUE (SINGLE) , TIME UNIT 200 ns

: WAIT-SAMPLE ( -- )
  BEGIN
      T?
      SAMPLE-TIME >
  UNTIL ;
```

```
Screen # 36
( DT?, AND DWAIT-SAMPLE                          RZQ 23:11 05/27/93)

: DT? ( --- d )
  T6 @   \ LOW WORD
  T5 @ ; \ HIGH WORD
         \ SHOW THE TIMER VALUE (DOUBLE)
         \ TIME UNIT 400 ns

: DWAIT-SAMPLE ( -- )
  BEGIN
      DT?
      DSAMPLE-TIME D<    \ D<:=D> SOFTWARE ERROR
  UNTIL ;                \ WAIT IN Ts SECONDS = SAMPLE TIME
```

```
Screen # 37
( TESTING                                        RZQ 09:54 05/24/93)

: IO IPLUS  IMIN + 2/  ; \ SIMULATION UTILITY

: NORMAL CR
  INIT-TIMER
  BEGIN
    TI VTH+ \ IO IS FOR SIMULATION, THE ACTUAL VALUE IS VTH+
    WAIT-SAMPLE
    >DAC SHOW-ERROR MENU
  UNTIL ; \ NORMAL STATE
```

```
Screen # 38
( integration                                    RZQ 23:12 05/27/93)

: integration
  TI VTH+
  WAIT-SAMPLE
  >DAC SHOW-ERROR ;
```

```
Screen # 39
( IGNITOR PULSE                                  ??? 03:32 03/23/93)

: IGNITOR-HIGH
  SETP2-0    \ SET THE IGNITOR ON, RELATED TO P2(0)
  750 TO VHIGH ; \ HYSTERETIC

: IGNITOR-LOW
  RESETP2-0     \ SET THE IGNITOR OFF, RELATED TO P2(0)
  790 TO VHIGH ; \ HYSTERETIC
```

```
Screen # 40
( STATE TABLE                                    RZQ 14:06 06/03/93)

: CELLS 2* ;

: CELL+ 2+ ;

\ : COLUMN <VFC> V-STATE   2*  <IOUT> I-STATE   + ;

: COLUMN ASCII ? EMIT KEY ASCII 0 - DUP 5 U> ABORT" BAH! " ;

: STATE-TABLE  ( -- )
  CREATE DOES>
  #COLUMNS 2* CELLS   OLD-STATE *   +
  COLUMN   2* CELLS   +
  DUP @ TO OLD-STATE CELL+ @ EXECUTE ;
```

```
Screen # 41
( STATES: INIT, NOP, IGNIT, AND CONTR            ??? 14:50 06/04/93)

: INIT BEEP
     INIT-DAC
     INITP2-0
     IGNITOR-LOW
   0 TO OLD-STATE
  790 TO VHIGH
  250 TO ILOW
     ." INIT " CR ;

: NOP ." NOP "   OLD-STATE .   <VFC> .   VFC . CR ;

: IGNIT BEEP IGNITOR-HIGH  250 TO ILOW  ." IGNIT " CR ;

: CONTR IGNITOR-LOW  200 TO ILOW  integration  ." CONTR " CR ;
```

```
Screen # 42
( PRINT-STATE, AND MESSAGES                    RZQ 14:07 06/03/93)

: PRINT-STATE CR ." OLD-STATE = " OLD-STATE .
              CR ." V-STATE   = " <VFC> V-STATE   .
              CR ." I-STATE   = " <IOUT> I-STATE   . ;

: MESS1 ." SHORT CIRCUIT " PRINT-STATE  IGNITOR-LOW ABORT ;

: MESS2 ." IT'S NOT A LAMP " PRINT-STATE IGNITOR-LOW ABORT ;

: MESS3 ." OVERLOAD " PRINT-STATE IGNITOR-LOW ABORT ;

: MESS4 ." CIRCUIT IS DEFECT " PRINT-STATE IGNITOR-LOW ABORT ;

: MESS5 ." LAMP IS DEFECT " PRINT-STATE IGNITOR-LOW ABORT ;
```

```
Screen # 43
( TABLE                                        RZQ 12:59 05/27/93)

: >n CREATE , IMMEDIATE DOES> @ , ;

 0 >n :0    1 >n :1    2 >n :2    3 >n :3   4 >n :4    5 >n :5

STATE-TABLE CONTROLLER

 ] :0 NOP   :3 MESS1  :0 NOP    :3 MESS2  :1 IGNIT  :3 MESS3  [
 ] :3 MESS4 :2 CONTR  :3 MESS4  :2 CONTR  :1 NOP    :3 MESS3  [
 ] :3 MESS5 :2 CONTR  :0 INIT   :2 CONTR  :1 IGNIT  :2 CONTR  [
 ] :3 NOP   :3 NOP    :3 NOP    :3 NOP    :3 NOP    :3 NOP    [
```

```
Screen # 44
( RUN CONTROLLER                               RZQ 13:22 05/28/93)

: RUN
  INIT
  INIT-TIMER
  BEGIN
    CONTROLLER
    MENU
  UNTIL
    PRINT-STATE
    INIT-DAC
    IGNITOR-LOW ;
```

```
Screen # 45
( IGNITOR-TEST                                 RZQ 03:52 03/23/93)

37500000. DVALUE DT-MAX

: IGNITOR-TEST
  BEGIN
    <VFC> DUP CR .
    780 >
  UNTIL
    INIT-TIMER  T!
  BEGIN
    IGNITOR-HIGH
    <VFC> 300  <   DT? DT-MAX D>   OR
  UNTIL IGNITOR-LOW ;
```

```
Screen # 46
( CHANGE POWER                                 RZQ 04:10 03/23/93)

: POW500 500 TO PREF 500 TO SCALE ;

: POW600 600 TO PREF 600 TO SCALE ;

: TEST-VFC
  BEGIN
    <VFC> CR .
    ?TERMINAL
  UNTIL ;
```

```
Screen # 47
(                                              RZQ 13:12 04/08/93)
```

APPENDIX G. POWER MEASUREMENT RESULTS

In figure G.1 the poles are real, so there is no oscillation in the transient characteristic.

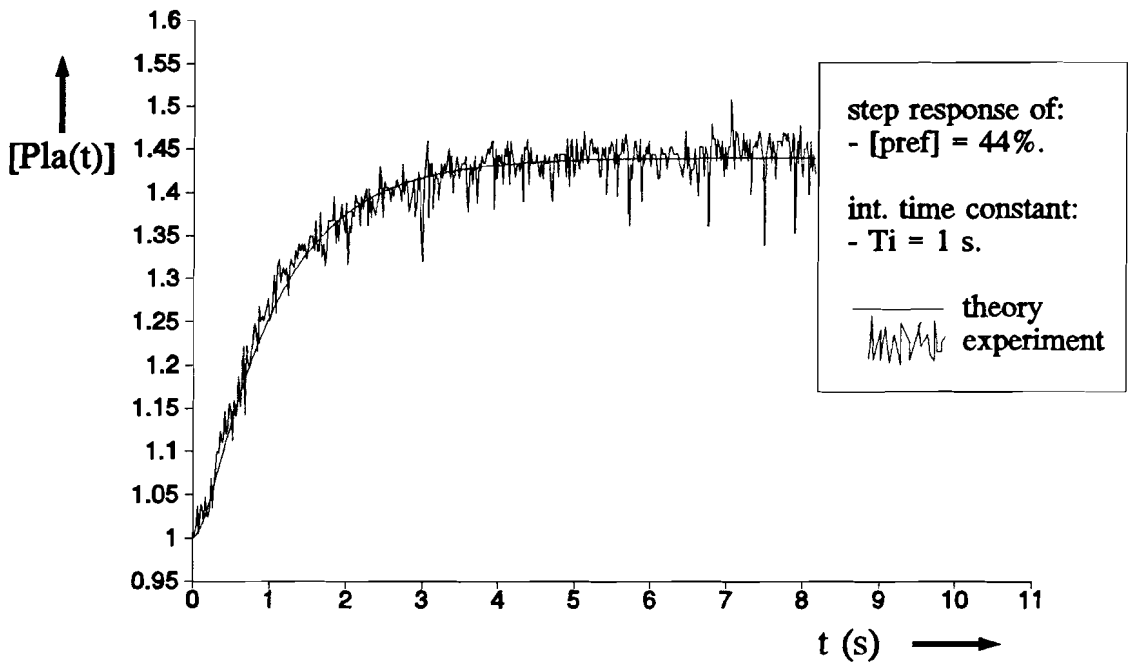


Figure G.1. Power step response by too large integration time constant.

In figure G.2 the poles are complex, so there is oscillation in the transient characteristic.

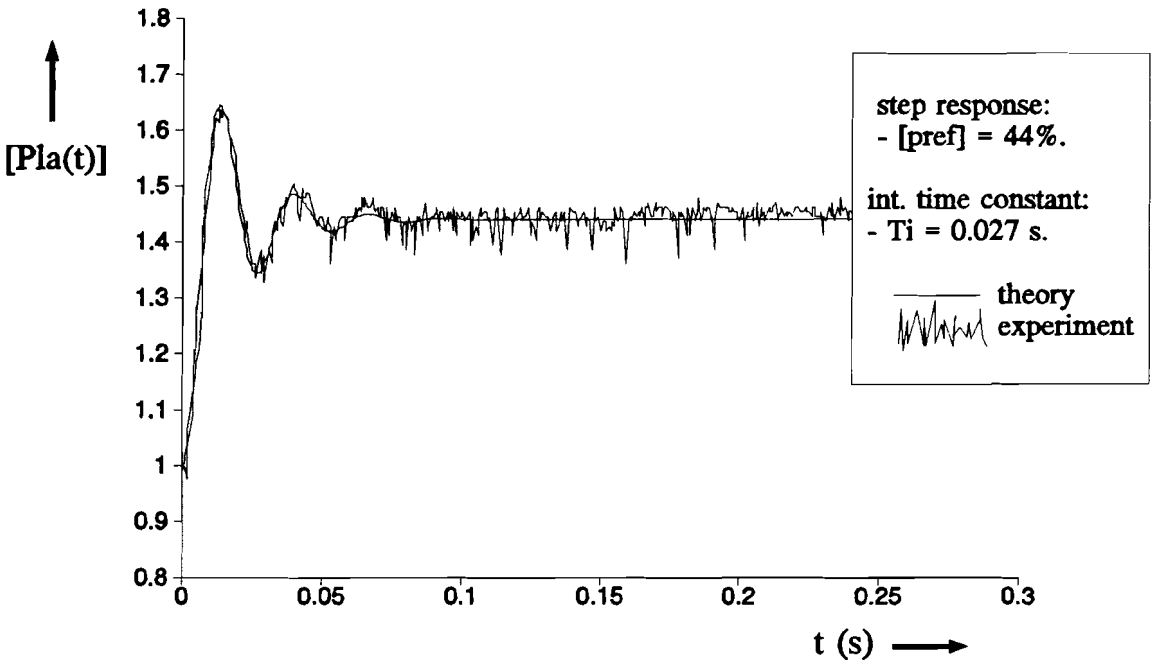


Figure G.2. Power step response by too small integration time constant

In figure G.1 and figure G.2 these following conditions are valid: $\alpha\beta\gamma=0.9$ and $\beta\gamma=1.05$. So $\alpha=0.86$ (see also chapter 5.2.3).