An inquiry into the use of BIMOS-techniques in designing digital output circuits

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AN INQUIRY INTO THE USE OF BIMOS-TECHNIQUES IN DESIGNING DIGITAL OUTPUT CIRCUITS.

by P.van der Zee.

Verslag van het afstudeerwerk uitgevoerd van juli 1983 tot mei 1984 in opdracht en onder begeleiding van
prof. dr. F.M. Klaassen.

VOORWOORD

Dit verslag is geschreven ter afsluiting van een afstudeerperiode van ongeveer een jaar.
Gedurende deze tijd ben ik op het Philips Natuurkundig Laboratorium te Eindhoven bezig geweest met het onderzoeken van de mogelijkheden, die het BIMOS proces biedt bij het ontwerpen van bufferschakelingen voor het schakelen van grote capacitieve belastingen. Daarbij is een vergelijking gemaakt met soortgelijke schakelingen ontworpen in een CMOS proces. Een aantal van de ontworpen schakelingen is geïntegreerd, om de theorie aan de praktijk te kunnen toetsen. Op het moment van dit schrijven zijn de geïntegreerde schakelingen nog niet klaar en daarom zijn in dit verslag geen meetgegevens van de praktijk-schakelingen te vinden.
Hierbij wil ik een woord van dank uitspreken aan prof.dr. F.M. Klaassen, onder wiens leiding dit onderzoek heeft plaatsgevonden en die gezorgd heeft voor waardevolle op- en aanmerkingen ter verbetering van dit verslag.
Tevens wil ik Marleen Jansen en Agnes Carli bedanken voor hun inzet bij het typen van dit verslag.

TABLE OF CONTENTS

0. INTRODUCTION

For the manufacture of integrated circuits different processes are being used. For CMOS this can be for example the C500 process.
Every process has its own qualifications and C500 for instance is an n-well process with a polysilicon gate located on 500 Å thin oxide. Shallow n, shallow p, and deep n diffusions are being used to form the NMOST, the PMOST and the n-well respectively. Apart from the dope of these diffusions it is not possible in this process to make a bipolar transistor, because for that we need an extra base diffusion and a burried n^+ layer to reduce the collector resistance.
The differences between a bipolar and a CMOS process as mentioned above are not the only ones, but they give a fair impression of the way in which both processes differ.
When one wants to make circuits, which contain bipolar transistors as well as MOS transistors, a new process has to be developed. This will be a more complex process, because more masks and more processing steps are needed.
In developing such a process it is important, that the parameters of the bipolar and MOS transistors correspond with those in the individual bipolar- and MOS processes. In that situation designs already existing in bipolar- or MOS-techniques can be realized with this new process without any adaption. At this moment the development of the new combination process has come in its final state and the process is referred to as the BIMOS process. In this report an impression is given of the qualities this new process offers in designing digital output circuits, in which bipolar and MOS transistors are being used. The output circuits have been designed to be capable of switching a capacitive load of 50 pF in 5 ns between 0 and 5V.

In the first chapter some calculations are given concerning the combination of MOS transistors and bipolar transistors. These calculations will be compared with results obtained with the circuit analysis program PHILPAC.

In the second chapter some BIMOS driver circuits will be described with their pros and cons. Each circuit has been simulated with the PHILPAC program.

In the third chapter the switching properties of a conventional CMOS driver circuit are examined and compared with those of the BIMOS-circuits in chapter two.

The fourth chapter deals with a BIMOS-inverter circuit, which consists of minimum area components. The performance of this BIMOS-circuit is compared with a CMOS-inverter. This comparison is based upon the results obtained with a ringoscillator consisting of BIMOS- or CMOS inverters.

In the fifth chapter the layout of the integrated circuits has been described. These are three BIMOS driver circuits, a ringoscillator consisting of BIMOS circuits loaded with a capacitor of 1 pF and a ringoscillator with unloaded BIMOS inverters.

1. CALCULATIONS ON A BIMOS DRIVER-CIRCUIT

1.1. Introduction

In order to calculate the various switchingtimes of a bipolar transistor, that is driven by a MOST, in this chapter we use the charge-control model as described in the lecture notes "On semiconductor devices" written by prof.dr. F.M. Klaassen [1] . Introducing several simplifications, it is possible to find analytical solutions of the differential equations. Without those simplifications, we get more accurate switching times, but then the equations cannot be solved analytically. Therefore in this case the differential equations are solved numerically with the computerprogram PHILPAC.
The analytical and numerical solutions are compared in order to assess the validity of the simplifications.

1.2. The discharge of a load-capacitor

The circuit, which we are going to examine, is drawn in fig. 1.1.

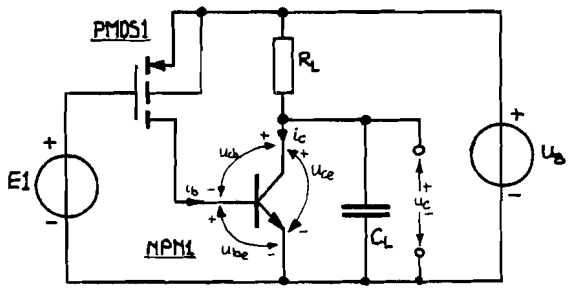


fig. 1.1.

In this circuit E1 is a voltage source, that can be switched between 0V and 5V. At $t<0$ this voltage is 5V, so PMOS1 is not turned on and the bipolar transistor NPN1 is not

driven. Due to R_L the load-capacitor C_L is charged to the power-supply voltage U_b. At t=0 we assume the base-emittor voltage to be zero because of the negligible base-current i_b.

1.2.1. The turn-on delaytime of the pull-down circuit

When E1 is switched to zero, the PMOST starts to conduct and the drain current first has to charge the base-emitter depletion capacitor C_e to a sufficiently large voltage V_T ($V_T \approx 0.7V$), before the bipolar transistor starts drawing a significant collector current. The time necessary to reach this voltage is called the turn-on delaytime.
We can calculate this time as follows.
When we assume the depletion-capacitors to be constant, the equations of i_b and i_c in the charge-control model (see [1] pp. 43-45) become:

$$i_b = \frac{q_F}{\tau_F} + \frac{dq_F}{dt} + C_e \frac{du_{be}}{dt} - C_c \frac{du_{cb}}{dt} \qquad (1)$$

and

$$i_c = \beta_F \frac{q_F}{\tau_F} + C_c \frac{du_{cb}}{dt} \qquad (2)$$

with q_F = storage-charge
τ_F = forward transit-time
C_e = base-emitter depletion-capacitor
C_c = base-collector depletion-capacitor
β_F = forward current-gain.

In this case, since $u_{be} < 0.7V$, q_F is very small and negligible with respect to the depletion-charges. So (1) and (2) become:

$$i_b = C_e \frac{du_{be}}{dt} - C_c \frac{du_{cb}}{dt} \tag{3}$$

and

$$i_c = C_c \frac{du_{cb}}{dt} \tag{4}$$

Because R_L is very large, we may neglect the current through this resistor. A second equation for the collector-current can now be given:

$$i_c = -C_L \frac{du_c}{dt} = -C_L \frac{du_{ce}}{dt} \tag{5}$$

With (4) and (5) we find:

$$C_L \frac{du_{ce}}{dt} + C_c \frac{du_{cb}}{dt} = 0 \tag{6}$$

and with

$$\frac{du_{ce}}{dt} = \frac{du_{cb}}{dt} + \frac{du_{be}}{dt}$$

it follows that

$$\frac{du_{cb}}{dt} = \frac{-C_L}{C_L + C_c} \frac{du_{be}}{dt} \tag{7}$$

Combining (3) and (7) gives a simple differential equation for the base-emitter voltage:

$$\frac{du_{be}}{dt} = \frac{i_b}{\left[C_e + \frac{C_L C_c}{C_L + C_c}\right]} \tag{8}$$

From circuit 1.1 we see that the following inequality applies to the drain-source voltage of PMOS1:

$$-(u_B - u_{be}) < -(u_B - V_{th})$$

Therefore this transistor always operates in saturation and

the basecurrent is given by:

$$i_{bs} = \frac{\beta}{2}(u_B - V_{th})^2 = \frac{W}{L}\frac{\beta_\square}{2}(u_B - V_{th})^2 \qquad (9)$$

with V_{th} = threshold voltage
β = gain-factor
$\beta_\square$ = gain-factor of square transistor
W = width of the channel
L = length of the channel.

As the base-current is constant, the solution of the differential equation (8) becomes:

$$u_{be} = \frac{i_{bs}\, t}{C_e + \frac{C_L C_c}{C_L + C_c}} \qquad (10)$$

Now we consider two different situations.
In the first place the loadcapacitor can be relatively large ($C_L \gg C_c$), which means that C_c is negligible with respect to C_L. This occurs, for example, when the transistor is used in a linedriver circuit. Then (10) becomes:

$$u_{be} = \frac{i_{bs}\, t}{C_e + C_c} \qquad (10a)$$

As a second possibility C_L is assumed to be relatively small ($C_L \ll C_c$), for example in an invertercircuit. The equation then becomes:

$$u_{be} = \frac{i_{bs}\, t}{C_e} \qquad (10b)$$

In the latter case the base-emitter voltage rises faster, so the delaytime will be shorter. Usually we are interested in the first situation. The delaytime t_d is defined as the time, in which u_{be} rises to the turn-on voltage V_T of the bipolar transistor NPN1 ($V_T \approx 0.7V$). When u_{be} exceeds this

voltage the collector current increases rapidly. Now the delaytime can be calculated with the following equation:

$$t_d = \frac{(C_e + C_c)\, V_T}{i_{bs}} \qquad (11)$$

Taking into account the bodyeffect, we find for the threshold voltage of PMOS1 (see [1] p. 57).

$$V_{th} = V_{TO} + k\sqrt{2\varphi_F} \qquad (12)$$

with V_{TO} = zero-bias threshold-voltage
k = body-factor
$2\phi_F$ = diffusion-voltage

The relevant parameters of the components used are listed below (from appendices B1 and B3).

C_e	= 2 pF
C_c	= 0.44 pF
V_{TO}	= 1.1 V
K	= 0.75 $V^{1/2}$
$2\varphi_F$	= 0.65V
$\beta_\square$	= 15 µA/V^2

With these parameters we find:

V_{th} = 1.7V
and i_{bs} = 40.8*W µA (W in µm) (13)

Now it is possible to write down the delaytime t_d as a function of the MOS transistor width W :

$$t_d = 41.9/W \text{ ns} \quad (W \text{ in } \mu m) \qquad (14)$$

1.2.2. The falltime

Here we use the same circuit as drawn in fig. 1.1. For $u_{be} > V_T$ the storage-charge q_F increases much faster with base-emitter voltage than the depletion charge and therefore the latter can be neglected in the calculations. As PMOS1 operates in saturation, the basecurrent remains constant and causes the storage-charge q_F to increase.

Consequently we find for the base- and collectorcurrent:

$$i_b = \frac{q_F}{\tau_F} + \frac{dq_F}{dt} - C_c \frac{du_{ce}}{dt} \tag{15}$$

$$i_c = \beta_F \frac{q_F}{\tau_F} + C_c \frac{du_{ce}}{dt} \tag{2}$$

These are the transistor equations. In the circuit these currents are determined by the PMOST and the load-capacitor C_L.

$$i_b = i_{bS} = \frac{W}{L} \frac{\beta_n}{2} (u_B - V_{th})^2 \tag{9}$$

$$i_c = -C_L \frac{du_{ce}}{dt} \tag{16}$$

With (2) and (16) the storage-charge can be determined:

$$q_F = -\frac{\tau_F}{\beta_F} (C_c + C_L) \frac{du_{ce}}{dt} \tag{17}$$

$$\frac{dq_F}{dt} = -\frac{\tau_F}{\beta_F} (C_c + C_L) \frac{d^2 u_{ce}}{dt^2} \tag{18}$$

Inserting (17) and (18) in (15) we obtain a differential equation for the collector-emitter voltage, which is the desired output-voltage.

$$\frac{d^2 u_{ce}}{dt^2} + \frac{du_{ce}}{dt} \frac{1}{\tau_F} \left(1 + \frac{\beta_F C_c}{C_c + C_L}\right) = -\frac{\beta_F i_{bs}}{\tau_F (C_c + C_L)} \tag{19}$$

With the initial conditions t=0: $u_{ce} = U_B$ and $i_c=0$ the solution of this differential equation becomes (see appendix A1):

$$u_{ce} = U_B - \frac{\beta_F \delta_1 i_{bs}}{C_L + (\beta_F+1)C_c}\left[\frac{t}{\delta_1} - 1 + \exp\frac{-t}{\delta_1}\right] \qquad (20)$$

$$\text{with} \quad \delta_1 = \frac{\tau_F C_c + C_L}{C_L + (\beta_F+1)C_c} \qquad (20a)$$

The relevant parameters of the bipolar transitor used are (see appendix B1):

$$\tau_F = 50 \text{ pS}, \; C_c = 0.44 \text{ pF} \text{ and } \beta_F = 100$$

Substituting these parameters δ_1 equals 27 pS. As we are interested in a falltime to the order of nanoseconds, t/δ_1 is large and the only significant term between brackets. As a consequence a rather simple expression for u_{ce} remains:

$$u_{ce} = U_B - \frac{\beta_F i_{bs} t}{C_L + (\beta_F+1)C_c} \qquad (21)$$

The definition of the falltime reads:

$$t_f \equiv t_2 - t_1 \quad \text{with } U(t_1) = U(0) - 0.1[U(0)-U(\infty)] \quad \text{and } U(t_2) = U(0) - 0.9[U(0)-U(\infty)] \qquad (22)$$

This is illustrated in Fig. 1.2.

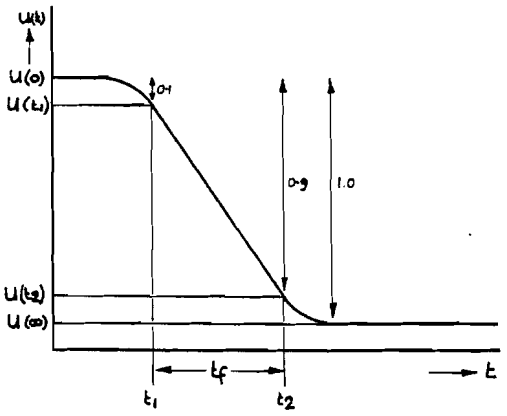


Fig. 1.2.

Because for the bipolar transitor with the parameters as listed in appendix B1 u_{cesat} is very small compared to U_B (U_B=5V, $u_{cesat} < 100$ mV) we will neglect u_{cesat} and calculate the falltime with $U(0)=U_B$ and $U(\infty)=0$.
Substituting these values in eq. (21) we find t_1, t_2 and t_f:

$$t_1 = (U_B - 0.9\,U_B)\,\frac{C_L+(\beta_F+1)C_c}{\beta_F\, i_{bs}},\quad t_2 = (U_B - 0.1\,U_B)\,\frac{C_L+(\beta_F+1)C_c}{\beta_F\, i_{bs}}$$

$$t_f = 0.8\,U_B\,\frac{C_L+(\beta_F+1)C_c}{\beta_F\, i_{bs}} \qquad (23)$$

Inserting the parameters of the bipolar transistor (appendix B1) and the equation of the basecurrent i_b (13) into eq. (23), we find the falltime t_f as a function of the MOS-transistor width W :

$$t_f = \frac{92.6}{W}\ \text{ns} \quad (\text{with } W \text{ in } \mu m) \qquad (24)$$

The delay- and falltime have been calculated for W=24, 26, 28, 30 and 32 µm and the results are shown in table 1.1 and fig. 1.3.

table 1.1.

W [µm]	24	26	28	30	32
t_d [ns]	1.7	1.6	1.5	1.4	1.3
t_1 [ns]	0.5	0.4	0.4	0.4	0.4
t_2 [ns]	4.3	4.0	3.7	3.5	3.3
t_f [ns]	3.9	3.6	3.3	3.1	2.9

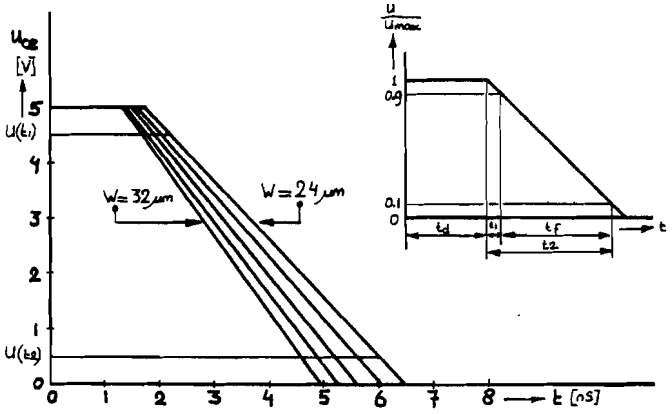


fig. 1.3.

The current-equations of the circuits in fig. 1.1, obtained with complete models for both transistors and without the simplifications (C_c and C_e to be constant), have been solved numerically with the circuit analysis program PHILPAC. The parameters used for this program are listed in appendix B. Figures 1.4 to 1.7 show the output-voltage u_c, the base-emitter voltage u_{be}, the base-current i_b and the collector-current i_c respectively as a function of time. The transitor width W has been varied from 24 µm to 32 µm.

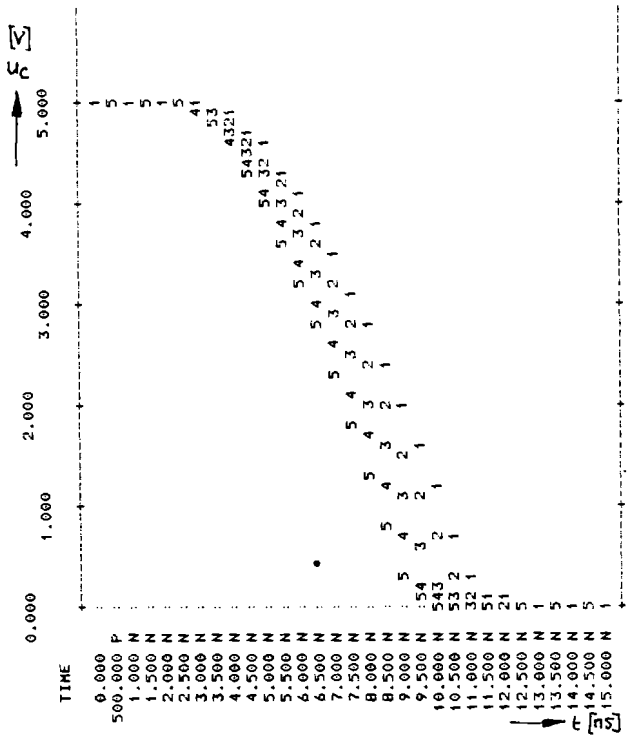


fig. 1.4

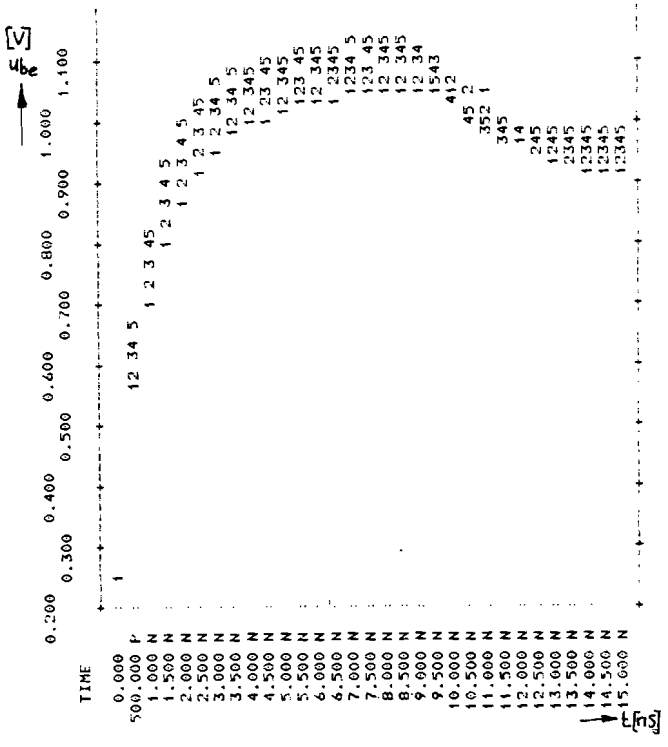


fig. 1.5

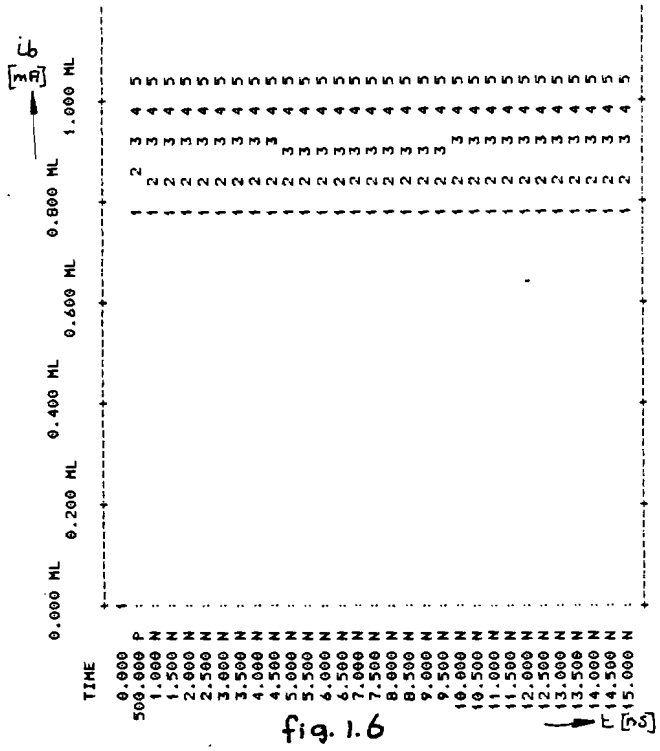


fig. 1.6

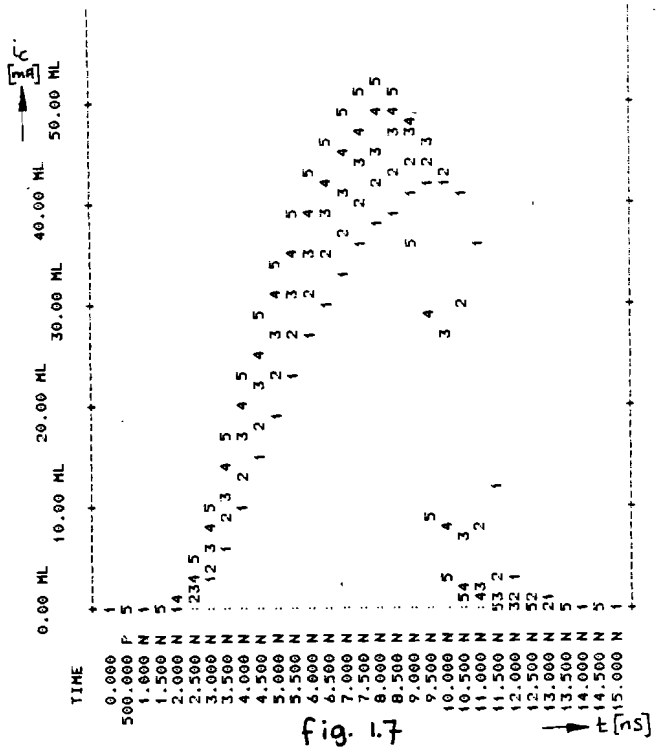


fig. 1.7

The result obtained with the equations (14) and (24) together with the PHILPAC-results are shown in figs. 1.8a and 1.8b. Comparing both results we see, that the simple equation of the turn-on delay-time t_d agrees fairly well to the PHILPAC simulation. Unfortunately the results for the falltime t_f do not agree very well. When we take a look at fig. 1.6 and compare the base-currents i_{bs} in this figure with the base-currents obtained with equation (13), it becomes clear, that part of the disagreement is caused by a wrong base-current and that equation (9) is not a good description for a short-channel MOST in saturation. We obtain the values in fig. 1.6, when the base current i_{bs} is calculated with 32*W. The delaytime and the falltime have been calculated too with this corrected basecurrent and the results agree much better now (see fig. 1.8a and fig. 1.8b).
The analytical and PHILPAC results for the output voltage u_c with W=24µm have been shown in fig. 1.9. In this figure we see, that there is a rather large difference between both results at $t \approx 4$ ns.

In the first place this is caused by the fact, that at this point the changes in depletion-charge and q_F are to the same order of magnitude, so both have to be used in the calculations.

Secondly we have assumed the base-emitterdiode to be a perfect diode, which changes from $R_{diff}=\infty$ to $R_{diff}=0$ at $u_{be}=V_T$.
It should be noticed, that the tangent of the curve obtained with the corrected base current corresponds reasonably well with the tangent of the PHILPAC result and that the difference in the falltime is mainly caused in the interval between t=4ns and t=7 ns.

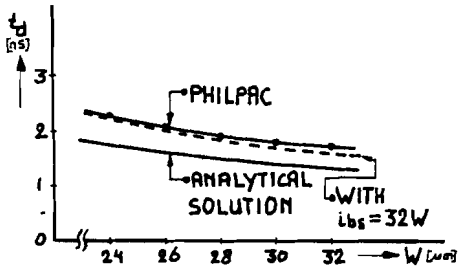


fig. 1.8a.

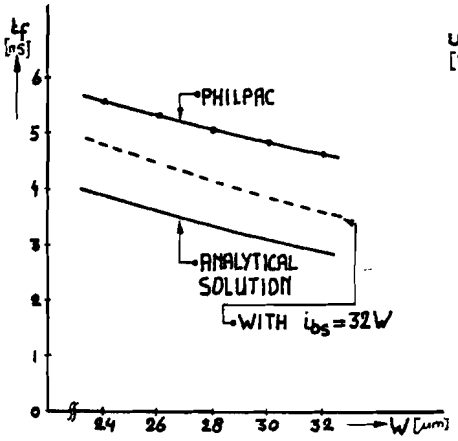


fig. 1.8b.

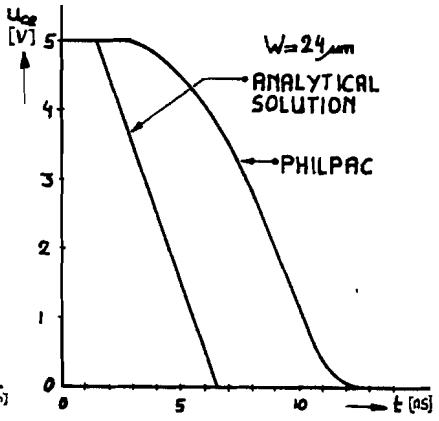


fig. 1.9.

1.3. The charge of a loadcapacitor

The circuit in fig. 1.10 charges the loadcapacitor. At $t<0$ the voltage source E_1 is 5V, so the PMOST is off.

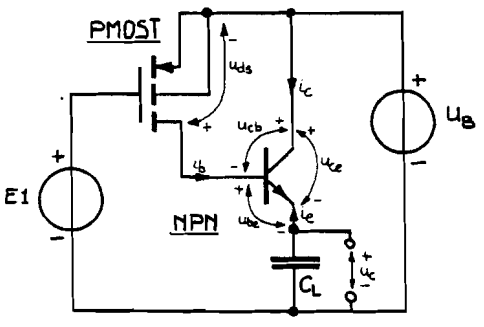


fig. 1.10

Therefore there will be no significant base current i_b. As a consequence the emitter current will be negligible. For $t<0$ we assume the capacitor C_L to be discharged ($u_c=0$). When E1 has been switched to zero, the current i_b first has to charge the base-emitter depletion-region. The bipolar transistor will not turn-on until the base-emitter voltage has reached V_T ($\sim 0.7V$). For $u_{be} > V_T$ the active base region will be charged, which causes an emitter-current to flow, that charges the loadcapacitor C_L.

1.3.1. The turn-on delaytime of the pull-up circuit

Here we start again with the equations (2) and (3), where q_F has been neglected with respect to the depletion-charge. The emitter-current consists of the base-current and the collector-current:

$$i_e = -(i_b + i_c) = -C_e \frac{du_{be}}{dt} \tag{25}$$

with C_e = base-emitter depletion-capacitance

As a second equation for the emitter-current we find:

$$i_e = -C_L \frac{du_c}{dt} \tag{26}$$

From fig. 1.10 we see

$$\frac{du_{cb}}{dt} + \frac{du_{be}}{dt} + \frac{du_c}{dt} = 0 \tag{27}$$

so with (25) and (26) we find for $\frac{du_{cb}}{dt}$:

$$\frac{du_{cb}}{dt} = -\left(\frac{C_L}{C_e + C_L}\right) \frac{du_{be}}{dt} \tag{28}$$

Now the equation of the base current (2) becomes:

$$i_b = \left[C_e + C_c\left(\frac{C_L}{C_e+C_L}\right)\right]\frac{du_{be}}{dt} \qquad (29)$$

During this turn-on delaytime the base-voltage does not exceed V_T and $u_C \approx 0$, so $-U_{ds} < -(U_B - V_{th})$ and the PMOST operates in saturation. This implies, that the basecurrent i_b is constant.

Thus we find the differential equation for u_{be}:

$$\frac{du_{be}}{dt} = \frac{i_{bs}}{C_e + \frac{C_c C_L}{C_e+C_L}} \qquad (30)$$

and its solution

$$u_{be} = \frac{i_{bs}\, t}{C_e + \frac{C_c C_L}{C_e+C_L}} \qquad (31)$$

This equation differs slightly from equation (10), but because C_C and C_e are to the same order of magnitude, we find the same equations, when loading the circuit with a large or small capacitor C_L:

$$u_{be} = \frac{i_{bs}\, t}{C_e + C_c} \qquad (C_L \gg C_e)$$

$$u_{be} = \frac{i_{bs}\, t}{C_e} \qquad (C_L \ll C_e)$$

So the turn-on delaytime will be the same too (see eq. (11) and (14))

$$t_d = \frac{(C_e + C_c)\, V_T}{i_{bs}}$$

and with the parameters of the components used:

$$t_d = \frac{41.9}{W} \text{ ns} \quad (W \text{ in } \mu m)$$

1.3.2. The risetime

As long as $-[U_B-u_{be}-u_c] < -[U_B-V_{th}]$ is valid, the PMOST operates in saturation. After charging the base-emitter depletion-region, we can assume u_{be} to be contantly 0.7V. So we find that, when the outputvoltage u_c exceeds $(V_{th}-0.7)=1.0V$, the PMOST no longer operates in saturation and the basecurrent i_b becomes a function of u_c. We are now going to find a differential equation for the output-voltage u_c as a function of time and base-current i_b. After that, we have to find two solutions: when the output-voltage is below 1V (PMOST in saturation) and when the output-voltage has exceded this voltage (PMOST not in saturation).

As explained in 1.2.2. we can now neglect the changes of the depletion-charge q_{be} with respect to the changes in the storage-charge q_F. Therefore the basic equations for the base- and emitter-current are:

$$i_b = \frac{q_F}{\tau_F} + \frac{dq_F}{dt} - C_c \frac{du_{ce}}{dt} \qquad (15)$$

$$i_e = -\left[(\beta_F+1)\frac{q_F}{\tau_F} + \frac{dq_F}{dt}\right] \qquad (32)$$

Because i_b does not change abrupt during the time C_L is being charged, and because ß is relatively high ($\sim$100), it is allowed to neglect the term $\frac{dq_F}{dt}$ in the equation of the emitter-current. This equation now becomes:

$$i_e = -(\beta_F+1)\frac{q_F}{\tau_F} \qquad (32a)$$

Neglecting the current through resistor R_L we obtain the following equation for the emitter-current:

$$i_e = -C_L \frac{du_c}{dt} \qquad (33)$$

With (33) and (32a) we find:

$$\frac{q_F}{\tau_F} = \frac{C_L}{(\beta_F+1)} \frac{du_c}{dt} \tag{34}$$

$$\frac{dq_F}{dt} = \frac{C_L \tau_F}{\beta_F+1} \frac{d^2u_c}{dt^2} \tag{35}$$

From fig. 1.10 it is clear that $\frac{du_{ce}}{dt} = -\frac{du_c}{dt}$, so we find with (15), (34) and (35) the differential equation for the output-voltage u_c:

$$\frac{d^2u_c}{dt^2} + \frac{1}{\tau_F}\left[\frac{C_L+(\beta_F+1)C_c}{C_L}\right]\frac{du_c}{dt} = \frac{(\beta_F+1)\, i_b}{C_L \tau_F} \tag{36}$$

For u_c 1V the basecurrent is constant and with the initial conditions t=0: u_c=0 and t=0: i_c=0 we find the following solution for the output voltage u_c (See appendix A2):

$$u_c = \frac{(\beta_F+1)\,\delta_2\, i_{bs}}{C_L+(\beta_F+1)C_c}\left[\frac{t}{\delta_2} + 1 - \exp\frac{-t}{\delta_2}\right] \text{ for } 0 \leq u_c < (V_{th}-V_T) \tag{37}$$

$$\text{with } \delta_2 = \frac{C_L \tau_F}{C_L+(\beta_F+1)C_c} \text{ and } i_{bs} = \frac{\beta_a}{2}\frac{W}{L}(u_B-V_{th})^2$$

This solution has great resemblance to equation (20) and now again δ_2 is very small with the components used ($\delta_2 \approx 0.026$ ns).

As we are interested in times to the order of 1ns, equation (37) reduces to:

$$u_c = \frac{(\beta_F+1)\, i_{bs}\, t}{C_L+(\beta_F+1)C_c} \quad \text{for } 0 \leq u_c < (V_{th}-V_T) \tag{38}$$

With the relevant parameters of the components used C_L=50 pF, β_F=100, C_c=0.44 pF (see appendix B1) and eq. (13) for the base-current i_{bs} we obtain:

$$u_c = 0.044\, W\, t \tag{39}$$

u_c in V
W in μm
t in ns

When u_C exceeds $(V_{th}-V_T)$, then the PMOST no longer operates in saturation and as a consequence the basecurrent becomes a function of u_C: (see [1] p. 59)

$$i_b = \beta_\square \frac{W}{L}\left[(u_B - V_{th})(u_B - V_T - u_c) - \frac{1}{2}(u_B - V_T - u_c)^2\right]$$
$$\text{for } (V_{th}-V_T) \leq u_c < (u_B - V_T) \qquad (40)$$

with $\beta_\square$ = gain-factor of square transistor
W = channelwidth of PMOST
L = channellength of PMOST
U_B = power-supply voltage
V_T = turn-on voltage of bipolar transitor (0.7V)
u_C= output-voltage.

This function is illustrated in fig. 1.11.

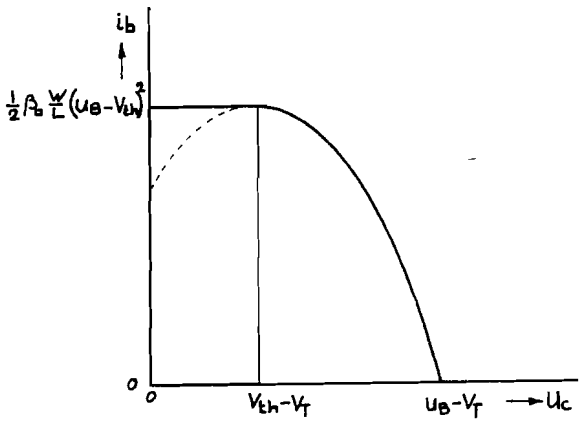


fig. 1.11.

When we insert the equation for the base-current (40) in equation (36) we obtain the differential equation for the output-voltage u_C. Because eq. (40) is a quadratic equation in u_C, there will be no analitical solution for u_C. Therefore we approximate eq. (40) by a linear function in u_C.

This linear function is:

$$i_{b1} = \frac{1}{2}\beta_\square \frac{W}{L}\left(u_B - V_{th}\right)^2 \quad \text{for} \quad 0 \leq u_C < V_o$$

and $$i_{b1} = r\left[u_C - (u_B - V_T)\right] \quad \text{for} \quad V_o \leq u_C < (u_B - V_T) \qquad (41)$$

$$\text{with} \quad r = \frac{\beta_\square \, W \, (u_B - V_{th})^2}{2 \, L \, (V_o + V_T - u_B)}$$

By variation of V_o and consequently r we can choose the function in such a way, that one of the inequalities ($i_{b1} \leq i_b$) and ($i_{b1} \geq i_b$) is always valid. With $V_o = V_{th} - V_T$ we find the function, that meets the first inequality and with this function we will find an upper limit for the rise-time t_r. We will find a lower limit for the risetime, when we choose the tangent on function (40) in the point where $i_b = 0$ for the second part of function (41).

The function gives an upperlimit for the risetime with

$$V_o = V_{th} - V_T$$
$$r = -\frac{\beta_\square \, W}{2 \, L}\left(u_B - V_{th}\right) \qquad (41a)$$

and a lower limit for the rise-time with

$$V_o = \tfrac{1}{2}\left(u_B + V_{th}\right) - V_T$$
$$r = -\beta_\square \frac{W}{L}\left(u_B - V_{th}\right) \qquad (41b)$$

Both functions are shown in fig. 1.12.

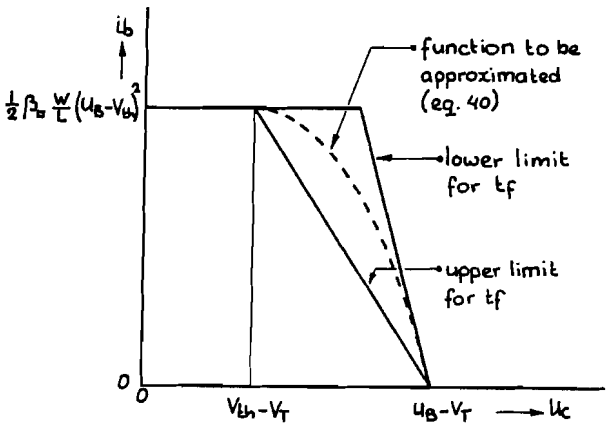


fig. 1.12.

The solution of the differential equation with the first part of function (41) is already given in eq. (38), but it is now valid for $0 \leqslant u_C < V_o$.
With the second part of the function inserted in eq. (36) we obtain a new differential equation:

$$\frac{d^2u_C}{dt^2} + \frac{1}{\tau_F}\left[\frac{C_L+(\beta_F+1)C_C}{C_L}\right]\frac{du_C}{dt} - r\frac{(\beta_F+1)}{C_L\tau_F}u_C = -r(u_B-V_T)\frac{\beta_F+1}{C_L\tau_F} \quad (42)$$

This differential equation is only valid for $V_o \leqslant u_C < (u_B - V_T)$
To solve eq. (42) we have to know two starting conditions. These are:

$$u_C(t_o) = V_o \quad (43a)$$

$$\text{and} \quad \left.\frac{du_C}{dt}\right|_{t_o} = \frac{(\beta_F+1)\ ibs}{C_L+(\beta_F+1)C_C} \quad (43b)$$

$$\text{with} \quad t_o = \frac{[C_L+(\beta_F+1)C_C]V_o}{(\beta_F+1)\ ibs}$$

$$\text{and} \quad ibs = \frac{\beta_\square}{2}\frac{W}{L}(u_B - V_{th})^2 \quad (44)$$

t_o is the moment, on which the output-voltage reaches V_o. The solution of the differential equation (42) has been calculated in appendix A3 and is:

$$u_C = u_B - V_T + \left[\frac{\tau_1}{\tau_2-\tau_1}(u_B-V_T-V_o) + \frac{\tau_1\tau_2}{\tau_2-\tau_1}\frac{(\beta_F+1)\ ibs}{C_L+(\beta_F+1)C_C}\right]\exp\frac{t-t_o}{\tau_1}$$
$$- \left[\frac{\tau_2}{\tau_2-\tau_1}(u_B-V_T-V_o) + \frac{\tau_1\tau_2}{\tau_2-\tau_1}\frac{(\beta_F+1)\ ibs}{C_L+(\beta_F+1)C_C}\right]\exp\frac{t-t_o}{\tau_2} \quad (45)$$

with time constants:

$$\tau_1 = \frac{C_L+(\beta_F+1)C_C}{2r(\beta_F+1)} + \sqrt{\left[\frac{C_L+(\beta_F+1)C_C}{2r(\beta_F+1)}\right]^2 + \frac{C_L\tau_F}{r(\beta_F+1)}} \quad (45a)$$

$$\tau_2 = \frac{C_L+(\beta_F+1)C_C}{2r(\beta_F+1)} - \sqrt{\left[\frac{C_L+(\beta_F+1)C_C}{2r(\beta_F+1)}\right]^2 + \frac{C_L\tau_F}{r(\beta_F+1)}} \quad (45b)$$

With the relevant parameters of the components used $V_{TO}=1.1V$, $k=0.75V^{1/2}$, $\beta_\square = 15\mu A/V^2$, $L=2\mu m$, $\beta_F=100$, $C_C=0.44pF$, $\tau_F=50\,pS$, $C_L=50$ pF and $U_B=5V$. (see appendix B1 and B3) we find for the time-constants:

With upper limit conditions (41a)
$$\tau_1 = -\frac{1}{W}\left[37.8-\sqrt{1428.8-2.0W}\right] \text{ ns}$$
$$\tau_2 = -\frac{1}{W}\left[37.8+\sqrt{1428.8-2.0W}\right] \text{ ns}$$

With lower limit conditions (41b)
$$\tau_1 = -\frac{1}{W}\left[18.9-\sqrt{357.2-1.0W}\right] \text{ ns}$$
$$\tau_2 = -\frac{1}{W}\left[18.9+\sqrt{357.2-1.0W}\right] \text{ ns}$$

When W is to the order of 30 um, τ_1 is very small with respect to τ_2 and has a value of approximately 27 ps.

Writing down eq. (45) in a different way, it becomes clear that we can leave out part of the terms:

$$u_C = u_B - V_T - \frac{\tau_2}{\tau_2-\tau_1}(u_B-V_T-V_0)\exp\frac{t-t_0}{\tau_2}\left[1-\frac{\tau_1}{\tau_2}\exp\frac{\tau_2-\tau_1}{\tau_2\tau_1}(t-t_0)\right]$$
$$-\frac{\tau_1\tau_2}{\tau_2-\tau_1}\frac{(\beta_F+1)i_{bs}}{C_L+(\beta_F+1)C_c}\exp\frac{t-t_0}{\tau_2}\left[1-\exp\frac{\tau_2-\tau_1}{\tau_2\tau_1}(t-t_0)\right]$$

The time-constant $\frac{\tau_2\tau_1}{\tau_2-\tau_1}$ of the exponential term between brackets can be approximated by τ_1 when $\tau_1 \ll \tau_2$ and as we are interested in times $(t-t_0)$ to the order of nanoseconds, the exponential terms between brackets can be neglected with respect to one.
With the parameters of the components used we find also:

$$(u_B-V_T-V_0) \gg \left|\frac{\tau_1(\beta_F+1)i_{bs}}{C_L+(\beta_F+1)C_c}\right| \qquad (46)$$

Worst case we find:
$$u_B-V_T-V_0 \approx 1.65V$$
$$\frac{\tau_1(\beta_F+1)i_{bs}}{C_L+(\beta_F+1)C_c} \approx 35\,mV$$

When the approximations mentioned above has been applied, then the solution of the differential equation (45) reduces to

$$u_c = u_B - V_T - (u_B - V_T - V_0)\exp\frac{t-t_0}{\tau_2} \quad \text{for } t \gg t_0 \qquad (47)$$

Fig. 1.13 shows the output-voltage u_c as a function of time.

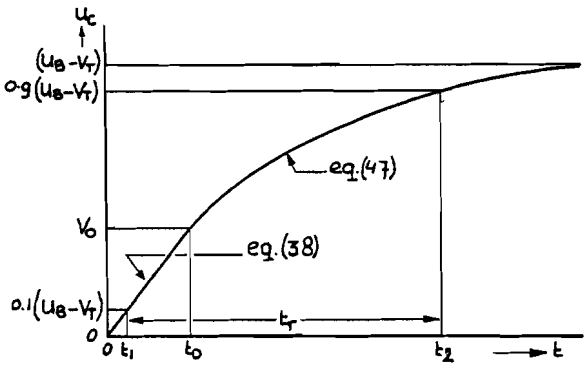


fig. 1.13

Now it is possible to determine the risetime t_r. The times t_1 and t_o can be calculated with eq. (38) and t_2 with eq. (47)

$$t_1 = 0.1\,(u_B - V_T)\,\frac{C_L + (\beta_F+1)C_c}{(\beta_F+1)\,i_{bs}} \qquad (48a)$$

$$t_o = V_o\,\frac{C_L + (\beta_F+1)C_c}{(\beta_F+1)\,i_{bs}} \qquad (48b)$$

$$t_2 = t_o + \tau_2\,\ln\left[\frac{0.1\,(u_B - V_T)}{u_B - V_T - V_o}\right] \qquad (48c)$$

$$t_r = t_2 - t_1 = \left[V_o - 0.1(u_B - V_T)\right]\frac{C_L + (\beta_F+1)C_c}{(\beta_F+1)\,i_{bs}} + \tau_2\,\ln\left[\frac{0.1\,(u_B - V_T)}{u_B - V_T - V_o}\right] \qquad (48)$$

With the parameters of the components used and with the width of the PMOST to the order of 30 µm it is allowed to reduce the time constant τ_2 to:

$$\tau_2 \approx \frac{C_L + (\beta_F+1)C_c}{r\,(\beta_F+1)} \qquad (49)$$

Inserting the parameters in eq. (48d) we find with the conditions (41a) and (41b) an upper limit and a lower limit of the risetime:

$$t_{r\,max} = \frac{167}{W} \text{ ns} \quad (W \text{ in } \mu m) \tag{50a}$$

$$t_{r\,min} = \frac{102}{W} \text{ ns} \quad (W \text{ in } \mu m) \tag{50b}$$

The turn-on delay time t_d of the pull-up circuit and the limits of the risetime t_r have been calculated for W=26, 28,30,32,34 and 36 µm. The results are shown in table 1.2, fig. 1.14 and fig. 1.15.

table 1.2.

W [µm]	26	28	30	32	34	36
t_d [ns]	1.61	1.50	1.40	1.31	1.23	1.16
t_{rmin} [ns]	3.92	3.64	3.39	3.18	3.00	2.83
t_{rmax} [ns]	6.43	6.00	5.57	5.22	4.92	4.64

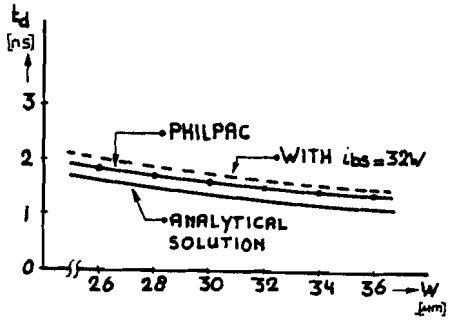


fig. 1.14

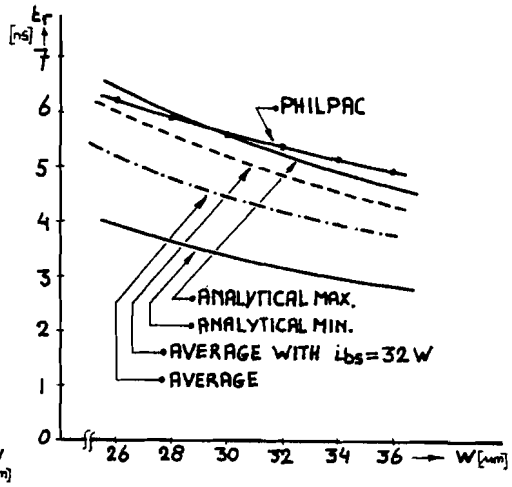


fig. 1.15.

The circuit in fig. 1.10 has been simulated with PHILPAC. The turn-on delaytime t_d and the risetime t_r have been calculated by this program and they are drawn too in fig. 1.14 and fig. 1.15 respectively.
Comparing the analytical results with the results obtained with the PHILPAC-simulation we notice, that the turn-on delay-time t_d corresponds very well. Unfortunately the lower limit and upper limit for the risetime are not close enough to be usefull in giving an approximation. When we take the arithmetical average of both limits, then the approximation gives a reasonable result, but taking this average is without proper foundation. The delay-time and risetime have been calculated too with the corrected base current also used in the last part of section 1.2.2.
With the corrected basecurrent ($i_{bs}=32*W$), we find for the delay time $t_d=53/W$ nS and for arithmetical average of the risetime $t_r=156/W$ nS. In this case the base-current corresponds very good to the PHILPAC simulation and the analyticial solution gives a better agreement with the PHILPAC-results.

1.4. Conclusion

The calculations in this chapter concerning the turn-on delay-times and the falltime are relatively simple and the analytical solutions have good correspondence with the numerical results obtained with the circuit analysis program PHILPAC. In the first part of the region, in which the output voltage u_c starts to fall, the neglects in the equations are not yet valid and consequently the calculations do not give a fair description during this interval. The results obtained with the linear approximations, to calculate the risetime, are a little bit disappointing. To get better results, the approximation should consist of more linear intervals with different gradients.

1.5. The extended models of the MOS-transistors

In the preceding sections we have assumed the MOS transistors to be only a gate with ideal source and drain connections. In the practical case, the drain and source connections consist of a P-N diode. The gate also represents a capacitance between gate connection and substrate. Therefore in the next chapters the simulations with the circuit analysis program PHILPAC have been performed with extended models of the MOS transistors. These models are shown in fig. 1.16.

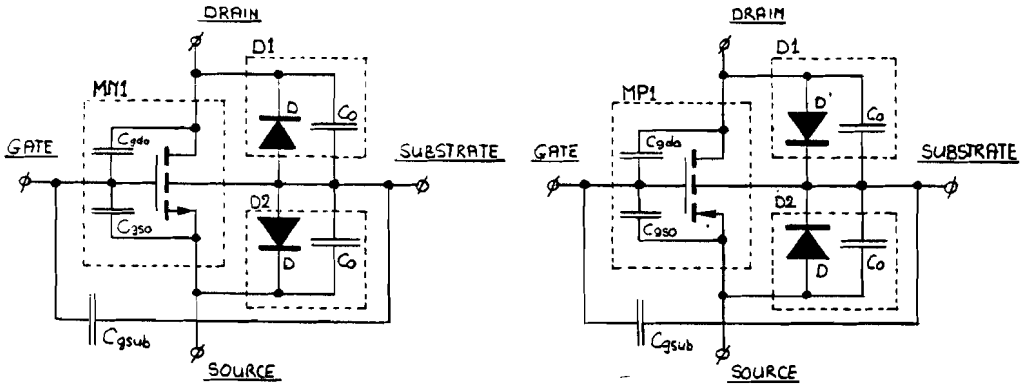


fig. 1.16.

The models are extended versions of the level 7 MOS model in PHILPAC. In the center we see the MOST with its gate overlapp capacitances C_{gdo} and C_{gso} as described in level 7. The first addition is the gate-substrate capacitance C_{gsub}. Secondly the drain-substrate and source-substrate diodes hav been added with their depletion capacitances C_O. Especially the drain-substrate diode is important, because sometimes th drainvoltage will drop below the substrate-voltage or above N-well voltage (substrate of PMOST). The source-substrate diode is only important in circuits where an NMOST has been put between the base and the collector of a bipolar transistor. In all other cases this diode has no influence, because then the source is connected to the substrate (or N-well). The various parameters have been related to the MOS transistor width W and are listed in appendix B3.

1.6. High injection in the base of the bipolar transistor

The collectorcurrent in a bipolar transistor is caused by the injection of minority carriers in the active base region on the emitterside. In the base of an NPN transistor, the minority carriers are electrons and when the collectorcurrent density is low, the concentration of electrons is still negligible with respect to the hole-concentration. In this situation the hole-concentration can be assumed to be constant and undependent on the minority-injection. These are the normal working conditions of a bipolar transistor. Where the concentration of the injected minority carriers (electrons) approaches or exceeds the dope-concentration of the base, the assumptions mentioned above are not valid and the emitter efficiency decreases. Consequently the current gain factor decreases (see 2 p. 139-143). To avoid this situation we have to fix a limit to the minority-injection. As the colletor current density is linearly dependent on the minority-injection, this restriction also gives a maximum for the current density. The collector current density is equal to (see [1] p. 43 and [3] p. 109).

$$J_c = q * D_n * n_p(o) / W_B$$

with : J_c = collector-current density
D_n = diffusion-constant of electrons in the active base
$n_p(0)$= electron-density on the emitterside of the active base
W_B = width of the active base.

When we put the limit for the minority-injection at the half the base dope N_A, the maximum collector current becomes:

$$I_{cmax} = J_{cmax} A_e = q D_n \frac{N_A}{2} \frac{A_e}{W_B}$$

with A_e = emitter area
N_A = base dope

Practical values for the bipolar NPN transistors in the BIMOS

process are:

$N_A = 3*10^{17}$ cm^{-3}
$W_B = 0.2$ µm
$D_n = 12$ cm^2/s (see [2] p. 29).

With these values we find:

$$I_{cmax} = 144 * A_e \ \mu A \quad (\text{with } A_e \text{ in } \mu m^2)$$

The maximum collector current needed to discharge a capacitor of 50 pF in 5nS is approximately 50 mA, so the emitterarea should be at least 350 µ^2 to avoid high-injection effects.
At the time the designs of the circuits were made, the values for N_A and W_B differed slightly with the ones listed above. Then we found $I_{cmax}=64*Ae$ µA and therefore the emitter of the bipolar transistor has an area of 800 µ^2 instead of 350 µ^2.

2. HIGH PERFORMANCE BIMOS DRIVER CIRCUITS

2.1. Introduction

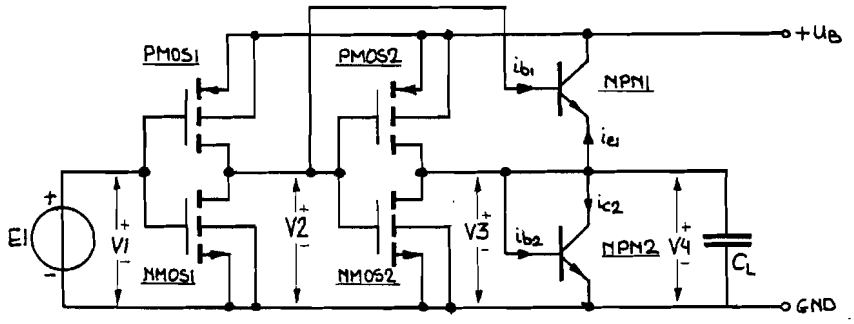
A driver-circuit will consist of the combination of a pull-up circuit and a pull-down circuit. Sometimes for one of the two a passive network is chosen, for example a resistor or a current-source. The disadvantage of this method is the relatively high power-consumption, for the active circuit has to supply the load as well as the passive network.
The BIMOS drivers in this chapter all exist of two active bipolar transistors, which are driven by a CMOS circuit. The circuits are designed to switch a capacitive load of 50 pF between 0V and 5V with rise- and falltimes of 5 ns. The pull-up and pull-down-circuits are basicly the same circuits already given in fig. 1.10 and fig. 1.1. respectively. Because the circuits are both turned on, when the input voltage becomes low, the two inputs have to be operated in opposite phase. Therefore an inverter should be included, which leads to a circuit like the one shown in fig. 2.1. The pulse-response of the circuit has been calculated with the circuit analysis program PHILPAC. With those results the circuit is examined and several improvements have been made.

2.2. The initial circuit

In designing a BIMOS driver circuit one has the opportunity to choose some parameters of the MOS- and bipolar transistor. These are the parameters, which depend on the geometry of the transistor. For the MOS transistor these are the width and length of the channel and the drain and source capacitances. To have a high current-gain factor β, the length of the channel should be as short as possible. Therefore the length is chosen to be 2µm, which is the minimum width of the polysilicon in the C500 process. The width of the MOS-transistor can be choosen to obtain the specified rise- or fall-time.

As the drain- and source-capacitors are parasitic elements, which slow down the operation of the circuit, these capacitors should be as small as possible. This has been obtained by designing the drain- and source-regions as narrow as permitted by the design-rules of the C500 process. The bipolar transistor has been designed in such a way, that high injection effects have been avoided (see chapter 1). With this restriction we obtain a minimum emitter area. For minimum delay times the base-emitter depletion-capacitance C_e should be small, so C_e is determined by the minimum emitter area. For fast switching times the base-collector depletion-capacitance C_c should be small, so the base diffusion region should be as small as possible.
For this reason the bipolar transistor has been designed with a single base connection. The resistance of the MOS transistor, which drives the bipolar transistor is rather high, compared to the base resistance, so a double base contact would show no profit. The base diffusion should also be chosen to provide a small collector resistance. Thus all the parameters of the bipolar transistor are determined mainly by the minimum emitter-area.

The first BIMOS driver circuit we are going to examine is called circuit 1 and is shown in fig. 2.1.



PMOS1 : W = 37 µm NMOS : W = 7 µm C_L = 50 pF
PMOS2 : W = 37 µm NMOS : W = 7 µm U_B = 5V

fig. 2.1. Circuit 1

PMOS1 and PMOS2 provide the base-currents of NPN1 and NPN2 respectively in the same way as in the preceding chapter. To prevent the bipolar transistors from being switched on simultanously for some time, NMOS1 and NMOS2 drain the storage-charge, so the bipolar transistors will be switched of rapidly. The combination PMOS1 and NMOS1 acts like an inverter, so driving PMOS2 and NMOS2 by this inverter, the bipolar transistor NPN2 will be switched on and off in opposite phase with respect to NPN1.
When NPN2 is switched on, the collector-base voltage will become negative, when the load-capacitor C_L is almost discharged. This causes the transistor to operate in the saturation-mode (see [2] p. 175). To avoid this situation, a Schottky diode D1 has been added to the circuit. Because the voltage drop across the Schottky diode is much lower than across the base-collector diode when forward biased, the drain current of PMOS2 will flow mainly through the Schottky diode. This causes the basecurrent to decrease and the total storage-charge will be much less than without diode D1. Now the storagecharge is smaller, the transistor will be switched off faster, which decreases switching time and power consumption [4] .

Circuit 1 has been simulated with the circuit analysis program PHILPAC. At t=0 the input voltage source E1 has been switched within 1ns from 5V to 0V and at t=21 ns this source has been switched to 5V again. In fig. 2.2 the voltages V1, V2, V3 and V4 are shown as has been calculated by the computer program. Figure 2.3. shows the base-currents i_{b1} and i_{b2} and fig. 2.4. shows the emitter-current i_{e1} and collector-current i_{c2} of NPN1 and NPN2 respectively.

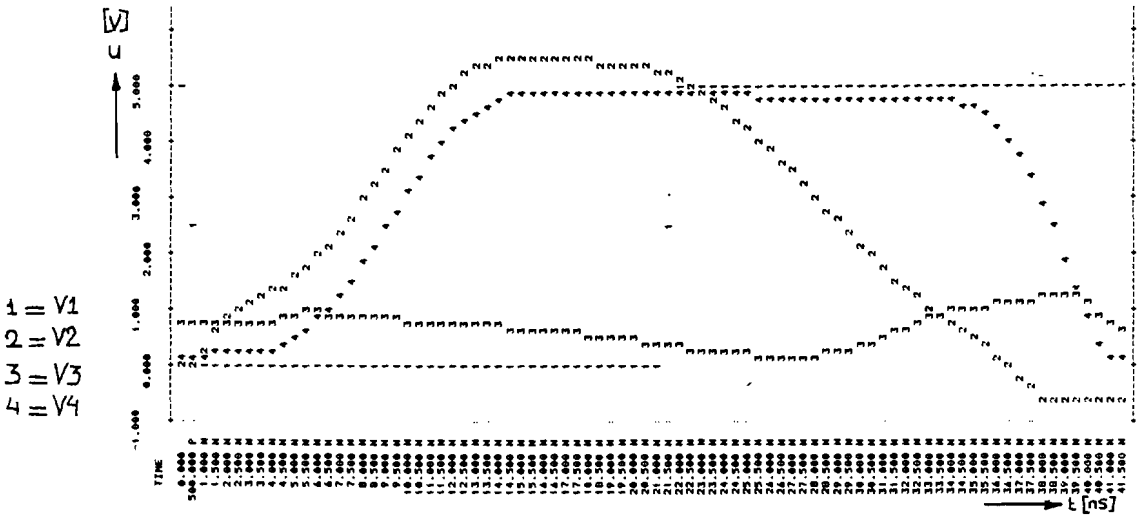


fig. 2.2. The voltages V_1, V_2, V_3 and V_4 as functions of time in circuit 1.

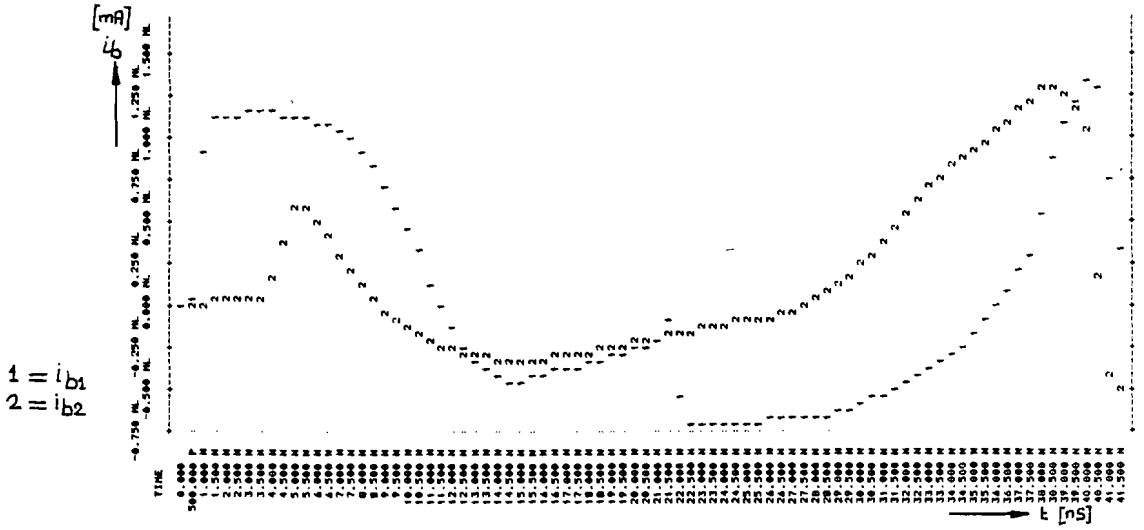


fig. 2.3. The base-currents i_{b1} and i_{b2} as functions of time in circuit 1.

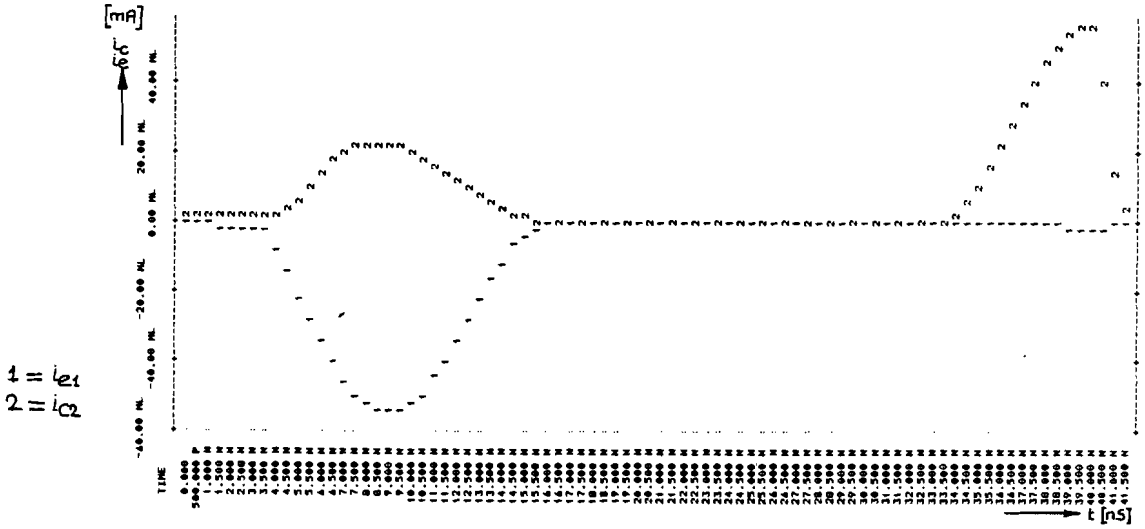


fig. 2.4. The emittercurrent i_{e1} and the collector-current i_{c2} as functions of time in circuit 1.

When we examine fig. 2.2. the first to notice is the long delay-time of the output-voltage V4. Taking a closer look to the other voltages, we see that this is caused by the slow decay of voltage V2.

When the output voltage is high and the input voltage V1 is switched to 5V, NMOS1 is switched on and discharges the input-capacitance of the bipolar transistor. This is formed by the series capacitance of the load-capacitor and the base emitter depletion-capacitor, together with the base-collector depletion capacitor. With C_e=2pF, C_c=0.44 pF and C_L=50 pF this becomes 2.4 pF. This capacitance is rather high and that is the reason, why V2 decreases slowly. Transistor PMOS2 starts to switch on the bipolar transistor NPN2 only when V2 has fallen below (U_B-V_{th}). This will be at approximately 3.3V. In fig. 2.2 at t=27 ns we see that the base-emitter voltage V3 increases, when V2 drops below 3V. In fig. 2.3 at the same time the base-current i_{b2} starts increasing. At t=27 ns transistor NMOS2 is still turned on and therefore i_{b2} starts increasing rather slowly. When V2 decays, this increase is accelerated. When the base-emitter voltage has exceded approximately 1V (V_T + voltage-drop across the base-resistance) the bipolar transistor is turned on and discharges the load-capacitor C_L.

When the driver-circuit is switched to charge the capacitor C_L, the voltage V2 increases rather fast, because PMOS1 charges the depletion-capacitors of the bipolar transistor NPN1. Exceding the turn-on voltage V_T, NPN1 is turned on and after that the voltage V2 will remain about 1V above the output voltage, because the base-emitter diode is forward biased. Initially the load-capacitor is discharged, so V2 will be low and PMOS2 with NPN2 will still be turned on. Therefore a part of the emitter-current i_{e1} is drained away through NPN2 and doesnot contribute to the charge of capacitor C_L. In fig. 2.4. we can see this increase of i_{c2} between t=4 ns and t=15 ns. This effect causes extra-power consumption and a rather high rise-time of the output-voltage.

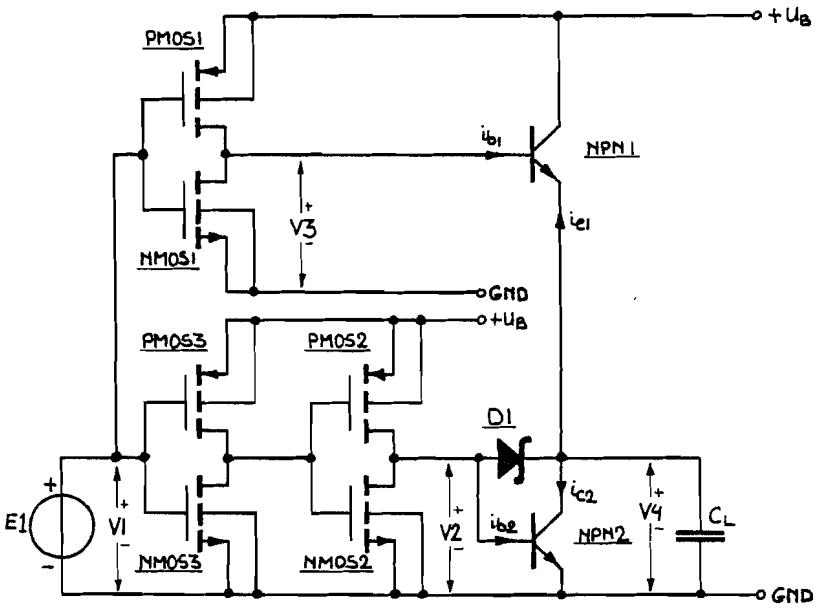
With PHILPAC some characteristic switching-times have been calculated too. In the first place the time t_{dr} has been determined, in which the output-voltage rises to 0.5V, after the input has been switched from 5V to 0V. This time is a measure of the delay before rise. Secondly the rise-time t_r has been determined. The delay-time before fall t_{df} has been obtained as the third switching-time. In this time the output-voltage falls to 4.2V after the input has been switched from 0V to 5V. The last time obtained with PHILPAC is the fall-time t_f. Finally PHILPAC determines the mean power-dissipation during 40 ns, in which time a full switching-cycle has been completed. The properties of circuit 1 are given in table 2.1.

table 2.1. Circuit 1

t_{dr}	[ns]	5.1
t_r	[ns]	7.0
t_{df}	[ns]	15.1
t_f	[ns]	4.6
mean pwr	[mW]	50.7

2.3. Improvement of the power-consumption and the delaytime

The drawbacks of circuit 1 are both caused by the relatively slow changing V2. To improve the switching qualities of the circuit, PMOS2 and NMOS2 should not be driven by PMOS1 and NMOS1, but by another inverter circuit. This leads towards the second circuit, which has been examined and is shown in fig. 2.5.



PMOS1	: W = 37μm	NMOS1	: W = 7μm	C_L	= 50 pF
PMOS2	: W = 37μm	NMOS2	: W = 7μm	U_B	= 5V
PMOS3	: W = 7μm	NMOS3	: W = 7μm		

fig. 2.5. Circuit 2

The inverter added to the circuit has been formed with PMOS3 and NMOS3. Because this inverter does not have to drive a bipolar transistor, the width of PMOS3 can be small. Circuit 2 has been simulated with PHILPAC and the results for the voltages and currents as functions of time are shown in fig. 2.6., 2.7. and 2.8.
The two disadvantages of the previous circuit (circuit 1) now almost have disappeared. In fig. 2.6. we see, that the base-emitter voltage V3 increases almost immediately, when the input is switched from 0 to 5V, so the remaining delay is the turn-on delay of the bipolar transistor.
With fig. 2.8 it becomes clear, that the improvement also holds for the power-consumption. During the time the load-capacitor C_L is being charged, the base-current i_{b2} never becomes positive and the collector-current i_{c2} does not increase significantly. Therefore the risetime is shortened and the power-consumption has been decreased.

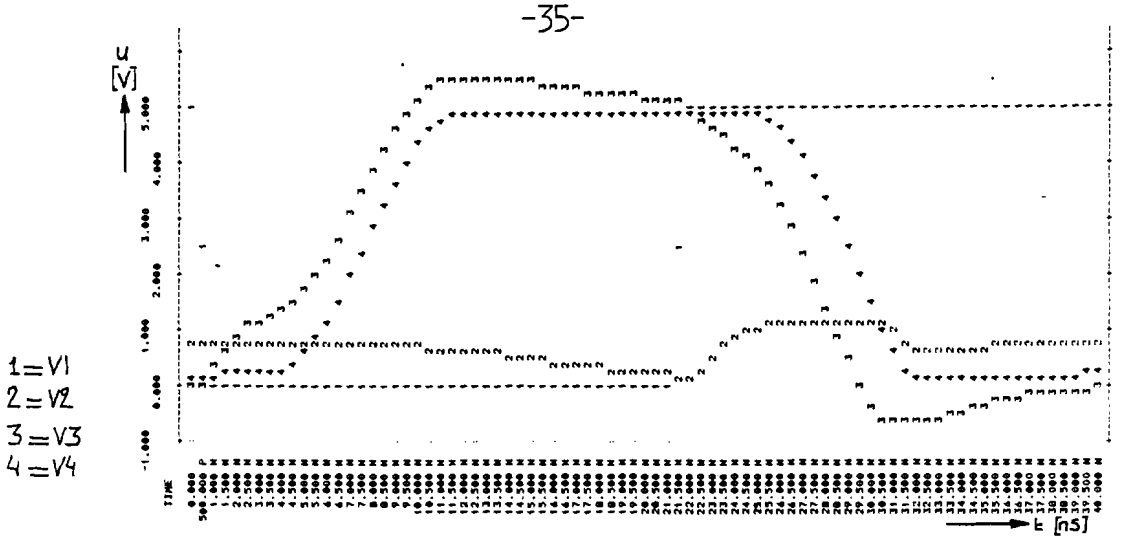


fig. 2.6. The voltages V_1, V_2, V_3 and V_4 as functions of time in circuit 2

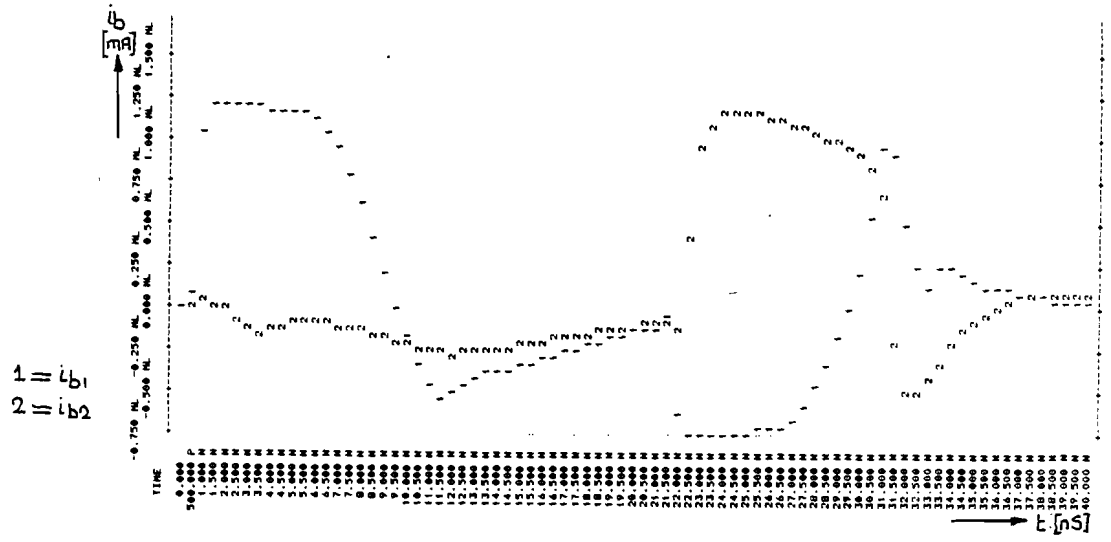


fig. 2.7. The base-currents i_{b1} and i_{b2} as functions of time in circuit 2.

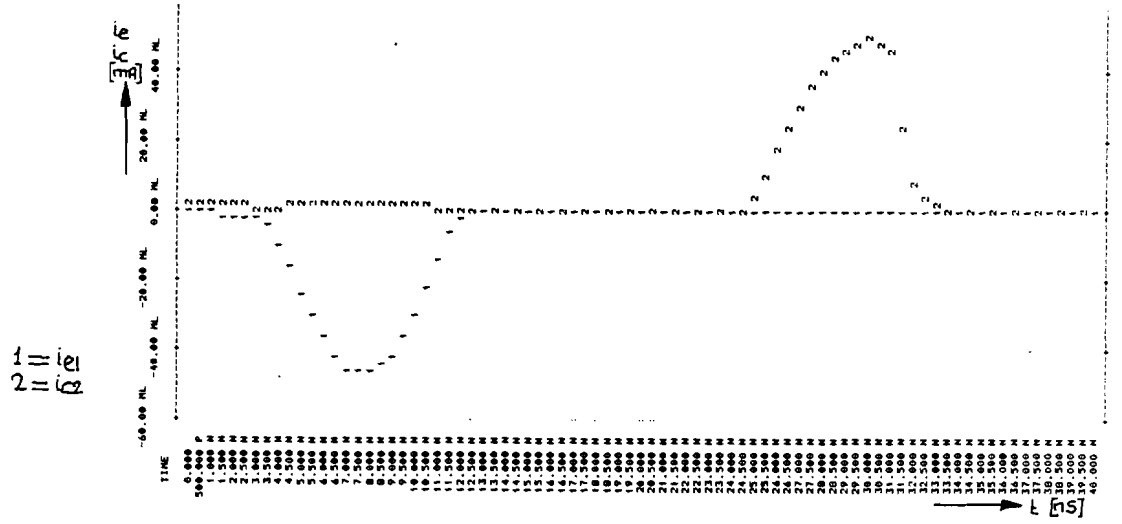


fig. 2.8. The emitter-current i_{e1} and the collector-current i_{c2} as functions of time in circuit 2.

In table 2.2. the switching-times of circuit 2 are listed together with the mean power-consumption during 40 ns.

table 2.2. Circuit 2

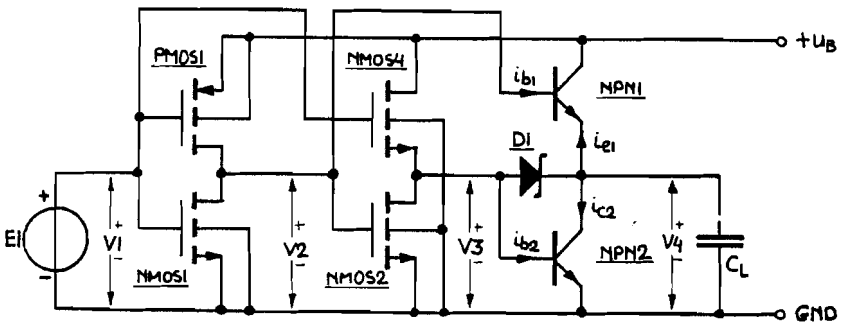
t_{dr}	[ns]	4.8
t_r	[ns]	5.1
t_{df}	[ns]	5.8
t_f	[ns]	4.6
mean pwr	[mW]	34.8

Comparing the results of circuit 1 and circuit 2, the improvements are rather impressive. The disadvantages of circuit 1, the long delay-time t_{df} and the high power-dissipation, are both decreased with circuit 2. In table 2.3 the improvements have been related to the properties of circuit 1.

table 2.3. Improvements of circuit 2 related to circuit1.

t_{dr}	improved by 6%	(0.3 ns)
t_r	improved by 27%	(1.9 ns)
t_{df}	improved by 62%	(9.3 ns)
t_f	improved by 0%	(0 ns)
mean pwr	improved by 31%	(15.9 ns)

The major point in avoiding a long delaytime, when discharging the load capacitor is, that transistor PMOS2 should not be driven by PMOS1 and NMOS1. In circuit 2 (see fig. 2.5) this is achieved by driving PMOS2 by an extra inverter with PMOS3 and NMOS3.
When we replace PMOS2 by an NMOST, this transitor can be driven by E1 directly. This circuit is given in fig. 2.9.



PMOS1 : W = 37µm NMOS2 : W = 7µm C_L = 50 pF
NMOS1 : W = 7µm NMOS4 : W = 17µm U_B = 5V

fig. 2.9. Circuit 3

In circuit 3 NMOS4 is turned on at once, when E1 becomes high and because NMOS1 has to drive one transitor less, the voltage V2 will fall a little faster. Therefore NMOS2 will be turned off faster too. Both effects cause the delaytime to be shortened.

When E1 falls to zero, the transistor NMOS4 is turned off immediately. PMOS1 drives the bipolar transistor NPN1 and when V2 exceeds approximately 1V NPN1 starts charging the loadcapacitor C_L. The voltage V2 stays about 1V above the output-voltage. Therefore NMOS2 is not yet switched on completely, when the output starts rising and the capacitance of the Schottky diode is able to provide a positive base-current ib_2 to transistor NPN2. This causes an undesirable collector-current i_{ce}. In circuit 1 this collector-current was mainly caused by the delayed and slow turn-off of PMOS2. Thus it is clear that circuit 3 will show a decreased current i_{c2} during the charge of load-capacitor C_L.
Circuit 3 has been simulated with PHILPAC and the various voltages and currents indicated in fig. 2.9 are shown as functions of time in fig. 2.10, 2.11 and 2.12.

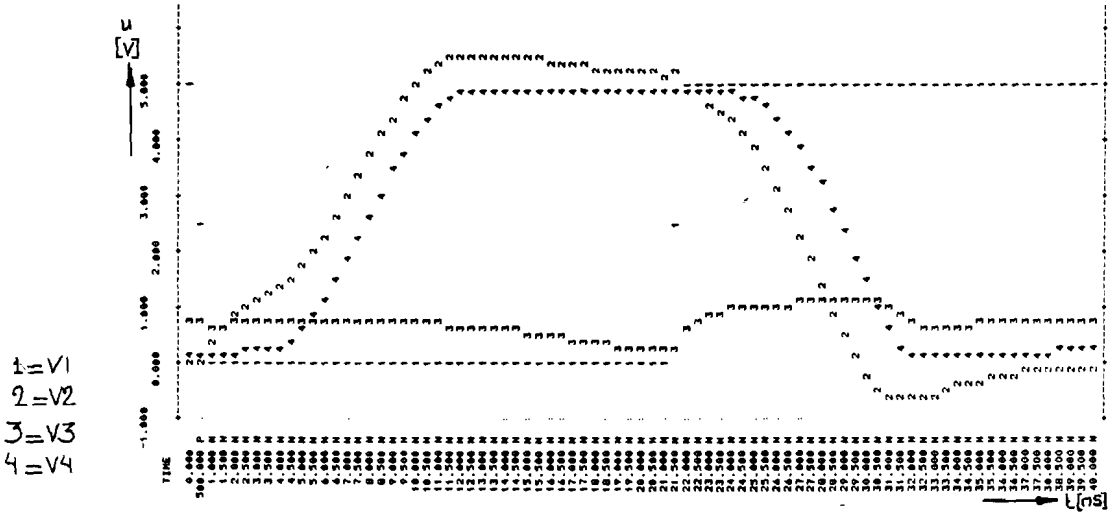


fig. 2.10. The voltages V1, V2, V3 and V4 as functions of time in circuit 3.

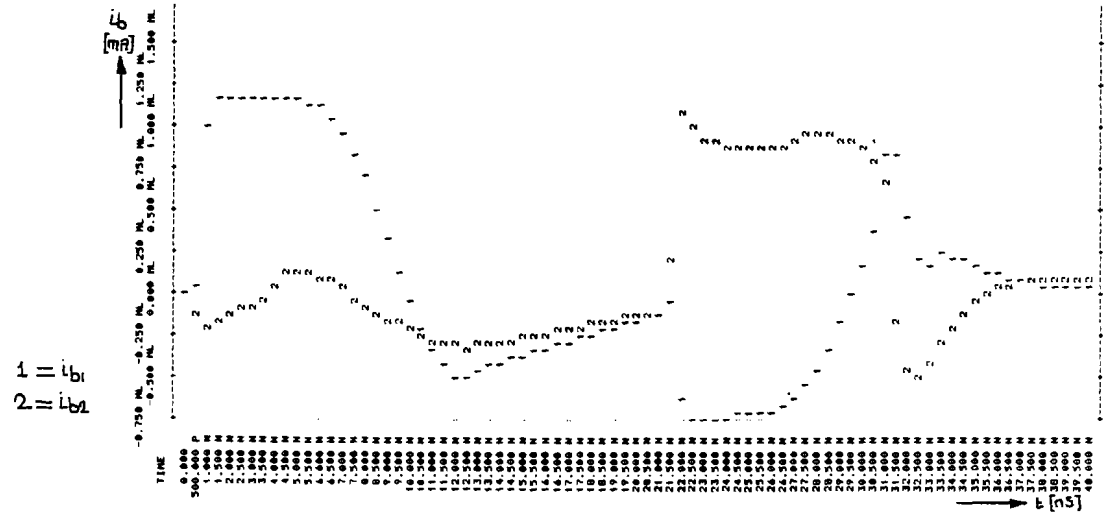


fig. 2.11. The base-currents i_{b1} and i_{b2} as functions of time in circuit 3.

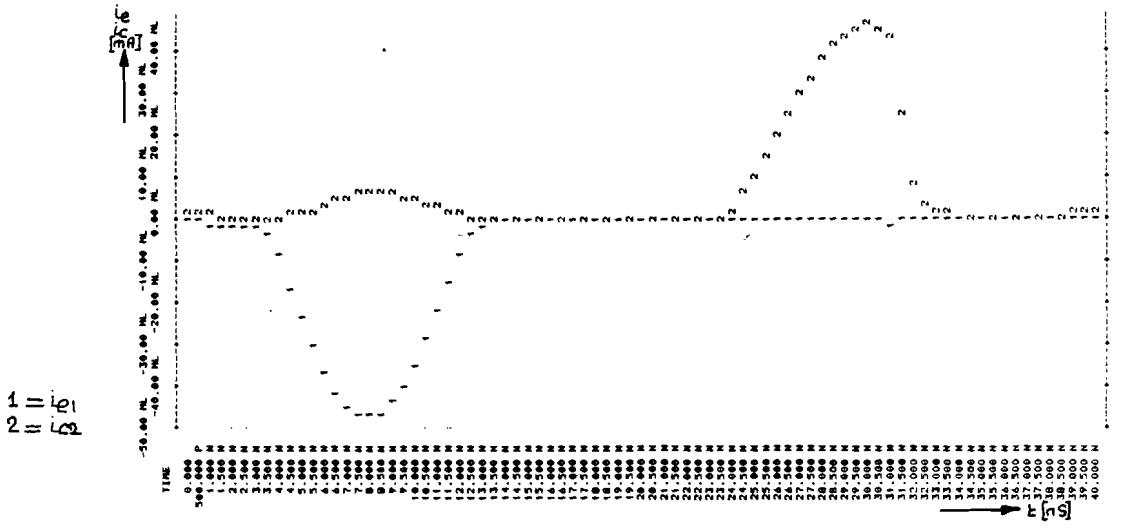


fig. 2.12. The emittercurrent i_{e1} and the collector-current i_{c2} as functions of time in circuit 3.

The time-diagram of fig. 2.10 shows, that the delaytime has been reduced. In fig. 2.12. we see, that the maximum collector-current of NPN2, when charging the loadcapacitor, has been reduced from $\sim$22 mA to $\sim$ 7 mA. Due to the latter effect the maximum collector-current of NPN1 can be significantly smaller to obtain the same risetime and therefore the power dissipation will be reduced with respect to circuit 1. In table 2.4. some characteristic values are given, which have been calculated with the PHILPAC program.

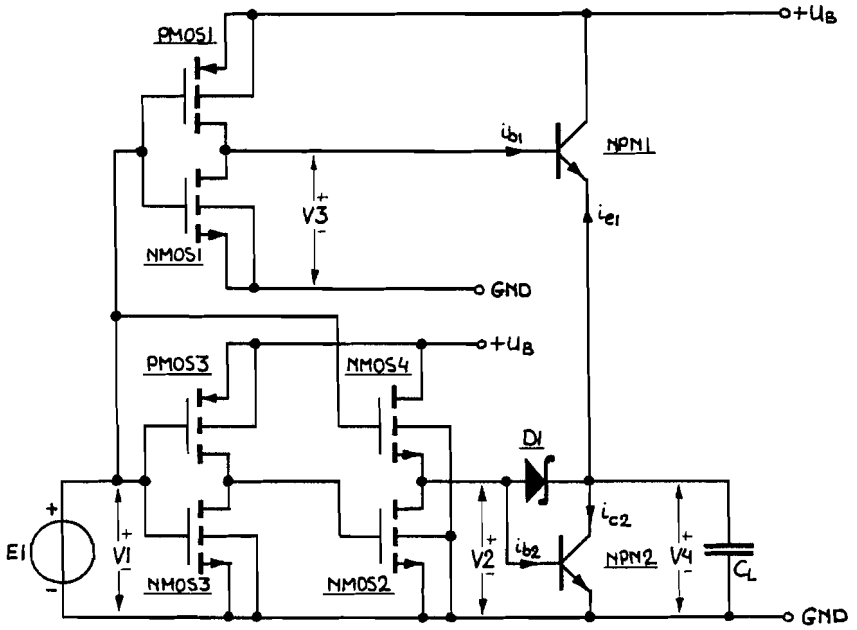
table 2.4. Circuit 3

t_{dr}	[ns]	4.8
t_r	[ns]	5.5
t_{df}	[ns]	5.4
t_f	[ns]	5.1
mean pwr	[mW]	37.3

Comparing the results in table 2.4. with those of circuit 2 in table 2.2, we see in the first place that the delaytime t_{df} before discharging the load-capacitor has been

reduced, while the falltime t_f has been increased. This is caused by the fact, that the current through NMOST decreases, when the base-emitter voltage increases. This can be seen clearly in fig. 2.11, where i_{b2} starts rather high and decreases when the voltage V3 increases. Therefore the base-emitter depletion-capacitor is charged with a current higher than the basecurrent, that causes the bipolar transistor to discharge the loadcapacitor. In circuit 2 the current through PMOS2 remains constant, so the ratio delaytime:falltime of circuit 3 will be smaller than that of circuit 2. The second difference between the two circuits is the longer risetime of the latter. This, in combination with the higher power-dissipation, is caused by the slow turn-on of NMOS2, as explained before.

The ideas used in circuit 2 and circuit 3 can be combined in one circuit, which is drawn in fig. 2.13. The difference of circuit 4 with circuit 3 is the additional inverter consisting of PMOS3 and NMOS3, that only drives NMOS2.



PMOS1 : W = 37µm NMOS2 : W = 7µm C_L = 50 pF
PMOS3 : W = 7µm NMOS3 : W = 7µm U_B = 5V
NMOS1 : W = 7µm NMOS4 : W =17µm

fig. 2.13. Circuit 4

The results obtained by simulation with PHILPAC are shown in fig. 2.14, 2.15 and 2.16.

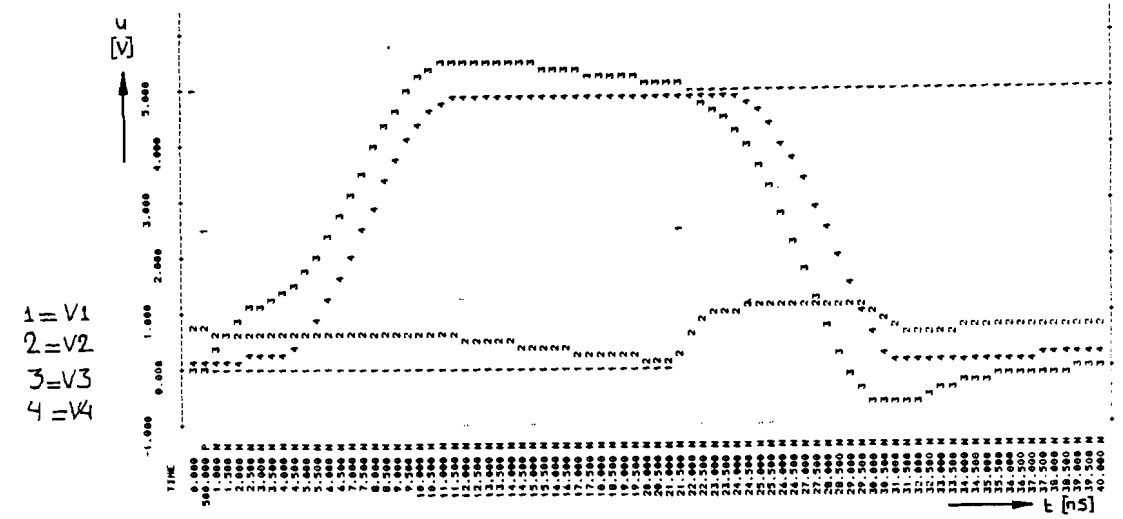


fig. 2.14. The voltages V1, V2, V3 and V4 in circuit 4

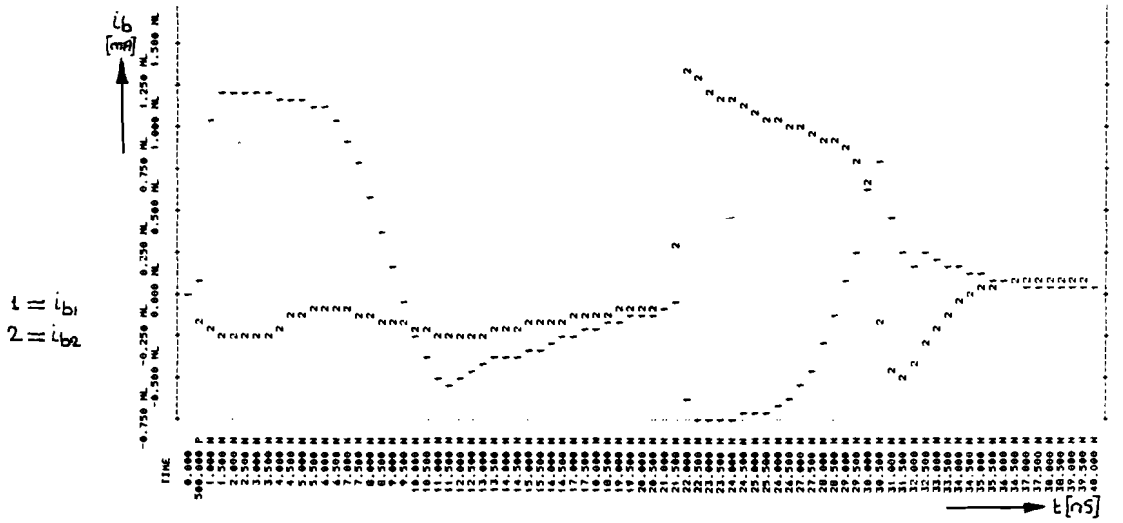


fig. 2.15. The base-currents i_{b1} and i_{b2} in circuit 4

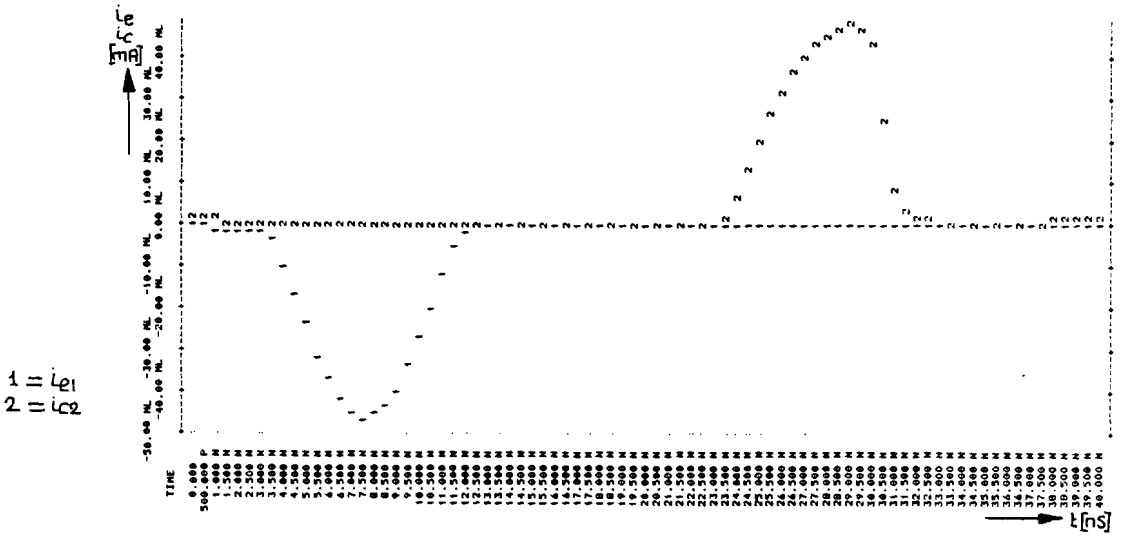


fig. 2.16. The emitter-current i_{e1} and the collector-current i_{c2} in circuit 4

With this addition, we expect a faster turn-on of the bipolar transistor NPN2, because NMOS2 is turned-off faster, which causes a higher basecurrent i_{b2}.
Secondly we expect a lower dissipation, because NMOS2 is switched on faster. This will also cause a shorter risetime for the output-voltage.
The results obtained by simulation are shown in fig. 2.14, 2.15 and 2.16.
In figure 2.16 we see, that when the load-capacitor is being charged, the collectorcurrent i_{c2} remains very low. This is comparable with the results obtained by the simulation of circuit 2 and is an improvement of circuit 3.

With PHILPAC some specific switching-times of circuit 4 have been calculated together with the mean power-dissipation. They are listed in table 2.5.

table 2.5. Circuit 4

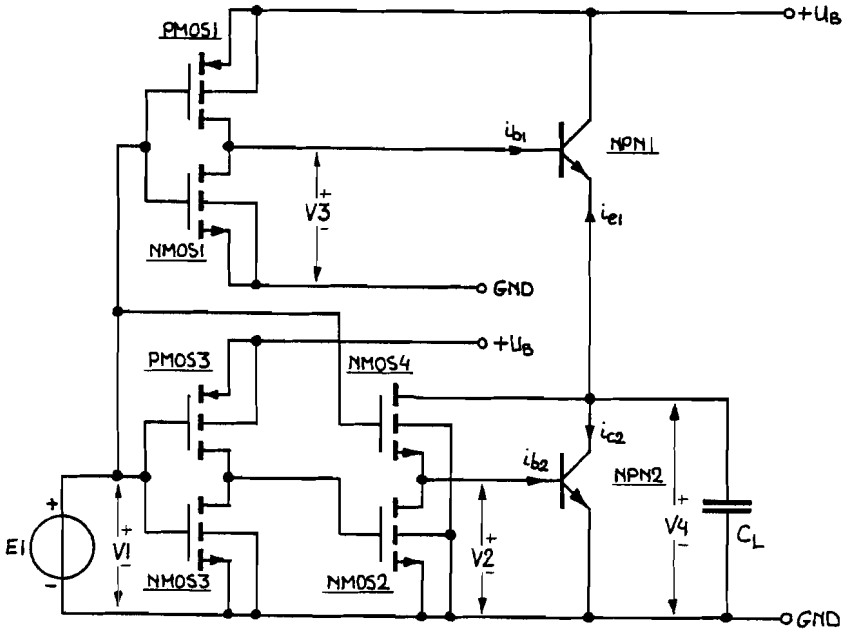
t_{dr}	[ns]	4.7
t_r	[ns]	5.0
t_{df}	[ns]	4.7
t_f	[ns]	4.7
mean pwr	[mW]	33.6

Comparing the properties of circuit 4 in table 2.5 with those of circuit 3 in table 2.4, we see a rather remarkable improvement. The delaytime before fall t_{df} and the falltime t_f have both become better, which can be explained by the faster turn-off of NMOS2. The risetime t_r, together with the mean power-dissipation, have been improved, because NMOS2 turns on faster.

2.4. Another way of avoiding saturation in the bipolar transistor

In the circuits described so far, the bipolar transitor NPN2 is guarded against saturation by the Schottky diode D1. When the collector voltage falls below the base voltage, the Schottky diode is forward-biased and takes over almost all the current from the driving-circuit. Therefore the base-current decreases and the active base region is less charged with minority carriers.

Circuit 3 and circuit 4 offer a second possibility of avoiding saturation. When we leave out the Schottky diode and connect the drain of NMOS4 to the output instead of to the power-supply, then the drain-source voltage of this MOS-transistor decreases, together with the output-voltage. The base-current will decrease too and becomes zero, when the output-voltage equals the base-potential. Therefore the base-collector diode of the bipolar transistor is never biased forward and thus the transistor never operates in saturation. This modification has been adapted to circuit 4 in fig. 2.13. This new circuit is given in fig. 2.17.



PMOS1 : 37µm NMOS1 : 7µm NMOS3 : 7µm C_L = 50 pF
PMOS3 : 7µm NMOS2 : 7µm NMOS4 : 17µm U_B = 5V

fig. 2.17. Circuit 5

Circuit 5 in fig. 2.17 will act almost the same as circuit 4 with a schottky diode, except that the falltime will be longer as a consequence of the decreasing base-current. This circuit has been simulated with PHILPAC again and the voltages and currents as a function of time obtained with this program are given in fig. 2.18, 2.19 and 2.20. In table 2.6 the specific times with the mean power-dissipation during 40 ns are listed.

table 2.6 Circuit 5

t_{dr}	[ns]	4.8
t_r	[ns]	5.0
t_{df}	[ns]	4.6
t_f	[ns]	4.9
mean pwr	[mW]	31.4

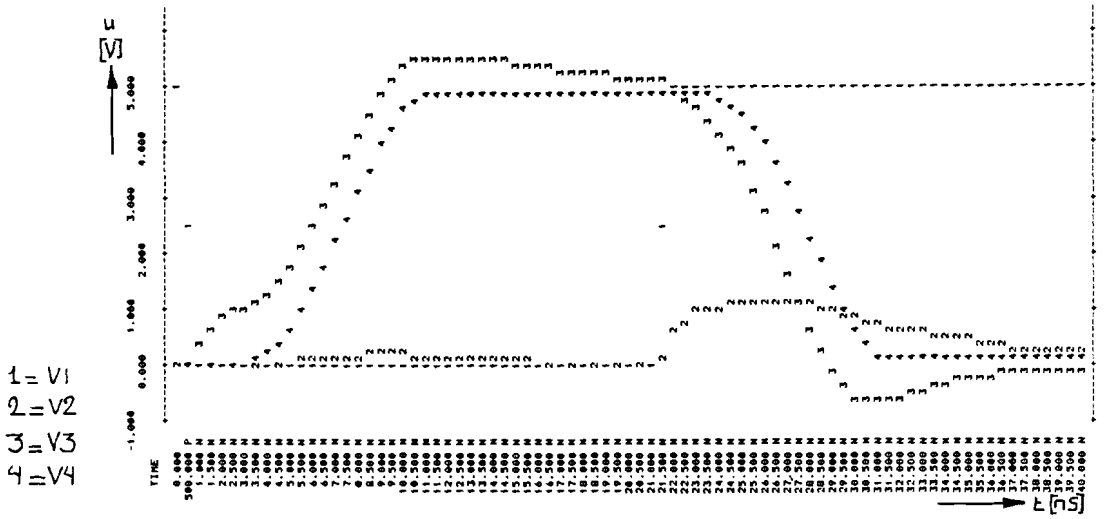


fig. 2.18. The voltage V_1, V_2, V_3 and V_4 in circuit 5.

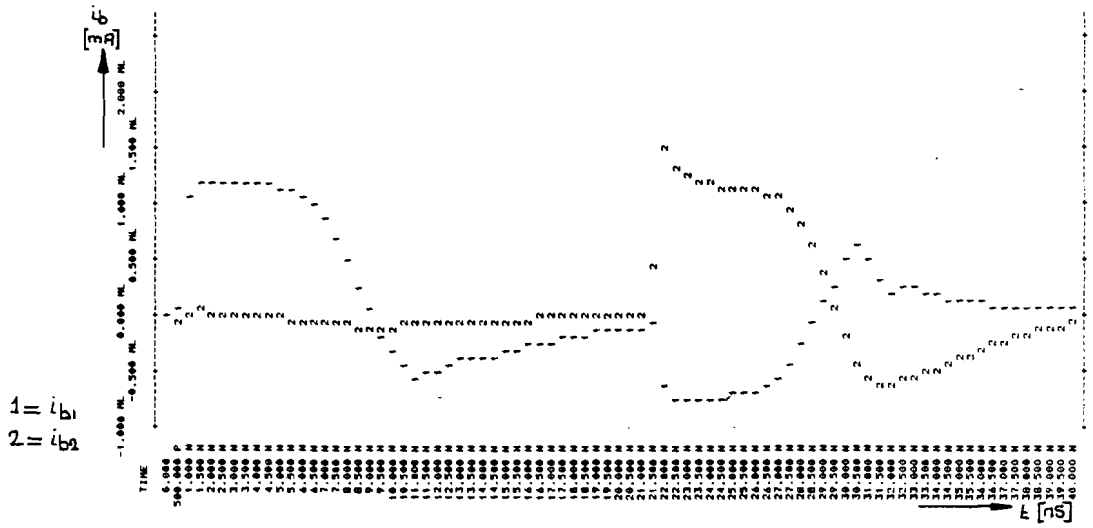


fig. 2.19. The base-currents i_{b1} and i_{b2} in circuit 5.

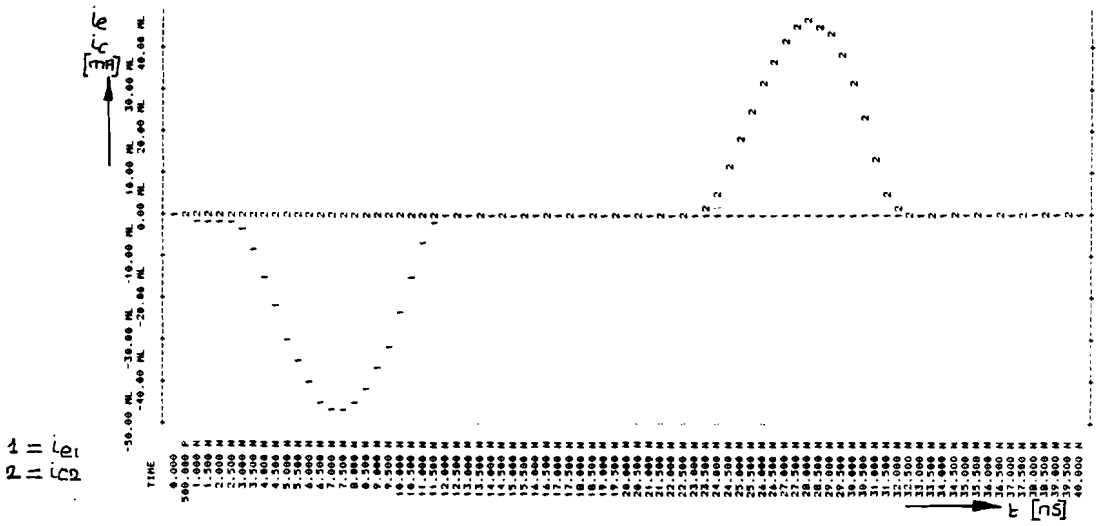


fig. 2.20 The emittercurrent i_{e1} and the collectorcurrentr i_{c2} in circuit 5

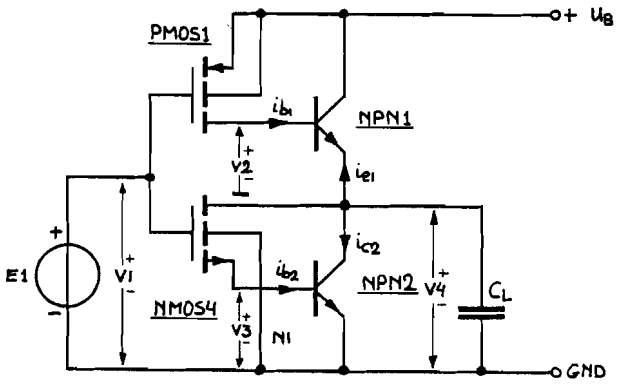
The most striking advantage of this circuit is the decreased power-dissipation. This can be understood very easily. The MOS-tansistor NMOS4 is no longer connected to the power-supply, so when the bipolar transistor is turned on, there is no current flow from the power-supply through NMOS4 to the base of NPN2. The base-current has now been provided by the load-capacitor.

As the Schottky diode has been removed, the collector-base capacitance of NPN2 has become smaller and therefore the transistor switches a little faster. Thus the disadvantage

of the smaller drive capacity of NMOS4 has been compensated and the falltime of this circuit is only a little longer than the one obtained with circuit 4.
Connecting the drain of NMOS4 to the output-terminal still has another advantage. When the output-voltage falls below the base-voltage, a current will flow from base to collector, because NMOS4 is still turned on. Therefore the active base-region is already being discharged, immediately after the discharge of the loadcapacitor, while NMOS2 has not yet been turned on.

2.5. A simplified circuit

When we look at the base-currents of NPN1 and NPN2 in fig. 2.15 we see that they become negative just before the output-voltage has reached its final value. This means, that the base-region already is being discharged immediately after the charging or discharging of the load-capacitor and therefore NMOS1 and NMOS2 are not really necessary.
However, there is one restriction to this alteration. The collector-base depletion-capacitor should be small enough with respect to the base-emitter depletion-capacitor. When the emitter voltage of NPN1 is forced down by NPN2, then the collector-emitter voltage of NPN1 is distributed over the depletion-capacitors between the base and collector and between the base and emitter.



PMOS1 : W = 37 µm C_L = 50 pF
NMOS4 : W = 17 µm U_B = 5V

fig. 2.21 Circuit 6

The depletion-capacitor between the base and the collector of NPN1 consists of the drain diode of PMOS1 and the collector-base junction of the bipolar transistor. When the ratio between the collector-base capacitor and the emitter-base capacitor is in such a way, that the base-emitter voltage rises above the turn-on voltage V_T, then, as a consequence, the transistor NPN1 will be turned on and behaves like a capacitor with the value $(\beta_F+1)(C_C+C_d)$ (see app. A5). In circuit 6 this is approximately 50 pF, so NPN2 is loaded with 100 pF instead of 50 pF and this increases the falltime t_f together with the power-dissipation.
The same process applies to NPN2, when NPN1 charges C_L, with one difference. For this transistor the source diode of NMOS4 is parallel to the base-emitter junction and therefore NPN2 behaves like a capacitor with value $(\beta_F+1)\ C_C$, when the base-emitter voltage exceeds V_T (see app. A5).
The circuit is given in fig. 2.21 and has been simulated with PHILPAC. The characteristic properties of this circuit are listed in table 2.7. The voltages and currents indicated in fig. 2.21 can be found in fig. 2.22, 2.23 and 2.24.

table 2.7. Circuit 6

t_{dr}	[ns]	3.6
t_r	[ns]	5.0
t_{df}	[ns]	3.7
d_f	[ns]	4.8
mean pwr	[mW]	29.6

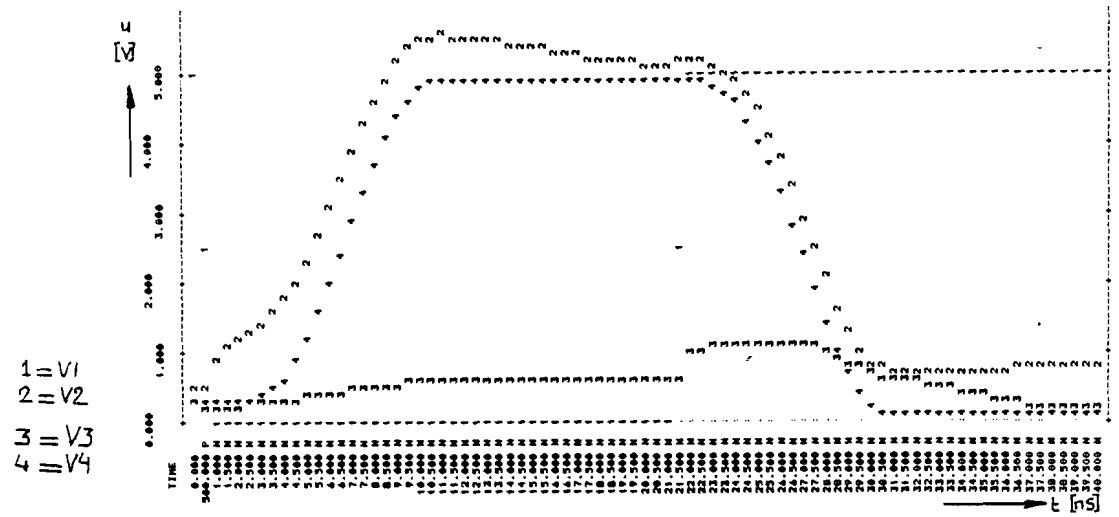


fig. 2.22. The voltages V1, V2, V3 and V4 in circuit 6

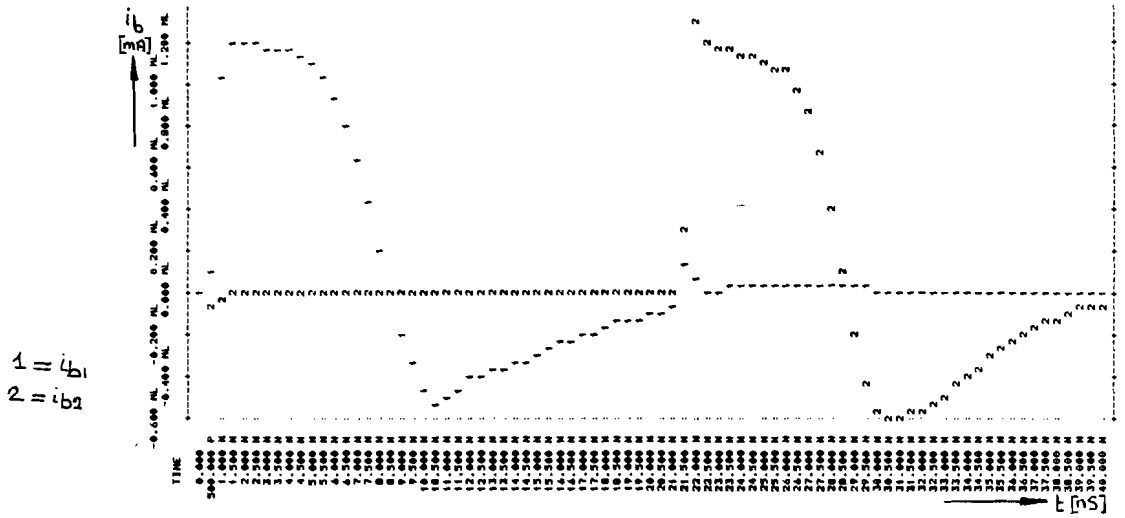


fig. 2.23. The base-currents i_{b1} and i_{b2} in circuit 6.

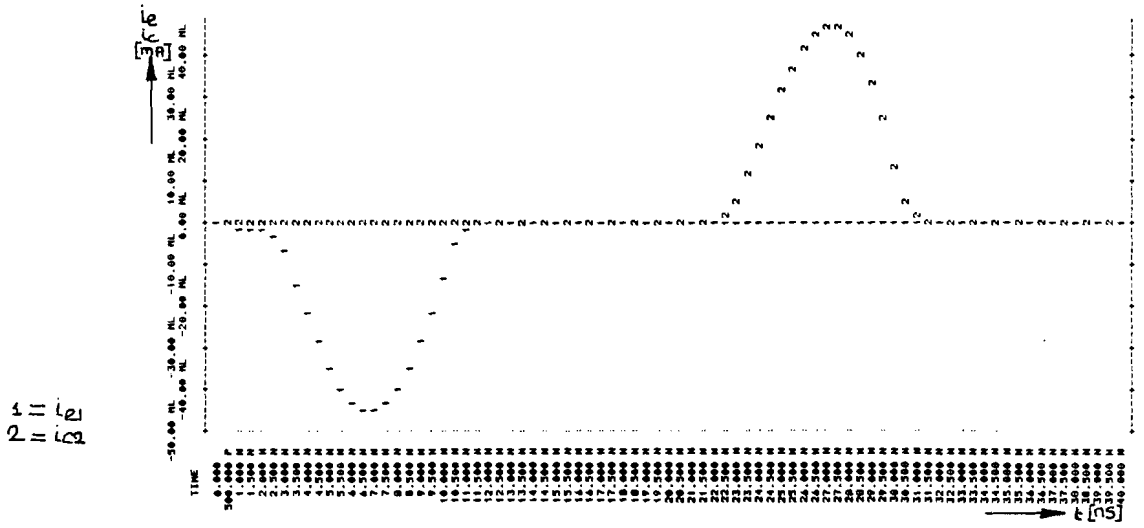


fig. 2.24. The emittercurrent i_{e1} and the collectorcurrent i_{c2} in circuit 6

In fig. 2.22 we see, that the base-voltage V_2 of NPN1 follows the output-voltage V_4, when the load-capacitor C_L is being discharged. The base-emitter voltage of this transistor increases slightly to a maximum of approximately 0.7V. This voltage almost exceeds the turn-on voltage V_T of the bipolar transistor ($\sim$ 0.7V), but in fig. 2.24 there is no noticeable emitter-current. As the base-emitter voltage is not pulled down to zero, but stays about 0.7V, in the next phase the turn-on delay-time t_{dr} will be shorter. The MOS transistor PMOS1 doesnot have to charge the base-emitter depletion-capacitor of NPN1 from zero to V_T, but starts already at about 0.7V. This can be seen in fig. 2.22 at t$\approx$38 ns.

When the load capacitor is being charged, the base-emitter voltage of NPN2 just rises to approximately 0.6V, so transistor NPN2 will not be turned on. In fig. 2.24 there is no significant collector-current i_{c2} at t$\approx$ 7ns, which demonstrates that NPN2 has not turned on indeed. Now again the base-emitter voltage is not pulled down to zero, so the delaytime t_{df} is also shortened. Transistor NMOS4 has to charge the base-emitter capacitor only from 0.6V to V_T for turning-on the bipolar transistor NPN2.
Comparing the results of circuit 6 in table 2.7 with those of circuit 5 in table 2.6, we see that the rise-time, the falltime and the mean power-dissipation remain nearly the same. The most stricking advantage of this circuit is the decrease of both delaytimes. As the base-emitter voltage of NPN1 is higher than this voltage of NPN2, just before the transistor will be turned on, the delay time t_{dr} is shorter than the delaytime t_{df}. This difference in voltage is caused by the fact, that the drain depletion-capacitance of PMOS1 is parallel to the collector-base capacitance of NPN1, while the source depletion-capacitance of NMOS4 is parallel to the base-emitter capacitance of NPN2. Therefore, when the outputvoltage has been pulled down, the base-emitter voltage of NPN1 rises more than the base-emitter voltage of NPN2, when the outputvoltage has been pulled up (see app. A5).

2.6. Conclusion

All the BIMOS circuits in this chapter behave very well, except the first. The circuits without a Schottky diode show almost the same switching properties as the circuits with a Schottky diode, and offer a reduction in power-dissipation. For this reason, these circuits have some preference with respect to the circuits with a Schottky diode.
As the base-emitter depletion-region has not been discharged completely, the delay-times of the last circuit in this chapter (circuit 6) have been shortened. For this last circuit it is important that the base-emitter voltage does not exceed the turn-on voltage of the bipolar transistor, when the transistor is not driven by the MOS transistor. Therefore the ratio between the base-emitter and base-collector capacitance is rather important.

3. THE BIMOS-DRIVERS COMPARED WITH A CMOS-DRIVER

3.1. Introduction

In this chapter a comparison has been made between the BIMOS drivers presented in chapter 2 and a CMOS driver. The performance of this CMOS driver will be discussed in the first two sections of this chapter. The falltime of the output-voltage will be calculated and in section 3.3 a practical circuit is presented. This circuit has been simulated with the circuit analysis program PHILPAC. Section 3.4 compares the results obtained with the BIMOS circuits and those obtained with the CMOS driver.

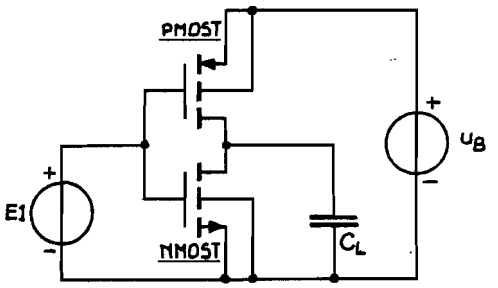


fig. 3.1.

3.2. The discharge of a loadcapacitor by a MOS-transistor

The basic circuit of a CMOS driver is shown in fig. 3.1. When the input is high, the NMOST discharges the loadcapacitor and the output-voltage is forced to zero. When the input is low, the NMOST has been turned off and the PMOST charges the capacitor. In the latter case the output-voltage is forced to the power-supply voltage. Both

transistors operate in the same way and therefore it is sufficient to examine the switching properties of only one transistor. In this section we consider the NMOST, which discharges the load-capacitor. If we insert (U_B-u_c) instead of u_c and use the magnitude of the threshold voltage of the PMOST $|V_{th}|$, the results obtained for the NMOST are also valid for the PMOST, which charges the capacitor C_L. Fig. 3.2. shows the circuit to be examined with the voltages and currents used in the calculations.

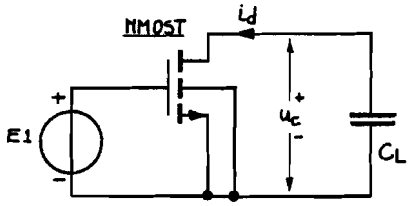


fig. 3.2.

For $t<0$ the output of voltage-source E1 equals zero. Therefore the NMOST is not switched on and the output-voltage u_c has been forced to U_B by the PMOST (see fig. 3.1). $u_c(0)=U_B$ is the initial condition. If $t>0$, E_1 is switched to U_B. This causes the NMOST to be turned on and the capacitor C_L will be discharged.
The MOST operates in saturation as long as $u_c > (U_B-V_{th})$. When this inequality is not valid, the MOST operates in triode-mode. Consequently the discharge of the loadcapacitor has been divided into two intervals. We first consider the interval, in which the MOST operates in saturation. The drain

current is (see [1] p. 59).

$$i_d = \frac{1}{2}\beta\left(u_B - V_{th}\right)^2 = \frac{1}{2}\beta_\square \frac{W}{L}\left(u_B - V_{th}\right)^2 \qquad (1)$$

With the capacitor we find a second equation for the drain-current

$$i_d = -C_L \frac{du_c}{dt} \qquad (2)$$

The combination of both equations gives a first order differential equation for the output-voltage u_C.

$$\frac{du_c}{dt} = -\frac{\beta_\square W}{2 C_L L}\left(u_B - V_{th}\right)^2 \qquad (3)$$

The general solution of this equation is

$$u_c = C_1 - \frac{\beta_\square W}{2 C_L L}\left(u_B - V_{th}\right)^2 t \qquad (4)$$

The initial condition $u_C(0)=U_B$ produces the constant C1. The curve of the output-voltage as a function of time can now be described as:

$$u_c = u_B - \frac{\beta_\square W}{2 C_L L}\left(u_B - V_{th}\right)^2 t \quad \text{for} \quad u_c > \left(u_B - V_{th}\right) \qquad (5)$$

This equation is used to calculate the time t_o at which the output-voltage u_C equals $(U_B - V_{th})$.

$$t_o = \frac{2 C_L L}{\beta_\square W} \frac{V_{th}}{\left(u_B - V_{th}\right)^2} \qquad (6)$$

Equation (5) is not valid for $t > t_o$. For this interval we consider the NMOST to operate in triode-mode.
The drain-current i_d in triode-mode is (see [1] p. 59)

$$\begin{aligned} i_d &= \beta\left[\left(u_B - V_{th}\right)u_c - \frac{1}{2}u_c^2\right] \qquad (7) \\ &= -\frac{1}{2}\beta_\square \frac{W}{L}\left[u_c^2 - 2\left(u_B - V_{th}\right)u_c\right] \end{aligned}$$

Equation (2) is still valid and the combination of eq. (2) and eq. (7) gives a first order differential equation for the output-voltage u_C when $t > t_o$.

$$\frac{du_C}{dt} = \frac{\beta_\square W}{2 C_L L}\left[u_C^2 - 2(u_B - V_{th})u_C\right] \tag{8}$$

In appendix A4 this equation has been solved with the separation of variables method. With the initial condition $u_C(t_o)=(U_B-V_{th})$ we find the output-voltage u_C as a function of time for $t > t_o$.

$$u_C = \frac{2(u_B - V_{th})}{1 + \exp\left[\frac{t-t_o}{\tau}\right]} \tag{9}$$

$$\text{with} \quad \tau = \frac{C_L L}{(u_B - V_{th})\beta_\square W} \tag{9a}$$

The voltage u_C in both intervals has been shown in fig. 3.3.

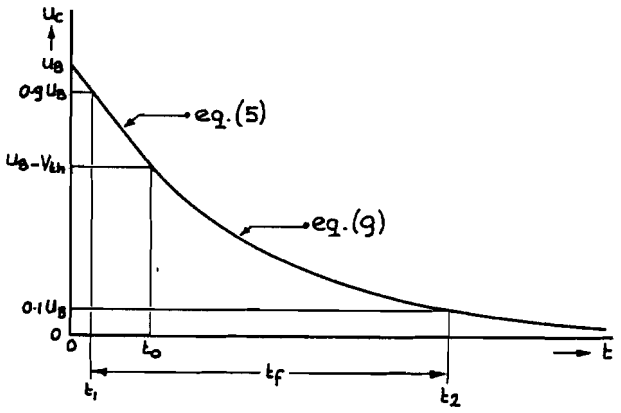


fig. 3.3

With the results obtained thus far, it is possible to find the falltime t_f as the difference between t_1 and t_2. These times are indicated in fig. 3.3. The time t_1, when u_C equals 0.9 U_B, has to be calculated with eq. (5):

$$t_1 = \frac{0.2\ U_B\ C_L\ L}{(U_B - V_{th})^2\ \beta_0\ W} = 0.2\ \tau \frac{U_B}{(U_B - V_{th})} \qquad (10)$$

The time t_2, when u_C equals 0.1 U_B, has to be calculated with the aid of eq. (9).

$$t_2 = \tau\left[\frac{2V_{th}}{(U_B - V_{th})} + \ln\left(19 - 20\frac{V_{th}}{U_B}\right)\right] \qquad (11)$$

The falltime t_f has been indicated in fig. 3.3 and is equal to the difference between t_2 and t_1:

$$t_f = t_2 - t_1 = \tau\left[\frac{2(V_{th} - 0.1U_B)}{(U_B - V_{th})} + \ln\left(19 - 20\frac{V_{th}}{U_B}\right)\right] \qquad (12)$$

It should be noticed, that this equation is only valid when $t_1 < t_0$. The threshold-voltage has to meet the inequality $V_{th} > 0.1\ U_B$. If $V_{th} < 0.1\ U_B$, the time t_1 should be calculated too with equation (9).

$$t_1' = \tau\left[\frac{2V_{th}}{(U_B - V_{th})} + \ln\left(11 - 20\frac{V_{th}}{U_B}\right)\right] \qquad (13)$$

Now the falltime becomes:

$$t_f' = t_2 - t_1' = \tau \ln\left(\frac{1.9U_B - 2V_{th}}{1.1\ U_B - 2V_{th}}\right) \quad \text{for } V_{th} < 0.1U_B \qquad (14)$$

The driver is not loaded only by the loadcapacitor C_L, but also by the drain depletion-capacitors of both transitors. These capacitors are linearly dependent on the width of the transistors. If the ratio γ is defined as $\gamma = W_p/W_n$, the drain-

capacitance becomes

$$C_d = C_{dp} W_p + C_{dn} W_n = (\gamma C_{dp} + C_{dn}) W_n \qquad (15)$$

with C_{dp} = drain depletion-capacitance of PMOST per unit of length

C_{dn} = drain depletion-capacitance of NMOST per unit of length

$\gamma = W_p/W_n$

Adding this drain-capacitance C_d to the load-capacitance C_L in eq. (9a) we find for the NMOST the timeconstant τ_n :

$$\tau_n = \frac{L_n}{(u_B - V_{thn})\beta_{n\square}} \left(\frac{C_L}{W_n} + \gamma C_{dp} + C_n \right) \qquad (16)$$

and similarly the timeconstant τ_p for the PMOST:

$$\tau_p = \frac{L_p}{(u_B - V_{thp})\beta_{p\square}} \left(\frac{C_L}{W_p} + C_{dp} + \frac{C_{dn}}{\gamma} \right) \qquad (17)$$

(The index n or p indicates the type of MOS-transistor).

3.3. A CMOS-driver

In the previous sections the basic circuit of the CMOS driver has been discussed and the circuit is shown in fig. 3.1. To be of practical value, this driver circuit should be preceded by one or more identical circuits, which have been designed to drive the gate capacitances. In this way the driver circuit can be designed to have an input-capacitance comparable to the one of the BIMOS circuits. This can be obtained by three stages. The circuit is shown in fig. 3.4.

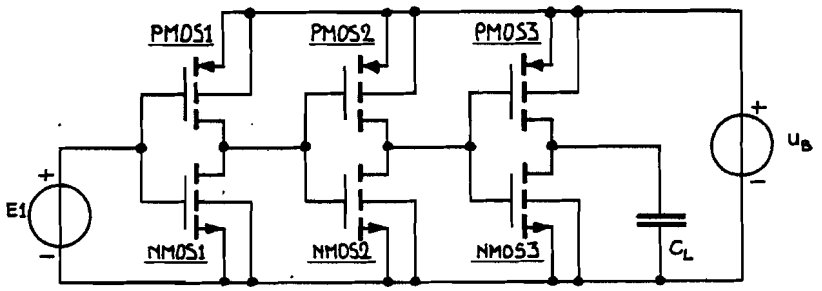


Fig. 3.4. The CMOS-driver circuit.

In this circuit the fall- and risetimes of the individual invertercircuits cannot be calculated by the equations found in the previous section, because the gate-voltages are now changing exponentially as shown in fig. 3.3, instead of abrupt. With the circuit analysis program PHILPAC this circuit has been investigated and designed to have rise- and fall-times of approximately 5nS. The output-voltage and the drain-currents of PMOS3 and NMOS3 as a function of time have been obtained with PHILPAC and are shown in figs 3.5 and 3.6

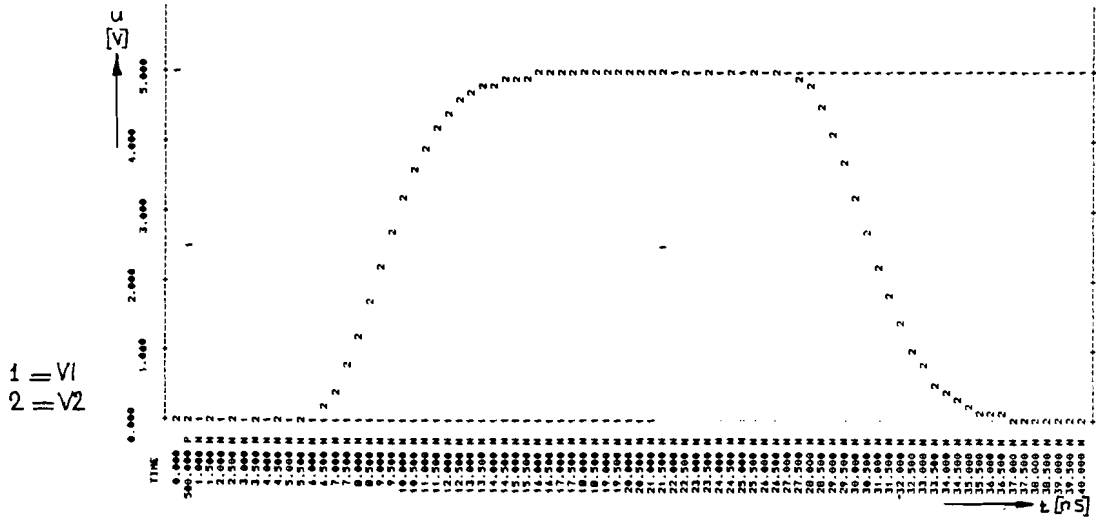


Fig. 3.5. The input voltage V_1 and the output voltage V_2 of the CMOS-driver circuit in fig. 3.4.

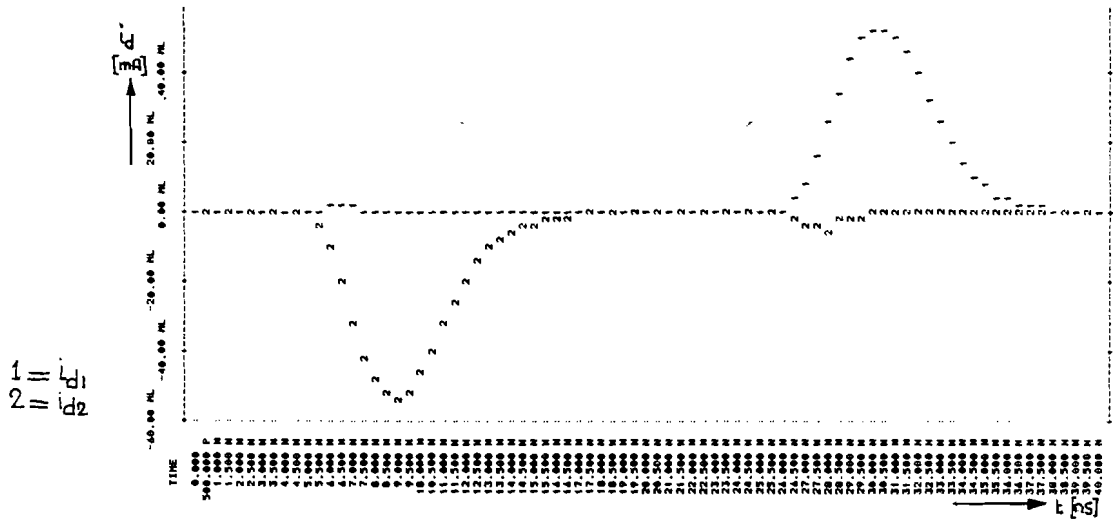


Fig. 3.6. The drain-current i_{d1} of NMOS3 and the drain-current i_{d2} of PMOS3 of the CMOS-driver circuit.

The results above are obtained with the parameters given in appendix B3. The most significant ones are listed in table 3.1

table 3.1.

Description	Symbol	NMOST	PMOST	dim.
Zero-bias threshold-voltage	V_{T0}	0.75	1.1	V
Body-factor	K	0.31	0.75	$\sqrt{V}$
Channel-length	L	2	2	µm
Square gain-constant	$\beta_{\square}$	45	15	$\mu A/V^2$

The delay times, the falltime, the risetime and the mean power-dissipation during 40 ns have been determined by PHILPAC and are listed in table 3.2.

table 3.2. CMOS circuit

t_{dr}	(V_4=0.5)	[ns]	7.5
t_r		[ns]	5.1
t_{df}	(V_4=4.5)	[ns]	7.1
t_f		[ns]	5.2
Mean power		[mW]	43.5

Each individual inverter in this driver circuit introduces some delay, because the gate-voltages do not change abrupt. The MOS transistors of the next inverter stage just become active, when the gate-voltage exceeds the threshold-voltage V_{th}. In the previous section the input-voltage of an NMOST, which discharges a capacitor has been calculated. In the CMOS driver-circuit (see fig. 3.4) the load-capacitor of the first inverter consists of the drain depletion-capacitance and the gate-capacitance of the next stage. The PMOST of this next inverter just becomes active, when its gate-voltage falls below (U_B-V_{th}). This condition has been met, when $t > t_o$ and therefore the delay is to the order of t_o (see eq. (6)). The second inverter is loaded with the final driverstage and introduces a similar delay. When we define the delaytime as the time, in which the output-voltage exceeds one tenth of the total voltage-change, the final driverstage introduces a delay to the order of t_1 (see eq. (10)).

3.4. A comparison of a CMOS-driver with the BIMOS-drivers

For this comparison, the results of the circuits as obtained with the circuit analysis program PHILPAC, are summarized in table 3.3.

table 3.3

Circuit	t_{dr} (ns)	t_r (ns)	t_{df} (ns)	t_f (ns)	Mean power (mW)
1	5.1	7.0	15.1	4.6	50.7
2	4.8	5.1	5.8	4.6	34.8
3	4.8	5.5	5.4	5.1	37.3
4	4.7	5.0	4.7	4.7	33.6
5	4.8	5.0	4.6	4.9	31.4
6	3.6	5.0	3.7	4.8	29.6
CMOS	7.5	5.1	7.1	5.2	43.5

As explained in chapter 2 section 2 the first circuit (nr.1) does not meet the requirements. Therefore this BIMOS circuit has not been used in the following comparison between the BIMOS circuits and the CMOS circuit.
As all other circuits have been designed to yield switching times to the order of 5ns, the most important differences occur in the mean power-dissipation and the delaytimes.
In the first place all the BIMOS-circuits dissipate less power than the CMOS circuit. In this respect the circuits 5 and 6 are superior and this is caused by the fact, that the MOS-transistor, which drives bipolar transistors NPN2, is not connected with the power-supply, but with the output of the circuit. Therefore there is no current from the powersupply to the base of the bipolar transistor, when the load-capacitor has been discharged.
The power-dissipation of the CMOS circuit is rather high, because in this circuit three capacitors have to be switched: the gate-capacitors of the second and third inverterstage and the loadcapacitor.
A second advantage of the BIMOS-circuits with respect to the CMOS-circuit is the shorter delay-time. Especially circuit 6 gives a remarkable improvement.

In table 3.3. only the electrical properties of the circuits have been given. However, there is still a third advantage of the BIMOS-circuits. The area occupied by the integrated BIMOS-circuit is much smaller than the area of the integrated CMOS circuit. More about this can be found in chapter 5.

3.5. Conclusion

When a BIMOS- and a CMOS driver circuit both are designed to have prescribed rise- and fall times, the BIMOS circuit has two important advantages with respect to the CMOS circuit. In the first place the power-dissipation of the BIMOS circuit is less than the dissipation of the CMOS circuit. If designed properly, this can be reduced to 75% of the CMOS dissipation. Secondly the BIMOS driver circuits have the advantage of a shorter delaytime. The best design offers a decrease in the delaytime to about 60% of the CMOS delaytimes.

4. BIMOS INVERTER CIRCUITS

4.1. Introduction

In this chapter the qualities of a BIMOS-circuit, which has been designed with a minimum bipolar transistor, are compared with a CMOS-circuit. As the BIMOS circuit is still able of driving a relatively high load-capacitor, this circuit is compared with a CMOS circuit, which has the same drive capacity.
With this BIMOS-circuit two ringoscillators have been designed: one oscillator with inverters, which are loaded by capacitors of 1 pF and one oscillator consisting of inverters, which are loaded only by the next stage. This second oscillator gives an impression of the highest speed possible with BIMOS.

4.2. Calculations on a CMOS inverter circuit

The switching times of a MOS-transistor, which discharges a load-capacitor have already been calculated in chapter 3. With those results we now are going to examine the properties of the CMOS-inverter, which is loaded by an identical circuit. The results of these calculations give an impression on the highest possible speed, which can be obtained with the CMOS inverter.
The circuit to be examined is given in fig. 4.1.

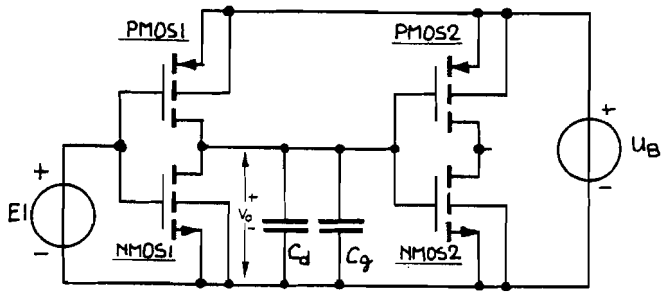


fig. 4.1.

The first inverter with PMOS1 and NMOS1 is loaded by the drain depletion-capacitances of both transistors and the gate-capacitance of the next inverter stage.
In chapter 3 the drain-capacitance has already been taken into account. When we insert the gate-capacitance for the load-capacitance C_L in the equations (16) and (17), we obtain the time-constants we are looking for.
The gate-capacitance depends linearly on the width of the MOS transistors:

$$C_g = (C_{gp} W_p L_p + C_{gn} W_n L_n) = C_{ox} (\gamma L_p + L_n) W_n \quad (1)$$

with C_{ox} = gate-capacitance per unit of area

With (1) we find for the timeconstant of the NMOST (falltime)

$$\tau_n = \frac{L_n}{(\mu_B - V_{thn})\beta_{n\square}} \left[C_{ox} (\gamma L_p + L_n) + \gamma C_{dp} + C_{dn} \right] \quad (2)$$

and for the timeconstant of the PMOST (rise time):

$$\tau_p = \frac{L_p}{(\mu_B - V_{thp})\beta_{p\square}} \frac{1}{\gamma} \left[C_{ox} (\gamma L_p + L_n) + \gamma C_{dp} + C_{dn} \right] \quad (3)$$

These last two equations show, that the switching-times are not dependent on the width of the transistors, when the ratio γ is kept constant. On the other hand, the time-constants strongly depend on the channellength. Therefore the minimum length should be taken to obtain the highest speed.

In chapter 3 the ratio γ has already been calculated to obtain equal rise- and falltimes. With $\gamma = 3.8$ and the parameters of the MOS transistors listed in table 4.1 (see app. B3), we can find the minimum switching time.

		NMOST	PMOST
V_{th}	V	1.0	1.7
$\beta_{\square}$	$\mu A/V^2$	45	15
L	μm	2	2
Cd	$fF/\mu m$	0.6	1.8
Cox	$fF/\mu m^2$	0.68	0.68

The minimum switching-time has been calculated with the aid of eq. (12) in chapter 3 and eq. (2) in this chapter.

$$t_{min} = 0.42 \text{ nS} \qquad (4)$$

4.3. Calculations on a BIMOS inverter circuit

The BIMOS circuit, which has been examined is shown in fig. 4.2.

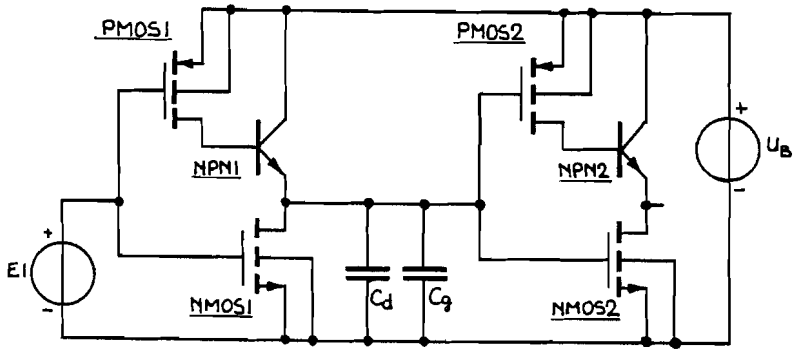


fig. 4.2.

In this circuit the PMOST's and the bipolar transistors are minimum components. The width of the PMOST is 7 μm and the parameters of the minimum bipolar transistor are listed in appendix B2. The width of the NMOST has been chosen to give

equal rise-and falltimes.
The loadcapacitance consists of the drain depletion-capacitance of NMOS1 C_d and the gate-capacitances of the next inverter stage C_g.

$$C_d + C_g = C_{dn} W_n + C_{ox} \left(L_p W_p + L_n W_n\right) \qquad (5)$$

with C_{dn} = drain-capacitance of NMOST per unit of length.
C_{ox} = gate-capacitance per square unit.

The rise-time can be found with the equations in chapter 1 section 3. All the simplifications still hold for the minimum transistor in this circuit. When the NMOST is not too large, the loadcapacitance can be neglected with respect to $(\beta_F+1)\ C_c$. Therefore we find the equation:

$$t_r = \left[V_0 - 0.1\left(U_B - V_T\right)\right]\frac{C_c}{i_{bs}} + \frac{C_c}{2r}\ln\left[\frac{0.1\left(U_B - V_T\right)}{U_B - V_T - V_0}\right] \qquad (6)$$

We find an upper limit with:

$$V_0 = V_{th} - V_T \quad \text{and} \quad r = -\tfrac{1}{2}\beta_\square \frac{W}{L}\left(U_B - V_{th}\right)$$

and a lower limit with:

$$V_0 = \tfrac{1}{2}\left(U_B + V_{th}\right) - V_T \quad \text{and} \quad r = -\beta_\square \frac{W}{L}\left(U_B - V_{th}\right)$$

(see chapter 1 eq. 41a and 41b).

The parameters needed to calculate this risetime are listed in table 4.2.

table. 4.2.

V_{th} = 1.7V	$\beta_\square$ = 15 µA/V^2
C_c = 65 fF	W = 7 µm
V_T = 0.7V	L = 2 µm
U_B = 5V	

The limits for this risetime are:

t_{rmin} = 0.75 ns
t_{rmax} = 0.98 ns

4.4. CMOS ringoscillators

Two ringoscillators have been simulated by PHILPAC. The first oscillator consists of seven inverters loaded with a capacitor of 1 pF. The second oscillator has eleven unloaded inverter circuits. The PMOSt has a width of 136 µm and the width of the NMOST is 40 µm. The length of the channels of both transistors is 2 µm. Fig. 4.3. and fig. 4.4. show the output-voltage and the draincurrents respectively of the ringoscillator consisting of the inverter-circuits with a loadcapacitor of 1 pF.

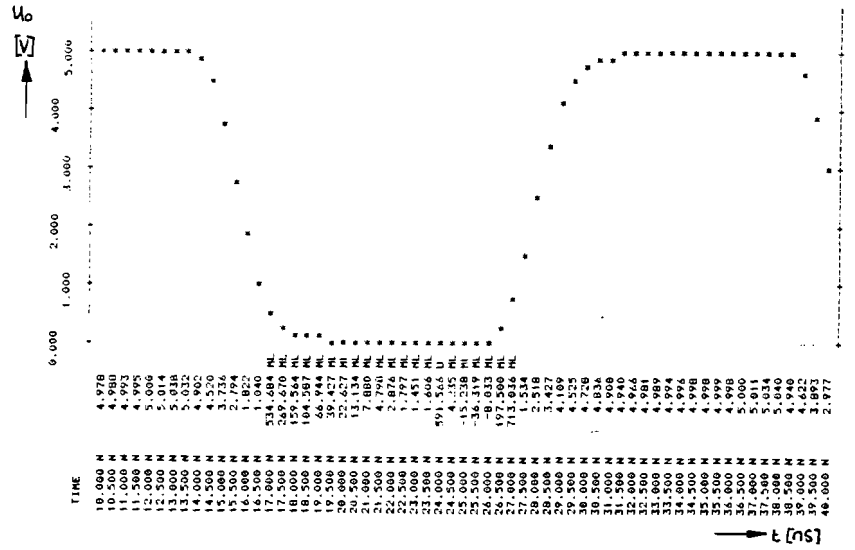


fig. 4.3. The output-voltage of the CMOS ringoscillator with seven loaded inverter-circuits

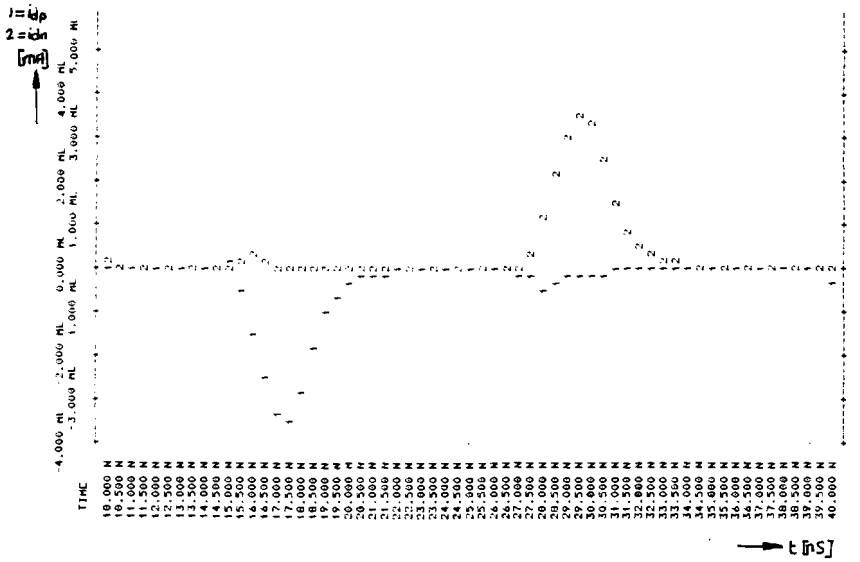


fig. 4.4. The drain-currents of the CMOS ringoscillator with seven loaded inverter-circuits

In fig. 4.3. we see, that this seven-stage ringoscillator has a period-time of 25 ns. With fig. 4.4. it becomes clear, that the oscillator operates in a proper way, because there is just a small unwanted drain-current.

Simulating the eleven-stage ringoscillator with unloaded CMOS inverter-circuits results in an output-voltage and drain-currents shown in fig. 4.5. and fig. 4.6. respectively.

fig. 4.5. The output-voltage of an unloaded inverter in an eleven-stage ringoscillator

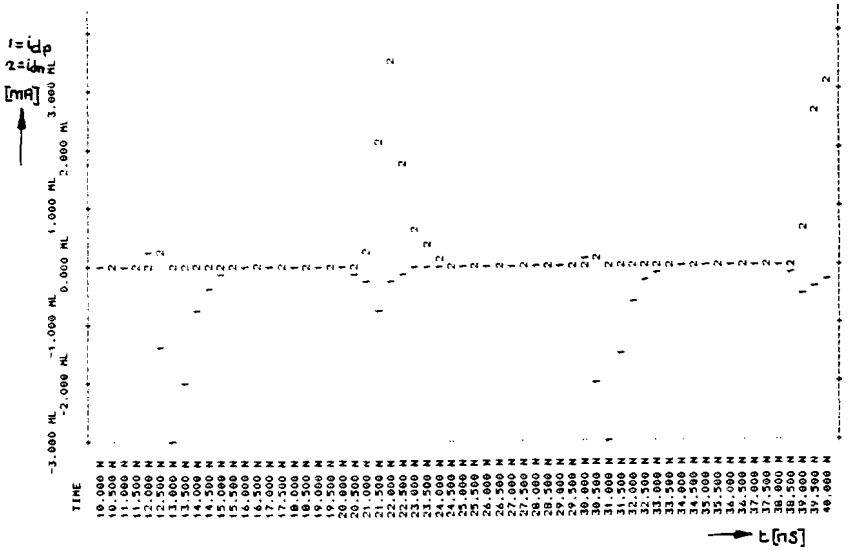


fig. 4.6. The drain-currents of an unloaded inverter in an eleven-stage ringoscillator

This eleven-stage ringoscillator has a period of 18 ns, which gives 0.8 ns delay per stage.

4.5. BIMOS ringoscillators

Ringoscillators also have been formed with the circuit shown in fig. 4.2. One oscillator consists of BIMOS inverter circuits, which are loaded with a capacitance of 1 pF, and a second oscillator operates with unloaded inverters. Both oscillators have been simulated with the circuit analysis program PHILPAC and the results are shown in fig. 4.7. to fig. 4.10.

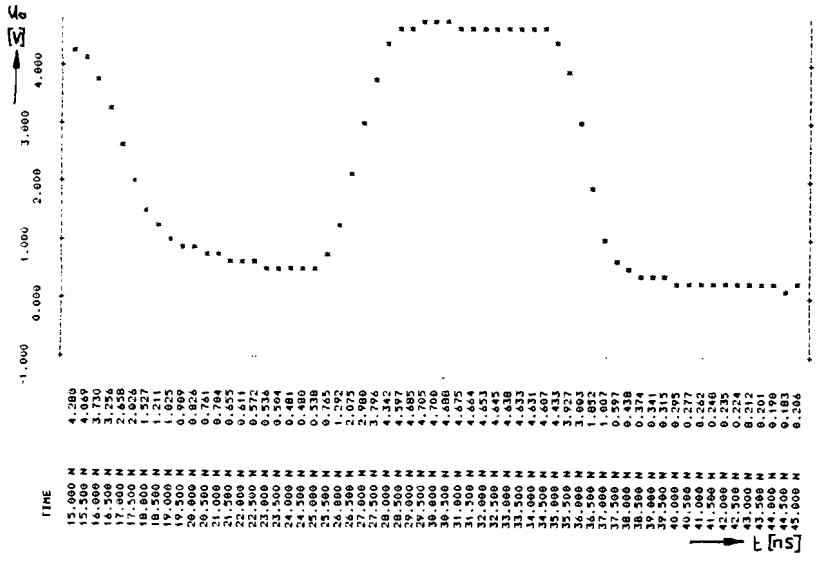


fig. 4.7. The output voltage of an inverter circuit, loaded with 1 pF, being part of a seven-stage ringoscillator

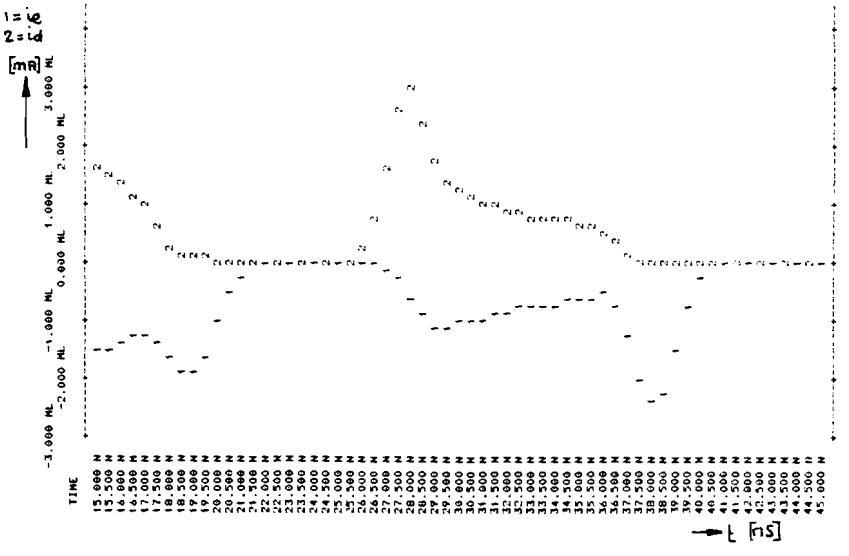


fig. 4.8. The emitter- and drain current of an inverter circuit, loaded with 1 pF, being part of a seven stage ringoscillator

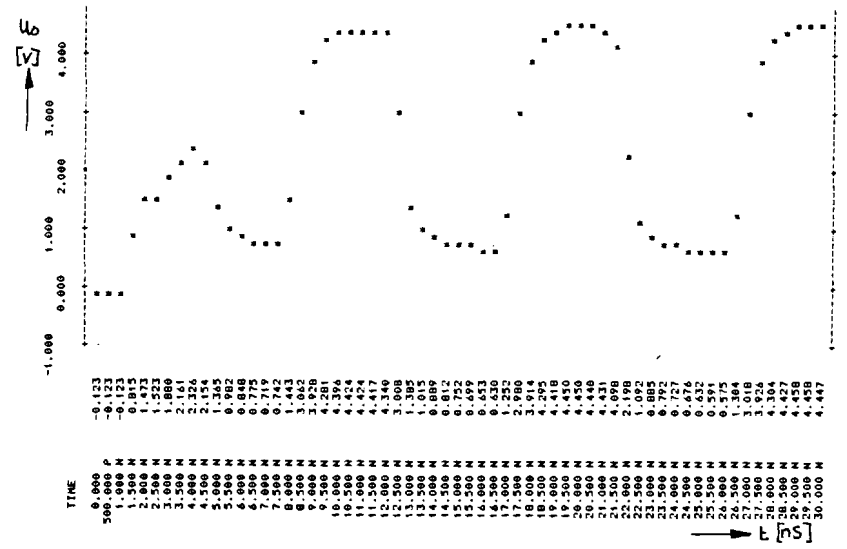


fig. 4.9. The output-voltage of an unloaded inverter-circuit, which is part of an eleven-stage ringoscillator

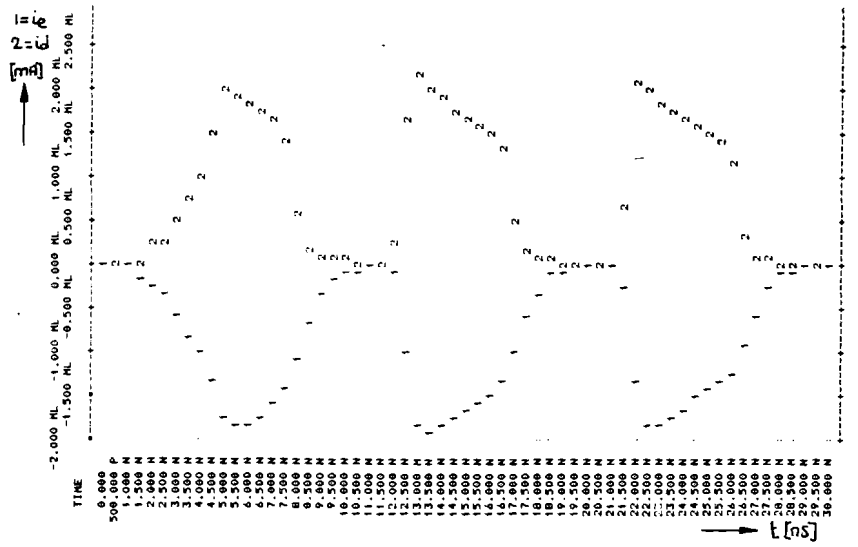


fig. 4.10. The emitter- and draincurrent of an unloaded inverter-circuit, which is part of an eleven-stage ringoscillator

When we take a look to fig. 4.8. and 4.10, it becomes clear, that the BIMOS inverters do not switch in a proper way. The bipolar transistor is not switched off at all and therefore there is always an emitter-current during the time the NMOS transistor is turned on (output-voltage low).
Of course this is an undesirable effect, because this causes a rather high power-consumption. Yet there is one advantage of this operation. As the bipolar transistor is not turned off, the output will become high immediately after the moment, when

the NMOST is turned off. There is no delaytime, caused by the charge of the active base-region of the bipolar transistor. Therefore the oscillation frequency of this ringoscillator is rather high. The oscillator with seven loaded inverters has an output-signal with a period of 19.5 ns and the oscillator with eleven unloaded circuits oscillates with a period of 9.5 ns. Both periods are considerably shorter than the periods of the CMOS ringoscillators in the previous section.
To make sure, that the bipolar transistor is turned off, a second NMOS transistor should be added to the inverter circuit. This is shown in fig. 4.11.

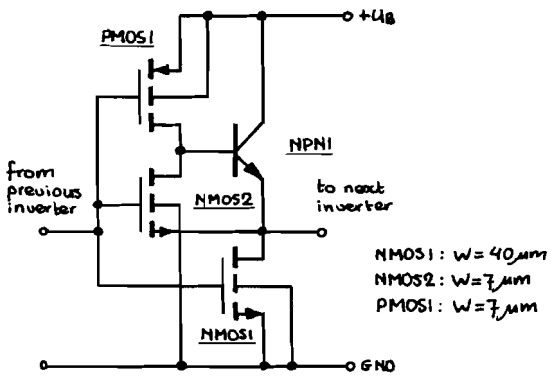


fig. 4.11.

This circuit is used loaded with 1 pF in a seven stage ringoscillator and unloaded in a ringoscillator with eleven stages. The results of the simulation by PHILPAC are shown in fig. 4.12 to fig. 4.15.

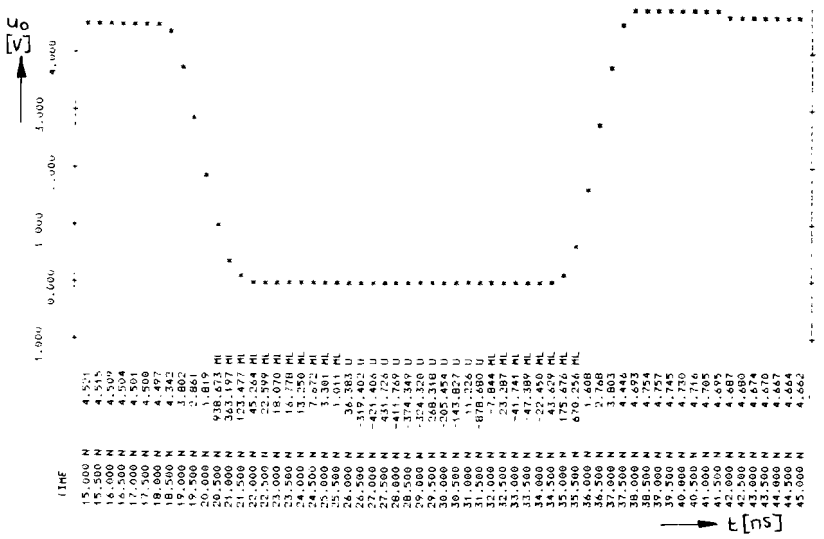


fig. 4.12. The output-voltage of the improved inverter loaded with 1pF

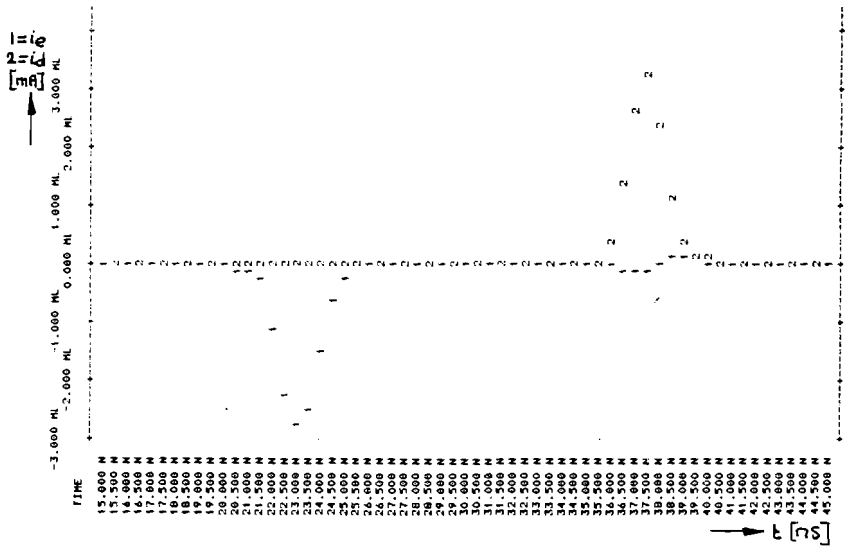


fig. 4.13. The emitter- and draincurrents of the improved inverter circuit loaded with 1 pF

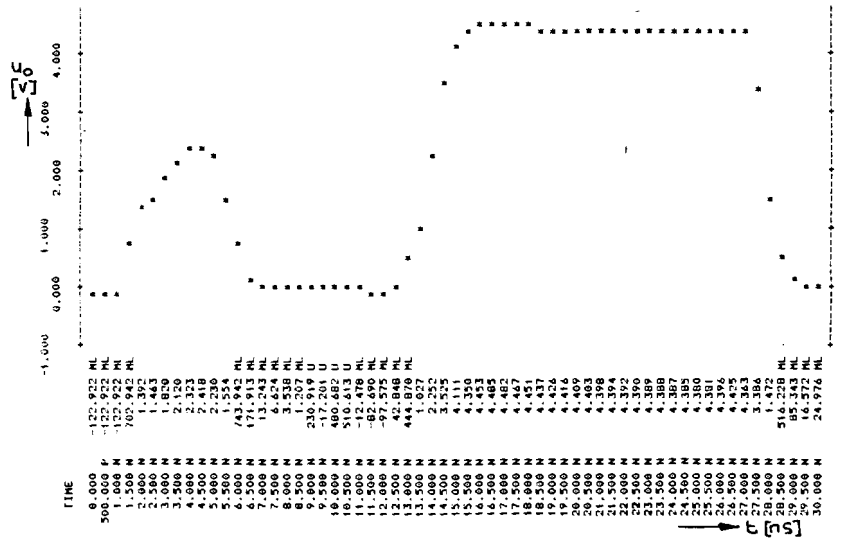


fig. 4.14. The output-voltage of the improved inverter in an elevenstage ringoscillator

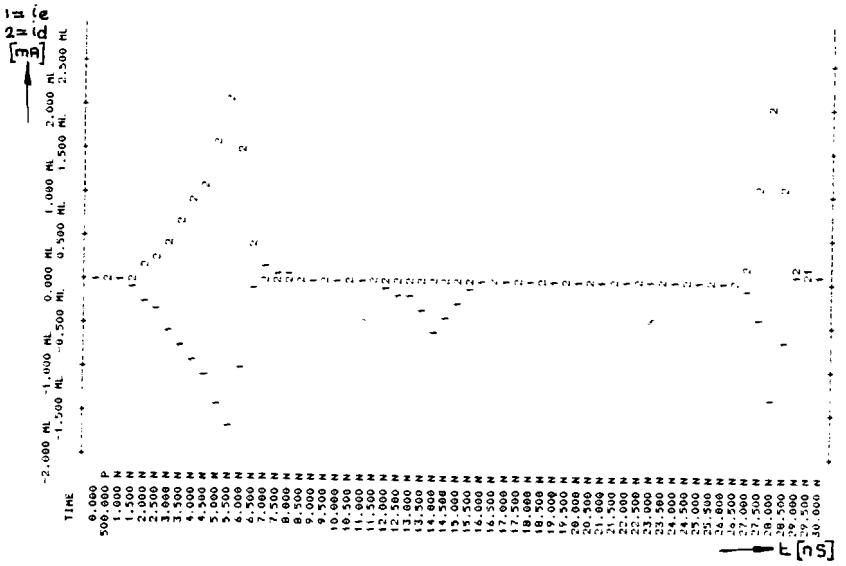


fig. 4.15. The emitter- and draincurrents of the improved inverter in an eleven-stage ringoscillator

The figures 4.13 and 4.15 show clearly, that the bipolar transistor operates much better now. The period of the ringoscillator with loaded circuits is approximately 33 ns, which is rather long in respect with the 25 ns of the CMOS oscillator. This is caused by the turn-on delaytime of the bipolar transistor.
The period of the oscillator with unloaded inverters is about 30 ns. This shows, that the turn-on delaytime determines for a great deal the oscillation frequency, even with loads of 1 pF.

4.6. Conclusion

The BIMOS inverter circuits with minimum area components do not act very well. With the BIMOS ringoscillators it is possible to obtain a higher oscillation frequency, than with the CMOS-ringoscillator, but this costs a high power consumption.
When the BIMOS-circuits operate in a proper way, they are clearly slower than the CMOS-circuits, because of the turn-on delaytime of the bipolar transistor.

5. THE LAYOUT OF THE BIMOS CIRCUITS

5.1. The design-rules

The design-rules of a process give a prescription of the minimum dimensions, which can be used in designing the layout of the masks. As the BIMOS-process is the combination of a CMOS-process and a bipolar-process, the design-rules are divided in two sets. The layout of the MOS-part has to be designed with the design-rules of the C500-process [5]. The layout of the bipolar-part in the circuits should be designed with the special rules drawn up for the BIMOS process [6] . Due to one special design-rule for the bipolar part, the bipolar transistors are individually surrounded by a guard-ring. This ring has been added to minimize the influence of a substrate-current on the devices surrounding this bipolar transitor.

5.2. The layout of the driver circuits

Three of the circuits described in chapter 2 have been integrated. These circuits are circuit 2, 5 and 6 and have been indicated with BIMOS3, BIMOS12 and BIMOS13 respectively. The circuits have been designed to occupy a minimum area on the chip. The layouts of these circuits have been shown in fig. 5.1 and 5.2 and 5.3

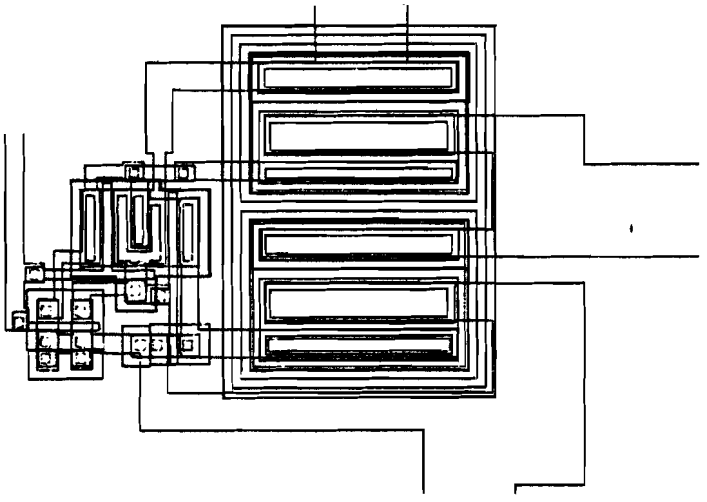


Fig. 5.1. BIMOS3 (circuit 2)

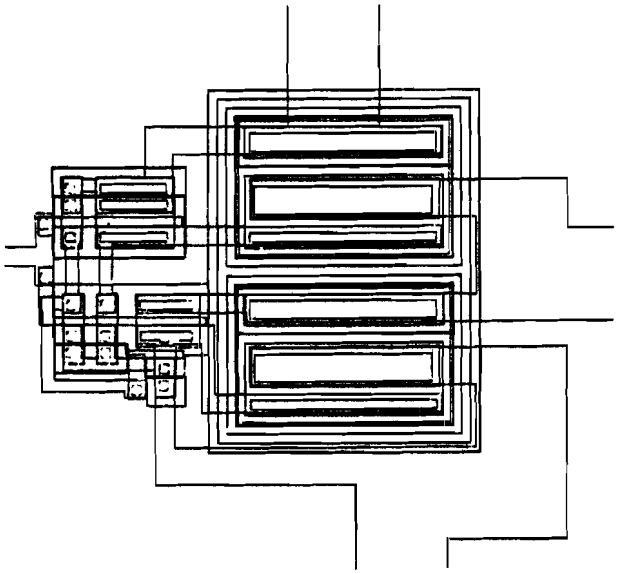


Fig. 5.2. BIMOS12 (circuit 5)

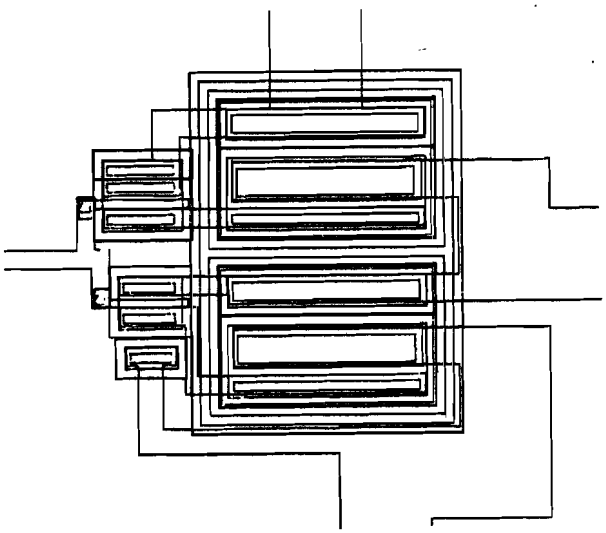


Fig. 5.3. BIMOS13 (circuit 6)

The parameters of the MOS-transistors known at the time the layouts of the circuits were designed differ slightly with the parameters used in this report and listed in appendix B3. Therefore the width of the MOS-transistors, which drive the bipolar transistors, also differ with the width obtained in chapter 2. The circuits have been simulated too with the new parameters (app. B3) and the results are listed in table 5.1.

table 5.1

circuit		BIMOS3	BIMOS12	BIMOS13
t_{dr}	(ns)	6.3	6.1	4.6
t_r	(ns)	6.5	6.4	6.3
t_{df}	(ns)	7.6	4.1	3.4
t_f	(ns)	6.8	4.3	4.3
mean pwr	(mW)	32.2	31.3	30.5

It should be mentioned that the parameters given in appendix B and used in this report are still tentative parameters for the BIMOS process. Therefore it is possible that the properties of the circuits differ from the results listed in table 5.1 due to altered parameters.
For this reason the MOS and bipolar transistors used in the circuits have been integrated individually. With those transistors we are able to determine the parameters of the components and then it is possible to simulate the circuits in a proper way. With the results obtained by measurement the circuits can be simulated and designed again to meet the specified properties.

The dimensions of all BIMOS-driver circuits are approximately 140µ x 160µ and this is much smaller than the dimensions of the CMOS driver circuit with identical switching properties. The latter circuit measures about 200µ x 380µ. This has been illustrated in fig. 5.4.

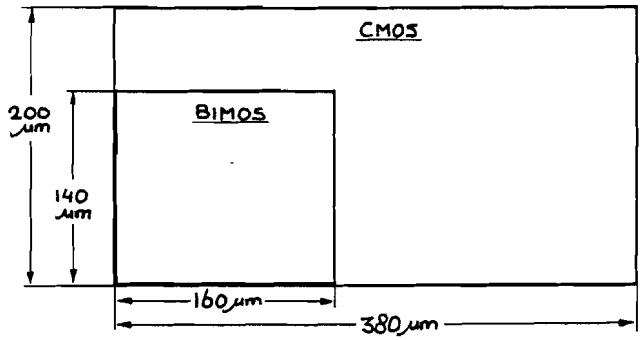
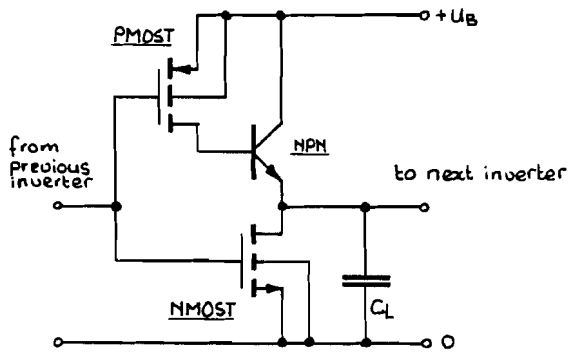


fig. 5.4.

Because of their smaller area, the BIMOS driver circuits are given preference over the CMOS circuit, especially in circuits with many driver-outputs.

5.3. The layout of the ringoscillators

Two ringoscillators with identical basic invertercircuits have been integrated. The first oscillator consists of seven invertercircuits loaded with a capacitance of 1 pF. The circuit of one inverter is shown in fig. 5.5.



PMOST : W = 7 µm NPN : emitter area = 50 µm^2 U_B = 5V
NMOST : W =40 µm C_L = 1pF

Fig. 5.5

An eighth inverter circuit without loadcapacitor has been added, which takes care of the output-signal.
This ringoscillator has been indicated with RING7 and the layout of the integrated oscillator is shown in fig. 5.6.

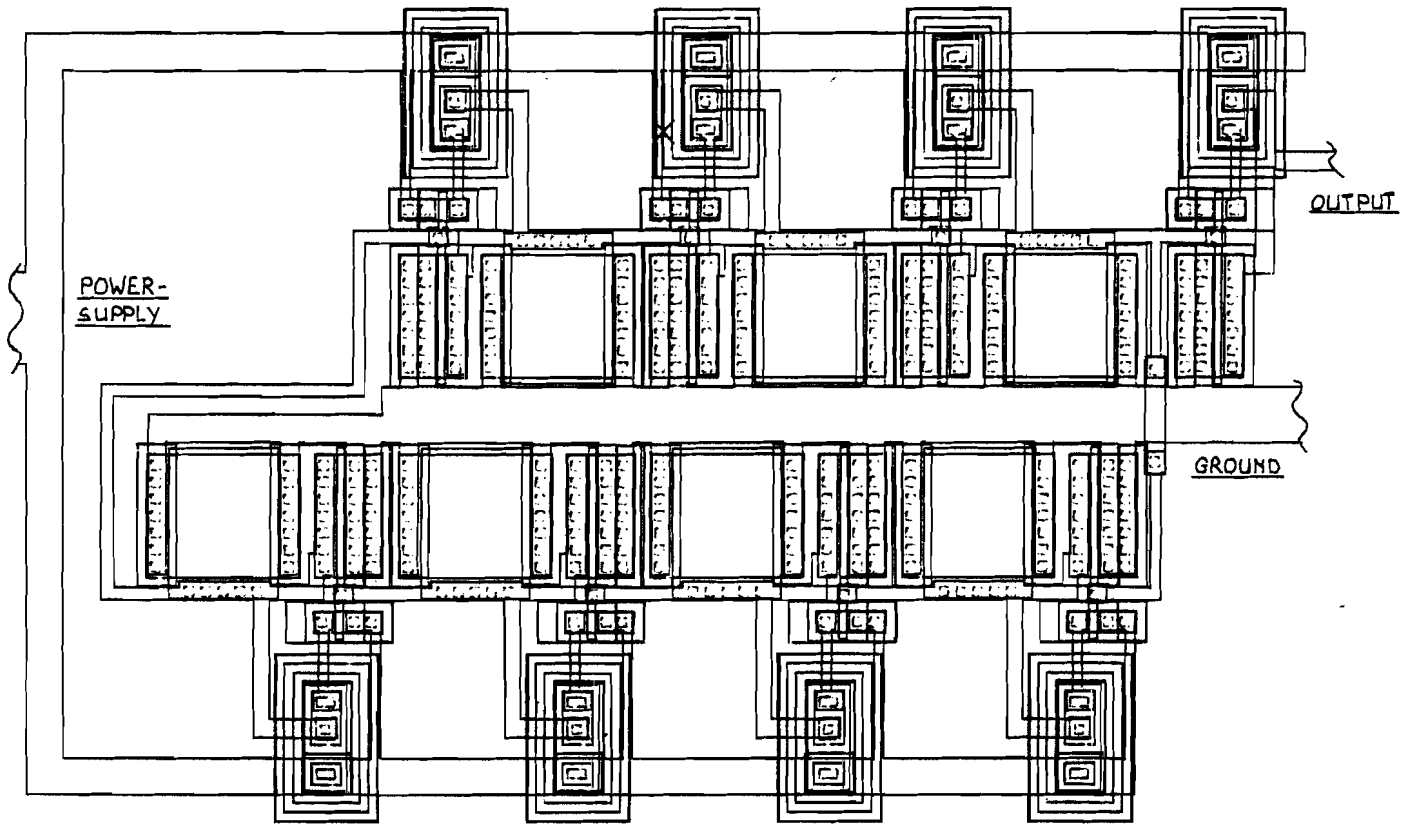


Fig. 5.6. Ringoscillator RING7

The second oscillator consists of twenty-seven inverter circuits like the one shown in fig. 5.5, without load-capacitor C_L. In this oscillator the inverters are loaded by the input-capacitance of the next stage and as this capacitance is much smaller than 1 pF, the number of inverter circuits has been increased to obtain an output-signal with an oscillation-frequency, that can be measured easily with an oscilloscoop.
As the oscillator should not be loaded by a large capacitor, the circuit, which provides the output-signal, only consists of a PMOST in combination with an NPN bipolar transistor. The circuit is similar to the one shown in fig. 5.5 without the NMOST.
This ringoscillator has been indicated with RING27 and the layout of the integrated oscillator is shown in fig. 5.7.

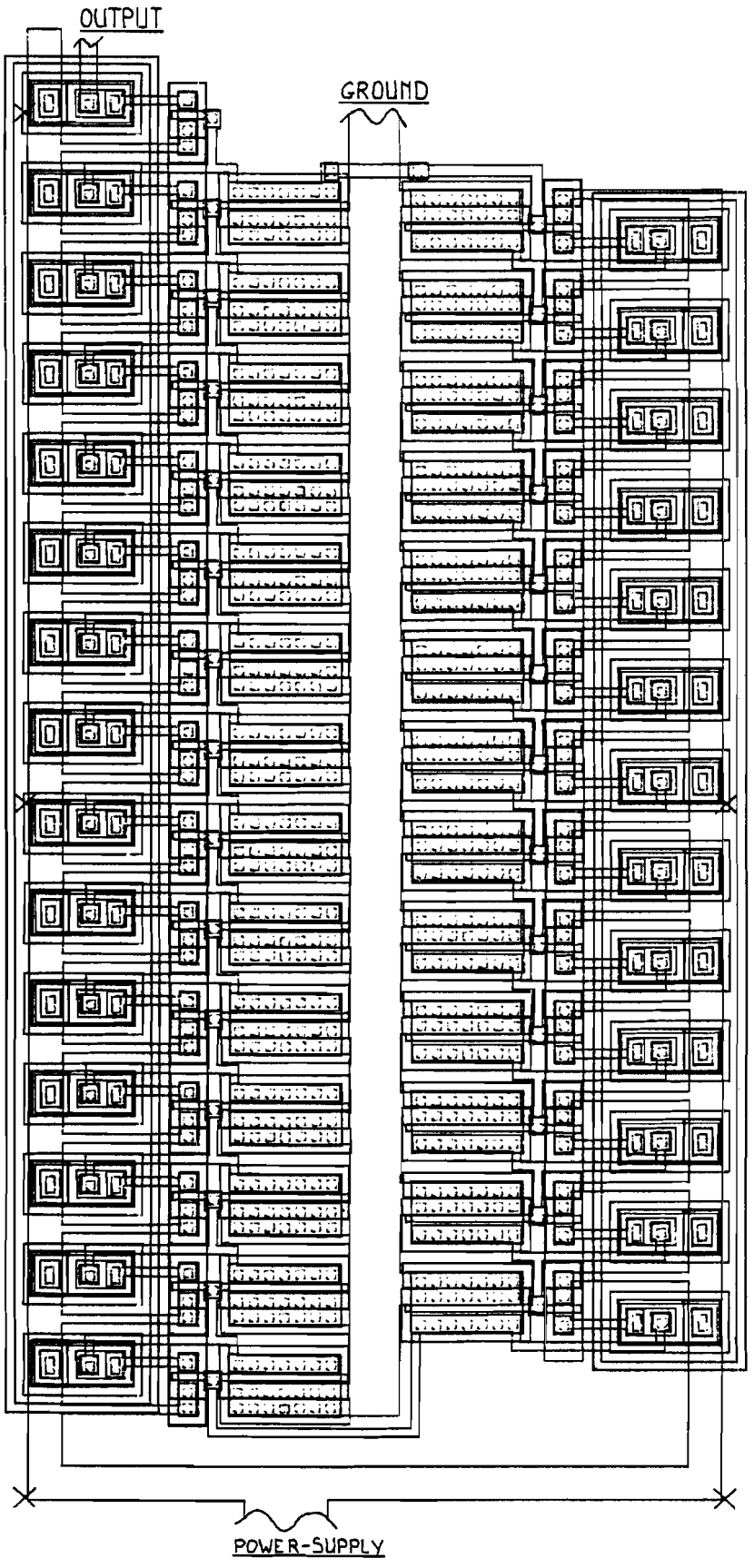


Fig. 5.7. Ringoscillator RING27

REFERENCES

[1] F.M. Klaassen "Halfgeleider electronica" Lecture notes T.H. Eindhoven, nr. 5.516, 1981.

[2] S.M. Sze "Physics of semiconductor devices" 2e edition. John Wiley and Sons 1981.

[3] F.M. Klaassen "Bouwstenen voor geïntegreerde schakelingen" Lecture notes T.H. Eindhoven, nr. 5.533, 1980.

[4] K. Tada, J.L.R. Laraya "Reduction of the storage time of a transistor using a Schottky-barrier diode" Proc. IEEE, nov. 1967 p. 2064.

[5] C500 design manual.

[6] Tentative design rules for the N***63 process.

APPENDIX A1

The differential equation is:

$$\frac{d^2 u_{ce}}{dt^2} + \frac{1}{\tau_F}\left(1 + \frac{\beta_F C_c}{C_c + C_L}\right)\frac{du_{ce}}{dt} = -\frac{\beta_F i_b}{\tau_F (C_c + C_L)} \qquad (1)$$

In the first place we have to solve the homogeneous d.e.:

$$\frac{d^2 u_{ce}}{dt^2} + \frac{1}{\tau_F}\left(1 + \frac{\beta_F C_c}{C_c + C_L}\right)\frac{du_{ce}}{dt} = 0 \qquad (2)$$

The characteristic equation, with its solutions is:

$$\lambda^2 + \lambda \frac{1}{\tau_F}\left(1 + \frac{\beta_F C_c}{C_c + C_L}\right) = 0 \qquad (3)$$

$$\lambda_1 = 0$$
$$\lambda_2 = -\frac{1}{\tau_F}\left(1 + \frac{\beta_F C_c}{C_c + C_L}\right)$$

Thus the solution of the homogeneous differential equation is:

$$u_{ce} = A + B \exp \lambda_2 t \qquad (4)$$

A particular solution is:

$$u_{ce} = -\frac{i_b \beta_F t}{C_L + (\beta_F + 1) C_c} \qquad (5)$$

The general solution now becomes:

$$u_{ce} = -\frac{i_b \beta_F t}{C_L + (\beta_F + 1) C_c} + A + B \exp \lambda_2 t \qquad (6)$$

From the initial conditions we obtain two equations in

A and B: $t=0: \; u_{ce} = u_B$ gives $u_B = A+B$

$$t=0: \; \frac{du_{ce}}{dt} = 0 \quad \text{gives} \quad B = -\frac{\beta_F \tau_F (C_c+C_L)}{[C_L+(\beta_F+1)C_c]^2}\, i_b$$

With these equations we find A:

$$A = u_B + \frac{\beta_F \tau_F (C_c+C_L)\, i_b}{[C_L+(\beta_F+1)C_c]^2}$$

Inserting the constants A and B in eq. (6) we obtain the complete general solution of the differential equation (1).

$$u_{ce} = u_B - \frac{\beta_F \tau_F (C_c+C_L) i_b}{[C_L+(\beta_F+1)C_c]^2} \left\{ \left[\frac{C_L+(\beta_F+1)C_c}{\tau_F (C_c+C_L} \right] t - 1 + \exp\left[\frac{-1}{\tau_F} \left(\frac{C_L+(\beta_F+1)C_c}{C_c+C_L} \right) t \right] \right\}$$

APPENDIX A2

In this appendix the general solution of the differential equation (36) in chapter 1 has been calculated. This equation is given below:

$$\frac{d^2u_c}{dt^2} + \frac{1}{\tau_F}\left[\frac{C_L+(\beta_F+1)C_c}{C_L}\right]\frac{du_c}{dt} = \frac{(\beta_F+1)}{C_L\tau_F}\, i_{bs} \qquad (1)$$

The homogeneous differential equation is:

$$\frac{d^2u_c}{dt^2} + \frac{1}{\tau_F}\left[\frac{C_L+(\beta_F+1)C_c}{C_L}\right]\frac{du_c}{dt} = 0 \qquad (2)$$

and the characteristic equation, with its solutions is:

$$\lambda^2 + \frac{1}{\tau_F}\left[\frac{C_L+(\beta_F+1)C_c}{C_L}\right]\lambda = 0 \qquad (3)$$

$$\lambda_1 = 0$$
$$\lambda_2 = -\frac{1}{\tau_F}\left[\frac{C_L+(\beta_F+1)C_c}{C_L}\right]$$

Thus the general solution of the homogeneous differential equation is:

$$u_c = A + B\exp\lambda_2 t \qquad (4)$$

A particular solution is:

$$u_c = \frac{(\beta_F+1)\, i_{bs}\, t}{C_L+(\beta_F+1)C_c} \qquad (5)$$

and the general solution now becomes:

$$u_c = \frac{(\beta_F+1)\, i_{bs}\, t}{C_L+(\beta_F+1)C_c} + A + B\exp\lambda_2 t \qquad (6)$$

With the initial conditions mentioned in chapter 1 we obtain two equations in A and B:

$$t=0:\ u_c=0 \qquad \text{gives} \qquad A+B=0$$

$$t=0:\ \frac{du_c}{dt}=0 \qquad \text{gives} \qquad B=\frac{\tau_F C_L(\beta_F+1)\,i_{bs}}{\left[C_L+(\beta_F+1)C_c\right]^2}$$

Now we find for A:

$$A=\frac{-\tau_F C_L(\beta_F+1)\,i_{bs}}{\left[C_L+(\beta_F+1)C_c\right]^2}$$

With the two constants A and B inserted in eq. (6) we find the complete general solution of the differential equatoin (1).

$$u_c=\frac{(\beta_F+1)C_L\tau_F i_{bs}}{\left[C_L+(\beta_F+1)C_c\right]^2}\left\{\left[\frac{C_L+(\beta_F+1)C_c}{C_L\tau_F}\right]t-1+\exp-\left[\frac{C_L+(\beta_F+1)C_c}{C_L\tau_F}\right]t\right\}$$

APPENDIX A3

In this appendix the general solution of the differential equation (42) in chapter 1 has been calculated.

$$\frac{d^2u_c}{dt^2} + \frac{1}{\tau_F}\left[\frac{C_L+(\beta_F+1)C_c}{C_L}\right]\frac{du_c}{dt} - r\frac{(\beta_F+1)}{C_L\tau_F}u_c = -r(u_B-V_T)\frac{(\beta_F+1)}{C_L\tau_F} \quad (1)$$

The homogeneous differential equation is:

$$\frac{d^2u_c}{dt^2} + \frac{1}{\tau_F}\left[\frac{C_L+(\beta_F+1)C_c}{C_L}\right]\frac{du_c}{dt} - \frac{r(\beta_F+1)}{C_L\tau_F}u_c = 0 \quad (2)$$

This gives the characteristic equation with its solution:

$$\lambda^2 + \frac{1}{\tau_F}\left[\frac{C_L+(\beta_F+1)C_c}{C_L}\right]\lambda - \frac{r(\beta_F+1)}{C_L\tau_F} = 0 \quad (3)$$

$$\lambda_{1,2} = -\frac{1}{2\tau_F}\left[\frac{C_L+(\beta_F+1)C_c}{C_L}\right] \pm \sqrt{\left(\frac{1}{2\tau_F}\left[\frac{C_L+(\beta_F+1)C_c}{C_L}\right]\right)^2 + \frac{r\beta_F+1}{C_L\tau_F}} \quad (4)$$

With this solution we can obtain the time-constants of the differential equation :

$$\tau_{1,2} = \frac{1}{\lambda_{1,2}} = \frac{C_L+(\beta_F+1)C_c}{2r(\beta_F+1)} \pm \sqrt{\left[\frac{C_L+(\beta_F+1)C_c}{2r(\beta_F+1)}\right]^2 + \frac{C_L\tau_F}{r(\beta_F+1)}} \quad (5)$$

The solution of the homogeneous equation now becomes:

$$u_C = A\exp t/\tau_1 + B\exp t/\tau_2 \quad (6)$$

A particular solution of the differential equation (1) is:

$$u_C = u_B - V_T \quad (7)$$

Addition of eq. (6) and eq. (7) gives the general solution of the differential equation:

$$U_C = U_B - V_T + A \exp t/\tau_1 + B \exp t/\tau_2 \qquad (8)$$

With the two initial conditions given in (43a) and (43b) we obtain two equations in A and B and so A and B can be found.

$t=0$: $U_C = V_0$ gives $A + B = V_0 + V_T - U_B$

$t=0$: $\frac{dU_C}{dt} = \frac{(\beta_F+1)\, ibs}{[C_L + (\beta_F+1)C_C]}$ gives $A + \frac{\tau_1}{\tau_2} B = \frac{\tau_1 (\beta_F+1)\, ibs}{C_L + (\beta_F+1)C_C}$

So we find: $A = \frac{\tau_1}{\tau_2 - \tau_1}\left(U_B - V_T - V_0\right) + \frac{\tau_1 \tau_2}{\tau_2 - \tau_1} \frac{(\beta_F+1)\, ibs}{C_L + (\beta_F+1)C_C}$

$$B = \frac{-\tau_2}{\tau_2 - \tau_1}\left(U_B - V_T - V_0\right) - \frac{\tau_1 \tau_2}{\tau_2 - \tau_1} \frac{(\beta_F+1)\, ibs}{C_L + (\beta_F+1)C_C}$$

and therefore the solution of the differential equation becomes:

$$U_C = U_B - V_T + \left[\frac{\tau_1}{\tau_2 - \tau_1}\left(U_B - V_T - V_0\right) + \frac{\tau_1 \tau_2}{\tau_2 - \tau_1} \frac{(\beta_F+1)\, ibs}{C_L + (\beta_F+1)C_C}\right] \exp t/\tau_1 \qquad (9)$$

$$- \left[\frac{\tau_2}{\tau_2 - \tau_1}\left(U_B - V_T - V_0\right) + \frac{\tau_1 \tau_2}{\tau_2 - \tau_1} \frac{(\beta_F+1)\, ibs}{C_L + (\beta_F+1)C_C}\right] \exp t/\tau_2$$

APPENDIX A4

In this appendix the first order differential equation given in equation (1) has been solved with the "separation of variables" method. This equation can be found in chapter 3 eq. (8).

$$\frac{dU_C}{dt} = \frac{\beta_\square W}{2C_L L}\left[U_C^2 - 2(U_B - V_{th})U_C\right] \qquad (1)$$

We first have to separate the variables u_C and t.

$$\frac{dU_C}{U_C\left[U_C - 2(U_B - V_{th})\right]} = \frac{\beta_\square W\, dt}{2C_L L} \qquad (2)$$

Writing the left term in eq. (2) in another way we obtain:

$$\frac{1}{2(U_B - V_{th})}\left[\frac{dU_C}{U_C - 2(U_B - V_{th})} - \frac{dU_C}{U_C}\right] = \frac{\beta_\square W\, dt}{2C_L L} \qquad (3)$$

Integration of the terms on both sides of the equation-sign gives:

$$\frac{1}{2(U_B - V_{th})} \ln\left[\frac{U_C - 2(U_B - V_{th})}{C_1\, U_C}\right] = \frac{\beta_\square W\, t}{2C_L L} \qquad (4)$$

This can be evaluated to:

$$U_C = (U_B - V_{th})\,\frac{2}{1 - C_1 \exp t/\tau} \qquad (5)$$

$$\text{with} \quad \tau = \frac{2C_L L}{(U_B - V_{th})\beta_\square W} \qquad (5a)$$

The constant C_1 can be solved by using the initial condition $u_C(0) = U_B - V_{th}$ and equals -1.
The output-voltage as a function of time thus becomes:

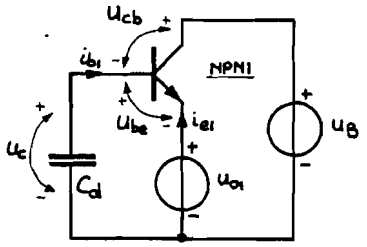
$$U_C = (U_B - V_{th})\,\frac{2}{1 + \exp t/\tau}$$

APPENDIX 5

In this appendix we examine the behaviour of the bipolar transistor in circuit 6, which is not driven by a MOS transistor. As the transistors NPN1 and NPN2 are connected in different ways (common collector and common emitter respectively), they will behave differently. Therefore we examine NPN1, when the output-voltage is pulled down and NPN2, when the output-voltage is pulled up. In this appendix we assume the output-voltage to be a linearly increasing or decreasing function of time:

$$u_o = \beta \pm \alpha t \qquad (1)$$

The first circuit to examine is given in fig. 1.



C_d = drain depletion-capacitance of PMOS1 (fig. 2.21)
U_{o1} = output-voltage $U_B - \alpha t$
U_B = 5V power-supply

fig. 1. NPN1, when NPN2 discharges the loadcapacitor in circuit 6

When we assume $u_{be} < V_T$ at t=0, the transistor equations for i_b and i_e become:

$$i_{b1} = C_e \frac{du_{be}}{dt} - C_c \frac{du_{cb}}{dt} \qquad (2)$$

$$i_{e1} = -C_e \frac{du_{be}}{dt} \qquad (3)$$

With

$$-\frac{du_{cb}}{dt} = \frac{du_{be}}{dt} + \frac{du_{o1}}{dt} \qquad (4)$$

we find an equation for the basecurrent i_{b1} :

$$i_{b1} = (C_e + C_c)\frac{du_{be}}{dt} + C_c\frac{du_{o1}}{dt} \qquad (5)$$

With

$$\frac{du_c}{dt} = \frac{du_{be}}{dt} + \frac{du_{o1}}{dt} \qquad (6)$$

we find a second equation for the base-current i_{b1}:

$$i_{b1} = -C_d\left(\frac{du_{be}}{dt} + \frac{du_{o1}}{dt}\right) \qquad (7)$$

The combination of eq. (5) and eq. (7) gives an equation for the base-emitter voltage:

$$\frac{du_{be}}{dt} = -\left[\frac{C_d + C_c}{C_d + C_c + C_e}\right]\frac{du_{o1}}{dt} \qquad (8)$$

The emitter-current thus becomes:

$$i_{e1} = \left[\frac{C_e(C_d + C_c)}{C_e + C_d + C_c}\right]\frac{du_{o1}}{dt} \qquad (9)$$

In eq.(8) we see, that the voltage-drop of u_o has been distributed over (C_d+C_c) and Ce. Equation (9) shows, that the bipolar transistor NPN1 behaves like a capacitor with the value of Ce in series with (C_d+C_c). For the buffer circuits this is a capacitance of 0.4 pF. When the base-emitter voltage exceeds V_T, the transistor equations to be used are:

$$i_{b1} = \frac{q_F}{\tau_F} + \frac{dq_F}{dt} - C_c\frac{du_{cb}}{dt} \qquad (10)$$

$$i_{e1} = -\left[(\beta_F + 1)\frac{q_F}{\tau_F} + \frac{dq_F}{dt}\right] \qquad (11)$$

Assuming $U_{cb}=U_{ce}$, we find a second equation for the base-current i_{b1}:

$$i_{b1} = -C_d\frac{du_{o1}}{dt} \qquad (12)$$

With eq.(10), eq.(11) and eq.812) we obtain:

$$q_F = \frac{\tau_F}{\beta_F}\left[(C_d + C_e)\frac{du_{o1}}{dt} - i_{e1}\right] \qquad (13)$$

and $$\frac{dq_F}{dt} = \frac{\tau_F}{\beta_F}\left[(C_d+C_e)\frac{d^2u_{o1}}{dt^2} - \frac{di_{e1}}{dt}\right] \qquad (14)$$

As we have assumed the output-voltage u_{o1} to be a linear function of time, $\frac{d^2u_{o1}}{dt^2}$ equals zero.
When we insert eq.(13) and eq.(14) in eq.(11) we obtain a differential equation for the emitter-current i_{c1}:

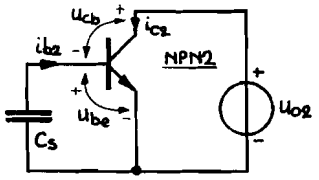
$$\tau_F \frac{di_{e1}}{dt} + i_{e1} = (\beta_F+1)(C_d+C_c)\frac{du_{o1}}{dt} \qquad (15)$$

With the initial condition $i_{c1}(0)=0$, the solution of this differential equation becomes:

$$i_{e1} = (\beta_F+1)(C_d+C_c)(1-exp^{-t/\tau_F})\frac{du_{o1}}{dt} \qquad (16)$$

For $t > 5\tau_F$ the exponential term can be neglected with respect to 1. In this case, the bipolar transistor behaves like a capacitor with the value of $(\beta_F+1)(C_d+C_c)$. For the buffer circuits this is a capacitance of 50 pF.

When the output-voltage is pulled up by the bipolar transistor NPN1, while NPN2 is not driven by NMOS4, we can examine the behaviour of NPN2 with the circuit given in fig. 2.



C_s= source depletion-capacitance of NMOS4.
U_{o2}= output voltage $\propto .t$

fig. 2. NPN2, when NPN1 charges the load-capacitor in circuit 6.

The calculations for this circuit are similar to the previous ones for the circuit in fig. 1. For $U_{be} < V_T$ we find for u_{be} and i_{c2}:

$$\frac{du_{be}}{dt} = \left(\frac{C_c}{C_s+C_e+C_c}\right)\frac{du_{o2}}{dt} \qquad (17)$$

and

$$i_{c2} = \left(\frac{C_c(C_s+C_e)}{C_c+C_s+C_e}\right)\frac{du_{o2}}{dt} \qquad (18)$$

In this situation the bipolar transistor behaves like a capacitor consisting of C_c in series with (C_e+C_s). For the buffer circuit this is approximately 0.36 pF.
When u_{be} exceeds V_T, we obtain with calculations similar to the previous ones an equation for the collectorcurrent i_{c2}:

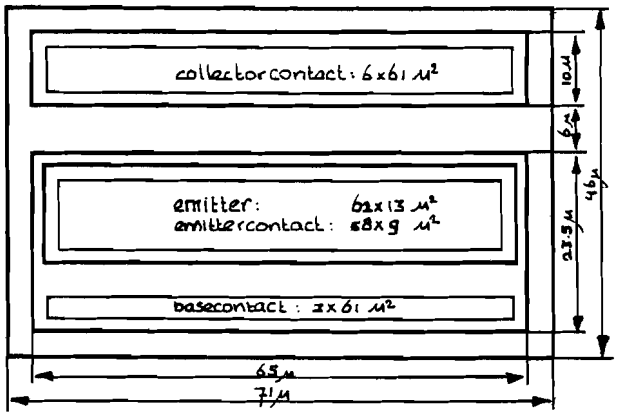
$$i_{c2} = (\beta_F+1)C_c\left(1-\exp -t/\tau_F\right)\frac{du_{o2}}{dt} \qquad (19)$$

For $t > 5\,\tau_F$ the exponential term can be neglected again and then the bipolar transistor behaves like a capacitor with the value of $(\beta_F+1).C_c$. For the buffer circuit this is a value of approximately 44 pF.

APPENDIX B1

The parameters of the bipolar transitors with emitterarea of 800 μm^2.

The parameters listed in the following table are used in the PHILPAC-model TNS level 1. This is a model of a bipolar vertical NPN transistor with substrate connection. One of the transistors is combined with a Schottky diode and therefore the geometry has been changed a little, which caused the collector and substrate depletion capacitors to be increased. The parameters of both transistors are listed and the significant dimensions are given in the figures.



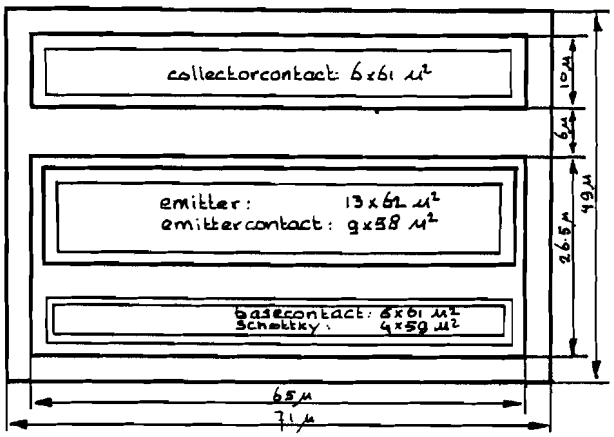


Table with the parameters of the bipolar transistor with emitterarea of 800 μm^2

Description	Symbol	Dimension	Without Schottky	With Schottky
Saturation current	I_O	aA	400	400
Forward current-gain	β_F	-	100	100
Forward early-voltage	V_{eaf}	V	50	50
Reverse current-gain	β_R	-	7	7
Substrate current-gain	β_{CS}	-	12	12
Collector series-resistance	R_{CC}	Ω	4.6	4.6
Base series-resistance	R_{bc}	Ω	250	250
Emitter series-resistance	R_e	Ω	0.7	0.7
Forward transit-time	τ_F	pS	50	50
Zero-bias emitter depletion capacitance	C_{JE}	pF	2	2
Emitter-junction diffusion-voltage	V_{DE}	V	0.66	0.66
Emitter grading-coefficient	P_E	-	0.33	0.33
Inverse transit-time	τ_R	pS	500	500
Zero-bias collector depletion-capacitance	C_{JC}	pF	0.44	0.50
Collector-junction diffusion-voltage	V_{DC}	V	0.62	0.62
Collector grading-coefficient	P_C	-	0.5	0.5
Zero-bias substrate depletion-capacitance	C_{JS}	pF	0.60	0.63
Substrate-junction diffusion-voltage	V_{DS}	V	0.46	0.46
Substrate grading-coefficient	P_S	-	0.33	0.33

APPENDIX B2

The parameters of the bipolar transistors with emitter area of 50 μm^2

The parameters listed in the table are used in the PHILPAC-model TNS level 1. The transistor with emitter area of 50 μm^2 is the minimum bipolar transistor that can be realized with the BIMOS-process. There are two versions listed: one without and one with a Schottky diode between the base and the collector.
The significant dimensions are given in the figures.

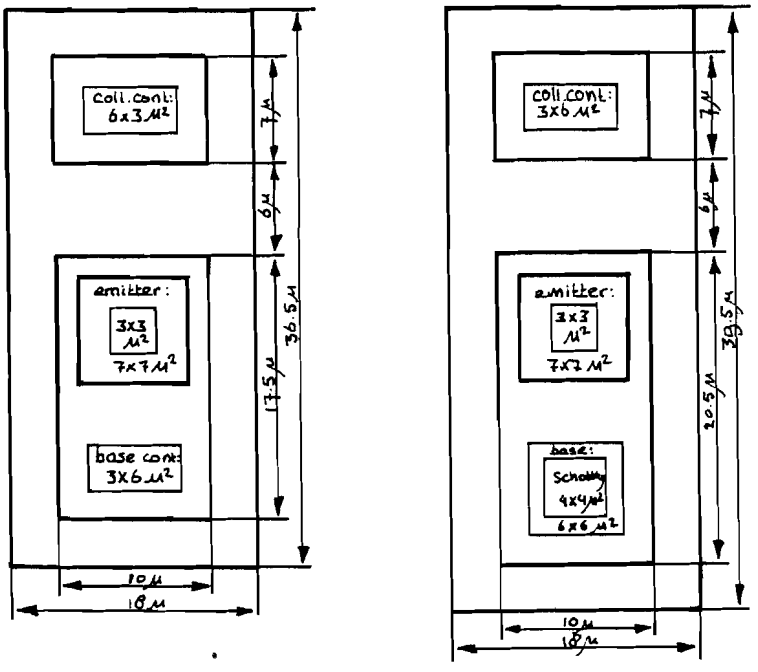


Table with the parameters of the minimum bipolar transitors

Description	Symbol	Dimension	Without Schottky	With Schottky
Saturation-current	I_O	aA	25	25
Forward current-gain	β_F	-	100	100
Forward early-voltage	V_{eaf}	V	50	50
Reverse current-gain	β_R	-	7	7
Substrate current-gain	β_{cs}	-	12	12
Collector series-resistance	R_{cc}	Ω	34	34
Base series-resistance	R_{bc}	Ω	1255	1255
Emitter series-resistance	R_e	Ω	33	33
Forward transit-time	τ_F	pS	50	50
Zero-bias emitter depletion capacitance	C_{JE}	fF	165	165
Emitter-junction diffusion-voltage	V_{DE}	V	0.66	0.66
Emitter grading-coefficient	P_E	-	0.33	0.33
Inverse transit-time	τ_R	pS	500	500
Zero-bias collector depletion-capacitance	C_{JC}	fF	65,	75
Collector-junction diffusion-voltage	V_{DC}	V	0.62	0.62
Collector grading-coefficient	P_C	-	0.5	0.5
Zero-bias substrate depletion-capacitance	C_{JS}	fF	245	260
Substrate-junction diffusion-voltage	V_{DS}	V	0.46	0.46
Substrate grading-coefficient	P_S	-	0.33	0.33

APPENDIX B3

The parameters of the MOS-transistors

The parameters listed in the table are used in the PHILPAC-models MN and MP level 7. These are models describing short channel NMOS and PMOS transistors respectively. The models have been extended as explained in section 1.5 and the parameters of the extra components are given in a second table.

Table with parameters of NMOST and PMOST

Description	Symbol	Dimension	MN (NMOST)	MP (PMOST)
Zero-bias threshold-voltage	V_{TO}	V	0.75	1.1
Active-gate capacitance	C_{ox}	$fF/\mu m^2$	0.68	0.68
Body-factor	K	$\sqrt{V}$	0.31	0.75
Channel-length	L	μm	2	2
Square gain-constant	β_o	$\mu A/V^2$	45	15
Channel-width	W	μm	-	-
Mob.red.factor normal field	θ_A	1/V	0.06	0.11
Mob.red. factor lateral-field	θ_C	1/V	0.13	0.05
Static feedback-fact.	γ	-	0.06	0.05
Diffusion-potential	2φ	V	0.65	0.65
Gain-ratio	ratio	-	1	1
Flat-band voltage	V_{FB}	V	-0.8	0.3
Gate-source overlapp	C_{GSO}	fF/μm	0.272	0.408
Gate-drain overlapp	C_{GDO}	fF/μm	0.272	0.408

Extra parameters for extended models

Gate-substrate cap.	C_{gsub}	fF/μm	1.36	1.36
Source and Drain diodes :				
Saturation-current	I_O	fA/μm	0.7	0.7
Junction emission-coeff.	M		1	1
Seriesresistor	Rs	Ω	0	0
Transit-time		nS	1	1
Zero-bias depl. cap.	C_O	fF/μm	0.595	1.75
Diffusion-voltage	V_D	V	0.8	0.8
Grading-coefficient	P		0.5	0.5