

MASTER

A digital-to-analog converter and central controller for a slope adaptive delta modulator

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Eindhoven University of Technology
Department of Electrical Engineering
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**A Digital-to-Analog Converter and Central Controller
for a Slope Adaptive Delta Modulator**

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PREFACE

In this master theses report the design of an 8-bit digital-to-analog converter (DAC) is described. In addition a central controller concept is presented. DAC and controller are subcircuits of a single chip *Slope Adaptive Delta Modulator* (SADM), intended as analog-to-digital converter in an ISDN communication system.

The purpose of the DAC in the SADM is to translate the binary weighted contents of the accumulator into a proportional analog voltage. The controller provides clock-signals which controls the timing of individual subcircuits, and synchronizes the SADM timing process with the ISDN channel code.

The report is divided in three parts. After a general introduction to the SADM system in part I, where the function of all subcircuits is portrayed, the DAC design is subject in part II. First the relation of DAC parameters with the overall SADM system performance is established. Optimal values are derived theoretically and checked against simulation results. Next the realization of the DAC as a so-called charge redistribution converter is given, built with a weighted parallel capacitor array. Design objects are minimal area and high accuracy. It will be shown that capacitor ratio errors are the major limiting factor in the final circuit layout.

Part III is devoted to the central controller. Here the design objects are flexibility and high capacitive load capability of the clock circuits. A novel gate construction is introduced, based upon a bootstrap circuit arrangement. The controller incorporates a clock recovery network, a 15-bit cyclic shift-register and two four-phase clock circuits.

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PART I ISDN PROJECT

CHAPTER 1 INTRODUCTION

1.1 PROJECT OVERVIEW

In 1986 a research program was started at the Electronic Circuit Design Group (EEB), at the department of Electrical Engineering of the Eindhoven University of Technology (TUE), designated as the ISDN project. In this project master graduates participate in the development of a communication IC, compatible with the initial proposed ISDN standards. The design effort has been concentrated on the development of an analog-to-digital converter, employing delta modulation converter techniques. A special variant of delta modulation is used, a so-called Slope Adaptive Delta Modulator. Ultimately the design effort cumulates in a physical layout on transistor level, used to produce circuits in NMOS technology. The production of the IC's is done by EFFIC (Eindhoven Fabrication Facility for IC's).

Next to the intention of actually producing an ISDN communication IC, the tutorial aspects are a major program goal. Gaining experience in the design of large, mixed analog - digital circuits, proceeding through the whole IC design process, pushing the limits of the EFFIC NMOS fabrication process, are examples of these aspects.

Until now ten students have been working at the project, each for a time period of six to nine months. To work effectively, the digital-to-analog converter has been divided in several functional modules, called subcircuits. A subcircuit performs a specific largely autonomous task. The following subcircuits can be identified;

- anti-alias input filter (IF)
- active loop-filter (LF)
- analog-to-digital converter (ADC)
- digital accumulator (ACCU)
- digital-to-analog converter (DAC)
- control logic (CL)

As soon as the design of a module has reached its final state (layout), it is fabricated by the EFFIC, thus enabling a fast feedback from measurements. For all subcircuits, designs have already been made, references [1] to [12]. However due to new insights in circuit structure and the gained experience in the development, major parts of the delta modulator had to be redesigned. These include analog-to-digital converter, accumulator, digital-to-analog converter and control logic. The last two are treated in this report. Redesigns of ADC and ACCU can be found in references [11] and [12].

Following a theoretical analysis, the modulator was simulated with a high-level simulator; TON.SIM (Ref. [5]), used to establish optimal values for the characteristic modulator parameters. For this, functional descriptions in PASCAL were made for all modules. On a lower level, in the design of individual subcircuits, the well known circuit-simulator SPICE has been used extensively. Other design-tools are the switch-level simulator SLS and the layout editor EULER with accompanying SPICE circuit extractor.

The complete modulator will be placed into a 24 pin ceramic IC package. Three supply connections are needed and two ground pins; analog ground and digital ground. The remaining nineteen pins are used for input, output and to facilitate test applications.

The global IC specifications are summarized below.

power supply voltage	+ 5 Volt, $\pm 10\%$ - 5 Volt, $\pm 10\%$
reference voltage	+ 2 Volt, $\pm 0.1\%$ (0°C to 70°C)
digital output	3 bit logarithmic + sign 8 bit linear + sign (optional)
dynamic range	> 48 dB
sample frequency	64.000 KHz
master clock frequency	4.096 MHz

1.2 THE INTEGRATED SERVICES DIGITAL NETWORK

Communications facilities supporting user applications are numerous and diverse. The communication systems are supported by analog dial-up telephone lines, supporting voice and/or data, requiring different types of interfaces. In addition, many telephone companies have dedicated leased lines, either analog or digital, or perhaps a combination of both. Added to these systems are the older TELEX services, facsimile, packet switched lines etc. This range of different system creates many types of access problems. In many instances, different protocols are required. Moreover, different types of lines are needed to support these devices. Consequently there is a great need for one standard to organize the above pictured diversity, ISDN provides that standard.

Digital telephony is extending nowadays almost to the subscribers premises. The Integrated Services Digital Network (ISDN) extends the digital connectivity from end to end user. ISDN is centered on three main areas: (1) the standardization of services offered to subscribers in order to foster international compatibility; (2) the standardization of user-to-network interfaces in order to foster independent terminal equipment and network equipment development; and (3) the standardization of network capabilities in order to foster user-to-network and network-to-user communications. ISDN will support service for voice, data, text, graphics, music and video, all transmitted digitally. It uses the common telephone wiring and a standard interface plug.

The basic end-user ISDN terminal, called TE (Terminal Equipment), is connected to the ISDN channel through a twisted pair 4-wire digital link. This link uses time-division multiplexing to provide three channels, designated B, B and D (or 2B+D). The B channels operate at a speed of 64,000 Kbits/s; the D channel operates at 16,000 Kbits/s. Up to eight TE's share one basic 2B+D channel. In addition to these channels, ISDN provides for framing control and other overhead bits, which totals to a 192 Kbit/s bitrate. The B channels are intended to carry user information streams. They provide for several different kinds of applications support. For example, channel B can provide for voice at 64 Kbit/s. The D channel is intended to carry control and signalling information. Other ISDN channels (E and H) are intended for faster speeds and are derived from multiple B channels.

CCITT recommendations I.110 – I.464 (Ref. [21]) cover the ISDN standards. The additional CCITT recommendation G.712 is of particular interest here as it provides technical performance standards for digital equipment.

The analog-to-digital converter designed by graduates at EEB is intended as part of a TE; an interface between existing analog telephone equipment and the basic ISDN channel 2B+D. It must perform the conversion from analog speech, bandlimited to 4 kHz, to digital code, compatible with the ISDN standards.

CHAPTER 2 SLOPE ADAPTIVE DELTA MODULATOR

2.1 SYSTEM DESCRIPTION

Delta Modulation (DM) is a variation of Puls Code Modulation (PCM). It is based upon the same principle of digital modulation where the message is represented by a coded group of digital (discrete-amplitude) pulses. The distinct difference between DM and PCM is that in contrast to PCM where sampled values of the message are coded, in DM the difference between two successive samples is coded. In general differences can be coded with fewer bits; indeed, only one bit is required in a conventional delta modulator.

Figure 2.1 is the functional block diagram of a basic delta modulator. The message $x(t)$ is compared with a stepwise approximation $x_a(t)$ by subtraction. The difference is being passed through a hard limiter whose output equals $\pm\Delta$ depending on the sign of $x(t) - x_a(t)$. This, in turn, modulates an ideal sampling wave $s_\delta(t)$ to produce $x_p(t)$ a periodic pulse train from which $x_a(t)$ is generated by integration. Since there are only two possible pulse weights in $x_p(t)$, it can be coded with a singular bit. The demodulator (Fig. 2.1b) consist of an integrator and low-pass filter, yielding $x(t)$ plus quantization noise.

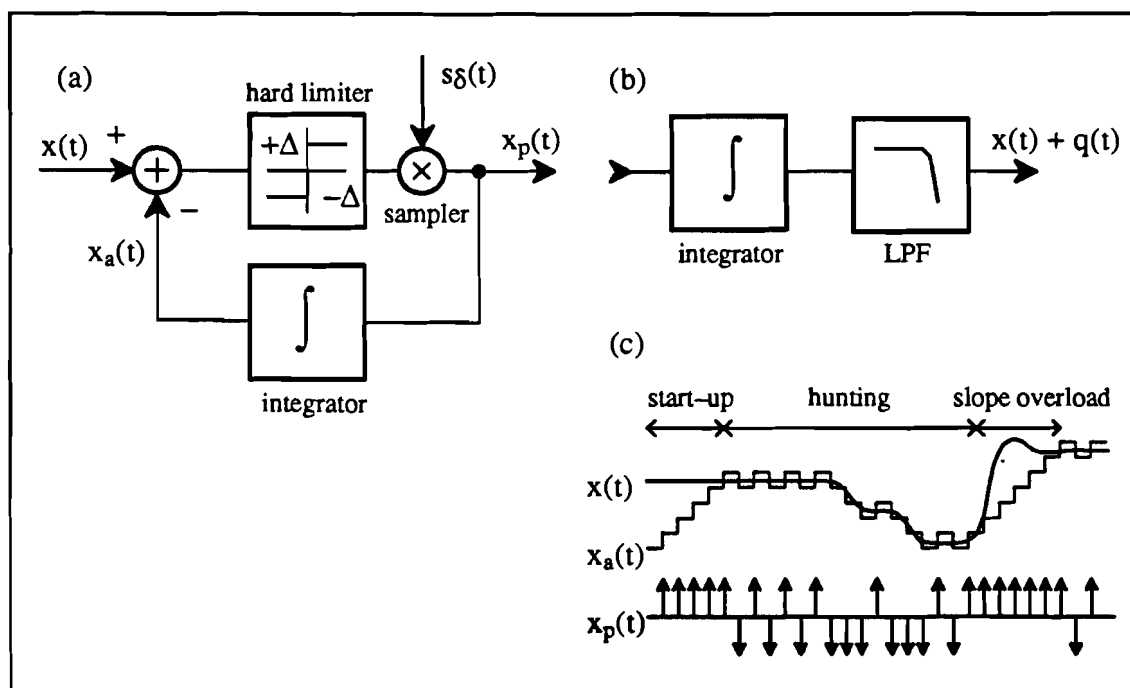


Figure 2.1 Delta modulation. (a) Modulator; (b) demodulator; (c) waveforms.

A basic limitation of DM is the slope-overload phenomenon, illustrated in figure 2.1 (c). It occurs when the rate of change of $x(t)$ is too great. To prevent slope-overload, $f_s \Delta$ must be greater than $2\pi A W$ (where f_s is the sampling frequency, A is the maximum signal amplitude and W is the message bandwidth), in general demanding a very high sampling frequency (Ref. [20]).

Delta modulation has the advantage of greatly simplified hardware. In exchange for these equipment savings, DM generally requires a larger transmission bandwidth than

PCM. For voice signals, however, a novel method of DM utilizing a Slope Adaptive Delta Modulator approach first described by Giancarlo and Sodini, Ref. [15], has brought the bandwidth requirement down to a point where DM is a strong competitor of PCM. The ISDN project at the Electronic Circuit Design Group makes use of a DM based upon the same concept. The new modulator requires a far lower sampling rate than the conventional modulator of figure 2.1. This improvement is brought about through the use of a slope adaptive modulation technique.

The simplified hardware needed in a delta modulator as compared to a PCM system is a direct consequence of the oversampled nature of the DM. First, a high sample frequency makes the design of an anti-alias input filter much easier. A first order low-pass filter provides sufficient attenuation of aliasing components because the sample frequency is substantially higher than the Nyquist rate ($2 \times$ message bandwidth). Also the modulator itself provides some band limiting.

Second, the modulator does not require high-accuracy components to produce a high-accuracy signal (Ref. [15]). Errors in the various modulator blocks in general cause small gain errors and some minimal shifting in frequency response of the modulator. Uncorrelated random errors are partly compensated by the averaging effect of an over-sampled modulator/demodulator system.

Third, it requires no prefilters to reject low frequencies such as 50 Hz and DC. The signal-to-noise ratio for low frequencies is extremely high. Furthermore no μ -law or A-law encoding is necessary because the proposed DM has a built-in compressed coding characteristic. Smaller, more frequently occurring, amplitude samples are coded more accurately.

Finally because of its simple structure, it lends itself well to a straightforward implementation in an NMOS monolithic circuit containing also digital signal processing elements. In the next paragraph the individual subcircuits of the SADM as designed by the student participants of the ISDN project, are described.

2.2 SUBCIRCUIT DESCRIPTION

A block diagram of the new modulator is shown in figure 2.2, the different blocks represent functional subcircuits. This system uses a sample rate of 64 kHz to encode a voice band signal bandlimited to approximately 4 kHz. After a brief system portrayal, details of all subcircuits will be given.

Following the signal path in figure 2.2, the input signal is first fed through a simple first-order low-pass filter providing 21 dB attenuation at 60 kHz to prevent aliasing. The signal is then fed to the modulator consisting of an analog active filter (switched-capacitor), a logarithmical weighted quantizer (ADC), a digital accumulator and a digital-to-analog converter (DAC). The DAC converts the output of the accumulator into an analog signal which is fed back and subtracted from the input signal. A processable code can be extracted from either the ADC or the accumulator. The encoder yields a code which is the derivative of the input signal while the code of the accumulator gives the value of the input signal.

A Anti-alias filter

A prefilter is required to remove aliasing components in the input signal. To provide an acceptable signal quality these components should be at least attenuated by 30 dB prior to downsampling (CCITT recommendation). Assuming a voice band of 4 kHz and sampling rate of 64 kHz, input signals with frequencies higher than 60 kHz fold

back in the voice band due to the sampling. Thus band limiting must take place at 60 kHz. The loop provides some 9 dB attenuation at 60 kHz. So the prefilter at the input of the SADM must provide at least 21 dB attenuation at this frequency. A first order time continuous low-pass filter with corner frequency $f_c=5.7$ kHz, and an optional switched-capacitor pre-emphasis filter are described in reference [6]. The low-pass filter is placed outside the chip.

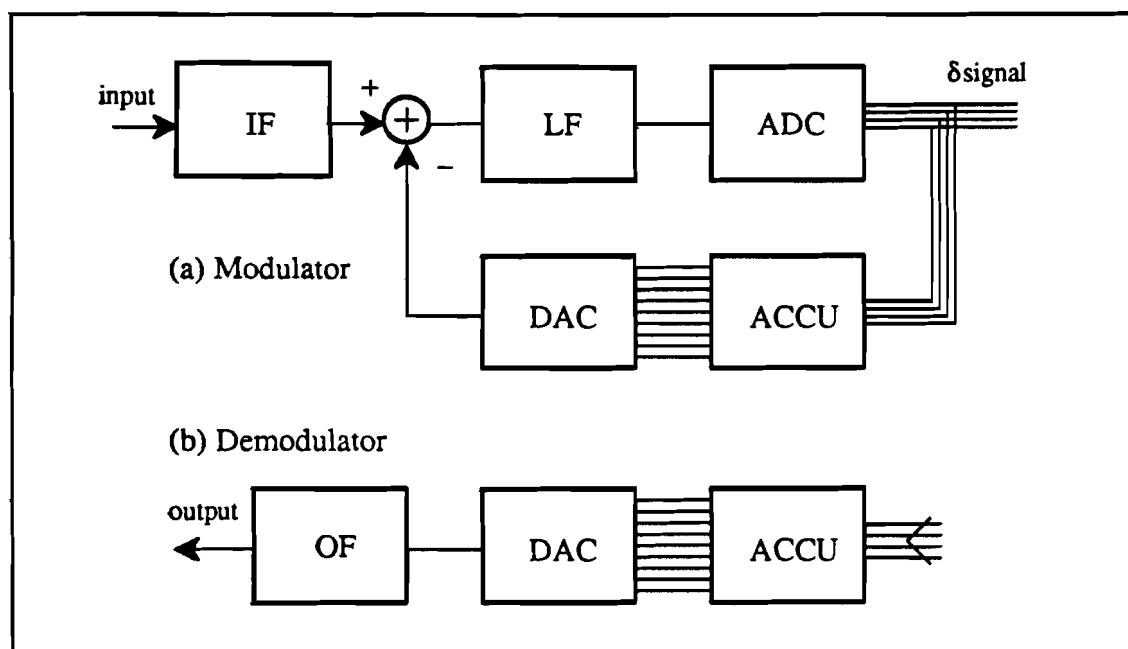


Figure 2.2 Block diagram of the SADM. (a) Modulator; (b) demodulator.

B Active loop-filter

The loop-filter is one of the key subcircuits in the SADM. It has to perform several partwise conflicting functions;

- Suppression of quantization noise generated in the ADC.
- Stabilization of the loop.
- Ensure a fast step-response.
- Preventing slope-overload.

A first order PI controller is used for this application. The proportional part reflects the trade-off between prevention of slope-overload and large signal-to-noise ratio. The integral part reflects the trade-off between large signal-to-noise ratio, stability and fast step-response. Initial optimal loop parameters were derived by Koenen, Ref. [3]. In reference [10] a switched capacitor realization is given. The subtractor is integrated in the loop-filter design. In part II of this report a more detailed description is given.

C Analog-to-digital converter

This is the other key subcircuit of the SADM. A binary weighted logarithmic quantizer using 7 positive and 7 negative reference levels is used. The levels in the ADC are companded such that each successive reference level is twice as large as the previous one. Thus each level is related to a binary power and is, therefore, related to a binary digit location in a 7-bit word. As only 14 different words are

possible they can be coded with $3+1=4$ bits (1 sign-bit). This signal can be transmitted to the ISDN channel.

The magnitude of a signal presented at the input of the ADC is proportional to the change, relative to a sample period, of the input signal (its slope). In contrast to a conventional DM where only one bit is used to code the slope (positive or negative), now 4 bits are available. The ADC output is thus dependent of the slope of the input signal and therefor the modulator is called slope adaptive. As a result the sampling frequency, compared with a 1-bit DM, can be much lower.

Through the use of logarithmic spaced reference levels the first level can be very small, while still large changes of the input signal can be followed with the courser steps. Thus for low level, low frequency signals (small slope) the quantization noise is very small. For speech, characterized by large crest-factors, this will be the normal operating mode of the SADM. So the increase in quantization noise or deterioration of coding accuracy which results for large changes of the input signal, in practice only occurs occasionally.

The choice of ADC parameters in relation with the other system parameters is described in part II. In references [9] and [12] different realizations are given, showing the development of the ADC as the ISDN project progressed.

D Digital accumulator

The output of the ADC is a weighted digital representation of the change, relative to one sampling period, of the input signal. In order to be able to produce this difference signal, an estimated value of the input signal delayed by one sample period has to be presented to the subtractor. Thus the difference signal must be delayed and converted to an amplitude sample, the conversion is the function of the accumulator analogue with integration in the time domain (Fig. 2.1)

The basic operations that take place in the accumulator are addition and storage of the result. If the difference signal produced by the ADC is negative, this value is added to the current accumulator contents, for positive input the value is also added. Each new ADC code word updates the accumulator contents, an estimated value of the SADM input signal.

As was noted earlier the ADC bears a special relation with the accumulator; every ADC code word is related to a digit location in the accumulator. The ADC and accumulator work together to add or subtract a "1" from a single bit position in the accumulator at each sample interval. The output of the accumulator is a 2-complement digital code as this makes its design easier. This signal can also be used as output to the ISDN channel. The high bit-rate of N times the sample frequency, where N is the accumulator length, can be lowered with subsequent decimation filters and resampling at a lower rate, if necessary.

Important features of the accumulator are the addition of a so-called "leak-bit" and its length. As difference signals are transmitted, transmission errors result in a defective new accumulator content; it is offset by the error value. In contrast to PCM where only one amplitude sample is affected, the error is maintained forever in a DM system. If a transmission error is present in the most significant bit, clipping of the demodulator is possible. So the demodulator must incorporate some error correction mechanism; the accumulator in the demodulator must slowly forget its past. Hence an extra bit is added to the accumulator, with half the significance of the accumulator's LSB. If the new accumulator contents is positive the leak-bit is

subtracted at each sample interval, for negative accumulator contents the leak-bit is added. For the modulator the leak-bit is not necessary as the feedback loop effectively eliminates all offset voltages. To maintain symmetry the leak-bit must also be incorporated in the modulator. Simulations (Ref. [2]) show that the system performance is not significantly effected by the presence of the leak.

The length of the accumulator determines the dynamic range of the modulator. To be comparable with a standard 8-bit PCM system, a dynamic range of 48 dB is a minimum requirement. In part II it will be shown that 54 dB is achievable.

References [2] and [11] are devoted to the design of the accumulator, in reference [11] the latest version is described.

E Digital-to-analog converter

In the DAC the output of the accumulator is translated into its analog complement, which is next presented to the subtractor. Conversion of the leak-bit is not necessary, so the DAC length is one bit smaller then the accumulator length. As this report is mainly devoted to the design of the DAC, see part II for a specific explanation. An earlier design is given in reference [1].

F Central control unit

In figure 2.3 the timing diagram of the SADM is illustrated, showing the location of all active intervals off the former subcircuits in one sample period. The function of the controller is to supply clock signals which ensure the successive timing termination. The controller can be divided in a global part consisting of a clock recovery network (reference [8]) and circuits providing basic clock signals. The second part is an array of local controllers, located close to, and assigned to each subcircuit. Here subsequent processing of the basic clock signals is performed, reflecting the need for specific clock signals for each subcircuit. In part III of this report an implementation of the global controller is presented. Considerable parts of the controller already are designed, references [4] and [7], but as will be shown in part III, are unsatisfactory.

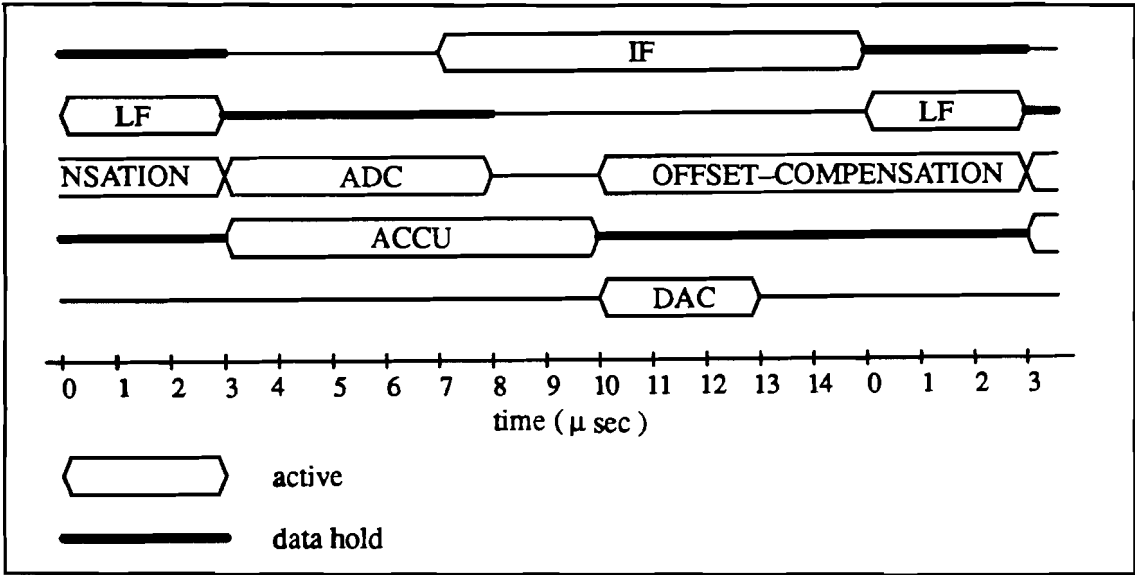


Figure 2.3 SADM timing diagram

2.3 SADM MODEL

For purposes of signal and noise analysis the modulator can be represented by the equivalent diagram of figure 2.4. In this diagram the signal is filtered, then ideally sampled by the analog-to-digital converter with quantization noise component $E_q(s)$. The digital accumulator and digital-to-analog converter are represented by an analog integrator whose input is a train of weighted pulses from the sampler. The output of the actual modulator is a series of digital values which represents the analog values exiting the analog integrator. Thus, we must filter the output of the analog integrator in figure 2.4 by an inverse $\sin(x)/x$ function in order to obtain the transfer function of the actual modulator. In this model we can identify; the PI controller parameters β and τ ; and the amplification constant α , which is the ratio of LSB voltages in DAC and ADC multiplied by a loop delay coefficient.

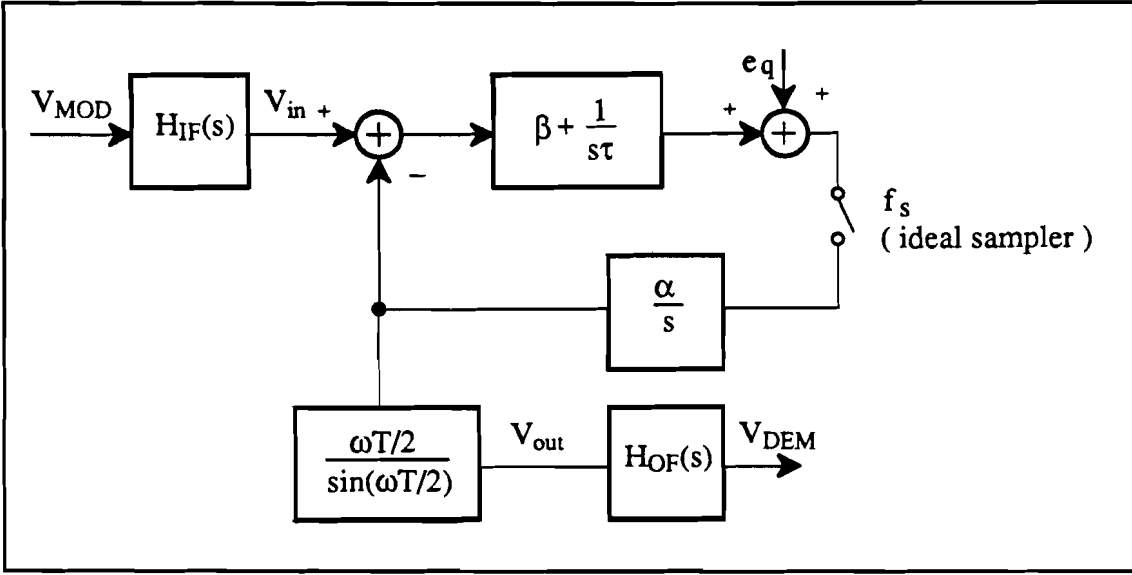


Figure 2.4 Equivalent circuit diagram of the SADM, continuous-time model

In earlier reports (references [2], [3] and [9]) a discrete-time model of the SADM is used, figure 2.5. Here the transfer function of a subcircuit is described by the z-transform ratio of sampled output and input signal sequences. In doing so the exact stability criteria for the SADM can be more easily derived. Also this model represents the actual physical structure of the SADM more accurately. In part II of this report both models are used, figure 2.4 for signal analysis purposes and figure 2.5 for the calculation of stability criteria and optimal modulator parameter values. The discrete-time model was developed without reference to the continuous-time model, consequently there is only a functional relationship between equivalent modules in the two models. These functional relationships are (for $b=1$):

$$\beta + \frac{1}{s\tau} : \text{loop-filter} \longrightarrow K_{LF} \frac{z - a}{z - 1}$$

$$\alpha_0 e^{-sT_s} : \text{gain constant} \times \text{loop-delay} \longrightarrow \frac{V_{dac}}{V_{adc}} \frac{1}{z}$$

$$\frac{1}{sT_s} : \text{integrator} \longrightarrow \frac{z}{z - 1}$$

As we want to find the relation between the continuous-time parameters (β and τ) and the discrete-time parameters (a , b and K_{LF}) as used in previous SADM reports, the bilinear s - z transformation is employed to transform the continuous-time loop-filter transfer function. The bilinear transformation is used because the loop-filter is designed using this transformation (Reference [3]). For $b=1$ the result is:

$$\beta = \frac{K_{LF} (1 + a)}{2} \quad [2.1]$$

$$\tau = \frac{1}{K_{LF} (1 - a) f_s} \quad [2.2]$$

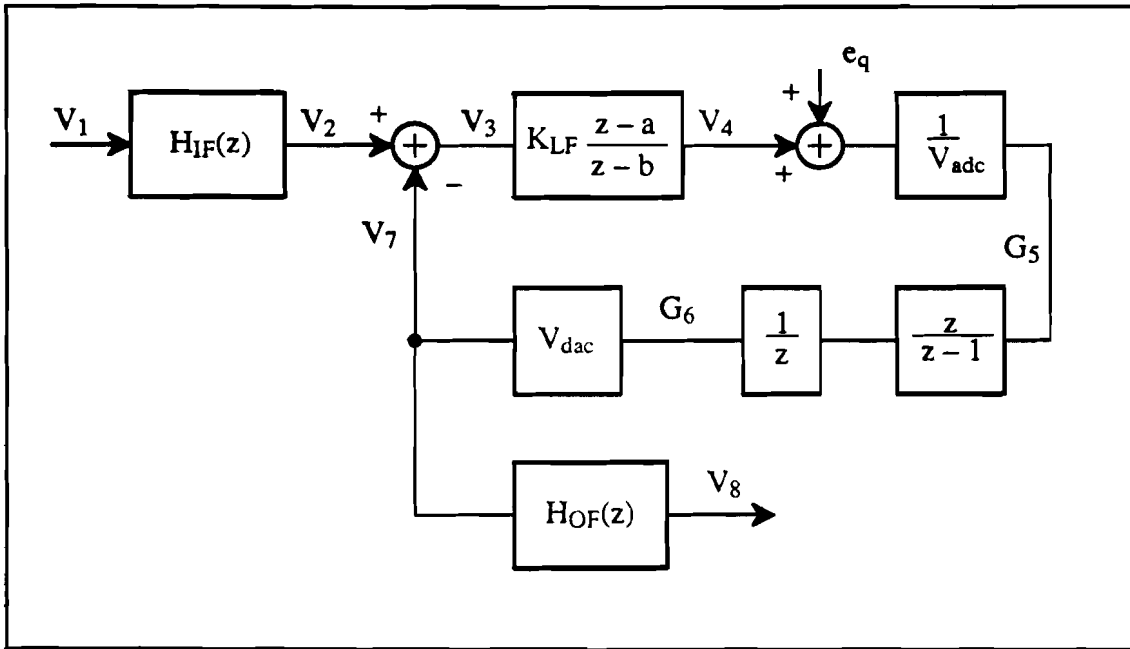


Figure 2.5 Equivalent circuit diagram of the SADM, discrete-time model

PART II DIGITAL TO ANALOG CONVERTER

CHAPTER 1 INTRODUCTION

1.1 FUNCTIONAL DESCRIPTION DAC

The purpose of the digital to analog converter in the delta modulator is to translate the binary weighted contents of the accumulator into a proportional voltage. This must be accomplished within the allowed conversion time of 3 μsec and ideally the output signal should be the same as the input signal delayed by one clock cycle. Referring to figure I2.5:

$$V_7(nT) = V_2(n(T-1)) \quad \text{hence } V_7(z) = z^{-1}V_2(z) \quad [1.1]$$

Equation [1.1] applies to the whole modulator, built with ideal components, the target design object. At the accumulator output words are coded in 2-complement, they are translated to sign-and-magnitude prior to the digital to analog conversion. The DAC has uniform spaced quantum levels and no overload should occur. So the maximum word length at the output of the accumulator (N_{acc}) determines the number of bits required in the DAC (N_{dac}), they differ only by the leak-bit:

$$N_{dac} = N_{acc} - 1 \quad (\text{both excluding sign-bit}) \quad [1.2]$$

From equation [1.2] the dynamic range of the SADM can be calculated:

$$D = 6(N_{dac} + 1) \quad (\text{dB}) \quad [1.3]$$

When the maximum voltage V_{2op} is known the absolute value of the least significant bit voltage, V_{dac} , can be derived:

$$V_{dac} = V_{2op} / 2^{N_{dac}} \quad [1.4]$$

Because the DAC translates a sign-and-magnitude code the transfer function is simply given by:

$$H_{dac}(z) = V_7(z) / [V_{dac}G_6(z)] = 1 \quad [1.5]$$

Together with the timing demands, equations [1.2] and [1.4], the system demands for the DAC are known, and a suitable converter can be designed. Naturally the error at the DAC output must be as small as possible. Preferable smaller than half the lsb-voltage V_{dac} :

$$V_{7err} = V_7^* - V_7 < 1/2 V_{dac} \quad [1.6]$$

$$\text{with } V_7 = G_6 V_{dac} \quad [1.7]$$

V_7^* = actual converter output (with faults)

There are however certain faults that can be tolerated even when the above error condition is not fulfilled. They are a direct consequence of the delta modulation principle and the notion that the same DAC's are used in modulator and demodulator. This will be discussed in the next chapter.

1.2 MODULATOR PARAMETER CHOICE: SIGNAL-TO-NOISE RATIO

DAC parameters N_{dac} and V_{dac} affect not only the DAC design but play also a important role in several modulator features e.g. signal-to-noise ratio, stability, slope overload and dynamic range. To determine optimal values for these and other modulator parameters only a linear analyses of the modulator will not be sufficient because of the non-linear nature of the ADC. Optimization has to follow also some trial and error method using a simulation program. The linear analysis given below serves as a starting point for these simulations. For this purpose the program TON.SIM was used, see reference [5], a high level circuit simulator. A possible danger of this method is the exclusion of certain parameter values which could simplify or improve the design, but are not tried (or in the wrong combination) in a simulation-run. Also at the start of the SADM project in 1986 the ISDN standards where not certain. This led to an initial delta modulator design with a rather high bit rate (4-bit words at 64 kHz or 256 kbit/sec), and a large accumulator length ($N_{acc}=12$). Resulting in a large N_{dac} and small V_{dac} , making it very hard to fulfil condition [1.6]. As the ISDN project evolved several changes where made to this initial design, part of which is not documented in a report.

In this and the next paragraph a condensed overview is given of previous work, completed with new simulation results, with special emphases on the considerations which effect the DAC parameters.

In previous work by Koenen (Ref.[3]) an optimal first-order loop-filter, with one pole and zero, characterized by parameters 'a' - 'b' - ' K_{LF} ', has been determined. The parameter choice is governed primarily by making the noise transfer minimal while maintaining reasonable stability margins and a signal transfer close to unity in the speech band. Assuming additive quantization noise uncorrelated with the input signal, Koenen showed that noise transfer is minimal for $b=1$. Parameters 'a' and 'K' have a lower and upper limit to maintain stability. Figure 1.1 gives a graphical presentation;

$$\begin{cases} b = 1 \\ 0 < a < 1 \\ 0 < K < 4/(1 + a) \end{cases} \quad [1.8]$$

$$\text{where } K = K_{LF} V_{dac} / V_{adc} \quad [1.9]$$

Koenen chose $a=0.25$ and $K=3$ a point in the left top of the stability region. Because Koenen did not calculate the signal-to-noise ratio, the parameter choice is not so evident. Here an alternative method is used, which approaches the problem the same way as in a paper by Giancarlo and Sodini (Ref. [15]). The noise and signal transfer functions are given by equations [1.10] and [1.11] *).

$$H_{sys}(s) = \frac{V_{Sout}}{V_{in}} = \frac{1 + s\tau\beta}{(1 + s\tau\beta) + \left[\frac{s}{j\omega_s - s} \right] \left[\frac{s}{j\omega_s - s} + s\tau\beta \right] + s^2 T_s \tau / \alpha} \frac{\omega T_s / 2}{\sin(\omega T_s / 2)} \quad [1.10]$$

$$H_N(s) = \frac{V_{Nout}}{e_q} = \frac{1}{\beta + \frac{1}{s\tau}} H_{sys}(s) \quad [1.11]$$

where $\omega_s = 2 \pi f_s$ and $T_s = 1/f_s$

*) Equations [1.10] and [1.11] are obtained using the model of figure 2.4 in part I. Reference [15] provides a detailed calculation.

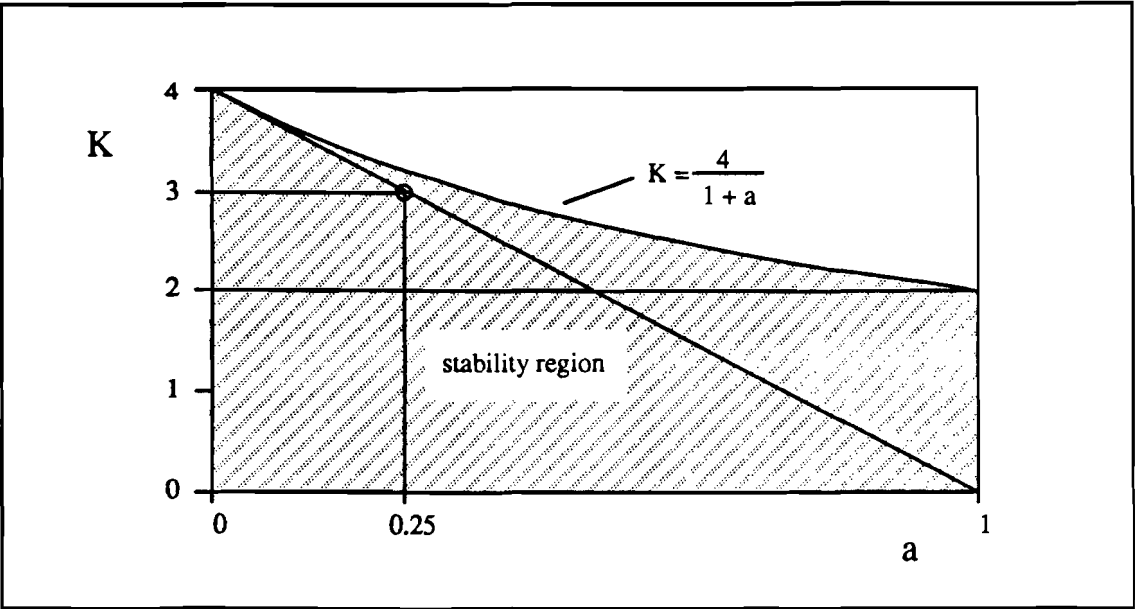


Figure 1.1 Stability region for a and K with $b=1$

The signal transfer is almost unity in the speech band, as can be seen in figure 1.2, where also the transfer is shown when the anti-alias filter is switched in (first-order low-pass with $f_{IF} = 5.7$ kHz).

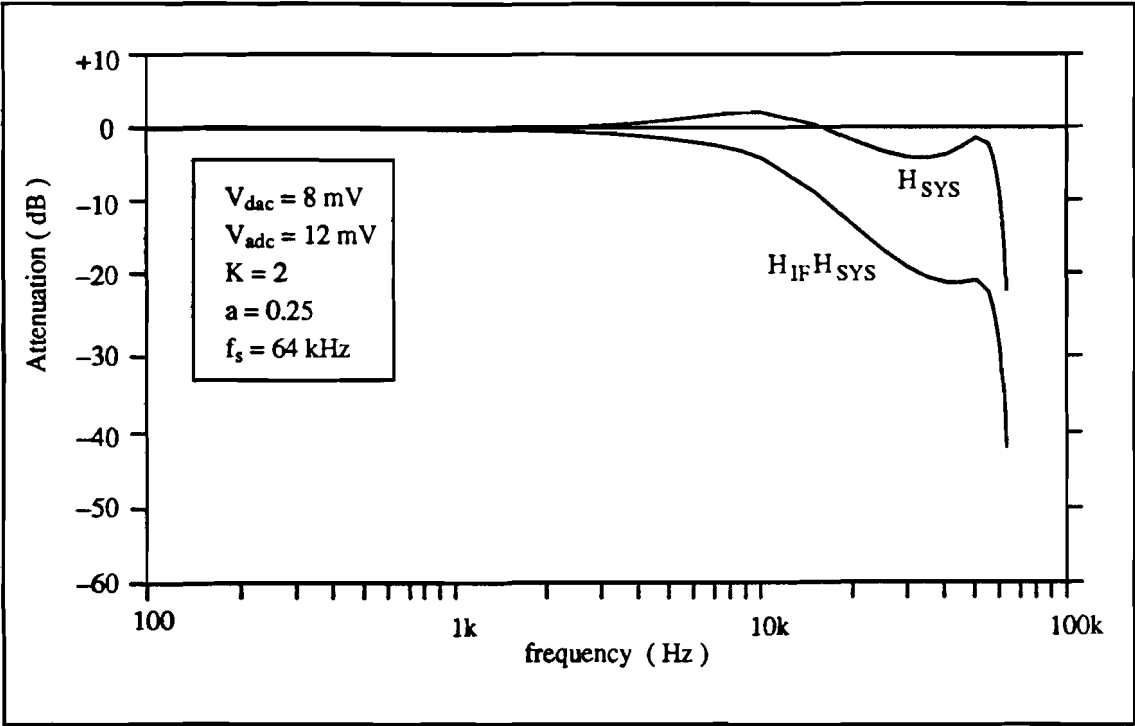


Figure 1.2 System transfer function

In appendix A the low frequency part of figure 1.2 is repeated and compared with CCITT recommendation G.712 for system transfer errors.

Assuming the quantization noise has a white spectrum and looking at inband noise components where the system transfer function is approximately unity, the noise power N_q can be represented as:

$$N_q = \int_0^{f_b} |E_q(f)H_n(f)|^2 df \quad [1.12]$$

For $f \ll f_s$ and defining $E_q(f)$ as $e_0/(f_s)^{1/2}$ yields *)

$$N_q = \frac{1}{3} \left[\frac{2\pi\tau e_0}{f_s} \right]^2 f_b^3 \quad \text{with } \tau = \frac{1}{K_{LF}(1-a)f_s}$$

$$N_q = \frac{1}{3} \left[\frac{2\pi e_0}{K_{LF}(1-a)} \right]^2 \left(\frac{f_b}{f_s} \right)^3 \quad [1.13]$$

Where f_b is the modulator/demodulator band-width, normally set by the corner frequency of the low-pass filter at the demodulator output. Quantity e_0 (the generated quantization noise) is composed of a constant part dependent on the size of the LSB in the encoder (ADC), and a variable part which is dependent on the first derivative of the input signal (its slope). Thus e_0 can be represented by (Ref. [15]):

$$e_0 = [V_{\text{adc}} + 2Af_{\text{IN}}/f_s]/\sqrt{6} \quad [1.14]$$

where A , f_{IN} are respectively amplitude and frequency of the input signal

Combining this result with [1.13], we find that noise power N_q is dependent of both amplitude and frequency of the input signal ($f_{\text{IN}} \ll f_s$):

$$N_q = \frac{1}{18} \left[\frac{2\pi V_{\text{adc}}}{K(1-a)} \right]^2 \left(\frac{f_b}{f_s} \right)^3 \left[1 + \frac{2Af_{\text{IN}}}{V_{\text{adc}}f_s} \right]^2 \quad [1.15]$$

The signal-to-noise ratio is given by:

$$\frac{S}{N} = \frac{A^2/2}{N_q} \quad [1.16]$$

For small amplitude, low frequency signals equation [1.16] may be approximated by:

$$\frac{S}{N} = 9 \left[\frac{K(1-a)A}{2\pi V_{\text{adc}}} \right]^2 \left(\frac{f_s}{f_b} \right)^3 \quad [1.17]$$

Concentrating on the normal operation mode of the SADM (low level), in [1.17] we see the relation with modulator parameters a , K and V_{adc} . For minimal noise and hence for maximal signal-to-noise ratio, K must be as large as possible while ' a ' and V_{adc} must be as small as possible. Recalling the limitations for parameters ' a ' and ' K ' set by the stability criterium (Eq. [1.8]), it is obvious that the choice of Koenen was correct. The signal-to-noise ratio plotted against input amplitude for various frequencies is shown in figure 1.3.

*) The following simplifications are made to calculate N_q : $H_{\text{sys}} \approx 1$ and $\text{invtan}(x) \approx x - x^3/3$ for $|x| \ll 1$

With a , b and K chosen the question remains how to choose V_{dac} . We only know that V_{dac} must be as small as possible, but how small? One methodology of finding the size of V_{dac} is by preventing slope overload. Using equations [1.2], [1.4] and [1.9] will reveal the other properties we want, for instance LSB-voltage V_{adc} for a certain loop-filter gain K_{LF} , and consequently the size of the DAC and accumulator. Preventing slope overload is the subject in the next paragraph.

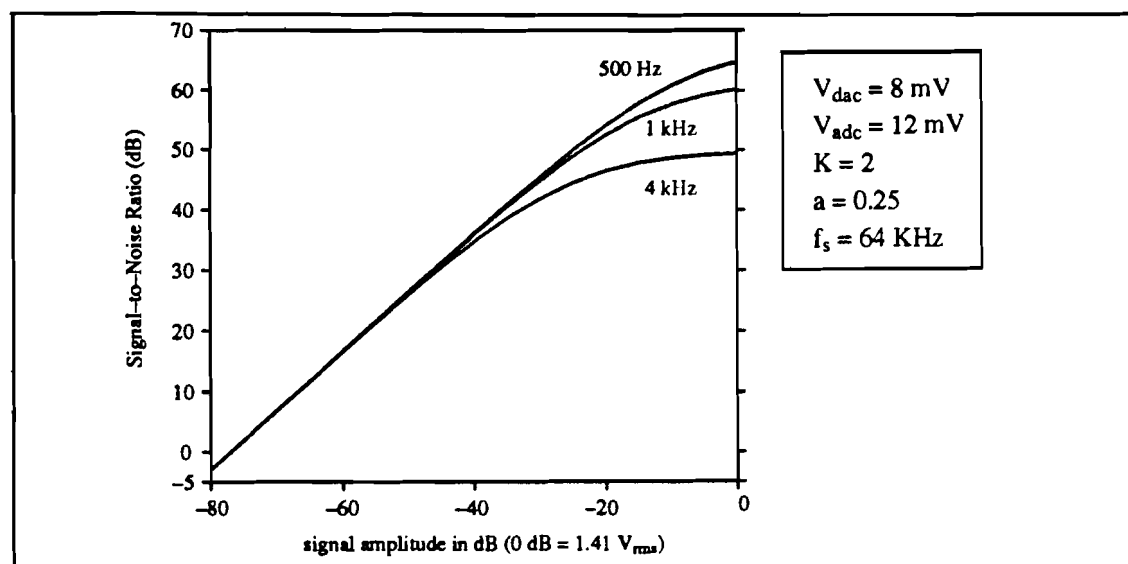


Figure 1.3 Signal-to-noise ratio versus signal input level

1.3 MODULATOR PARAMETER CHOICE: SLOPE OVERLOAD

A disadvantage of delta modulation is the rather high sample frequency, as compared to PCM. Reducing the sample frequency is possible by increasing the number of quantum levels in the ADC, as is done here. Introducing logarithmic spaced quantum levels gives the opportunity to decrease idle channel- and quantization noise for low amplitude low frequency signals, but at the same time prevents slope overload. With the same number of bits (or quantum levels) the first level in the logarithmic ADC can be much smaller, while due to the exponential character still a large dynamic range can be coded correctly, see figure 1.4.

To prevent slope overload a high V_{adc} is necessary, increasing the number of bits in the ADC is a second possibility, but circuit speed limitations bound this to approximately 4 bits (including sign bit) for a sample frequency of 64 kHz. For constant K and K_{LF} the ratio V_{dac}/V_{adc} is fixed, when V_{adc} is increased, V_{dac} must be made larger by the same amount. From paragraph 1.2 we know that this is not wanted because it degrades the signal-to-noise ratio. A compromise between preventing slope overload and maximizing the signal-to-noise ratio has to be found by careful choice of the modulator parameters.

When the properties of the speech input signal are known it is easy to derive a lower limit for V_{dac} preventing slope overload. For a sinusoid with amplitude A and frequency f_{IN} , the maximum difference between two successive samples, V_{3max} , is equal to $2A\sin(\pi f_{IN}/f_s)$. Signal V_3 is next passed through the loop-filter. Voltage V_4 is composed of two terms, a gain factor and secondly an integral part:

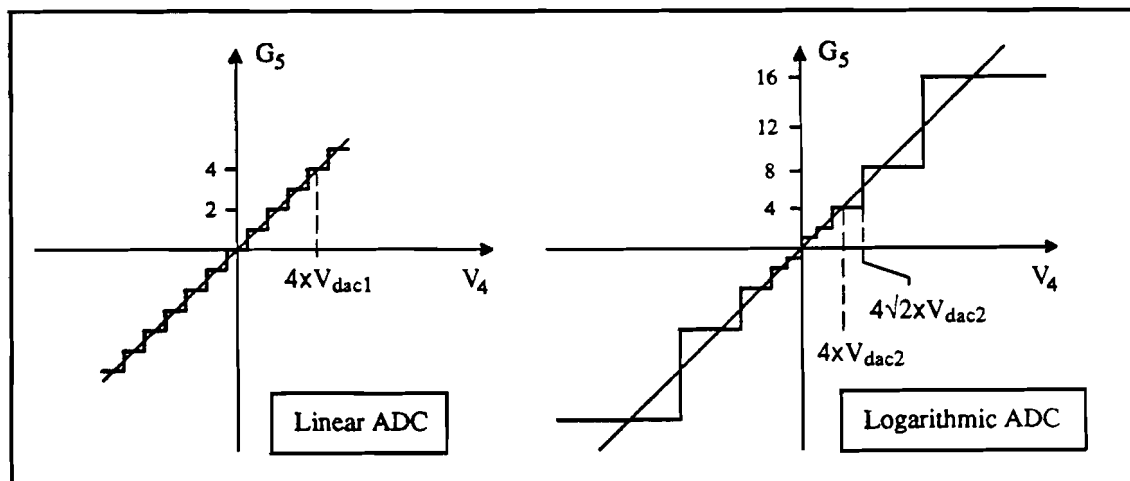


Figure 1.4 Comparing logarithmic and linear multi-bit ADC's

$$V_4(t) = \frac{K_{LF}(1+a)}{2} V_3(t) + \frac{1}{\tau} \int_{-\infty}^t V_3(\tau) d\tau \quad [1.18]$$

$$\text{where } 1/\tau = K_{LF}(1-a)f_s$$

The integral reflects the accumulated weighted sum of the error $V_2 - V_1$ of all past time. For a fast step response the integral part should be small, so τ must be large. Consequently K_{LF} must be small and 'a' should be large (remember $0 < a < 1$), for 'a' precisely the opposite of what was wanted for maximum signal-to-noise ratio. The noise power N_q is proportional to $1/(1-a)^2$. Enlarging 'a' to for instance 0.75, in order to increase the step response speed, results in an 9.5 dB lower S/N-ratio. As can be seen in appendix A, CCITT recommendation G.712 is then violated. The choice $a=0.25$ is maintained. Noting that $V_4 = V_3 K_{LF}(1+a)/2$ if we assume negligible errors in V_1 , the no-slope overload condition can be derived as follows (see also fig 1.4);

maximum input voltage the ADC can encode \geq maximum voltage at ADC input

$$2^N V_{adc} \sqrt{2} \geq \frac{K_{LF}(1+a)}{2} 2A \sin(\pi f_{IN}/f_s) \approx K_{LF}(1+a) A \pi f_{IN}/f_s$$

$$V_{adc} \geq \frac{K_{LF}(1+a) A \pi f_{IN}}{2^N f_s \sqrt{2}} \quad [1.20]$$

$$N = \text{number of logarithmical spaced reference levels in the ADC} = 2^{N_{adc}} - 1$$

As the sinusoid is first passed through the anti-alias input filter, amplitude A decreases at higher frequencies; $A = A(f) = A_0 |1/(1+jf/f_{IF})|$. The product ' $A \cdot f_{IN}$ ' in equation [1.20] has thus maximum value $A_0 f_{IF}/\sqrt{2}$ at frequency $f_{IN} = f_{IF}$, and equation [1.20] changes to

$$V_{adc} \geq \frac{K_{LF}(1+a) A_0 \pi f_{IF}}{2^{N+1} f_s} \quad [1.21]$$

Taking typical values; $A_0=2$, $K=3$, $a=0.25$, $N=7$, $f_{IF}=5.7\text{kHz}$ and $f_s=64\text{kHz}$, lsb-voltage V_{adc} must be greater than or equal to 8.2 mV. The same lower limit applies for V_{dac} if $K=K_{LF}$ as can be seen when $K_{LF}=KV_{adc}/V_{dac}$ is substituted in equation [1.21]. What is left now is a choice for loop-filter gain K_{LF} and LSB-voltage V_{adc} , under the restriction that

the ratio K_{LF}/V_{adc} is the same as the ratio K/V_{dac} . An upper limit for V_{adc} can be derived from the observation that the loop-filter makes use of a operational amplifier with maximum output voltage swing ± 2 Volt, hence;

$$2^N V_{adc} \sqrt{2} \leq 2 \text{ Volt}$$

$$V_{adc} \leq 11 \text{ mVolt for } N=7$$

Additional upper bounds for V_{dac} and the ratio V_{adc}/V_{dac} follow from a minimum required dynamic range, and a minimum required signal-to-noise ratio. For $D \geq 48$ dB, and using equations [1.3] and [1.4] yields;

$$\begin{aligned} N_{dac} &\geq 7 \\ V_{dac} &\leq 15.6 \text{ mVolt } (|V_{2top}| = 2 \text{ Volt}) \end{aligned}$$

From appendix A, where lower limits for S/N-ratio versus signal input level are given according to CCITT recommendation G.712, and choosing $S/N \geq 40$ dB ($f_N=4$ kHz, $A_0=2$ Volt), yields when [1.15] and [1.16] are applied;

$$\frac{V_{dac}}{V_{adc}} \leq 0.92K \quad \text{substituting } K = K_{LF} \frac{V_{dac}}{V_{adc}} \quad \text{yields } K_{LF} \geq 1.09$$

We have obtained the following set of parameters and restrictions

a) $b = 1$	minimum noise transfer
b) $a = 0.25$	maximal S/N ratio
c) $K 2.73 \times 10^{-3} \leq V_{dac} \leq 15.6 \times 10^{-3}$ $K_{LF} 2.73 \times 10^{-3} \leq V_{adc} \leq 15.6 \times 10^{-3} K_{LF}/K$	no slope overload, lower limit dynamic range
d) $N_{dac} \geq 7$	lower limit dynamic range
e) $V_{adc} \leq 11 \text{ mV}$ $V_{dac} \leq (K/K_{LF}) \times 11 \text{ mV}$	maximum voltage swing
f) $K_{LF} \geq 1.09$	lower limit S/N ratio
g) K_{LF} small	fast step response
h) V_{dac} small	maximal S/N ratio
i) K large	maximal S/N ratio
j) $0 < K < 3.2$	stability for $b=1$ and $a=0.25$
k) $K/V_{dac} = K_{LF}/V_{adc}$	by definition

To optimize the tradeoff between maximum S/N ratio, preventing slope overload and fast step response, simulation of the SADM is necessary.

1.4 MODULATOR PARAMETER CHOICE: SIMULATION

Because the analog to digital converter has logarithmic spaced reference levels, the quantization noise is correlated with the input signal. High amplitude, high frequency signals cause larger quantization noise, while slope overload is also a possible danger with such signals. The results of the previous paragraphs only apply if the quantization noise can be separated from the signal. In general this will not be possible and some precaution is appropriate when interpreting these results. Furthermore the assumption of negligible errors in the predicted value V , was made. To analyze the modulator more thoroughly, computer simulations are needed.

Simulations of the modulator with the program TON.SIM where first performed by Vercoulen, see Ref. [2]. Here instead of a lower limit for V_{adc} , the size of the accumulator N_{acc} was determined. From his report it is not quite clear what has been

done. Probably he took fixed values for K and V_{adc} ($K=3$, $V_{\text{adc}}=33$ mV as mentioned on pages 13 and 6 in his report). So lsb-voltage V_{adc} and K_{LF} are variable, but their product must be equal to KV_{adc} . The size of the accumulator follows from equations [1.2] and [1.4]. A typical voice signal, corresponding with a Dutch pronounced letter 'a', was taken as input signal, with the maximum amplitude set to 2 Volt. By repeated simulations and visually inspecting the voltages $V_1(t)$ and $V_2(t)$ for differences, a lower limit for V_{adc} was found; $V_{\text{adc}}=2$ mV. Vercoulen chose this rather low value as the basis for the accumulator design. With $V_{\text{adc}}=2$ mV the total accumulator length is 12 bit; 10 for coding magnitude, 1 for the sign and 1 leak bit, so using equation [1.2], $N_{\text{adc}}=10$. The accumulated error for any input word caused by imperfections in the DAC design must thus be smaller than $2V/(2^{N_{\text{adc}}+1}-1)=0.5$ mV, 0.025% of full scale output, the dynamic range is 66 dB. While a large dynamic range is a nice feature, the accuracy demands placed on the DAC are very hard to fulfill.

The above outcome is rather strange because such a low V_{adc} would mean that K_{LF} is quite large ($K_{\text{LF}}=333\text{mV}/2\text{mV}=166.5$). Using equation [1.21] the no slope overload condition now prescribes $V_{\text{adc}} \geq 135\text{mV}$, a factor 4 larger than the actual value. Slope overload will occur but the choice of input signal and evaluation method makes this hard to detect. The input signal contains only one high amplitude peak of short duration, causing slope overload. But as the rest of the input signal is of relative low amplitude during a long period, there is enough time for the loop to correct this. In general voice signals are characterized by large crest factors (the ratio of peak amplitude to rms value). So occasional high peaks do not much harm. Nevertheless using only one typical voice signal is dangerous, it would have been better to use several different input signals and to evaluate the difference $V_2(t)-V_1(t)$.

Leenhoven (Ref. [9]) performed more elaborated simulations using TON.SIM. In a memo, date 15 feb 1989, Leenhoven gives an overview of his conclusions. Here the voice signal was modeled by a white noise signal passed through two first-order low-pass filters with corner frequencies 800 and 4000Hz. Using two modulator descriptions, one with a quantizer the other without, the quantization noise (and distortion) was separated from the signal. By performing a fast fourier transform on these signals, signal-to-noise versus frequency curves were calculated. His conclusions harmonize more with the results of the previous paragraphs. The final parameter choice (see the list at the bottom of this page) is in close agreement with points a) to k) in paragraph 1.3. Also shown by Leenhoven is that the step response is faster for lower K_{LF} , and least significant bit voltage V_{adc} can be much larger ($V_{\text{adc}}=8\text{mV}$ as compared to 2mV) without any significant reduction in signal-to-noise ratio. This is probably due to the simulation method, which doesn't differentiate between noise and distortion. Low noise and high distortion (slope overload) are present for $V_{\text{adc}}=2\text{mV}$. The situation is reversed for $V_{\text{adc}}=8\text{mV}$, higher noise but lower distortion. With $V_{\text{adc}}=8\text{mV}$ the accumulator and digital-to-analog converter length can be made smaller ($N_{\text{acc}}=9$, $N_{\text{dac}}=8$). Simplified and less demanding circuits are positive outcomes off his research. For instance with $V_{\text{adc}}=8\text{mV}$ the upper limit for DAC errors reduces from 0.025% to 0.78% of full scale output, while the dynamic range of 54 dB still is adequate.

To conclude this chapter the latest set of parameters, as derived by Leenhoven, is given.

```

a = 0.25      b = 1      KLF = 3      K = 2
Vadc = 12mV   Nadc = 3
Nacc = 9      Ndac = 8      Vdac = 8mV
(Nadc, Nacc and Ndac all excluding sign-bit)
|Vin|max = 2V (1.41 Vrms)
D = 54 dB

```

CHAPTER 2 DIGITAL TO ANALOG CONVERTER DESIGN

2.1 GENERAL CONSIDERATIONS

There are many ways to design an integrated digital to analog converter, based on various principles and using different fabrications techniques. The contents of this chapter will focus on DAC networks that could be realized using the EFFIC NMOS fabrication proces. Simple circuit layout and easily achievable elements are additional design objects.

Using the EFFIC NMOS technology places certain constraints upon the design, most notable are consequences of the relative large minimal surface dimension ($6\text{ }\mu\text{m}$). This will have serious effects on circuit speed. Since the MOS transistor is a field-effect device (majority carriers only), the switching speed of MOS circuits is limited only by the time required to charge and discharge the capacitances between device electrodes and from interconnecting lines. While the current through a NMOS transistor is proportional to the ratio of width and length of the gate area, stray capacitances associated with that transistor are in first order proportional to the product of width and length. Hence for equal size reduction in W and L the current remains the same, while capacitances are reduced, the time to charge them will now be shorter. So a significant feature of MOS circuits, the sharp improvement in circuit speed by reduction in the internal dimensions of individual devices, can only be used to an certain extend. Knowing the required conversion time ($3\text{ }\mu\text{sec}$), the in general slower serial converter types are less suited to fit the speed requirements than parallel converter types. With a parallel accumulator an extra conversion stage would also be necessary.

NMOS fabrication process disadvantages are the difficult to obtain accurate resistors- and capacitors values, which are of prime importance in most parallel DAC designs. Also the "on-resistance" of a MOS transistor, which is very dependent on device parameters (V_{th} , C_{ox}) and voltages, thus very inaccurate and hard to control, cant be neglected in circuits using resistors. High resistor values are a possible solution, but they normally occupy far to much chip area. This excludes most of the widely used weighted-resistor converter types. An additional problem in circuits based on capacitor networks are the large and mostly voltage dependent stray capacitances.

Weighted current converter types, constructed with active current source arrays, are not regarded. This is not done because the converter accuracy depends to much on the actual fabrication proces. Photo-mask misalignment, control of threshold voltages and other transistor parameters, temperature dependence, make the design of a accurate DAC very difficult. There are easier and far more reliable ways to design a digital-to-analog converter.

A way to avoid the heavy dependence on component accuracy is transforming the multi-bit input into a lower number of bits. By reducing the number of bits from 8 to for instance 4, the accuracy requirements reduce with a factor $2^8/2^4=16$. To maintain the same performance these methods depend on gross oversampling and noise shaping to redistributed quantization noise over a wider bandwidth and to move it out of the speech band. The speed limitation due to the $6\text{ }\mu\text{m}$ NMOS proces prohibits the use of these techniques. Extra stages prior to the actual DA-conversion are also needed to perform the oversampling and noise shaping.

There are however also certain advantages when using capacitor networks e.g. accurate capacitor ratios are easy to obtain on the same chip (resistor ratios to a lesser degree). This results from the fact that capacitors can be made square while resistors in general have a very large length to width ratio. Small random edge uncertainties have a much

larger impact on resistor accuracy. Also MOS transistors are very well suited as charge switches because of their high input resistance and resulting extremely low leak-current. Furthermore they have no voltage offset in this application.

To summarize the DAC design is biased towards a solution with a parallel converter type using some kind of binary weighted capacitor network, where the accuracy depends on capacitor ratios and not on absolute values. From a literature study by Geloven, reference [1], it is clear that the above type of DAC is chosen in most cases using NMOS technology.

2.2 CONSIDERATIONS REGARDING DAC ACCURACY

The delta modulator is a system with feedback, offset errors in the loop-filter will be compensated by the loop. Offset errors in the input-filter can be regarded as part of the input signal. Here small errors should not present a problem, only the dynamic range decreases somewhat. As the ADC has an internal offset compensation circuit and the ACCU operates digitally, these two modules have no offset error. Offset voltages in the DAC are treated differently. Not the actual value is important, rather the combination of offset voltage and other DAC errors sources should be small (see next page). If the offset voltage in the loop-filter, input-filter or DAC is too large and the input signal contains high amplitude high frequency components (large rate of change) it is possible that some device in the modulator saturates. Furthermore the dynamic range is compressed by large offset voltages. Small offset voltages can however be tolerated and are not regarded as error sources.

The ISDN chip is intended for coding/decoding speech signals, where the same type of DAC is applied in coder and decoder. The SADM transfer from modulator input to demodulator output is proportional to $V_{dac, demod}/V_{dac, mod}$. CCITT ISDN recommendation G.712 prescribes a total system gain error smaller then ± 0.5 dB (appendix A). This is very important for the DAC design, as now only gain ratio errors are meaningful. So the actual gain (or V_{dac} value) error in one converter is no longer important, rather the ratio $V_{dac, demod}/V_{dac, mod}$ must be within certain limits. Identifying four gain error sources in the system transfer function;

$$H_{sys} \approx K_{IF} K_{OF} V_{dac, demod} / V_{dac, mod} \quad (f < 4 \text{ kHz}) \quad [2.1]$$

where K_{IF} = gain input anti-alias filter (coder)
 K_{OF} = gain output filter (decoder)

and assuming equal errors, the absolute error ϵ in the ratio $V_{dac, demod}/V_{dac, mod}$ must be smaller then $\pm 0.5/3 = \pm 0.17$ dB. Consider for example $\epsilon=0.01$ (0.1 dB), a value satisfying the ± 0.17 dB constraint. This ϵ is equivalent with 2.5 LSB in an 8-bit converter, for a stand-alone 8-bit DAC unacceptable. Seen as part of the whole modulation-demodulation system it is however of no significance.

Gain errors in the DAC cause a deviation in the target value of V_{dac} . They can be accounted for (together with errors in loop-filter gain K_{LF} and LSB-voltage V_{lsb}) by a uncertainty in loop-gain K . The loop is stable for K values in the range [0 to 3.2]. So for target value $K=2$, V_{dac} can vary widely without causing any problems, and we can delete the difference between the target and absolute value of V_{dac} as an error source. To eliminate this error source (gain) from condition [1.7], the DAC transfer is modeled by a first order approximation of the transfer function:

$$V_7 = V_{dac} G_s(i) + V_{odac} \quad [2.2]$$

Condition [1.6] can now be restated, it does no longer contain gain errors:

$$\frac{V_7^*}{V_{dac}} < 1/2 \quad [2.3]$$

Inequality [2.3] must hold for all input words $G_6(i)$, where i ranges from -255 to 255 for an 8-bit DAC.

V_{dac} and V_{odac} are determined by minimizing the error function E (linear regression method):

$$E = \sum_{i=-255}^{255} [V_7^*(i) - (G_6(i)V_{dac} + V_{odac})]^2 \quad [2.4]$$

Voltages $V_7^*(i)$ are obtained from measurements or from a SPICE simulation of the DAC. Solving the two equations $\partial E / \partial V_{dac} = 0$ and $\partial E / \partial V_{odac} = 0$ leads to:

$$V_{dac} = \frac{\sum G_6(i) \sum V_7^*(i) - N \sum G_6(i) V_7^*(i)}{[\sum G_6(i)]^2 - N \sum G_6^2(i)} \quad [2.5]$$

$$V_{odac} = \frac{\sum V_7^*(i) - V_{dac} \sum G_6(i)}{N} \quad [2.6]$$

where $\sum = \sum_{i=-255}^{255}$

$$N = 255 + 255 + 1 = 511$$

2.3 WEIGHTED-CAPACITOR PARALLEL CONVERTERS

The basic parts of a parallel DAC are shown in figure 2.1, there are four major parts: 1. analog reference supply, 2. logic circuitry, 3. analog switches and 4. weighing network.

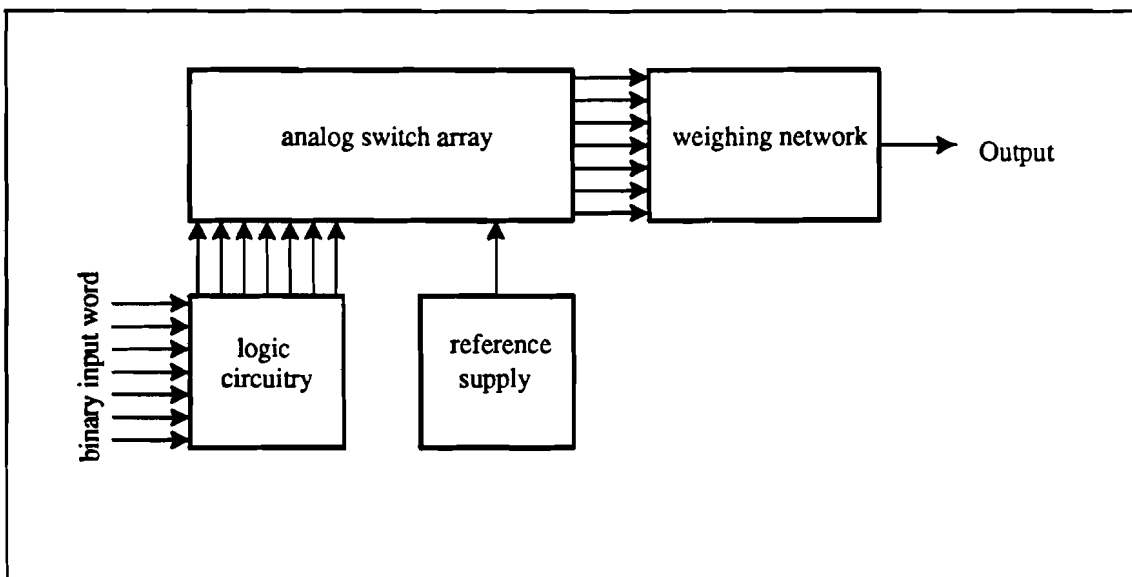


Figure 2.1 Block diagram parallel DAC

The purpose of the reference supply is to provide a standard for the analog magnitude of the binary input code. The logic circuitry performs a holding function for, and possible translation of, the binary input code. Also it activates the corresponding analog switches which connect the reference supply or ground to the proper terminal of the weighing network depending on the state of an input bit. The weighing network divides the reference supply down so that a voltage (or current) is added to the DAC output whose magnitude is proportional to the equivalent weight of that particular bit.

When scaling a weighing network, in general knowledge is needed of the magnitude of parasitic capacitors, for instance given as a percentage of a network capacitor value (Ref. [14]). This percentage often is uncertain and will vary from chip to chip. To avoid problems with stray capacitances from network capacitors and MOS switches it is better to choose a converter with a common summing point. DAC's using the capacitor equivalent of R-2R ladder type converters (which occupy minimal chip area) are therefor not discussed.

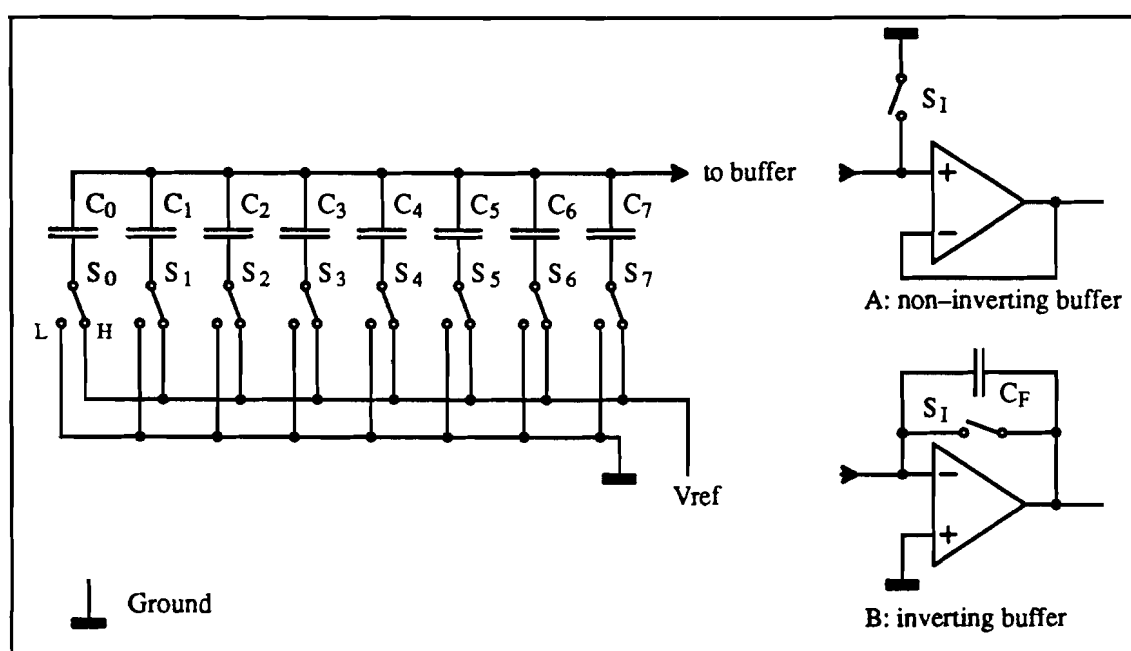


Figure 2.2 Basic circuit layouts; inverting and non-inverting

Figure 2.2 shows the basic circuit configurations for an 8 bit parallel $C-2^N$ DAC, an important feature is the common summing point. Every bit of the input word b is assigned to a switch; LSB b_0 to switch S_0 MSB b_7 to switch S_7 . The correct division of the reference voltage is done by making all capacitors C_i twice as large as C_{i-1} . To maintain the same output voltage for equal input words, capacitor C_F in figure 2.2B must be twice as large as C_7 . The conversion takes place in two phases, for simplicity a sign and magnitude input code and ideal circuit elements are assumed. For positive respectively negative input codes the switching order is slightly different:

Positive input code

- In the first phase all switches are in position L, switch S_1 is closed, resetting all capacitor voltages. In the second phase switch S_0 to S_7 connect capacitor C_0 to C_7 to V_{ref} (position H) if the corresponding bit value is '1', they stay in position L for bit value '0', switch S_1 is open.

- Negative input code
- In the first phase capacitor C_0 to C_7 are connected to V_{ref} if the corresponding bit value is '1', switch S_i is closed. In the second phase S_i is open and S_0 to S_7 switch from position H to L if the bit value is '1', for bit value '0' they stay in position L.

Disregarding delay and polarity the output voltage from the two circuits is given by:

$$V_{out} = V_{ref} \frac{\sum_{i=0}^7 b_i C_i}{\sum_{i=0}^7 C_i} \quad [2.7]$$

Equation [2.7] presents the basic property of the circuits; accuracy depends not on absolute capacitor values but on proper capacitor ratios.

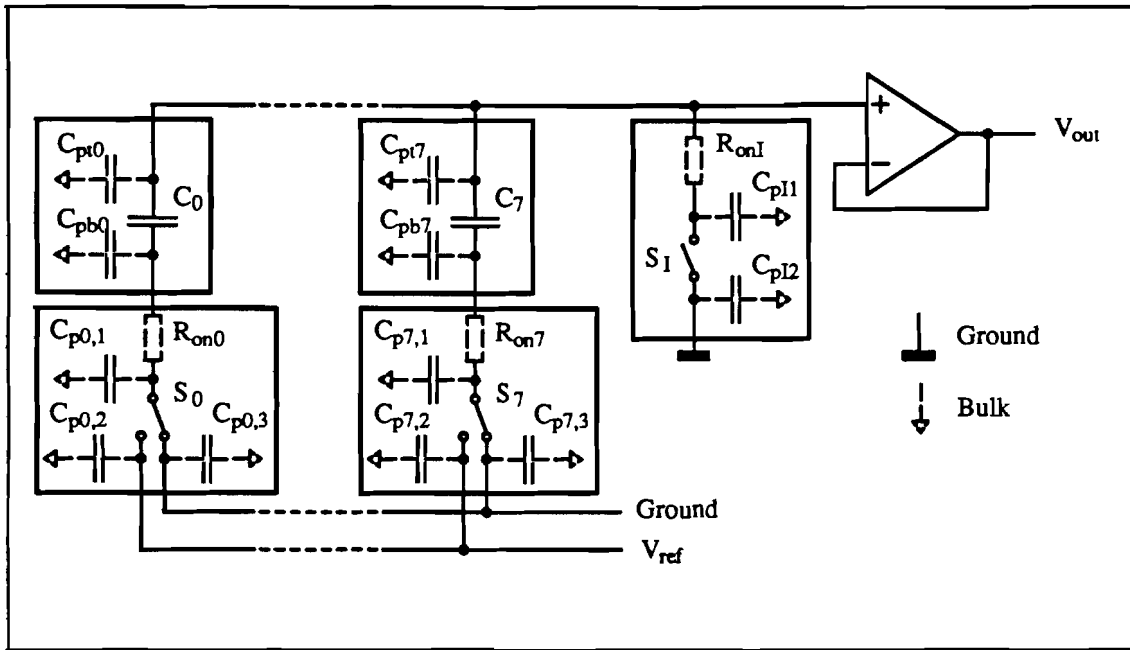


Figure 2.3 Parasitic capacitances capacitors/switches

To determine the effect of parasitic capacitances and non-ideal switches, consider the converter with errors as shown in figure 2.3. For this circuit the steady state output voltage is given by;

$$V_{out} = V_{ref} \frac{\sum_{i=0}^7 b_i C_i}{\sum_{i=0}^7 C_i + \sum_{i=0}^7 C_{pi} + C_{pi1}} \quad [2.8]$$

Parasitic capacitances from switches S_0 to S_7 have no effect on steady state DAC performance, while parasitic capacitors at the common summing point will only lead to gain errors in case of the non-inverting DAC. With the inverting buffer these parasitics are eliminated altogether because they are connected between virtual ground and bulk. These nice features are a direct effect of the common summing point in both converters, and is one of the main reasons why this converter type was chosen. Other

reasons are the simple circuit arrangement and that accuracy relies on ratio exactness.

2.4 CONVERSION SPEED ESTIMATION

With an ideal operational amplifier, on-resistance R_{ON} or more correctly the current limitations of MOS switches, restricts the conversion speed. To estimate the conversion speed, given by transit time τ , consider the circuit in figure 2.4. Switch S_i is constructed with two enhancement transistors T_{E1} and T_{E2} , connecting ground or V_{ref} to C_i according to the value of b_i .

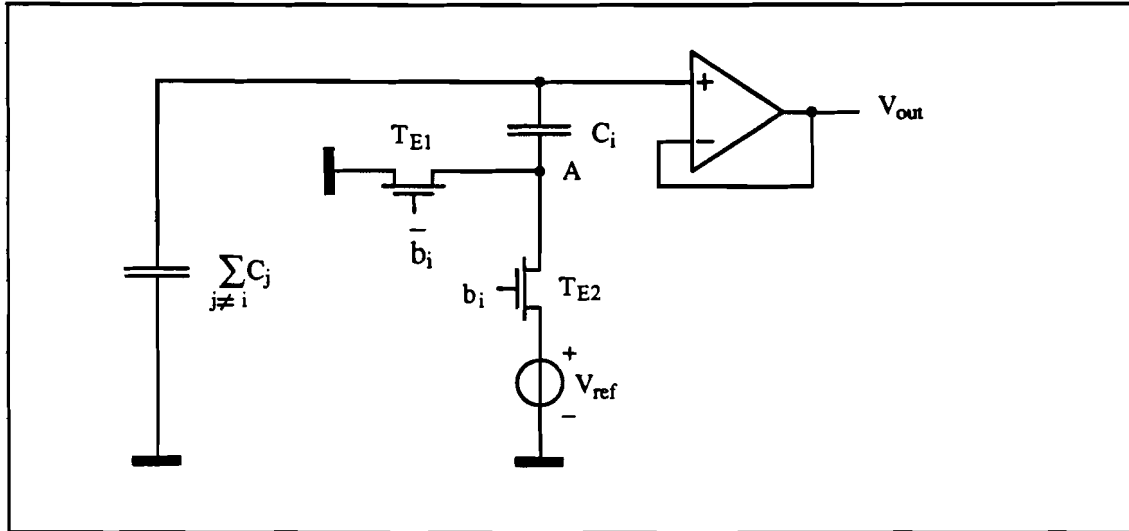


Figure 2.4 Simplified load circuit

Next assume a positive input word with only bit b_i high. So at the start of the second phase of the conversion, the voltage across all network capacitors is zero. The conversion ends after $1.5\mu\text{sec}$. The transit time must be smaller then this time value. Taking typical values for logic high- and low-levels ($\pm 5\text{ V}$), $V_{ref}=2\text{ V}$ and $V_{TE}=0.55\text{ V}$, transistor T_{E2} works in its linear region during the whole conversion. An coarse estimate of the conversion time can be obtained as follows; the approximate average capacitor charging current I_{mean} is found by averaging the load current at $V_A=0$ ($t=t_0$) and at $V_A=V_{ref}/2$ ($t=t_1$), Ref. [19]:

$$I_{mean} = \frac{(w/L)kV_{ds}(t_0)[2V_{gs}(t_0)-2V_{TE}-V_{ds}(t_0)] + (w/L)kV_{ds}(t_1)[2V_{gs}(t_1)-2V_{TE}-V_{ds}(t_1)]}{2}$$

$$= 9.85(w/L)k \quad [2.9]$$

$$\text{where } k = \frac{\mu_n \epsilon_{ox}}{2t_{ox}}$$

The equivalent capacitance from point A to ground is maximal when $C_F=C_7$, leading to a maximal transit time:

$$C_E = \frac{C_7 \sum_{i \neq 7} C_i}{C_7 + \sum_{i \neq 7} C_i} \approx 64C \quad [2.10]$$

The estimated transit time τ is equal to the change in charge divided by the mean load current:

$$\tau = \frac{\Delta Q}{I_{\text{mean}}} = \frac{C_E V_{ref}/2}{I_{\text{mean}}} = \frac{6.5C}{(W/L) k} \quad [2.11]$$

As an example take $C=1\text{pF}$, $W/L=1$ and $k=15\mu\text{A}/\text{V}^2$ giving a transit time of $0.43 \mu\text{sec}$. When compared to the allowed conversion time ($3 \mu\text{sec}$) or $1.5 \mu\text{sec}$ per phase, this is sufficient. But regarding the made simplifications, a still lower value would be preferable. A easy solution is increasing the ratio W/L , which is only necessary for switch S_7 and maybe for switch S_6 .

2.5 REDUCED AREA WEIGHTED-CAPACITOR CONVERTERS

An obvious disadvantage of the two converters in figure 2.2 is the large total capacitance. Note that the total capacitance for converter B in figure 2.2 is twice as large as for converter A, which still requires 255 capacitor units. A reasonable accurate NMOS unit-capacitor of 1 pF has dimensions $40\mu\text{m} \times 40\mu\text{m}$, the capacitor network would then minimal occupy $408000 \mu\text{m}^2$ (approx. 0.4 mm^2) chip area. This is far too large for both converters, and therefor not acceptable. By leaving the feature of one common summing point, it is possible to achieve a considerable size reduction. A second benefit is that now minimal area transistors can be used as switches. If the size reduction is relatively large a sharp improvement in conversion speed can also be expected. The new circuit still benefits from a common summing point however in a somewhat altered form. It will be shown later that capacitor ratio errors limit the achievable size reduction.

In figures 2.5 and 2.6 multi-stage converters are illustrated, demonstrating the use of coupling capacitors to reduce size. The common summing point is split in two or three parts, dividing the network in two or three stages, starting with stage 1 at the LSB-side. The values of these coupling capacitors are chosen such that the division of V_{ref} is correctly continued into the next higher stage. Each stage can be regarded as having its own common summing point. Stray capacitances connected at each stage summing point have no influence on the correct division for that particular stage. However they do affect the value of the coupling capacitor to the next higher stage. Now precise knowledge is needed of their size to calculate the coupling capacitance. Size reduction originates from choosing a small capacitance value ($1 \times$ the value of C_0 in figure 2.2) for the less significant capacitors in each stage. Capacitors connected to the same stage are, as before, related in value by $C_i = 2C_{i-1}$.

To give a mathematical background to the above observations, the general transfer function of 2- and 3-stage converters is calculated. Furthermore formulas are given to calculate the coupling- and parasitic capacitances. The parasitics at each stage summing point are summed together to form the stage parasitics C_{p1} , C_{p2} and C_{p3} . The size of a parasitic capacitor is related to the originating capacitor value with factors ϵ_1 and ϵ_2 : $C_{p1} = \epsilon_1 C$, $C_{p2} = \epsilon_2 C$. Two factors ϵ are taken to model differences in the two capacitor plates.

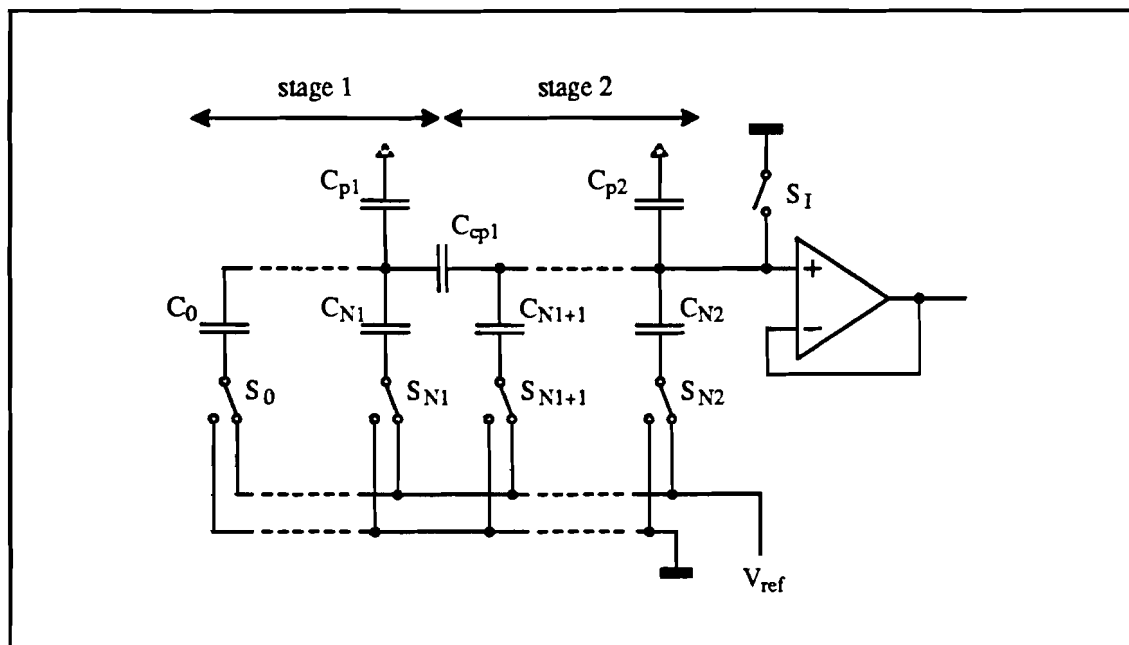


Figure 2.5 2-stage digital-to-analog converter

2-STAGE DAC

$$\text{transfer } V_{\text{out}} = V_{\text{ref}} \frac{\left[\sum_{\text{stage 2}} b_i C_i + \frac{C_{\text{cp1}}}{C_{v1}} \sum_{\text{stage 1}} b_i C_i \right]}{C_{v2} - C_{\text{cp1}}^2 / C_{v1}} \quad [2.12]$$

$$\text{where } C_{v1} = \sum_{\text{stage 1}} C_i + C_{p1} + C_{\text{cp1}}$$

$$C_{v2} = \sum_{\text{stage 2}} C_i + C_{p2} + C_{\text{cp1}}$$

Capacitor numbering: stage 1; 0 to N1 total N1+1 network capacitors
stage 2; N1+1 to N2 total N2+1-N1 network capacitors

Parasitic capacitances:

$$C_{p1} = \sum_{\text{stage 1}} \epsilon_i C_i + \epsilon_b C_{\text{cp1}} \quad [2.13a]$$

$$C_{p2} = \sum_{\text{stage 2}} \epsilon_i C_i + \epsilon_i C_{\text{cp1}} + C_{p1} \quad [2.13b]$$

Coupling capacitor:

$$C_{\text{cp1}} = \frac{\sum_{\text{stage 1}} C_i + C_{p1}}{2 \frac{C_{N1}}{C_{N1+1}} - 1} \quad [2.14]$$

$$C_{cp2} = \frac{\sum_{\text{stage } 2} C_i + C_{p2} + C_{cp1}[1 - C_{cp1}/C_{v1}]}{2 \frac{C_{N2}}{C_{N2+1}} - 1} \quad [2.17b]$$

Equations [2.12] to [2.17] explicitly show the influence of stray capacitances on the transfer functions and size of the coupling capacitors. Not their actual size is important (this can be accounted for by appropriate scaling of the coupling capacitors), but the uncertainty in their size. Equations [2.12] and [2.15] also display a way to reduce these unwanted errors. The trivial solution is to use network capacitors with minimal parasitics, this of course within the limitations set by the EFFIC NMOS fabrication proces. A second possibility is by means of different network topologies. Stray capacitances only appear as a possible error source in the multiplication factors prior to the summation $\sum b_i C_i$, for all stages except the last. By increasing the number of network capacitors connected to the last stage, the error is shifted towards less significant bits, relative to the MSB the error is thus reduced. The catch of this method is that the total capacitance increases. Note that when the method is applied to the extreme a 1-stage DAC, as in figure 2.2, is the result.

So a size reduction is possible but at the cost of a less accurate DAC. The trade-off between accuracy and size is the topic of the next chapter.

CHAPTER 3 ERROR LOCATION AND REDUCTION

3.1 NMOS CAPACITORS

In an implementation of the converter non-ideal active and passive components deteriorate the system performance from the idealized case. These non-ideal elements include parasitic capacitances, capacitor value errors, offset voltages from clock feed through and buffer, gain errors and reference source mismatch. From these several aren't important such as (small) offset voltages and gain errors as long as they don't differ in coder and decoder. Reference source mismatch, causing also gain errors, only contributes if different reference voltages are present in coder and decoder (for instance caused by temperature differences). As the reference source is an external component it can be selected from a large number of standard IC's for minimum error.

Assuming an ideal buffer it is apparent from the description of the operating principle that what is really important for accurate conversion is not the absolute values of the capacitors, but rather the ratio between them. While the DAC has to be realized in NMOS technology, first an overview is given of some physical aspects of this technology applied to capacitors. In general there are two ways of making capacitors using the EFFIC NMOS fabrication proces; single- and double-poly capacitors. Figure 3.1 presents construction details.

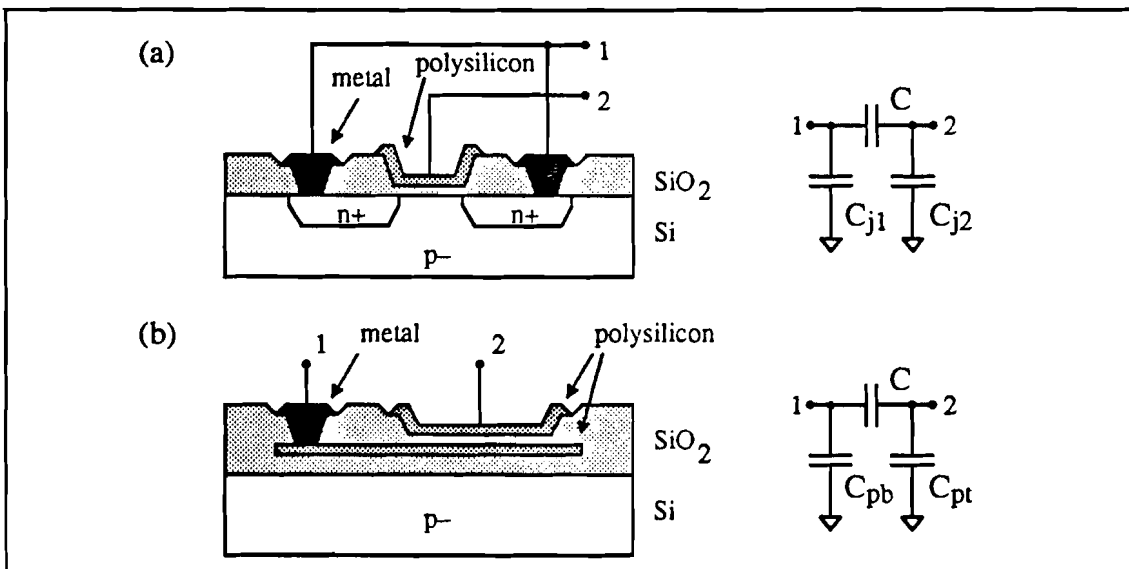


Figure 3.1 NMOS capacitors; (a) Single-poly; (b) double-poly.

The single-poly capacitor is formed from a polysilicon top-plate, the SiO_2 insulation layer and a bottom-plate created by the inversion layer which results when a voltage is applied to the top-plate. In fact this is a normal MOS transistor with the source and drain connected to the same node. The capacitance is voltage dependent, acceptable in some applications, but totally unsuitable as highly accurate capacitor. Capacitor C_j is the non-linear junction capacitance. The double-poly capacitor makes use of two polysilicon layers forming top- and bottom plate, they are separated by a thin SiO_2 layer. A second thicker SiO_2 layer (field oxide) separates the bottom plate from the bulk. Capacitor C (as C_{pt} and C_{pb}) is nearly linear and almost voltage independent. For single-poly capacitors the parasitic capacitance from top plate to bulk, C_{pt} , is about 1/10 of the capacitor value. In the case of the double-poly capacitor, C_{pt} is roughly 1/100 of the capacitor value (dependent on layout), and C_{pb} is about 1/10 of the capacitor value.

3.2 CAPACITOR ERROR SOURCES

Capacitor ratio errors result from several causes, the most important will now be summarized together with, where possible, solutions to circumvent them.

1) Random errors Errors of this source fall into two categories: random variation of the ideally straight edges of the capacitor and secondly a random fluctuation of the thickness and permittivity of the SiO_2 insulator in the capacitor. Measurements by McCreary [Ref. 16] on more than 32,000 capacitor arrays show that the standard deviation, σ_u , in capacitor ratio $\alpha = C_1/C_2$ is very small. The data was obtained from measurements on capacitor arrays constructed from identical unit capacitors with unit plate sizes $25\mu\text{m} \times 25\mu\text{m}$ and $72\mu\text{m} \times 72\mu\text{m}$. This data is used here to derive the expected relative error, $(\Delta C/C)_u$. For the EFFIC NMOS fabrication process no comparable data on capacitor accuracy is available. It is assumed that the capacitor matching properties of the EFFIC NMOS technology are comparable with the capacitor matching properties of the more accurate fabrication technologies tested by McCreary (CCD-1, CMOS-1, CMOS-2 and NMOS-EPM). Denote the standard deviation in the distribution of random errors in unit capacitor C_u , σ_u , as $\text{SD}[C_u]$, and define the expected relative error as:

$$(\Delta C/C)_i = \text{SD}[C_i]/C_i \quad (\text{further referred to as relative error})$$

Then assuming that the random errors are uncorrelated and normally distributed a capacitor made of m unit capacitors has standard deviation $\text{SD}[C_m] = \sqrt{m} \text{SD}[C_u]$, the relative error is thus

$$(\Delta C/C)_m = (1/\sqrt{m})(\Delta C/C)_u \quad [3.1]$$

Using the equations and measurement data given in Ref. [16], we find: $(\Delta C/C)_u = 1.6\%$ (unit capacitors with plate sizes $25\mu\text{m} \times 25\mu\text{m}$, CMOS-1 process).

Increasing the plate size can reduce relative errors, as is shown by Shyu et al. [13]. The relative error $\Delta C/C$ is proportional to $C^{-3/4}$ if only edge effects are present and to $C^{-1/2}$ if the oxide variations represent the dominant effect. Assuming oxide variations dominate (for double poly-capacitors very likely, Ref. [13]), increasing the plate size to $40\mu\text{m} \times 40\mu\text{m}$ results in a decrease of $(\Delta C/C)_u$ from 1.6% to 1.0%. Shyu also shows that for square capacitor plates the error from edge variations is minimal.

2) Etching errors Such as corner rounding and undercut contribute to each capacitor in the same way. Undercut results in a decrease of C , which is proportional to the perimeter of the device. Realization of each capacitor as a parallel combination of some unit capacitance (C_u), as is done in figure 3.2, will minimize errors of this source. For minimum area the smallest network capacitor should be chosen as $1 \times C_u$. Not being able to construct the coupling capacitors as a combination of unit capacitors (values $1.17 \times C_u$ to $2.24 \times C_u$, see paragraph 3.4), geometrical errors will be present in these capacitors.

However if we assume that undercut is the dominate factor (with constant undercut depth Δx along the perimeter, fig 3.3), Gregorian, Ref. [17] shows a method to eliminate undercut as an error source by fixing the length L_1 and width W_1 of a non-unit capacitor C_1 :

$$L_1 = L_u \alpha + (\alpha^2 - \alpha)^{1/2} \quad [3.2]$$

$$W_1 = L_u \alpha - (\alpha^2 - \alpha)^{1/2} \quad [3.3]$$

where $\alpha = C_1/C_u$ ($\alpha > 1$) and $W_u = L_u$

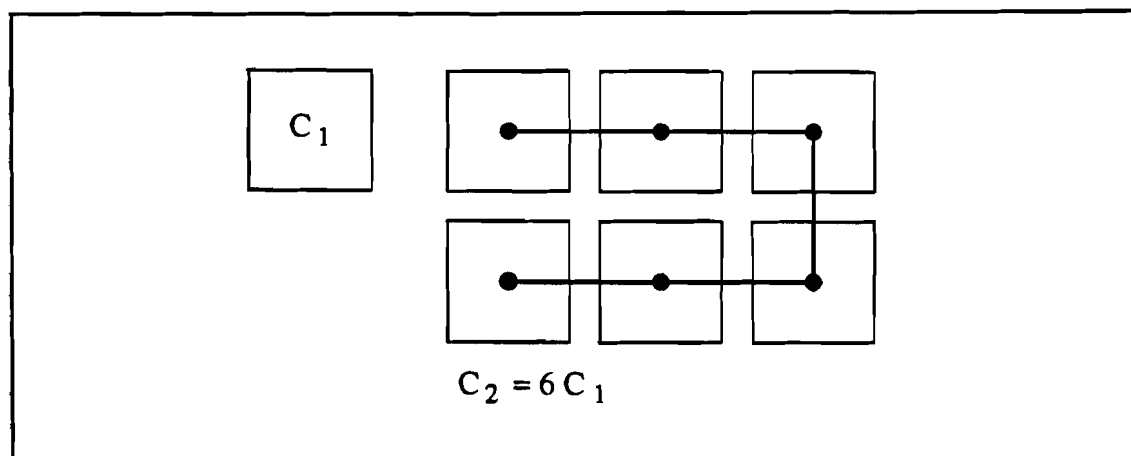


Figure 3.2 Unit capacitor structure

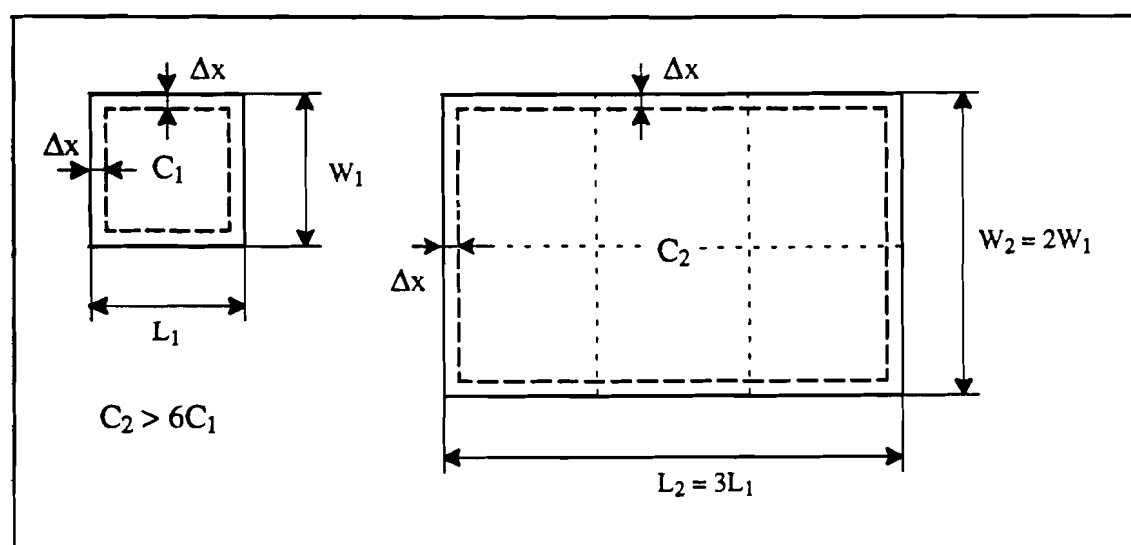


Figure 3.3 Undercut error

3) Photomask misalignment For the EFFIC fabrication process the maximum misalignment between two masks is smaller than $2\ \mu\text{m}$. As there are only two masks involved for a double-poly capacitor, an overlap of $6\ \mu\text{m}$ in all directions in the bottom plate with respect to the top plate, guarantees that the capacitance area is always defined by the top-plate size.

4) Long range gradients in oxide thickness These gradients arise from non-uniform oxide growth conditions. A first order approximation $t_{\text{ox}} = t_{\text{oxn}} + \epsilon x$ is used to model the oxide thickness, ϵ represents the gradient. Experimentally, values of $0.4\text{--}4\ \text{ppm}/\mu\text{m}$ have been observed for ϵ , Ref. [17]. It is apparent that errors of this source are proportional to the dimensions of the capacitor array. These errors can be minimized by a common-centroid geometry. This is done in figure 3.5 by locating the elements of the capacitors in such a way that they are symmetrically spaced about a common center point. For a multi-stage DAC this method can however only be applied to capacitors within the same stage, ratio errors are thus present between stages. For a typical 3-stage DAC the dimensions of the

capacitor array are approximately $300\mu\text{m}\times300\mu\text{m}$ ($40\mu\text{m}\times40\mu\text{m}$ capacitors), so the variation in thickness is 120 to 1200 ppm or 0.012 to 0.12 %. We then can expect the same error in capacitor ratios, since capacitance is proportional to $1/t_{\text{ox}}$ and the direction of the gradient along the capacitor array is not known. Hence a relative error of approximately $1/\sqrt{2}$ this value (0.009 to 0.09%) must be assigned to each capacitor in the array.

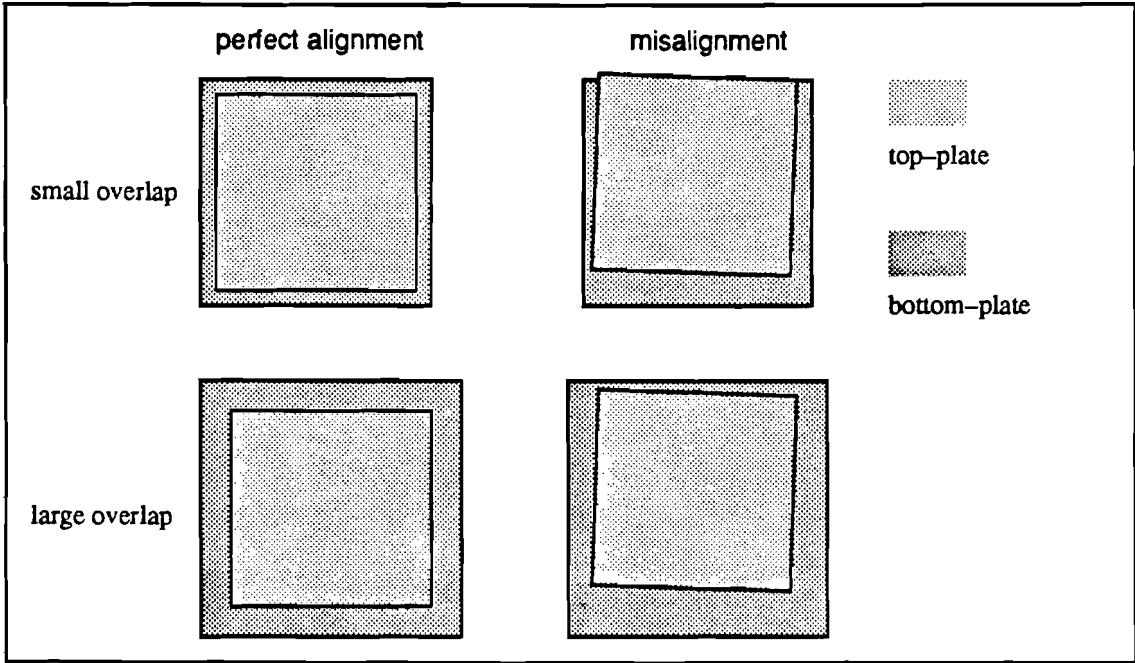


Figure 3.4 Photomask misalignment

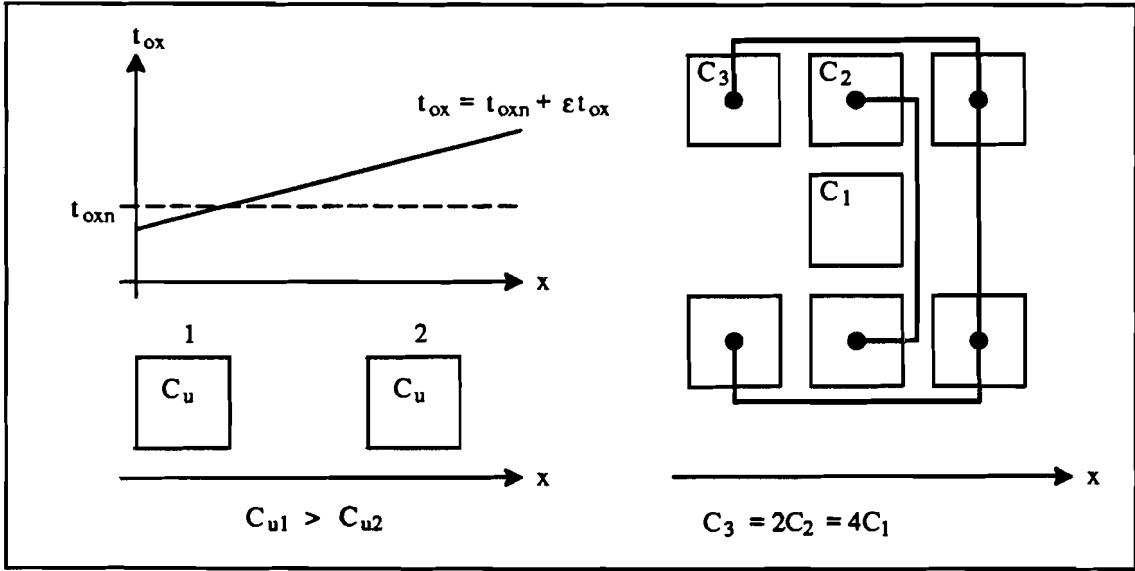


Figure 3.5 Common-centroid geometry

5) Leakage currents

As these are in the order of $16\text{ fA}/\mu\text{m}^2$, a voltage drop of 0.4 mVolt can be expected during one clock period (15 μsec) for $C=1\text{pF}$, compared to V_{ac} a negligible value.

- 6) **Temperature coefficient** The temperature coefficient of MOS capacitors is very small, only about 20 ppm/°C (Ref. [16]), and therefore insignificant.
- 7) **Voltage coefficient** The voltage coefficient is also very small; smaller than 10 ppm/V for double-poly capacitors (Ref. [16]). As the maximum voltage in the capacitor array is equal to V_{ref} (=2 Volt), the error from this cause is negligible.

3.3 RELATIVE CAPACITOR ACCURACY

Having identified the major error sources for MOS capacitors, together with several error reduction schemes, makes it possible to determine the relative capacitor accuracies. To avoid systematic capacitance-ratio errors, employing unit capacitors is a necessity. For a multi-stage DAC a centroid geometry is of limited use. Now only random and oxide gradient errors remain. The relative error in a capacitor constructed from m unit capacitors is then (m not too large) given by equation [3.1]. It should be noted that this error mechanism is due to the inherent random variations of capacitance parameters. Hence, the formulas derived represent an irreducible lower bound on the capacitance error, which cannot be improved by any deterministic a priori techniques. As capacitance unit a double-poly capacitor with top-plate size $40\mu\text{m} \times 40\mu\text{m}$ of value 1pF is used.

Regarding point 4) in paragraph 3.2 (oxide gradient), for larger network capacitances equation [3.1] no longer holds. A more realistic approach would be to use the formula given below, where the value of the relative error due to the oxide gradient is taken as 0.0009 and $(\Delta C/C)_g = 0.01$;

$$(\Delta C/C)_m = \left[\left(\frac{SD[C_m]}{C_m} \right)^2 + (0.0009)^2 \right]^{1/2} = \frac{[1/m + 0.09^2]^{1/2}}{100} \quad [3.4]$$

For $m < 124$ random errors dominate, with larger m the error from oxide gradients is the major factor.

Double-poly capacitors are employed because this capacitor type is linear and the top-plate parasitic capacitance is very small (approx. 0.01C, dependent on layout). When the top-plate is connected to the common node in each stage for network capacitors and to the most significant stage for coupling capacitors, then for the bulk of the circuit only 1% parasitics are present. The size of parasitic capacitors is suspect to vary widely. Several process dependent parameters such as oxide thickness and actual physical shape of these layers will introduce no errors in capacitor ratios but have a large effect on the actual parasitic capacitance value. Keeping the parasitic capacitance as small as possible is thus very important. Here the relative error of parasitic capacitances is taken as 20%. Additional error reduction is achievable with the introduction of "completion capacitors". These are unit capacitors connected between ground and each stage node, effectively they are connected in parallel with the stage parasitics. If the relative error in the completion capacitor is smaller than the relative error in the total stage parasitic, then the relative error of the parallel combination is also smaller. Appropriate scaling of the coupling capacitors will accommodate this circuit change.

For non-unit capacitances such as the coupling capacitors, the width and length must be chosen according to equations [3.2] and [3.3]. Coupling capacitors are larger than unit capacitors, so they have a somewhat smaller relative error. Small systematic errors will however still be present in these capacitors (corner rounding, non-uniform undercut),

counteracting the accuracy increase. For these capacitors a relative error of 1% is used in calculations.

We have derived the following relative capacitor accuracies;

network	$\Delta C/C = [1/m + 0.09^2]^{1/2} \%$	$C = mC_u, m=1,2,\dots$
completion	$\Delta C/C = 1 \%$	$C = C_u$
coupling	$\Delta C/C = 1 \%$	$C_u: 40\mu m \times 40\mu m, 1 \text{ pF}$
parasitic	$\Delta C/C = 20 \%$	

These values are used in a worst case and Monte Carlo analysis of several digital-to-analog converters, the subjects of the next two paragraphs.

3.4 WORST CASE ANALYSIS

In this paragraph a comparison is made between the converter types shown in figure 3.6. Included are three 3-stage DAC's, each with a different capacitor distribution among the stages. Also a 2-stage and 1-stage DAC are included, they serve as references. The point to be compared are lsb-voltage V_{dac} , total capacitance, worst case error and contribution of each capacitor to the worst case error. As can be seen in figure 3.6 no completion capacitor is used in the last stage for multi-stage DAC's and in the 1-stage DAC. This is not done because this completion capacitor reduces V_{dac} . Also in contrast to variations in parasitics of lower stages which introduce linearity errors, variations in the last stage parasitic only result in gain errors.

By inspection of the transfer functions and with the knowledge of the previous paragraphs it can be expected that increasing the number of stages will also increase the worst case error. Furthermore for DAC's with the same number of stages, the DAC with the largest number of network capacitors connected to the last stage will probably have the smallest worst case error. Both capacitor layout strategies reduce the influence of parasitic capacitances in the transfer functions.

The purpose of the comparison is to select a DAC which fulfills the accuracy requirements (worst case error $< 1/2\text{LSB}$) but uses minimal total capacitance. Secondly the comparison is used to show the effect of different capacitor layouts.

Worst case analysis implies that all individual errors are working maximal in the same direction. For this reason no hand calculations were performed as they result in very complex formulas. The calculation of the sensitivity in output voltage to a change in nominal value of only one capacitor is not that hard. But as this sensitivity is also dependent on the input word and all capacitor must be considered, the calculations are almost impossible to perform if the worst case error has to be found. As far as the transfer function is concerned any deviation in nominal capacitor value is an error source. To model such deviations it is assumed that each capacitor C_i is a random variable with a normal or gaussian probability density function (PDF), mean value $C_{i,\text{nom}}$ and standard deviation $\sigma_i = (\Delta C/C)_i C_i$. The maximum deviation from the nominal value is infinite in this model. However such deviations are very unlikely, here the maximum deviation is taken as 3σ . The probability that a gaussian random variable C_i has a value in the range $[C_i - 3\sigma_i, C_i + 3\sigma_i]$ is equal to 0.997, almost unity. Deviations larger than 3σ are thus very rare.

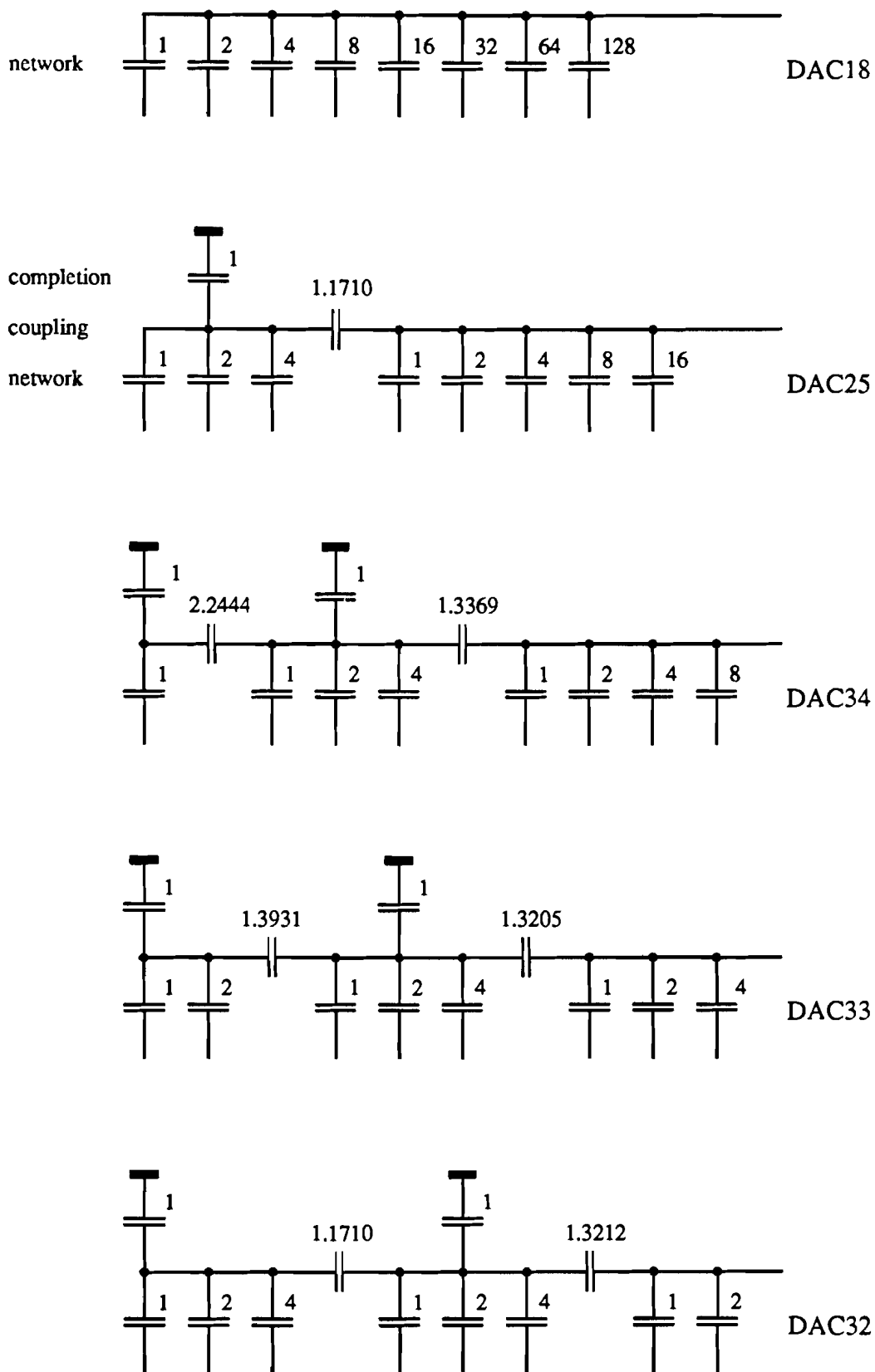


Figure 3.6 DAC versions (buffer and switches not shown)

To calculate the worst case error the following procedure is used:

For each capacitor C_i and for each input word b_j the partial derivative D_{ij} is calculated, giving Jacobian matrix D ;

$$D_{ij} = \left| \frac{\delta V_{out}(C, b_j)}{\delta C_i} \right|$$

where $j=0,1, \dots, 255$ and $i=0,2, \dots, N-1$
 N = number of capacitors in the circuit, parasitic capacitors connected to each common stage node are summed to form the stage parasitic C_{p1}, \dots, C_{p3}

Equations [2.13a] to [2.14] (2-stage DAC) and [2.16a] to [2.17b] (3-stage DAC) are used to calculate parasitic- and coupling capacitance. The output voltage as a function of vectors C and b is given by equations [2.12] and [2.15].

Next define the maximum relative error vector r as

$$r = (3\sigma_0/C_0, \dots, 3\sigma_{N-1}/C_{N-1})^T = (3(\Delta C/C)_0, \dots, 3(\Delta C/C)_{N-1})^T$$

The error in least significant bits is then given by

$$e = D \ r / V_{dac}$$

$$e = (e_0, e_1, \dots, e_{255})^T$$

Finally the worst case error is defined as the norm of e , the largest element of e .

Programs in PASCAL were written for the five DAC versions to calculate the worst case error, V_{dac} and the contribution of each capacitor to the worst case error. Appendix B gives the source code of one of these programs applied to DAC32. The programs differ only in the number of capacitors and the transfer function. Appendix B also includes a list of the relative error and size of all capacitors for the four other DAC versions.

Table I summarizes the obtained simulation results, table II gives the contribution in percent of each capacitor to the total worst case error. The following conclusions can be drawn from these tables.

- 1) As expected fewer stages result in a more accurate DAC
- 2) More capacitors in the last stage result also in a more accurate DAC
- 3) None of the DAC versions has an error smaller then 1/2LSB
- 4) The last stage parasitic is responsible for at least 50% of the worst case error for the 1- and 2-stage DAC
- 5) The 3-stage DAC's suffer relatively more from errors in last stage network capacitors, 37 to 51% of the worst case error

Table I Worst case error

DAC version	DAC18	DAC25	DAC34	DAC33	DAC32	
total capacitance	255	40.2	28.6	21.7	21.5	C_u
LSB voltage	7.765	7.704	7.653	7.544	7.442	mVolt
worst case error	1.76	2.98	3.25	4.30	5.25	#LSB
@ input word	224	195	159	159	127	decimal

Table II Error distribution (% of worst case error)

DAC version	DAC18	DAC25	DAC34	DAC33	DAC32
C_0	1.48	0.59	0.36	0.18	0.09
C_1	2.11	0.84	0.41	0.26	0.12
C_2	3.01	0.85	0.59	0.54	0.18
C_3	4.33	6.04	0.84	0.78	0.90
C_4	6.31	8.61	5.78	1.10	1.28
C_5	1.41	12.3	12.8	13.5	1.82
C_6	2.19	5.84	18.2	19.3	19.3
C_7	3.58	8.52	16.9	18.2	24.6
C_{p1}	75.6	1.64	2.76	1.85	1.91
C_{p2}	–	51.6	6.77	11.0	16.5
C_{p3}	–	–	29.3	25.2	14.9
C_{cm1}	–	0.42	0.56	0.52	0.48
C_{cm2}	–	–	1.43	2.25	3.68
C_{cp1}	–	2.78	0.34	0.19	0.20
C_{cp2}	–	–	2.91	5.28	14.0

Noting that the last stage parasitic only introduces a gain error, it may be neglected. If this error is subtracted, still only the 1-stage DAC is satisfactory. The worst case errors for this converter then is 0.44LSB. The 3-stage DAC's don't fulfill the accuracy requirements, and regarding point 5) a reduction is only possible if larger unit capacitors are used. But as the probability that all capacitors deviate precisely in the right direction and by more than 3σ is very small, the worst case error in practice seldom occurs;

$$\text{Probability}[C > C_{nom} + 3\sigma] = \text{Probability}[C < C_{nom} - 3\sigma] = 0.0015$$

For a capacitor network with 9 capacitors;

$$\text{Probability}[\text{all } C\text{'s deviate more then } 3\sigma \text{ from } C_{nom}] = (0.0015 + 0.0015)^9 = 2 \times 10^{-23}$$

We can therefor expect that typical production samples of the DAC are far more accurate, including the 3-stage converters. Monte Carlo analysis is a tool that can be used to predict the number of elements in a total of N , which have a certain quality. This is done in the next paragraph.

3.5 MONTE CARLO ANALYSIS

Choosing a converter type on the basis of worst cases error analysis is much too conservative. A more realistic approach would be to perform a Monte Carlo analysis. Then a choice can be made on the basis of expected, in stead of maximum, deviations in capacitor values. We then maybe can chose one of the 3-stage DAC's which have the advantage of smaller total capacitance. The purpose of the Monte Carlo analysis is to select a DAC version which has an error smaller then 1/2LSB with at least 75% probability.

Assuming as before normal distributed capacitor value errors, with the same standard deviations, the five converter types in this paragraph are subject of a Monte Carlo analysis. A disadvantage of this method is the large number of simulations that have to

be performed to get reliable results. For fabricated IC's there is always the possibility of large errors, the origin can either be the NMOS fabrication proces (larger oxide thickness variations then estimated, larger undercut, etc., so σ is higher) or just a DAC sample with large individual capacitor errors. Measuring a large number of DAC's would solve this problem but this takes too much time.

In simulation there is the additional difficulty of how to generate normal distributed numbers. However recognizing that uniform distributed numbers can easily be generated, using a custom written subroutine*) or the standard pascal function 'RANDOM', we can try to use a transformation of these numbers to obtain normal distributed numbers. The method of finding that transformation is given below.

Fist consider the function $y=f(x)$, with inverse $x=f^{-1}(y)$, for which

$$p_y(y) = \frac{1}{\sqrt{2\pi}\sigma_y} e^{-(y-\bar{y})^2/2\sigma_y^2} \quad \text{all } y \quad \text{normal distribution} \quad [3.5]$$

$$p_x(x) = 1 \quad 0 < x \leq 1 \quad \text{uniform distribution} \quad [3.6]$$

Since each value of x corresponds to a unique value of y , the probability of finding x in some differential range dx , equals the probability that y is in the corresponding range dy . Thus

$$p_x(x) |dx| = p_y(y) |dy| \quad [3.7]$$

Where absolute values are used to ensure that $p_y(y)$ will be non-negative. Solving for $p_y(y)$ and inserting $x=f^{-1}(y)$ then yields

$$p_y(y) = p_x(x) |dx/dy| = p_x[f^{-1}(y)] |df^{-1}(y)/dy| \quad [3.8]$$

With p_x and p_y according to equations [3.5] and [3.6], substitution yields

$$f^{-1}(y) = \int \frac{1}{\sqrt{2\pi}\sigma_y} e^{-(y-\bar{y})^2/2\sigma_y^2} dy \quad [3.9]$$

Unfortunately the integral cannot be solved, and thus no exact transformation is available. In practice numerical methods are used to calculate this integral in closed form. There is however a function

$$y = f(x) = \sqrt{-2\sigma^2 \ln(x)} \cos(2\pi x) \quad [3.10]$$

that transforms the uniform distributed variable x to an almost normal distributed variable y . Figure 3.7 gives simulation results using equation [3.10]. For 30,000 generated numbers the frequency function (or discrete probability density function), $P(x_j) = P(x_j < X < x_j + \Delta x)$, with $\Delta x = \sigma/20$, was calculated. As can be seen in figure 3.7 the difference with the normal PDF is very small.

A modified version of the worst case program (see appendix B) is used to calculate the yield in a total of 500 identical DAC's. Yield is here defined as the percentage in the total with an error smaller then ϵ , $\epsilon = 0.1\text{LSB}, \dots, 1.0\text{LSB}$. The procedure is as follows.

*) The routine makes use of the fact that in PASCAL variables have an arbitrary value if they are not initialized

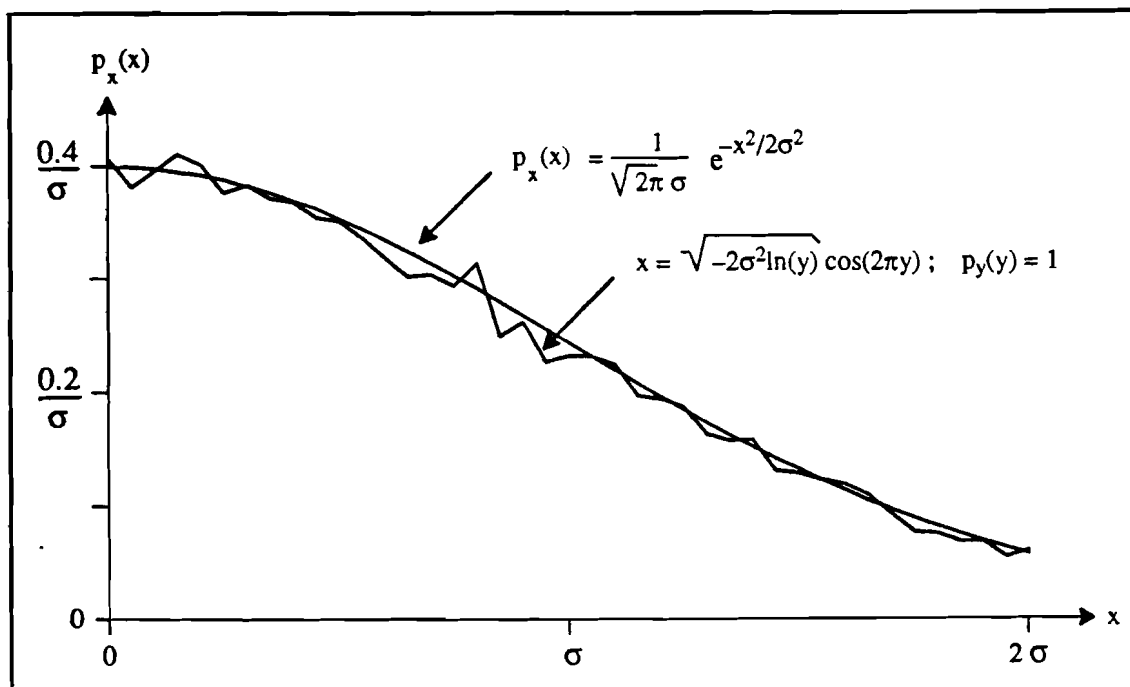


Figure 3.7 Normal PDF and simulated DPDF

First all nominal capacitor values $C_{nom,i}$ are displaced by a factor d_i calculated with equation [3.10], so

$$C_{d,i} = C_{nom,i} (1 + d_i)$$

Next using the transfer function corresponding with the DAC version, the output voltage is calculated for all input words b_j giving a total of 511 output voltages. These are then used to calculate V_{dac} and V_{odac} according to equations [2.5] and [2.6]. The error is now defined as the maximum difference

$$|V_{out}(C_d, b_j) - (V_{dac} G_{eq} + V_{odac})|$$

$$j = -255, \dots, 255$$

$$G_{eq} = \text{decimal equivalent of the binary input word } b_j$$

The above steps are repeated 500 times, giving 500 error-, V_{dac} - and V_{odac} -values. Now define

$$Y_\epsilon = \frac{\text{[number of errors} \leq \epsilon]}{500} \times 100\%$$

$$\epsilon = 0.1\text{LSB}, 0.2\text{LSB}, \dots, 1.0\text{LSB}$$

Furthermore the mean value and standard deviation of V_{dac} are determined with

$$\bar{V}_{dac} = (V_{dac}[1] + \dots + V_{dac}[500]) / 500$$

$$SD = (|\bar{V}_{dac}^2 - (\bar{V}_{dac})^2|)^{1/2}$$

The standard deviation of V_{dac} provides a measure for gain errors between DAC's in encoder and decoder. While the output voltage is the same for positive and negative

input words (except for the sign), the offset voltage V_{off} can be neglected. Table III summarizes the simulation results obtained for the five DAC versions. The last row of this table gives the maximum gain ratio error between two DAC's. Here the same reasoning is applied as in the worst case analysis: the probability that V_{off} has a value in the range $[V_{\text{off}}-3\text{SD}, V_{\text{off}}+3\text{SD}]$ is almost unity.

Table III Yield Y_ϵ

DAC version	DAC18	DAC25	DAC34	DAC33	DAC32	
mean LSB voltage	7.765	7.703	7.653	7.546	7.441	mVolt
SD LSB voltage	15.6	20.5	16.2	18.2	18.1	μVolt
Yield for $\epsilon =$						
0.1LSB	21	1	0	0	0	%
0.2LSB	80	10	5	2	2	
0.3LSB	98	39	16	8	8	
0.4LSB	100	64	38	20	16	
0.5LSB	100	83	60	34	27	
0.6LSB	100	93	75	48	36	
0.7LSB	100	98	87	61	48	
0.8LSB	100	99	92	72	57	
0.9LSB	100	100	96	81	66	
1.0LSB	100	100	99	88	75	
$\frac{\bar{V}_{\text{off}} \pm 3\text{SD}}{\bar{V}_{\text{off}} \mp 3\text{SD}}$	± 0.11	± 0.14	± 0.11	± 0.13	± 0.13	dB

The following conclusions can be drawn from the table

- 1) Fewer stages result in a higher yield
- 2) More capacitors in the last stage result also in a higher yield
- 3) The yield $Y_{0.5\text{LSB}}$ for the 1-stage and 2-stage DAC's is very high, respectively 100 and 83%
- 4) $Y_{0.5\text{LSB}}$ is much lower for the 3-stage DAC's, ranging from 60% for DAC34 to 27% for DAC32
- 5) The gain-ratio error is very small (< 0.14 dB), and is thus not exceeding the ± 0.17 dB limit derived in paragraph 2.2

The overall conclusion is that only the 1- and 2-stage DAC are satisfactory. The size reduction achievable with 3-stage DAC's introduces faults that are too high. The only way this can be circumvented is using larger capacitors. But then the preference for 3-stage DAC's is no longer valid. An alternative is increasing the number of network capacitors in the last stage, but this method also increases the total capacitance.

Some concluding remarks regarding DAC capacitor topology are appropriate here. For an 8-bit DAC there are many other capacitor layouts possible. One method that seems promising is using smaller unit capacitors. We then can use a 2-stage DAC without any significant increase in total capacitance compared to 3-stage DAC's. As is shown by Shyu the increase of $\Delta C_u/C_u$ for random errors is proportional to $1/\sqrt{C_u}$. For a size reduction with factor 2.5, the relative error only increases with factor 1.6. Knowing

from the worst case analysis that for 2-stage DAC's network capacitors contribute much less to the error than 3-stage DAC's, some decrease in relative accuracy of these capacitors may be acceptable in a 2-stage network. Next regarding conclusion 2) and using a 2-stage DAC, we can increase the number of (smaller) network capacitors in stage 2 to counteract this decrease in relative accuracy.

As an example consider a 2-stage DAC, DAC26, with 2 network capacitors in the first stage and 6 in the second stage. Unit-capacitors with plate size $25\mu\text{m} \times 25\mu\text{m}$ are used for this version. The total capacitance is approximately $70C_u$, equivalent with $70/2.5=28$ unit capacitors of $40\mu\text{m} \times 40\mu\text{m}$. So DAC26 has the same size as DAC34. If we assume a 1.6% relative error for the smaller unit capacitors, 3% for the coupling capacitor, and 20% for the parasitic capacitors, then the worst case error is 2.98LSB (the same as for DAC25). The yield for errors smaller than 0.5LSB is 71%, just below the target value.

As final choice it is decided to use DAC25 as digital-to-analog converter in the SADM. DAC26 is an alternative with smaller total capacitance. Both converters are intended to be fabricated.

3.6 CAPACITOR NETWORK LAYOUT

To achieve the high accuracy of DAC25 and DAC26 the layout of the capacitor network must be done with great care. Parasitic capacitance from interconnection wires is here the major problem. Therefore they are incorporated as part of the unit-capacitor structure. However the placement of individual capacitors is more difficult for this layout scheme. Figure 3.8 illustrates the unit-capacitor structure and dimensions for the two plate-sizes as used in DAC25 and DAC26.

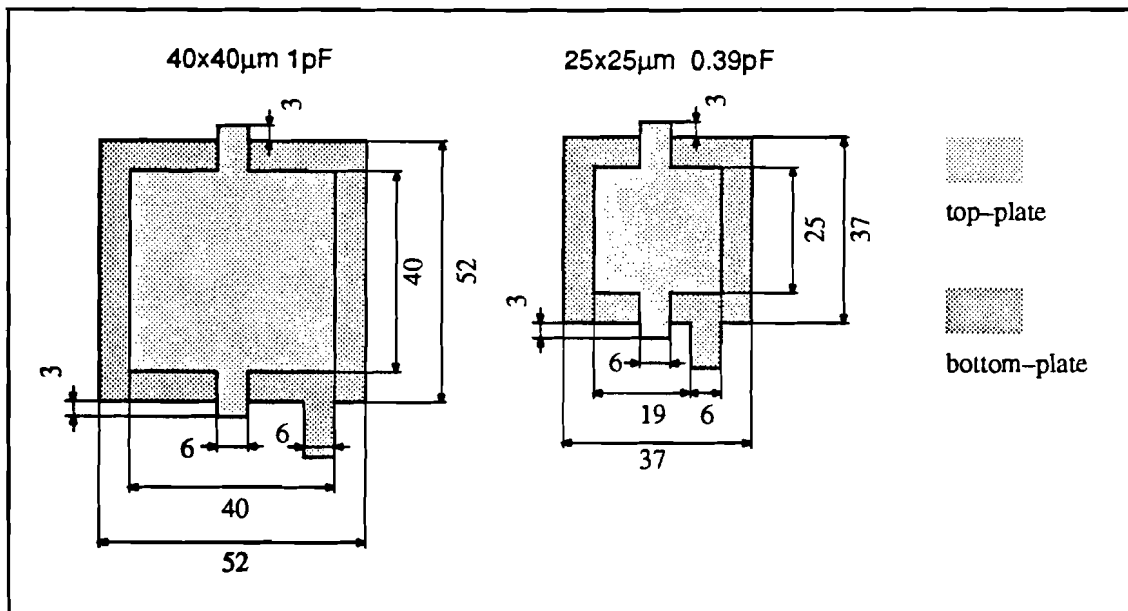


Figure 3.8 Dimensions unit capacitors

The following points need extra attention. First because the bottom-plate parasitic isn't important the lead-out wire for that plate can have any reasonable length. This gives some freedom in placement of the capacitors. Secondly top-plate lead-out wires are all $9 \text{ by } 6 \mu\text{m}$, and precisely two are used for each unit-capacitor. This means that unit-capacitors forming a larger capacitance, have to be placed in such a way that they

precisely touch. Thirdly for minimal area, every capacitor must be placed exactly $6\mu\text{m}$ apart from surrounding capacitors. In figure 3.9 an example is given of how a 4-capacitor array must be interconnected.

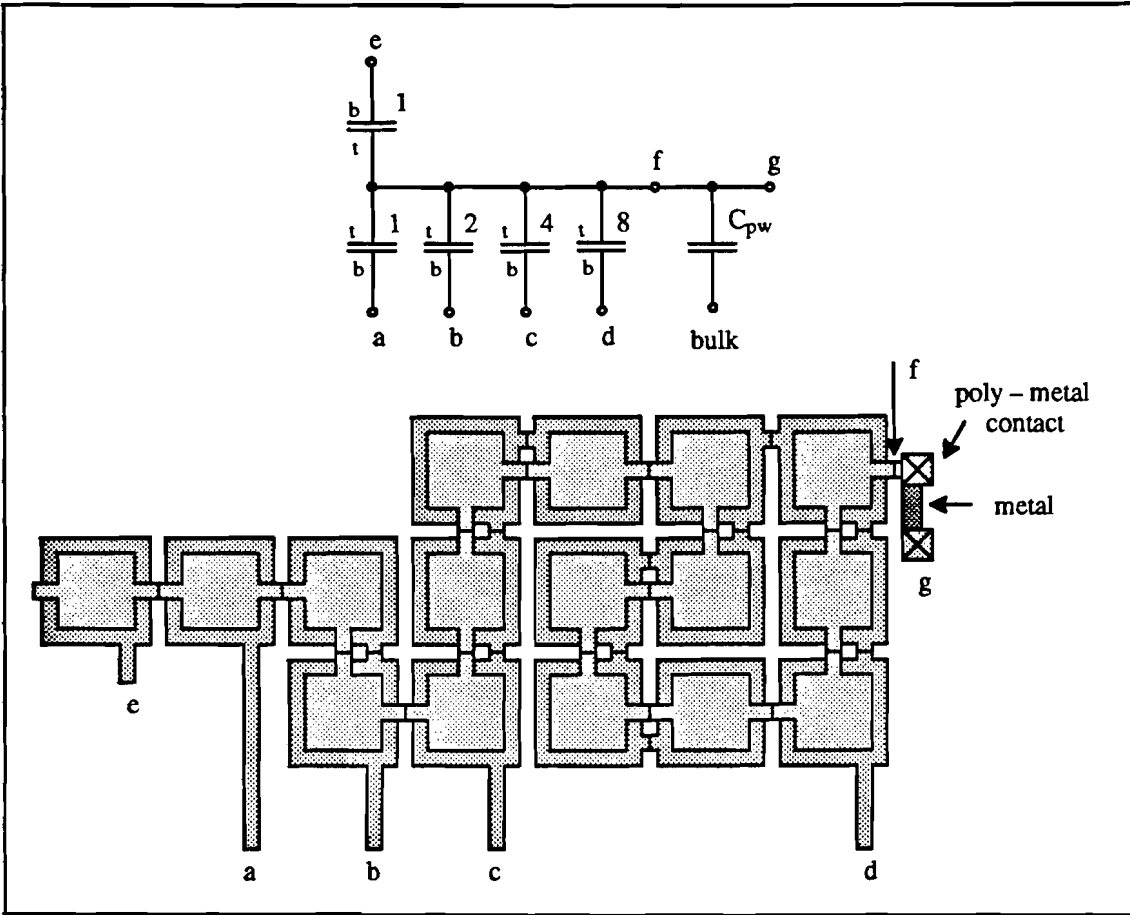


Figure 3.9 Capacitor array interconnections

Coupling capacitors are connected with their bottom-plate to the top-plate of network capacitors. In the EFFIC NMOS technology it is not possible to directly connect two different poly layers. A short metal interconnect wire is thus necessary, with two metal-poly contact holes. The parasitic metal-bulk capacitance of this wire (C_{pw}) must be accounted for in equation [2.13a], the total stage parasitic capacitance. Also equation [2.14] changes, the size of the coupling capacitor is altered. Furthermore the completion capacitor at the first stage wasn't considered in these equations. Equations [3.11] and [3.12] give the correct capacitor sizes;

$$C_{p1}^* = \sum_{\text{stage } 1} \epsilon_i C_i + \epsilon_1 C_{cm} + \epsilon_b C_{cp1}^* + C_{pw} \quad [3.11]$$

$$C_{cp1}^* = \frac{\sum_{\text{stage } 1} C_i + C_{p1}^* + C_{cm}}{\frac{2C_{N1+1}}{C_{N1}} - 1} \quad [3.12]$$

CHAPTER 4 OPERATIONAL AMPLIFIER DESIGN

4.1 FUNCTIONAL DEMANDS

To interface the capacitor network with the environment a buffer is necessary. The main function of this buffer is preventing charge leakage. An operational amplifier (opamp) applied as unity-gain buffer is used to perform this function.

Perfect buffers will exactly follow the input signal with no gain error, delay or compression. In practice these demands can't be met and are not called for. Less conservative requirements apply when for instance the allowed conversion time, maximum input voltage range and resolution of the DAC are considered.

In this paragraph an overview is given of limits placed upon several opamp parameters. The most important result from speed limitations in the opamp; unity gain bandwidth (f_{UGB}) and slew rate (SR). Other parameters such as DC-gain (A_{DC}) and common mode rejection ratio (C or CMRR) are not that critical as will be shown later in this paragraph. For purposes of analysis the opamp's frequency dependent gain $A(s)$ and CMRR $C(s)$ are modeled as first order functions

$$A(s) = \frac{A_{DC}}{1 + s\tau_A} \quad \text{gain} \quad [4.1]$$

$$C(s) = \frac{C_{DC}}{1 + s\tau_C} \quad \text{CMRR} \quad [4.2]$$

The input-output relation of the opamp is presented as

$$V_{out}(s) = A(s) \left[[V_{ninv}(s) - V_{inv}(s)] + \frac{V_{ninv}(s) + V_{inv}(s)}{2C(s)} \right] \quad [4.3]$$

Equations [4.1] to [4.3] are utilized to derive lower and upper limits for some opamp parameters, which are summarized below

1) DC-gain and CMRR

For the buffer application $V_{inv}=V_{out}$ and $V_{ninv}=V_{in}$, next assume $\tau_C A_{DC} \ll \tau_A 2C_{DC}$ then the transfer of the buffer is given by

$$H_{buf}(s) \approx \frac{A_{DC}}{1+A_{DC}} \frac{2C_{DC}}{2C_{DC} - \frac{A_{DC}}{A_{DC}+1}} \frac{1}{1+s\tau_A/(1+A_{DC})} = H_{DC} \frac{1}{1+s\tau_A/(1+A_{DC})} \quad [4.4]$$

In equation [4.4] we notice that the buffer gain is not unity, instead it is dependent on both A_{DC} and C_{DC} . The absolute values of DC-gain and DC-CMRR are not important, rather the variation in these parameters as the input voltage to the buffer changes. We can however allow considerable absolute errors in A_{DC} and C_{DC} before the relative error in H_{DC} exceeds the resolution of an 8-bit DAC ($2^{-(8+1)}$ or 0.2%). For example take

$$A_{DC} = 750 \pm 250 \quad \text{and} \quad C_{DC} = 10000 \pm 3000$$

$$\text{then } \Delta H_{DC}/H_{DC} = 0.05\%$$

The relative error is a factor 4 smaller then the DAC resolution. So no limits apply for the DC-gain and CMRR.

2) Unity-gain bandwidth

The response of the buffer to a step-function $V_m(t)=Eu(t)$ is easily derived as

$$V_{out}(t) = E H_{DC} [1 - e^{-t/\tau_1}] \quad [4.5]$$

$$\text{where } \tau_1 = \frac{\tau_A}{1 + A_{DC}} = \frac{1}{2\pi f_{UGB}} \quad [4.6]$$

It is required that the steady-state output voltage, $E \times H_{DC}$, is reached with an error smaller then 0.2% of this final value in 1.5 μsec . The allowed time of 1.5 μsec is the conversion time per phase of the DAC. Substitution in [4.5] yields

$$\frac{1}{\tau_1} \geq \frac{-\ln(0.002)}{1.5 \times 10^{-6}}$$

with [4.6] the lower limit for the unity-gain bandwidth follows

$$f_{UGB} \geq \frac{-\ln(0.002)}{2\pi \cdot 1.5} = 0.66 \text{ MHz} \quad [4.7]$$

3) Slew-rate

Differentiating equation [4.5], we notice that the rate of change of the output voltage is largest at $t=0$. The slew-rate must at least be equal to this value, see figure 4.1.

E is maximal equal to $\pm V_{ref}$ ($= \pm 2 \text{ Volt}$), hence with [4.7]

$$SR \geq 8.3 \text{ V}/\mu\text{sec} \quad [4.8]$$

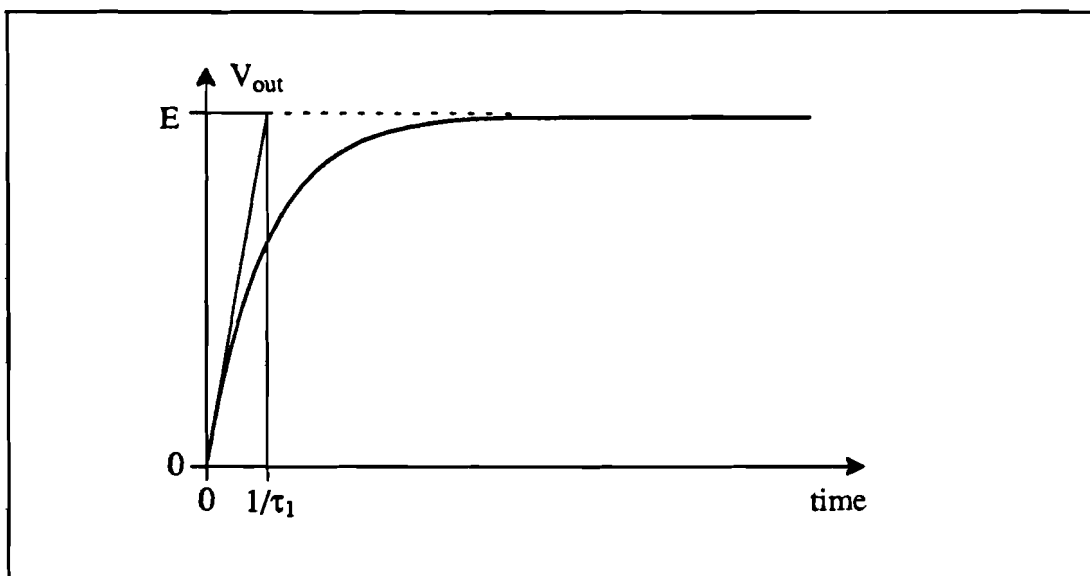


Figure 4.1 Step-response

The calculation of the slew-rate is done assuming that the small-signal parameters are the slew-rate limiting factors. As the slew-rate is a nonlinear large-signal phenomenon, equation [4.8] is only valid if the opamp can source or sink sufficient instantaneous current to charge or discharge the load capacitor.

4) Input offset voltage

In the DAC small offset voltages can be tolerated (see paragraph 2.2). For $V_{\text{dac}}=7.8$ mV and $|V_{\text{out}}|_{\text{max}} = 2$ V, the offset voltage can be as large as $2-255 \times V_{\text{dac}}=11$ mV before the dynamic range is reduced. For a small 1 dB reduction in the dynamic range an additional offset of 200 mV is allowable. Offset in the modulator DAC is only one offset source, other sources are offset from the opamp's used in the input-filter, the output-filter and the demodulator DAC. Assuming that the same type of opamp's are used and offset from the opamp's is the major offset source, the offset voltage value of one opamp should be approximately $(200+11)/4=53$ mV, so:

$$|V_{\text{off}}| < 53 \text{ mV} \quad [4.9]$$

5) Capacitive load

The DAC is connected directly to the loop-filter, the loop-filter performs the subtraction of node voltages V_2 and V_1 (Ref. [10]). The maximum capacitive load is equal to the sum of the two capacitors at the input section of this filter, so

$$C_L = 4 \text{ pF} \quad [4.10]$$

6) Supply voltages/PSRR

The opamp must operate, as the other circuit elements, with a positive supply voltage of +5 Volt, and negative supply voltage of -5 Volt. As the DAC operates at 64 kHz, the output voltage of the opamp changes every 15 μsec . In this short period, mains related interference with frequencies of 50 to 100 Hz doesn't change much and is already suppressed by the voltage regulators in the DC-supply circuit. More meaningful are high frequency rejection ratios, as on the ISDN chip large area is occupied by digital circuits and long supply lines are used. The capacitor array switches are located close to the opamp, they operate at a fundamental frequency of 64kHz. Other digital circuits have switch frequencies in the range 64 kHz to 4 MHz. So the power supply rejection ratio of the opamp must be high over a large frequency range. A lower PSRR limit is hard to determine as the magnitude of interference signals is not known. Good PSRR figures are in general of the same order as the open-loop gain of an opamp.

Methods to minimize interference include the use of separate supply lines for analog and digital circuitry, star supply connections and careful location of circuits on the chip.

7) Output voltage swing

The buffer must operate correctly for input voltages in the range -2 to +2 Volt. For the opamp a minimum output voltage swing in the same range must be possible without any deterioration in opamp performance.

4.2 CIRCUIT DESCRIPTION

In the past several opamps have been designed planned to be fabricated with the NMOS EFFIC technology, references [1], [10] and [18]. From these the opamp designed by Geloven (Ref. [1]) is used because it is one of the latest and it is primarily intended for buffer applications. Furthermore the functional demands of paragraph 4.1 are all satisfied, and the transistor parameters used in SPICE simulations are not significant different from the latest set of january 1990. The only differences are:

- oxide thickness t_{ox} (changed from 60N to 65N)
- electron mobility μ_0 (changed from 680 to 600 for depletion transistors)
- WD (changed from 0.9U to 0.5U)
- LD (changed from 0.75U to 0.5U)

From these changes, the last two have the greatest impact on opamp performance. Therefor new simulations are done with the latest parameter set, to see if the changes effect opamp performance. In figure 4.2 the circuit diagram of the opamp is illustrated. We can divide the circuit in five major parts; input stage, level shifters, intermediate stage, DC-feedback circuit and output stage.

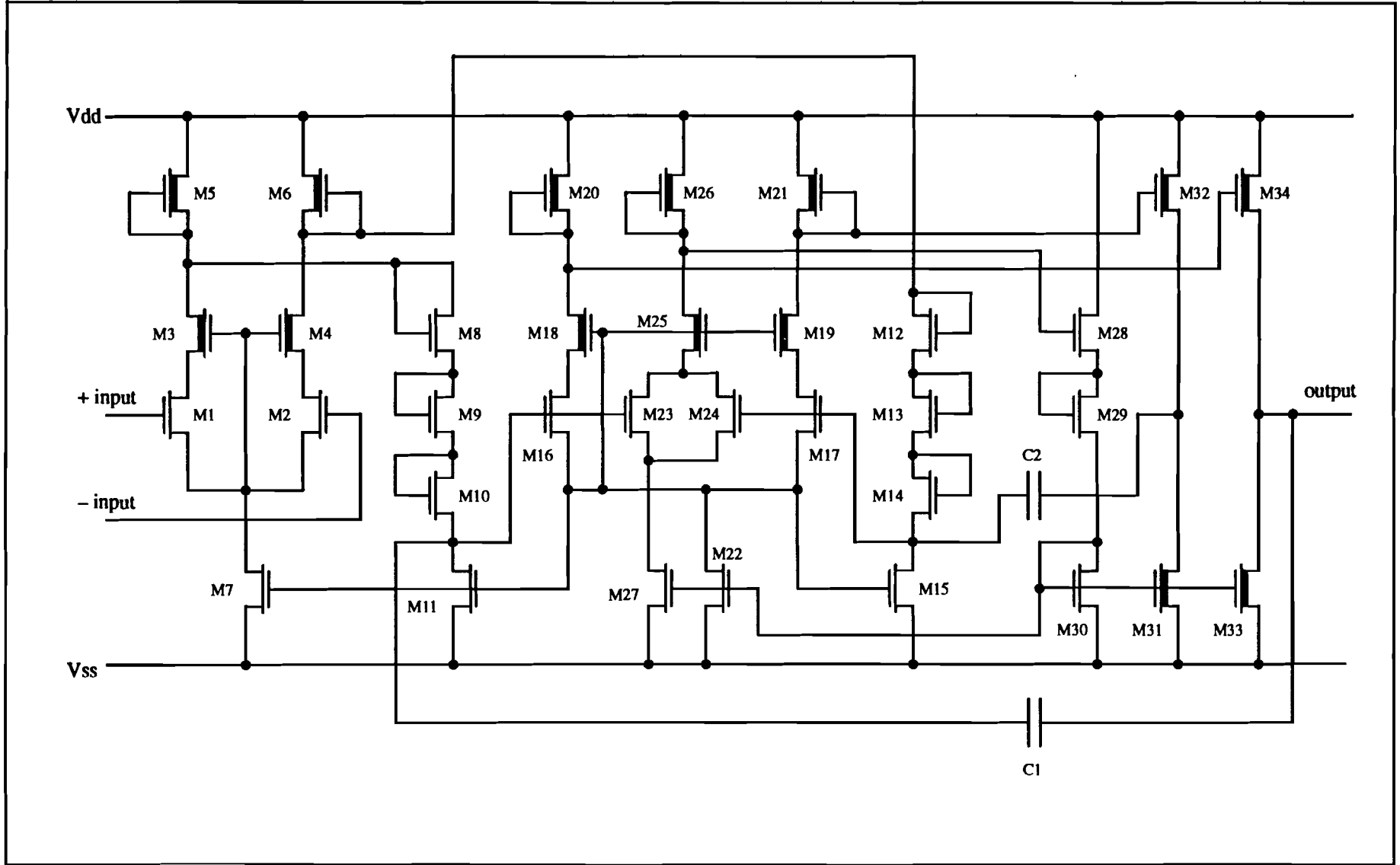
The first stage is the well known differential source-coupled pair with depletion load transistors. The two input transistors M_1 and M_2 are assisted by transistors M_3 and M_4 to form a cascode gain stage. In doing so the *Miller effect* is reduced. Depletion- (M_3 and M_4) instead of enhancement-loads are used because then a higher first-stage gain is possible. The differential configuration helps to achieve a large CMRR and power supply rejection ratio (PSRR), since the differential gain is much higher then the common mode gain. This last observation is valid for signals at the input terminals but also for variations in supply voltages.

The level shifters (M_8 to M_{11} and M_{12} to M_{15}) shift the high DC-level at the output of the first stage the a lower value. A high DC-level guarantees that the transistors in the first stage remain saturated. Saturated transistors are less sensitive to parameter variations resulting from voltage changes then transistors operating in the linear mode. The DC-current flowing in the level shifters is also flowing in transistors M_3 and M_4 . Although this reduces the first stage gain (g_{mb} of transistors M_3 and M_4 higher due to the excess DC-current), it also increases the output resistance of the level shifters (reference [18]). Making it easier to implement the frequency compensation of the opamp.

The current sources of the first stage (M_7), second stage (M_{22}) and level shifters (M_{11} and M_{15}) are part of a feedback loop which stabilizes the DC-conditions and aids the common mode rejection. The dummy network involving transistors M_{23} to M_{27} provides a common mode signal which, after level shifting (M_{28} to M_{30}), is applied to the current source of the second stage. Effectively stabilizing the DC-conditions of this stage. The common-source node voltage of transistor M_{16} and M_{17} contains only the common mode part of the input signals to the second stage. This signal is applied to the current sources of the level shifters and first stage. Improving CMRR and DC operation of the first stage.

The intermediate or second stage (transistors M_{16} to M_{22}) is essential the same as the first stage. It is designed to allow a large maximum voltage swing at the output. Here also a differential cascode gain stage with depletion loads is applied.

Figure 4.2 Circuit diagram operational amplifier



The output stage (M_{31} to M_{34}) was originally designed to drive capacitive loads of maximum 20 pF. It was therefor necessary to use depletion transistors because with the DC-conditions chosen in the previous stages, enhancement transistors would become far to large. The maximum capacitive load is now however smaller, 4 pF, hence we could use smaller output transistors.

To maintain a minimum of 45° phase margin when the opamp is used as buffer and is fully loaded, frequency compensation capacitors C_1 and C_2 are incorporated. These capacitors are connected between respectively the inverting opamp output/non-inverting input second-stage and non-inverting opamp output/inverting input second-stage. Small capacitor values can be used because the output impedance of the level shifters is high and the capacitor size is enlarged by the Miller effect with a factor $1+2A_2$ (A_2 is the gain of the second stage).

4.3 SPICE SIMULATIONS

The opamp designed by Geloven is simulated with the circuit simulator SPICE. Appendix C gives the input file (SPICE circuit description). The differences with the original opamp given in reference [1]*) are;

- New MOS parameter set
- Size of the output transistors
- Larger AS, AD, PS and PD values (larger parasitic capacitance from interconnections)

The simulation results are summarized below.

1) Small signal voltage gain – phase margin

parameter	C_L	0	4	pF
results	A_{DC}	57	57	dB
	f_{UGB}	5.5	5.0	MHz
	PM	62	56	degrees

These values are all within the limits derived in paragraph 4.1;
 $f_{UGB} \geq 0.66$ MHz $PM \geq 45$ degrees

2) Large signal voltage gain – output voltage swing

parameter	V_i	-3.2	0	+2.5	mVolt
results	V_{out}	-2	0	+2	Volt
	A_{VOL}	482	734	823	V/V

The results show that over the output voltage range the gain doesn't change too immoderate. The maximum and minimum value of $A_{VOL}/(1+A_{VOL})$ deviate only by 0.086%. Figure 4.5 shows that for $|V_{out}| > 2V$ the opamp performance rapidly declines.

*) In the layout of this opamp, several design rule violations are present in the output stage, these must be corrected before the opamp can be used as buffer in the DAC.

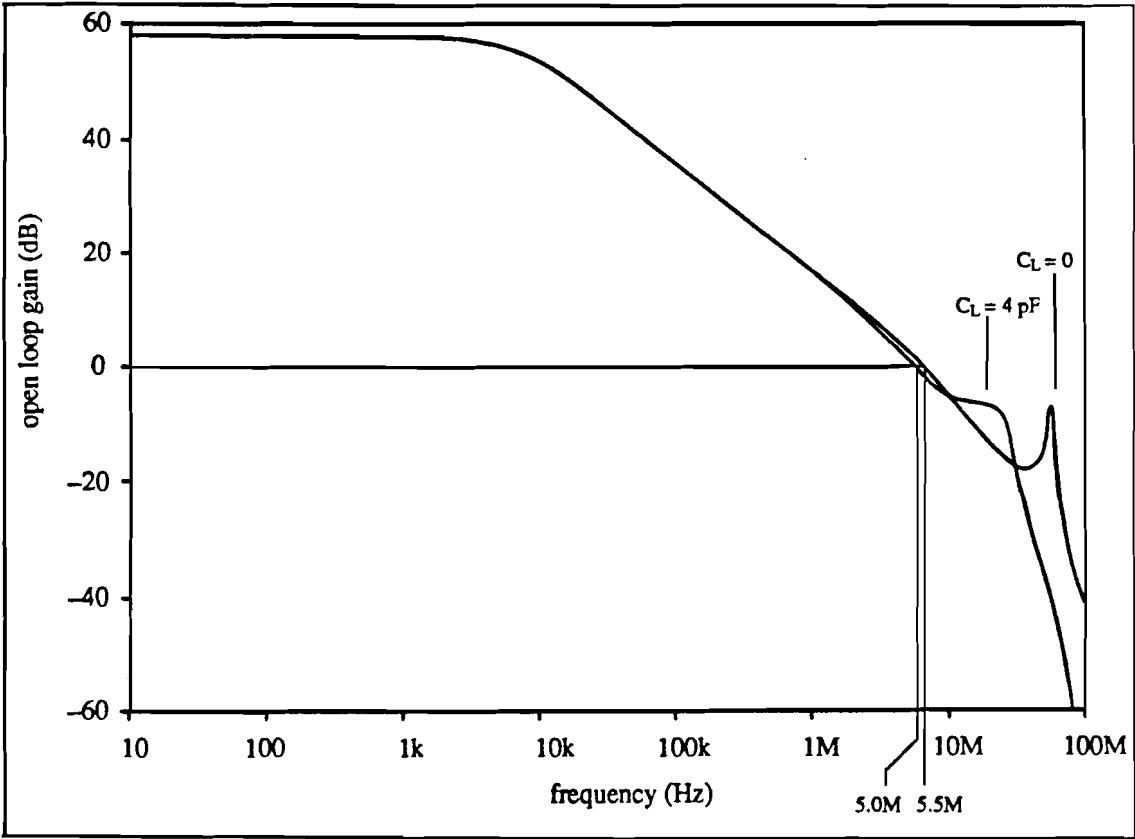


Figure 4.3 Small signal open-loop gain versus frequency

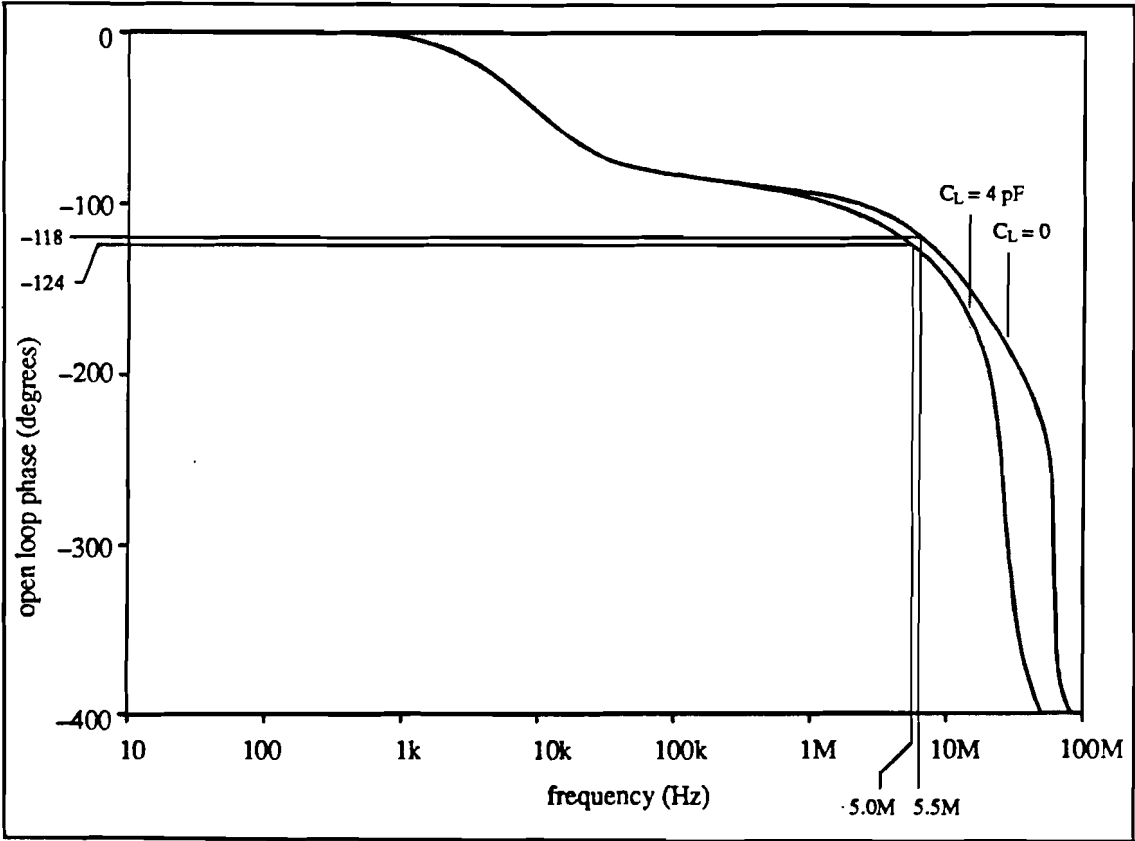


Figure 4.4 Small signal open-loop phase versus frequency

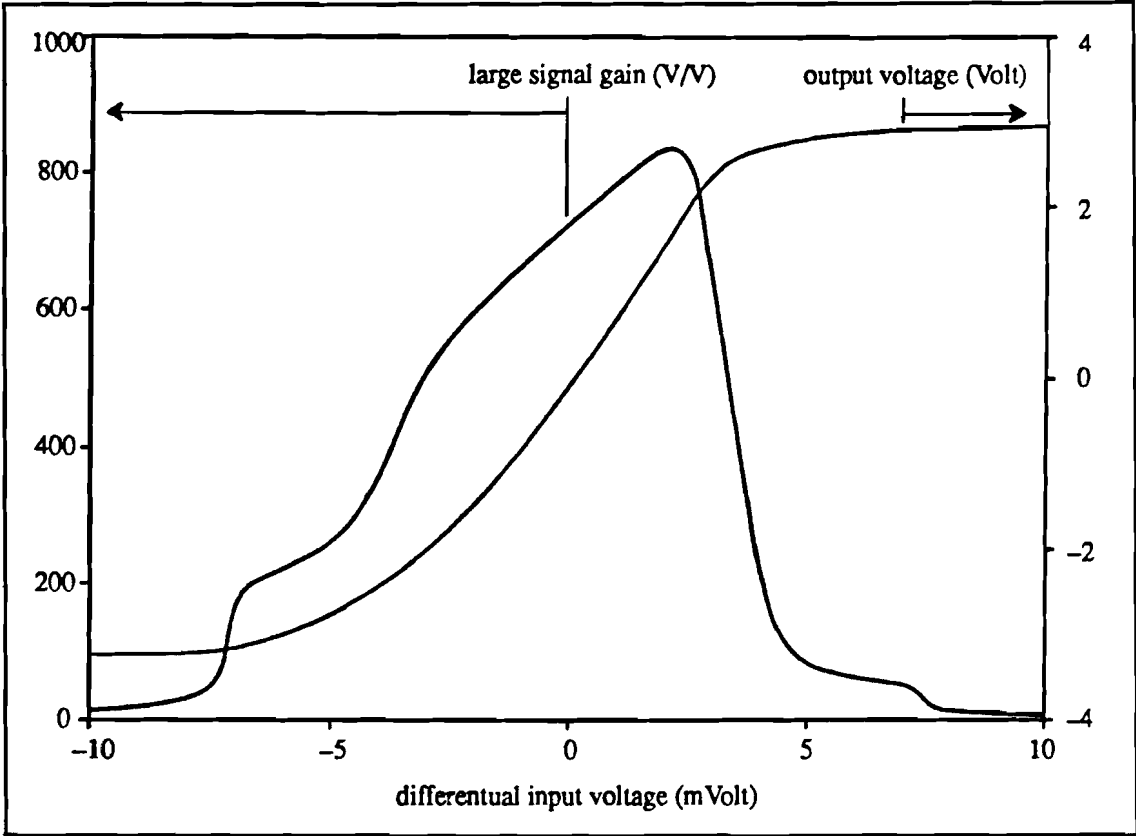


Figure 4.5 Large signal gain and output voltage versus differential input voltage

3) PSRR, positive supply (PSRR+) and negative supply (PSRR-)

parameter	frequency	10	64k	1M	2M	Hz
results	PSRR+	80	62	35	27	dB
	PSRR-	58	40	18	19	dB

PSRR for the negative supply is much lower then for the positive supply line. However they both are of the same order as the open-loop voltage gain $A(f)$.

4) CMRR

In figure 4.7 the CMRR versus frequency is illustrated, the minimum value observed for DC common-mode input voltages in the range -2 to $+2$ Volt is shown. For frequencies smaller then 64 kHz , CMRR values of maximum 155 dB and minimum 96 dB apply. The common-mode input voltage range where $C_{DC} > 100\text{ dB}$ is -3.3 to $+5$ Volt. These values are more then adequate for the buffer application.

5) Slew rate

The slew-rate of the opamp, when loaded with 4 pF , for positive and negative edges is respectively $10\text{ V}/\mu\text{sec}$ and $8.3\text{ V}/\mu\text{sec}$, thus equal to the lower limit derived in paragraph 4.1. The steady state output voltage is reached in 685 nsec , with an error smaller than 0.2% of that final output voltage.

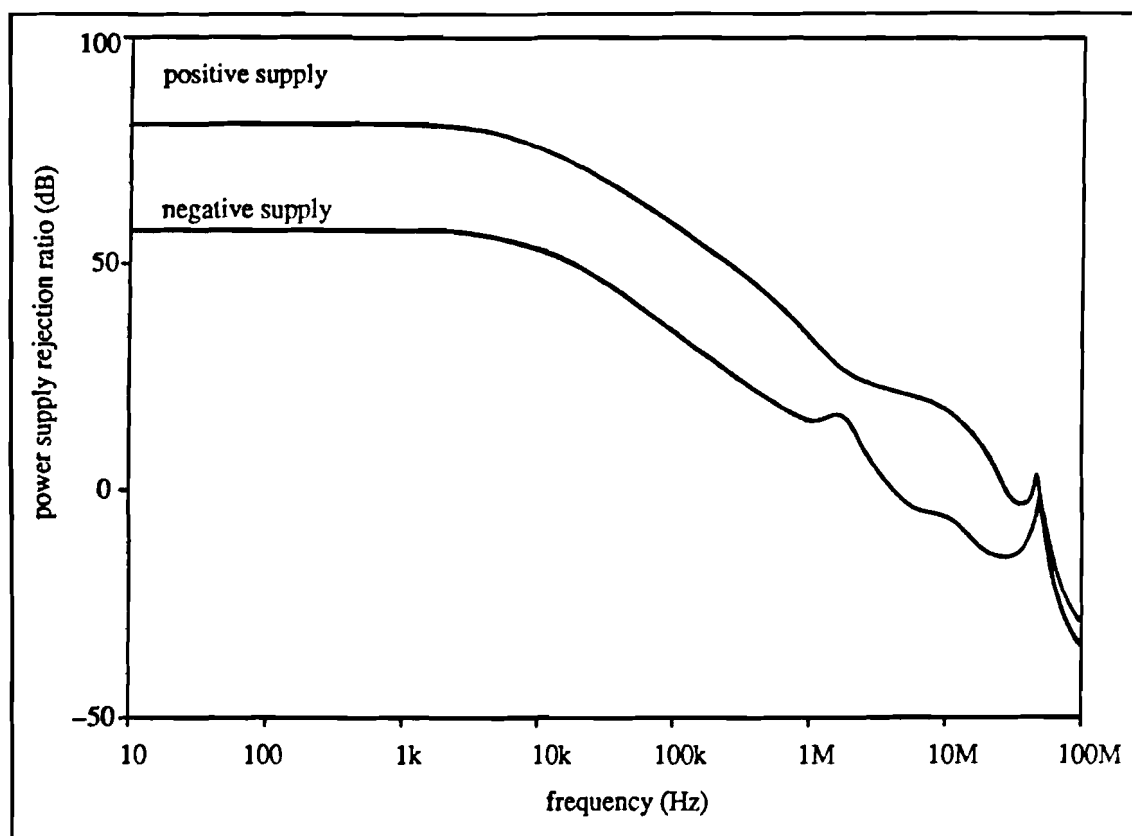


Figure 4.6 Positive and negative supply's PSRR versus frequency

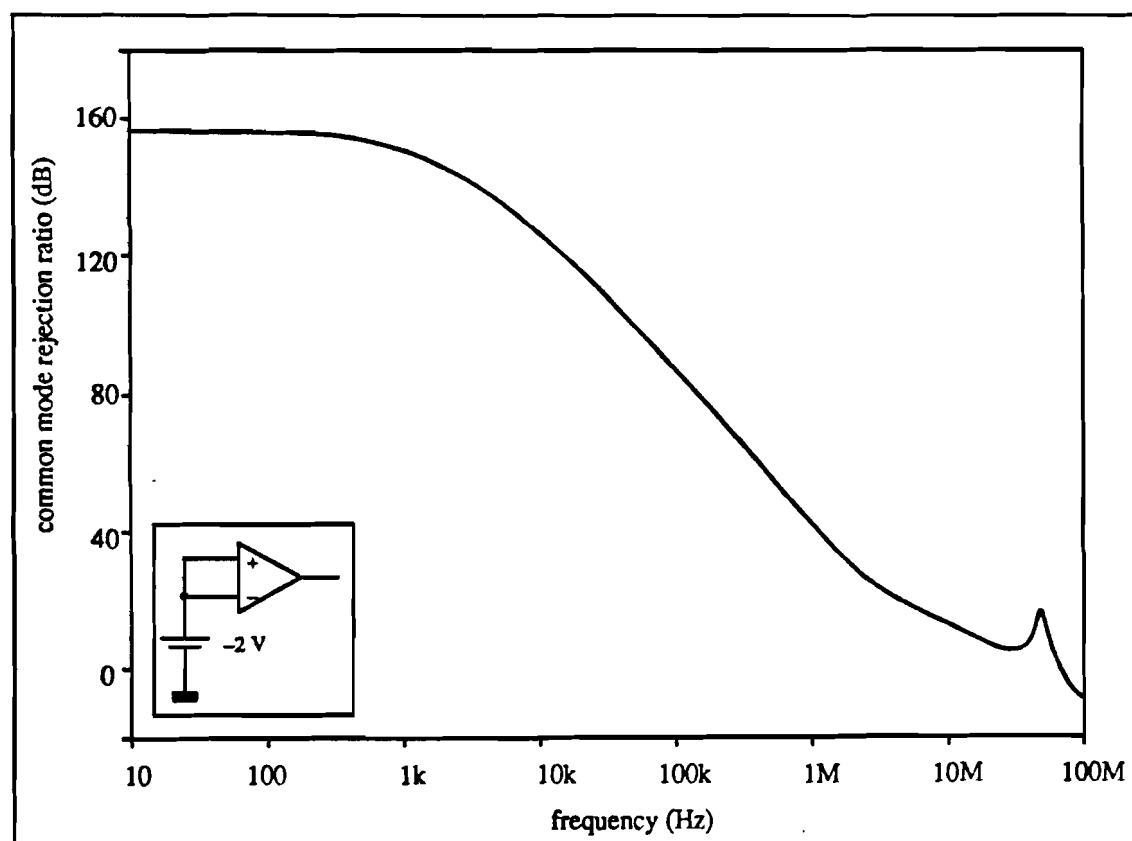


Figure 4.7 CMRR versus frequency, $|V_{com}| < 2$ Volt

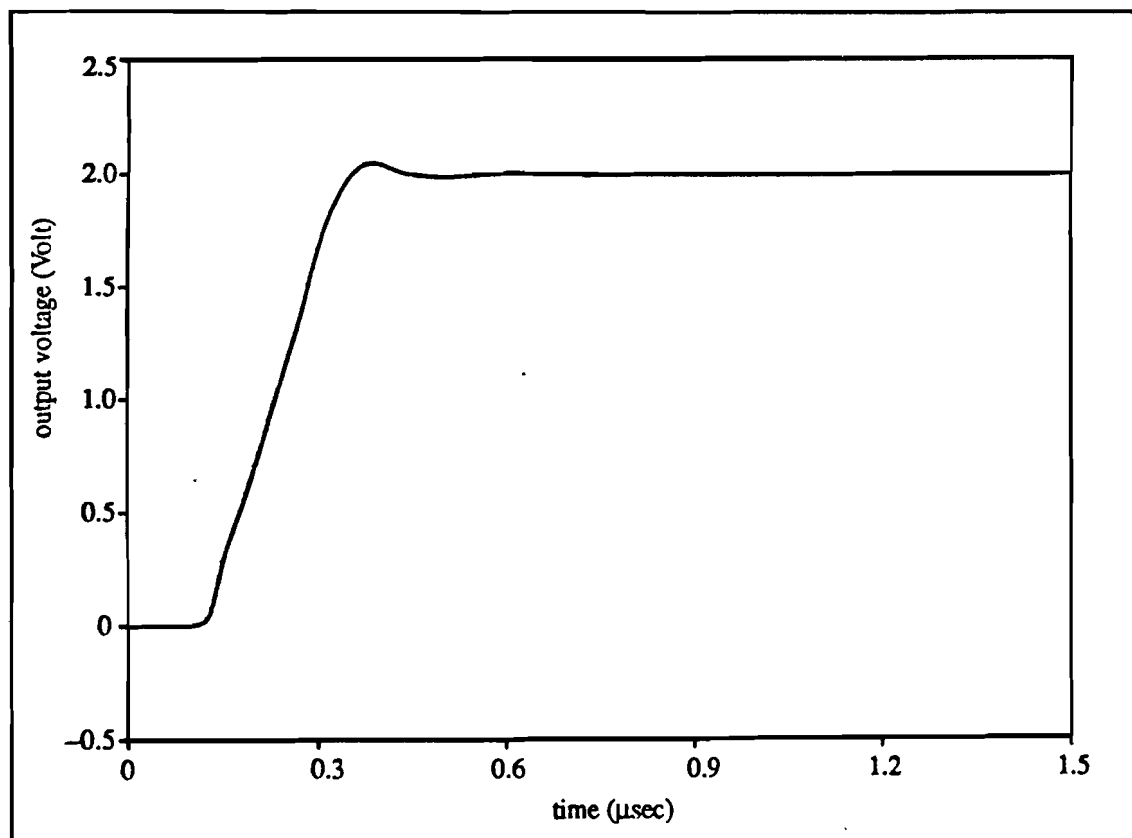


Figure 4.8 Slew-rate, rising edge

6) Offset voltage

The input-referred offset voltage is 14 μ Volt, a negligible value. However the simulation is done assuming equal threshold voltages for all enhancement and all depletion transistors. In practise this will not be the case and an much larger offset voltage can be expected. Offset voltage values not larger then 53 mVolt are acceptable.

The SPICE simulation results show that all functional demands are fulfilled, hence the opamp is suitable as buffer in the DAC. The performance of the combination; capacitor array, switches and opamp, is described in the next chapter.

CHAPTER 5 SPICE SIMULATION DAC

5.1 DAC-TIMING

Until now no realizations of the analog switches and logic circuitry of the DAC have been given. Although the implementation of these circuits has no influence on accuracy, it does control the transient behavior of the DAC. This paragraph deals with this subject. To start first the relation of DAC-timing with respect to the overall SADM-timing has to be established.

Figure 5.1 illustrates the above relation. The digital-to-analog conversion starts when the output of the accumulator is valid, time t_0 . Assuming the 2-complement to sign-and-magnitude translation is done in the accumulator, the digital input to the DAC is a sign-and-magnitude code. From paragraph 2.3 where the switching procedure is described, two phases can be identified in the conversion process. Denote the first phase as *Charge Initiation phase* (time t_0 to t_1 during T_{CI} seconds) and the second phase as *Charge Redistribution phase* (time t_1 to t_2 during T_{CR} seconds). T_{CI} and T_{CR} are chosen equal, hence $T_{CI} = T_{CR} = 1.5\mu\text{sec}$.

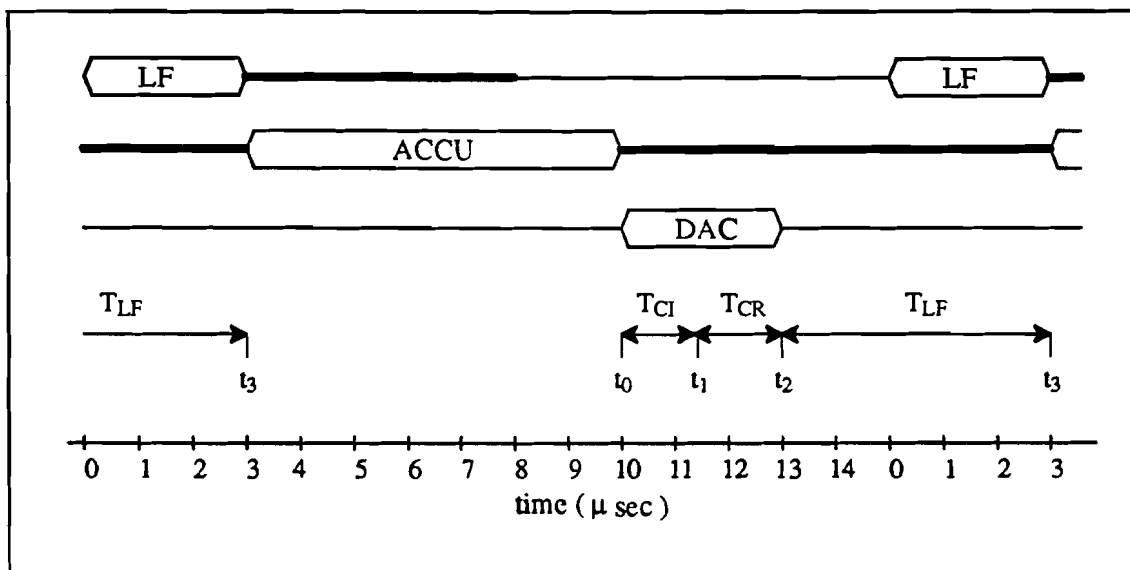
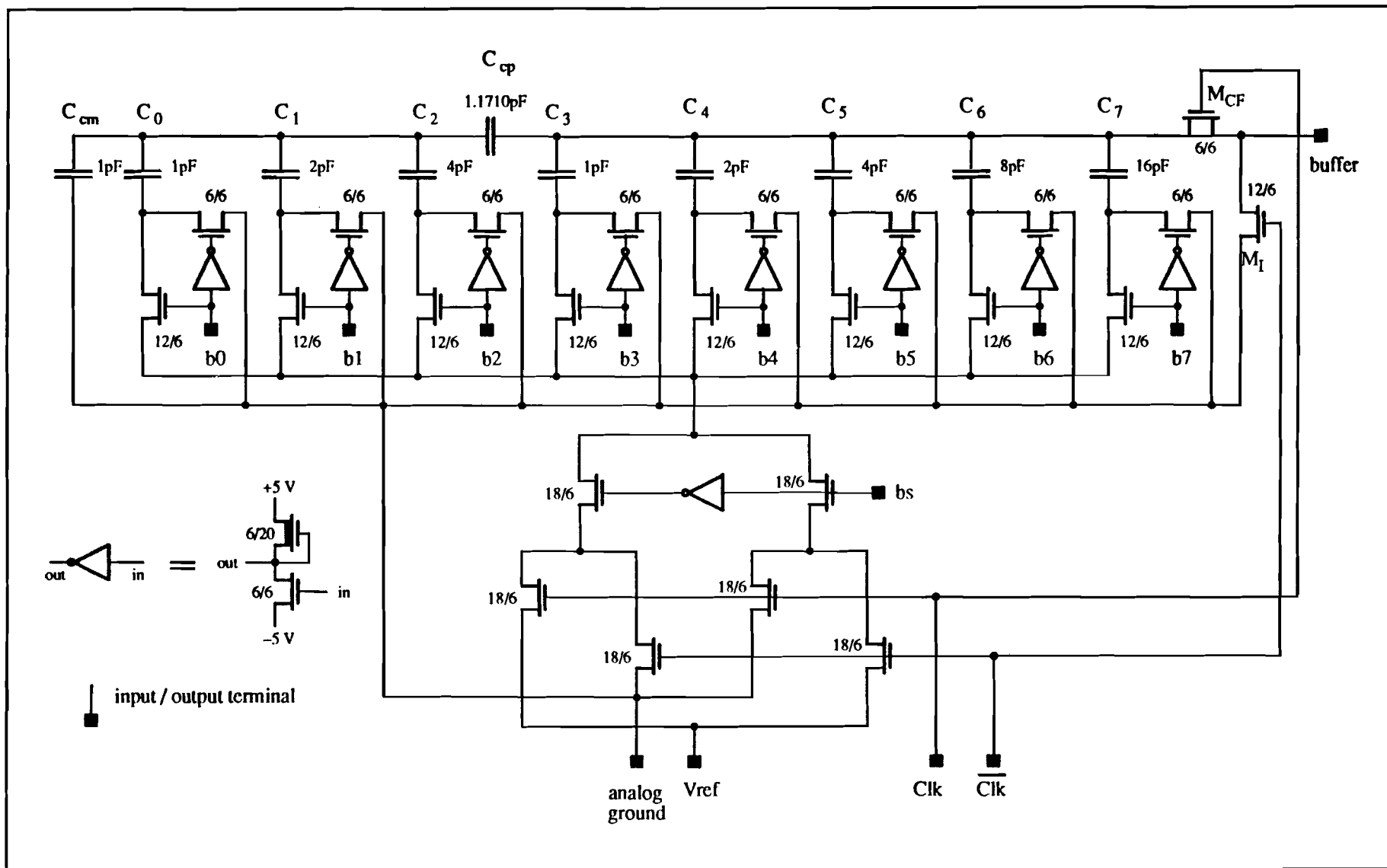


Figure 5.1 DAC-timing diagram

After the completion of the first phase all network capacitors either have zero charge (positive code) or a charge equal to $-b_i C_i V_{ref}$ (negative code). In both cases V_{out} must be zero at time t_1 . At the end of the conversion, time t_2 , the DAC's output voltage must have reached its final correct binary weighted value. This voltage must remain unchanged during at least the next T_{LF} seconds, the loop-filter active time (time t_2 to t_3). For this implementation it is dictated that the input word \underline{b} and sign-bit b_s remain the same from time t_0 to t_3 . Hence the accumulator must incorporate some memory device to hold these bit-values. Prior to time t_0 and after time t_3 the actual output voltage of the DAC is not important because it is not longer required.

In figure 5.2 the logic circuitry and analog switches are shown. Except for the capacitor array the same circuit applies for DAC26. Complements non- \underline{b} and non- b_s are generated in the DAC's logic circuitry. In fact this is one of the only two functions of that module. The other function is given later in this paragraph. The chosen switch arrangement performs the bulk of the required logic operations.

Figure 5.2 Analog switches and logic circuitry DAC25



As can be seen in figure 5.2 only one external clock signal and its complement are required to control the DAC switching. The different switching order for positive and negative input words (sign-bit b_i respectively 'high' and 'low') is accomplished by connecting the capacitors to V_{ref} only when b_i and Clk are low (positive words) or b_i and Clk are high (negative words), a EXCLUSIVE-OR operation. Transistor M_{CF} is added to compensate the offset voltage which results from clock feedthrough in transistor M_i .

Signal non-Clk governs the charge initiation phase, hence non-Clk must be 'high' from time t_0 to time t_1 , and 'low' from time t_1 to time t_2 . So automatically signal Clk, which controls the charge redistribution phase, is 'high' and must stay 'high' from time t_1 to time t_3 . To ensure correct operation clock signals Clk and non-Clk must be non-overlapping. The binary value of these signals before time t_0 and after time t_3 is, as was noted earlier, not important. The circuit complexity needed to generate Clk and non-Clk from signals supplied by the central controller is the dominating limiting factor here. Simple circuit layout is the aim. A realization with four gates is shown in figure 5.3, the second part of the DAC's logic circuit.

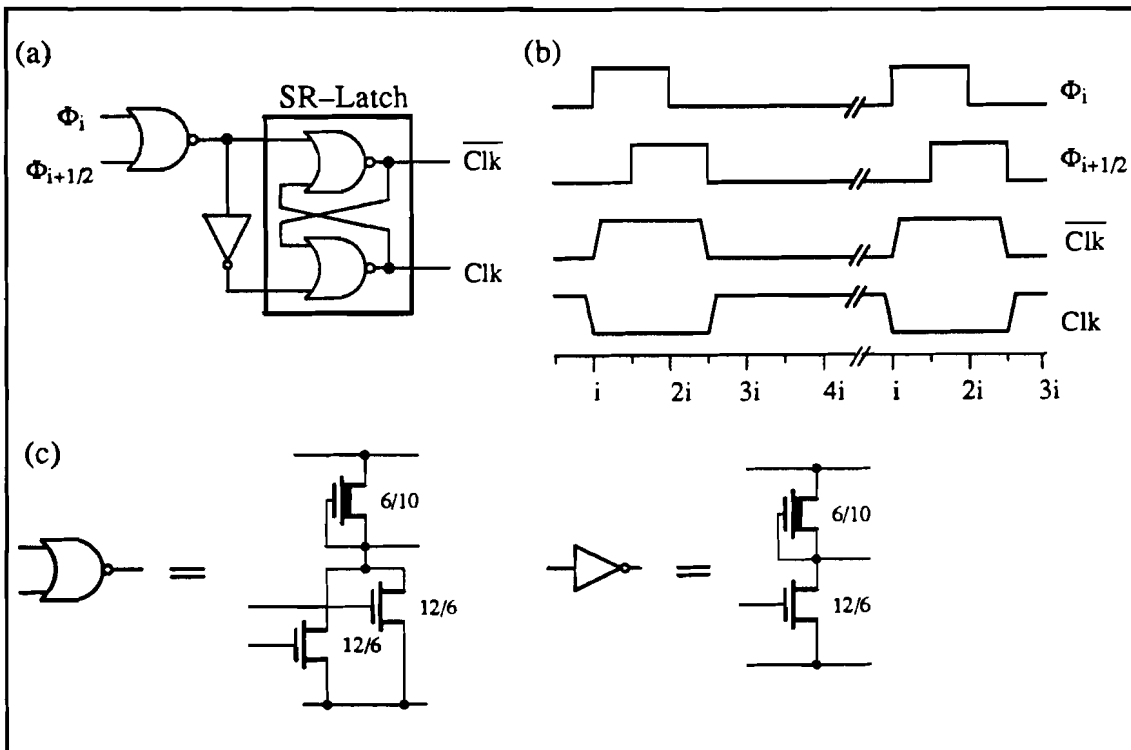


Figure 5.3 Local DAC clock generator; (a) Circuit; (b) timing diagram; (c) gates.

Signals Φ_i and $\Phi_{i+1/2}$ are provided by the central controller (for more details see part III of this report). Non-overlapping of Clk and non-Clk is ensured by the use of two NOR gates in the SET-RESET latch.

5.2 TRANSIENT RESPONSE DAC

In this paragraph the transient response of the complete digital-to-analog converter is determined using the circuit simulator SPICE. Included are logic circuitry (Fig. 5.3), analog switches (Fig. 5.2) and the opamp, loaded by 4pF (Fig. 4.2). Neglecting for the moment the transient characteristics of the opamp, the 'speed' of the DAC is primarily

ruled by the size of network capacitors and the W/L-ratio of the switches. Appendix D gives the SPICE circuit description.

The maximum capacitor values in DAC25 and DAC26 are respectively 16 pF and 12.8 pF. In paragraph 2.4, where the conversion speed was calculated for a DAC with 128 pF as largest capacitance value, a conversion time of 0.43 μ sec was found. The W/L-ratio of the switch was equal to one. As can be noticed in figure 5.2, now a serial combination of three switches is used to connect a capacitor to V_{ref} or ground. Effectively reducing the W/L-ratio to approximately one-third of the value of an individual switch. However, when regarding the reduction in maximum capacitance (with a factor eight), a conversion time in the order of $0.43\mu\text{sec} \times 3/8 = 160 \text{ nsec}$ can be anticipated. In the SPICE simulations it was found that the above conversion time is a too low estimate. In view of the resolution of the DAC, the error in the final output voltage must be smaller than 0.2%. This takes more time than found in the simple calculation in paragraph 2.4. Also allowance must be made for the non-ideal transient behavior of the buffer. So the (W/L)-ratio's of several transistors are increased to fulfill the conversion time requirement.

In SPICE simulations of DAC25 and DAC26, several transient parameters have been determined. Six different positive and negative input words are used; five with one bit 'high' (the five MSB's), and one with all bits 'low'. Clock signals Clk and non-Clk are pulse trains, alternatively 1.5 μ sec 'high' and 1.5 μ sec 'low'. Initially sign-bit b_s is 'low' and changes to 'high' after 18 μ sec.

The output voltage of the DAC is represented in figures 5.4 and 5.5, expanded views of these graphs are used to compute:

- propagation delay times t_{PHL} and t_{PLH}
- rise- and fall-time t_{THL} and t_{TLH}
- steady state output voltages V_{out} just before a transition

The characteristic transient times are given by the 10% and 90% points of the total voltage transition. In table IV the maximum observed values are given. Furthermore, the twelve steady state output voltages are used to determine V_{dac} and V_{odac} , with the help of equations [2.5] and [2.6]. Next the difference

$$V_{out} - (G_s V_{dac} + V_{odac})$$

is calculated, the error in the output voltage with respect to the interpolated theoretical value, table V summarizes the results.

The following conclusions can be drawn from the graph and tables;

- 1) The transient times are short, $t_p + 1/2t_r < 280 \text{ nsec}$
- 2) In the case of DAC25 the error is too large, max. approximately $0.70 \times V_{dac}$. For DAC26 the error is small enough.
- 3) V_{dac} is somewhat smaller then the values given in chapter 3.
- 4) V_{odac} is very small ($< 0.1V_{dac}$).
- 5) Switching spikes occur at every transition

Regarding conclusion 2), 3 μ sec is not sufficient time to perform the conversion in the case of DAC25. This is caused by the large capacitor values in combination with the on-resistance of the switches, time-constants $R_{on}C_i$ are too large compared to the conversion time. Also the increasing DC-gain of the opamp with increasing input voltage, contributes. This error must be added to the other errors present in the DAC. Therefor the yield will be somewhat smaller then the values presented in chapter 3. In the case of DAC26, employing smaller capacitor values, the error is only $0.25 \times V_{dac}$.

Looking at the SADM timing diagram, the conversion time can easily be lengthened to 4 μ sec, as was already proposed by Kooijman (Ref. [11]). With this choice there is still, if required, some freedom in the timing termination of other subcircuits. Increasing the W/L-ratios of the switches is a further improvement that could be used to increase speed. But the slew-rate limitations of the opamp will probably obstruct any further advancement in this area.

Regarding point 3), the slight decrease in LSB voltage is caused by the input capacitance of the opamp and parasitic capacitances of transistors M_i and M_{cf} .

The sum of clock feedthrough and opamp's offset voltages, results in an insignificant total offset value. The switching spikes normally occur at timing points, where the output voltage of the DAC is not required by the loop-filter, their presence is thus harmless.

Table IV Transient times

DAC version	DAC25	DAC26	
t_{PHL}	100	100	nsec
t_{PLH}	140	130	nsec
t_{THL}	160	160	nsec
t_{TLH}	280	210	nsec

Table V Simulation results

input word									decimal	output voltage (mV)		error (mV)	
b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	value	DAC25	DAC26	DAC25	DAC26
0	0	0	0	0	0	0	0	0	+ 0	-0.25	-0.17	-1.0	-0.3
0	0	0	0	1	0	0	0	0	+ 8	+61.52	+61.43	-0.6	-0.2
0	0	0	0	0	1	0	0	0	+ 16	+123.2	+123.0	-0.3	-0.2
0	0	0	0	0	0	1	0	0	+ 32	+246.5	+246.2	+0.1	-0.0
0	0	0	0	0	0	0	1	0	+ 64	+492.8	+492.6	+0.8	+0.3
0	0	0	0	0	0	0	0	1	+128	+986.2	+985.5	+2.9	+1.1
1	0	0	0	0	0	0	0	0	- 0	-0.25	-0.17	-1.0	-0.3
1	0	0	0	1	0	0	0	0	- 8	-61.82	-61.81	-1.1	-0.4
1	0	0	0	0	1	0	0	0	- 16	-123.5	-123.4	-1.4	-0.5
1	0	0	0	0	0	1	0	0	- 32	-246.9	-246.6	-1.9	-0.7
1	0	0	0	0	0	0	1	0	- 64	-493.6	-493.0	-3.0	-1.0
1	0	0	0	0	0	0	0	1	-128	-976.5	-982.2	+5.4	+1.9
V_{dac}										7.677	7.690	mVolt	
V_{odac}										0.695	0.141	mVolt	

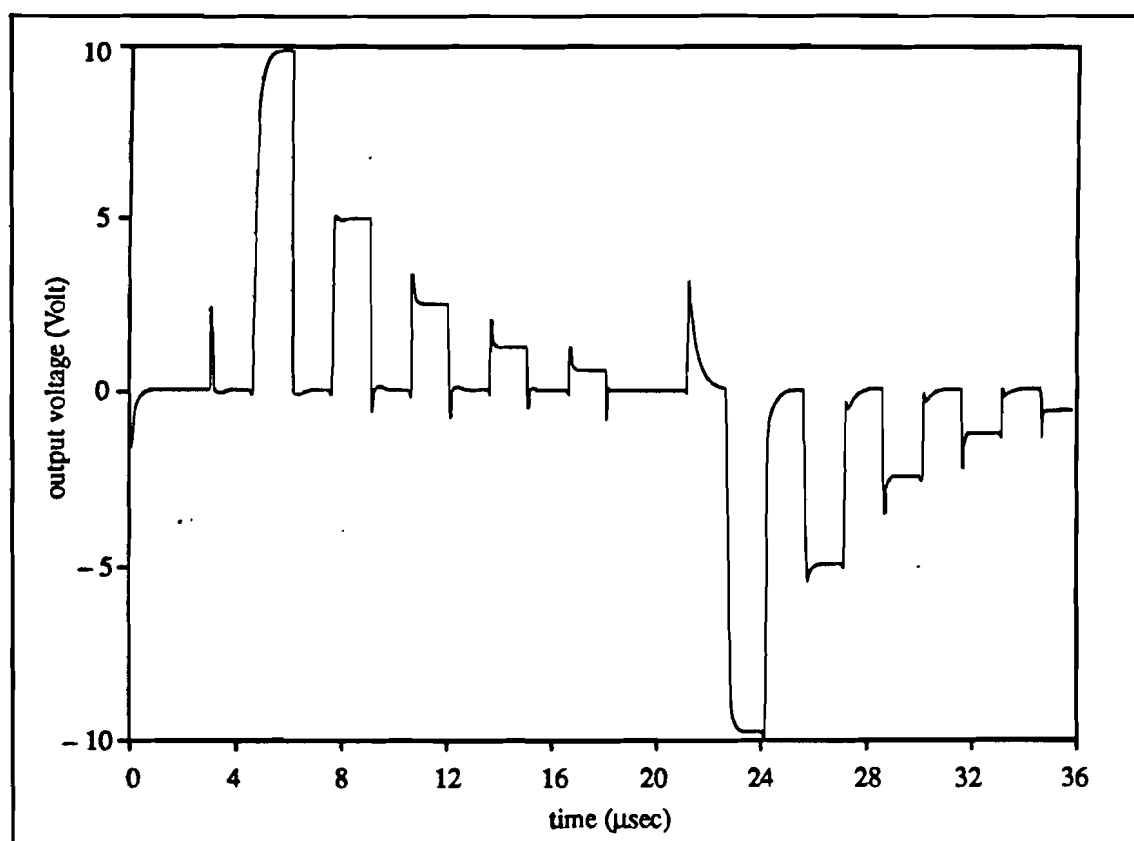


Figure 5.4 Transient response DAC25; output voltage.

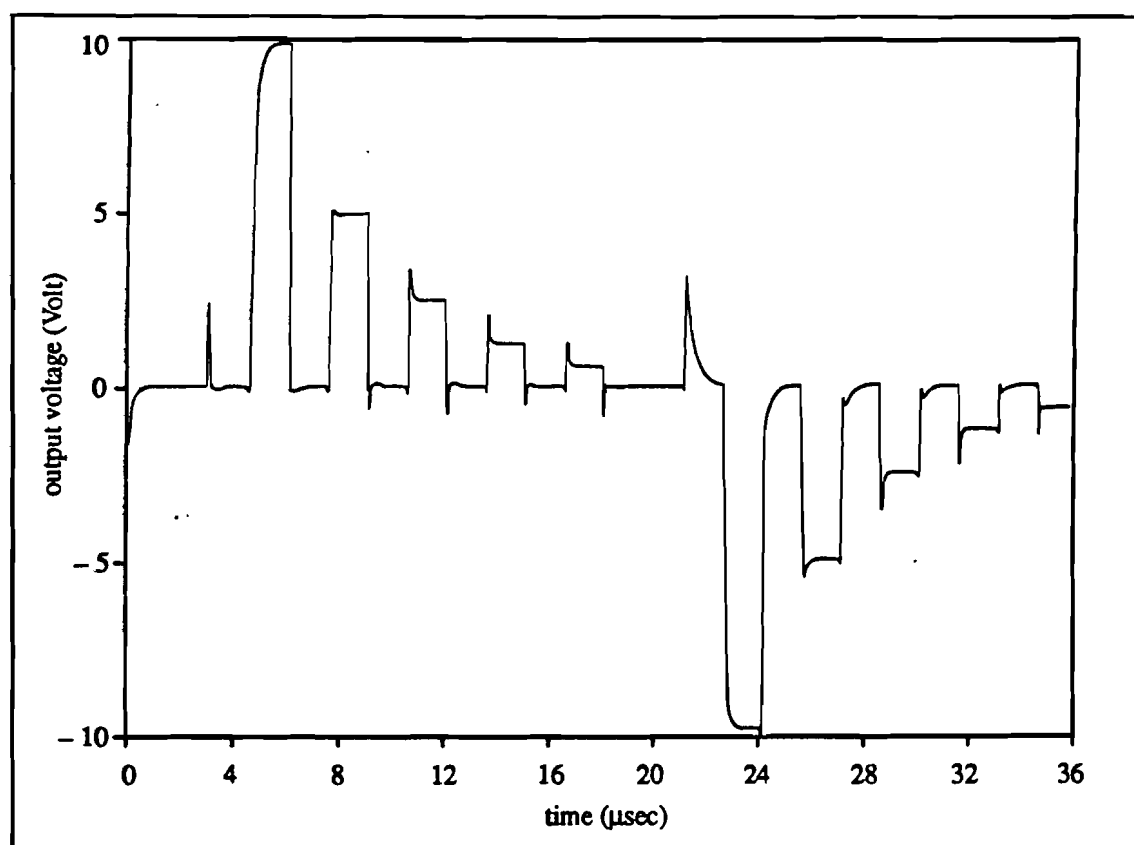


Figure 5.5 Transient response DAC26; output voltage.

These last simulations conclude the digital-to-analog converter design. There is however one important point which emerged when the DAC design was almost finished. Until now it was assumed that the input to the DAC was a sign-and-magnitude code. But as the accumulator operates with a 2-complement code, an additional interface between DAC and ACCU is necessary. This interface can be incorporated in the logical module of the DAC or as part of the output stage of the ACCU. The last option was initially chosen, requiring supplementary, rather large, chip area. As the design of the DAC and ACCU was done in the same time period, it was not until the end that a far more efficient solution was found. Some small alterations in the switch arrangement of the DAC (four extra transistors), and one extra network capacitor, also accomplish the desired interface function. This new circuit arrangement is illustrated in figure 5.6.

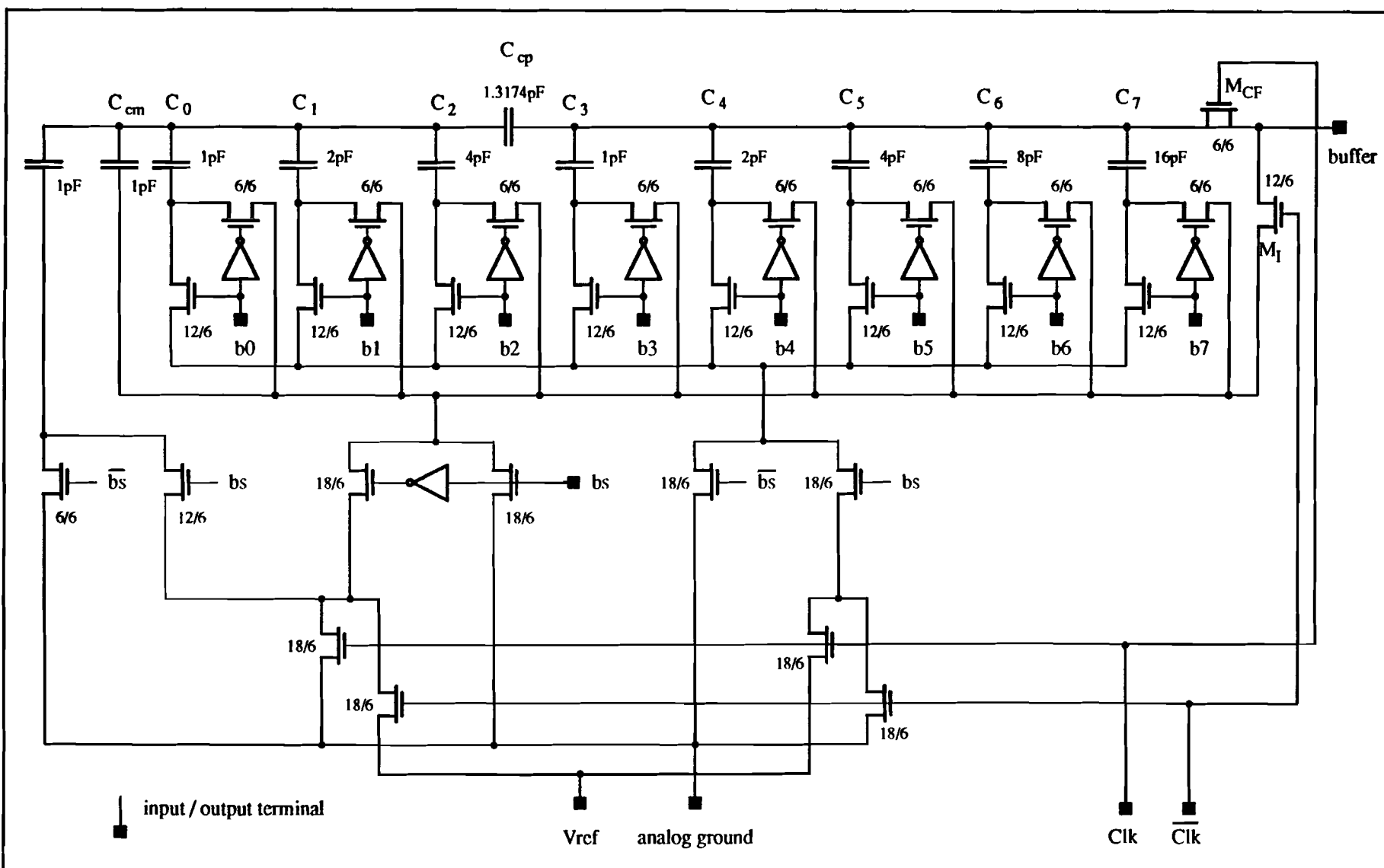
The interface function is only required if the input word is negative, hence when b_i is 'high'. Part of the translation is done by the addition of one LSB, requiring an additional capacitor with value $1 \times C_u$ in the first stage. In doing so, the binary word minus one LSB must be translated, a simple inversion of that binary word, e.g.

2-complement word	minus one LSB	inverted = sign-and-magnitude word
1 1 0 1 0 1 1 0	1 1 0 1 0 1 0 1	0 0 1 0 1 0 1 0

Because of the great resemblance between the original DAC circuit and figure 5.6, no extra simulations were performed. The accuracy is not seriously effected, as this is dependent on the network capacitor arrangement and capacitor dimensions. The additional capacitor only has a binary weight of one LSB. The transient response will also be the same, as the number of serial connected switches, used to connect a capacitor to ground or V_{ref} , isn't enlarged. Some minor changes in capacitor values will accommodate for the extra capacitor. Changing capacitor value C_{cm1} from $1 \times C_u$ to $2 \times C_u$ in equations [3.11] and [3.12], gives the correct values for coupling- and parasitic capacitors in the new DAC.

Due to an computer hard-disk crash, the layout files of the DAC are no longer available. But as the layout of the opamp already is created, the layout editing of the switches is straightforward, and with the help of the figures in paragraph 3.6, a layout should not be that hard to produce.

Figure 5.6 Circuit diagram DAC25, 2-complement input



CHAPTER 6 CONCLUSIONS DAC DESIGN

The designed digital-to-analog converter, based upon charge redistribution, and realized with a parallel capacitor array, demonstrated that a highly accurate DAC is easily achievable. This high accuracy is gained at the expense of chip area. DAC versions which use less chip area, are more susceptible to random error induced inaccuracies.

Furthermore, the notion that the same converters are used in modulator and demodulator, proved most valuable. Firstly this observation made it possible to largely delete gain related faults as error sources. The gain error is not longer measured in absolute terms, but as a ratio error expressed in dB. Interpolated, utilizing linear regression methods, gain and offset values are employed. As is indicated by the worst case analysis, this is a necessity if size reduction has to be achieved. Secondly, the functional demands placed upon opamp are relaxed by the above notion. Large variations in open-loop gain and common mode rejection ratio's, for instance caused by temperature differences in modulator and demodulator, can be tolerated.

Size reduction originates from a division of the capacitor array into two or more stages. The finally chosen capacitor arrangement is a compromise between required chip area, timing demands and accuracy. Two version are selected, both 2-stage, one with a total capacitance of 40 pF (DAC25), the other (DAC26) requiring a total capacitance of 29 pF. The probability that the transfer function of these DAC versions deviates not more than half the LSB-value from a interpolated straight line, is 83% and 71% respectively.

SPICE simulations of the complete digital-to-analog converter show that when nominal capacitor values are taken, the supporting elements (logic circuitry and opamp) do not seriously effect performance. DAC26 is fast enough to perform its task in the given time. If measurements reveal that the somewhat critical timing for DAC25 and limited accuracy of DAC26 present a problem, the conversion time can be lengthened with 1 to 2 μ sec and DAC25 must be applied as analog-to-digital converter.

Points for further research are measurment of matching properties and parasitic capacitance of NMOS capacitors fabricated with the EFFIC NMOS process. The results could be used to develop a theoretical model supporting the design of capacitor arrays with certain constraints (accuracy, size, application). In this report the DAC versions compared are only a very small selection from the large total of possible multi-stage capacitor network arrangements.

PART III CENTRAL CONTROLLER

CHAPTER 1 INTRODUCTION

1.1 CONTROLLER CONCEPT

To interface the timing termination of individual functional subcircuits in the SADM with each other, a central control unit is necessary. The control unit provides signals which activate the subcircuits at the right time and in the correct order. Also it supplies clock signals with a smaller time resolution. These can be used in combination with the former courser clock signals to generate specific user-defined signals. Here the controller is split in two parts, a global basic part and separate local controllers, located close to each subcircuit. In this chapter the global controller is described. Local controllers are regarded as part of a specific subcircuit. In figure 1.1 the above outlined controller concept is illustrated.

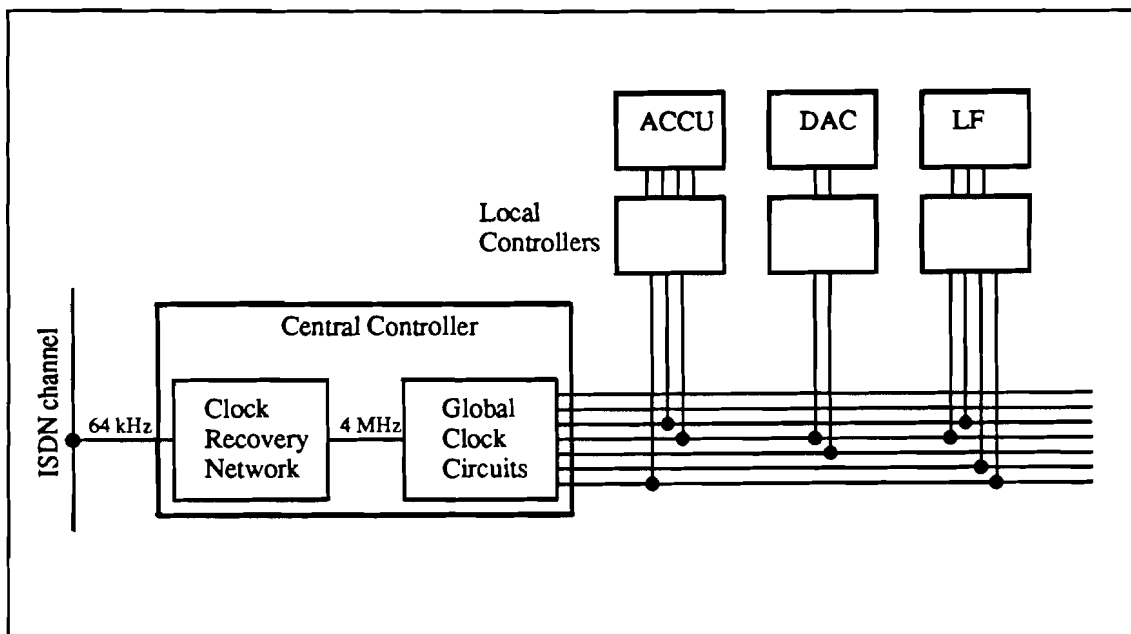


Figure 1.1 Controller concept

The division in separate parts is mainly done for flexibility, subsequent altering of the timing termination of a subcircuit can now more easily be implemented. Secondly, it is done to minimize power dissipation and to save chip area. In general long interconnections are needed to connect the controller to a subcircuit, with resulting large parasitic capacitances. The output stages of the controller must provide driving capability to ensure sharp clock signal edges. If all required clock signals are generated in the central controller a large number of buffers would be necessary. This is circumvented if only basic clock signals are generated in the central controller. The local controllers can then be realized with low-power, smaller area, gate circuits.

As master clock a 4,096 MHz signal, generated in the clock recovery network, is used. Reference [8] provides a detailed description of that circuit. It's main purpose is to lock on the 64 kHz AMI code present in the ISDN channel, and to synchronize the master

clock with that signal. Some modifications have to be performed in the clock recovery circuit as it was intentionally designed for a 2 MHz master clock frequency and with an old SPICE NMOS parameter set.

1.2 REQUIRED CLOCK SIGNALS

To determine the basic required controller output signals, a common divider has to be found in all clock signals needed to control the SADM. The basic SADM cycle has a repetition rate of 64,000 kHz. Thus in a period of 15,625 μsec one complete conversion has to take place. First the position, in that basic period, of each subcircuit active interval is determined. Next the smallest required pulse duration is derived.

The timing diagram given in the introduction to the SADM system in part I, is repeated in figure 1.2. It illustrates the active- and data hold intervals of all subcircuits in one SADM cycle. This cycle is divided into 15 equally long intervals of 1.0417 μsec . For convenience this value is rounded to 1 μsec *). All SADM modules start and are active during integer multiples of 1 μsec .

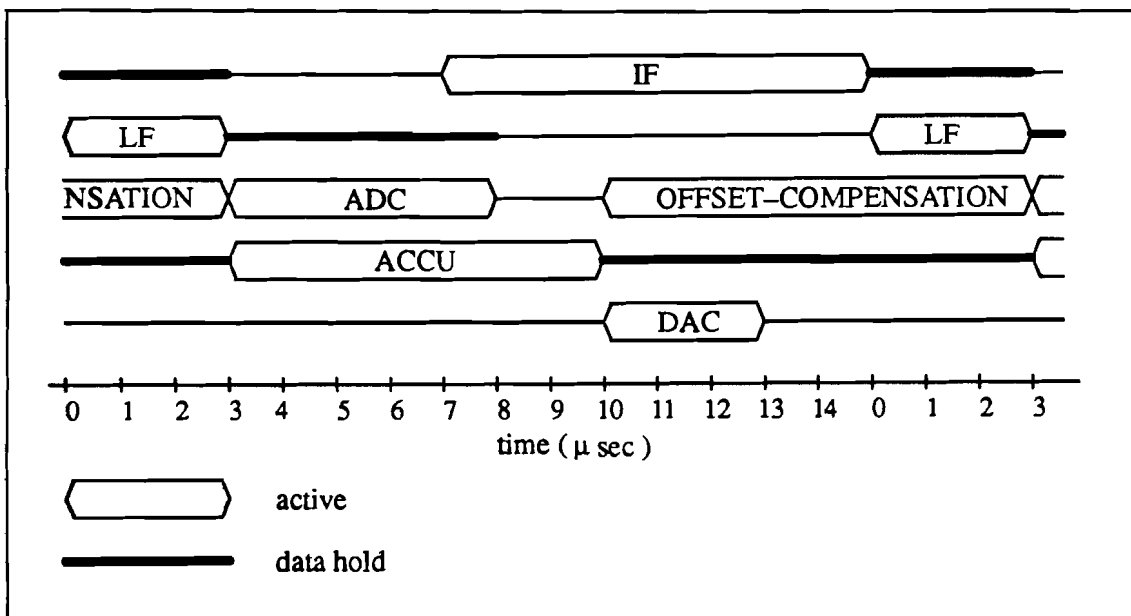


Figure 1.2 SADM timing diagram

So a fundamental part of the controller is a 15-phase clock circuit, which provides 15 outputs that are successively 'high' for 1 μsec , and 'low' for 14 μsec . A 15-bit cyclic shift register, where a 'one' is circulated, will perform this function. The fifteen outputs phases are named, $\Phi_0, \Phi_1, \dots, \Phi_{14}$. The index refers to the low-high transition point of a phase in the fundamental SADM cycle. A realization of this circuit is given in figure 1.3. This circuit has the advantage that besides the fifteen wanted phases Φ_i , the inverse $\bar{\Phi}_i$ is present, and also 15 signals shifted by 1/2 μsec , $\Phi_{i+1/2}$ and $\bar{\Phi}_{i+1/2}$. Signals $\Phi_{i+1/2}$ can be used to break up the 1 μsec pattern in a 1/2 μsec grid, for instance required to control the DAC switching. To control the shifting operation a 2-phase clock with 2.048 MHz frequency is necessary. But this also could be realized with two phases of the existing 2.048 MHz 4-phase clock.

*) Whenever in this report a reference is made to an absolute time period, that value must be multiplied with 1.0417.

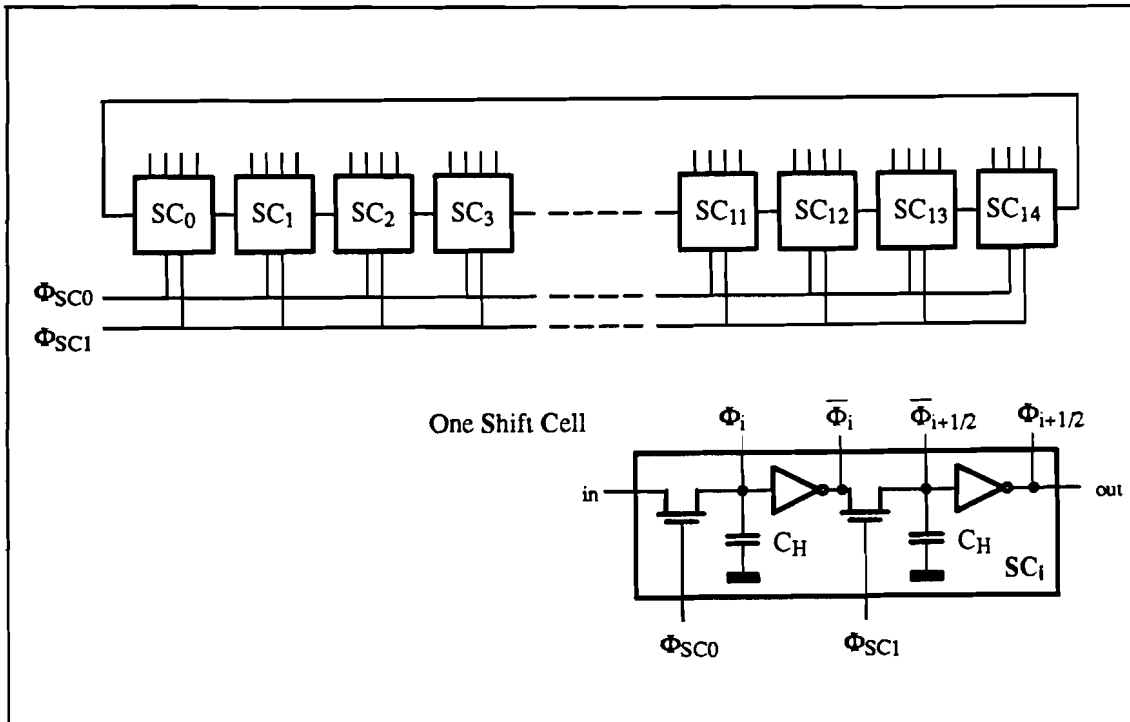


Figure 1.3 15-bit shift register

For the accumulator and analog-to-digital converter the $1/2 \mu\text{sec}$ pattern is too coarse. They require signals with smaller time resolution. These are supplied by two four-phase clock circuits, with frequencies of 1.024 and 2.048 MHz respectively. The pulse lengths are 250 and 125 nsec, and the four phases must be non-overlapping.

Using relative simple standard combinatorial logic and regenerative logic circuits (e.g. Flip-Flops, Latches), now any signal can be generated with transitions at integer multiples of 125 nsec. Thus the combination of 15-bit shift register and two 4-phase clocks, provides 68 different clock signals, more than adequate to control the SADM timing.

1.3 CONTROLLER CIRCUITS

In reference [7], the major part of the controller design is already implemented. Further investigation revealed that the 4-phase clock circuit given in that reference, is unsuitable for both the 1 MHz and 2 MHz application. This is mainly due to the inability to drive capacitive loads of more than 1 pF, over the full voltage range (10 Volt transition), with adequate (short) transient times. In general we wish to design circuits that can be loaded with a capacitance of 2 pF. This value is approximately equal to either (Ref. [11]):

- the input capacitance of 110 MOS transistors with $W/L = 6\mu\text{m}/6\mu\text{m}$
- the parasitic capacitance of approximately $1000\mu\text{m} \times 6\mu\text{m}$ aluminum interconnect

The high load value originates from the chosen controller concept. The controller is placed in a central position on the chip, bonds to subcircuits will be long.

An earlier design of a 4-phase clock is given in reference [4], where the 4-phase clock is realized with a minimum number of gates. This design proved more valuable, with some alterations in gate structure, a high capacitive load of 2 pF per phase presents no problem. Figure 1.4 shows the circuit diagram, yielding four 4-phase signals with pulse

lengths of 125 nsec and repetition rates of 2 MHz, designated as Φ_{F20} , Φ_{F21} , Φ_{F22} and Φ_{F23} . The lower part of the circuit is a special variant of a cyclic shift register, it provides two 2 MHz signals shifted by 125 nsec, and the inverse of these signals. This is sufficient to encode the four different output states. 3-input NOR's are employed in the output stage, the third input is necessary to ensure non-overlapping. The two hold-capacitors, C_H , are not physical required, the input capacitance of the inverters performs the holding function.

The circuit needs non-overlapping 4 MHz 2-phase signals (Φ_{T40} and Φ_{T41}) to control the shifting operation. These clock signals are derived directly from the master clock signal (Φ_{MC}); requiring one inverter and a SR-latch build with two NOR's, also shown in figure 1.4.

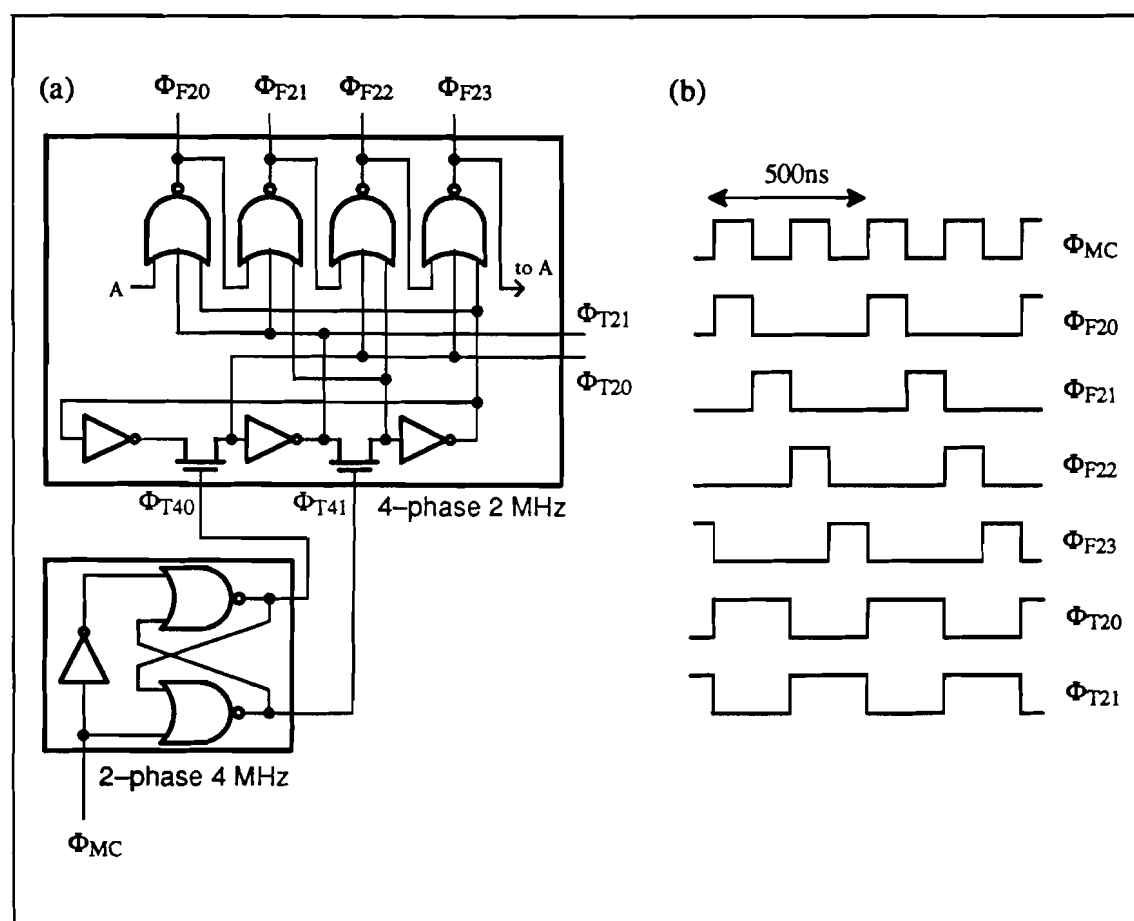


Figure 1.4 Circuit diagram 4-phase clock; (a) Circuit; (b) signals.

A nice feature of the above circuit is the presence of 2-phase signals with 2 MHz frequency, designated as Φ_{T20} and Φ_{T21} . These 2 MHz 2-phase signals are used to control the second required 4-phase clock. As Φ_{T20} and Φ_{T21} are overlapping, a repeater is necessary, this circuit is built with one NOR SR-latch. The circuit diagram of the second slower 4-phase clock is identical to that in figure 1.4. Here the four output signals are called Φ_{F10} , Φ_{F11} , Φ_{F12} and Φ_{F13} . Two outputs Φ_{F10} and Φ_{F12} are used to control the shift operation in the 15-bit shift register.

Figure 1.5 illustrates the complete controller, in figure 1.6 the timing diagram of the controller is shown.

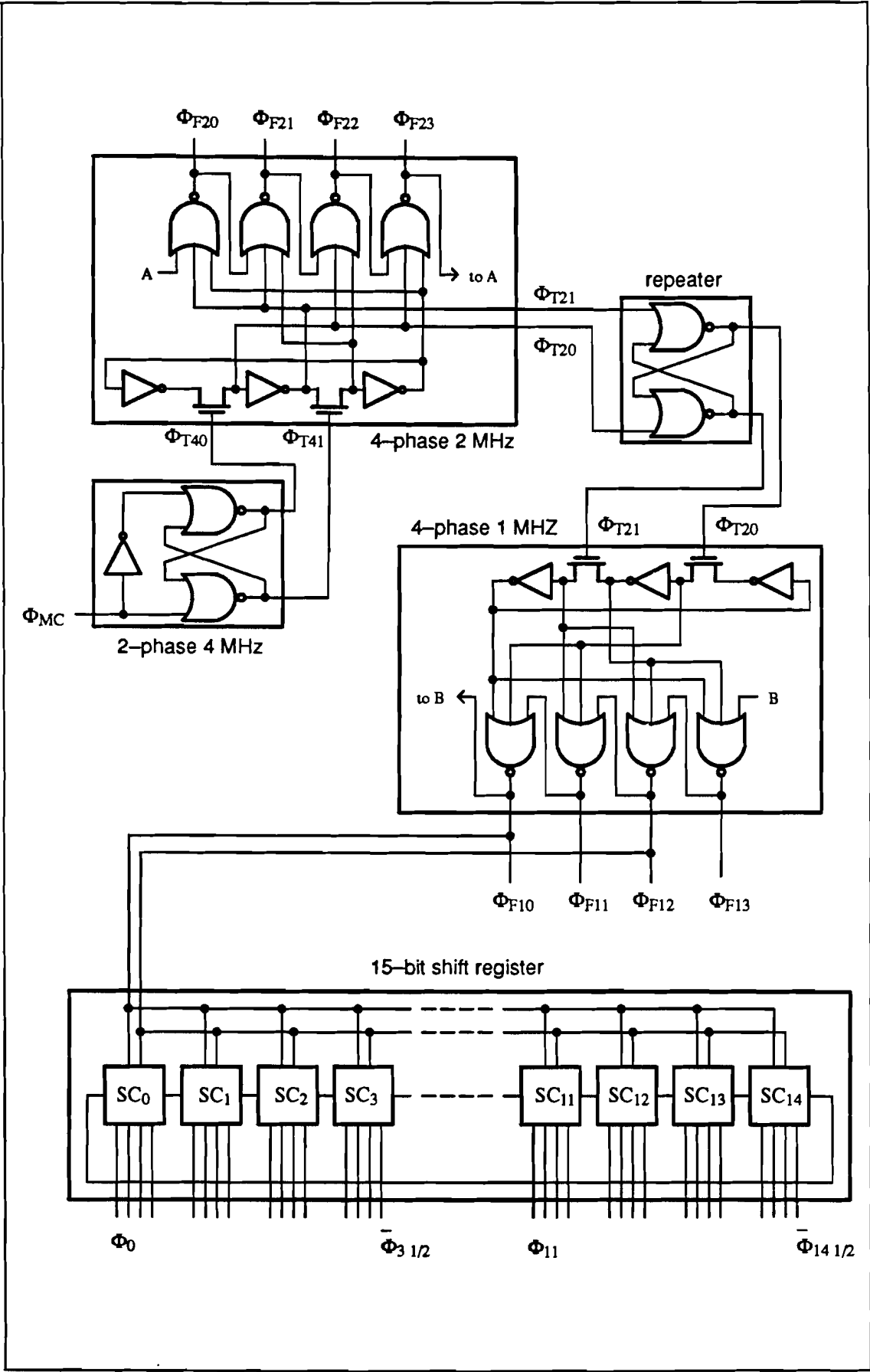


Figure 1.5 Controller

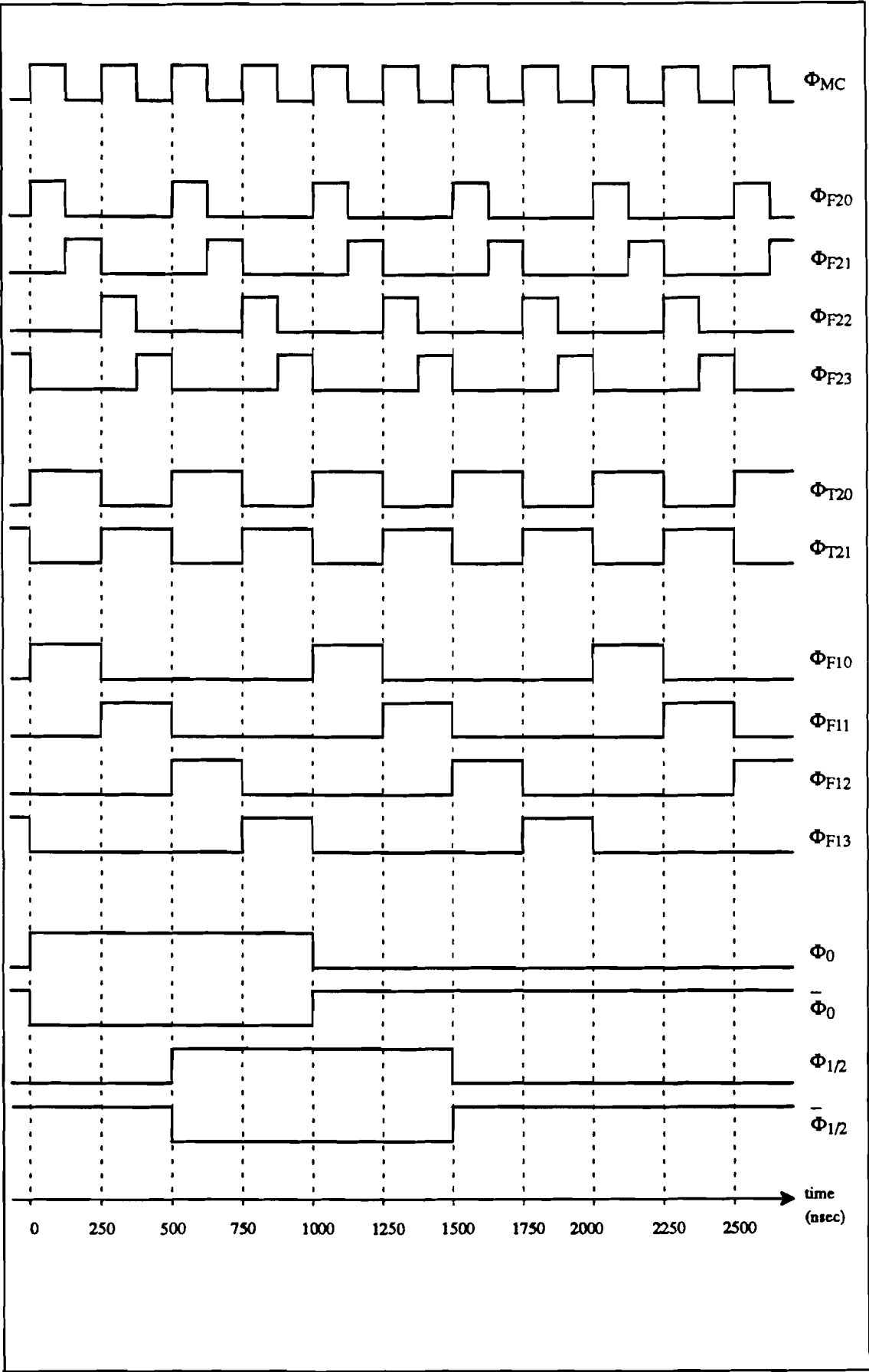


Figure 1.6 Timing diagram controller

A major concern in the above design is the synchronization of all clock signals, transitions must take place at approximately the same time. In the proposed controller this is accomplished firstly by the use of fast circuit devices. Secondly intermediate signals are used to control signal transitions and shifting operations. In figure 1.7 a schematic representation of the controller is given, portraying the delays present in the different circuit elements. As can be seen in the figure, the delay with respect to the 2 MHz 4-phase clock Φ_{F20} are: $\Delta A = \Delta 1 + \Delta 3 + \Delta 4$ (15-bit shift register output Φ_0) and $\Delta B = \Delta 1 + \Delta 3$ (1 MHz 4-phase clock, Φ_{F10}). $\Delta 1$, $\Delta 3$ and $\Delta 4$ must be as small as possible. The design of fast gate circuits, which fulfill these requirements, is the subject of the next chapter.

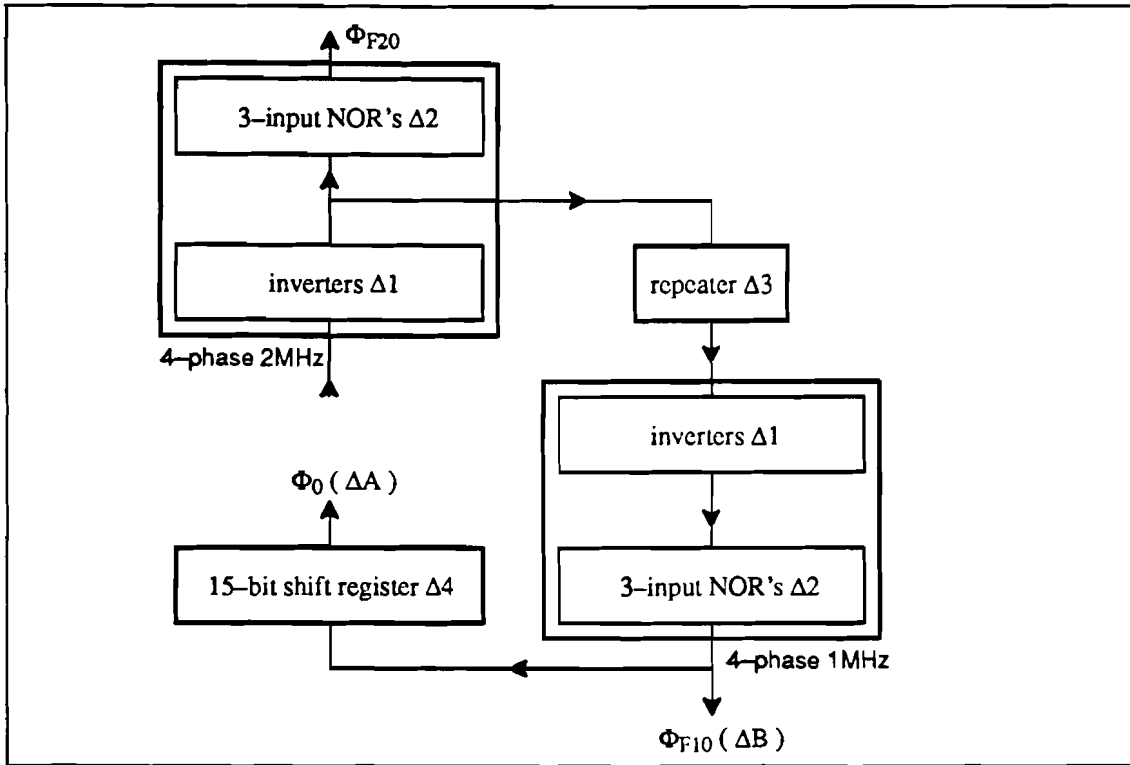


Figure 1.7 Schematic diagram controller; Delay elements.

CHAPTER 2 BOOTSTRAP GATE CIRCUITS

2.1 BASIC CIRCUIT ARRANGEMENT

In the controller all high power gates are variants of one basic circuit arrangement, illustrated in figure 2.1. In this figure a prototype inverter is shown, operation is based upon bootstrapping. Originally designed by Wieërs (Ref [4]), and further developed by Faasse (Ref. [7]), a novel application is introduced in this report. Both Wieërs and Faasse only used the circuit as high power buffer, they didn't recognize the full potential of the circuit; the standard inverter can easily be modified into high power NAND's and NOR's. These modifications will be analyzed in paragraph 2.2. Here the operation principle is explained and the inverter is compared to another buffer circuit.

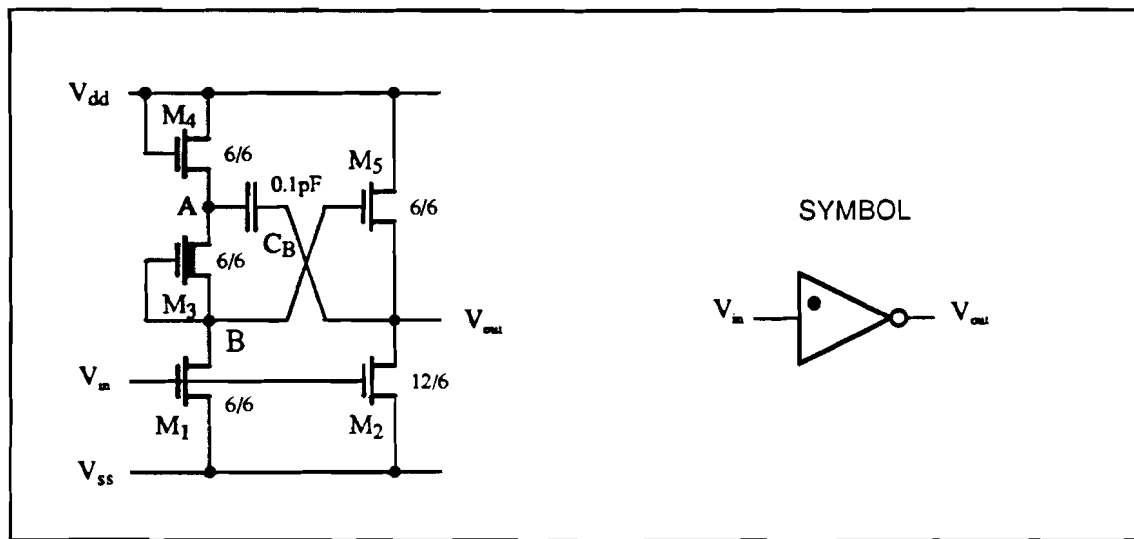


Figure 2.1 Prototype bootstrap inverter

In the prototype inverter, a voltage higher than the positive supply voltage is achieved, by means of a bootstrap capacitor. This voltage is applied to the gate of an output transistor, enabling very fast charging of large load capacitances. The operating principle will be explained with reference to Fig. 2.1.

Assume V_{in} is low and V_{out} is high. When V_{in} changes from low to high ($V_{in} = V_{DD}$), transistors M_1 and M_2 are conducting, with constant high gate-source voltage during the whole output voltage transition. Thus the load capacitor is rapidly discharged. After a short time period the voltage at point A is almost equal to the positive supply voltage minus the threshold voltage value of transistor M_4 ; transistor M_4 is open as long as $V_{gs4} = V_{DD} - V_{gs} > V_{TH4}$. In this static situation, the voltage at point B is slightly higher than the negative supply voltage, there is a small bias current flow. Consequently transistor M_3 is non-conducting ($V_{gs3} < V_{TH3}$) and the low-level, V_{OL} , of the output voltage is equal to the negative supply voltage V_{SS} . If any residual charge is present on the load capacitor, V_{out} is somewhat higher than V_{SS} , and M_2 is conducting, discharging the capacitor until $V_{out} = V_{SS}$.

When the input changes from high to low ($V_{in} = V_{SS}$), transistors M_1 and M_2 close. Due to the relative large value of bootstrap capacitor C_B as compared to parasitic transistor capacitances, the voltage across the bootstrap capacitor will remain unchanged. Via transistor M_3 this voltage is applied to the gate of M_5 . The output voltage will rise, but

with constant voltage across the bootstrap capacitor, so will the gate voltage of M_3 . Ultimately the voltage at point B, will rise to almost twice the positive supply voltage. Thus the gate-source voltage of M_3 will approximately stay the same during the whole output voltage transition. This mechanism ensures very fast charging of the load capacitor, preventing the commonly found slow rise times in conventional two-transistor inverters. Transistor M_3 remains conducting until V_{out} is equal to V_{DD} (then $V_{ds} = 0$). So the logical high-level of the output voltage, V_{OH} , is equal to V_{DD} .

The basic speed limitation of the above circuit, is caused by the gate capacitance of transistor M_3 and drain-gate capacitance of M_1 , in conjunction with the on-resistance of M_3 . Before M_3 becomes conducting, the gate-source voltage first has to reach the threshold voltage level. This will take some time, and C_B must supply a small load current. Hence the voltage across the bootstrap capacitor will initially decrease somewhat. But when the voltage at point A drops below $V_{DD}-V_{TH4}$, M_4 is conducting, providing a part of the load current and recharging the bootstrap capacitor.

To give an idea of the performance of the bootstrap inverter, it is compared with a second high power inverter, shown in figure 2.2. Here a normal inverter input stage is used to separate input and output. The performance of the input stage is now not affected by capacitive loads, this ensures fast rise- and fall-times of that stage. Assume first V_{in} is low and V_{out} is high. When V_{in} changes from low to high, the load capacitor is rapidly discharged by transistor M_4 (constantly high gate-source voltage). When V_{in} returns to its low state, the voltage at point A rises very fast to V_{DD} . Due to the presences of the load the output voltage will initially remain unchanged, the gate-source voltage of transistor M_3 has a high value. Thus M_3 will temporary supply a large load current, rapidly charging the load capacitance until $V_{out} = V_{DD}$.

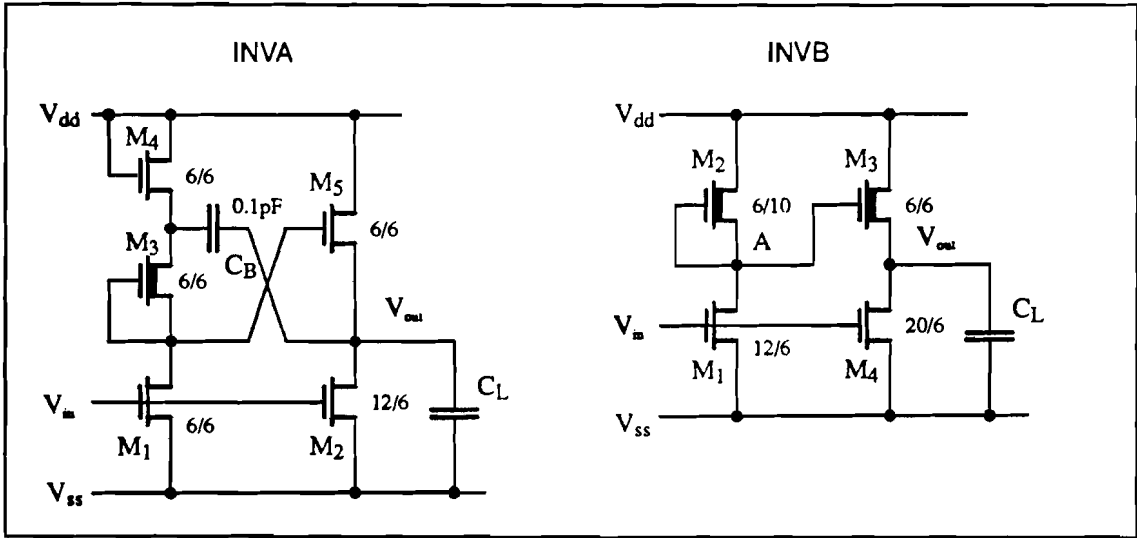


Figure 2.2 Circuit diagram high power inverters

Figure 2.2 presents the two inverters that are compared, they are denoted INVA and INVB. Width and length of individual transistors are, were possible, equal to the smallest surface dimension; $6\mu\text{m}$. The other's are optimized in several SPICE simulations, to obtain equal rise- and fall-times for the two circuits. The ratio of enhancement to depletion (W/L)-values for the 4-transistor inverter are chosen such that the logical low output voltage, V_{OL} , is comparable to that of INVA. Figure 2.3 shows the transient response of the two inverters, with no load and with $C_L=2\text{pF}$. Table I summarizes several characteristic features.

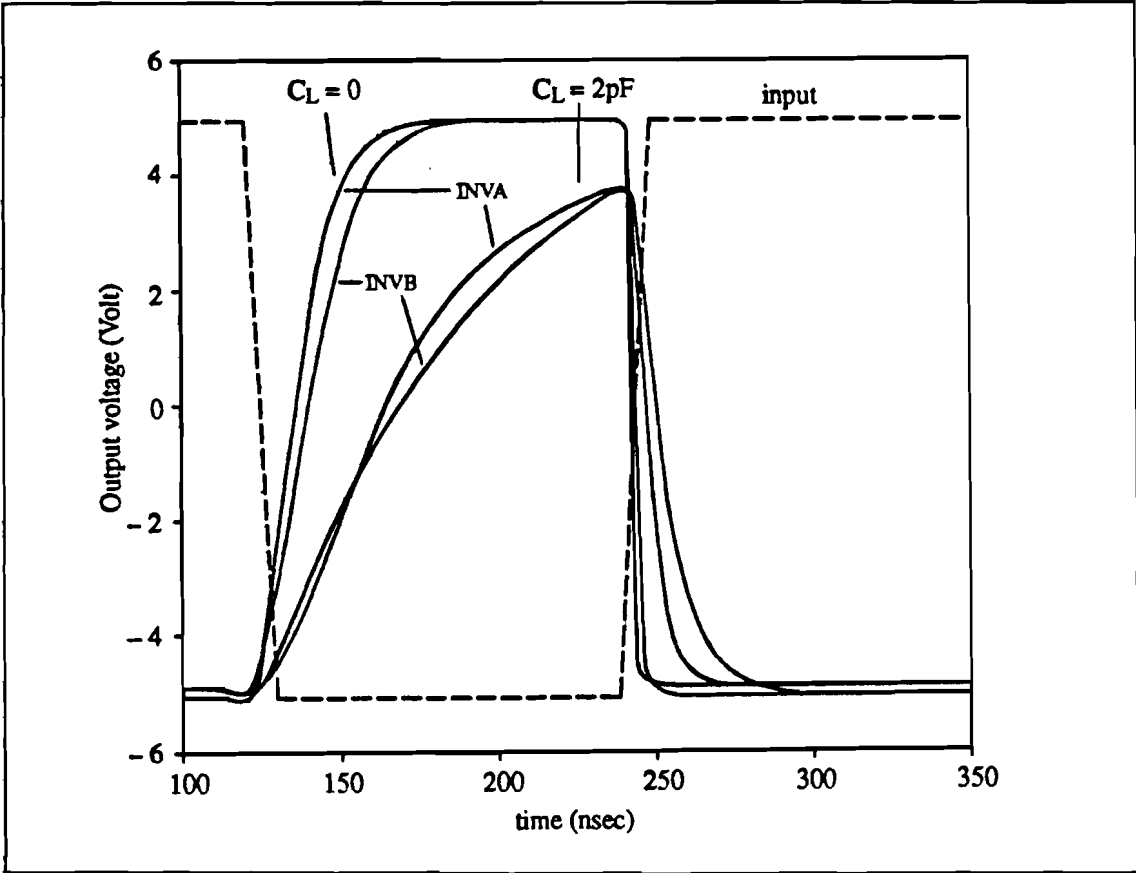


Figure 2.3 Transient response high power inverters

Table I High power Inverter features

load version	0.2 pF		0.6 pF		1.0 pF		2.0 pF		
	INVA	INVB	INVA	INVB	INVA	INVB	INVA	INVB	
rise time	25	32	50	52	72	72	–	–	nsec
fall time	6	4	11	6	15	10	23	14	nsec
$I_{S,mean}$	35	44	51	67	66	81	97	110	μA
$I_{S,top}$	310	390	450	580	550	715	580	900	μA
$I_{S,OL}$	42	81	μA	supply current when $V_{out}=V_{OL}$ (bias current)					
total size	430	290	μm^2	$\Sigma W_1 L_1 + W_{cap} L_{cap}$					
C_{IN}	55	97	fF	$C_{ox}[W_1 L_1 + W_2 L_2]$ where $C_{ox} = 5.04 \times 10^{-4} F/m^2$					

In the table we notice that for equal transient performance, the bootstrapped inverter is advantageous in almost all aspects. There is only one exception, it requires a larger chip area. This is caused by the large area occupied by the bootstrap capacitor. On the basis of the low input capacitance, the lower peak current and reduced power consumption, INVA is chosen as basic circuit element in the controller. It has ample drive to charge a 1 pF load in approximately 125 nsec to V_{OH} . Although the minimum pulse width is

125 nsec in the 4-phase clock, inverter INVA, is used in these circuits because of the reduced load requirements (input capacitance of one inverter and three gates).

2.2 GATE CIRCUITS

To modify the standard inverter into a high power 2- to 3-input NOR version, transistor M_1 and M_2 in figure 2.1 are replaced by a parallel combination 2 or 3 enhancement transistors, as is shown in figure 2.4. If such a NOR gate is used in the four-phase clock circuit, still higher power capability is required. In view of the short pulse width of 125 nsec and 250 nsec respectively, and the high capacitive load of 2 pF, circuit (b) in figure 2.4 is further developed in a version capable of satisfying the high speed/high load requirement.

The 2-input NOR version of figure 2.4 is used in the 2-phase clock and repeater, as they are only needed locally in the controller. Long interconnections can be avoided by careful layout editing. Also they merely have to drive small capacitances; 75 fF (2-phase clock: one NOR input, one switch) and again 75fF (repeater: one NOR input, one switch). The complete controller will be described in the next chapter. In this paragraph the (W/L)-ratio's and size of the bootstrap capacitor, for the 3-input NOR, are changed in order to obtain higher speed capability.

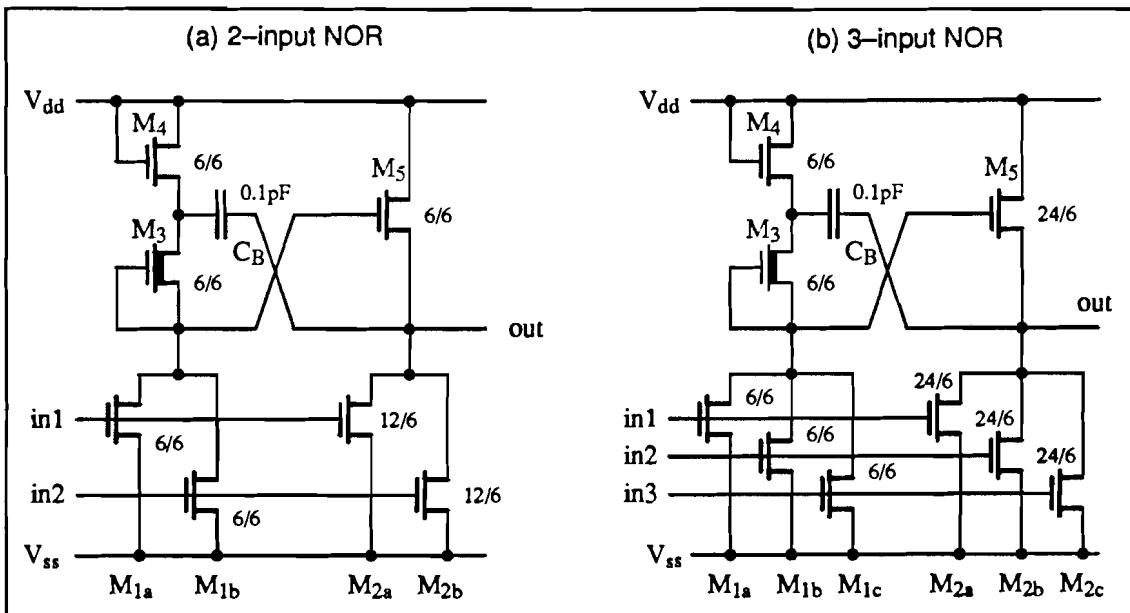


Figure 2.4 Power NOR's; (a) 2-input; (b) 3-input.

As initial parameter values those of the 3-input NOR in figure 2.4 are employed. As is shown later only one circuit element is changed seriously in value (C_B). The (W/L)-ratios don't change significantly. The input signal is an alternating pulse train 115 nsec high (+5 Volt) and 115 nsec low (-5 Volt). Rise- and fall-time are equal to 10 nsec (shorter times were not possible because of SPICE convergence problems). The NOR is loaded with 2 pF. Two inputs are connected to V_{ss} , hence the NOR operates as an inverter. In a total of six SPICE simulations the transient response is calculated. In one simulation run, the value of only one circuit element is altered. Each time five different values are taken, from the resulting graph the optimal or nearly optimal parameter values are determined. Figures 2.6 to 2.10 at the end of this paragraph present these graphs. Each time a simulation has ended the altered parameter is reset to the value given in figure 2.4(b) before the next simulation is started.

As can be seen in the figures the (W/L)-ratio of transistor M_1 , must be as small as possible, so here the minimum transistor size of $6\mu\text{m}\times 6\mu\text{m}$ is taken. The slower rise time for larger (W/L)-ratio is caused by the then also larger feedback capacitance between drain and gate of M_1 . Transistor M_2 is only important for the falling edge in the output transition, W/L values larger then 30/6 don't improve the transient response seriously. As it also determines the input capacitance of the NOR, a value of 30/6 is chosen for this transistor. The (W/L)-ratio of transistor M_3 is not effective if it rises above 10/6. Initially responsible for a fast rising edge, the curves for $W/L>10/6$ bend below that of $W/L=10/6$ after approximately 50 nsec. Secondly if $(W/L)_3$ is too large (compared to $(W/L)_1$ and $(W/L)_4$), transistor M_3 is conducting when V_{in} is high. Consequently $V_{OL} > V_{SS}$, a situation that has to be avoided. For this transistor a (W/L)-ratio of 10/6 is chosen. Transistor M_4 has no influence on the transient response, all curves are the same (tested: $W/L=6/6$ to $22/6$). So the minimum transistor size of $6\mu\text{m}\times 6\mu\text{m}$ is also appropriate here. The (W/L)-ratio of transistor M_5 is chosen as 30/6, larger values don't result in notable improvement of the rise time. Finally the value of the bootstrap capacitor is chosen. An increase from 0.1 pF to 0.3 pF gives a significant progression in the rise time. Larger values are not considered as they increase the required chip area to much and don't improve the rise time meaningful. Figure 2.5 illustrates the finally chosen 3-input NOR circuit arrangement, some important features of this gate are summarized in table II.

Table II Transient characteristics 3-input NOR

load	none	2 pF	3 pF	
rise time	13	38	45	nsec
fall time	5	11	15	nsec
prop. delay (LH)	12	23	27	nsec
prop. delay (HL)	0	5	6	nsec
<hr/>				
total area	1560 μm^2			
C_{in} per input	109 fF			

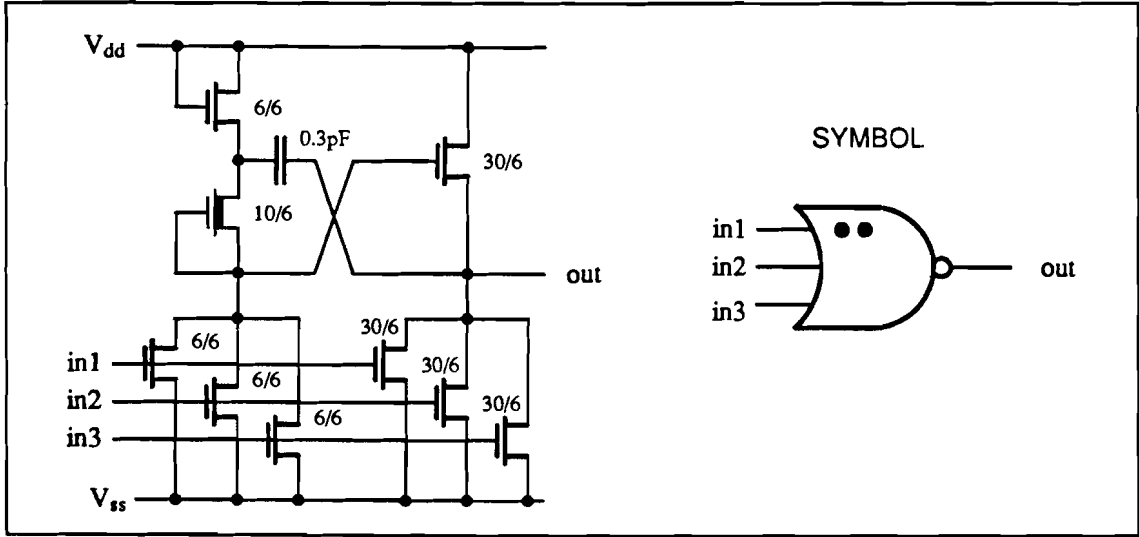


Figure 2.5 3-Input power NOR

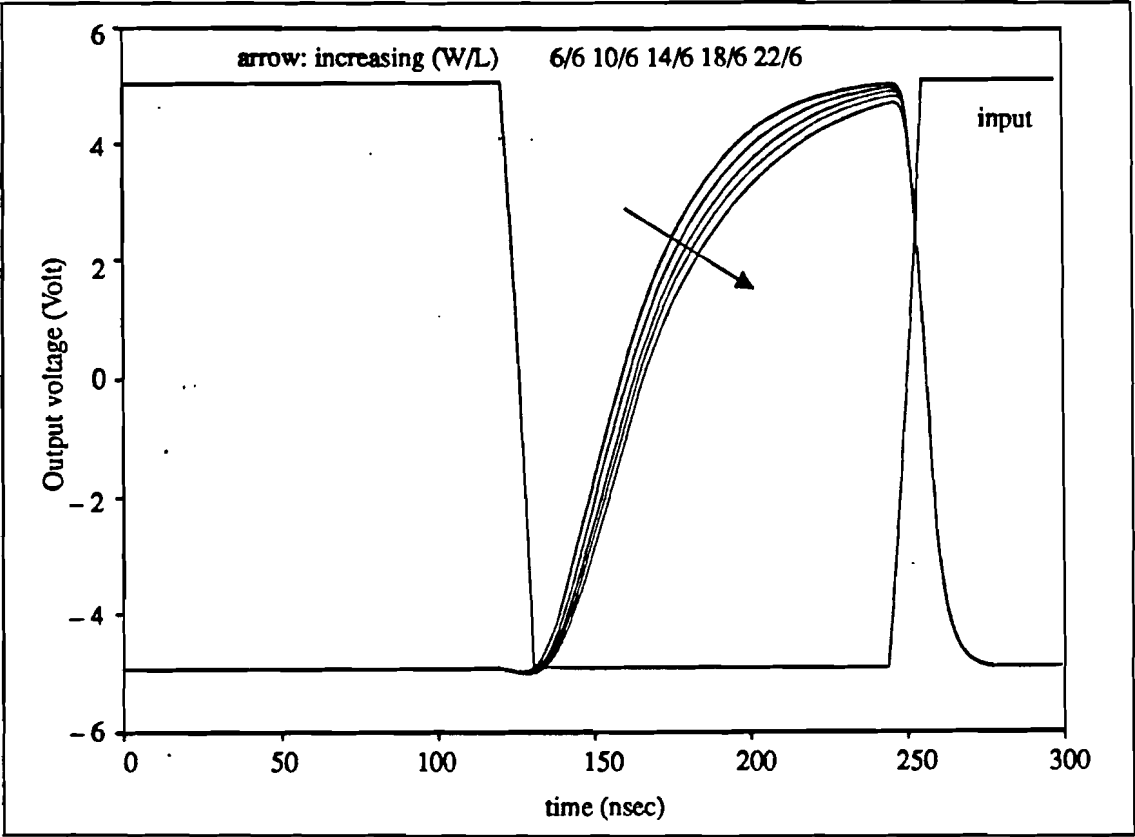


Figure 2.6 Transient response; dependency on $(W/L)_1$,

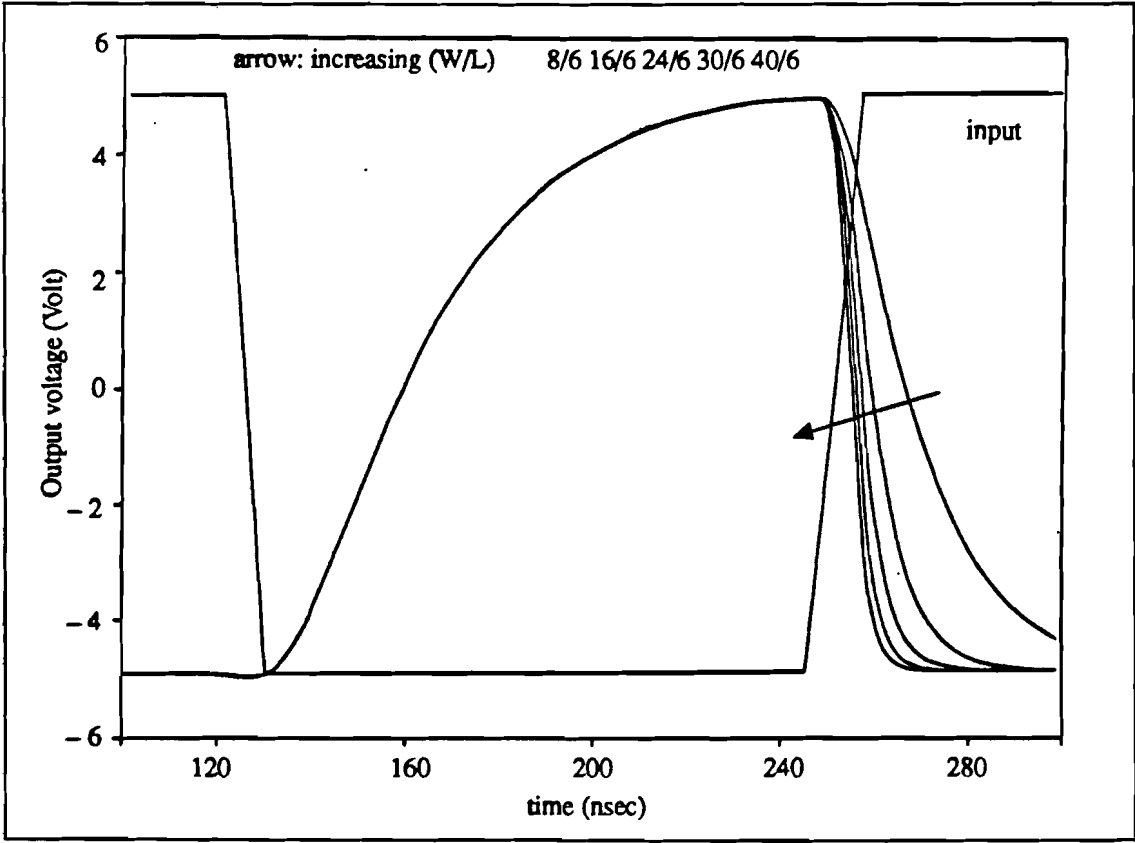


Figure 2.7 Transient response; dependency on $(W/L)_2$

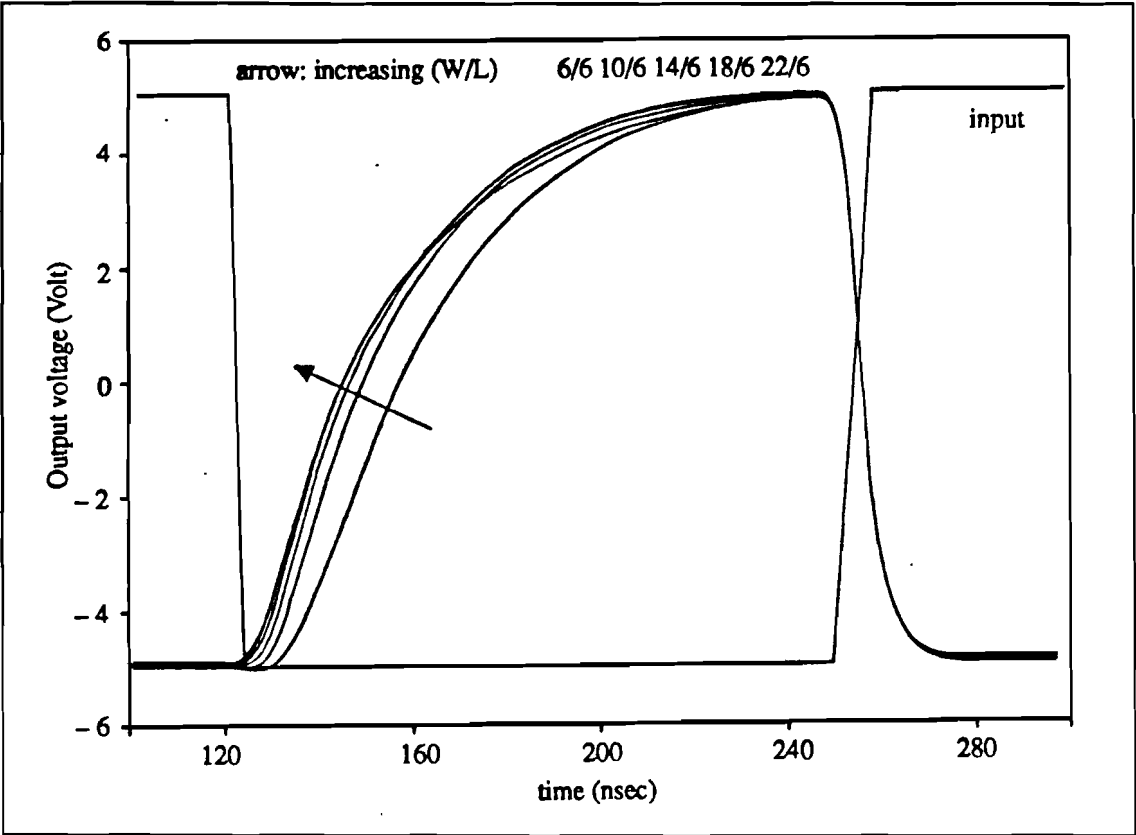


Figure 2.8 Transient response; dependency on (W/L) ,

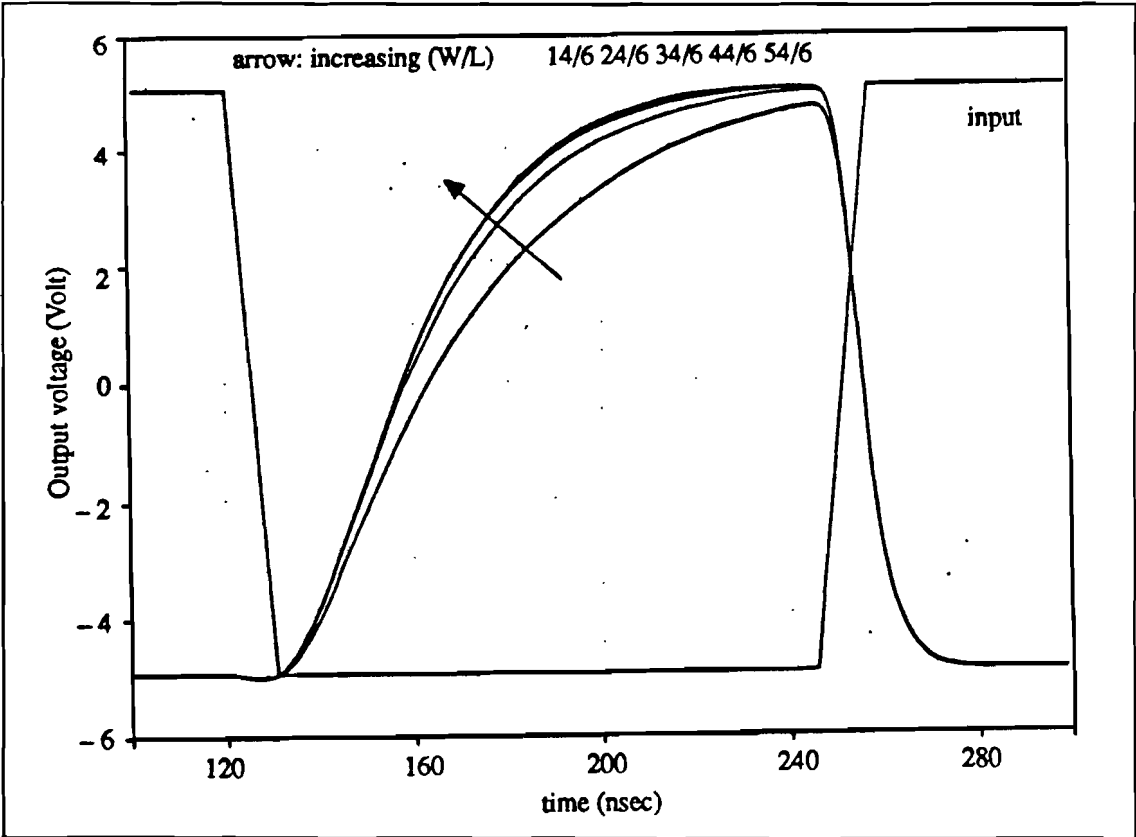


Figure 2.9 Transient response; dependency on (W/L) ,

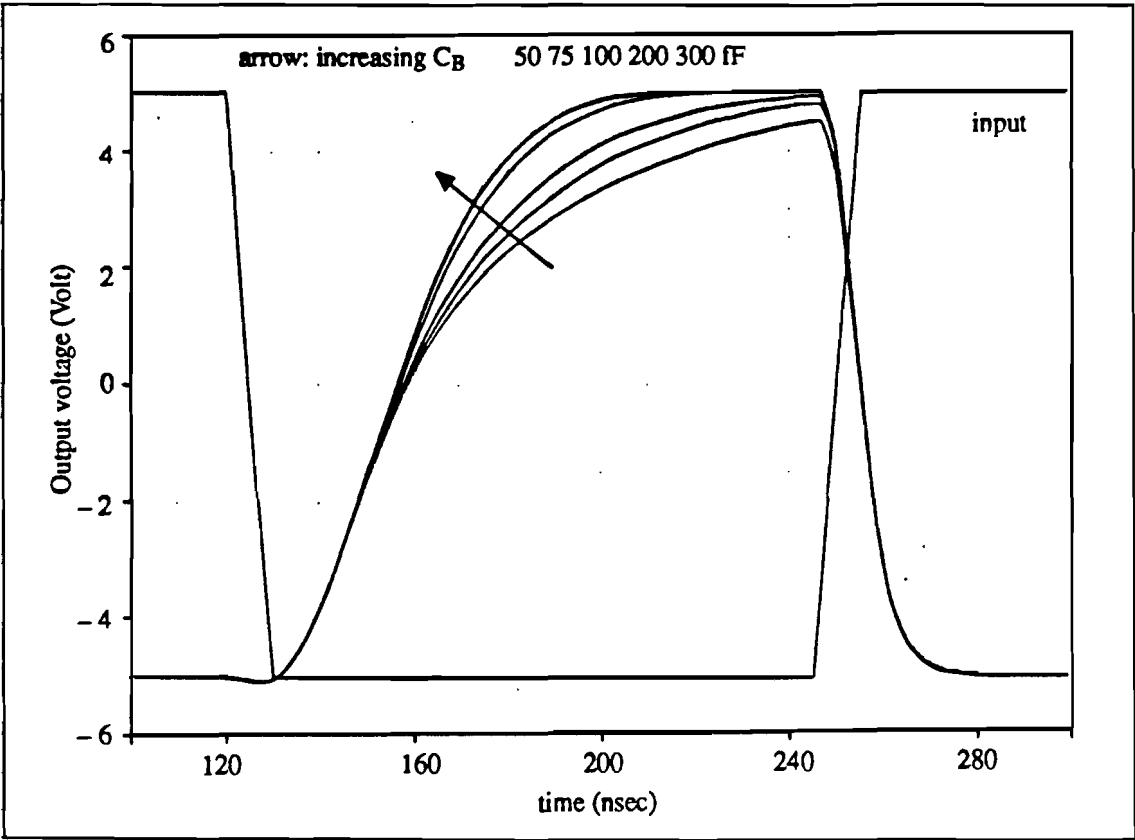


Figure 2.10 Transient response; dependency on C_B

CHAPTER 3 SPICE SIMULATION CONTROLLER

3.1 CONTROLLER CIRCUIT DESCRIPTION

The controller built with the previous described gates, is illustrated in figure 3.7 at the end of this chapter. Owing to the already mentioned hard-disk crash, the created controller layout, was lost. To help future layout editing, figure 3.6 gives an area efficient block diagram of the originally devised controller layout. This paragraph continues with two SPICE circuit descriptions, derived from figure 3.7. In the next paragraph the SPICE simulation results are discussed.

As figure 3.7 shows, the 15-bit shift register is constructed with 15 identical shift cell's, consisting of two inverters, four power inverters, four switches and two resistors. In comparison with figure 1.3, some additional circuit elements are inserted; two switches to perform reset functions (M_{R1} and $M_{R1/2}$). Secondly current limiting resistors (depletion transistors M_{CL1} and $M_{CL1/2}$), connected in series with the shift control switches (M_{SC1} and $M_{SC1/2}$). They limit the size of the voltage dip in the output of an inverter when the switch is activated, a possible cause of errors in succeeding circuits (Ref. [4] and [7]). Thirdly, in view of the possible high capacitive load, buffers are added to each shift register output. The circuit arrangement of these buffers is the same as for the 3-input power NOR, with two inputs deleted.

The reset function is not implemented in the same manner in all shift-cells. The object is to set phases Φ_0 and $\Phi_{14/2}$, and reset all other non-inverting outputs. Therefore the two reset transistors of the first shift-cell (SC0) are connected to V_{DD} . In the last shift-cell (SC14) they are both connected to V_{SS} . In the intermediate shift-cell's (SC1 to SC13) one transistor is connected to V_{DD} , while the other is connected to V_{dd} .

In the two 4-phase circuits also a reset-switch is incorporated (M_{R1} and M_{R2}). Setting phase 0 and resetting phases 1 to 3. To synchronize the reset operation with the master clock, an extra NOR gate is added, with signals $\Phi_{T41}(=\Phi_{MC})$ and \overline{RESET} as inputs (output = $\overline{\Phi_{T41} + RESET} = \Phi_{MC} \cdot RESET$). Current limiting transistors are not utilized because here the voltage dip is relative small and does not affect the performance of the circuit (power inverters as compared to normal inverters in the 15-bit shift register). The input capacitance of the inverters is here also employed as hold capacitor.

Employing a repeater guarantees non-overlapping of the two signals applied to the 1MHz 4-phase clock. Also this circuit restores the logical 'high' and 'low' voltage levels to V_{DD} and V_{SS} .

Because of the large number of transistors involved, it was not possible to simulate the whole controller in one SPICE run. The circuit consisting of the 4MHz 2-phase clock, 2MHz 4-phase clock, and repeater is simulated first. The 2MHz 4-phase circuit outputs are all loaded with 2 pF, the two repeater outputs are loaded each with 200fF, simulating the load presented by interconnections and 1MHz 4-phase clock. Serving as master clock is a signal with 4 MHz frequency, 115 nsec high/115 nsec low and rise/fall time of 10 nsec. The SPICE input file is given in appendix E, a schematic circuit diagram is illustrated in figure 3.1. Node numbers, <.> in the figure, correspond with the node numbering in the SPICE input file.

In a second SPICE run, pulse shaped approximations of the signals Φ_{T20} and Φ_{T21} , obtained from the previous simulation, are used as clock signals. These signals are applied to the inputs of the 1 MHz 4-phase clock. A 2-bit, instead of the 15-bit shift register is employed to reduce the size of the circuit that has to be simulated. Because of the sequential character of the shift register this circuit modification doesn't affect

the simulation results. All outputs are loaded with 2 pF each. This simulation is used to determine the transient response of the 15-bit shift register and 1 MHz 4-phase clock. The schematic circuit diagram is shown in figure 3.2, appendix F gives the SPICE input file.

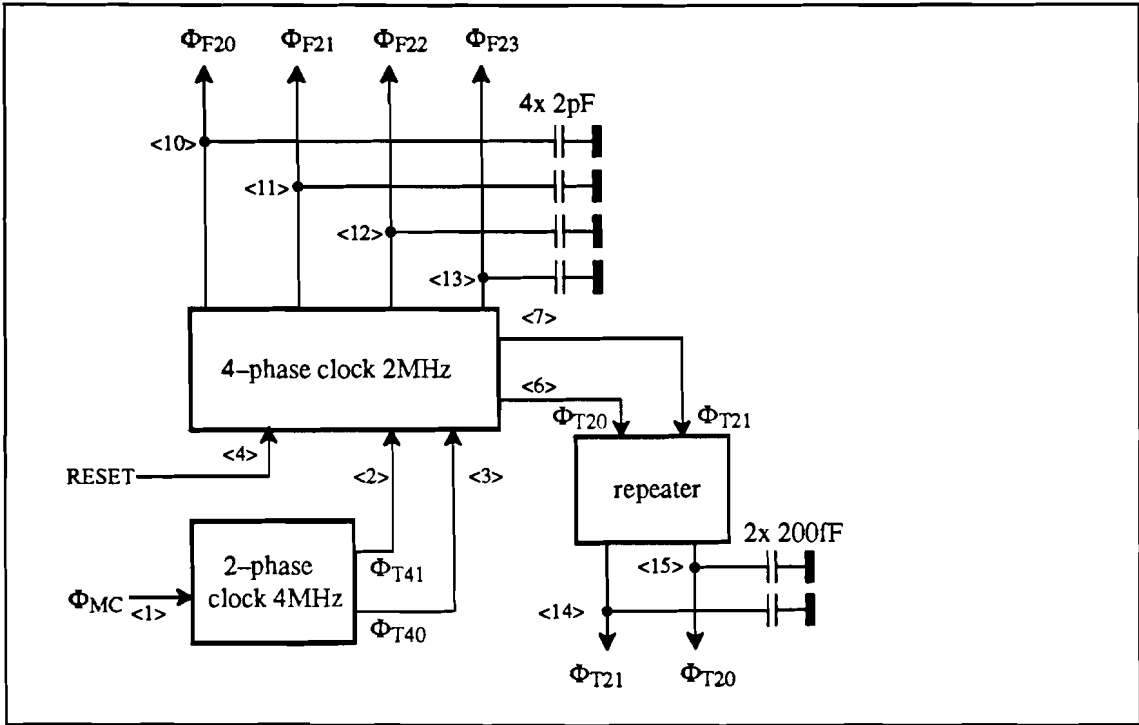


figure 3.1 Schematic diagram clock circuit A

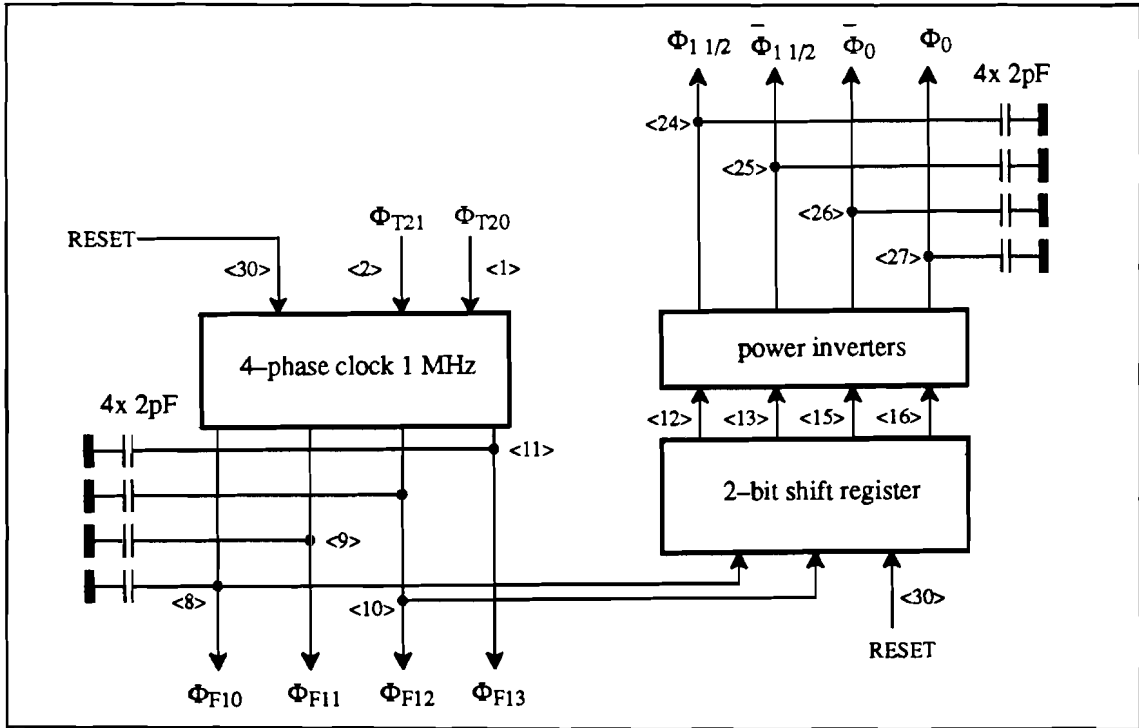


Figure 3.2 Schematic diagram clock circuit B

3.2 SIMULATION RESULTS

First the results from simulation A are discussed, next those of simulation B. The most important controller parameters are delay between signals and the rise/fall-time of these signals. All delay times are measured from time differences between the 50% low-high transition point of a signal and the master clock 50% low-high transition. Rise/fall times are taken from time differences at the 10% and 90% transition points.

The four output signals from the 4-phase clock are shown in figure 3.3, displaying the non-overlapping character and pulse shapes. In figure 3.4 the input signals to the repeater are illustrated, showing degenerated pulse shapes and overlap between these signals. Figure 3.5 displays the two repeater output signals, showing restored, non-overlapping, pulse shapes. From these figures the transient times summarised below are determined.

Delays with respect to the master clock signal are respectively:

- 63 nsec, phase Φ_{F20}
- 52 nsec, phase Φ_{T20}

Rise- and fall-times for phases Φ_{F2i} are:

- 37 nsec (rise)
- 21 nsec (fall)

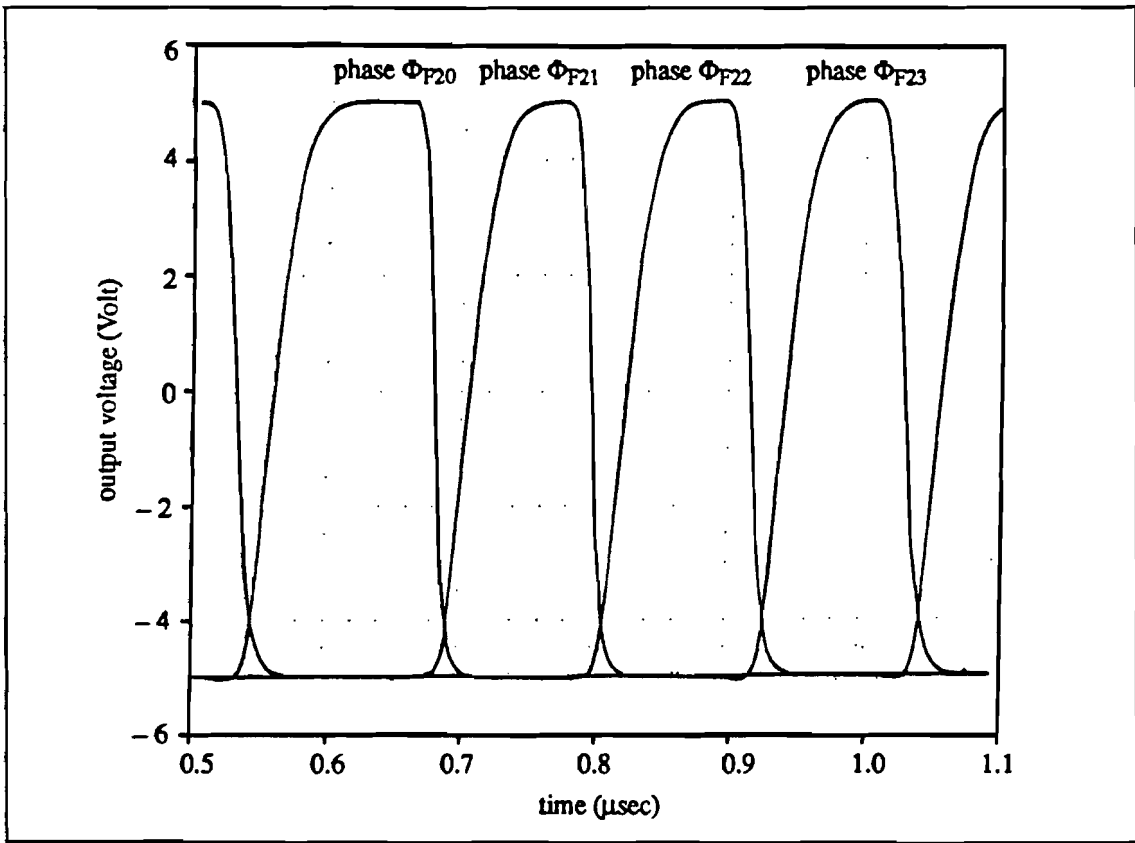


Figure 3.3 2 MHz 4-phase clock output signals ($C_L = 2\text{ pF/phase}$)

From similar graphs obtained with circuit B the transient times of the 15-bit shift register and 1MHz 4-phase clock are determined. The result is shown in the table on page 83.

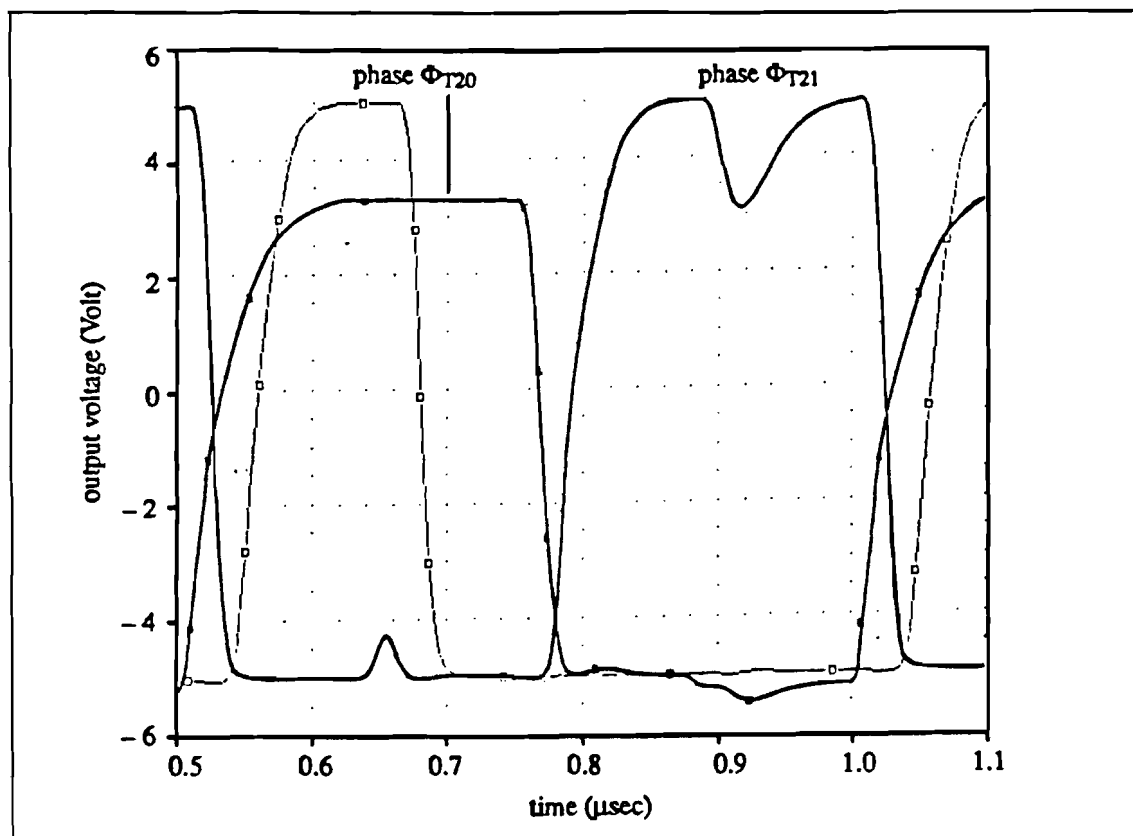


Figure 3.4 Repeater input signals

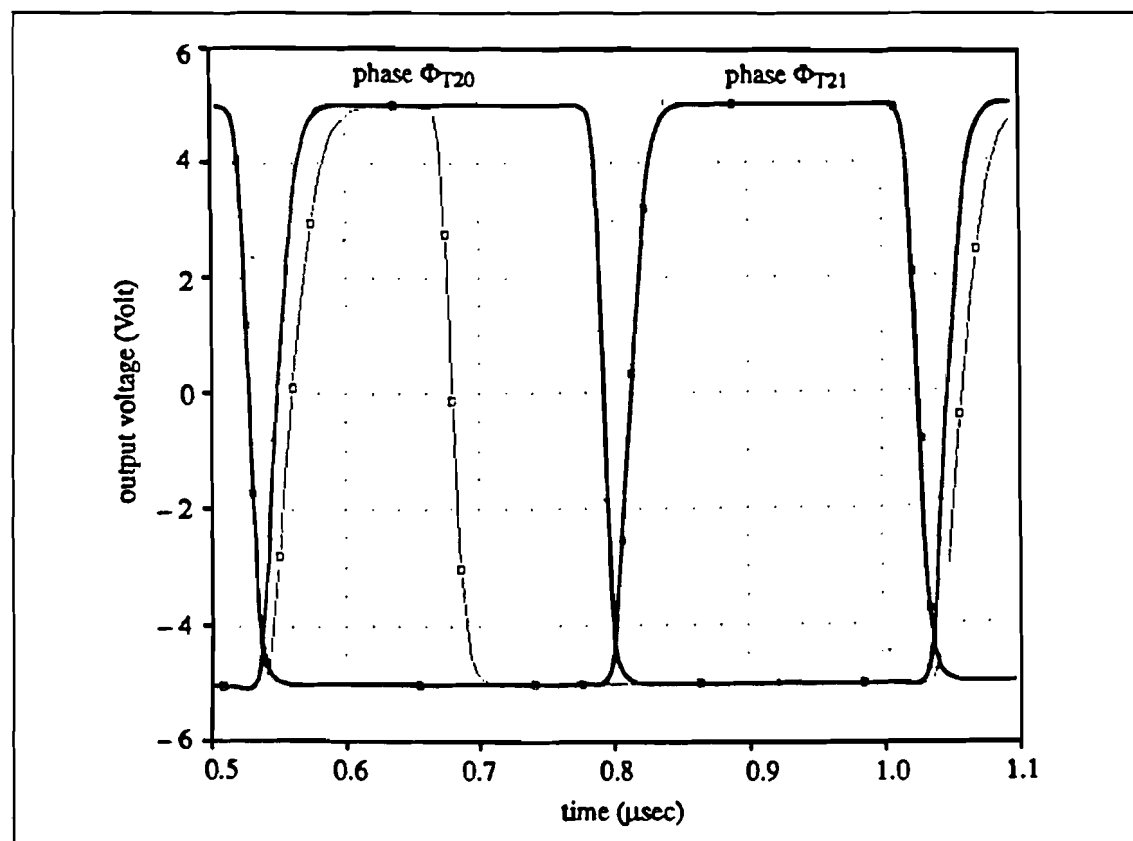


Figure 3.5 Repeater output signals

	phase Φ_{F10}	phase Φ_0	
Delay	91	122	nsec (relative to Φ_{MC})
rise time	36	37	nsec
fall time	20	21	nsec

Delay times ΔA and ΔB as defined in chapter 2, are now equal to:
 $\Delta A = 122 - 63 = 59 \text{ nsec } (\Phi_0 \text{ to } \Phi_{F20}); \quad \Delta B = 91 - 63 = 28 \text{ nsec } (\Phi_{F10} \text{ to } \Phi_{F20})$

Both delay times are smaller than the smallest pulse width of 125 nsec. Delay ΔB is very short and should not present any problems. ΔA is somewhat too large, this can be a possible cause of errors. For example consider an AND gate with phase Φ_{F10} and one of the non-inverted outputs of the 15-bit shift register as inputs. With no delay two pulses should be generated, 125 nsec 'high' and spaced by 375 nsec. Now however the first pulse will probably be too short, in order to be usefull as a control signal. Also the possibility exists that an unwanted (short) third pulse is generated. A solution would be to use phase Φ_{F21} , but then the two pulses are shifted by 125 nsec, violating the timing relation.

The above remarks show that the delay of the 15-bit shift register must be reduced. This can be accomplished by further development of the high power gates in still faster devices. The circuits designed by Faasse (Ref. [7]) provide a good starting point. A second alternative is to use a different clock circuit arrangement. We could use a second repeater connected in the same manner as the first one. Now however with input signals from the 1MHz 4-phase clock circuit. The repeater outputs are then used to control the shifting operation in the 15-bit shift register. With this method ΔA will be 11 nsec shorter (the difference between delays in phases Φ_{F20} and Φ_{T20}). However, as the simulation results strongly depend on the capacitive load, first a good estimate of the capacitive load per clock phase has to be found. Such an estimate can only be obtained when all subcircuits are designed and the layout of the entire SADM chip is completed. Then not only the parasitic capacitance of interconnects is known, but also the amount, and size of the transistors connected to each clock phase.

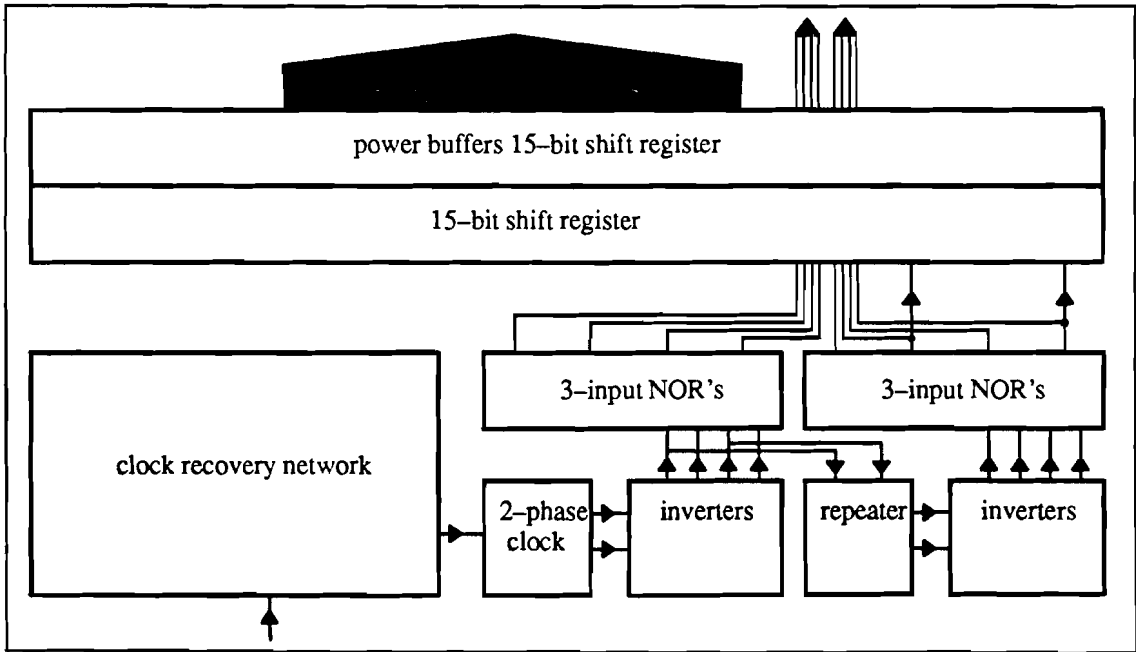


Figure 3.6 Schematic layout controller

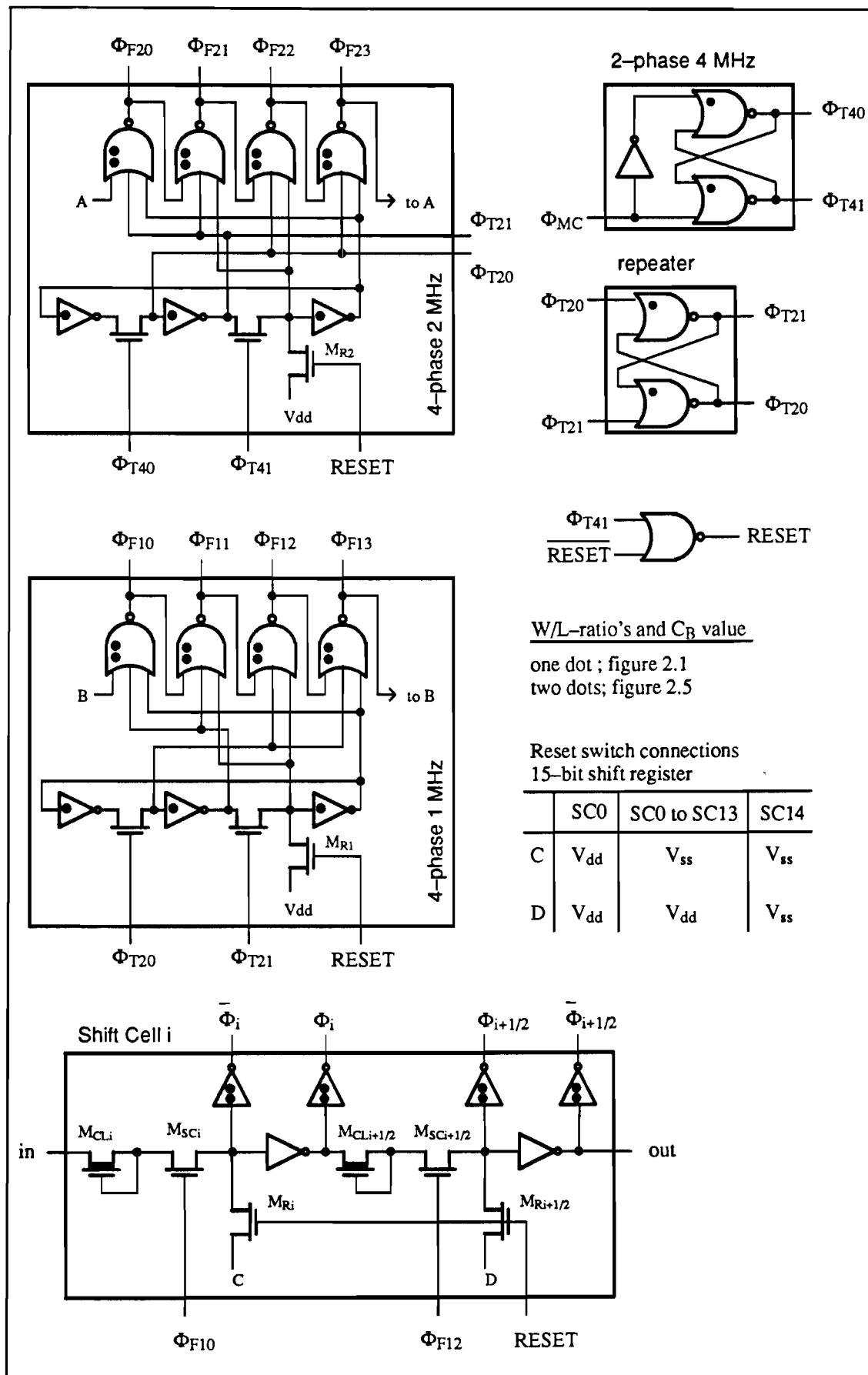


Figure 3.7 Circuit diagram controller

CHAPTER 4 CONCLUSIONS CONTROLLER DESIGN

The presented controller concept provides an total of 68 different signals to control the SADM timing process. The circuit complexity needed to generate these signals is very modest. Furthermore the controller is very flexible, any signal in an time grid of 125nsec and with a basic repetition rate of 64kHz, can be generated from the basic controller signals. Also the outputs can drive long interconnects and an large number of gates.

The introduced novel bootstrapped gate structure proves very useful. The logic function of a gate and buffering are realized in one circuit. In this circuit almost all of the supply current is used to charge or uncharge a capacitive load, there is only a small bias current flow. Compared to conventional buffers the bootstrapped buffer has lower power consumption, smaller peak current and smaller input capacitance. The gate variant of the bootstrap buffer can be easily modified into still higher power versions.

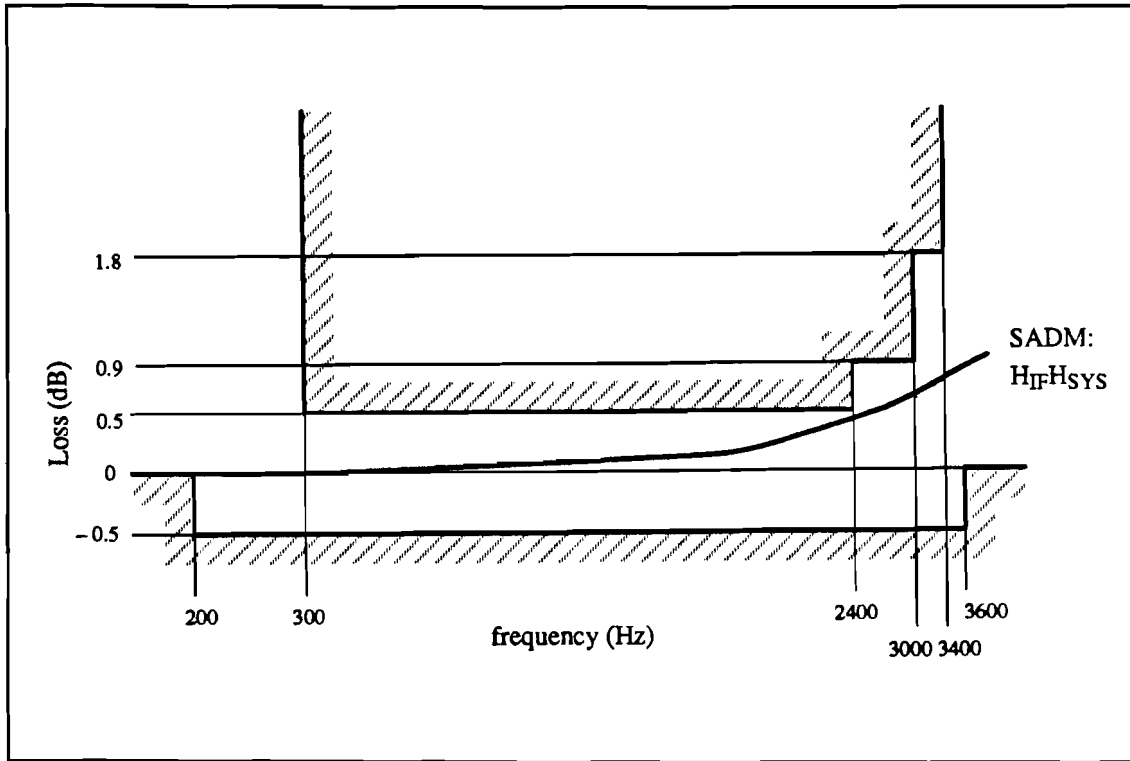
The observed delay in the 15-bit shift register is a possible error cause. It is therefor suggested to either reduce the load capacitance or alter the controller circuits/circuit arrangement. But as the delay is very dependent on the capacitive load, first the size of the capacitive load at all controller outputs must be known. Maybe it is not nescessary to modify the existing controller. If a modification is required then it is only nescessary to alter circuit elements where it is needed. For instance unused outputs of the 15-bit shift register don't need buffering, and moderately loaded outputs ($C_L < 1 \text{ pF}$) can use the existing standard inverting buffer. Loads in excess of 1 pF (connected to the outputs of the 15-bit shift register) require a buffer with higher power capability than those presented in this report. In this respect further study is needed.

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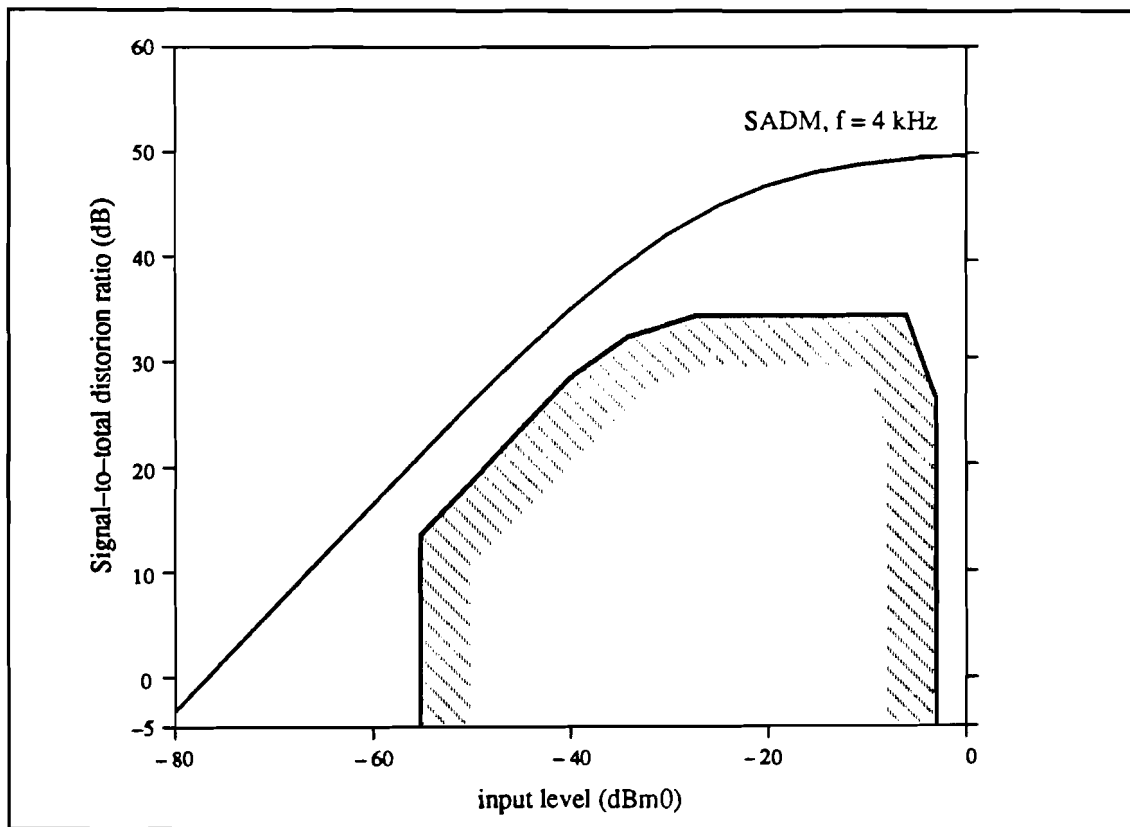
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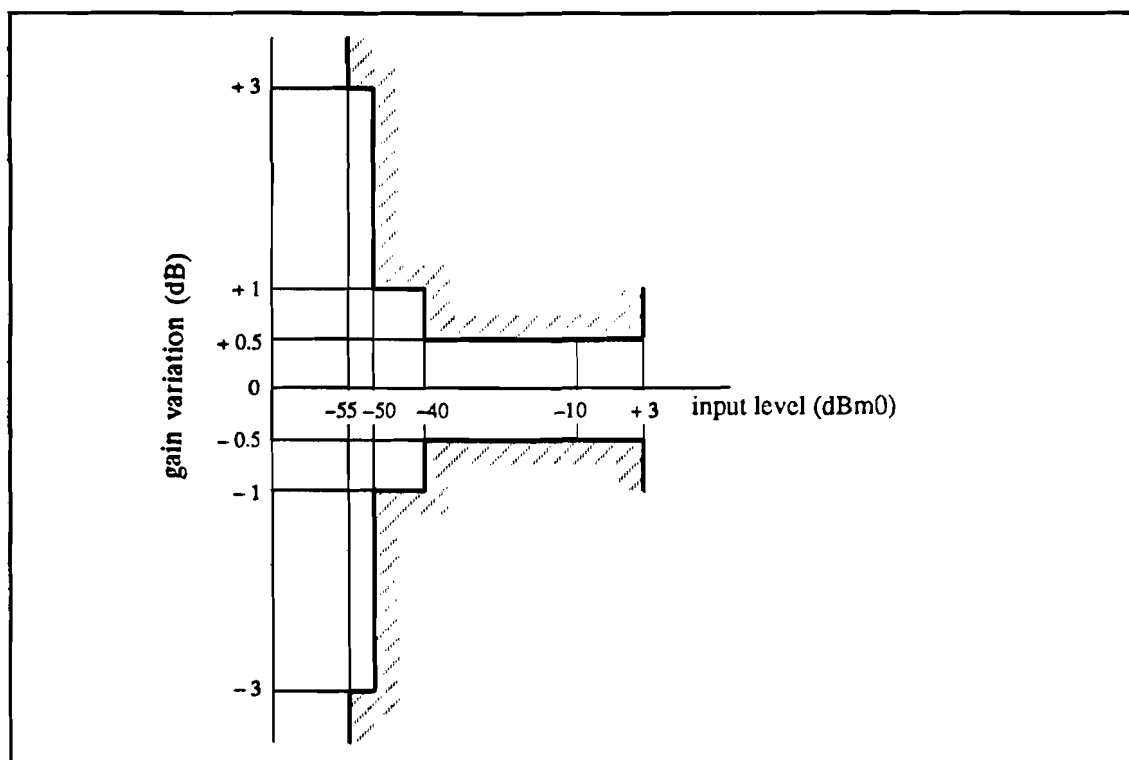
APPENDIX A CCITT RECOMMENDATION G.712



Attenuation/frequency distortion



Signal-to-noise ratio versus input signal level



Gain error versus input signal level

dBm0 = the absolute signal power, in decibels, referred to a point of zero relative level

APPENDIX B

1

2

3

4

TABLE CAPACITOR VALUES

TABLE RELATIVE ACCURACY CAPACITORS

SOURCE CODE WORST CASE ANALYSIS PROGRAM

SOURCE CODE MONTE CARLO ANALYSIS PROGRAM

1 TABLE Capacitor values in unit capacitances C_u

DAC version	DAC18 ¹	DAC25 ¹	DAC26 ²	DAC34 ¹	DAC33 ¹	DAC32 ¹
C_0	1	1	1	1	1	1
C_1	2	2	2	1	2	2
C_2	4	4	1	2	1	4
C_3	8	1	2	4	2	1
C_4	16	2	4	1	4	2
C_5	32	4	8	2	1	4
C_6	64	8	16	4	2	1
C_7	128	16	32	8	4	2
C_{p1}	2.55	0.1971	0.1793	0.2444	0.1793	0.1971
C_{p2}	–	0.3271	0.6439	0.2361	0.2435	0.2238
C_{p3}	–	–	–	0.1634	0.0932	0.0432
C_{cm1}	–	1	1	1	1	1
C_{cm2}	–	–	–	1	1	1
C_{cp1}	–	1.1710	1.3931	2.2444	1.3931	1.1710
C_{cp2}	–	–	–	1.3369	1.3205	1.3212

- 1) One unit capacitor = 1 pF
- 2) One unit capacitor = 0.39 pF

2 TABLE Relative accuracy capacitors, ΔC/C (%)

DAC version	DAC18	DAC25	DAC26	DAC34	DAC33	DAC32
C ₀	1.004	1.004	1.603	1.004	1.004	1.004
C ₁	0.713	0.713	1.135	1.004	0.713	0.713
C ₂	0.508	0.508	1.603	0.713	1.004	0.508
C ₃	0.365	1.004	1.135	0.508	0.713	1.004
C ₄	0.266	0.713	0.805	1.004	0.508	0.713
C ₅	0.198	0.508	0.572	0.713	1.004	0.508
C ₆	0.154	0.365	0.410	0.508	0.713	1.004
C ₇	0.126	0.266	0.297	0.365	0.508	0.713
C _{p1}	20.0	20.0	20.0	20.0	20.0	20.0
C _{p2}	–	20.0	20.0	20.0	20.0	20.0
C _{p3}	–	–	–	20.0	20.0	20.0
C _{cm1}	–	1.00	1.60	1.00	1.00	1.00
C _{cm2}	–	–	–	1.00	1.00	1.00
C _{cp1}	–	1.00	3.00	1.00	1.00	1.00
C _{cp2}	–	–	–	1.00	1.00	1.00

3 SOURCE CODE WORST CASE ANALYSIS PROGRAM

The program is written in 'TURBO PASCAL', version 4.0,
traded by Borland International Inc.

```

PROGRAM WORST_CASE_ANALYSIS; {WCDAC33}

USES CRT          ;

CONST Vref=2      ;
      h  =0.00001;

TYPE Binary      =-1..1          ;
OutArray  =ARRAY[1..255] OF REAL ;
DerivArray=ARRAY[0..14,1..255] OF REAL;
CapArray  =ARRAY[0..14 ] OF REAL ;
BinArray  =ARRAY[0..7  ] OF Binary ;

VAR  C,Cdisturb,S,Max      :CapArray ;
     Deriv                 :DerivArray;
     BinaryCode            :BinArray  ;
     Error                 :OutArray  ;
     i,j,k,Code            :INTEGER   ;
     Inputcode,Maxerror,   :          ;
     Vlsb,temp             :REAL      ;

PROCEDURE Initialyse;
VAR i :INTEGER;
BEGIN
  C[7 ]:=4;C[6 ]:=2;C[5 ]:=1;          {network capacitors 3e stage      }
  C[4 ]:=4;C[3 ]:=2;C[2 ]:=1;          {network capacitors 2e stage      }
  C[1 ]:=2;C[0 ]:=1;                  {network capacitors 1e stage      }
  C[8 ]:=0.17931;C[11]:=1.0;           {parasitic + completion 1e stage  }
  C[9 ]:=0.24350;C[12]:=1.0;           {parasitic + completion 2e stage  }
  C[10]:=0.09321;                     {parasitic 3e stage               }
  C[13]:=1.39310;C[14]:=1.32050;       {coupling capacitors              }
  S[7 ]:=0.00508;S[6 ]:=0.00713;       {relative error network capacitors}
  S[5 ]:=0.01004;S[4 ]:=0.00508;       {      "      "      "      "      }
  S[3 ]:=0.00713;S[2 ]:=0.01004;       {      "      "      "      "      }
  S[1 ]:=0.00713;S[0 ]:=0.01004;       {      "      "      "      "      }
  FOR i:=8 TO 10 DO S[i]:=0.200 ; {relative error parasitic capacitors }
  FOR i:=11 TO 12 DO S[i]:=0.010 ; {relative error completion capacitors }
  FOR i:=13 TO 14 DO S[i]:=0.010 ; {relative error coupling capacitors  }
  FOR i:=0 TO 14 DO S[i]:=3*S[i] ; {max relative error capacitors      }
  FOR i:=0 TO 14 DO Cdisturb:=C[i];
END;

FUNCTION Transfer(b:BinArray;C:CapArray):REAL;
VAR Cv1,Cv2,Cv3,
    factor1,factor2,
    temp1,temp2      :REAL;
BEGIN
  Cv1 :=C[0]+C[1]+C[8]+C[11]+C[13] ;
  Cv2 :=C[2]+C[3]+C[4]+C[9 ]+C[12]+C[13]+C[14] ;
  Cv3 :=C[5]+C[6]+C[7]+C[10]+C[14] ;
  factor1 :=1-(SQR(C[13]/(Cv1*Cv2))) ;
  factor2 :=1-(SQR(C[14]/(factor1*Cv2*Cv3))) ;
  temp1 :=b[5]*C[5]+b[6]*C[6]+b[7]*C[7] ;
  temp2 :=(C[14]/(Cv2*factor1))*
           (b[2]*C[2]+b[3]*C[3]+b[4]*C[4]+(C[13]/Cv1)*
            (b[0]*C[0]+b[1]*C[1])) ;
  Transfer:=(temp1+temp2)*Vref/(factor2*Cv3) ;
END;

```

```

FUNCTION Sign(Input:REAL):INTEGER;
BEGIN
  IF Input<0 THEN Sign:=-1
    ELSE Sign:=1
END;

```

```

PROCEDURE Calculate_maximum_error(k:INTEGER;Error:REAL);
VAR i:INTEGER;
BEGIN
  IF ABS(Error) > MaxError THEN
    BEGIN
      MaxError:=ABS(Error);
      Code      :=k      ;
      FOR i:=0 TO 14 DO Max[i]:=Deriv[i,k]*S[i]
    END
END;

```

```

PROCEDURE Calculate_binary_code(Decimal:REAL);
VAR i,j :INTEGER;
    temp:REAL;
BEGIN
  temp:=128;
  FOR j:=1 TO 8 DO
    BEGIN
      i:=ABS(j-8);
      IF ABS(Decimal) >= temp THEN
        BEGIN
          BinaryCode[i]:=Sign(Decimal);
          Decimal:=Decimal-Sign(Decimal)*temp
        END
      ELSE BinaryCode[i]:=0;
      temp:=ROUND(temp/2)
    END;
  END;
END;

```

```

BEGIN { MAIN }
  CLRSCR                      ;
  Writeln                     ;
  Write(' capacitor number (total 14): ');
  Initialyse                  ;

  { calculate least significant bit voltage }

  Calculate_binary_Code(1)      ;
  Vlsb:=Transfer(BinaryCode,C)  ;
  Write('      Vlsb = ',Vlsb)   ;

  { calculate Jacobian matrix D }

  FOR i:=0 TO 14 DO
    BEGIN
      Cdisturb:=C[i]*(1+h)      ;
      GOTOXY(32,2)              ;
      Write(i)                  ;
      FOR k:=1 TO 255 DO
        BEGIN
          InputCode :=k                      ;
          Calculate_binary_code(InputCode)    ;
          Deriv[i,k]:=(Transfer(BinaryCode,Cdisturb) -
            Transfer(BinaryCode,C))/h          ;
        END;
      Cdisturb[i]:=C[i]      ;
    END;
  END;

  { Calculate maximum error in all 255 input words b }

```

```

MaxError:=0;
FOR k:=1 TO 255 DO
  BEGIN
    Error[k]:=0;
    FOR i:=0 TO 14 DO Error[k]:=Error[k]+ABS(Deriv[i,k]*S[i]);
    Calculate_maximum_error(k,Error[k]);
  END;
GOTOXY(1,4);
WRITELN(' error in #LSB   inputcode at maximum error ');
WRITELN(' ',(MaxError/Vlsb):10,' ',Code);
WRITELN;

{ calculate percentual contribution to maximum error of all capacitors }

temp:=0;
FOR i:=0 TO 14 DO temp:=temp+ABS(Max[i]);
WRITELN;
WRITELN(' capacitor      % of error');
FOR i:=0 TO 14 DO
  BEGIN
    Max[i]:=ABS(100*Max[i]/temp);
    WRITELN('  C('',i:2,'')', ' ',Max[i]:9);
  END;
END.

```


4 SOURCE CODE MONTE CARLO ANALYSIS PROGRAM

```

PROGRAM MONTE_CARLO_ANALYSIS; {MCDAC33}

USES CRT      ;

CONST Vref=2      ;
      MaxNrOfAnalyses=1000;
      NrOfFractions =10 ;

TYPE Binary      =-1..1      ;
      OutArray   =ARRAY[0..510] OF REAL      ;
      CapArray   =ARRAY[0..14 ] OF REAL      ;
      BinArray   =ARRAY[0..7 ] OF Binary     ;
      ErrorArray =ARRAY[1..MaxNrOfAnalyses] OF REAL;
      FracArray  =ARRAY[1..NrOfFractions ] OF REAL;

VAR C,Cdisturb,S,      :CapArray      ;
    BinaryCode        :BinArray      ;
    MaxError          :ErrorArray    ;
    Output            :OutArray      ;
    i,j,k             :INTEGER       ;
    Vdac,MeanVdac,    :              ;
    Vodac,MeanVodac,  :              ;
    MeanSqrVdac,SD,   :              ;
    Inputcode,Input,  :              ;
    Error, UpperLimit, :              ;
    SumInput,SumOutput, :              ;
    SumInOut,SumSqrIn :REAL          ;
    Fraction          :Fracarray     ;

FUNCTION Sign(Input:REAL):INTEGER;
BEGIN
  IF Input<0 THEN Sign:=-1
    ELSE Sign:=1
END;

PROCEDURE Initialyse;
VAR i :INTEGER;
BEGIN
  C[7 ]:=4;C[6 ]:=2;C[5 ]:=1;      {network capacitors 3e stage      }
  C[4 ]:=4;C[3 ]:=2;C[2 ]:=1;      {network capacitors 2e stage      }
  C[1 ]:=2;C[0 ]:=1;               {network capacitors 1e stage      }
  C[8 ]:=0.17931;C[11]:=1.0;        {parasitic + completion 1e stage }
  C[9 ]:=0.24350;C[12]:=1.0;        {parasitic + completion 2e stage }
  C[10]:=0.09321;                  {parasitic 3e stage               }
  C[13]:=1.39310;C[14]:=1.32050;    {coupling capacitors              }
  S[7 ]:=0.00508;S[6 ]:=0.00713;    {relative error network capacitors }
  S[5 ]:=0.01000;S[4 ]:=0.00508;    { " " " " " " " " " " " " " " }
  S[3 ]:=0.00713;S[2 ]:=0.01000;    { " " " " " " " " " " " " " " }
  S[1 ]:=0.00713;S[0 ]:=0.01000;    { " " " " " " " " " " " " " " }
  FOR i:=8 TO 10 DO S[i]:=0.200 ; {relative error parasitic capacitors }
  FOR i:=11 TO 12 DO S[i]:=0.010 ; {relative error completion capacitors }
  FOR i:=13 TO 14 DO S[i]:=0.010 ; {relative error coupling capacitors }
  FOR i:=0 TO 14 DO Cdisturb:=C[i];
END;

PROCEDURE Calculate_maximum_error(i:INTEGER;Error:REAL);
VAR i:INTEGER;
BEGIN
  IF ABS(Error) > MaxError THEN MaxError:=ABS(Error);
END;

```

```

FUNCTION Transfer(b:BinArray;C:CapArray):REAL;
VAR Cv1,Cv2,Cv3,
    factor1,factor2,
    temp1,temp2 :REAL;
BEGIN
    Cv1      :=C[0]+C[1]+C[8]+C[11]+C[13]      ;
    Cv2      :=C[2]+C[3]+C[4]+C[9 ]+C[12]+C[13]+C[14]  ;
    Cv3      :=C[5]+C[6]+C[7]+C[10]+C[14]      ;
    factor1   :=1-(SQR(C[13]/(Cv1*Cv2)))        ;
    factor2   :=1-(SQR(C[14]/(factor1*Cv2*Cv3)))    ;
    temp1     :=b[5]*C[5]+b[6]*C[6]+b[7]*C[7]      ;
    temp2     :=(C[14]/(Cv2*factor1))*
                (b[2]*C[2]+b[3]*C[3]+b[4]*C[4]+(C[13]/Cv1)*
                (b[0]*C[0]+b[1]*C[1]))          ;
    Transfer:=(temp1+temp2)*Vref/(factor2*Cv3)      ;
END;

PROCEDURE Calculate_binary_code(Decimal:REAL);
VAR i,j :INTEGER;
    temp:REAL;
BEGIN
    temp:=128;
    FOR j:=1 TO 8 DO
        BEGIN
            i:=ABS(j-8);
            IF ABS(Decimal) >= temp THEN
                BEGIN
                    BinaryCode[i]:=Sign(Decimal);
                    Decimal:=Decimal-Sign(Decimal)*temp
                END
            ELSE BinaryCode[i]:=0;
            temp:=ROUND(temp/2)
        END;
    END;
END;

PROCEDURE Calculate_fraction(Number:INTEGER;Limit:REAL);
VAR i:INTEGER;
BEGIN
    Fraction[Number]:=0;
    FOR i:=1 TO NrOfAnalyses DO
        BEGIN
            IF MaxError[i] <= Limit THEN Fraction[Number]:=
                Fraction[number]+1/NrOfAnalyses;
        END;
    END;
END;

PROCEDURE Disturb_capacitor_values;
VAR i :INTEGER;
    Disturb:REAL ;
BEGIN
    RANDOMIZE;
    FOR i:=0 TO 14 DO
        BEGIN
            Disturb:=SQRT(-2*SQR(S[i]*LN(RANDOM)))*COS(2*PI*RANDOM);
            Cdisturb:=C[i]*(1+Disturb);
        END;
    END;
END;

BEGIN { MAIN }
    CLRSCR ;
    WRITELN ;
    WRITELN ;
    WRITE(' Give the number of analyses (max 1000): ');
    READLN(NrOfAnalyses) ;
    WRITELN ;
    WRITELN ;

```

```

WRITE( ' Analysis number: ' ) ;
Initialyse ;
MeanVdac :=0 ;
MeanVodac :=0 ;
MeanSqrVdac:=0 ;
FOR i:=1 TO NrOfAnalyses DO
  BEGIN
    GOTOXY(19,6) ;
    WRITE(i) ;
    Disturb_capacitor_values;
    MaxError :=0 ;
    SumInput :=0 ;
    SumSqrIn :=0 ;
    SumInOut :=0 ;
    SumOutput:=0 ;
    FOR k:=0 TO 510 DO
      BEGIN
        Inputcode:=k-255 ;
        Calculate_binary_code(InputCode) ;
        Output[k]:=Transfer(Binarycode,Cdisturb);
        Input :=InputCode ;
        SumInput :=SumInput+Input ;
        SumSqrIn :=SumSqrIn+SQR(Input) ;
        SumOutput:=SumOutput+Output[k] ;
        SumInOut :=SumInOut+Input*Output[k] ;
      END;
      Vdac :=(-(SumInput*SumOutput) + (511*SumInOut))/
        (-SQR(SumInput) + (511*SumSqrIn)) ;
      Vodac:=(SumOutput-(Vdac*SumInput))/511 ;
      GOTOXY(33,6) ;
      WRITE('Vdac = ',Vdac:10,' Vodac = ',Vodac:10) ;
      MeanVdac :=MeanVdac + Vdac/NrOfAnalyses ;
      MeanSqrVdac:=MeanSqrVdac + SQR(Vdac)/NrOfAnalyses;
      MeanVodac :=MeanVodac + Vodac/NrOfAnalyses ;
      FOR k:=0 TO 510 DO
        BEGIN
          Inputcode:=k-255 ;
          Error :=(output[k]-(Vdac*InputCode+Vodac))/Vdac;
          Calculate_maximum_error(i,Error) ;
        END;
      END;
    WRITELN;
    WRITELN;
    FOR i:=1 TO NrOfFractions DO
      BEGIN
        UpperLimit:=0.1*i ;
        Calculate_fraction(i,UpperLimit);
        WRITELN(' FRACTION WITH ERROR SMALLER THEN ',UpperLimit:1:2, ' LSB: ',
          Fraction[i]:1:2) ;
      END;
    SD:=SQR(ABS(MeanSqrVdac-SQR(MeanVdac))) ;
    WRITELN ;
    WRITELN(' mean values over all analyses: Vdac = ',MeanVdac:10,
      ' Vodac = ',MeanVodac:10) ;
    WRITELN(' standard deviation of Vdac, SD = ',SD:10);
  END.

```

APPENDIX C SPICE LISTING OPERATIONAL AMPLIFIER

SIMULATION OPAMP: OPEN-LOOP GAIN VERSUS FREQUENCY

```

*****
*****
*
* SUPPLY- AND BULK VOLTAGES
*
VDD 20 0 DC 5V
VSS 29 0 DC -5V
VBULK 30 0 DC -5V
*
*****
*****
*****
***** OPAMP *****
*****
*****
*****
*
* 1E STAGE
*
M1 4 1 3 30 ENH W=36U L= 6U AS=432P AD=432P PS= 96U PD= 96U
M2 5 2 3 30 ENH W=36U L= 6U AS=432P AD=432P PS= 96U PD= 96U
M3 6 3 4 30 DEP W= 6U L= 6U AS= 72P AD= 72P PS= 36U PD= 36U
M4 7 3 5 30 DEP W= 6U L= 6U AS= 72P AD= 72P PS= 36U PD= 36U
M5 20 6 6 30 DEP W=12U L=26U AS=144P AD=144P PS= 48U PD= 48U
M6 20 7 7 30 DEP W=12U L=26U AS=144P AD=144P PS= 48U PD= 48U
M7 3 8 29 30 ENH W=21U L=19U AS=252P AD=252P PS= 66U PD= 66U
*
*****
*****
*
* LEVEL SHIFTER 1
*
M8 6 6 9 30 ENH W=12U L=10U AS=144P AD=144P PS= 48U PD= 48U
M9 9 9 10 30 ENH W=12U L=10U AS=144P AD=144P PS= 48U PD= 48U
M10 10 10 11 30 ENH W=12U L=10U AS=144P AD=144P PS= 48U PD= 48U
M11 11 8 29 30 ENH W=12U L=20U AS=144P AD=144P PS= 48U PD= 48U
*
*****
*****
*
* LEVEL SHIFTER 2
*
M12 7 7 12 30 ENH W=12U L=10U AS=144P AD=144P PS= 48U PD= 48U
M13 12 12 13 30 ENH W=12U L=10U AS=144P AD=144P PS= 48U PD= 48U
M14 13 13 14 30 ENH W=12U L=10U AS=144P AD=144P PS= 48U PD= 48U
M15 14 8 29 30 ENH W=12U L=20U AS=144P AD=144P PS= 48U PD= 48U
*
*****
*****
*
* 2E STAGE
*
M16 17 11 8 30 ENH W=60U L= 6U AD=720P AS=720P PD=144U PS=144U
M17 18 14 8 30 ENH W=60U L= 6U AD=720P AS=720P PD=144U PS=144U
M18 15 8 17 30 DEP W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M19 16 8 18 30 DEP W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M20 20 15 15 30 DEP W= 6U L=24U AD= 72P AS= 72P PD= 36U PS= 36U
M21 20 16 16 30 DEP W= 6U L=24U AD= 72P AS= 72P PD= 36U PS= 36U
M22 8 19 29 30 ENH W=12U L=14U AD=144P AS=144P PD= 48U PS= 48U
*

```

```

*****
*****
*
* CM-FEEDBACK CIRCUIT
*
M23 22 11 23 30 ENH W=31U L= 6U AD=372P AS=372P PD= 86U PS= 86U
M24 22 14 23 30 ENH W=31U L= 6U AD=372P AS=372P PD= 86U PS= 86U
M25 21 8 22 30 DEP W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M26 20 21 21 30 DEP W= 6U L=24U AD= 72P AS= 72P PD= 36U PS= 36U
M27 23 19 29 30 ENH W= 6U L=12U AD= 72P AS= 72P PD= 36U PS= 36U
*
*****
*****
*
* LEVEL SHIFTER CM-FEEDBACK CIRCUIT
*
M28 20 21 25 30 ENH W= 7U L=15U AD= 84P AS= 84P PD= 38U PS= 38U
M29 25 25 19 30 ENH W= 7U L=15U AD= 84P AS= 84P PD= 38U PS= 38U
M30 19 19 29 30 ENH W= 6U L=12U AD= 72P AS= 72P PD= 36U PS= 36U
*
*****
*****
*
* OUTPUT STAGE
*
M31 20 15 27 30 DEP W=22U L= 8U AD=264P AS=264P PD= 68U PS= 78U
M32 27 19 29 30 DEP W=17U L=10U AD=312P AS=312P PD= 76U PS= 76U
M33 20 16 28 30 DEP W=22U L= 8U AD=264P AS=264P PD= 68U PS= 68U
M34 28 19 29 30 DEP W=17U L=10U AD=312P AS=312P PD= 76U PS= 76U
*
*****
*****
*
* FREQUENCY COMPENSATION
*
CM1 11 27 0.7PF
CM2 14 28 0.7PF
*
*****
*****
*
* CAPACITIVE LOAD
*
CL 27 0 4PF
*
*****
*****
*
* INPUT VOLTAGES
*
VIN1 1 0 AC 0.0001V
VIN2 2 0 AC -0.0001V
*
*****
*****
*
* SPICE ANALYSIS
*
.AC DEC 20 10HZ 100MEG
.NODESET V( 3)=-1.05 V( 4)= 0.20 V( 5)= 0.20 V( 6)= 1.95
+ V( 7)= 1.95 V( 8)=-3.50 V( 9)= 0.32 V(10)=-1.21
+ V(11)=-2.65 V(12)= 0.32 V(13)=-1.21 V(14)=-2.65
+ V(15)= 1.80 V(16)= 1.80 V(17)=-2.01 V(18)=-2.01
+ V(19)=-3.35 V(21)= 0.57 V(22)=-2.09 V(23)=-3.52
+ V(25)=-1.44 V(27)= 0.00 V(28)= 0.00
.OPTIONS LIMPTS=5000 RELTOL=0.0001 ITL1=100 ITL2=50 ITL4=40
+ ITL5=0 ABSTOL=1PA VNTOL=1UV NUMDGT=7
.PROBE V( 1) V( 2) V(27)
*

```

```
*****
*****
*
* TRANSISTOR MODEL PARAMETERS
*
*
.MODEL DEP NMOS (LEVEL=2 VTO=-2.5 PB=0.75 CGSO=370P CGDO=370P
+ CGBO=395P RSH=20 XQC=0.4 CJ=80U MJ=0.5 CJSW=330P
+ MJSW=0.25 JS=6.2U TOX=65N NSUB=1.66E15 XJ=1U
+ LD=0.5U WD=0.5U UO=600 UCRIT=65000 UEXP=0.115
+ VMAX=5E4 DELTA=1)
*
.MODEL ENH NMOS (LEVEL=2 VTO=0.55 PB=0.75 CGSO=370P CGDO=370P
+ CGBO=395P RSH=20 XQC=0.4 CJ=80U MJ=0.5 CJSW=330P
+ MJSW=0.25 JS=6.2U TOX=65N NSUB=9.00E14 XJ=1U
+ LD=0.5U WD=0.5U UO=680 UCRIT=65000 UEXP=0.115
+ VMAX=5E4 DELTA=1)
*
*
.END
```

APPENDIX D SPICE LISTING DIGITAL-TO-ANALOG CONVERTER

```
SIMULATION COMPLETE DAC
*****
*****
* SUPPLY- REFERENCE- AND BULK VOLTAGES
*
VDD      20   0 DC    5V
VSS      29   0 DC   -5V
VBULK    30   0 DC   -5V
VREF     31   0 DC    2V
*
*****
*****
***** OPAMP CONNECTED AS BUFFER *****
*****
*****
* 1E STAGE
*
MA1       4   1   3 30 ENH W=36U L= 6U AS=432P AD=432P PS= 96U PD= 96U
MA2       5 27   3 30 ENH W=36U L= 6U AS=432P AD=432P PS= 96U PD= 96U
MA3        6   3   4 30 DEP W= 6U L= 6U AS= 72P AD= 72P PS= 36U PD= 36U
MA4        7   3   5 30 DEP W= 6U L= 6U AS= 72P AD= 72P PS= 36U PD= 36U
MA5       20   6   6 30 DEP W=12U L=26U AS=144P AD=144P PS= 48U PD= 48U
MA6       20   7   7 30 DEP W=12U L=26U AS=144P AD=144P PS= 48U PD= 48U
MA7        3   8 29 30 ENH W=21U L=19U AS=252P AD=252P PS= 66U PD= 66U
*
*****
*****
* LEVEL SHIFTER 1
*
MA8         6   6   9 30 ENH W=12U L=10U AS=144P AD=144P PS= 48U PD= 48U
MA9          9   9 10 30 ENH W=12U L=10U AS=144P AD=144P PS= 48U PD= 48U
MA10       10 10 11 30 ENH W=12U L=10U AS=144P AD=144P PS= 48U PD= 48U
MA11       11   8 29 30 ENH W=12U L=20U AS=144P AD=144P PS= 48U PD= 48U
*
*****
*****
* LEVEL SHIFTER 2
*
MA12        7   7 12 30 ENH W=12U L=10U AS=144P AD=144P PS= 48U PD= 48U
MA13       12 12 13 30 ENH W=12U L=10U AS=144P AD=144P PS= 48U PD= 48U
MA14       13 13 14 30 ENH W=12U L=10U AS=144P AD=144P PS= 48U PD= 48U
MA15       14   8 29 30 ENH W=12U L=20U AS=144P AD=144P PS= 48U PD= 48U
*
*****
*****
* 2E STAGE
*
MA16       17 11   8 30 ENH W=60U L= 6U AD=720P AS=720P PD=144U PS=144U
MA17       18 14   8 30 ENH W=60U L= 6U AD=720P AS=720P PD=144U PS=144U
MA18       15   8 17 30 DEP W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
MA19       16   8 18 30 DEP W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
MA20       20 15 15 30 DEP W= 6U L=24U AD= 72P AS= 72P PD= 36U PS= 36U
MA21       20 16 16 30 DEP W= 6U L=24U AD= 72P AS= 72P PD= 36U PS= 36U
MA22        8 19 29 30 ENH W=12U L=14U AD=144P AS=144P PD= 48U PS= 48U
*
*****
*****
```

```

*
* CM-FEEDBACK CIRCUIT
*
MA23 22 11 23 30 ENH W=31U L= 6U AD=372P AS=372P PD= 86U PS= 86U
MA24 22 14 23 30 ENH W=31U L= 6U AD=372P AS=372P PD= 86U PS= 86U
MA25 21 8 22 30 DEP W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
MA26 20 21 21 30 DEP W= 6U L=24U AD= 72P AS= 72P PD= 36U PS= 36U
MA27 23 19 29 30 ENH W= 6U L=12U AD= 72P AS= 72P PD= 36U PS= 36U
*
*****
*****
*
* LEVEL SHIFTER CM-FEEDBACK CIRCUIT
*
MA28 20 21 25 30 ENH W= 7U L=15U AD= 84P AS= 84P PD= 38U PS= 38U
MA29 25 25 19 30 ENH W= 7U L=15U AD= 84P AS= 84P PD= 38U PS= 38U
MA30 19 19 29 30 ENH W= 6U L=12U AD= 72P AS= 72P PD= 36U PS= 36U
**
*****
*****
*
* OUTPUT STAGE
*
MA31 20 15 27 30 DEP W=22U L= 8U AD=264P AS=264P PD= 68U PS= 78U
MA32 27 19 29 30 DEP W=17U L=10U AD=312P AS=312P PD= 76U PS= 76U
MA33 20 16 28 30 DEP W=22U L= 8U AD=264P AS=264P PD= 68U PS= 68U
MA34 28 19 29 30 DEP W=17U L=10U AD=312P AS=312P PD= 76U PS= 76U
*
*****
*****
*
* FREQUENCY COMPENSATION
*
CM1 11 27 0.7PF
CM2 14 28 0.7PF
*
*****
*****
*
* CAPACITIVE LOAD
*
CL 27 0 4PF
*
*
*****
*****
*****
*****
*****
*****
*****
*****
*
* CLOCK SIGNALS FROM 15-BIT SHIFT REGISTER
*
VCLK1 200 0 PULSE(-5V 5V 0NS 20NS 20NS 1480NS 3US)
VCLK2 201 0 PULSE( 5V -5V 0NS 20NS 20NS 1480NS 3US)
*
*****
*****
*
* LOGIC CIRCUITRY: NON-OVERLAPPING 2-PHASE CLOCK
*
.SUBCKT NOR 1 2 3 20 29 30
MC1 20 3 3 30 DEP W= 6U L=10U AD= 72P AS= 72P PD=36U PS=36U
MC2 3 1 29 30 ENH W=12U L= 6U AD=144P AS=144P PD=48U PS=48U
MC3 3 2 29 30 ENH W=12U L= 6U AD=144P AS=144P PD=48U PS=48U
.ENDS
*
MC4 29 203 203 30 DEP W= 6U L=10U AD= 72P AS= 72P PD=36U PS=36U
MC5 203 202 29 30 ENG W=12U L= 6U AD=144P AS=144P PD=48U PS=48U

```



```

*
X1 200 201 202 20 29 30 NOR
X2 202 105 104 20 29 30 NOR
X3 203 104 105 20 29 30 NOR
*
*****
*****
*
* CAPACITOR NETWORK
*
C0 106 109 1PF
C1 106 110 2PF
C2 106 111 4PF
C3 1 112 1PF
C4 1 113 2PF
C5 1 114 4PF
C6 1 115 8PF
C7 1 116 16PF
CCP 106 1 1.1710PF
CCM 106 0 1PF
*
*****
*****
*
* PARASITIC CAPACITORS
*
CPT1 106 30 0.1971PF
CPT2 1 30 0.3217PF
CP0B 109 30 0.1PF
CP1B 110 30 0.2PF
CP2B 111 30 0.4PF
CP3B 112 30 0.1PF
CP4B 113 30 0.2PF
CP5B 114 30 0.4PF
CP6B 115 30 0.8PF
CP7B 116 30 0.16PF
*
*****
*****
*
* RESISTORS AT NODE 106 AND 1: DC-PAD TO GROUND
*
R1 106 0 10G
R2 1 0 10G
*
*****
*****
*
* CAPACITOR SWITCHES
*
MD0G 109 117 0 30 ENH W= 6U L=6U AD= 72P AS= 72P PD=36U PS=36U
MD0R 109 118 133 30 ENH W=12U L=6U AD=144P AS=144P PD=48U PS=48U
MD1G 110 119 0 30 ENH W= 6U L=6U AD= 72P AS= 72P PD=36U PS=36U
MD1R 110 120 133 30 ENH W=12U L=6U AD=144P AS=144P PD=48U PS=48U
MD2G 111 121 0 30 ENH W= 6U L=6U AD= 72P AS= 72P PD=36U PS=36U
MD2R 111 122 133 30 ENH W=12U L=6U AD=144P AS=144P PD=48U PS=48U
MD3G 112 123 0 30 ENH W= 6U L=6U AD= 72P AS= 72P PD=36U PS=36U
MD3R 112 124 133 30 ENH W=12U L=6U AD=144P AS=144P PD=48U PS=48U
MD4G 113 125 0 30 ENH W= 6U L=6U AD= 72P AS= 72P PD=36U PS=36U
MD4R 113 126 133 30 ENH W=12U L=6U AD=144P AS=144P PD=48U PS=48U
MD5G 114 127 0 30 ENH W= 6U L=6U AD= 72P AS= 72P PD=36U PS=36U
MD5R 114 128 133 30 ENH W=12U L=6U AD=144P AS=144P PD=48U PS=48U
MD6G 115 129 0 30 ENH W= 6U L=6U AD= 72P AS= 72P PD=36U PS=36U
MD6R 115 130 133 30 ENH W=12U L=6U AD=144P AS=144P PD=48U PS=48U
MD7G 116 131 0 30 ENH W= 6U L=6U AD= 72P AS= 72P PD=36U PS=36U
MD7R 116 132 133 30 ENH W=12U L=6U AD=144P AS=144P PD=48U PS=48U
*
*****
*****
*

```

* CHARGE INITIATION TRANSISTOR

MD1 1 104 0 30 ENH W=12U L=6U AD=144P AS=144P PD=48U PS=48U

* CLOCK FEEDTHROUGH COMPENSATION TRANSISTOR

MD2 1 105 1 30 ENH W= 6U L=6U AD= 72P AS= 72P PD=36U PS=36U

* SWITCHES

MD3 134 105 0 30 ENH W=18U L=6U AD=216P AS=216P PD=60U PS=60U

MD4 134 104 31 30 ENH W=18U L=6U AD=216P AS=216P PD=60U PS=60U

MD5 135 104 0 30 ENH W=18U L=6U AD=216P AS=216P PD=60U PS=60U

MD6 135 105 31 30 ENH W=18U L=6U AD=216P AS=216P PD=60U PS=60U

MD7 133 136 134 30 ENH W=18U L=6U AD=216P AS=216P PD=60U PS=60U

MD8 133 137 135 30 ENH W=18U L=6U AD=216P AS=216P PD=60U PS=60U

* INPUT WORDS: +0 +128 +64 +32 +16 +8
 * -0 -128 -64 -32 -16 -8

VB0 118 0 DC -5V

VNB0 117 0 DC 5V

VB1 120 0 DC -5V

VNB1 119 0 DC 5V

VB2 122 0 DC -5V

VNB2 121 0 DC 5V

VB3 124 0 PULSE(-5V 5V 14980NS 20NS 20NS 2980NS 18US)

VNB3 123 0 PULSE(5V -5V 14980NS 20NS 20NS 2980NS 18US)

VB4 126 0 PULSE(-5V 5V 11980NS 20NS 20NS 2980NS 18US)

VNB4 125 0 PULSE(5V -5V 11980NS 20NS 20NS 2980NS 18US)

VB5 128 0 PULSE(-5V 5V 8980NS 20NS 20NS 2980NS 18US)

VNB5 127 0 PULSE(5V -5V 8980NS 20NS 20NS 2980NS 18US)

VB6 130 0 PULSE(-5V 5V 5980NS 20NS 20NS 2980NS 18US)

VNB6 129 0 PULSE(5V -5V 5980NS 20NS 20NS 2980NS 18US)

VB7 132 0 PULSE(-5V 5V 2980NS 20NS 20NS 2980NS 18US)

VNB7 131 0 PULSE(5V -5V 2980NS 20NS 20NS 2980NS 18US)

VBS 136 0 PULSE(-5V 5V 18US 20NS 20NS 17980NS 36US)

VNBS 137 0 PULSE(5V -5V 18US 20NS 20NS 17980NS 36US)

* SPICE ANALYSIS

.TRAN 50NS 36US

.NODESET V(3)=-1.05 V(4)= 0.20 V(5)= 0.20 V(6)= 1.95

+ V(7)= 1.95 V(8)=-3.50 V(9)= 0.32 V(10)=-1.21

+ V(11)=-2.65 V(12)= 0.32 V(13)=-1.21 V(14)=-2.65

+ V(15)= 1.80 V(16)= 1.80 V(17)=-2.01 V(18)=-2.01

+ V(19)=-3.35 V(21)= 0.57 V(22)=-2.09 V(23)=-3.52

+ V(25)=-1.44 V(27)= 0.00 V(28)= 0.00

.OPTIONS LIMPTS=5000 RELTOL=0.0001 ITL1=100 ITL2=50 ITL4=40

+ ITL5=0 ABSTOL=1PA VNTOL=1UV NUMDGT=7

.PROBE V(200) V(201) V(202) V(203) V(104) V(105) V(106) V(1) V(27)

+ V(109) V(110) V(111) V(112) V(113) V(114) V(115) V(116)

```
*
* TRANSISTOR MODEL PARAMETERS
*
*
.MODEL DEP NMOS (LEVEL=2 VTO=-2.5 PB=0.75 CGSO=370P CGDO=370P
+ CGBO=395P RSH=20 XQC=0.4 CJ=80U MJ=0.5 CJSW=330P
+ MJSW=0.25 JS=6.2U TOX=65N NSUB=1.66E15 XJ=1U
+ LD=0.5U WD=0.5U UO=600 UCRIT=65000 UEXP=0.115
+ VMAX=5E4 DELTA=1)
*
.MODEL ENH NMOS (LEVEL=2 VTO=0.55 PB=0.75 CGSO=370P CGDO=370P
+ CGBO=395P RSH=20 XQC=0.4 CJ=80U MJ=0.5 CJSW=330P
+ MJSW=0.25 JS=6.2U TOX=65N NSUB=9.00E14 XJ=1U
+ LD=0.5U WD=0.5U UO=680 UCRIT=65000 UEXP=0.115
+ VMAX=5E4 DELTA=1)
*
*
.END
```

APPENDIX E SPICE LISTING CONTROLLER CIRCUIT A

```

SIMULATION FOUR-FASE CLOCKCIRCUIT A
*****
*****
*
* SUPPLY- AND BULKVOLTAGES
*
VDD 60 0 DC 5V
VSS 50 0 DC -5V
VBULK 40 0 DC -5V
*
*****
*****
*
*          2-INPUT NOR
*
*          in1 in2 out Vdd Vss Bulk
*          |  |  |  |  |  |
.SUBCKT NOR 1 2 7 10 9 8
*
M1 10 10 6 8 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M2 6 5 5 8 DEP W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M3 10 5 7 8 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M4 5 1 9 8 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M5 7 1 9 8 ENH W=12U L= 6U AD=144P AS=144P PD= 48U PS= 48U
M6 5 2 9 8 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M7 7 2 9 8 ENH W=12U L= 6U AD=144P AS=144P PD= 48U PS= 48U
CB 6 7 0.1PF
*
.ENDS
*
*****
*****
*
*          TWO-FASE CLOCK
*
*          in out1 out2 Vdd Vss Bulk
*          |  |  |  |  |  |
.SUBCKT TFCLK 1 3 4 7 6 5
*
X1 1 4 3 7 6 5 NOR
X2 2 3 4 7 6 5 NOR
*
M1 7 2 2 5 DEP W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M2 2 1 6 5 ENH W=18U L= 6U AD=216P AS=216P PD= 60U PS= 60U
*
.ENDS
*
*****
*****
*
*          INVERTER
*
*          in out Vdd Vss Bulk
*          |  |  |  |  |
.SUBCKT INV 1 2 7 6 5
*
M1 7 7 3 5 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M2 7 4 2 5 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M3 3 4 4 5 DEP W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M4 4 1 6 5 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M5 2 1 6 5 ENH W=12U L= 6U AD=144P AS=144P PD= 48U PS= 48U
CB 3 2 0.1PF
*
.ENDS
*

```

```

*****
*****
*
*           3-INPUT POWNOR
*
*           in1 in2 in3 out Vdd Vss Bulk
*           |   |   |   |   |   |
.SUBCKT PWNOR      1   2   3   6   9   8   7
*
M1   9   9   4   7 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M2   9   5   6   7 ENH W=30U L= 6U AD=360P AS=360P PD= 84U PS= 84U
M3   4   5   5   7 DEP W=10U L= 6U AD=120P AS=120P PD= 44U PS= 44U
M4   5   1   8   7 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M5   5   2   8   7 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M6   5   3   8   7 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M7   6   1   8   7 ENH W=30U L= 6U AD=360P AS=360P PD= 84U PS= 84U
M8   6   2   8   7 ENH W=30U L= 6U AD=360P AS=360P PD= 84U PS= 84U
M9   6   3   8   7 ENH W=30U L= 6U AD=360P AS=360P PD= 84U PS= 84U
CB   4   6   0.3PF
*
.ENDS
*
*****
*****
*
* CAPACITIVE LOAD
*
* load capacitors 2MHz four phase clock
*
CL1  10   0   2.0PF
CL2  11   0   2.0PF
CL3  12   0   2.0PF
CL4  13   0   2.0PF
*
* load capacitors repeater
*
CL5  14   0   200FF
CL6  15   0   200FF
*
*
*****
*****
*
* CLOCK CIRCUIT A
*
* 4 MHz two phase clock
*
X1   1   2   3 60 50 40 TFCLK
*
* 2 MHz four phase clock
*
X2   9   5 60 50 40 INV
X3   6   7 60 50 40 INV
X4   8   9 60 50 40 INV
*
X5   7   9 13 10 60 50 40 PWNOR
X6   7   8 10 11 60 50 40 PWNOR
X7   6   8 11 12 60 50 40 PWNOR
X8   6   9 12 13 60 50 40 PWNOR
*
MSC1  5   3   6 40 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
MSC2  7   2   8 40 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
*
* repeater
*
X9   6 15 14 60 50 40 NOR
X10  7 14 15 60 50 49 NOR
*

```

```

* reset switch
*
MR1 58 4 8 40 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
*
* MASTER CLOCK
*
VCLK1 1 0 PULSE(5V -5V 115NS 10NS 10NS 115NS 250NS)
*
VRESET 4 0 PWL(0NS 5V 40NS 5V 50NS -5V 1250NS -5V)
*
*****
*****
*
* SPICE ANALYSIS
*
*
.TRAN 2NS 1250NS
.OPTIONS LIMPTS=5000 RELTOL=0.0001 ITL1=100 ITL2=50 ITL4=40
+ ITL5=0 ABSTOL=1PA VNTOL=1UV NUMDGT=7
.PROBE V( 1) V( 2) V( 3) V( 4) V( 5) V( 6) V( 7) V( 8) V( 9)
+ V(10) V(11) V(12) V(13) V(14) V(15)
*
*****
*****
*
* TRANSISTOR MODEL PARAMETERS
*
.MODEL DEP NMOS(LEVEL=2 VTO=-2.5 PB=0.75 CGSO=370P CGDO=370P CGBO=395P
+ RSH=20 XQC=0.4 CJ=80U MJ=0.5 CJSW=330P MJSW=0.25 JS=6.2U
+ TOX=65N NSUB=1.66E15 XJ=1U LD=0.5U WD=0.5U UO=600
+ UCRIT=65000 UEXP=0.115 VMAX=5E4 DELTA=1)
*
*
.MODEL ENH NMOS(LEVEL=2 VTO=0.55 PB=0.75 CGSO=370P CGDO=370P CGBO=395P
+ RSH=20 XQC=0.4 CJ=80U MJ=0.5 CJSW=330P MJSW=0.25 JS=6.2U
+ TOX=65N NSUB=9.00E14 XJ=1U LD=0.5U WD=0.5U UO=680
+ UCRIT=65000 UEXP=0.115 VMAX=5E4 DELTA=1)
*
.END

```

APPENDIX F SPICE LISTING CONTROLLER CIRCUIT B

```

SIMULATION FOUR-FASE CLOCKCIRCUIT B
*****
*****
*
* SUPPLY- AND BULKVOLTAGES
*
VDD 60 0 DC 5V
VSS 50 0 DC -5V
VBULK 40 0 DC -5V
*
*****
*****
*
*          INVERTER
*
*          in out Vdd Vss Bulk
*          |  |   |   |   |
.SUBCKT INV 1 2 5 4 3
*
M1 5 2 2 3 DEP W= 6U L=10U AD= 72P AS= 72P PD= 36U PS= 36U
M2 2 1 4 3 ENH W=12U L= 6U AD=144P AS=144P PD= 48U PS= 48U
*
.ENDS
*
*****
*****
*
*          POWER INVERTER
*
*          in out Vdd Vss Bulk
*          |  |   |   |   |
.SUBCKT PWINV 1 2 7 6 5
*
M1 7 7 3 5 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M2 7 4 2 5 ENH W=30U L= 6U AD=360P AS=360P PD= 84U PS= 84U
M3 3 4 4 5 DEP W=10U L= 6U AD=120P AS=120P PD= 44U PS= 44U
M4 4 1 6 5 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M5 2 1 6 5 ENH W=30U L= 6U AD=360P AS=360P PD= 84U PS= 84U
CB 3 2 0.1PF
*
.ENDS
*
*****
*****
*
*          3-INPUT POWERNOR
*
*          in1 in2 in3 out Vdd Vss Bulk
*          |  |   |   |   |   |   |
.SUBCKT PWNOR 1 2 3 6 9 8 7
*
M1 9 9 4 7 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M2 9 5 6 7 ENH W=30U L= 6U AD=360P AS=360P PD= 84U PS= 84U
M3 4 5 5 7 DEP W=10U L= 6U AD=120P AS=120P PD= 44U PS= 44U
M4 5 1 8 7 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M5 5 2 8 7 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M6 5 3 8 7 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
M7 6 1 8 7 ENH W=30U L= 6U AD=360P AS=360P PD= 84U PS= 84U
M8 6 2 8 7 ENH W=30U L= 6U AD=360P AS=360P PD= 84U PS= 84U
M9 6 3 8 7 ENH W=30U L= 6U AD=360P AS=360P PD= 84U PS= 84U
CB 4 6 0.3PF
*
.ENDS
*

```

```

*****
*****
*
* CAPACITIVE LOAD
*
* load capacitors 2MHz four phase clock
*
CL1  8  0  2.0PF
CL2  9  0  2.0PF
CL3 10  0  2.0PF
CL4 11  0  2.0PF
*
* load capacitors 2-bit shift register
*
CL5 24  0  2.0PF
CL6 25  0  2.0PF
CL7 26  0  2.0PF
CL8 27  0  2.0PF
*
*****
*****
*
*          CLOCK CIRCUIT B
*
* 1 MHZ FOUR PHASE CLOCK
*
X1   7  3 60 50 40 INV
X2   4  5 60 50 40 INV
X3   6  7 60 50 40 INV
*
X4   5  7 11  8 60 50 40 PWNOR
X5   5  6  8  9 60 50 40 PWNOR
X6   4  6  9 10 60 50 40 PWNOR
X7   4  7 10 11 60 50 40 PWNOR
*
MSC1  3  1  4 40 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
MSC2  5  2  6 40 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
*
MR1   60 30  6 40 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
*
* TWO SHIFT CELL'S
*
X8   12 13 60 50 40 INV
X9   15 16 60 50 40 INV
X10  18 19 60 50 40 INV
X11  21 22 60 50 40 INV
*
X12  12 24 60 50 40 PWINV
X13  13 25 60 50 40 PWINV
X14  15 26 60 50 40 PWINV
X15  16 27 60 50 40 PWINV
*
* Current Limiting transistors
*
MCL1 13 14 14 40 DEP W= 6U L=10U AD= 72P AS= 72P PD= 36U PS= 36U
MCL2 16 17 17 40 DEP W= 6U L=10U AD= 72P AS= 72P PD= 36U PS= 36U
MCL3 19 20 20 40 DEP W= 6U L=10U AD= 72P AS= 72P PD= 36U PS= 36U
MCL4 22 23 23 40 DEP W= 6U L=10U AD= 72P AS= 72P PD= 36U PS= 36U
*
* Shift Control switches
*
MSC3 14  8 15 40 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
MSC4 17 10 18 40 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
MSC5 20  8 21 40 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
MSC6 23 10 12 40 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
*

```


* Reset switches

```

*
MR2  60 30 15 40 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
MR3  60 30 18 40 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
MR4  50 30 21 40 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
MR5  50 30 12 40 ENH W= 6U L= 6U AD= 72P AS= 72P PD= 36U PS= 36U
*

```

* CLOCK SIGNALS FROM REPEATER OUTPUT

```

*
VCLK   1  0 PULSE( 5V -5V 180NS 40NS 40NS 240NS 500NS)
VNCLK  2  0 PULSE(-5V  5V 240NS 40NS 40NS 180NS 500NS)
*

```

VRESET 30 0 PWL(0NS 5V 40NS 5V 50NS -5V 4US -5V)

```

*****
*****

```

* SPICE ANALYSIS

```

*
.TRAN      25NS 4US
.OPTIONS LIMPTS=5000 RELTOL=0.0001 ITL1=100 ITL2=50 ITL4=40
+          ITL5=0 ABSTOL=1PA VNTOL=1UV NUMDGT=7
.PROBE     V( 1) V( 2) V( 8) V( 9) V(10) V(11) V(12) V(13) V(15)
+          V(16) V(18) V(19) V(21) V(22) V(24) V(25) V(26) V(27)
+          V(30)
*

```

```

*****
*****

```

* TRANSISTOR MODEL PARAMETERS

```

*
.MODEL DEP NMOS(LEVEL=2 VTO=-2.5 PB=0.75 CGSO=370P CGDO=370P CGBO=395P
+          RSH=20 XQC=0.4 CJ=80U MJ=0.5 CJSW=330P MJSW=0.25 JS=6.2U
+          TOX=65N NSUB=1.66E15 XJ=1U LD=0.5U WD=0.5U UO=600
+          UCRIT=65000 UEXP=0.115 VMAX=5E4 DELTA=1)
*

```

```

*
.MODEL ENH NMOS(LEVEL=2 VTO=0.55 PB=0.75 CGSO=370P CGDO=370P CGBO=395P
+          RSH=20 XQC=0.4 CJ=80U MJ=0.5 CJSW=330P MJSW=0.25 JS=6.2U
+          TOX=65N NSUB=9.00E14 XJ=1U LD=0.5U WD=0.5U UO=680
+          UCRIT=65000 UEXP=0.115 VMAX=5E4 DELTA=1)
*

```

.END